AN ON-LINE COMPUTER ASSISTED MASS SPECTROMETER

by

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ABSTRACT

An analog data acquisition system incorporating an Interdata Model 4 digital computer has been designed and built for a mass spectrometer. This system has been conceived with the primary objectives of improving analytical precision and production. Automated mass spectrometer operation allows for the collection of larger quantities of data while decreasing operator involvement and consequently diminishing operator bias and fatigue.

The analog signal from the mass spectrometer measuring system is digitized using a digital voltmeter and transmitted, via an interface, to the processor where the digital information is manipulated in accordance with a computer program. An additional facility is provided whereby digital data from the processor can be displayed, if desired, on a 5 decade numerical readout situated at the mass spectrometer console. Hardware is also available in the interface to provide control of the magnetic field scan rate. A function control switch at the mass spectrometer console allows the operator to convey a variety of predetermined instructions to the computer at any time during the course of a run. Thus, the system provides for on-line (real time) data processing of mass spectra as well as limited computer control over the mass spectrometer.

This thesis is primarily concerned with the design and construction of the logic hardware for this system together with a demonstration of its operating ability.

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CHAPTER 1

INTRODUCTION

1.1 General Background

During the past few years a number of important advances have been made in the field of isotope geophysics. New analytical techniques, such as the double spiking procedures of Compston and Oversby (1969) and the triple-filament technique for lead (Catanzaro, 1967), benefit from a high order of precision in mass spectrometer analysis. In order to do full justice to these improved analytical techniques it is necessary to increase the measurement precision of mass spectrometer ion-currents. One way in which this can be achieved is by means of digital data collection and analysis procedures. Using an on-line digital computer, Wasserburg and his associates at the California Institute of Technology have demonstrated the value of these procedures by achieving results of outstanding precision on analyses of strontium (Papanastassiou and Wasserburg, 1969) and gadolinium (Albee et al, 1970).

At the University of British Columbia, research of digital data collection systems commenced in 1963, using a gas-source mass spectrometer. A servo-voltmeter ion-current amplifier (Stacey et al, 1965) was utilized which had, as a primary output, the shaft rotation of a motor-driven potentiometer. Thus analog —to-digital conversion was easily achieved using a shaft position encoder (Weichert et al, 1967). Digital data was initially stored on punched paper tape but, as the system was developed, the paper tape punch was replaced by an incremental magnetic tape recorder. In both cases, the data was processed using the facilities of the University's Computing Centre which presently include a duplex IBM 360/67 computer.

To maintain completely independent data acquisition systems for the three mass spectrometers operated by the Department would have required the purchase of two more tape recorders, and the construction of suitable interfaces. A small digital computer was therefore purchased in 1969 and work began on the design of a suitable digital logic interface to a mass spectometer. The on-line data acquisition system that was subsequently built is capable of immediately and simultaneously supervising the operation and processing the data from the three mass spectrometers, which are used at different times for isotopic analysis of Pb, Th, U, Rb, Sr, Gd, Eu and Sm.

The system description presented in this thesis is intended as an example of what is possible and no claim is made that the design is optimum in any sense.

1.2 Design Objectives

The system was conceived with three main objectives in mind:

1. A decrease in the overall time required to process the data from the mass spectrometer.
2. A reduction in operator involvement and hence a reduction of operator bias and operator strain.
3. An increase in analytical precision.

These objectives have been realized by using an on-line digital computer interfaced to the mass spectrometer. The computer should be able to filter the incoming digital data in real time and display the filtered data points at the mass spectrometer console for the operator's convenience. In addition, it should be possible to reduce the mass spectra from the input data and display the results at his request. The computing system should have the capability of automatically adjusting the operating conditions of the mass spectrometer. The system built has the facility for controlling the magnetic scan rate but additional control features may be added at a later time.

The writer's research was primarily concerned with the design and construction of the necessary digital electronics for the interface together with a demonstration of its operating ability.

A simplified block diagram of the computer to mass spectrometer interface is shown in Figure 1.

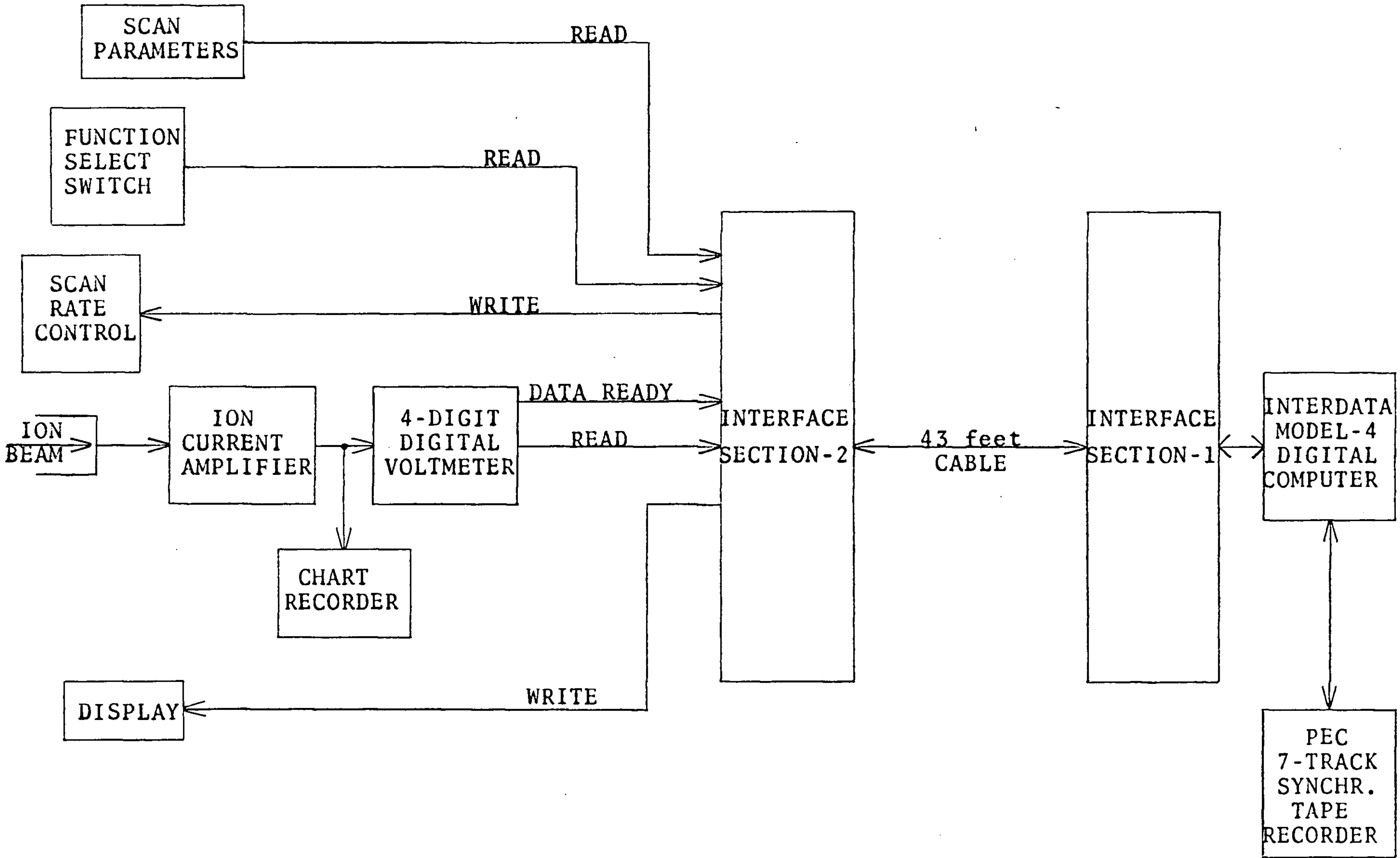


FIGURE 1. COMPUTER TO MASS SPECTROMETER INTERFACE

CHAPTER 2

GENERAL DESCRIPTION

2.1 The Mass Spectrometer

The mass spectrometer used in this research project was designed principally by R. D. Russell in cooperation with F. Kollar, J. S. Stacey and T. J. Ulrych, and was brought to its present state of operating efficiency by J. Blenkinsop. It is a 90-degree sector, 30 cm radius, solid source machine, with single order focussing and a variable magnetic field scan. In the past and at present this machine has been used for rubidium-strontium analyses but it is in no way limited to these elements.

The analog section of the mass spectrometer measuring system incorporates a hybrid amplifier using an electrometer vacuum tube and integrated circuit components. The voltage output from this amplifier can be attenuated by factors of 1, 1/3, 1/9, 1/27, 1/81 using a shunt switching network. The schematic circuits for the ion current amplifier and output attenuator, both designed by R. D. Russell, can be found in Appendix I.

The analog output of the measuring system, which is generally of the order of one volt for most isotope peaks, is fed to a digital voltmeter which displays the input voltages and also functions as an analog -to-digital converter for the computer interface.

2.2 The Computer

An Interdata Model 4 computer was chosen chiefly because of its versatility at a reasonable cost. In addition, it uses a halfword length of 16 bits and a programming language that is similar to the University of B.C. IBM 360/67 computer with which it can be easily interfaced if required. The 8k 8-bit bytes of memory supplied with the Model 4 Processor are marginally adequate for sophisticated mass spectrometer control and data reduction programs, however additional memory modules may be added, up to a maximum of 65k bytes, at any time.

A Teletype Model ASR33 and Peripheral Equipment Corporation PEC 3520-72 synchronous tape transport were purchased with the Model 4 Processor (see Table I). The teletype was supplied ready interfaced to the computer and the tape transport was interfaced in our laboratory by R. D. Meldrum using logic circuitry of his own design.

Figure 2 shows the complete analog data acquisition system for one mass spectrometer. The processor can communicate with the teletype and mass spectrometer via a multiplexor channel which has the capacity to handle a total of 256 devices. Each peripheral device is connected via a device controller to the multiplexor bus, it is this controller that provides the interface between the computer and an external device. The only essential requirement of the device is that it can supply data to the device controller in an acceptable digital format. In

TABLE I DATA PROCESSING EQUIPMENT PURCHASED

ITEM	MODEL NUMBER	MANUFACTURER	APPROXIMATE COST (1969)
PROCESSOR	4	INTERDATA INC.,	$7,800 *
8,192 BYTE MEMORY		INTERDATA INC.,	$6,000 *
SELECTOR CHANNEL		INTERDATA INC.,	$2,900 *
HIGH SPEED ARITHMETIC & INPUT/OUTPUT		INTERDATA INC.,	$1,500 *
TYPEWRITER & PAPER TAPE READER/PUNCH	ASR33	TELETYPE CORPORATION	$1,900
MAGNETIC TAPE TRANSPORT	PEC 3520-72	PERIPHERAL EQUIPMENT CORPORATION	$4,000
DIGITAL VOLTMETER	DT-344-2	DATA TECHNOLOGY CORPORATION	$ 500
NUMERICAL DISPLAY	DS-103-5	DISPLAY GENERAL INCORPORATED	$ 300
POWER SUPPLY	PS-200	DISPLAY GENERAL INCORPORATED	$ 60

* - 1971 PRICES ARE ABOUT 40% LOWER THAN 1969 PRICES

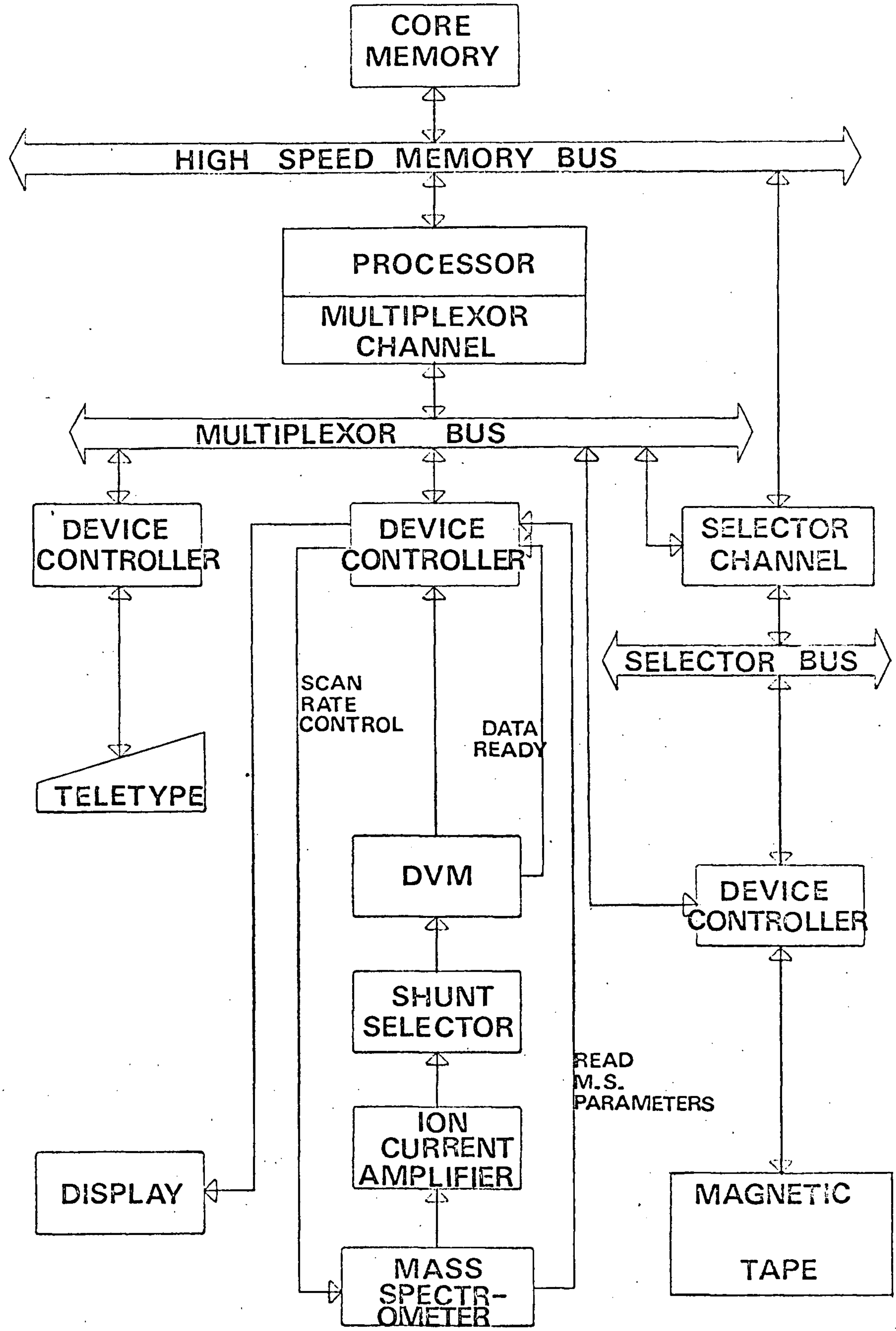


Figure 2. Analog Data Acquisition System Block Diagram

the case of the mass spectrometer this is achieved by using the binary-coded-decimal (BCD) outputs of a digital voltmeter.

Figure 3 shows the 27 lines that constitute the multiplexor bus; 16 lines are reserved for data input and output which is matched to the 8-bit byte. The 8 control lines, with one exception, are used to enable data onto the data lines. The control designated ACKO, together with the attention line (ATNO) and the system clear line (SCLRO), are associated with the processor interrupt facility which is an optional feature of every device controller. The synchronize line (SYNO) is used to notify the processor when a signal on one of the control lines is accepted by a device controller.

A typical sequence of operations to service the mass spectrometer over the multiplexor channel would be:

1. A pulse from the digital voltmeter, signifying that data is available at the mass spectrometer, causes a signal to be sent along the attention line (ATNO) which interrupts the processor. The processor acknowledges the interrupt and sends a signal over the ACKO line which initiates a hardware scan cycle to determine which device caused the ATNO signal. The mass spectrometer automatically returns its device number to the processor over the data request lines (DRL's). The processor is now ready to service the mass spectrometer.

2. The mass spectrometer is addressed by the processor over the 8 data available lines (DAL's). This address appears on the bus to all device controllers.

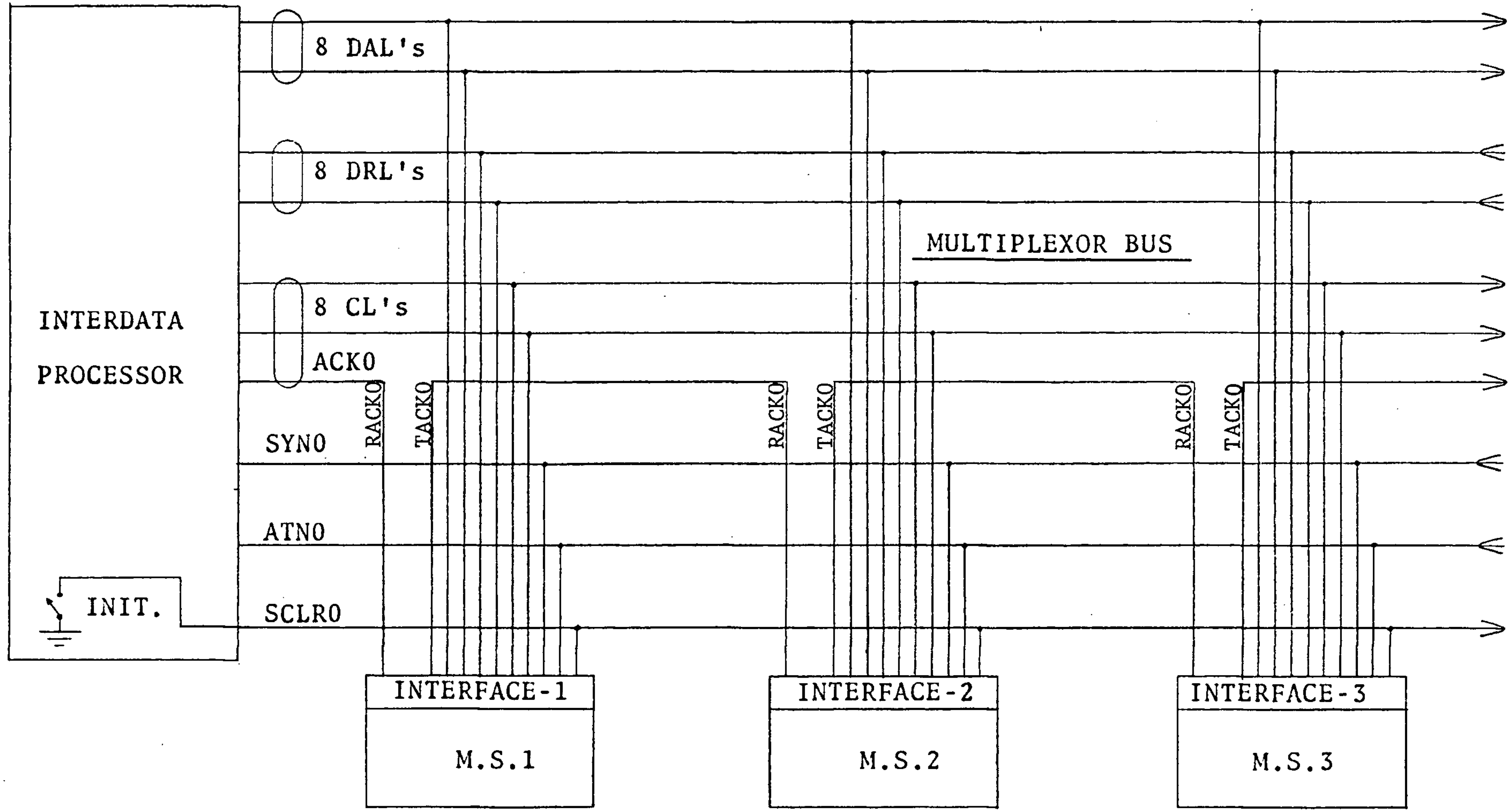


FIGURE 3. THE MULTIPLEXOR CHANNEL

3. The processor then activates the address control line which signifies that the DAL's now provide an address (as opposed to data).

4. The mass spectrometer interface decodes its address, sets a flip-flop memory, and sends a signal back to the processor along the SYNO line. The mass spectrometer remains addressed until another device controller is addressed or until a system clear signal (SCLRO) is received.

5. The processor places an "output command" on the DAL's.

6. The processor then activates the command control line; this causes the data from (for instance) one particular decade of the digital voltmeter, specified by the output command, to be made available. A SYNO signal is sent back to the processor to indicate the command has been stored in the device controller.

7. The mass spectrometer is again addressed by the processor, as described in steps 2, 3 and 4.

8. The processor then activates the data request (DR) control line which enables the byte of data, made available in step 6, from the digital voltmeter to the processor, along the DRL's. A synchronize signal (SYNO) is generated to indicate that the data has arrived at the processor.

2.3 Programming the Interdata Model 4

The Interdata Model 4 computer possesses a repertoire of 75 basic instructions which can manipulate data between core memory, 16 general registers, and up to 256 external devices. In addition, the Interdata system also provides for the direct transfer of a block of data between core memory and a peripheral device under control of an optional selector channel. Once initiated by the processor, this direct transfer takes place invisibly without interruption to normal processing.

Data of three different word lengths; the 8-bit byte, 16-bit halfword, and 32-bit fullword, can be manipulated by the instruction set. In the Interdata system hexadecimal notation (base 16) is used to express binary information, so that, for example, a byte of data can be represented by two hexadecimal digits.

Three instruction formats are available in the Interdata system: register to register (RR), register to indexed memory (RX), and register to storage (RS). A total of sixteen 16-bit general registers, numbered 0 to F in hexadecimal notation, function as accumulators or index registers in arithmetic and logical operations. In all three instruction formats, bits 0-7 specify the machine operation to be performed (th 8-bit OP code); bits 8-11 specify the address of the first operand, which is normally a general register. In the RR format the address of the second operand is specified by bits 12-15 and is always a general register. In the RX instruction formats, bits 12-15 always specify the address of a general register whose content is used as an index value. The remaining 16 bits (bits 16-31) specify a memory address in the RX format, and, in the case of the RS format, an integer value for use as an immediate operand.

A summary of the Interdata Model 4 programming instructions is given in Appendix III.

The information necessary for program execution is contained in the 32-bit program status word (PSW). Bits 0-11 of the PSW define the status of the current user program; bits 12-15 constitute the 4-bit condition code (CC) which is set after execution of input/output, logical, shift or arithmetic instructions. The memory address of the next instruction to be executed is specified by the 16-bit instruction address field (bits 16-31 of the PSW).

In instances of machine malfunctions, divide faults, illegal instructions, and external device service requests, system interrupts are generated. When an interrupt is recognised, the current PSW, which defines the present operating status of the processor, is placed in a reserved storage area (the old PSW) and a new PSW re-defines the status of the machine. On completion of the interrupt service sub-program the previous machine status, stored in the old PSW, is restored.

Input/output data transfer in the Interdata system can be either program controlled or interrupt controlled. The former method interrogates the device to ascertain if it is ready to transfer data, and waits if necessary until transfer can occur. The interrupt method allows the device to demand service when it is ready for the transfer of data. This latter method is the one employed for the mass spectrometer interface.

CHAPTER 3

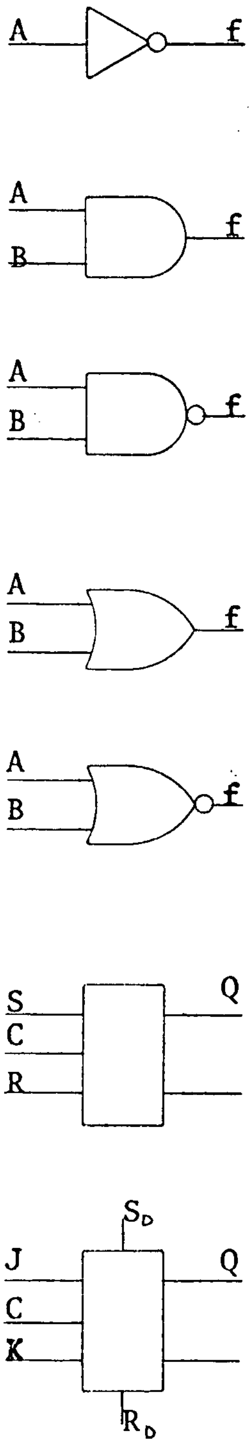
THE INTERFACE HARDWARE DESIGN

3.1 Introduction

The construction of a successful computer interface involves the design of suitable logic circuitry which will enable the computer to communicate with the particular peripheral device.

The hardware design is evolved using the standard logic elements available, namely gates, inverters and flip-flops. Figure 4 summarises the most commonly used logic elements together with their respective truth tables. In general, gates are used to direct the signals to and from the computer and flip-flops are used to store information, acting as one-bit memories.

Logic circuit design is in general easier than most analog circuit designs because only two voltage levels are employed, and the only major concern is the duration and timing of these voltage signals. There are two classes of signal, the steady voltage level and the pulse, the latter having a duration of a few tens of nanoseconds (typically). The timing of both types of signal are controlled by the processor and the peripheral device.



TRUTH TABLES

INVERTER (1/6 MC834P)

A	B	f
0		1
1		0

AND GATE (1/4 MC1806P)

A	B	f
0	0	0
0	1	0
1	0	0
1	1	1

NAND GATE (1/4 MC849P)

A	B	f
0	0	1
0	1	1
1	0	1
1	1	0

OR GATE (1/4 MC1809P)

A	B	f
0	0	0
0	1	1
1	0	1
1	1	1

NOR GATE

A	B	f
0	0	1
0	1	0
1	0	0
1	1	0

CLOCKED FLIP-FLOP (MC845P)

S_n	R_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	?

J-K FLIP-FLOP (1/2 MC855P)

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

FIGURE 4. BASIC LOGIC FUNCTIONS & TRUTH TABLES

Once the interface logic circuitry has been designed, by suitably matching the computer and peripheral device specifications to perform the required functions, it is then only necessary to select appropriate integrated circuit logic packages (chips) to perform the required task consistently.

When choosing logic packages there is normally a choice between five different logic families namely, resistor-transistor logic (RTL), diode-transistor logic (DTL), transistor-transistor logic (TTL), high-threshold logic (HTL), and emitter-coupled logic (ECL); Table II compares the 2-input NAND function for the five logic families. ECL is a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, it is used where extremely high speed operation is required. HTL was developed for applications such as in industry requiring a higher degree of inherent electrical noise immunity than is available with the more standard integrated circuit logic families. Disadvantages of HTL are a relatively high supply voltage (15±1 volts) and slow speed. TTL is a medium speed, high noise-immunity family of saturating integrated logic circuits, it is presently the most commonly employed logic family. DTL offers moderate speed and good noise immunity, it is somewhat inferior to TTL and used to be less expensive. RTL is slow, has poor noise immunity and a large power dissipation, it is no longer used commercially in high quality digital electronics.

TABLE II SPECIFICATIONS OF QUAD 2-INPUT NAND FUNCTION FOR THE FIVE LOGIC FAMILIES

LOGIC FAMILY	TYPICAL MOTOROLA NUMBER	SUPPLY VOLTAGE VOLTS	OUTPUT LOADING FACTOR	RELATIVE NOISE IMMUNITY	PROPAGATION DELAY ns TYPICAL	TOTAL POWER DISSIPATION mW TYPICAL/PKG.	APPROX. COST/ PKG.
RTL	MC9714P	+3±.3	5	WORST	55	145	$1.55
DTL	MC849P	+5±1/2	7	MODERATE	25	66	$1.65
TTL	MC7400P	+5±1/2	10	GOOD	13	40	$1.29
HTL	MC672P	+15±1	10	BEST	110	114	$1.40
ECL	MC1048P	-5.2±1/2	25	BAD	5	130	$3.90

Diode-transistor logic was chosen for the mass spectrometer interface because its specifications are more than adequate for the relatively slow speeds involved and because, at the time of purchase, it was slightly less expensive than the equivalent transistor - transistor logic, it is also the logic family most used in the Interdata Model 4 Processor. Where a particular logic function was not available in DTL then the appropriate TTL function was employed.

An aggravating problem often encountered with digital logic circuitry is electrical noise pickup, either, from adjacent lines running in close proximity (interline crosstalk) or, from other sources. The best way of eliminating it is to use high-threshold logic (HTL) which operates at a 7.5 volt threshold level. This logic family is somewhat inconvenient to use, unfortunately, since a separate 15 volt regulated power supply is required together with HTL/DTL level converters on all lines to and from the interface. In addition, HTL is about five times slower than DTL. Using diode-transistor logic, with careful circuit design, it is generally possible to keep noise pickup at a negligible level. Where a circuit element is required to drive a long line, for instance between the processor and a peripheral device, a power gate and appropriate pull-up resistor are always used. This helps to provide good noise immunity, primarily by lowering the impedance level of the lines. In addition, all long lines are made false-active, i.e., a line is active when it is at ground potential (zero volts), to further reduce the possibility of noise pickup.

The following pages describe the logic circuitry in some detail. It has been found convenient, for circuit description, to divide the interface into five sections, namely, device addressing, data and status input, data and command output, interrupt control, and read/write sequencing circuitry.

3.2 Device Addressing

The Interdata device addressing logic diagram is shown in Figure 5.

The mass spectrometer address (hexadecimal D) is wired into the device number selection board. When this address appears on the data available lines (DAL00 through DAL07) the decoded device output (DDO) goes low. A signal on the address control line (ADRS0), in conjunction with DDO, sets the address flip-flop so that its output (DENB1) is made high. During the presence of ADRS1, a synchronize signal is returned to the processor via the address synchronize line (ADSY0). A delay of about 200 nanoseconds is produced by capacitor C1 on the synchronize line (SYN0). This prevents the processor from lowering the ADRS0 line before the address flip-flop has been set. The device enable line (DENB1) gates all other input/output control lines to the interface.

When the address of another device appears on the data available lines, DD1 goes low, causing ADRS1 to reset the address

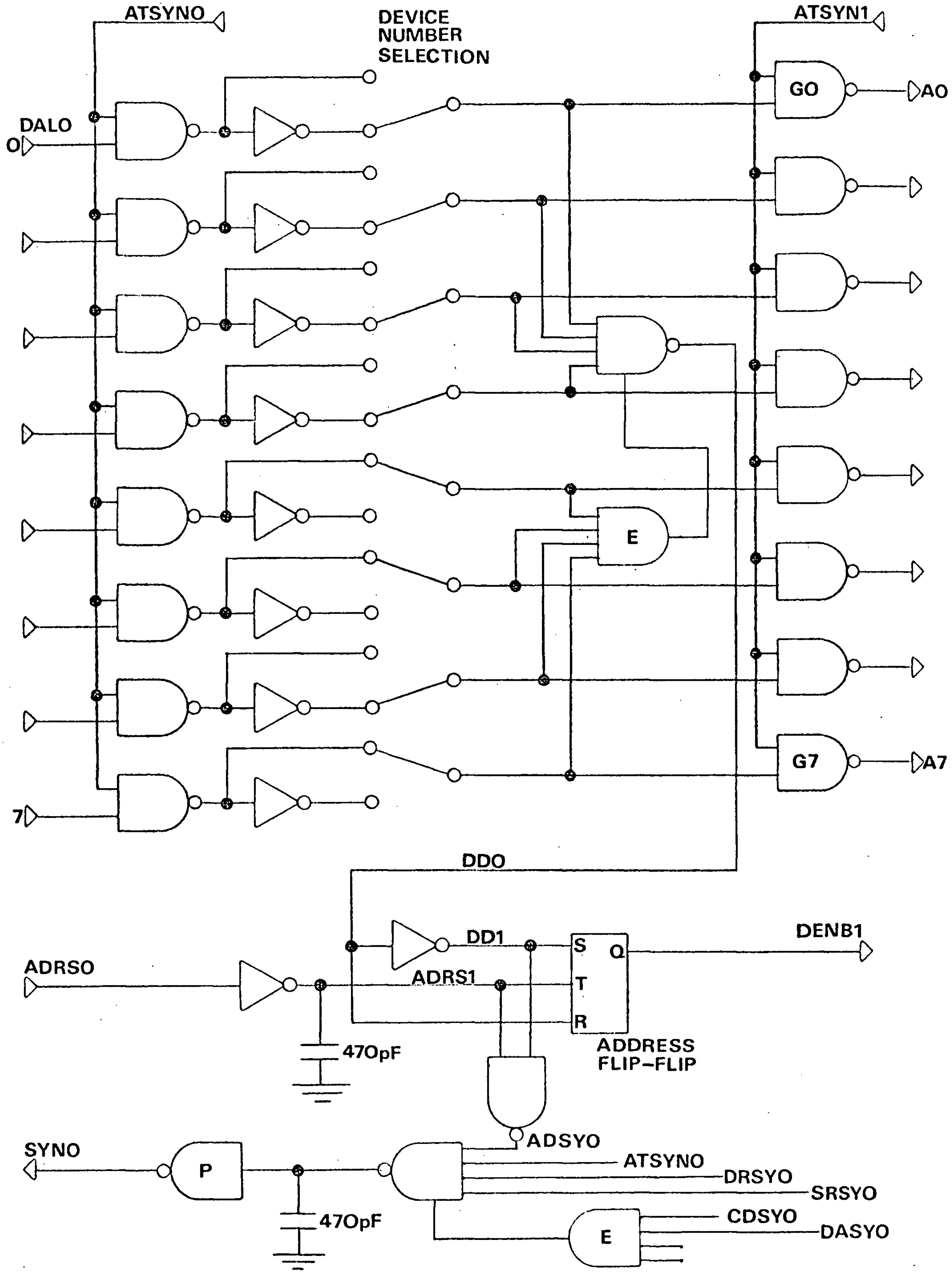


Figure 5. Device Addressing, Logic Diagram

flip-flop, and disable the mass spectrometer interface.

The eight NAND gates, G0 through G7, together with the lines ATSYN0 and ATSYN1, are part of the interrupt control circuitry described in section 3.5

3.3 Data and Status Input

Figure 6 shows the Interdata input gating logic diagrams.

When the mass spectrometer is addressed, DENB1 is high, enabling the data request (DRO) or status request (SRO) control line. The data or status byte is thus enabled onto the data request lines (DRL00 through DRL07). A return synchronize signal, DRSYO or SRSYO, is automatically generated when either of the control lines is enabled.

The lines A0 through A7 connect to the eight gates, G0 through G7, shown in Figure 5 and form part of the interrupt controller described in section 3.5.

3.4 Data and Command Output

The circuit shown in Figure 7 is used to control the flow of data and commands from the processor.

When the mass spectrometer is addressed, DENB1 is high, enabling the data available (DAO) or command (CMDO) control line. DAO or CMDO, in turn, enable the data or command byte onto the data available lines (DALOP0 through DALOP7). In addition, control pulses are sent to the read/write logic (Figure 9)

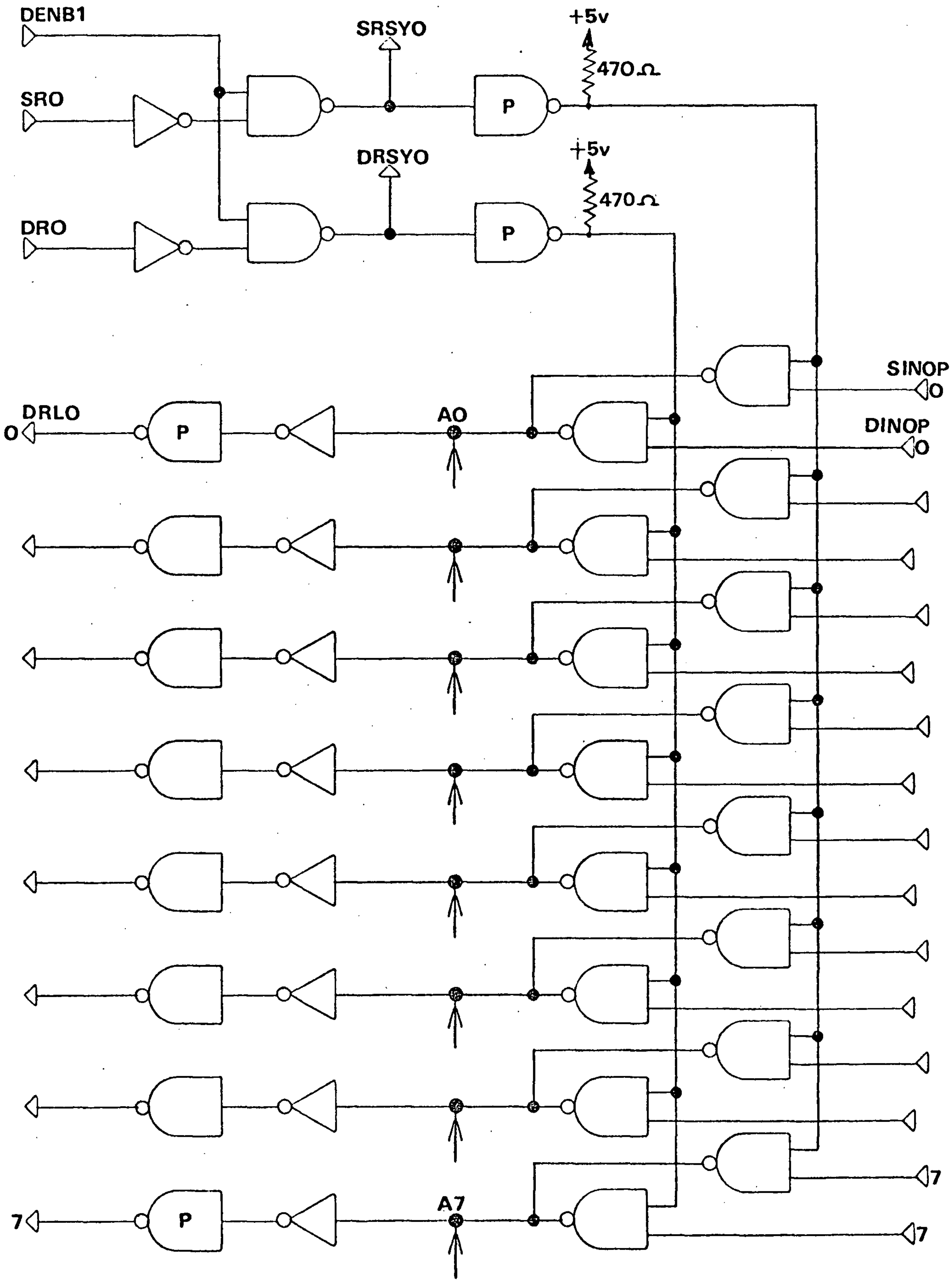


Figure 6. Data and Status Input, Logic Diagram

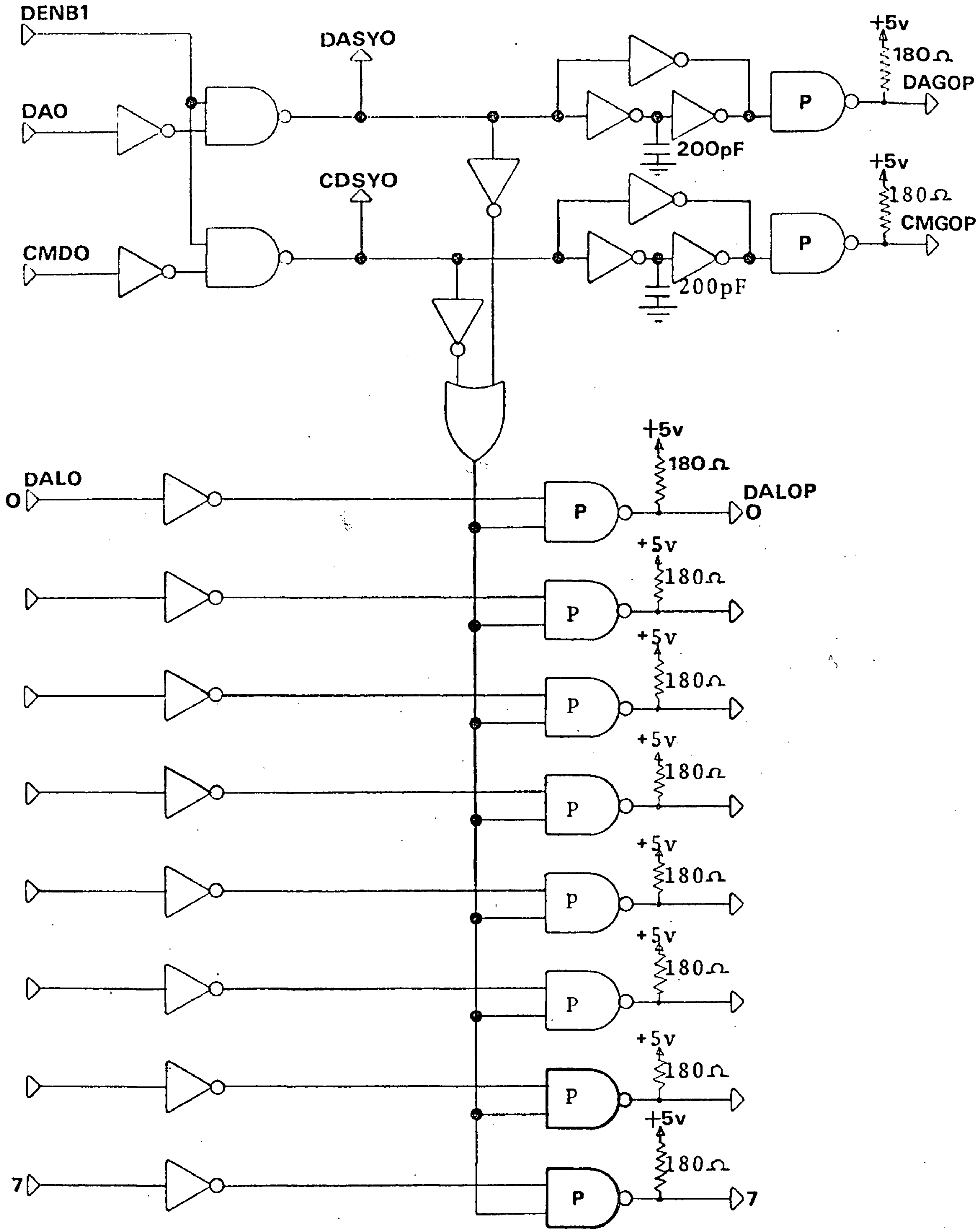


Figure7. Data and Command Output, Logic Diagram

via the DAGOP or CMGOP line. The duration of these pulses is shortened, from about 800 ns to about 400 ns, by the use of a one-shot multivibrator in each line; this ensures that the control pulses are removed before the data disappears from the DALOP lines. The lines DASYO and CDSYO return the respective synchronize signals to the processor.

The data available and command control lines are OR ed so that there cannot be any data or commands on the DALOP lines except when one of the two control lines is active. Thus this OR gate eliminates extraneous noise on the data transmission cable, an advantage when several interface cables are run in close proximity.

3.5 Interrupt Control

The logic circuit for the Interdata interrupt controller is shown in Figure 8.

The detailed operation of this circuit is described in the Interdata "Systems Interface Manual" and only a brief explanation will be given here.

The enable/disable switch is set in the enable position to activate the interrupt controller. When a byte of data is available at the digital voltmeter a data ready pulse is generated which causes the queue flip-flop to be direct set. The output from the queue flop-flop sends an attention signal (ATNO) to the processor via G12. The processor responds by returning

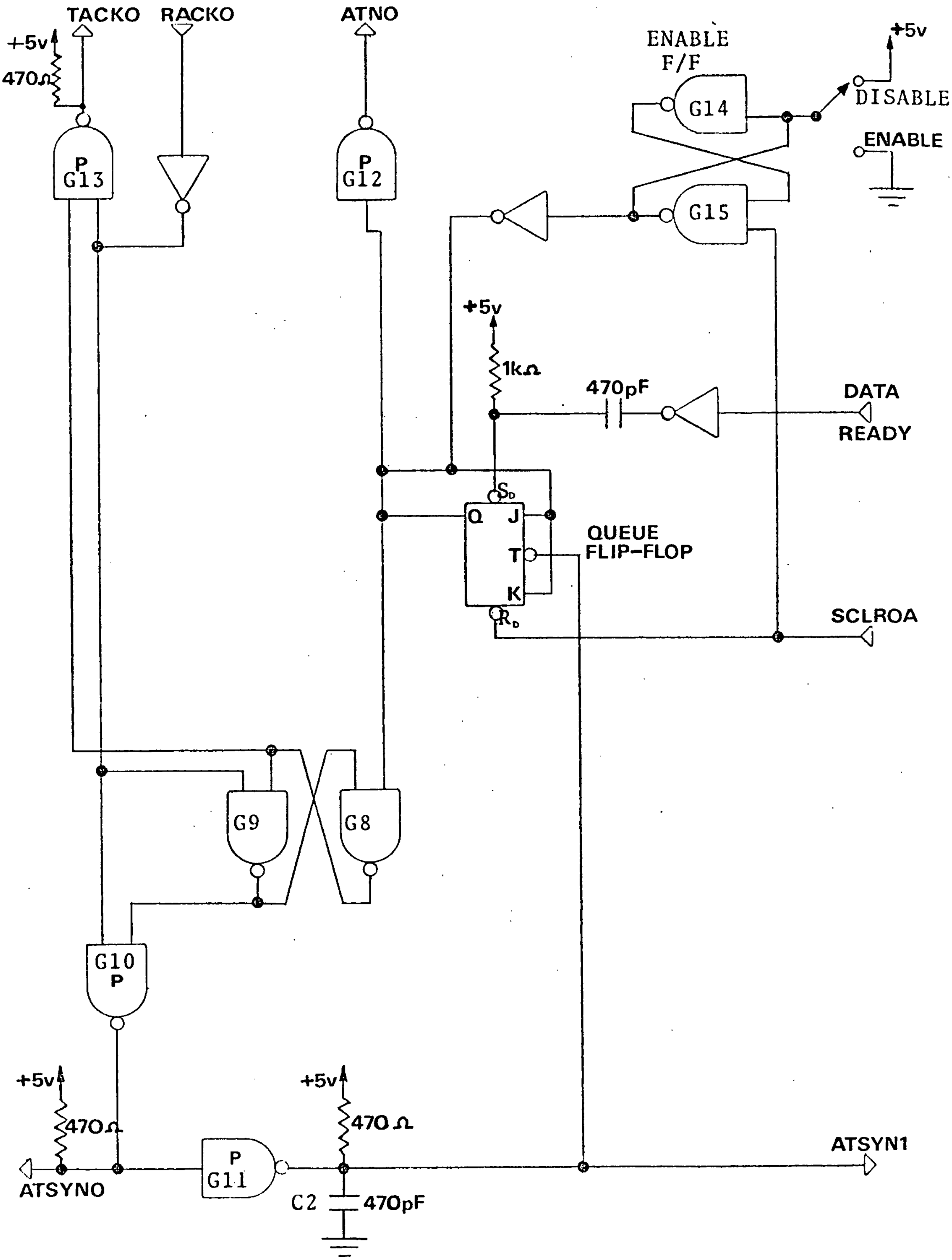


Figure 8. Interrupt Control, Logic Diagram

a receive acknowledge signal (RACKO) to the controller. The gate G8 disables G13 and prevents the transmit acknowledge signal (TACKO) from being sent to the next device. Gates G9 and G10 generate attention synchronize (ATSYNO) which sends a synchronize signal (SYNO) to the processor as well as causing the mass spectrometer address to appear on the inputs of G0 through G7 (see Figure 5). This address is then enabled onto the data request lines by the ATSYNI output from G11. On receiving the SYNO signal, the processor raises RACKO, causing the output of G11 to drop and the queue flip-flop to reset.

If the processor is busy servicing another device interrupt, when a data ready pulse is generated, RACKO is low and the mass spectrometer interrupt is disabled. However, this latter interrupt is stored in the queue flip-flop and is serviced immediately after the previous interrupt has been serviced.

A push-button switch situated at the processor (the initialize switch) is connected via the system clear line (SCLRO) to each interrupt controller such that all queue flip-flops can be direct reset simultaneously.

The interrupt acknowledge control line (ACKO) shown in Figure 3 is divided up into a series of short lines to form the daisy-chain priority system. Clearly the acknowledge signal must pass through every interface equipped with an interrupt controller, and the device situated closest (electrically) to the processor, along the daisy-chain, has highest priority.

3.6 Read/Write Sequencing

The logic circuit shown in Figure 9 is used to control the sequencing of the read and write operations called for by the computer program.

Data and command bytes from the processor arrive along the DALOP lines and are fed to the output command (ØC) memory and display logic (Figure 15) via the four DALIP lines. Three of the outputs from the ØC memory are used to drive a 1-of-8 decoder which provides the sequencing signals for both read and write operations. The remaining output is used to provide a read or write enable signal to a series of AND gates.

Both the data bytes received from the digital voltmeter and the data bytes to be written upon the display have to be sequenced in a particular order. This is accomplished partly by the software and partly by the sequencing logic.

The external connections to the read-write sequencing logic (interface section 2) are shown in Figure 10.

3.6.1 Read Operation

Binary-coded-decimal (BCD) information is available on four lines from each decade of the digital voltmeter. This data, together with the overrange digit, is gated onto the lines DINOP4 through DINOP7; the lines DINOP0 through DINOP3 being unused. Additional information pertaining to shunt number, scan direction and display function switch position, are also gated onto the DINOP lines.

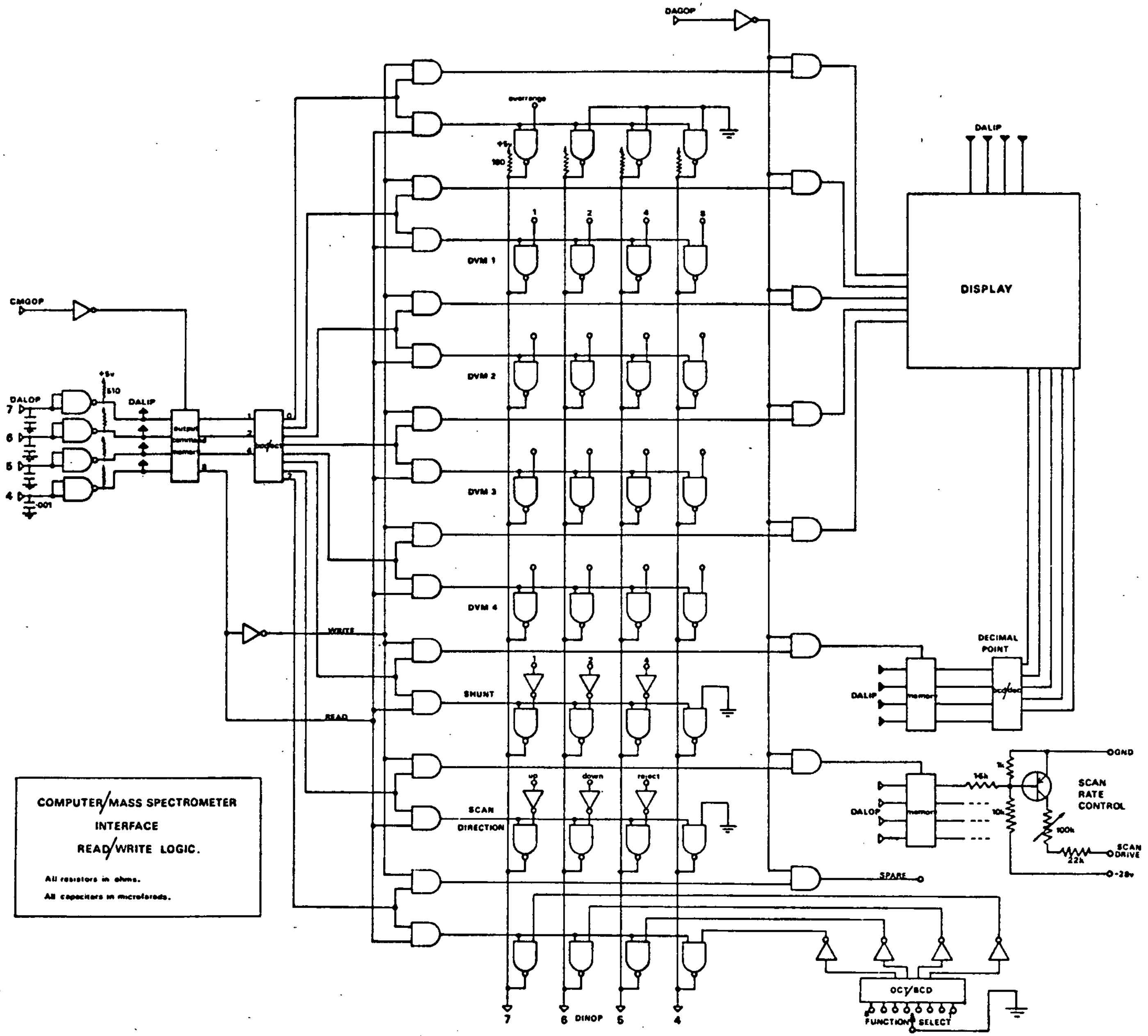


FIGURE 9. COMPUTER/MASS SPECTROMETER INTERFACE READ/WRITE LOGIC

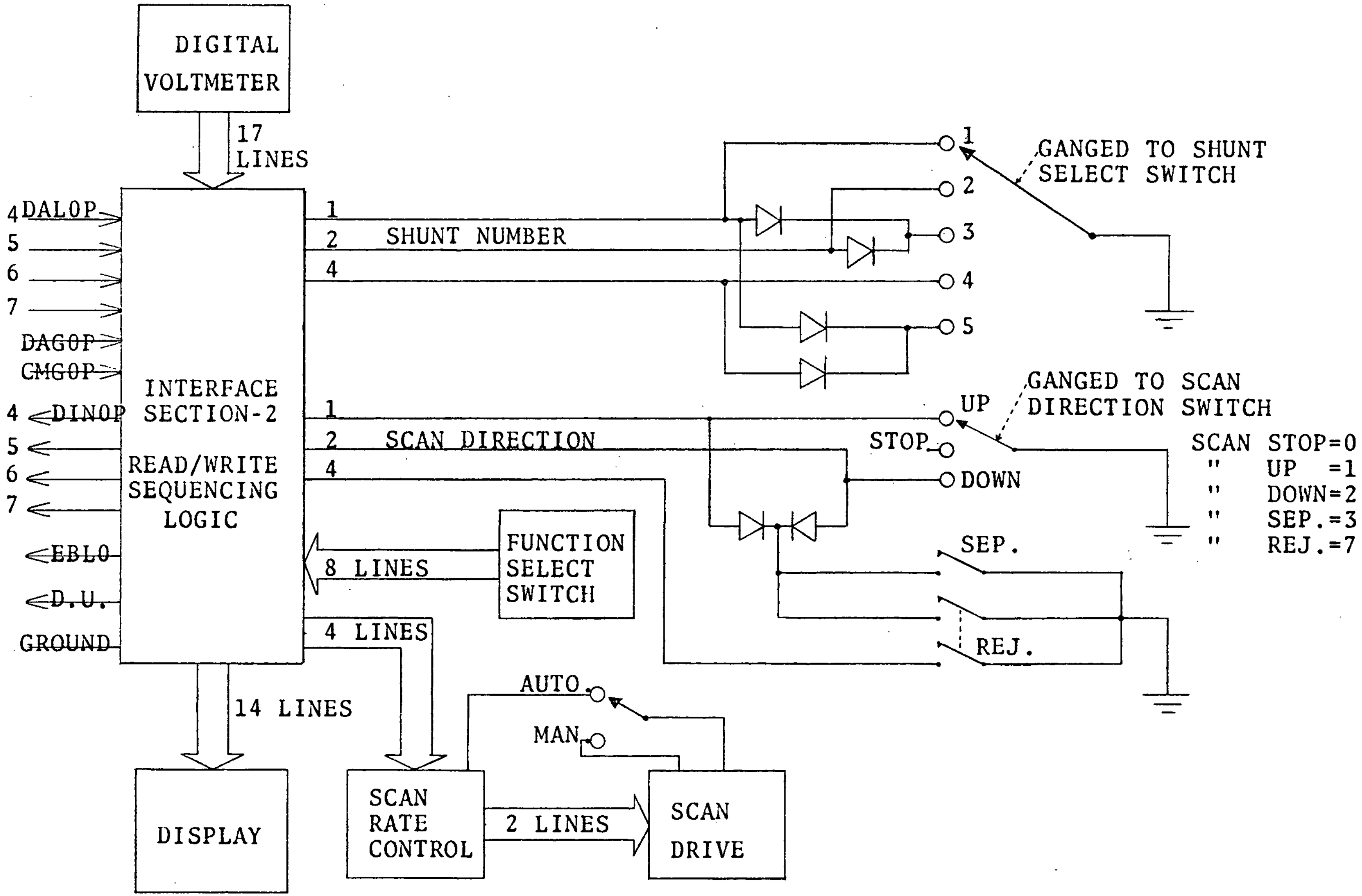


FIGURE 10. EXTERNAL CONNECTIONS TO READ/WRITE SEQUENCING LOGIC

Figure 11 shows a typical sequence of instructions necessary to read the digital voltmeter, shunt number, scan direction, and display function switch position. It is assumed here that the digital voltmeter has generated an interrupt and the processor is now ready to service the mass spectrometer. An "output command (ØC)" is sent from the processor, arrives at the ØC memory (Figure 9), and is promptly stored on receipt of a command strobe pulse (CMGOP). This first ØC contains the coded information requesting that the overrange digit of the digital voltmeter be placed on the DINOP lines. The next instruction is "read data (RD)" which causes the data on the DINOP lines to be read into a specified location in core memory. The "add halfword register (AHR)", "compare logical halfword immediate (CLHI)", and "branch on low (BL)", instructions cause the ØC index register to be repetitively incremented by one until all available information has been read, one byte at a time, into separate locations in core memory.

3.6.2 Write Operation

The sequence of instructions necessary to write (output) data from core memory (Figure 12) resemble those used to read (input) data from the mass spectrometer (Figure 11). The "output command (ØC)" sequences the output bytes in a similar manner to that described in Section 3.6.1, however bit 4 of the

```
0000R 0809     RCMD    DC     X'0809'        DEFINE CONSTANTS
0002R 0A0B             DC     X'0A0B'
0004R 0C0D             DC     X'0C0D'
0006R 0E0F             DC     X'0E0F'
0008R          RDATA   DS     8              DEFINE STORAGE
0010R 0755             XHR    5,5            ZERO REG#5
0012R C820             LHI    2,H'1'         LOAD 1 INTO REG#2
      0001
0016R C830             LHI    3,H'13'        LOAD 13 INTO REG#3
      000D
001AR DE35     RSTART  OC     3,RCMD(5)      OUTPUT COMMAND(READ)
      0000R
001ER DB35             RD     3,RDATA(5)     READ ONE BYTE DATA
      0008R
0022R 0A52             AHR    5,2            INCREMENT REG#5 BY 1
0024R C550             CLHI   5,8            CONTENTS REG#5<8?
      0008
0028R 4280             BL     RSTART         YES; BRANCH TO RSTART
      001AR
```

FIGURE 11. READ SEQUENCING INSTRUCTIONS

```
0000R 0001     WCMD    DC     X'0001'        DEFINE CONSTANTS
0002R 0203             DC     X'0203'
0004R 0400             DC     X'0400'
0006R          WDATA   DS     6              DEFINE STORAGE
000CR 0755             XHR    5,5            ZERO REG#5
000ER C820             LHI    2,H'1'         LOAD 1 INTO REG#2
      0001
0012R C830             LHI    3,H'13'        LOAD 13 INTO REG#3
      000D
0016R DE35     WSTART  OC     3,WCMD(5)      OUTPUT COMMAND(WRITE)
      0000R
001AR DA35             WD     3,WDATA(5)     WRITE ONE BYTE DATA
      0006R
001ER 0A52             AHR    5,2            INCREMENT REG#5 BY 1
0020R C550             CLHI   5,5            CONTENTS REG#5<5?
      0005
0024R 4280             BL     WSTART         YES; BRANCH TO WSTART
      0016R
```

FIGURE 12. WRITE SEQUENCING INSTRUCTIONS

ØC is now a zero causing the write line to be made active. When a "write data (WD)" instruction is executed, a byte of data is fetched from a specified location in core memory and placed on the DAL's. A pulse on the DAGOP control line strobes this data byte into one decade of the display designated by the previous ØC.

The location of the decimal point on the display is controlled by a separate memory and decoder, and can be updated when required by a suitably coded ØC and WD instruction. Similarly the mass spectrometer magnetic scan rate can be varied using another memory. Each output of this latter memory is connected to a simple transistor switching circuit which controls the frequency of a unijunction transistor oscillator. This, in turn, determines the magnetic scan rate via a stepping motor and potentiometer. The complete scan drive circuit, designed by R. D. Russell, is given in Appendix II. In the present system there are four possible scan speeds which are considered ample for the programmed control envisaged.

A programming guide for the mass spectrometer interface is given in Appendix IV.

3.7 The Analog-To-Digital Converter

A Model 344-2 digital voltmeter (DVM) manufactured by the Data Technology Corporation is used as an analog-to-digital (A/D) converter in the data acquisition system. This instrument, utilizes the dual slope integration technique for A/D conversion.

Figure 13 shows a block diagram of the DVM and Figure 14 illustrates some typical dual slope waveforms.

The analog voltage output from the mass spectrometer measuring system is applied to the input amplifier of the DVM. A pulse from the reset oscillator (frequency: 5Hz) initiates a 10,000 count such that the input signal is integrated for a period of 50ms. This integration time is controlled by a 200KHz oscillator (clock). The integrating capacitor (C1) is discharged until the 10,000 count is completed (full scale), leaving a voltage on C1 which is proportional to the input signal. Upon reaching full scale the input current (I_{IN}) is switched off and a constant current source (I_{REF}) is switched to C1. The capacitor is then charged at a constant rate while the counter continues to run. When the voltage across the capacitor reaches the start voltage (15 volts), a zero detect (ZD) pulse is generated which resets the ZD flip-flop and disables the clock. The number of counts (N), accumulated by the counter, is proportional to the input voltage. The output of the ZD flip-flop triggers a one-shot pulse (data ready) which enables the quatch-latch memories to accept the new BCD numbers into storage. The BCD outputs from these memories are used to provide the digital information for the computer interface.

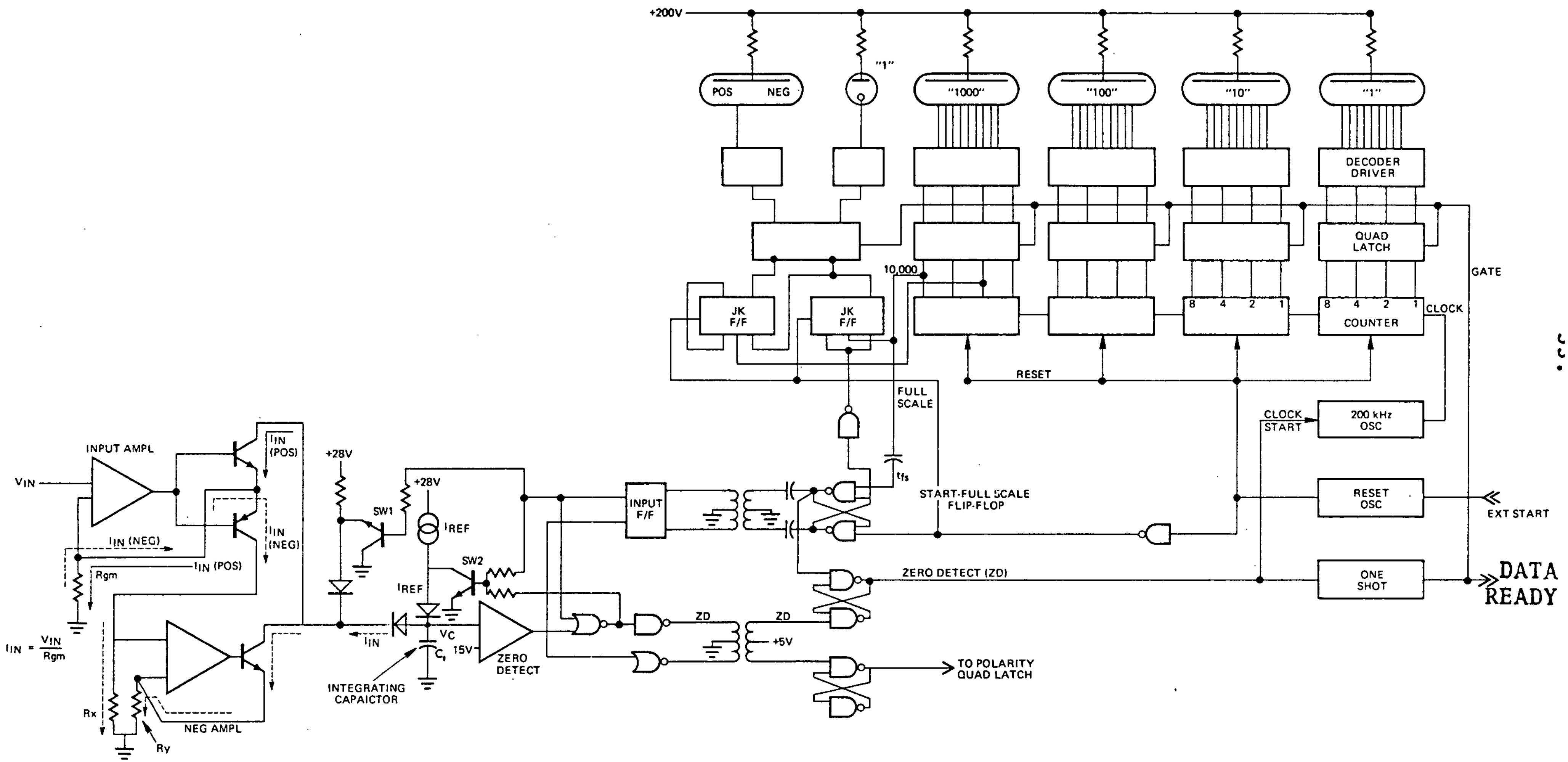


FIGURE 13. ANALOG-TO-DIGITAL CONVERTER BLOCK DIAGRAM
(Reproduced, by permission, from Data Technology Corp., Manual#18915-10)

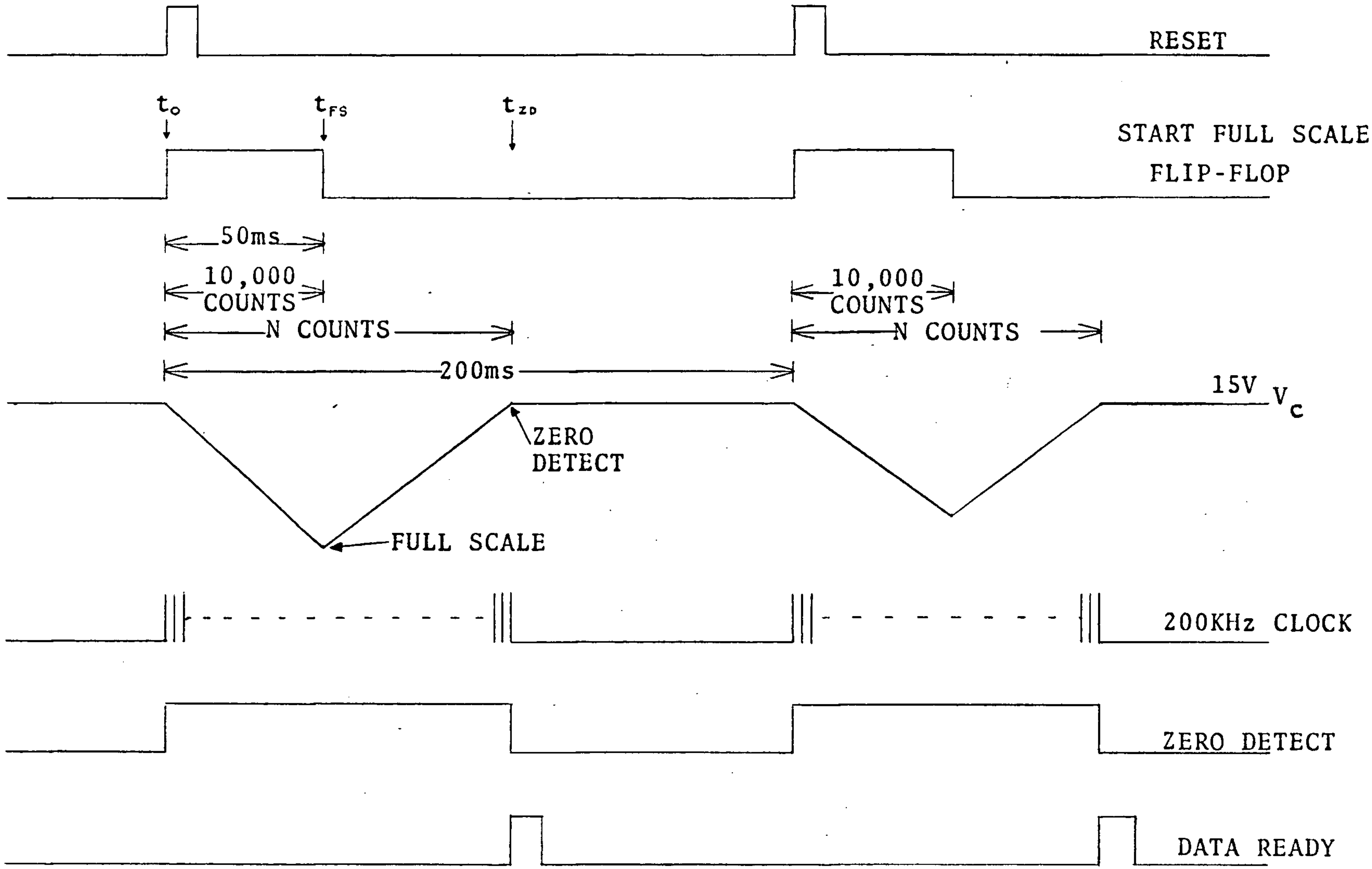


FIGURE 14. DUAL SLOPE WAVEFORMS FOR DIGITAL VOLTMETER

An important feature of the dual slope technique is that the accuracy of the A/D conversion is not dependent on the drift of the 200KHz oscillator. Since the 10,000 count remains constant, the integrating time varies in accordance with any oscillator drift such that the total count, N, remains constant for a given input voltage.

The Model 344-2 DVM has a full scale voltage range of 0-1.0000 volts with a 40% overrange capability. The manufacturers quoted accuracy is ±(.01% reading + .0001) volts.

3.8 The Numerical Display

The numerical output display for the mass spectrometer interface consists of 5 Datecon DS-103 display modules. Each module consists of a quad-latch memory which stores the input data (in BCD format) on application of a strobe pulse. The output from the memory is fed to a BCD-to-Decimal decoder which drives a cold-cathode decade display tube. Each display tube incorporates a decimal point which can be controlled by a separate quad-latch memory and decoder (Figure 9). Power requirements, in addition to the +5 volts logic supply, are a +200 volts supply for the display tube anodes.

Figure 15 shows the complete display logic circuit.

3.9 Construction of the Interface

The interface was constructed in two sections to try

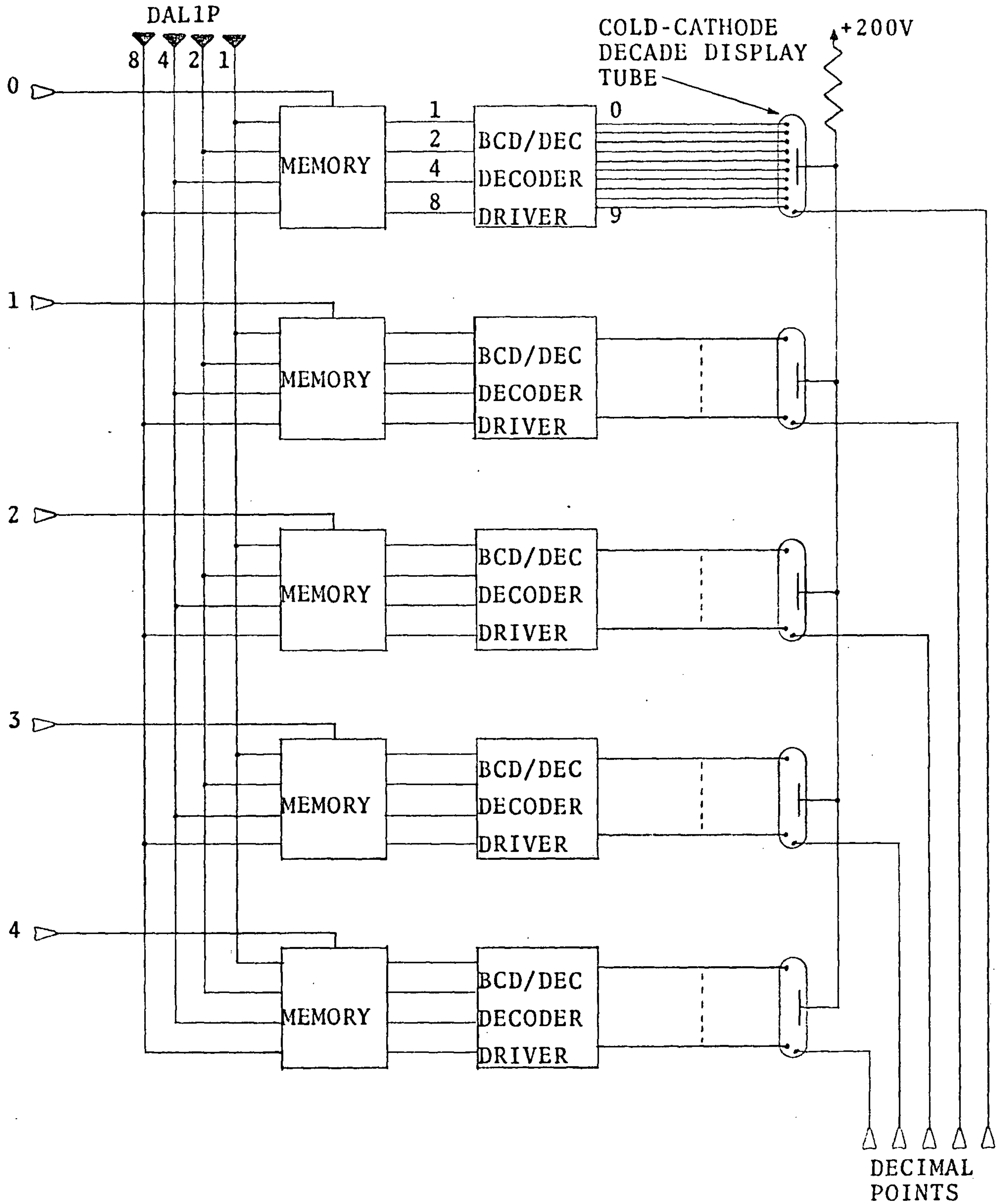


FIGURE 15. THE NUMERICAL DISPLAY

and minimize the number of communication lines between the computer and mass spectrometer. Section 1 consists of the address logic, the data and status input logic, the data and command output logic, and the interrupt circuitry built on two double-sided printed circuit boards which slide into a rack situated inside the computer cabinet. Section 2 contains the read/write logic circuitry illustrated in Figure 9; the prototype unit constructed by the writer was built on 6 single-sided printed circuit boards which could communicate with each other through 22 pin connectors. The 6 printed circuit boards, numerical display, digital voltmeter, and power supply are mounted on an aluminum chassis which fits into the mass spectrometer console. An aluminum front panel incorporates the display and voltmeter bezels and all the necessary switches.

The integrated circuit (i.c.) logic packages (chips) used in the construction of the interface are mostly Motorola DTL plastic types with the exception of the complex functions (decoders and quad latch memories) which are of the TTL family (see Table III). Each 14 or 16 pin plastic package contains from 1 to 6 logic elements depending upon the particular logic function desired. All the i.c. packages employed in the mass spectrometer interface were designed for operation from a 5±1/2 volts regulated power supply (±5%).

The power supply (PS-200) in section 2 supplies the 200 volts for the cold-cathode decade display tubes and a stabilized 5 volts for the read/write logic circuitry. The i.c. packages in section 1 utilize the Interdata Processor 5 volt

TABLE III INTEGRATED CIRCUIT PACKAGES USED IN CONSTRUCTION OF INTERFACE LOGIC CIRCUITRY

MOTOROLA NUMBER	FUNCTION	FAMILY	OUTPUT LOADING FACTOR /OUTPUT	PROPAGATION DELAY ns TYPICAL	TOTAL POWER DISSIPATION mW TYP/PKG	COST /PKG $	QUANTITY USED IN INTERFACE
MC834P	HEX INVERTER	DTL	8	30	66	2.00	8
MC845P	CLOCKED FLIP-FLOP	DTL	12	40	60	1.62	1
MC849P	QUAD-2 INPUT NAND	DTL	7	25	66	1.65	17
MC855P	J-K FLIP-FLOP	DTL	11	40	140	2.10	1
MC858P	QUAD-2 INPUT POWER	DTL	27	30	130	2.70	17
MC1803P	8-INPUT NAND	DTL	7	25	16.5	1.55	2
MC1806P	QUAD-2 INPUT AND	DTL	8	35	72	1.90	6
MC1809P	QUAD-2 INPUT OR	DTL	7	30	115	1.90	1
MC4038P	1-OF-8 DECODER	TTL	11	45	240	6.65	1
MC7442P	BCD/DEC DECODER	TTL	11?	45?	105?	6.75	1
MC7475P	QUAD LATCH MEMORY	TTL	10	30	160	4.50	3

supply which serves to eliminate one line between sections 1 and 2.

An unshielded cable, approximately 43 feet in length, is used to transfer information on 13 lines between section 1 and 2; this cable should be kept as short as possible. No noise or crosstalk problems were experienced provided all the lines were made false-active and power gates, with a suitable pull-up resistor, were used at the transmission end of each line. In addition great care was taken to avoid ground loops which can easily arise during the construction of complex electronic equipment.

After the prototype interface had proved itself reliable over several months of testing, a double-sided, one piece printed circuit board was designed (by E. J. Bellis) for the section 2 logic circuitry. Using this new printed circuit board, two more complete interfaces were constructed and installed in the remaining two 30 cm radius mass spectrometers at the University of B.C., isotope geophysics laboratory. All three interfaces are now operating and are being used for isotope analyses, and it is intended that the one Interdata computer will service all three mass spectrometers on a time sharing basis.

CHAPTER 4

4.1 On-Line Filtering of Data

The simplest mode of operation of the data acquisition system is the on-line filtering of data from the digital voltmeter and the display of the filtered data on the numerical readout.

Previous computer off-line programs designed to process mass spectral data have always incorporated some form of digital filtering to reduce higher frequency noise. It therefore seemed reasonable to design a digital filter program for the Interdata computer which would display the filtered data points at the mass spectrometer console immediately, as well as storing a smoothed version of the mass spectrum in a memory buffer, from which it could be transferred to magnetic tape via the Selector Channel.

A suitable low-pass digital filter had been designed by R. D. Russell and J. Blenkinsop for an IBM 360/67 and this program was rewritten (by J. Blenkinsop) in the Interdata programming language. A flow-diagram of the filter program is shown in Figure 16.

The digital voltmeter produces 5 data points/second which corresponds to a Nyquist frequency of 2.5Hz. The fundamental sampling theorem requires that in order to completely recover the original signal, the sampling frequency must be

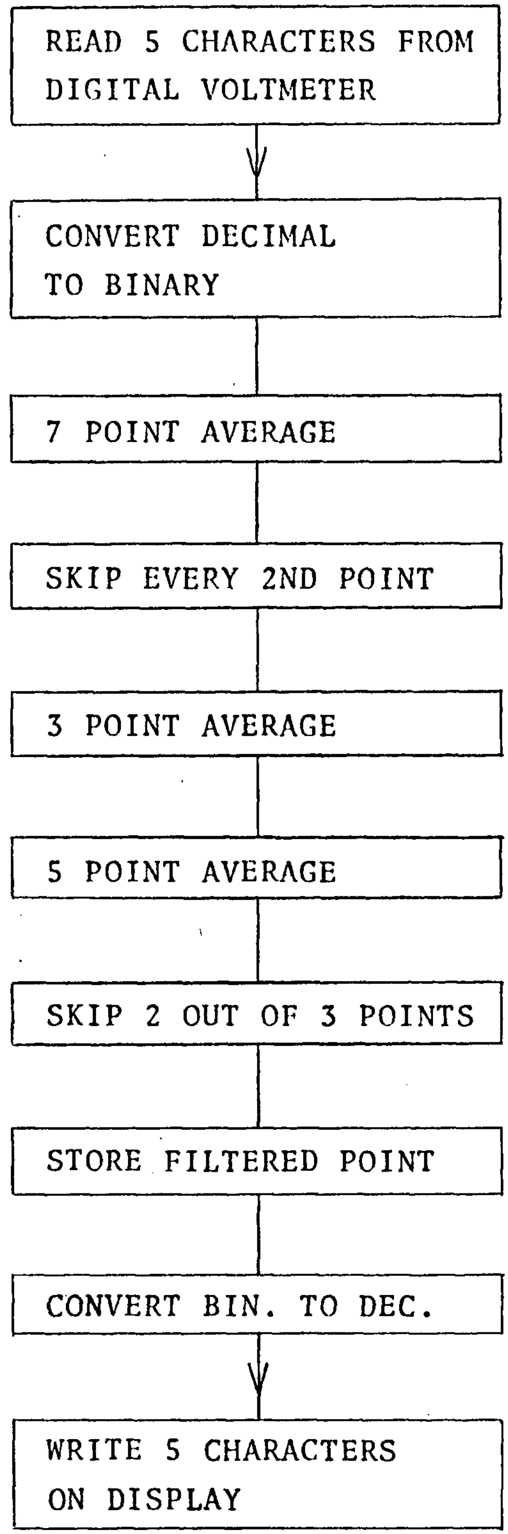


FIGURE 16. MASS SPECTROMETER FILTER-DISPLAY PROGRAM

at least twice the highest occurring frequency in the sampled signal. Physical signals, however, do not have a finite frequency content. The part of the signal spectrum lying above the Nyquist frequency will be reflected and superimposed (folded back) onto lower frequencies, and the original signal can only be recovered approximately. The best one can do is to choose the Nyquist (folding) frequency (and therefore the sampling rate) high enough to include all frequencies lying in the passband of the ion current measuring system. However, frequencies above 2.5Hz do not contribute significantly to the mass spectral records encountered and a sampling rate of 5 points/second should therefore be quite adequate.

When selecting a filter for mass spectral data it is important that the width of the total averaging function (the data window) is less than or equal to the mininum width of the peak tops. For the filter used, the width of the data window is 3.8 seconds which necessitates dwelling on a peak top for a period of at least 3.8 seconds.

Digital filtering is accomplished in the Processor by adding together points to form a moving average by sevens and applying every other averaged point to a three point moving average, followed by a five point moving average. One out of every three points from the five point average is stored in a memory buffer, converted from binary to decimal notation, and then written on the display. The 7-point, 3-point, and 5-point averages all have tapered endpoints, which is to say that the end-points have weighting coefficients of one half (in our case).

This has the effect of reducing the amplitude of side lobes on the filter response (Figure 17).

It should be evident from the above description that there is one filtered point available, at the output of the filter, for every six raw input data points, hence the display is updated once every 1.2 seconds.

The Nyquist frequency is lowered to 2.5/6 Hz after filtering, but since there is little signal or noise still present above 0.1Hz, it is clear that no information is being discarded in this way.

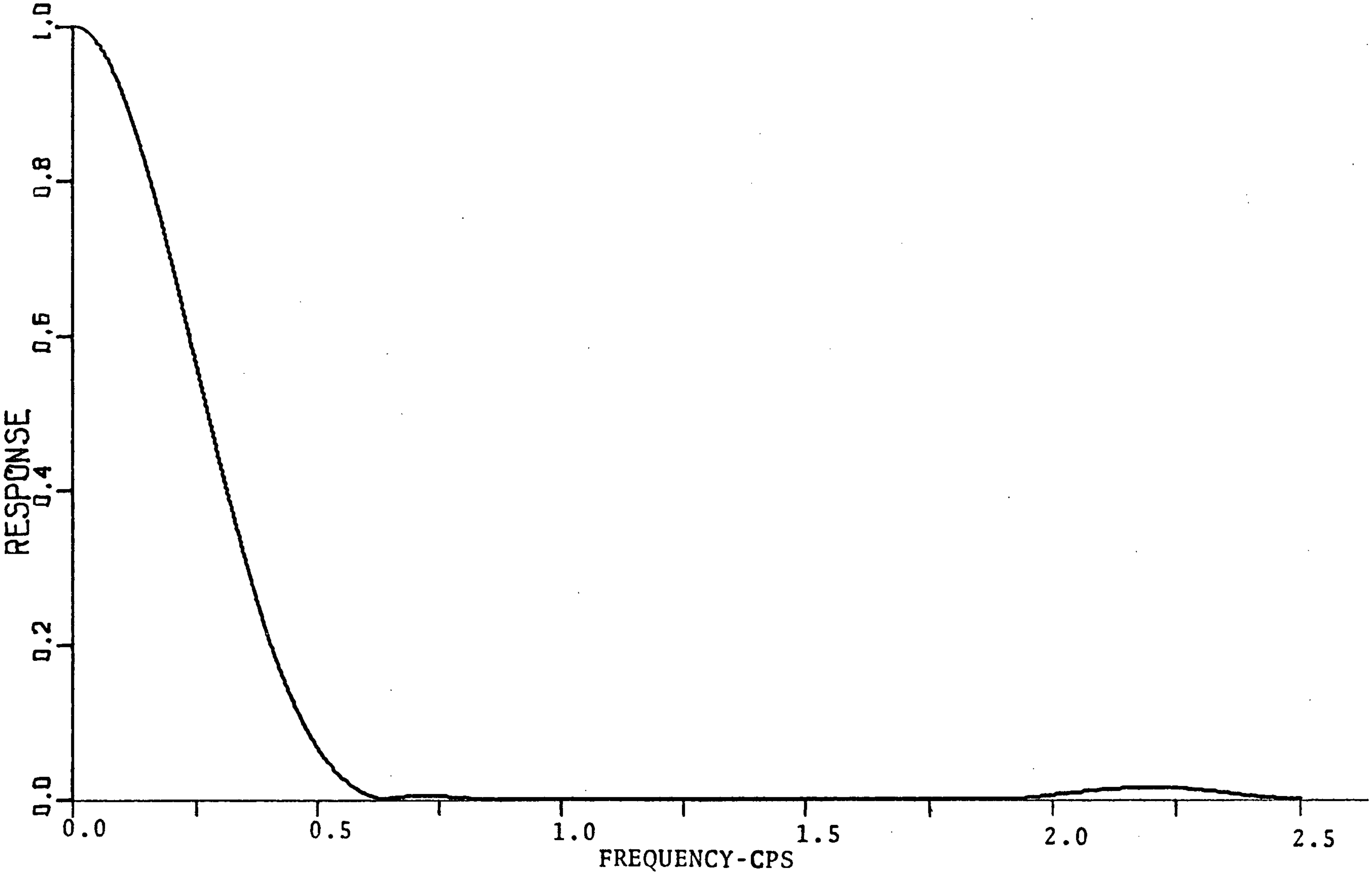


FIGURE 17. FREQUENCY RESPONSE OF DIGITAL FILTER

CHAPTER 5

SYSTEM PERFORMANCE

5.1 Introduction

In order to test the accuracy and reliability of the computer interface two strontium isotope analyses were performed using both an interlaboratory standard and a rock sample of unknown composition.

The mass spectrometer which has been interfaced to the computer is principally used for the rubidium-strontium age dating of rock samples. Natural rubidium has two isotopes, Rb^{85} which is stable, and Rb^{87} which is radioactive and decays to Sr^{87} with a half-life of approximately $5x10^{10}$ years. There are four stable isotopes of strontium, namely Sr^{84}, Sr^{86}, Sr^{87} and Sr^{88}, and of these, in a closed chemical system, only the abundance of Sr^{87} increases with time. If the initial amount of Sr^{87} in the sample can be determined, and the present abundances of Sr^{87} and Rb^{87} in the sample are measured, the age of the sample can be determined.

5.2 Preparation of Strontium Samples

The method devised by B. D. Ryan (1971) for the chemical spearation of strontium from a rock sample is used.

The rock sample is crushed to a fine powder and approximately 0.25 gms is weighed out into a teflon beaker. The sample is completely dissolved in H_2SO_4 and HF, heated, and evaporated to dryness. The residue is dissolved by warming with HCl and allowed to cool. The sample is centrifuged and the solution transferred to the top of a cation exchange column, of length 21 cms, containing Dowex 50W-X8 Resin (200-400 Mesh). The column is eluted with 6NHCl and the eluate collected in a measuring cylinder. The first 25 ml of eluate are discarded and the next 40 ml collected. The cut of 40 ml is evaporated dry and taken up in 2 ml 2NHCl. Meanwhile, the columns are back aspirated with 2NHCl. The sample (2 ml) is added to the column and eluted with 2 NHCl. The first 90 ml of eluate are discarded and the next 40 ml collected. This cut of 40 ml is evaporated to dryness and the residue dissolved in 3 drops 2NHCl.

5.3 Analysis of Eimer and Amend $SrCO_3$ Interlaboratory Standard

The Eimer and Amend $SrCO_3$ was chosen because it has been analysed at a large number of different laboratories, including The University of British Columbia, where it has been analysed a number of times previously using the same mass spectrometer. For the purposes of interlaboratory comparison the Sr^{87}/Sr^{86} ratio is taken as 0.70800.

The $SrCO_3$ is dissolved in 2NHCl to produce a solution containing approximately 400μg strontium per ml of 2NHCl. Two drops of the solution are deposited on each of the outgassed rhenium side-filaments* and evaporated to dryness by passing a current of about one Amp through each filament while they are exposed to the atmosphere. The two side-filaments and a rhenium centre-filament are mounted in a stainless steel block which, in turn, is positioned inside the mass spectrometer.

The whole system is evacuated to a low pressure ($< 2x10^{-7}$ mm Hg).

The centre-filament is heated by passing a current of about 4.0 Amps through it. Collision with the hot centre-filament produces efficient ionization of the sample that is being gently evaporated from the relatively cool side-filaments. The positive ions produced are accelerated by a potential of 5000 volts and can be focussed into a Faraday cup using a variable field strength electromagnet. The charges that collect in the cup, constitute the ion current which is measured, the magnitude of this current is directly proportional to the abundance of the particular isotope ion beam focussed into the Faraday cup. The centre-filament current is slowly increased and a search is made for a Rb^{85} contamination peak. If any rubidium is present, it is burnt off the side-filaments at a filament temperature just below that required to produce an appreciable strontium spectrum. When the height of the Rb^{85}

*The triple-filament technique of solid-source mass spectrometry was used for all the analyses.

peak is negligible, which implies that the height of the Rb^{87} peak is also negligible (since the ratio Rb^{85}/Rb^{87} = 2.593 is constant), the centre-filament current is increased to a value such that a Sr^{88} peak height of about 1 Volt is obtained with the output attenuator set on shunt 3. A check is made for rubidium contamination at this new centre-filament temperature and if a Rb^{85} peak is still detectable it is burnt away before the strontium spectrum is scanned.

The strontium 86, 87 and 88 peaks are scanned in sequence about 12 times by varying the magnet field intensity using a peak-hopping technique. The peak heights and baselines are read from the filter display and are written by hand on the chart recorder which provides a visual record of the spectrum.

In order to calculate the Sr^{87}/Sr^{86} ratio for each scan it is necessary to correct the measured ratio for the growth or decay of the peak heights, then this ratio is corrected for mass discrimination at the ion source. Fortunately the peak heights grow or decay almost linearly and hence a correction is easily applied. Discrepancies in the isotope abundances due to mass discrimination (fractionation) can be simply corrected for in the case of strontium since the ratio Sr^{87}/Sr^{86} is constant (=0.1194). The Sr^{86}/Sr^{88} ratio is calculated for each scan and the discrimination per unit mass determined.

An average value for the corrected (normalised) Sr^{87}/Sr^{86} ratio over all the scans is calculated, together with a value for the standard deviation of the mean.

The result, given in Table IV, indicates about a twofold increase in precision over previous values obtained by J. Blenkinsop, using the same mass spectrometer, without the computer interface.

5.4 Analysis of Strontium in a Rock Sample

As a further test of the performance of the computer interface two analyses were performed on a rock sample. The sample selected was a light grey argillite (slightly metamorphosed claystone) from the Creston formation outcropping in S.E. British Columbia. This formation is part of the Purcell Series which is stratigraphically equivalent to the Belt Series which outcrops in western Montana and northern Idaho. Smith and Barnes (1966) refer to these two series as the Belt-Purcell Supergroup. The Supergroup, which crops out over an area of more than 50,000 square miles, consists largely of metamorphosed sediments which have not undergone intense deformation. Thicknesses of greater than 40,000 feet have been attained. The sediments contain no useful datable fossils and therefore provide excellent material for isotope dating studies of Precambrian rocks (1400 - 900 m.y. [million years]).

Obradovich and Peterman (1968) have dated rocks of the Belt Series using Rb-Sr and K-Ar techniques. Their determinations yield ages ranging from about 900 m.y. to around 1300 m.y.

Rb-Sr isotope measurements performed by Ryan and Blenkinsop (1971) on the Hellroaring Creek Stock in the Purcell Mountains indicate an approximate age of 1260 m.y. This stock, which intrudes the lowest known formation of the Purcell Series (the Aldridge Formation), is the oldest recognized in British Columbia.

The sample of argillite was collected by Dr. W. C. Barnes of the Geology Department, University of B.C., and was made available to the writer by Mr. B. D. Ryan.

X-ray fluorescence measurements, performed by C. Croucher, have shown that this sample contains 80 ± 2% ppm (parts per million) rubidium and 248 ± 2% ppm strontium.

The chemical spearation described in Section 5.2 was carried out twice to provide two strontium samples (A and B) from the one specimen of argillite. This duplicate separation was used to provide a check on the reproducibility of the chemistry since, ideally, samples A and B should yield identical isotope abundance ratios.

Mass spectrometric analyses of samples A and B were performed in a similar manner to that described in Section 5.3 for the Eimer and Amend standard. The much lower concentration of strontium in the argillite samples necessitates much greater care in the filament preparation. Consequently it is important to ensure that all the sample is deposited on the side-filaments, which normally entails pipetting three or more drops of solution onto each side-filament. In order to perform this task, and still maintain all the sample within the middle one-third uppersurface of each side-filament ribbon, the following technique has been found satisfactory. Place one drop of solution in the centre of each side-filament, slowly evaporate the drop to dryness by passing a current of about one Amp through each filament, cool completely, add another drop to the middle of each ribbon, evaporate to dryness, and so on until all the sample solution is shared equally between the side-filament. The current through each filament is then increased until the filaments glow with a dull red color and are then left to "cook" for about one minute. This latter procedure helps produce a more stable ion beam.

Table V gives the results of the two mass spectrometer runs for the samples A and B and the concentrations of the four isotopes of strontium in the argillite sample. These concentrations were calculated using the X-ray fluorescence data and the ratio Sr^{87}/Sr^{86} derived from the mass spectrometer runs.

The percentage deviation from the mean of the ratio SR^{87}/Sr^{86} at a 95% confidence level is about 0.05% which is as good or better than previous analyses performed on rock samples using the same chemical separation procedure and mass spectrometer without the digital filtering of data.

TABLE IV RESULTS OF ANALYSES OF EIMER & AMEND INTERLABORATORY STANDARD $SrCO_3$

LABORATORY	RATIO $(Sr^{87}/Sr^{86})_n$	COMMENTS
UBC (RUSSELL ET AL, 1971)	0.7080±0.0002*	ON-LINE FILTER, HAND CALCULATED (THIS THESIS)
UBC (RYAN & BLENKINSOP, 1971)	0.7082±0.0004	HAND CALCULATED
USGS (STACEY ET AL, 1971)	0.7080±0.0002	DIGITALLY RECORDED & COMPUTED
USGS (STACEY ET AL, 1971)	0.7079±0.0006	HAND CALCULATED
MIT (SPOONER & FAIRBAIRN, 1970)	0.7082±0.0008	HAND CALCULATED
YALE (DASCH, 1969)	0.7075±0.0012	HAND CALCULATED
U of T (PURCY & YORK, 1968)	0.7080±0.0012	HAND CALCULATED
ACCEPTED VALUE	0.70800	

TABLE V RESULTS OF ANALYSES OF GREY ARGILLITE

SAMPLE	RATIO $(Sr^{87}/Sr^{86})_n$
A	0.7419±0.0003*
B	0.7420±0.0005
MEAN OF A & B	0.7419±0.0004

CONSTANT RATIOS:

$Sr^{84}/Sr^{86} = 0.0568$; $Sr^{86}/Sr^{88} = 0.1194$

ISOTOPE CONCENTRATIONS (parts per million) ±2%

$Rb_{(TOTAL)}$	$Sr_{(TOTAL)}$	Sr^{84}	Sr^{86}	Sr^{87}	Sr^{88}
80	248	1.3	23.9	17.9	204.8

* - ALL UNCERTAINTIES QUOTED ARE TWO STANDARD DEVIATIONS (95% CONFIDENCE LEVEL)

CHAPTER 6

6.1 Conclusions

The analyses described in Chapter 5 were not expected to show any appreciable increase in precision over previous analyses, performed on the same mass spectrometer, without the computer interface, but only to test the design and operating reliability of the system. With this end in mind one can only be very satisfied with the results so far obtained. The full potential of this on-line data acquisition system will only be realized when the processor is programmed to determine peak heights and baselines, control scan rates and apply the various analytical corrections.

J. Blenkinsop has completed a prototype program to provide on-line processing of data from the mass spectrometer and his initial results, from several trial runs, indicate about a threefold increase in precision over previous off-line analyses.

No further improvements in the hardware are envisaged in the immediate future, although possible areas of investigation may lie with the computer control of source conditions and the direct reading of the magnetic field intensity for each peak.

There remains great scope for improvements in the software and it is in this field that much effort is being channelled.

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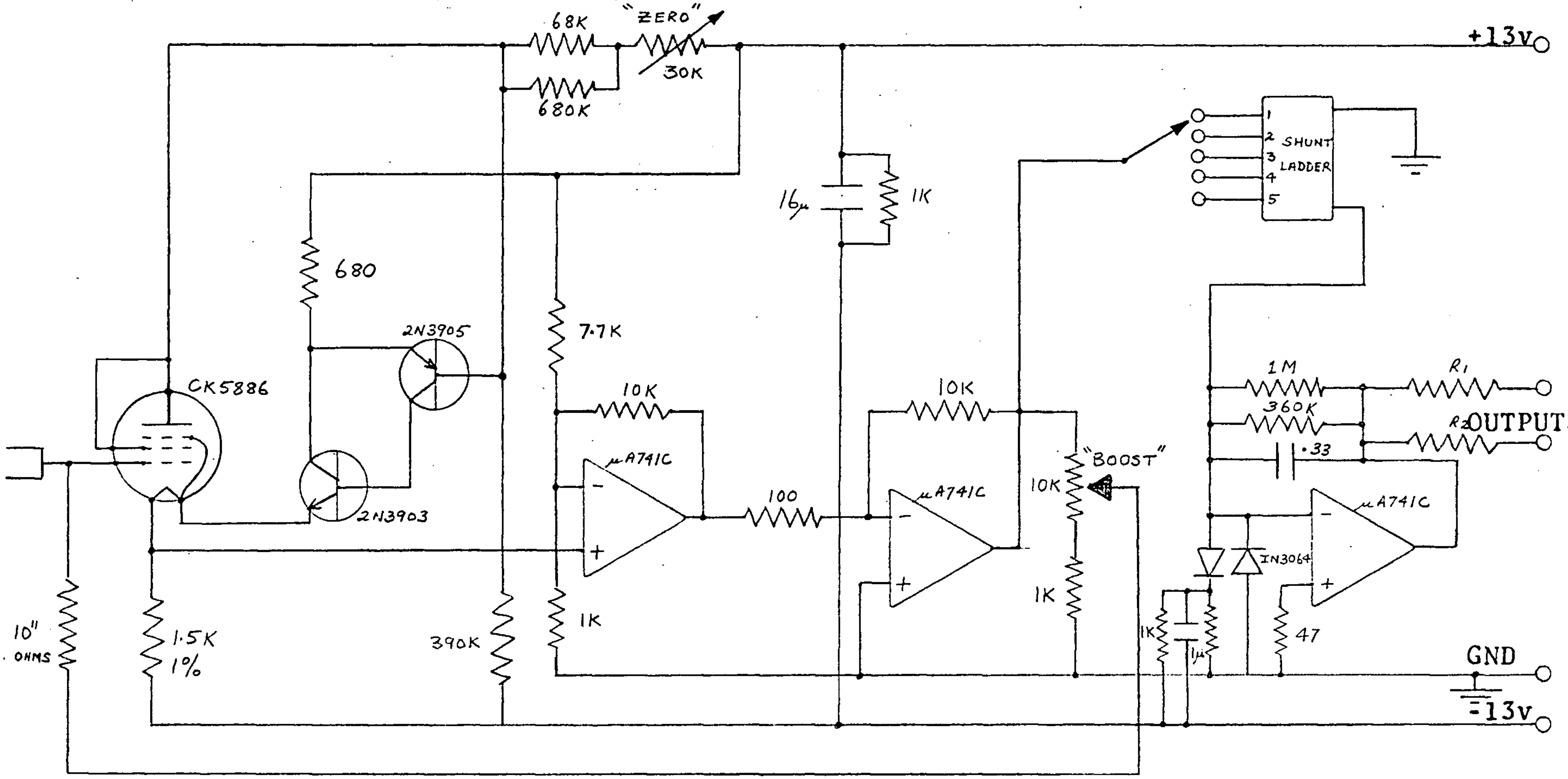
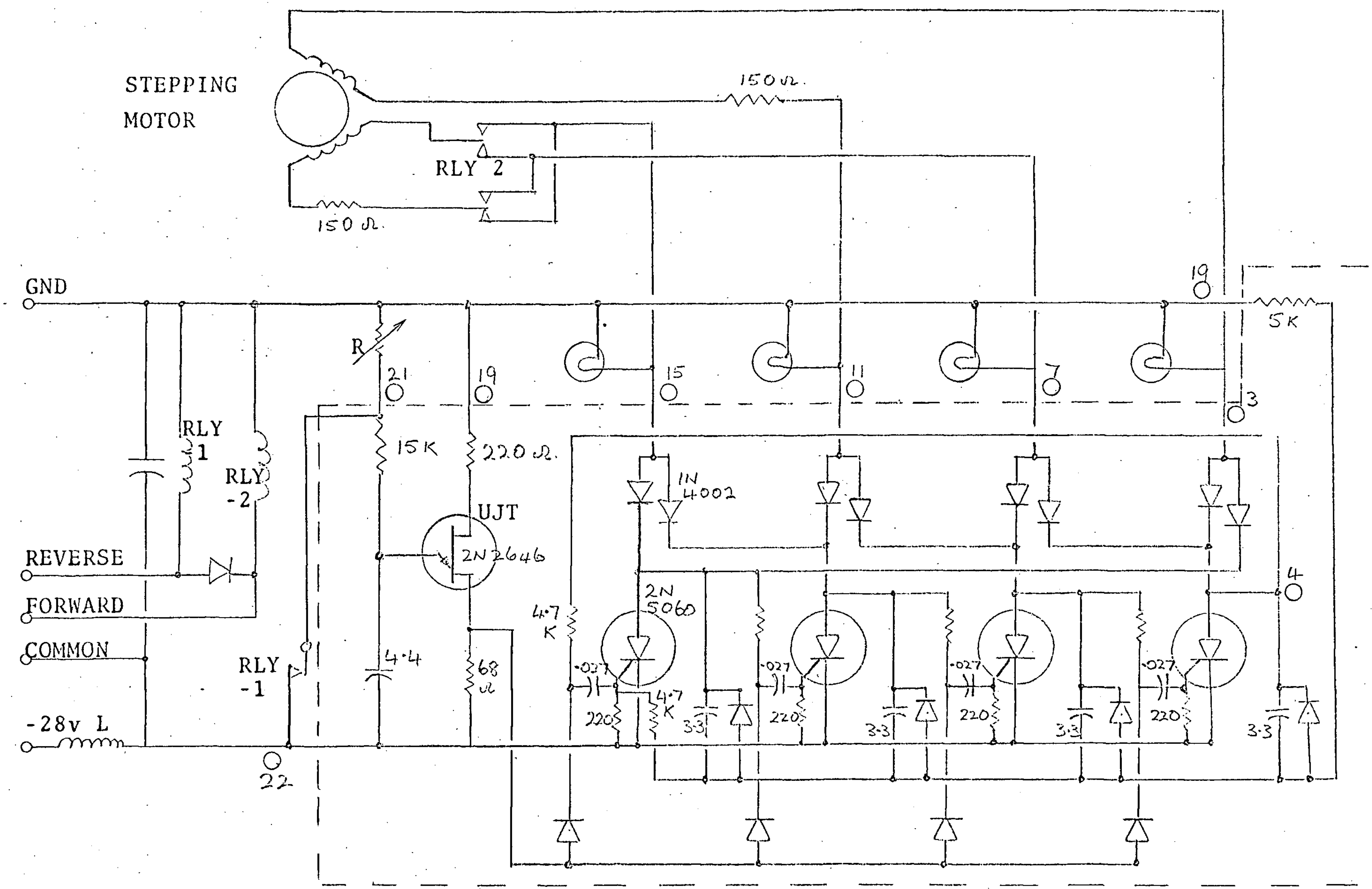


APPENDIX I. ION CURRENT AMPLIFIER & OUTPUT ATTENUATOR CIRCUIT.

(Designed by R.D.Russell, June 1969.)



APPENDIX II. SCAN DRIVE CIRCUIT (designed by R.D.Russell, June 1966)

APPENDIX III.

SUMMARY OF INTERDATA PROGRAMMING INSTRUCTIONS*

OP CODE	TYPE	MNEMONIC	INSTRUCTION
01	RR	BALR	Branch and Link
02	RR	BTCR	Branch on True Condition
03	RR	BFCR	Branch on False Condition
04	RR	NHR	AND Halfword
05	RR	CLHR	Compare Halfword
06	RR	OHR	OR Halfword
07	RR	XHR	Exclusive OR Halfword
08	RR	LHR	Load Halfword
0A	RR	AHR	Add Halfword
0B	RR	SHR	Subtract Halfword
0C	RR	MHR	Multiply Halfword
0D	RR	DHR	Divide Halfword
0E	RR	ACHR	Add with Carry Halfword
0F	RR	SCHR	Subtract with Carry Halfword
28	RR	LER	Floating-Point Load
29	RR	CER	Floating-Point Compare
2A	RR	AER	Floating-Point Add
2B	RR	SER	Floating-Point Subtract
2C	RR	MER	Floating-Point Multiply
2D	RR	DER	Floating-Point Divide
40	RX	STH	Store Halfword
41	RX	BAL	Branch and Link
42	RX	BTC	Branch on True Condition
43	RX	BFC	Branch on False Condition
44	RX	NH	AND Halfword
45	RX	CLH	Compare Logical Halfword
46	RX	OH	OR Halfword
47	RX	XH	Exclusive OR Halfword
48	RX	LH	Load Halfword
4A	RX	AH	Add Halfword
4B	RX	SH	Subtract Halfword
4C	RX	MH	Multiply Halfword
4D	RX	DH	Divide Halfword
4E	RX	ACH	Add with Carry Halfword
4F	RX	SCH	Subtract with Carry Halfword
60	RX	STE	Floating-Point Store

OP CODE	TYPE	MNEMONIC	INSTRUCTION
68	RX	LE	Floating-Point Load
69	RX	CE	Floating-Point Compare
6A	RX	AE	Floating-Point Add
6B	RX	SE	Floating-Point Subtract
6C	RX	ME	Floating-Point Multiply
6D	RX	DE	Floating-Point Divide
90	RR	UNCH	Unchain
92	RR	STBR	Store Byte
93	RR	LBR	Load Byte
96	RR	WBR	Write Block
97	RR	RBR	Read Block
9A	RR	WDR	Write Data
9B	RR	RDR	Read Data
9D	RR	SSR	Sense Status
9E	RR	OCR	Output Command
9F	RR	AIR	Acknowledge Interrupt
C0	RS	BXH	Branch on Index High
C1	RS	BXLE	Branch on Index Low or Equal
C2	RX	LPSW	Load Program Status Word
C4	RS	NHI	AND Halfword Immediate
C5	RS	CLHI	Compare Logical Halfword Immediate
C6	RS	OHI	OR Halfword Immediate
C7	RS	XHI	Exclusive OR Halfword Immediate
C8	RS	LHI	Load Halfword Immediate
CA	RS	AHI	Add Halfword Immediate
CB	RS	SHI	Subtract Halfword Immediate
CC	RS	SRHL	Shift Right Logical
CD	RS	SLHL	Shift Left Logical
CE	RS	SRHA	Shift Right Arithmetic
CF	RS	SLHA	Shift Left Arithmetic
D0	RX	STM	Store Multiple
D1	RX	LM	Load Multiple
D2	RX	STB	Store Byte
D3	RX	LB	Load Byte
D5	RX	AL	Autoload
D6	RX	WB	Write Block
D7	RX	RB	Read Block
DA	RX	WD	Write Data
DB	RX	RD	Read Data
DD	RX	SS	Sense Status
DE	RX	OC	Output Command
DF	RX	AI	Acknowledge Interrupt

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APPENDIX IV

MASS SPECTROMETER INTERFACE PROGRAMMING GUIDE

ADDRESSES

HEX D - M.S.2
HEX E - M.S.1
HEX F - M.S.3

STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE								DU
COMMAND BYTE					1-READ 0-WRITE	SEQUENCING		

DU - The device unavailable bit is set when the M.S. 5v power supply is off.

READ - This command sets the output command memory so that data can be read from the M.S.

WRITE - This command sets the OC memory so that data can be written on the display. The scan rate is also controlled in the write mode.

SEQUENCING - Bits 5,6 and 7 are used for sequencing the data in both the read and write modes.

READ SEQUENCING - COMMAND BYTE

BIT NUMBER	4	5	6	7	
	1				-Read DVM overrange
	1			1	-Read DVM decades in sequence
	1		1		"
	1		1	1	"
	1	1			"
	1	1		1	-Read shunt number
	1	1	1		-Read scan direction code
	1	1	1	1	-Read function select switch

Data is read using the OC instruction followed by the read data (RD) instruction.

WRITE SEQUENCING - COMMAND BYTE

BIT NUMBER	4	5	6	7	
					-Write on display decades in sequence
				1	"
			1		"
			1	1	"
		1			"
		1		1	-Write decimal point
		1	1		-Set scan rate
		1	1	1	-Not used

Data is written using the OC instruction followed by the write data (WD) instruction.

DVM - DECADE NUMBERING (Front view).

OVER-RANGE	1	2	3	4

DISPLAY - DECADE NUMBERING (Front view).

0	1	2	3	4