Transport in Graphene Nanoelectronic Devices

Effects Due to Gold Deposition on the Surface of Graphene

by

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Abstract

Graphene is a unique material with extraordinary properties, in both its mechanical structure and strength as well as its superb electronic transport. It has become an important focus of physical and chemical research, and many practical applications that take advantage of its properties have been found as well. Since graphene is a single atomic layer all charge carriers involved in conduction through it are always in contact with the surface. Thus, surface effects are expected to play a very important role in determining the characteristics of a sheet of graphene. In this project, graphene nanoelectronic devices are fabricated, and the effects on their transport properties of depositing minute amounts of gold onto their surfaces are investigated.

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Finally, I would like to thank Dr. Rob Kiefl for providing general but very useful advice regarding the presentation of research, in both written and oral form.

Dedication

To my parents, who have supported me in every way possible throughout my time at UBC.

Chapter 1

Introduction

1.1 Graphene

Graphene, the material studied in this project, is novel for a wide variety of reasons.

Graphene is a single atomic sheet of carbon which exhibits a honeycomb lattice molecular structure. Being only one atom 'thick', graphene can be said to be the thinnest material known to the world. In 2004, A. Geim and K. Novoselov performed groundbreaking experiments involving graphene that brought the material to the attention of physicists and engineers around the globe, kickstarting the plethora of research undergone since then [1, 2]. They were awarded the 2010 Nobel Prize in Physics for their achievement.

1.1.1 Physical Properties and Interest

The properties of graphene make it of great interest for fundamental physical research [2, 3].

Graphene has an extraordinarily high conductance, and this is a main motivator for graphene research. Expectedly then, it also exhibits high electron mobility, and, in an ideal situation, perfect charge homogeneity. However, situations are often not ideal and much research has been devoted to improving the quality of obtainable graphene, through both new synthesis techniques and alternate methods of device fabrication [4–8].

Graphene's energy dispersion can be described by the following equation

$$E(k) = \pm\sqrt{\Delta^2 + (\hbar v_F k)^2} \tag{1.1}$$

where v_F is the Fermi velocity and Δ is the difference in energy between the two triangular sublattices that comprise the honeycomb lattice of graphene. If $\Delta = 0$, as is normally the case, the energy dispersion becomes linear:

$$E(k) = \pm\hbar v_F |k|. \tag{1.2}$$

This is the reason graphene does not have a bandgap (See Figure 1.1[1]).

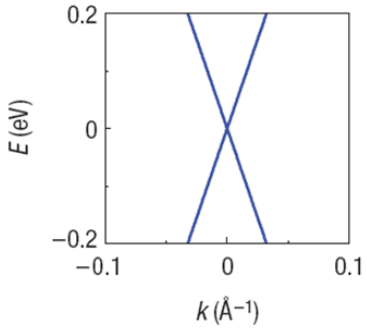

Figure 1.1: The linear energy dispersion of graphene. Note the lack of a bandgap.

1.1.2 Applications

Graphene's properties are not only interesting, but useful as well, and it is currently used in a wide variety of practical applications [9–16]. Graphene-based materials are utilized for their combination of strength and flexibility. The desirable electrical properties of graphene are most often exploited in nanoelectronics, such as graphene-based transistors, discussed further in Chapter 2. Graphene-based optical displays are an interesting example of using both the mechanical and electrical properties of the substance.

[1] Figure adapted from a talk slide of group member Dennis Huang.

Chapter 2

Graphene Nanoelectronics

Graphene nanoelectronics refer to any electrical device that incorporates graphene, typically built on the nanometre scale. These include a wide variety of objects of varying size, complexity, and purpose, including:

- Simple devices, such as the ones used in this project. These devices' only purpose is to allow a piece of graphene to be electrically contacted, so that electrical measurements of the graphene flake can be performed, usually to characterize the electrical properties of the flake. An example can be seen in Figure 2.1.
- Complex devices, also fabricated for research purposes. Often one requires a graphene flake of a precise size (and therefore etching of the flake is required) or wishes to incorporate additional features such as top gates. These devices are made in order to perform more precise or sophisticated measurements. [2]
- Practical purpose devices, such as ones outlined in Section 1.1.3. Graphene field-effect transistors, such as the ones studied in [9, 10] are likely the most prominent example.

[2] For example, see [17], where a top gate is used to tune the bandgap of bilayer graphene.

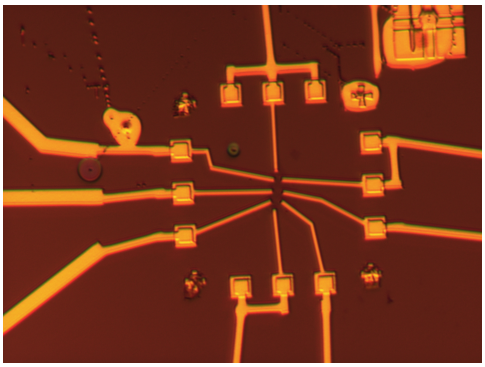

Figure 2.1: An example of a simple device. The graphene flake can be seen in the centre, and it is contacted by eight gold leads. This number is simply to ensure there are a variety of leads to perform 4-probe resistance measurements with, and in case some leads fail there isn't a danger of falling below four.

2.1 Fabrication

The fabrication of graphene nanoelectronics is a many-step process, outlined below. Quantitative specifics (such as equipment settings and other values) can be found in the Appendix.

2.1.1 Mechanical Exfoliation

In order to build a graphene device one must first obtain a monolayer flake of graphene on a substrate.[3] This is done through mechanical exfoliation. Silicon wafers (which naturally form a silicon oxide layer on their surface) are patterned with gold bonding pads and alignment marks and then broken into individual chips. Then, thin pieces of graphite (which molecularly are large stacks of graphene sheets) are attached to adhesive tape and the tape is pressed down onto the chip. When it is peeled away, some of the graphite remains on the tape while some remains on the chip. Since the bonds between carbon atoms within a layer of graphene are very strong, but the inter-layer bonds between sheets are very weak, the graphite splits easily and leaves a few layers of graphene behind. One must then examine the chip under a microscope and search for graphene monolayers (as opposed to bi-

[3]This step is described for completeness, but was never performed by me. It is done in batches, and I was able to simply take chips from these batches when needed.

or multi-layer flakes). One can tell the thickness of a flake by its colour relative to the substrate. In this sense, obtaining a good quality and good-sized graphene flake is left to chance. Microscope images of a graphene flake on the typical substrate can be seen in Figures 2.2 and 2.3.

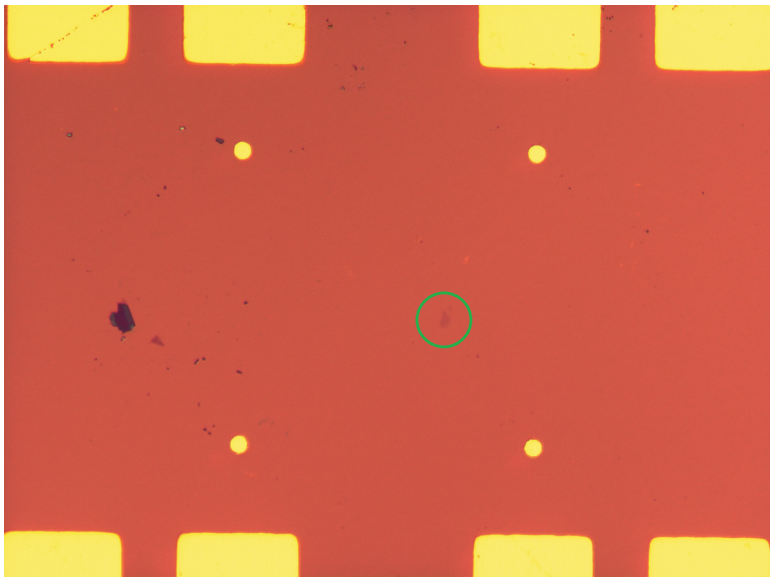

Figure 2.2: A microscope image of part of a chip. Gold bonding pads can be seen at the top and bottom of the image, and circular gold alignment marks are also present. A monolayer graphene flake is circled. Thicker flakes can be seen nearby.

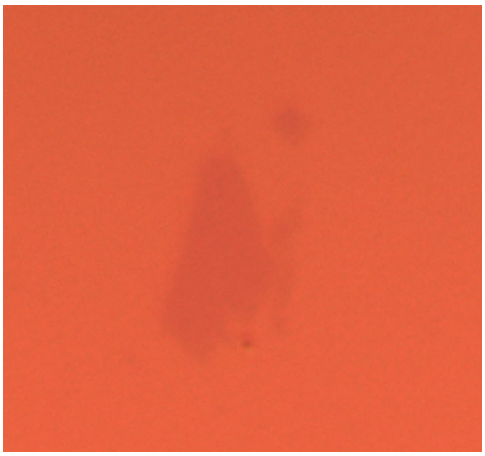

Figure 2.3: A monolayer graphene flake on a Silicon Oxide substrate. The contrast between them is not high, as the graphene is only one atom thick.

2.1.2 Device Design

Once an appropriate flake has been identified, the device must be designed. An image of the area surrounding the flake is taken and imported into DesignCAD after an alignment process. Then, one can literally draw wires from the pads towards the graphene flake at will. Typically, when there is space, one ends up with a spider-like pattern, as in Figure 2.11. Also, it is generally a good idea to design multiple paths from a pad to the destination, so that if one small area of the wire is ruined the pad is still electrically connected to where it should be.

2.1.3 Electron-Beam Lithography

Preparation

Once the design is complete it is time to perform the actual lithography. This is done in a cleanroom setting to avoid allowing particles that may otherwise land on the surface of the chip to interfere.

First, the chip is cleaned in acetone and dried (Figure 2.4). Then, it is placed in a spinner and a few drops of a polymer called PMMA are deposited on top. PMMA consists of long molecular chains. The spinner then spins the chip at a set angular frequency for a set duration. This spreads the PMMA over the chip in a particular known thickness, so that the exposure

rate of the Scanning Electron Microscope (SEM) to be used in a future step can be set accordingly. After the PMMA is spun onto the chip it is baked. (Figure 2.5)

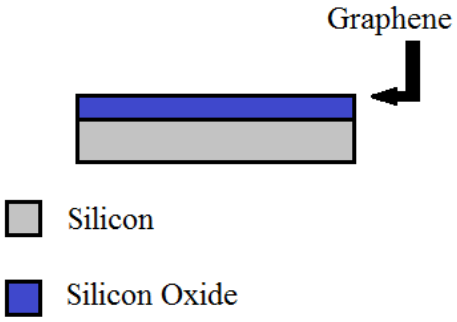

Figure 2.4: You begin with a (cleaned) chip that simply has graphene resting on top.

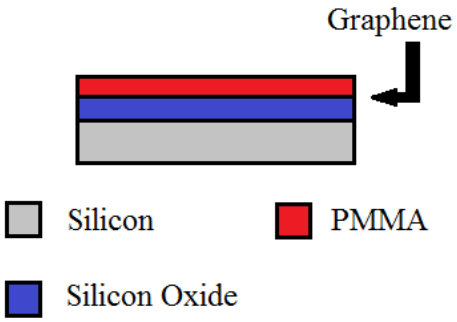

Figure 2.5: PMMA is spread over the entire chip using a spinner, and then it is baked.

The process is repeated a second time using a slightly different variety of PMMA. The two varieties have different strengths, so that when an area is exposed to the electron beam (see next section) the extent of the destruction of the polymers is different, resulting in 'trenches' with a different width near their top than their bottom.

Lithography with Scanning Electron Microscope

The PMMA-coated chip is then placed into the vacuum chamber of the SEM. The design file created earlier is loaded into the computer. Focussing of the electron beam and alignment of the sample stage must be done by hand. However, once the beam is focussed and the chip is aligned (via the gold alignment marks) the computer performs the actual exposure (Figure 2.6).

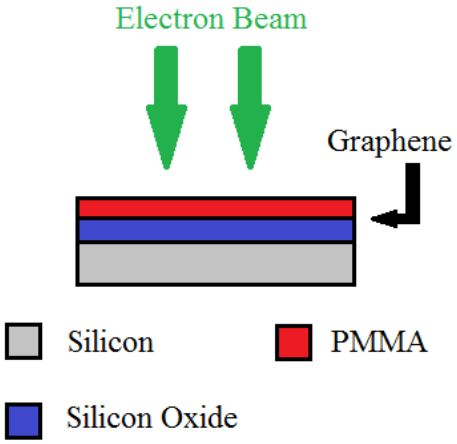

Figure 2.6: The chip is placed inside the SEM and the associated computer program provides the instructions necessary to guide the electron beam and draw out the pre-designed pattern.

The electron beam breaks up the long polymer chains of the PMMA in the areas exposed (Figure 2.7).

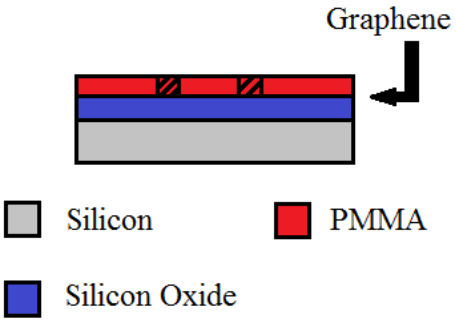

Figure 2.7: The polymers of PMMA that were exposed to the beam have been broken down into smaller molecules, whereas the unexposed PMMA retains its original structure.

After the exposure is complete, the chip is removed from the SEM's vacuum chamber and placed in a weak solvent. This solvent can dissolve the broken-down PMMA molecules but not the intact long strands. Thus, 'trenches' in the PMMA are left where the polymer was exposed to the electron beam. (See Figure 2.8)

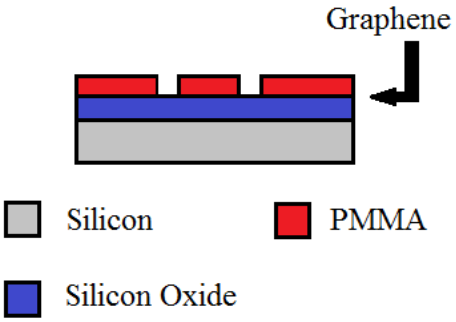

Figure 2.8: The entire chip is immersed in a solvent that is potent enough to dissolve the broken down chunks of PMMA but not the intact long polymers. This leaves 'trenches' in the PMMA in the exposure pattern.

Evaporation and Liftoff

After the use of the SEM the chip is placed in the top of a metal evaporator, which consists of a chamber that can be pumped to near vacuum containing tungsten boats used to vaporize metals. Gold is placed in one of the boats and heated until it evaporates. The gold atoms deposit themselves uniformly over the chip (Figure 2.9). The rate of deposition can be observed via a crystal monitor in the evaporation chamber, and thus specific thicknesses of gold can be deposited.

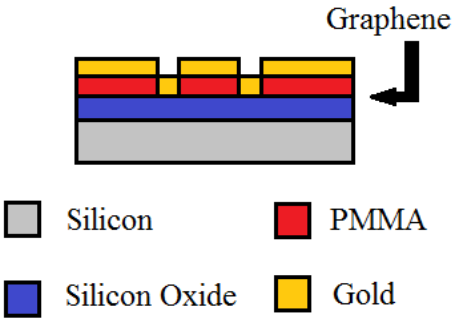

Figure 2.9: The chip is placed in a metal evaporator and gold is evaporated, which coats the entire chip in a thin layer of gold, filling the trenches.

After the gold deposition the chip is placed in hot acetone, which is a solvent that can dissolve the long strands of PMMA that were not exposed to the electron beam. With the PMMA gone, the gold that sat on top of it floats away from the chip. This may need to be encouraged with the use of a sonicator, a device that sends pulses through the beaker containing the chip, in the hopes that any gold that did not already float away will be knocked away. After this and a rinse in more acetone all of the unwanted gold is gone, leaving the situation in Figures 2.10 and 2.11. The entire process must be done twice. The second time there is more precision throughout the process, due to closer alignment marks and a thinner electron beam. One is finally left with a contacted graphene flake, as in Figure 2.12. The chip is now ready to be bonded.

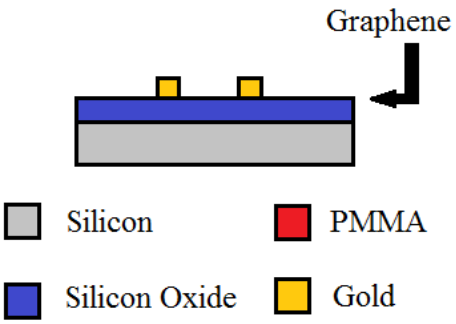

Figure 2.10: The chip is immersed in a stronger solvent, which is able to dissolve the intact PMMA. The gold that was deposited on top of the PMMA then floats away from the chip, whereas the gold that was deposited into the trenches is attached to the graphene/silicon oxide and remains as the desired nanowires.

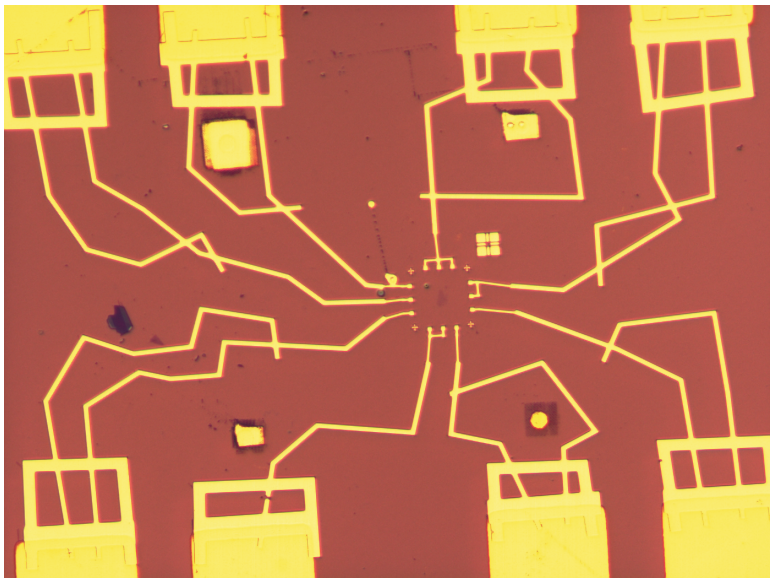

Figure 2.11: A chip after the first stage of lithography and evaporation is complete. Wires approach the graphene flake but do not contact it. Rather, they connect to a new set of small pads, with their own alignment marks. This is done so the mold for the wires close to the graphene can be created with more precision.

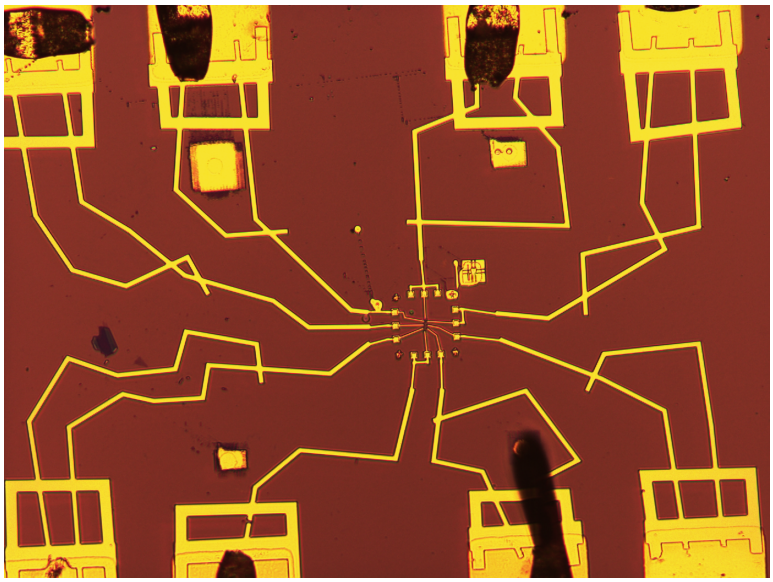

Figure 2.12: A chip after the second stage of lithography and evaporation is complete. Small wires now connect the small pads directly to the graphene, and so the large bonding pads are finally connected to the flake.

2.1.4 Bonding

The final stage in producing a measurable device is bonding. First, the bottomside of the chip is scratched in order to expose the silicon beneath the silicon oxide layer. With the silicon exposed, the chip is glued to a chip carrier using silver paste. In this way, the silicon beneath the silicon oxide that the graphene sits on can also be electrically contacted, which is essential for the measurements described in the next section.

After the chip is in its carrier, macroscopic gold threads are attached to pads on the carrier and to the gold pads of the device, electrically connecting them. This is done using a bonder (pictured in Figure X). The graphene devices can now be accessed by macroscopic measurement apparatus via the chip carrier. See Figure 2.13 for an image of the bonding wires.

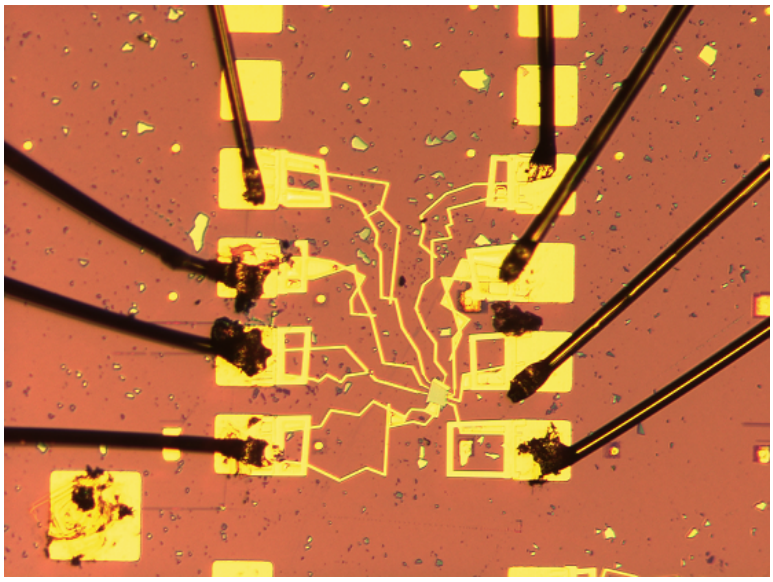

Figure 2.13: An image of bonds to a device. The bonding wires are first attached to the chip carrier pads, and then drawn over to the device bonding pads, where they are melted together to form electrical contact.

2.2 Characterization Measurements

As discussed above, the principle purpose of the simplest graphene nanoelectronic devices is to facilitate electrical measurements of the graphene flake(s) involved. These measurements can characterize the flake in a few important ways, as discussed below.

2.2.1 Method

Preparation

There are three important steps to take before a proper measurement can be made. First, the device should be annealed. This is a process where the device is heated in the presence of forming gas (a mixture of hydrogen and nitrogen). Figure 2.14 shows the setup. A low temperature anneal (200 C) is useful for removing water from the surface of the device due to exposure to the air. A higher temperature anneal (400 C) can burn away PMMA residue left on the graphene as well. Annealing immediately before a measurement

can drastically improve the results due to its ability to eliminate unwanted surface effects (See the difference between Figures 2.17 and 2.18).

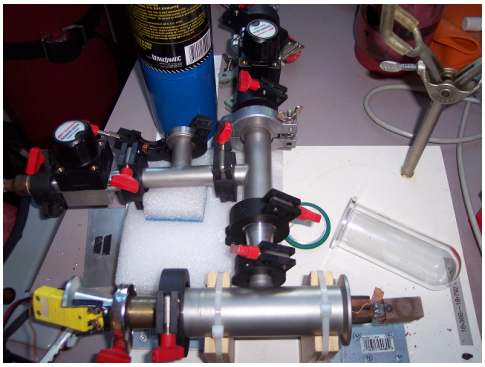

Figure 2.14: The lightbulb annealer used in this project. The chip is placed on the copper sheet in the bottom right, which surrounds a projector-bulb. The voltage to the bulb can be adjusted, which adjusts the amount of heat it releases and therefore the temperature of the chip, which is constantly measured. The chip and heat source can be encased in a glass tube and put into vacuum or into forming gas.

After annealing, the sample is quickly placed in a dunker stick, which is then sealed and pumped down to near vacuum. This is to avoid undoing what the annealing accomplished and letting water settle on the graphene again. See Figure 2.15 for an image.

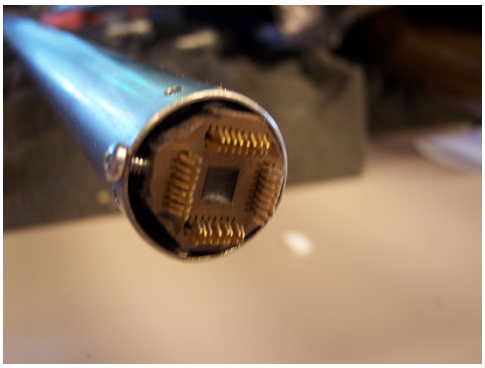

Figure 2.15: The end of the dunker stick, showing the pins that connect to chip carriers. Wires for all 32 possible leads run through the stick to the measurement devices. The stick is placed in a sheath to seal it and pump down to vacuum.

A small amount of helium is then let into the dunker stick, and the stick is then immersed in liquid nitrogen. The helium serves to carry thermal energy from the graphene. The liquid nitrogen would not be able to cool the sample very quickly without it. Since helium is inert there is no danger of it affecting the measurements. Measurements are done at 77 K to reduce noise.

Measurement

The principle measurement performed on a device is a measurement of device resistance vs. a changing back gate voltage. Resistance is measured using a Lock-In Amplifier, with either a 2-probe or a 4-probe setup. All of the data presented here was taken using a 4-probe setup to ensure only graphene resistance and not contact resistance was being measured.

The resistance of a substance depends in part on its charge carrier density n. If there are more electrons (or holes) in the graphene flake, current will flow more easily. One can control n via the application of a voltage to the previously mentioned back gate. When no voltage is applied, the charge carrier density in the graphene is unchanged. However, applying a voltage to the back gate causes charge of the appropriate sign to build up in the silicon. This induces charge of the opposite sign in the graphene (See Figure 2.16). These extra charges can also serve as charge carriers. So in theory, as one increases V_{BG} one increases n, which in turn lowers the resistance R

of the graphene flake.

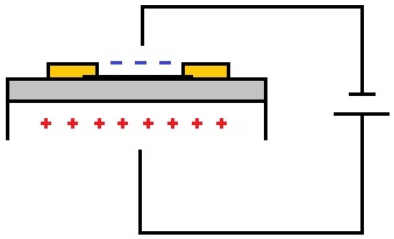

Figure 2.16: The effect of applying a voltage to the back gate of a device. Charge builds up in the silicon due to the voltage, which in turn induces opposite charge in the graphene. These new charges can easily serve as charge carriers, increasing the effective charge carrier density n of the flake.

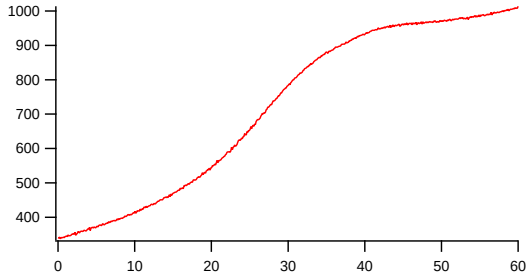

Figure 2.17: A measurement of R (in ohms) vs. V_{BG} (in volts), without having annealed the device prior to measurement.

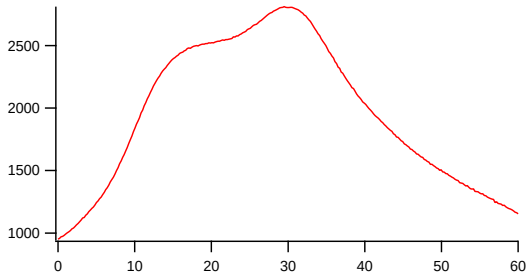

Figure 2.18: Another measurement of R (in ohms) vs. V_{BG} (in volts) of the same device measured in the previous figure, this time after having annealed the device prior to measurement. Note how the peak shifts drastically towards the 0V point.

2.2.2 Analysis

The peaks obtained when performing the described measurements are called Dirac peaks. Their shape contains much information regarding the characteristics of the graphene.

Inhomogeneity

The 'inhomogeneity' is not a numerical property of a graphene flake, but a sense of how inhomogeneous a flake is can still be obtained from these measurements. It was mentioned above that, in theory, increasing V_{BG} should increase the charge carrier density n, and therefore reduce the resistance R of the graphene flake. However, as can be seen in both Figure 2.17 and 2.18, the R of the graphene actually *increases* when V_{BG} is increased. The explanation is simple: there are excess charges or charge traps present in the flake due to inhomogeneity. These may come from water on the surface from the brief time the devices are exposed to air, or, more often, from charge traps in the silicon oxide. The oxide is not uniform, crystalline SiO_2, but may have areas of SiO_3 or SiO, which introduce electrons or holes to the graphene. Thus, when $|V_{BG}|$ is increased, it *does* introduce more electrons (or holes) to the graphene flake, but at first these only serve to cancel out the excess holes (or electrons) that were already present in the flake and able to carry charge. Therefore increasing V_{BG} actually serves to reduce n and therefore increase R.

However, as V_{BG} continues to increase, eventually a turning point is

reached. This happens when the new electrons (or holes) have finally completely cancelled out the intrinsic holes (or electrons). From that point forward, adding even more electrons *does* serve to increase n, and so R decreases as expected. This is what causes the peak structure observed in measurements.

The location of the Dirac peak (i.e. the value of V_{BG} where R is maximal) can therefore tell us 'how inhomogeneous' the flake is. A perfectly homogeneous flake would have its peak at 0 V. The further the peak is from that point, the more charges there are to overcome, and so the more inhomogeneous the graphene is. One can notice that the peak shifts much closer to 0 V if annealing is done before measurement (See Figures 2.17 and 2.18). This is because the annealing process removes the water and residue from the surface of the flake, which contributed to inhomogeneity. However it doesn't effect the inhomogeneity of the substrate, which is why the peak doesn't move all the way to 0 V.

The FWHM (the width of the peak at half its maximum value) is another way to read off the amount of charge inhomogeneity in the device. A thinner peak corresponds to less charge inhomogeneity.

Mobility

Perhaps the most important characteristic of a graphene flake is its electron mobility. Mobility is a measure of how easily electrons (or holes) can travel through a solid. As discussed Chapter 1, one of the properties that makes graphene so interesting is its very high mobility.

Electron mobility μ is defined as follows

$$\mu = \frac{\sigma}{ne} \tag{2.1}$$

It is expectedly related to the conductance σ (since conductance is also a measure of how easily electrons can travel through a solid), as well as the charge carrier density n and the elementary charge e.

One can measure the mobility of a graphene flake by manipulating the data that gives the Dirac peaks above. First, it was asserted that V_{BG} is proportional to n (if the peak is shifted to 0 V). Thus, after scaling the horizontal axis one can plot the data against n rather than V_{BG}.

Secondly, R is related to the resistivity ρ of the graphene through the flake's aspect ratio, which in turn is equal to $\frac{1}{\sigma}$. Thus, after scaling the vertical axis and inverting the values one can obtain a plot of σ vs. n, as in Figure 2.19.

From the definition above,

$$\sigma = \mu e n \tag{2.2}$$

and therefore the slope of a graph of σ vs. n, multiplied by e is the mobility μ of the flake.

A perfect flake will exhibit a 'V' shape, with two linear portions of the same slope, as in theory the electron mobility and hole mobility of graphene are equal. However, in a flake with inhomogeneity, the graph of σ vs. n will not necessarily be linear near the peak, nor have equal slopes on either side of the peak when it does become linear. This can be seen in the example shown in Figure 2.19, which is not a particularly homogeneous flake. However, despite this the electron mobility (calculated from the positive slope) of this flake was quite good, with $\mu \approx 4000 \frac{cm^2}{Vs}$.

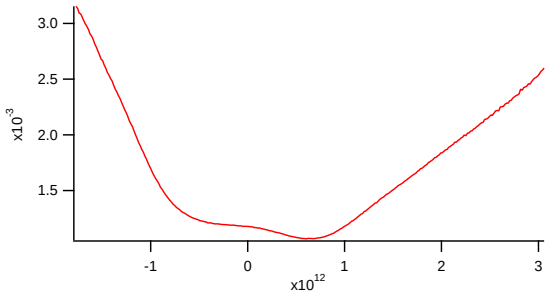

Figure 2.19: The same dataset shown in the previous two figures, but with the axes manipulated in order to extract the mobility. The horizontal axis is now charge carrier density n, and the vertical is now $1/R$. The mobility can then be obtained from the slope of the linear sections.

Chapter 3

Gold Deposition

The main experiment done to the devices fabricated in this project involve the deposition of sub-monolayer amounts of gold onto a flake of graphene and an investigation of the effects this has on electronic transport.

3.1 Theory and Motivation

Graphene is comprised of a single atomic layer, so all charge carriers involved in conduction are automatically always in contact with the surface of the material, unlike in traditional conductors, where many travel through the material's body. This makes surface effects an extremely important aspect to consider in terms of graphene conduction, as they are especially able to harm transport properties.

However surface effects could also potentially be utilized for interesting or valuable purposes. For example, there exist predictions and experiments that suggest depositing small amounts of gold atoms onto the surface of graphene can induce strong spin-orbit interaction in the electrons within [18]. This means that as an electron moves within the graphene its spin is quickly rotated. This is interesting in its own right, but is also the basis for 'spintronic' transistors.

Furthermore, studies show that various amounts of gold deposition onto the surface of graphene can drastically effect its mobility and inhomogeneity. For example, Y. Ren et al. show that the deposition of few-monolayer amounts of gold on the surface of graphene shifts the Dirac peak of the sample [19]. This is explained by the differing work functions of gold and graphene 3.1. Since the work function of gold is higher, it takes more energy to remove an electron from a gold atom than a carbon atom in graphene. Thus, it is energetically favourable for some of the electrons in graphene to be donated to the gold atoms. This has the effect of reducing the number of negative charge carriers, shifting the Dirac peak in the positive direction (See Figure 3.1).

Graphene	4.6
Gold	4.8

Table 3.1: The differing work functions of graphene and gold [19]. The difference means that electrons will favour being attached to gold over graphene, which causes the graphene to donate some of its charge carriers, shifting the Dirac peak.

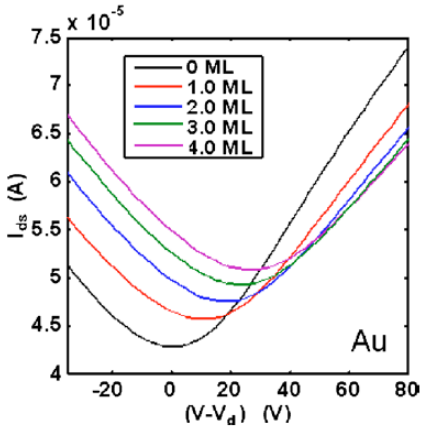

Figure 3.1: Results from [19], where few-monolayer amounts of gold were deposited on the surface of graphene. The Dirac peak shifts to the right as more gold is deposited. This is explained by the differing work functions of gold and graphene.

The effects of depositing a much smaller amount of gold appear to be very different [20]. The Dirac peak is shifted in the opposite direction, and the mobility is decreased (See Figure 3.2).

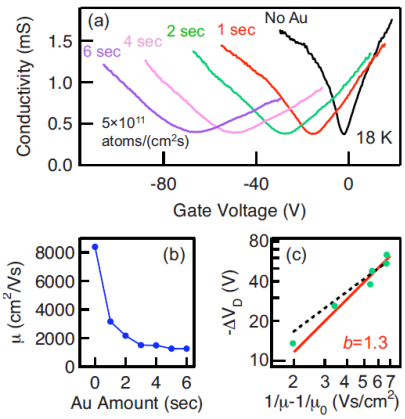

Figure 3.2: Results from [20]. Submonolayer (on the order of 1000^{th}s of monolayers) gold was deposited at cryogenic temperatures. a) The effect on the location of the Dirac peak. Gold amounts are measured by the amount of time the sample was exposed to gold that was evaporating at a very low rate. The peak shifts the opposite direction of the previous experiment, so something more complicated must be happening. b) The mobility as a function of gold deposited.

It has also been observed that the effects shown in Figure 3.2 are irreversably undone once the sample is brought to room temperature (See Figure 3.3). This can make measurement and reproducability difficult without the proper equipment.

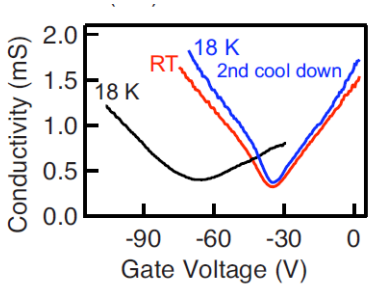

Figure 3.3: The effects shown in Figure 3.2 are undone when the sample is brought to room temperature, and do not reappear if recooled.

The apparent discrepancy of the work in [19] and [20] might be explained by the vastly differing amounts of gold deposited on the graphene. This project does its own investigation of the effects of submonolayer gold deposition on the surface of graphene nanoelectronic devices.

3.2 Method

In order to deposit an appropriate amount of gold with the sample at an appropriate temperature, a few modifications to the metal evaporator had to be made.

3.2.1 Liquid Nitrogen Cooling System

In order to keep the sample at 77 K during the evaporation, a new stage for the sample had to be constructed. The result is pictured in Figure 3.4. The chip is attached to the bottom of the copper plate, which is in thermal contact with copper tubes leading outside the evaporator. Liquid nitrogen can be pumped through the tubes to cool the plate, and ultimately the sample. It possible to flow the liquid nitrogen through at a steady rate throughout the evaporation.

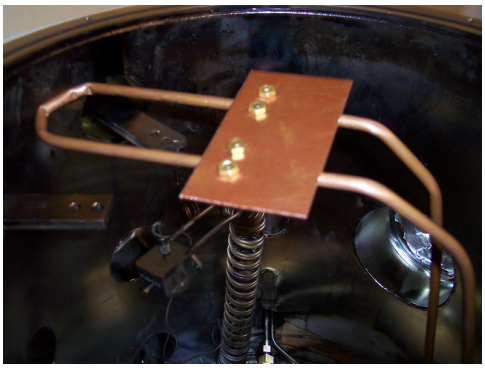

Figure 3.4: The cooling system for the remodelled evaporator. The sample is attached to the bottom of the copper plate. Liquid nitrogen is pumped through the tubes from outside the chamber while depositing gold. This keeps the sample at 77 K throughout the process.

3.2.2 Rotating Slit Shutter

A new shutter had to be designed and built for the evaporator. The original shutter was simply a metal plate that could be moved to either cover the sample or expose it to the evaporating gold. This is sufficient for large evaporations, such as those done when fabricating a device. Once the evaporation rate is steady, the shutter is opened and the amount deposited simply depends on how long it is left open and the evaporation rate. Evaporation in this way usually takes 10 to 20 minutes.

However, in order to deposit an amount of gold equivalent to ≈0.1% of a monolayer (roughly 1 mÅ) the shutter would have to be opened and closed far more quickly and precisely than was possible.

The new shutter allows for depositions of this magnitude. It shields the sample from the evaporating metal regardless of its position, except for a small slit of width $w = 1.6mm$. With this design, rather than having simply and 'on' and 'off' state, the slit can be quickly passed over the sample to produce a very low effective exposure time. Once the slit has passed the sample is again covered (See Figure 3.5).

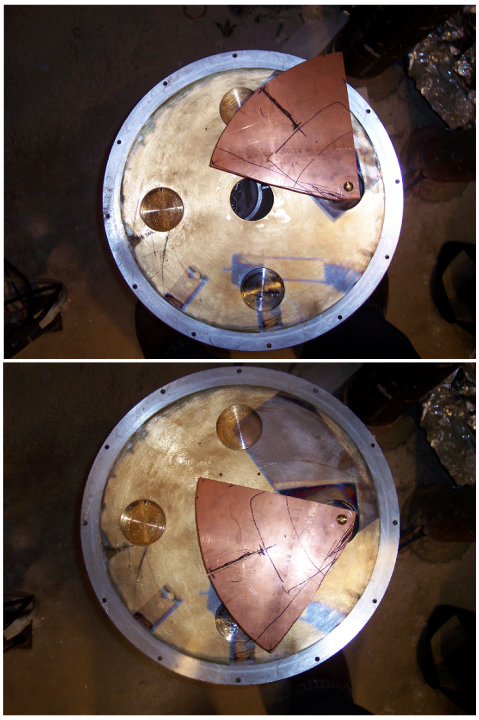

Figure 3.5: The new evaporator shutter. TOP: The chip will be aligned roughly with the visible hole in the evaporator lid when everything is put together. BOTTOM: The shutter can be rotated to quickly pass the slit over the sample.

The effective exposure time t can be calculated as follows.

$$t = \frac{w}{v} \tag{3.1}$$

where w is the slit width and v is the velocity of the slit as it passes over the sample. Furthermore,

$$v = \frac{d}{T} \tag{3.2}$$

$$T = \frac{\theta}{\omega} \tag{3.3}$$

where d is the total distance the slit moves (or at least the part of the slit that will pass over the small graphene device) when the shutter is rotated

an angle θ and T is the time it takes for the shutter to rotate that same angle θ at a rate ω rad/s. However

$$d = \theta R \tag{3.4}$$

where R is the distance from the pivot point of the shutter to the sample. Therefore

$$v = \frac{\theta R}{\theta \omega} = \frac{R}{\omega} \tag{3.5}$$

and so

$$t = \frac{w\omega}{R} \tag{3.6}$$

Then, the thickness h that is evaporated is

$$h = rt = \frac{rw\omega}{R} \tag{3.7}$$

where r is the rate of evaporation. Therefore, using the parameters in Table 3.2, one can calculate that $h \approx 6.52$ mÅ.

r	0.5 Å/s
w	1.6 mm
R	11.5 cm
ω	1 rad/s

Table 3.2: The parameters used to deposit a submonolayer amount of gold onto a graphene nanoelectronic device. w and R are fixed by the geometry of the shutter. r is as low a rate as one can evaporate at and be sure only gold is being evaporated. ω is estimated. One improvement to the system would be to have a rotary encoder measure ω rather than trying to time it by hand.

3.3 Results

The results of 4-probe resistance vs. back gate voltage measurements for a particular graphene device are reproduced below. Figure 3.6 shows the results before gold deposition[4], and figure 3.7 shows the results of an identical

[4]Figure adapted from a graph produced by Ali Khademi, a group member

measurement (same flake and contact probes) after gold was deposited. A clear shift in the location of the Dirac peak can be observed.

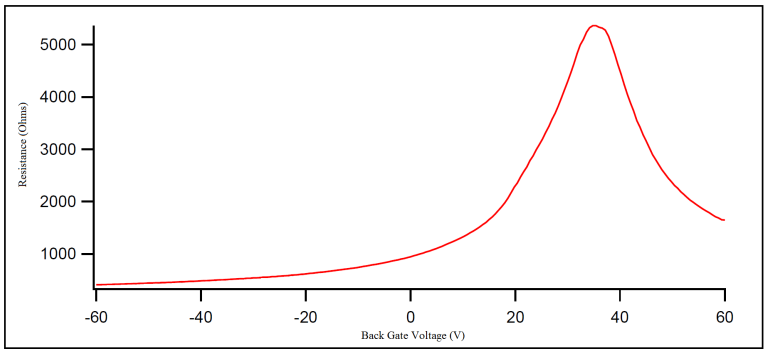

Figure 3.6: The result of the back gate voltage scan before gold was deposited. Note the position of the peak at slightly less than 40 V. The electron mobility was calculated to be $\approx 2000 \frac{cm^2}{Vs}$ from this data.

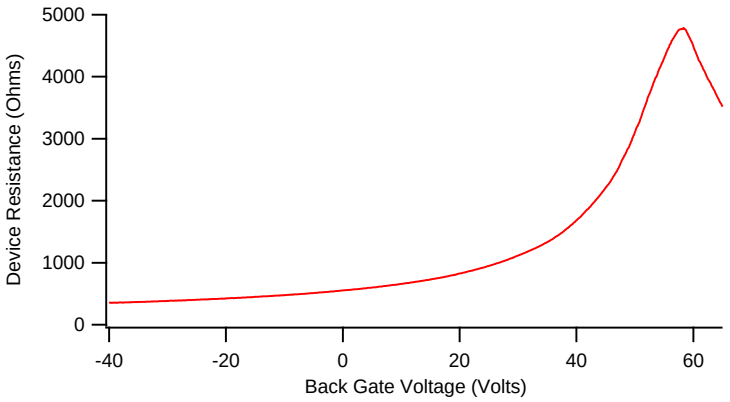

Figure 3.7: The result of a back gate voltage scan similar to the previous figure, done with the same contacts of the same flake, after a submonolayer amount of gold was deposited onto the graphene at 77 K. The peak has shifted roughly 20 V compared to the previous measurement.

Applying the methods discussed in Chapter 2, the mobility can be calculated from a modified form of this data (Fig 3.8). Most of the data lies to the left of the peak, and so the electron mobility cannot be calculated very

precisely. Nevertheless, an estimate of $\approx 2000\frac{cm^2}{Vs}$ can be obtained. This is the same estimate as before gold deposition.

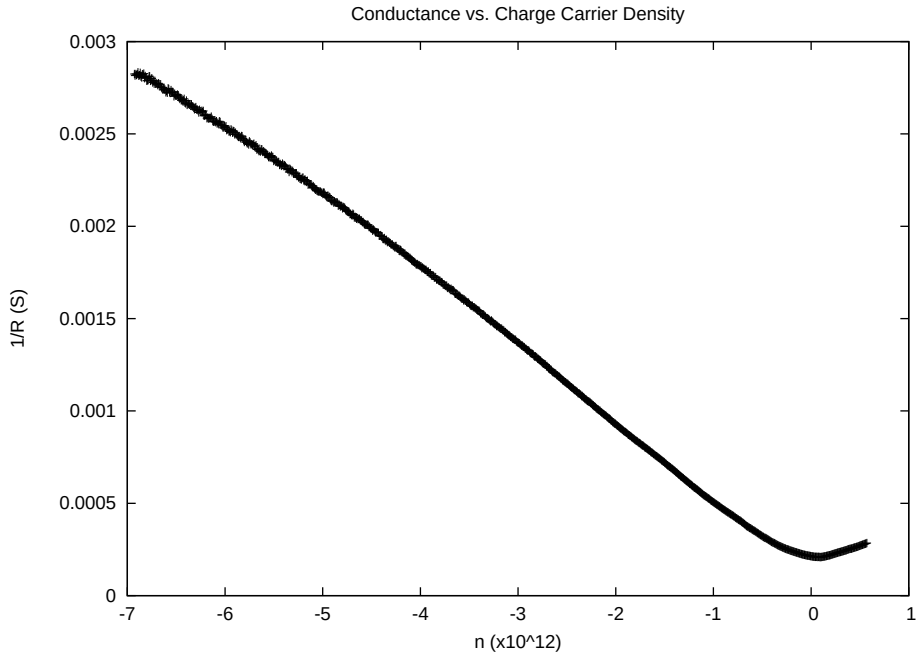

Figure 3.8: The data presented in Figure 3.7 manipulated to allow for a mobility calculation. Most of the data in on the hole side, so the estimate of electron mobility is not precise.

Disclaimer These results are very preliminary. Firstly, only one device was tested in this way, though it was tested using a variety of its probes and the results are consistent between those measurements. Secondly, it is possible that water is the cause of these shifts, as opposed to the deposited gold. This is suspected because, due to the nature of the experiment, the device cannot be annealed immediately before measurement. It was annealed before being placed in the evaporator chamber (which is filled with nitrogen gas when not pumped to vacuum), but after the gold deposition it had to be immediately placed in the dunker stick for measurement (which was then also pumped to vacuum, and cooled to 77 K). In theory, the chip should not be exposed to water while in the evaporator, and so effectively it is only exposed to air for roughly twice the time that a regular chip is

between annealing and measurement. Therefore, it is unlikely water could account for the entire change, but it does likely play some role. The effects of annealing after gold deposition have not yet been tested. Depending on the temperature it may or may not seriously effect the deposited gold.

Chapter 4

Conclusions and Future Work

4.1 Conclusions

The results in Section 3.3 suggest that gold deposited in the amounts discussed shifts the Dirac peak of the graphene flakes in the positive direction, as in [19]. This suggests the different-work-functions explanation to be valid. However, the amount of gold and the conditions in which it was deposited are much more similar to those in [20], yet the results do not compare at all. This may be due to the fact that the sample was briefly heated to room temperature before being re-cooled for measurement. As shown in Figure 3.3, the effects of gold deposition are irreversably undone when the sample is heated. Thus, it is reasonable to suggest that the gold deposited in this experiment initially produced results similar to those of [20] but, since the sample had to be heated due to apparatus restrictions, the effects were lost. The effects therefore resemble those in [19], yet far more gold was deposited in that experiment, and the Dirac peak experienced no shift from it's original point after reheating in [20]. This ambiguity requires much further experimental work to resolve.

4.2 Future Work

Further testing of the effects of gold deposition is certainly required to reach a true conclusion.

First, the effect of a gentle anneal to desorb water after the gold has been deposited should be investigated. Does it change the effect the gold has? Does it change the results significantly at all, suggesting water played a large role? Or do the results remain similar, suggesting water involvement was indeed negligible, as with a normal measurement.

Second, the effects of varying thicknesses of gold should be investigated. Does twice the gold produce twice the change? Also, if a gold is deposited,

and the chip is then measured, can another layer of gold be deposited even though the previous layer was twice brought to room temperature from 77 K? That is, would the results be different if twice the gold was deposited in the initial deposit at 77 K as opposed to over two deposits? Unfortunately, as important a fact this is to understand, a large number of finished devices would be required to fully investigate it, and time did not allow for that many devices to be fabricated.

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Fabrication Details

Below are some quantitative fabrication details.

- 1st stage lithography wires are typically designed to be $4\mu m$ wide, and 2nd stage wires are typically $500nm$ to $1\mu m$.
- Spinners are set to revolve at 5000rpm for 45 seconds. This spreads the PMMA to a layer $\approx 100nm$ thick. For contrast, the oxide layer that forms on the surface of the silicon chip is $\approx 300nm$.
- Chips with PMMA are baked at $180°C$ for 10 minutes.
- The electron beam current of the SEM is typically 170 pA for 1^{st} stage and 20 pA to 60 pA for 2^{nd} stage. In either case, other computer-decided settings such as beam dwell time ensure that the total exposure amount is 180 units/unit, for all patterning.
- The 'weak' solvent used to dissolve the broken-down PMMA is a mixture of methyl isobutyl ketone (MIBK) and isoproponal alcohol (IPA).
- When evaporating, a small layer of chromium is actually deposited before the gold. This helps the gold make a good contact with the chip. For 1^{st} stage, 2 - 5 nm of chromium are deposited before 75 - 100 nm of gold. Deposition rate for the gold is typically 1.2 to 1.5 Å/s. Chromium deposition rate varies but is smaller. For second stage only 0.5 nm of chromium are deposited, with 50 - 100 nm of gold following.
- For liftoff the chip is placed in $80°C$ acetone for 10 minutes, then sonicated for a few seconds if necessary. The chip is then rinsed with acetone as it is removed from the beaker and then set in IPA for another 10 minutes.
- The chip and chip carrier must be heated to $100°C$ for 10 minutes and then $200°C$ for 50 minutes in order for the silver paste to properly bond the two together.
- Annealing is done in forming gas at pressures of 20 mmHg to 60 mmHg.