The VHSRD1: A 6-Channel, 250V, very high slew-rate driver circuit for stick-slip piezoelectric motors

Comprehensive user’s Manual (version 1.0)

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**Introduction**

The VHSRD1 module was developed to create the high current, high slew rates waveforms necessary to drive shear-piezo based stick-slip motors. The module can provide output voltages of at-least 250V\(^1\), slew rates as high as 5MV/s and peak currents in excess of 0.5 A. The intended application for this module is driving the coarse approach linear motor in Scanning Tunneling Microscopes.

The module has 6 channels and uses a highly generic triggering scheme consisting of an independent 5V logic trigger for each channel. Therefore it may be possible to adapt the device to suit a variety of applications requiring fast voltage transitions and moderately high instantaneous currents.

The purpose of this document is to give an overview of the design and operation of the VHSRD1 as well as a detailed history of its development. The first few sections of the user’s manual present the basics of operation of the device in a concise manner that should enable an end-user with minimal training to operate the device with ease. The schematics, developer’s notes and references should assist a technician in trouble-shooting the device or facilitate a future developer in improving the design.

The module and this documentation were developed as a UBC ENPH 479 project course project during the 2011-2012 winter term. The project sponsor was Dr. Yan Pennec of the UBC Scanning Probe Microscopy group; the project work was undertaken by Ben MacLeod, an undergraduate in his 5th year of engineering physics at the time.

This document should be accompanied by an archive containing all the computer files and miscellaneous documents associated with the project: CAD files, computer code, excel calculations, references, component data sheets, communications (proposals, reports, presentations and parts orders). This archive may also be obtained by emailing the author at [email protected]. The project notebook should also be available upon request from the University of British Columbia Engineering Physics project lab.

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\(^1\) Theoretically the module should be able to provide output voltages of up to 500V. However testing has only been performed up to 250V
1 User’s manual

1.1 Safety warnings

1.1.1 Direct shock Hazard

If it becomes necessary to open the case of the VHSRD1 for trouble-shooting purposes, be aware of the fact that the IRF840 MOSTFETs inside have flanges which are tied to the drains of the devices. This results in some of these flanges being connected to the HV line. Avoid making oscilloscope probe measurements inside the housing when the HVIN line is at high voltage. If making such measurements is necessary, **take extreme care to avoid coming into contact with the transistor flanges as such contact may result in electric shocks.**

![Figure 1: IRF840 electrified flanges safety warning](image)

1.1.2 Unlimited peak output current Hazard

The outputs of the VHSRD1 are connected through transistors to the HVIN line and to a 1uF auxiliary capacitor (C5) charged to the HVIN line voltage. **THERE IS NO CURRENT LIMITING CIRCUITRY ON THESE OUTPUTS.**

This results in two major hazards:

1. Electric shock hazard: The peak current that can be delivered by the capacitor is extremely high. Combined with the high capacitor voltages (up to 250V) this presents an electrocution hazard.
2. Damage to equipment: Avoid short-circuiting the outputs of the VHSRD1. Depending on the trigger logic state, this may create a virtual short-circuit of the HV line to ground through the IRF840 (<1 Ω). This may damage the device supplying the HV line and/or the IRF840 switch.
1.2 Specifications / Data sheet

1.2.1 Inputs, outputs and Pin-out

Figure 2: Pin assignments for the inputs and outputs of the module. The labels used here match the designators on the circuit schematics and PCB layouts. Trig1 controls channel 1, Trig2 controls channel 2 and so on. The 15V power for the switching circuitry is intended to be supplied by a FEMTO PS-15-3-L power supply. Accordingly, an appropriate LEMO connector needs to be added to the red and green wires. Note that GND is common to both the HV coaxial outer conductor and the green wire.
1.2.2 Absolute maximum ratings

As the working prototype of the VHSRD1 which was produced is required for use by the Scanning Probe Microscopy group, it was not possible within the time-frame of the project to perform full stress tests of the module. Therefore, the absolute maximum ratings given below are only estimates developed based on the ratings of the relevant subcomponents of the VHSRD1 and. The device may not function for all voltages within these ranges but will probably not be damaged by them.

<table>
<thead>
<tr>
<th>Input</th>
<th>Min. Voltage</th>
<th>Max. Voltage</th>
<th>Critical Component</th>
<th>Justification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc (referenced to GND)</td>
<td>-0.3V</td>
<td>20V</td>
<td>IR2111 Gate Driver</td>
<td>Min/max : Voltage limits for Vcc in IR2111 datasheet</td>
</tr>
<tr>
<td>TRIG1-TRIG6 (referenced to IsolatedGND)</td>
<td>-6V</td>
<td>16.2V</td>
<td>H11L1M opto-coupler</td>
<td>Min: Reverse emitter voltage in H11L1M datasheet</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Max: 60 mA Continuous forward current thru emitter in H11L1M datasheet</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(16.2V/270ohm = 60 mA)</td>
</tr>
<tr>
<td>HVIN (referenced to GND)</td>
<td>0(^2)</td>
<td>500 V</td>
<td>IRF840 Transistor</td>
<td>Min:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Max: Drain to source breakdown voltage in the IRF840 datasheet</td>
</tr>
</tbody>
</table>

Table 1: Absolute maximum ratings for the VHSRD1
The VHSRD1 has NOT been tested to these ratings; they are theoretical ratings based on the ratings of the components contained within the module.

1.2.3 Recommended operating conditions

The VHSRD1 should operate properly for the conditions given in the table below.

<table>
<thead>
<tr>
<th>Input</th>
<th>Min. Voltage</th>
<th>Typ. Voltage</th>
<th>Max. Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc (referenced to GND)</td>
<td>-</td>
<td>15V</td>
<td>-</td>
</tr>
<tr>
<td>TRIG1-TRIG6 (referenced to IsolatedGND)</td>
<td>-</td>
<td>5V</td>
<td>-</td>
</tr>
<tr>
<td>HVIN (referenced to GND)</td>
<td>0</td>
<td>-</td>
<td>250 V</td>
</tr>
</tbody>
</table>

Table 2: Recommended operating conditions for the VHSRD1
The VHSRD1 has been successfully operated under these conditions.

\(^2\) DO NOT ATTEMPT TO OPERATE THE DEVICE WITH NEGATIVE HV VOLTAGES
1.2.4 Performance ratings

Performance tests using 3.3nF load capacitors indicate that the VHSRD1 can drive relatively high currents into capacitive loads at extremely high slew rates. The tests performed to obtain these results are discussed in section 2.5

<table>
<thead>
<tr>
<th>Performance Metric</th>
<th>Value</th>
<th>Performance Metric</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage range</td>
<td>350 V (250V base + 100V overshoot)</td>
<td>Voltage range</td>
<td>300 V (250V base + 50V overshoot)</td>
</tr>
<tr>
<td>Rise time</td>
<td>750 ns</td>
<td>Rise time</td>
<td>500 ns</td>
</tr>
<tr>
<td>Slew rate</td>
<td>4.67e8 V/s</td>
<td>Slew rate</td>
<td>6.00e8 V/s</td>
</tr>
<tr>
<td>Capacitive load</td>
<td>3.3 nF</td>
<td>Capacitive load</td>
<td>3.3 nF</td>
</tr>
<tr>
<td>Average current output per channel during rise time</td>
<td>1.54 A</td>
<td>Average current output per channel during rise time</td>
<td>1.98 A</td>
</tr>
</tbody>
</table>

Table 3: Performance metrics for the low to high transitions produced by the VHSRD1 under different test conditions

Figure 3: rising and falling output waveforms for the VHSRD1 under different test conditions

The top two waveforms are for a single channel trigger while the bottom two waveforms are for all 6 channels triggered at once.

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Defined here as time from voltage minimum to voltage maximum
1.3 Details of operation of the VHSRD1

The following sections outline the function, implementation and operation of the VHSRD1 module.

1.3.1 What it does

The VHSRD1 takes an arbitrary voltage input (tested to 250V, nominally up to 500V) and adds high-speed edges (~5 MV/s) to it through the use of a switching circuit. A 1uF charge reservoir allows high peak currents to be delivered over this time, making the device suitable for driving capacitive loads. 6 output channels, each with an independent trigger allow the device to produce a cascade of waveforms with customizable timing, appropriate for driving various types of stick-slip piezoelectric motors.

Depending on the trigger state, the outputs of the device either follow the arbitrary voltage input (trig. High) or remain at 0V (trig. Low). Thus, two types of waveforms can be produced, either with fast edges that go from 0V to the arbitrary input level or from the arbitrary input level to 0V. These occur when the trigger state is changed. Examples of these two types of waveforms are shown in Figure 4.

![Figure 4: The two types of output waveforms that can be generated using the VHSRD1. Note how the output waveform tracks the input waveform when the trigger is high.]

Independent trigger circuits allow the VHSRD1 to generate a cascade of output waveforms with arbitrary timings. With an appropriate input waveform and trigger sequence, all of the parameters in Figure 5 are adjustable. Naturally the time-reverse waveform cascade is also possible.

![Figure 5: Adjustable parameters of the output waveform cascade]

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4 THE DEVICE HAS ONLY BEEN TESTED TO 250V. 500V is the maximum operating voltage specified for the IRF840 switches.
5 Slew-rate performance will decrease as the capacitive load increases.
1.3.2 How it works

To add fast edges and increased instantaneous current to the output of a HV amplifier\(^6\), a circuit which is functionally equivalent to the circuit shown in Figure 6 is used.

![Functional equivalent of the switching circuit used to produce the output waveforms](image)

*Figure 6: Functional equivalent of the switching circuit used to produce the output waveforms*

The HV AMPLIFIER is not included in the circuit. This image was taken from the work of Hudson et. al. at MIT\(^1\)

This circuit works as follows:

1. The auxiliary capacitor \(C_a\) acts as a charge reservoir, buffering the output of the HV amplifier so that the large instantaneous currents necessary to quickly charge the piezo can be provided\(^7\)
2. The truth table for the state of the switches based on the trigger level is:

<table>
<thead>
<tr>
<th>Trigger state</th>
<th>High</th>
<th>Low</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch 1 state</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>Switch 2 state</td>
<td>OFF</td>
<td>ON</td>
</tr>
</tbody>
</table>

Basic configurations of the HV amplifier output and trigger timings for producing both forwards and backwards waveforms are shown in Figure 7

![Possible HV input waveform and trigger timing for using the VHSRD1 producing the two types of output waveforms necessary for driving a stick-slip motor in forwards and reverse.](image)

*Figure 7: Possible HV input waveform and trigger timing for using the VHSRD1 producing the two types of output waveforms necessary for driving a stick-slip motor in forwards and reverse.*

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\(^6\) Which generally have limited output bandwidth and current

\(^7\) NOTE: To charge a 2nF piezo to 250V in 1uS, an average current of 500 mA is required. HV amplifiers can typically provide only small output currents – for example, the Nanonis HV amplifier can provide a maximum 90 mA.
1.3.3 How to use it: Recommended configurations and modes of operation

Using the module is easy. All that is needed are an HV amplifier to provide the input voltage waveform and a device to provide the trigger sequence. A schematic of the recommended setup is shown below.

Figure 8: Block diagram of the recommended equipment configuration for using the VHSRD1 to drive a Piezo-motor
Depending on the programming of the pulse generator, the Piezo-motor can be driven in either stick-slip or inchworm mode.

1.3.3.1 Operation in inchworm mode

To operate a 6 element piezo-electric motor such as a Pan-style motor in inchworm mode using the VHSRD1 the channels need to be triggered sequentially at an appropriate time relative to the HV waveform. This can be readily accomplished using a programmable device which can generate delayed cascades of logic level pulses and accepts a trigger. A microcontroller with 6 digital output lines and at least 1 digital input line could be readily programmed for this purpose.

Figure 9: Input and output waveforms for using the VHSRD1 to drive a piezo-motor in inchworm mode in both directions.
The Arbitrary waveform generator produces a low level waveform (Voltage A) accompanied by a synchronization pulse (voltage B). The low level waveform is amplified by the HV amplifier to a high voltage waveform (voltage C) while the delay/pulse generator turns the single synchronization pulse into a cascade of trigger pulses (voltages D). These trigger pulses, arriving at the VHSRD1 while the HV waveform is high result in high speed transitions occurring on the outputs (voltages E). The direction of motion of the piezo-motor depends on the configuration of the trigger pulse cascade.
A possible set-up for producing these waveforms using some of the equipment available in the Scanning Probe Microscopy lab as would be as follows:

<table>
<thead>
<tr>
<th>Block diagram component</th>
<th>Real piece of equipment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arbitrary Waveform generator</td>
<td>Nanonis SC4 module</td>
</tr>
<tr>
<td>HV Amplifier</td>
<td>Nanonis HV amplifier</td>
</tr>
<tr>
<td>Delay/Pulse generator</td>
<td>Arduino Duemilanove Microcontroller</td>
</tr>
</tbody>
</table>

Table 4: Example of suitable equipment for use in conjunction with the VHSRD1

### 1.3.3.2 Operation in stick-slip mode

To operate a 6 element piezo-electric motor such as a Pan-style motor in stick-slip mode using the VHSRD1 all channels need to be triggered simultaneously. This can easily be accomplished by connecting a single channel of a suitable pulse generator to all 6 trigger lines.

![Waveform Diagrams](image)

**Figure 10: Input and output waveforms for using the VHSRD1 to drive a piezo-motor in stick-slip mode in both directions.**

Voltages D and E are shown as thick lines to emphasize that an identical waveform is present on all 6 channels.

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8 The sync pulse accompanying the waveform would come from the DIO port on the Nanonis Real-Time controller
9 Note that the input impedances of the opto-isolated trigger channels are only around 270 ohms and therefore the output current required to drive 6 of them at once would be around 100mA.
1.4 Known issues: Ringing and overshoot

The VHSRD1 is a first prototype which suffers from issues related to overshoot and ringing of the output. The severity of these issues depends on the capacitive load and mode of operation. Specifically, the higher the instantaneous current, the worse the overshoot and ringing were observed to be.

The worst case of overshoot observed during testing occurred when six 3.3nF capacitive loads\(^{10}\) were driven simultaneously, simulating the operation of a piezo-electric motor in stick-slip mode. The low and high voltage levels used in this test were 0 and 250V respectively. As can be seen in Figure 11, during the low to high transition, the device exhibited overshoot of ~100V and a small amount of slow ringing. The overshoot was substantially reduced in the high to low transition, however the ringing was worse.

Due to the extremely fast slew-rates and substantial currents delivered by the device, it is suspected that transient energy storage in parasitic inductances (in the power supply, auxiliary capacitor, and elsewhere) is the cause of the overshoot and ringing issues. The fact that the ringing was observed to be worse when the peak currents were higher supports this analysis. Should reduced overshoot and ringing be desired, operation of the VHSRD1 in inchworm mode is recommended.

These issues are examined further in the developers’ notes.

1.5 Recommended in-field improvements to the prototype module

The existing VHSRD1 is a rough working prototype. There are several modifications which could be implemented to improve the performance and reliability of this module for continued service.

The major electrical improvement to the module would be to add an auxiliary capacitor (C5) with lower equivalent series inductance or resistance. This could potentially reduce the overshoot and/or ringing present in the output waveform.

Mechanically, there are a few minor improvements which should be made:

1. Replacement of the red (Vcc) and green (GND) wires with the appropriate LEMO connector for use with the FEMTO PS-15-3-L 15VDC power supply (the insulation of the red wire is broken in one place)
2. 3 of the 4 tapped holes into which screws can be inserted to fasten the top cover to the chassis are stripped; these should be re-tapped or alternative attachment the top cover should be implemented.

\(^{10}\) Ceramic capacitors were used to approximate the electrical behaviour of piezoelectrics.
1.6 Conclusion and recommendations for future users

The VHSRD1 is a working prototype module which, when connected to an HV amplifier and triggered appropriately, can drive nano-farad capacitive loads at slew rates near 500 MV/s on 6 channels either simultaneously or in sequence. This makes the module appropriate for driving Pan-style stick-slip piezo-electric motors in either of the stick-slip or inchworm modes.

My recommendations to users of the existing VHSRD1 modules are as follows:

- Where possible, use the VHSRD1 to drive piezo-motors in inchworm mode in order to reduce the overshoot and ringing of the output waveform.
- Implement all of the recommended changes listed in the previous section.
2 Notes on the development of the VHSRD1

The following sections detail the development process of the VHSRD1 module.

2.1 Background and motivation

The Scanning Probe Microscopy (SPM) group at the University of British Columbia began developing a Pan-style Scanning Tunneling Microscope head during the year 2010. This type of instrument incorporates a stick-slip piezoelectric motor with 6 shear stacks. The particular head being developed used shear stacks with capacitances of approximately 2 nF each. In order to drive such a motor, electronics capable of driving high slew-rate waveforms into nano-farad capacitive loads were required.

As a result of this need, the VHSRD1 was designed and built by Ben MacLeod under the sponsorship of Dr. Yan Pennec of the SPM group, with support from the engineering physics project lab. The work was structured as a project for the ENPH 479 project course and took place during the 2011-2012 winter sessions.
2.2 Research and proposal development

The first step in the development process was to perform research and develop a project proposal.

Existing solutions to the challenge of driving capacitive loads with a high slew-rate waveform were examined. Several PhD theses and journal articles were studied, including the following:

- The PhD thesis of Niv Levy (2)
- The PhD thesis of Ching-Tzu Chen (3)
- A review of scientific instruments discussing a SPM facility built at NIST in Maryland (4)
- A review of scientific instruments about a high speed piezo driver circuit developed at MIT (1)

It was concluded that an approach based on the work contained in (1) would be taken and a project proposal entitled “ENPH 479 Project proposal: A high slew-rate driver circuit for actuating piezoelectric shear-stacks in a pan-style STM coarse approach motor” was developed. Further background information and details of the research can be found in this proposal, which is contained within the file archive enclosed with this user’s manual.

The chosen approach is based on the switching circuit shown below.

![Diagram of the high speed piezo driver circuit developed at MIT.](image)

*Figure 12: Diagram of the high speed piezo driver circuit developed at MIT. This diagram is taken from reference (1).*
2.3 Breadboard Prototyping

Following the approval of the project proposal by the engineering physics project lab, the development work began in earnest. Components were procured from Digikey.com, UBC Physics stores, the project lab, and the UBC physics E-lab and a prototyping a single channel of the VHSRD1 on a breadboard began. A complete list of the components used for the project is given in a later section of this document.

The topology of the first breadboard prototype was identical to the final circuit shown in the earlier diagram of the switching sub-circuit. The only difference between this first prototype and the final design was in the choice of component types and values (a choice which turned out to be critical to the circuit performance). The first prototype had the following values:

<table>
<thead>
<tr>
<th>Component</th>
<th>Vcc supply</th>
<th>HV supply</th>
<th>Auxiliary capacitor</th>
<th>Gate resistors</th>
<th>“piezo” capacitance</th>
<th>Resistance in parallel to “piezo”</th>
<th>Bootstrap capacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value/Description</td>
<td>0-25 V, 1 A supply</td>
<td>0-250 V, 100 mA supply</td>
<td>220nF, ceramic</td>
<td>10 ohm</td>
<td>3.3nF, ceramic</td>
<td>1 M Ohm</td>
<td>1 uF</td>
</tr>
</tbody>
</table>

Figure 13: Snapshots from the prototyping stage of the project

The first breadboard prototype part way through assembly (top), the project lab workstation used for the project (left) and a later iteration of the breadboard prototype with the 2.2K resistors and diodes added in parallel with the transistor gate/source (right).
### 2.3.1 On-time issue

Once the circuit was assembled properly, it was found that the on-time of the HV side IRF840 transistor was limited to a few hundreds of milliseconds. After some investigation it was determined that leakage from the bootstrap capacitor was discharging it to the point that the IR2111 gate driver no longer had a sufficient voltage supply to keep the transistor fully turned on, resulting in the waveform shown below. The bootstrap capacitor value was subsequently increased to 100uF from 1uF which appeared to resolve this issue.

![Output voltage from the breadboard prototype with a bootstrap capacitor value of 1uF.](image1)

*Figure 14: Output voltage from the breadboard prototype with a bootstrap capacitor value of 1uF. The HV voltage used in this test was ~45 Volts. Although the gate driver trigger was set high at t=0 and left in this state, note how the output voltage drops down after ~200 milliseconds.*

### 2.3.2 Ringing and overshoot issues

The major issue of overshoot and ringing became evident as soon as the switching time was examined. Although the desired high slew-rate was achieved immediately, the initial overshoot and ringing were extreme, even when only one channel was triggered, as can be seen in Figure 15, below. The overshoot and ringing were generally observed to be substantially worse for the low to high transition.

![Trigger (ch.1) and output (ch.2) voltages for an early test of the breadboard prototype.](image2)

*Figure 15: Trigger (ch.1) and output (ch.2) voltages for an early test of the breadboard prototype. This waveform was produced by triggering a single channel while using an HV voltage 15V. The trigger voltage in this case was also 15V as a manual switch connected to the DC power supply was being used to trigger the IR2111 gate driver directly (the IR2111 was found to require ~15V to trigger properly).*
Several measures were taken to attempt to reduce the overshoot and ringing, with varying degrees of success:

1. The extra components (diodes and 2.2K resistor) used in (1) were added to the circuit. This produced no noticeable decrease in the ringing and these components were subsequently removed\(^{11}\).

2. A snubber circuit\(^{12}\) consisting of a low value resistor (10 ohm) and a 20 nF capacitor (RC time constant = 200 nS, approximately the period of the ringing) was added in parallel with the 3.3 nF load capacitance. This circuit also failed to improve the ringing and was therefore removed.

3. Clamping diodes\(^{13}\) were added between the high-voltage side of the piezo and the HV and GND rails respectively. These diodes were oriented so that they would begin conducting if the piezo voltage rose above the HV voltage or dipped below the GND voltage. For reasons that were never uncovered, the HV and GND rails were also found to be exhibiting the same switching ripple as the piezo voltage. This prevented the clamping diodes from conducting and therefore this approach also failed to improve the ringing. The clamping diodes were therefore removed.

4. The values of the gate resistors were increased from 10 ohm to 40 ohms. This change produced a slight improvement in the ripple and motivated a further increase of the gate resistors to 160 ohms (the final value) which produced a further slight improvement. Overall, after this change, the ripple was still extremely bad.

5. In an effort to reduce parasitic inductances in the circuit\(^{14}\), the circuit was re-built in a much more compact configuration as seen below. This change did not noticeably improve the ringing but this circuit was used for the remainder of the testing regardless.

![Figure 16: Compact version of the breadboard prototype circuit](image)

\(^{11}\) As there was some confusion as to exactly what components were represented by the symbol \(\mathbb{Z}\), it is possible that this approach didn’t help because the wrong components were used. I initially thought that these were supposed to be 16V Zener diodes but it was later suggested that they were likely supposed to be high speed schottky diodes. Due to the relatively high frequency of the ringing it is possible that the turn-on time of the diodes I used was too large, although I tried the both zener and schottky diodes. As these components were included in the design of the group at MIT (for which no ringing was reported) I suspect that I improperly implemented some aspect of their design. This configuration of diodes is known as a Transorb.

\(^{12}\) Suggested by Gar Fisher with the UBC physics E-lab.

\(^{13}\) Also suggested by Gar Fisher

\(^{14}\) Which can apparently be appreciable in breadboards
6. Finally, the auxiliary capacitor was changed from a 220 nF ceramic to a 10uF electrolytic which essentially eliminated the ringing and overshoot. However, such a high value for the auxiliary capacitor is undesirable as it limits the frequency at which the HV amplifier can provide the slow ramps (the part of the waveform during which the piezo “sticks”) due to the output current limitations of common HV amplifiers. Therefore a 1uF electrolytic capacitor was substituted for the 10uF one, which resulted in negligible amount of overshoot being present on the output when tested for a HV voltage of 100V. As this approach substantially resolved the ringing issues, no other approaches were subsequently considered.

![Figure 17: 100V amplitude transitions demonstrating negligible ringing of the output after the replacement of the auxiliary capacitor.](image)

For this test, the better of the two types of 1uF, 50V electrolytic capacitor on hand in the project lab was used. A single channel was triggered.

Following this discovery, several different models of 1uF capacitor were tried and significant differences in performance were noted among these. The capacitor which gave the best performance also happened to have the lowest equivalent series resistance – 23 ohm as measured by the project lab LCR meter (which is not necessarily a reliable instrument). Unfortunately, this capacitor (a relatively large, black axial lead model) was only rated to 50V and would short at approximately 150V, below the required 250V operating level. After several attempts to test the breadboard prototype at voltages above 100V, the breadboard itself began shorting around 130V as well. At this point it was decided to conclude testing of the breadboard prototype and begin manufacture of a higher quality PCB version of the circuit.


2.4 PCB design, fabrication, assembly, testing and modification

2.4.1 Design

The PCB boards produced for this project were designed using Altium designer summer 2009 release. This software was made available through the UBC department of Physics.

Learning to use Altium took a considerable amount of time and the author would highly recommend working through several of the tutorials before attempting to do any real work with the software. The design process in Altium involved the following steps:

1. Schematic layout
   a. Importing component libraries
   b. Creating custom components
   c. Placing components and wiring them together
   d. Adding net labels, annotation (component designators) and choosing physical footprints for components
   e. Using sub-circuits and sub-sheets to simplify the top level schematic

2. PCB layout
   a. Setting up design rules: trace thicknesses, minimum clearances, hole sizes etc...
   b. Defining the board footprint
   c. Grappling with various issues in laying out a PCB for DIP components to be soldered by hand from the bottom size of the board only
   d. Using rooms to copy the layout from 1 channel to all channels
   e. Finalizing the layout for compatibility with the available PCB mill tool set (i.e. appropriate hole sizes)

2.4.2 Fabrication

The UBC engineering physics project lab has a LPKF S62 PCB mill suitable for fabricating the PCB’s that were designed. The fabrication process for the PCB boards involved the following steps:

1. Exporting CAM (gerber) files from ALTUIM using Altium’s outjob functionality
2. Processing these CAM files in CircuitCAM into LPKF format
3. Running the formatted CAM files on the project lab’s LPKF S62 PCB mill using the BoardMaster software.
   During this process several issues arose:
   a. Losing progress issue
      i. It was very easy to accidentally reset the job and lose all history of the cut/uncut tool paths. This can be avoided by being very careful not to change layers or de-select tool paths part way through running a layer.
   b. Hold-down issue:
      i. The cut thickness of the PCB mill is VERY sensitive to the height of the PCB. If the PCB is not very flat on the machine table, the cut thickness will change as the tool moves to different parts of the board, which can result in an unusable product.
      ii. The vacuum hold-down system on the PCB mill doesn’t work very well, therefore to ensure that the PCB board sits nice and flat, make sure to tape it down VERY WELL!
      iii. Making sure all surfaces are clean and that no bits of dirt (copper burrs, fiberglass dust) are on the PCB or the work surface will help in keeping the PCB flat.
   c. Indexing issue:
      i. Re-indexing the cutter after flipping the PCB is a hassle especially since the camera needs calibrating (estimated accuracy of camera is worse than 0.500 microns)

---

15 The author found this step to be very time consuming and would recommend taking advantage of Altium’s functionality for streamlining multi-channel PCB layout work wherever possible.

16 Altium has features for assisting with SMT routing which may make it preferable in some cases to use SMT instead of through-hole components.
2.4.3 Assembly

Assembly of the PCB’s was done by hand in the project lab. This included the following steps:

1. The PCB’s were immersed for ~2 min in Liquid tin.
2. The vias and then the other components were soldered in using a sharp soldering iron and fine, leaded solder.
3. The PCB’s were joined together using the header plugs.
4. The assembly was mounted inside the housing using nylon stand-offs.

Figure 18: Snapshots from the fabrication process
From left to right starting at top left: The Altium PCB layout; the PCB mill at work; the completed main PCB; the tinned and partially assembled PCB at the assembly station; the fully assembled module consisting of both the main and opto-isolator PCB’s mounted in the housing.
2.4.4 Functionality testing and modification

After the opto-isolator PCB was fully assembled and integrated with the main PCB, a design oversight became evident: the “high” output level (5V) of the inverters on the opto-isolator block was insufficient to trigger the input of the IR2111 gate drivers on the main PCB which require ~15V to trigger. Fortunately, it was possible to implement a relatively clean and simple design change which rectified this issue by increasing the output from the inverter stage to 15 V. This change hinged on the good fortune I had in finding a different hex-inverter IC that worked with higher voltages but had an identical pin-out.

Figure 19: Schematic of the opto-isolator block prior to making changes to the inverter stage
The entire schematic is shown at the top left, while detail views of the power configuration (top right) and one of the six identical channels (bottom) are shown for clarity.
The changes that were made were as follows:

1. The LM7805 regulator was removed and the VCC rail (formerly supplied +5V by the LM7805) was connected directly to pin 7 of the header connector (+15V from the main PCB) with a jumper.

2. The SN74LS06N hex-inverter (which accepts VCC up to 7V only) was replaced with the MC14106BCP hex-inverter (which can handle VCC up to 18V). This change was possible because these two IC’s have identical pin-outs.

3. The six 1K pull-up resistors were removed because the MC14106BCP has totem-pole type outputs (as opposed to the open-collector outputs on the SN74LS06N).

Following these changes, the module began working properly and performance testing was started.
2.5 PCB performance testing

Once the PCB circuit was working properly (i.e. after the changes to the opto-isolator block), performance testing for operation in inchworm and stick-slip mode was performed. For these tests one of the brown 1uF, 350V rated electrolytic capacitors (digkey part # 565-1400-ND) ordered especially for the project was used as the auxiliary capacitor\(^\text{17}\). The set-up for these test was as follows:

1. A 3.3 nF load capacitor was connected to each output channel of the VHSRD1 module
2. 15VDC was supplied to the VCC line of the module
3. 250VDC was supplied to the HV line of the module
4. Three oscilloscopes, each monitoring two of the six output channels, were synchronized to a trigger produced by an Arduino micro-controller
5. 5V triggers were applied to the 6 trigger inputs of the module by the Arduino micro-controller:
   a. sequentially (for the inchworm mode test)
   b. simultaneously (for the stick-slip mode test)

\[\text{Figure 21: The set-up for performance testing the VHSRD1 PCB}\]

\(^{17}\) This was the type of capacitor installed in the module upon delivery to the Scanning Probe Microscopy group on Jan 10, 2012.
2.5.1 *Inchworm mode (one channel triggered at once) performance results*

The inchworm mode performance test was successful. A very high slew-rate was observed and although the output did overshoot substantially on the low-high transition, the voltage settled quickly with negligible ringing.

![Figure 22: Results of the 250V test of the VHSRD1 in inchworm mode](image)

A single channel was triggered for this test. The REF A scale (50V, 500ns) describes the waveform on the left and the REF B scale (50V, 250ns) describes the waveform on the right. 3.3nF load capacitances were used for this test to simulate piezo-electrics.

<table>
<thead>
<tr>
<th>Performance Metric</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage range</td>
<td>300 V (250V base + 50V overshoot)</td>
</tr>
<tr>
<td>Rise time(^{18})</td>
<td>500 ns</td>
</tr>
<tr>
<td>Slew rate</td>
<td>6e8 V/s</td>
</tr>
<tr>
<td>Capacitive load</td>
<td>3.3 nF</td>
</tr>
<tr>
<td>Average current output per channel during rise time</td>
<td>1.98 A</td>
</tr>
</tbody>
</table>

*Table 5: Performance metrics for VHSRD1 in inchworm mode operation (for the low to high transition)*

\(^{18}\) Defined here as time from voltage minimum to voltage maximum
2.5.2 Stick – slip mode (all channels triggered at once) performance results

The stick-slip mode performance test was successful. A very high slew-rate was observed and although the output did overshoot substantially on the low-high transition, the voltage settled quickly with very little ringing. Some ringing did occur on the high to low transition but the amplitude of this ringing was relatively small.

![Graph showing stick-slip mode performance results](image)

**Figure 23: Results of the 250V test of the VHSRD1 in stick-slip mode**

All six channels were triggered simultaneously for this test. 3.3nF load capacitances were used for this test to simulate piezo-electrics.

<table>
<thead>
<tr>
<th>Performance Metric</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage range</td>
<td>350 V (250V base + 100V overshoot)</td>
</tr>
<tr>
<td>Rise time(^\text{19})</td>
<td>750 ns</td>
</tr>
<tr>
<td>Slew rate</td>
<td>4.67e8 V/s</td>
</tr>
<tr>
<td>Capacitive load</td>
<td>3.3 nF</td>
</tr>
<tr>
<td>Average current output per channel</td>
<td></td>
</tr>
<tr>
<td>during rise time</td>
<td>1.54 A</td>
</tr>
</tbody>
</table>

\(^{19}\) Defined here as time from voltage minimum to voltage maximum
2.6 Suggested changes to be considered in future versions of the VHSRD1

During the fabrication and testing of the prototype VHSRD1, several shortcomings in the electrical and mechanical design of the module became evident. Additionally, there was insufficient time to implement several desirable in the prototype design.

Should an improved version of the VHSRD1 be developed in the future, the designer may wish to consider implementing some or all of the changes given in the tables below.

<table>
<thead>
<tr>
<th>Design flaw</th>
<th>Suggested change(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>The opto-isolation PCB is cramped and isolated traces come too close to non-isolated sections of the circuit.</td>
<td>Integrate the opto-isolation circuits with the main PCB and improve the layout of these components.</td>
</tr>
<tr>
<td>The logic of the opto-isolator board is clumsy and requires an extra inversion stage (the hex inverter) to achieve active-high triggering</td>
<td>Redesign the opto-isolator logic by selecting opto-isolators with a different truth table.</td>
</tr>
<tr>
<td>No protection is provided to the VHSRD1 or the HV input source in the case of a short-circuited output</td>
<td>Implement short-circuit protection of the outputs by using a slow blow fuse or another appropriate technique.</td>
</tr>
<tr>
<td>Safety and convenience features such as indicator lights for power on, HV active and triggers active are missing</td>
<td>Add these features.</td>
</tr>
<tr>
<td>Overshoot and ringing issues are not fully resolved</td>
<td>Further reduce these issues through improved component selection, revised circuit design or additional circuitry such as working schottky clamping diodes or a transorb or snubber circuit.</td>
</tr>
</tbody>
</table>

*Table 7: electrical design flaws in the VHSRD1*

<table>
<thead>
<tr>
<th>Flaw description</th>
<th>Suggested change(s)</th>
</tr>
</thead>
</table>
| Some of the traces and pads were extremely small, close together and difficult to solder to, sometimes becoming detached were rework was necessary. Solder and small pieces of metal would also occasionally bridge between traces, causing unwanted short circuits. | • Increase the trace sizes as much as possible.  
• Increase the gaps between the traces as much as possible.                                                                                                                                                           |
| The integration of the electronics assembly into the housing is awkward and imperfect                                                                                                                                                                                   | • Integrate the two PCB’s into a single PCB for a cleaner design  
• Redesign the main PCB to have all the input and output plugs on one side, thus simplifying housing selection and assembly  
• Improve the mechanical design of the PCB by properly aligning all the mounting holes.                                                                                                                                 |

*Table 8: Mechanical design flaws in the VHSRD1*
2.7 Conclusion and recommendations for future developers

Overall, my conclusion is that the overshoot and ringing issues demonstrated by the VHSRD1 are highly dependent on the auxiliary capacitor characteristics. A possible explanation for these issues is that the VHSRD1 switching circuit is interacting with an inductance within the HV power supply – a transformer inductance for example. A simplified schematic of this situation is shown below.

![Schematic of VHSRD1 test set-up including power supply inductance](image)

**Figure 24: Schematic of VHSRD1 test set-up including power supply inductance**

Some key arguments for this explanation are as follows:

1. The presence of an inductance in the power supply (L1) results in the creation of an LC resonator circuit between the piezo and the inductor when S1 is closed, a condition which would be conducive to the overshoot and ringing observed.
2. Using larger capacitances for the auxiliary capacitor (C1) was found to reduce the overshoot and ringing observed. As a larger capacitor would provide a greater share of the current necessary to charge the piezo, this would result in less current (and therefore less energy storage) in the inductor L1 and would likely result in reduced overshoot and ringing.
3. It was observed that different capacitors of the same value (1uF) gave significant differences in the levels of overshoot and ringing observed. As superior capacitors with lower parasitics could also provide a greater share of the current necessary to charge the piezo (relative to inferior capacitors of the same value), this could also result in reduced overshoot and ringing by the same reasoning as in argument # 2.
4. The overshoot and ringing observed were not as pronounced for the high to low transition. This fits the proposed model because the power supply inductance HV is removed from the circuit during the high to low transition as switch S1 is opened during this transition.

My recommendations to anyone carrying out future work on the VHSRD1 or a successor are as follows:

- Expand upon or to disprove the proposed explanation for the overshoot and ringing through further testing of the VHSRD1 using different HV power supplies and with different auxiliary capacitors
- Consider implementing some or all of the suggested changes listed in the previous section
3 Works Cited

4 Appendices

4.1 List of parts used and project cost accounting

<table>
<thead>
<tr>
<th>Part Name</th>
<th>Digkey Part #</th>
<th>description</th>
<th>UNIT PRICE</th>
<th>QUANTIT</th>
<th>EXTENDED COST</th>
<th># USED IN FINAL MODULE</th>
<th>Net cost of part per module</th>
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<tr>
<td>MUR160-TP</td>
<td>MUR160-TPMSCT-ND</td>
<td>diode</td>
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<td>18</td>
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<td>1N4745A</td>
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<td>16v zener</td>
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<td>$28.08</td>
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<tr>
<td>1N4148</td>
<td>1N4148TACT-ND</td>
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<td>$0.14</td>
<td>36</td>
<td>$5.04</td>
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<tr>
<td>IRF840</td>
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<td>36</td>
<td>$100.44</td>
<td>12</td>
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<td>IR2111</td>
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<td>18</td>
<td>$58.86</td>
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<td>0</td>
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<td>H11L1m</td>
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<tr>
<td>Housing</td>
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<td>from UBC physics E-lab</td>
<td>$10.00</td>
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<td>$10.00</td>
<td>-</td>
<td>-</td>
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<tr>
<td>Misc</td>
<td>-</td>
<td>1 hex inverter, resistors, wire, solder</td>
<td>$20.00</td>
<td>1</td>
<td>$20.00</td>
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<tr>
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<td>TOTAL MODULE COST</td>
<td>$84.20</td>
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</tbody>
</table>
4.2 Diagrams

The following sub-sections give Altium circuit schematics and PCB layouts for the two PCBs which make up the VHSRD1 module.

4.2.1 Circuit schematics

4.2.1.1 Switch sub-circuit

Figure 25: Schematic of one switching sub-circuit
4.2.1.2 The opto isolator-block

A design change (red annotations) was implemented to this schematic after the fabrication of the corresponding PCB to up the output level of the inverters from 5 V to 15V. This design change is discussed further in the developers’ notes section of this document.
Figure 27: Schematic of the top-level layout.

The opto-isolator block PCB plugs into the headers P1 and P2.
4.2.2 PCB layouts

4.2.2.1 6 channel piezo driver PCB layout (top and bottom routes)

Figure 28: The routing and component placement for the main PCB.
Red traces are on the top of the PCB while blue traces are on the bottom. The top and bottom ground planes have been hidden for clarity. The board outline and the opto-isolator block PCB board footprint are shown in pink.
4.2.2.2 6 channel piezo driver PCB layout (top plane)

Figure 29: The main PCB with the top ground plane shown
Figure 30: The main PCB with the bottom ground plane shown
4.2.2.4 Opto isolator block pcb layout (routes)

Figure 31: The layout of the opto-isolator block PCB. Note that the 1K pull-up resistors (R4,R6,R10,R12,R16,R18) and the LM7805 voltage regulator (U1) have been removed in the working prototype as a result of the design change discussed in section 0.
4.2.2.5  Opto-isolator block pcb layout (Top plane)

Figure 32: Layout of the opto-isolator block PCB with the top plane shown
4.2.2.6 Opto-isolator block PCB layout (Bottom plane)

*Figure 33: Layout of the opto-isolator block PCB with the bottom plane shown*
Figure 34: Outlines and hole spacings for the two overlapped PCBs (dimensions in inches)