

A 400MHz  
**Direct Digital Synthesizer**  
with the AD9912

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# Part I

## Design and Fabrication of the Device

# Executive Summary

Part I of this report discusses the design and fabrication stage of this project. At time of writing, testing is on hold while a complete prototype device has been assembled. Part II will follow and will include documentation the testing procedures, the results and all recommendations.

This project aimed to design, build and test a complete and functional Direct Digital Synthesizer (DDS) device with output frequencies of up to 400MHz. A DDS is a device capable of digitally generating sinusoidal waves with programmable frequency and phase. The Analog Devices 9912 (AD9912) was chosen as a suitable DDS Integrated Circuit (IC) and this was used in the project design. An enclosure also had to be built to house the DDS device.

The device had to be compatible with an existing parallel control interface used in the lab, requiring a parallel-to-serial converter, as the AD9912 requires a serial interface. This parallel-to-serial converter was designed and prototyped on a breadboard to verify correct operation.

It was also necessary for the device to minimize noise. This was accomplished with a passive analog filter circuit that was simulated in SPICE and confirmed to meet design specifications.

Complete designs and fabrication files for the circuit and enclosure had to be provided. The schematics for the board were completed and a PCB layout was designed from this schematic. The PCB layout generated all files required for manufacturing. The enclosure was modified from an existing design to better accommodate the PCB layout and to improve heat dissipation.

Twenty PCBs had to be manufactured and parts had to be ordered for 15 boards. These have all arrived and a prototype device is currently being assembled. Enclosures for 15 boards also had to be ordered and these are all currently being manufactured.

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# Glossary

**AD9852** is a DDS IC produced by Analog Devices, with a maximum system clock of 300MHz.

**AD9912** is Analog Devices' highest-performance DDS IC, with a maximum system clock of 1GHz.

**DDS** is a device capable of digitally generating sinusoidal waves with programmable frequency and phase.

**ferrite bead** is a passive component which is primarily resistive at high frequencies. Therefore, they act to block high-frequency noise and are useful as an inexpensive means of isolating noisy power supply groups.

**FSC** is a digitally programmable 10-bit scale factor that sets the peak output current of the AD9912 Digital-to-Analog Converter (DAC)[3].

**prepreg** is a shorthand term for pre-impregnated material. In this report, it is a name for the dielectric material placed between copper layers on a PCB.

**via** is a connection between one or more copper layers on a PCB.

# Acronyms

**CSB** Chip Select Bit.

**DAC** Digital-to-Analog Converter.

**DAQ** Data Acquisition System.

**DIP** Dual In-line Package.

**EMI** Electromagnetic Interference.

**FTW** Frequency Tuning Word.

**IC** Integrated Circuit.

**LDO** Low-Dropout.

**NI** National Instruments.

**PCB** Printed Circuit Board.

**PHAS** Department of Physics and Astronomy.

**PLL** Phase-Locked Loop.

**QDG** Quantum Degenerate Gasses.

**SMD** Surface-Mount Devices.

**UTBus** University of Texas Bus.

**VCO** Voltage-Controlled Oscillator.

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# Introduction

The Quantum Degenerate Gasses (QDG) Laboratory at the University of British Columbia investigates the applications of ultra-cold gases to the physics of many-body quantum systems [8]. One such investigation attempts to trap, isolate and precisely control the movement of ultra-cold atoms.

Naturally, this experiment requires precise control of experimental conditions. To achieve this, they employ a complex computer-controlled electronic system. Contained within this control system are several devices called Direct Digital Synthesizer (DDS)s. The current generation of these devices are designed by Todd Meyrath and are capable of producing radio frequency signals between DC and 135MHz [9]. Todd Meyrath's device is shown in Figure 1.1. The DDSs are based around the Analog Devices 9852 (AD9852), a highly integrated 300MBPS CMOS digital synthesizer. This IC provides a highly stable frequency-, phase-, and amplitude-programmable cosine output[2].

Other key features of the AD9852 are the ability to internally multiply an external clock up to a maximum of 300MHz ( $20 \times 15\text{MHz}$ ) and an output update of speed up to  $10^8\text{Hz}$ . The AD9852 supports Phase-Shift Keying (PSK) and Frequency-Shift Keying (FSK), which allow switching between two pre-programmed phases or frequencies based upon the level of a digital signal. Further, a high-speed integrated analog comparator allows the AD9852 to be used as a programmable clock source.

The QDG lab requires eight devices capable of analog sinusoidal outputs with programmable frequencies of up to 400MHz. These devices will be used to control acousto-optic modulators, which can be used to precisely control the frequency of the laser beams. The QDG lab uses these lasers to control ultra-cold atoms in experiments that are beyond the scope of this document.

To fit the lab requirements, this project aims to redesign, implement and test a new DDS device, the AD9912, which replaces the AD9852 microchip with a similar chip, the AD9912. This IC is a newer and faster edition of the AD9852 - a 1GBPS digital synthesizer capable of producing radio frequency signals at frequencies of up to 400MHz and an output update speed of up to 2MHz. To simplify usage in the lab, the AD9912-based DDS device must support the existing AD9852 DDS device control interface.

As the AD9912 is a faster IC than the AD9852, it has several requirements that make a designing an AD9912-based DDS device more challenging. For example, the higher speed signals involved require much more careful impedance control of the signal lines than the AD9852 DDS devices. There are feature differences as well: the AD9912 does not support PSK or FSK, though the AD9852 does, and supports serial programming in place of a parallel control bus. The AD9912 also requires voltage supplies at 1.8V on top of the 3.3V the AD9852 required. Like the AD9852, the AD9912's output must be filtered to remove noise resulting from the digital synthesis process; this filter must be designed and characterized.

Due to these differences, the design for DDS device built for this project did not begin with the AD9852 DDS device. Instead, the design began with the AD9912 evaluation board. This is evident in the analog portion of the AD9912 DDS device, which uses similar structure and components choice as the evaluation board. However, the AD9912 DDS device did draw inspirations from the AD9852 device[9]. In particular, the digital control and power circuitry design is heavily based upon



the AD9852 device and the overall PCB layout is very similar.

To house the DDS device, an enclosure must be designed. This should securely fasten the AD9912 DDS device, provide noise isolation and be compatible with the rack mount solution used for the AD9852. Both the enclosures and the front panel mounting mechanism should be ordered.

This project is sponsored by Dr. Kirk Madison, Assistant Professor with the department of Physics and Astronomy at The University of British Columbia and head of the QDG Laboratory.

This report is organized into several chapters: Discussion, Conclusions and Project Deliverables. A chapter on recommendations will be included with Part II of this report. The Discussion is broken into Theory of Operation, PCB Layout Considerations, Design and Fabrication Methods, Board Features and Breadboard Testing. The Discussion aims to provide a quantitative description of the expected operation of the device and give insight into the methodology of the design process. The Conclusions provide closure to the report, summarise the important results and findings. The Project Deliverables describe the physical and electronic results of this project which are to be handed over to the QDG Laboratory. Finally, the Appendices present the design schematics, fabrication drawings, 3D renderings of the PCB and a full parts list.

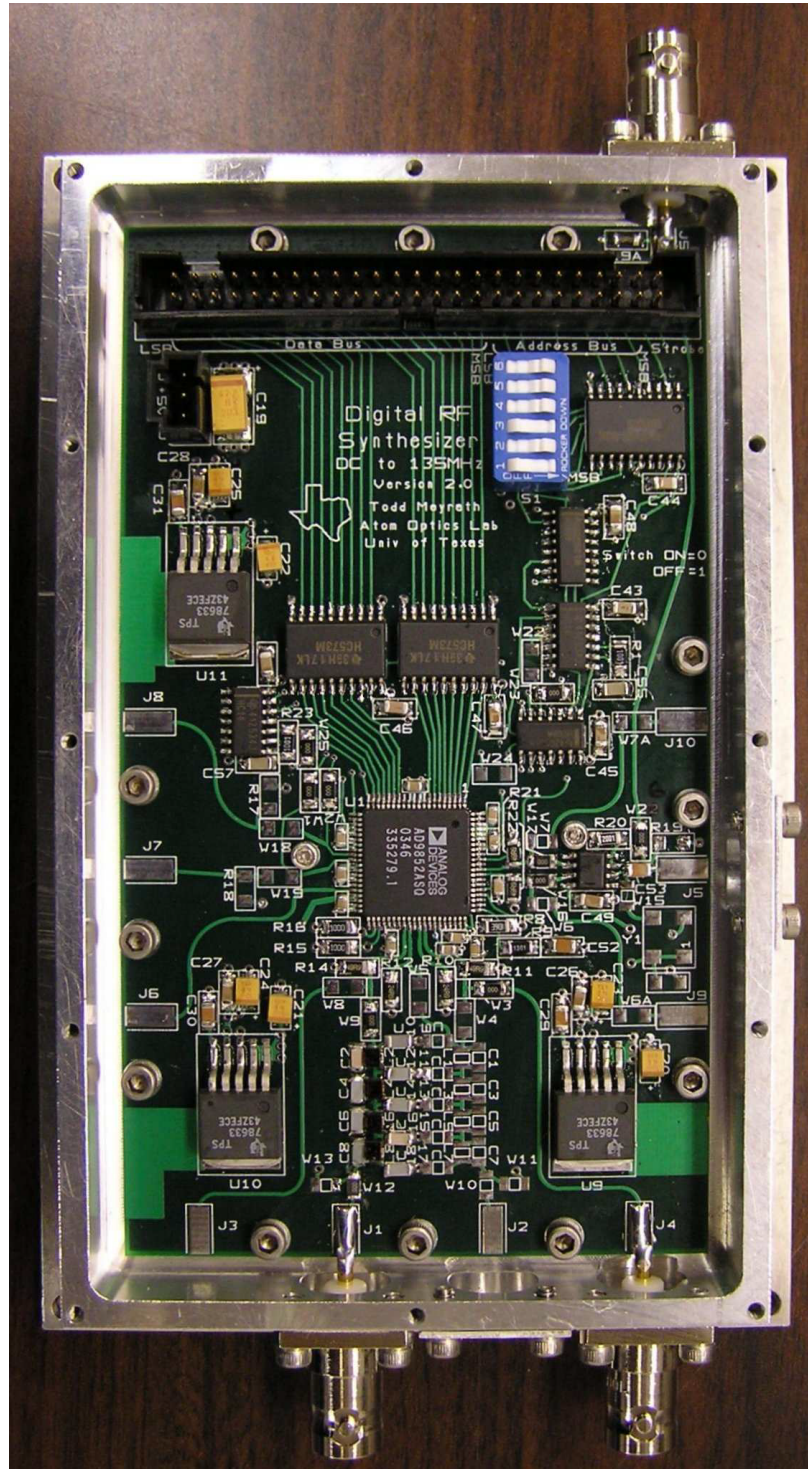


Figure 1.1: Photo of the 150MHz AD9852-based DDS designed by Todd Meyrath[9].

## 2

# Discussion

## 2.1 Theory of Operation

This section will begin by giving an overview of the functionality of the device. Next, the internal workings of the AD9912 IC itself will be discussed, providing an understanding what to expect from the IC's RF and clock outputs. Afterwards the supporting circuitry will be described block by block, returning as needed to the AD9912 IC to explain related concepts.

### 2.1.1 Device Overview

The device is designed to generate a sinusoidal or square output signal with a frequency of up to 400MHz. The frequency and phase of both output signals can be rapidly digitally programmed (but not independently). The output signal is generated by the AD9912, a high-performance, low-noise 14-bit DDS[3].

The sinusoidal output is filtered through a 400MHz low-pass filter to remove unwanted high-frequency noise. Depending on board configuration, the filtered RF signal can then be taken as the primary device output or it can be brought back to the AD9912 to become the input signal for either of the AD9912's two clock drivers - the CMOS output driver and the HSTL output driver (see Section 2.1.4).

Figure 2.1 is a high-level block diagram of the newly designed AD9912-based DDS device. The block diagram shows all existing BNC connection pads. Only three of these are intended for use in the finished devices. These are SYSCLK, the system clock input, RF, the sinusoidal signal output and CMOS, the CMOS clock driver output. The remaining connections are intended primarily for testing.

Significant omissions from the block diagram are the Phase-Locked Loop (PLL) loop filter (see Section 2.1.5.3) and the voltage regulation circuitry (see Section 2.2.2).

### 2.1.2 The AD9912 Direct Digital Synthesizer

Figure 2.2 is a block diagram showing the core internal functionality of the AD9912, reproduced from the datasheet[3]. This diagram consists of three main blocks: the 48-bit accumulator, angle to amplitude conversion and the DAC.  $f_s$  is the DAC sample rate[3].

Each cycle of  $f_s$ , the accumulator increments its running total by the 48-bit value of the Frequency Tuning Word (FTW)[3]. The accumulator will periodically reach its maximum value ( $2^{48}$ ) and roll over. The rate of roll over is equal to the frequency of the sinusoidal output,  $f_{DDS}$ , and is given by

$$f_{DDS} = \frac{FTW}{2^{48}} f_s [3]. \quad (2.1)$$

Equation 2.1 can be solved to give

$$FTW = \text{round}(2^{48}(\frac{f_{DDS}}{f_s})) [3]. \quad (2.2)$$

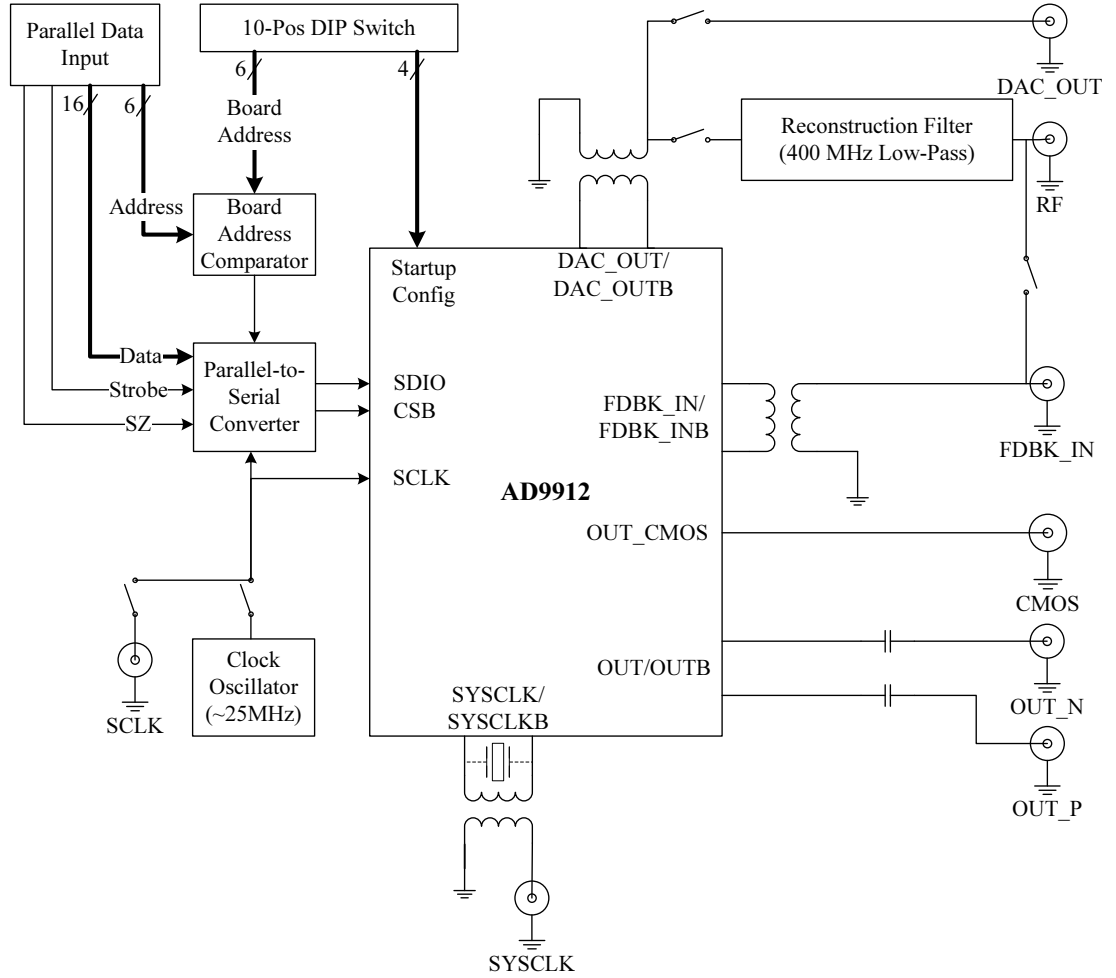


Figure 2.1: Block diagram of the full DDS device, showing input and outputs. Switches are implemented as  $0\Omega$  resistors. The crystal oscillator shown is optional and replaces the external SYSCLK input.

The output of the accumulator is offset by the 14-bit value Phase Offset. This results in a phase offset to  $f_{DDS}$  of  $\Delta\Phi$  given by

$$\Delta\Phi = 2\pi\left(\frac{\Delta\text{phase}}{2^{14}}\right)[3]. \quad (2.3)$$

Both the FTW and the Phase Offset can be digitally controlled by the user (see Section 2.1.6), allowing the frequency and phase of the output sinusoid to be controlled with 48 and 14 bits of precision, respectively. This corresponds to increments of approximately  $3.6\mu\text{Hz}$  (at  $f_s = 1\text{GHz}$ ) and  $3.8 \times 10^{-4}\text{rads}$ .

After the phase offset, the accumulator output (which is a digital representation of the phase of the output sinusoid) is converted to a 14-bit digital value representing the amplitude of the output sinusoid. The DAC then converts this value to an analog differential signal pair (DAC.OUT/DAC.OUTB). The frequency, phase and peak output current (see Section 2.1.2.1) of this signal are digitally controllable. It will be transformed into a single-ended signal and low-pass filtered (see Section 2.1.3) before becoming the output RF signal of the DDS device.

### 2.1.2.1 DAC Peak Output Current

The peak output current of the DAC is determined by two factors: a reference current on the DAC\_RSET pin ( $I_{DAC\_RESET}$ ) and a digitally programmable 10-bit scale factor referred to as the FSC[3]. The DAC\_RSET pin is internally connected to a reference voltage of 1.2V and externally connected to ground through the resistor  $R_{DAC\_REF}$  (R26 on the PCB), and therefore

$$I_{DAC\_REF} = \frac{1.2V}{R_{DAC\_REF}} [3]. \quad (2.4)$$

The AD9912 datasheet recommends  $I_{DAC\_REF} = 120\mu A$  which implies taking  $R_{DAC\_REF} = 10k\Omega$ .

The DAC full-scale output current ( $I_{DAC\_FS}$ ) is given by

$$I_{DAC\_FS} = I_{DAC\_REF} \left( 72 + \frac{192FSC}{1024} \right) [3]. \quad (2.5)$$

Digital control of the FSC allows the DAC output current to be digitally controlled in increments of  $0.1875\mu A$  from a minimum of  $8.64\mu A$  to a maximum of  $31.68\mu A$ <sup>1</sup>.

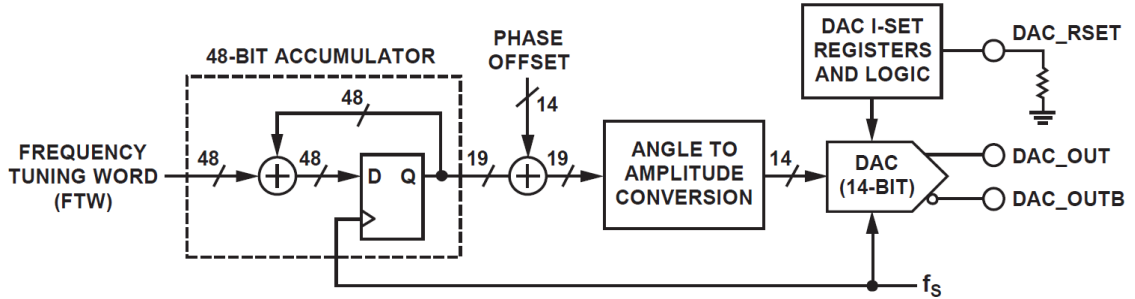


Figure 2.2: Block diagram showing internal functionality of the AD9912, reproduced from the datasheet[3].

### 2.1.3 RF Output and the Reconstruction Filter

The AD9912's DAC produces a sampled reconstruction of the desired sinusoidal signal. A basic result in Fourier Analysis says that this reconstructed signal contains both the desired baseband signal, extending from DC to the Nyquist frequency ( $f_s/2$ ), as well as images of this baseband signal which appear periodically at intervals of  $f_s/2$  and theoretically extend to infinity[3].

Note that the first unwanted image is that of the baseband signal, mirrored about  $f_s/2$ . This means that as the DDS output frequency is increased, the frequency of the fundamental spur in the first image decreases. For example, if the DDS output frequency is 400MHz, the first spur will appear at 600MHz. At an output frequency of 490MHz, the first spur will appear at 510MHz. So as the output frequency increases, the requirements on the filter become more stringent. The result is a practical limitation on the DDS output frequency which is less than the Nyquist frequency of  $f_s/2$ . The actual limit will depend upon the properties of the filter used and the requirements of the application.

Our application desires only the baseband signal, and therefore the DAC output must be low-pass filtered to remove higher frequency noise. This filter is referred to as the reconstruction filter. It is desired that this filter have a cut-off frequency of 400MHz, as steep a roll-off as possible (rejection at 500MHz is desired) and very good rejection in the stop-band (60dB attenuation at a minimum).

<sup>1</sup>This follows from Equation 2.4. Comparably, the datasheet's AC specifications table gives the DAC's typical and maximum full-scale output current as  $20\mu A$  and  $31\mu A$ , respectively.

Following from the AD9912 evaluation board design, a  $50\Omega$  surface mount RF transformer (ADT2-1T-1P+, Mini-Circuits) is used to transform the differential signal pair of Figure 2.2 (DAC\_OUT/DAC\_OUTB) into a single-ended signal prior to filtering[4]. A single-ended filter design is less susceptible to component variations than its differential counterpart[4]. A differential filter design might be more appealing to users who were only interested in the clock generation feature of the AD9912 (see Section 2.1.4), not the RF output, since no transformers would be required. However, our application requires a single-ended RF output, and so one the transformer would still be required. Note that the RF transformers have a  $(7 \times 8)mm^2$  footprint and cost approximately \$4.25.

Note that since transformers do not function at low frequencies, the RF output will be attenuated at very low frequencies and will not function near DC<sup>2</sup>. The ADT2-1T-1P+ RF transformers are rated for frequencies in the range of 8 to 600 MHz.

The reconstruction filter design is based on that of the AD9912 evaluation board, Rev. B<sup>3</sup>. It is a 7th-order passive elliptic low-pass filter, shown in Figure 2.3.

### 2.1.3.1 SPICE Verification

The reconstruction filter design was verified through a SPICE simulation (AC Analysis in NI MultiSim v11.0). Figure 2.3 shows the schematic used for SPICE simulation and Figure 2.4 shows the resulting transfer function.

As we can see from the transfer function, the cut-off frequency is 400MHz, the roll-off occurs in 100MHz and the stop-band attenuation is about 60dB. The data used to generate the plot shows that the pass-band ripple is a maximum of about 1.5dB.

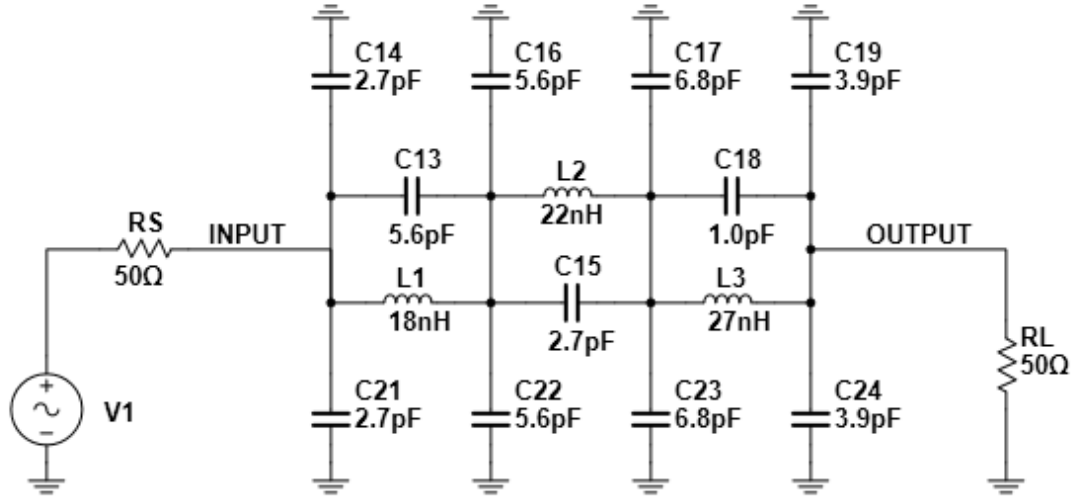


Figure 2.3: Reconstruction filter schematic used for SPICE simulation. This is a 7<sup>th</sup> order elliptic low-pass filter with a 400MHz cut-off frequency. Designators were taken to match the PCB.

### 2.1.4 Clock Drivers

The AD9912 has two on-board clock drivers, the CMOS output driver and the HSTL output driver. These clock drivers share the differential FDBK\_IN/FDBK\_INB inputs and effectively serve to transform the filtered sinusoidal DAC output into a square clock signal. A second ADT2-1T-1P+ RF

<sup>2</sup>This is not a concern for the QDG lab, as the existing AD9852-based devices function at frequencies from DC to 135MHz[9].

<sup>3</sup>Rev. A uses a 240 MHz low-pass filter with very similar design.



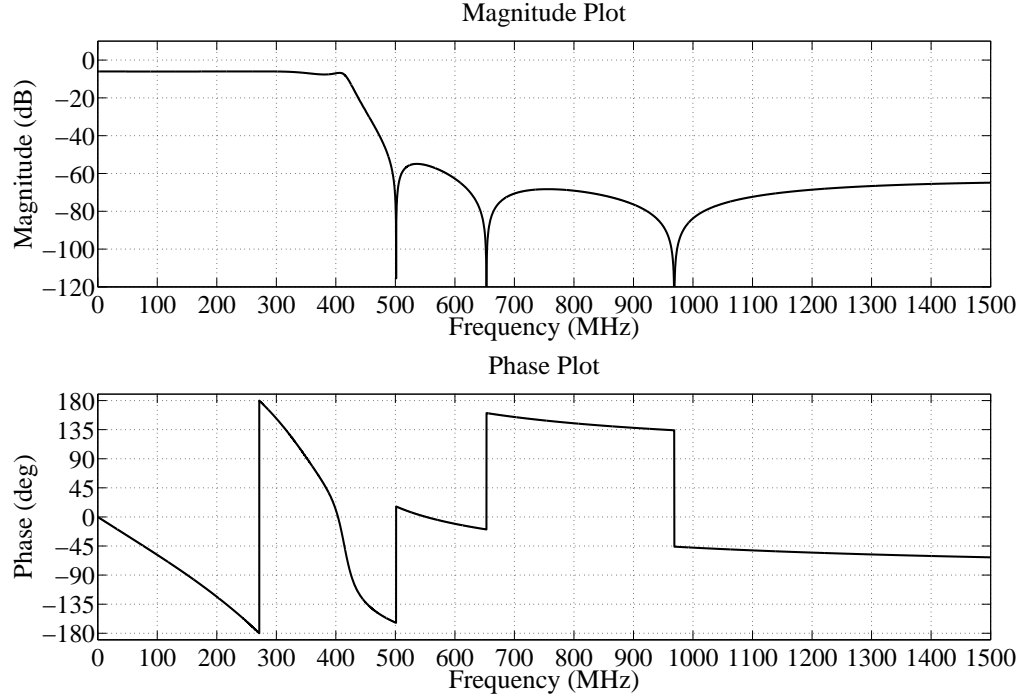


Figure 2.4: Reconstruction filter frequency-domain transfer function generated from a SPICE simulation of the circuit shown in Figure 2.3

transformer is used to transform the single-ended filter output into a differential signal suitable for the FDBK\_IN/FDBK\_INB inputs.

The CMOS output driver provides a CMOS-level clock signal and is suitable for frequencies in the range 8kHz to 150MHz[3]. The device can be configured at component population to have a CMOS voltage of either 3.3V or 1.8V (see Section 2.4). The CMOS output driver includes an integer divider which can be enabled or bypassed. When bypassed, the CMOS output frequency is the same as the signal on the FDBK\_IN/FDBK\_INB inputs. When enabled, this frequency can be reduced. At frequencies below 30MHz, noise on the CMOS output can be reduced by enabling the CMOS divider and running the DAC at a higher frequency[3]. See the AD9912 datasheet for more information.

The HSTL output driver provides a 1.8V differential clock signal and is suitable for frequencies in the range 20MHz to 725MHz[3]. Frequencies above the Nyquist rate for the AD9912 are achieved with a  $2\times$  frequency multiplier. The datasheet claims a duty cycle between 48% and 52%, while the CMOS driver's duty cycle is given as being between 45% and 55%. Note that unlike the AD9852, the AD9912 does not support digital control of the duty cycle of the output clock.

### 2.1.5 Clock Inputs

The DDS device has two clocks on-board. These are referred to as SYSCLK and SCLK. SYSCLK drives  $f_s$ , the internal DAC sample rate of the AD9912. The frequency of  $f_s$  is directly proportional to the output frequency of the DDS. If PLL is enabled on the AD9912,  $f_s$  can be made to have a frequency up to 66 times greater than that of SYSCLK. SCLK is the digital control clock and controls the frequency of the AD9912's serial control interface.

### 2.1.5.1 SCLK

SCLK controls the frequency of the AD9912's serial control input. This clock is also used to convert the incoming digital programming parallel signal into the serial signal used by the AD9912. Our implementation allows for two possible sources for SCLK: an external connection and an on-board clock oscillator (TXC 7C Series). The external connection is intended for testing purposes, particularly to determine the maximum frequency at which the serial input can reliably operate (see next paragraph). Once this frequency has been determined, an appropriately selected TXC 7C IC will be placed on board and used as SCLK.

An important note is that the TXC 7C datasheet does not specify whether the enable pin is active high or active low. The board includes jumpers to allow for both possibilities; see Section 2.4 for information on switching between these two options.

According to the AD9912 datasheet SCLK is limited to a maximum of 50MHz[3]. However, the maximum value of SCLK will likely be limited by the digital control logic and not the AD9912. Timing analysis based upon information in all relevant components' datasheets suggests that the maximum SCLK frequency should be around 25MHz; see Section 2.1.6 for details.

### 2.1.5.2 SYSCLK

SYSCLK is the main system clock. The DAC sample rate,  $f_s$ , is controlled by SYSCLK. As discussed below, the AD9912 has PLL multiplier circuitry which allows  $f_s$  to be up to 66 times greater than the frequency of SYSCLK. From the AD9912 datasheet,  $f_s$  is limited to a maximum of 1GHz, so the SYSCLK and PLL multiplier must be carefully chosen to be less than this speed[3].

The AD9912 supports the use of either a crystal oscillator or a clock oscillator; the DDS device supports both an on-board crystal oscillator and an external clock source (recommended). Depending on which is to be used, the jumpers necessary to connect the clock source or crystal oscillator to the AD9912 must be installed; see Table 2.7.

### 2.1.5.3 PLL

The AD9912's PLL circuitry allows the frequency of SYSCLK to be increased by any even multiple between 4 and 66. This circuitry generates an internal clock using a Voltage-Controlled Oscillator (VCO). The voltage that controls the VCO is generated by a current pump and an external loop filter consisting of components defined in Table 2.6 and is related to the phase difference between the internal clock, divided by a number set by the PLL register, and the SYSCLK. The voltage then raises and lowers to converge the internal clock on a set multiple of the SYSCLK[3].

The AD9912 PLL also includes a frequency doubler before the PLL circuitry itself. This functionality creates a clock pulse on both the rising and falling edge of SYSCLK, doubling the frequency. Using the frequency doubler creates a clock output that has an improved phase noise performance over simply using double the PLL multiplier instead. Unfortunately, the frequency doubler does not produce a clean rectangular pulse with constant duty cycle. That is, subharmonics are introduced at multiples of the SYSCLK input frequency. The PLL multiplier should be chosen to suppress these subharmonics[3].

Using the PLL allows for a slower clock to be used as the input to the DDS device. Slower clock sources are much cheaper and easier to acquire. However, the PLL will introduce additional noise and inaccuracy into the system, especially as the PLL multiplier approaches the maximum of  $66\times$ .

The ideal configuration of the PLL loop filter depends on the multiplier to be used. If PLL is to be bypassed, then the loop filter can also be bypassed. See Section 2.4 for details.

## 2.1.6 Digital Control

The devices are controlled through an existing parallel interface called the University of Texas Bus (UTBus). Custom circuitry on board our devices has been designed to interface the parallel UTBus with the AD9912's serial control port. This section will describe the UTBus, the serial control port and the custom interface between the two.



### 2.1.6.1 The UTBus

The UTBus is an existing parallel programming interface used by the QDG lab and based upon Todd Meyrath's work[9]. As the UTBus is already in use in the lab<sup>4</sup>, supporting this interface was a design requirement.

The interface uses ribbon cable and a 50-pin Molex connector with pin functionality as defined in Figure 2.5. As shown, these 50 pins are divided into 25 grounded pins, 8 address bits, 16 data bits and one additional bit, called the strobe. The 8 address bits are used to specify which device should receive the 16 bit command. The strobe bit is effectively a clock with a 1/3 duty cycle; when the strobe bit is high, the address and command are guaranteed to be stable. The UTBus address and data pins are asserted for three distinct periods with equal length: once, while the strobe remains low, a second time while the strobe is high, and a third time while the strobe is low[7]. These three periods together comprise one UTBus command. This timing is illustrated in Figure 2.6.

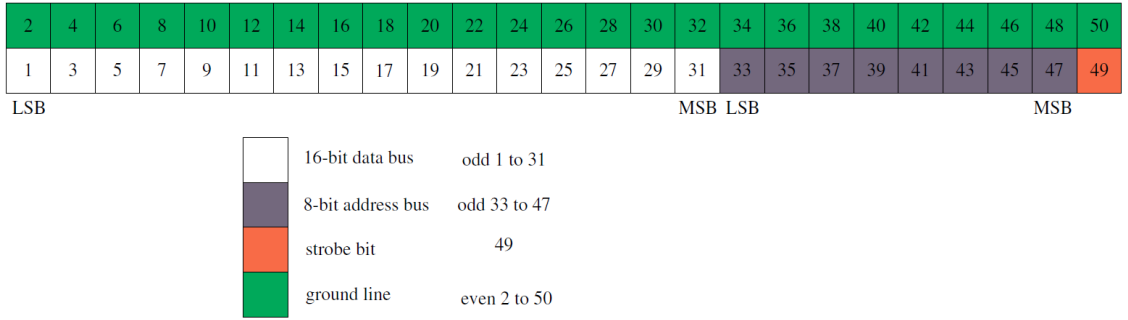


Figure 2.5: Diagram of the 50-Pin UTBus Connector, reproduced from [9].

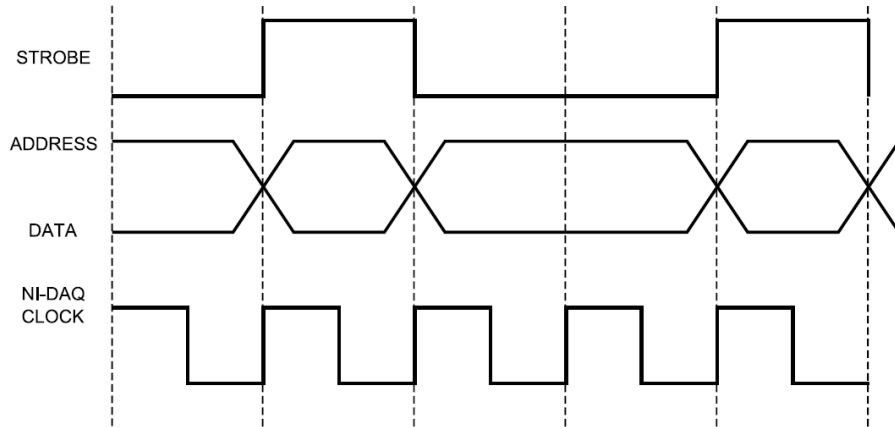


Figure 2.6: Timing diagram for the UTBus, showing the strobe, address, data and NI-DAQ clock. Each command sent to a device requires three periods of the NI-DAQ clock to complete. Reproduced from Keith Ladouceur's Master's Thesis[7].

The QDG lab currently uses an NI-DAQ, controlled by a desktop computer running a custom python script, to drive the UTBus. Current uses of the UTBus send one command at a time, with an NI-DAQ clock frequency of up to 5MHz.

<sup>4</sup>The UTBus is used to control various devices in the QDG lab, including analog output devices and the existing AD9852-based DDSs[7].

### 2.1.6.2 The AD9912's Serial Control Port

In contrast with the parallel programming interface of the AD9852, which was used on the previous generation of DDS devices, operation of the AD9912 is controlled through a serial interface. This is inconvenient from a design standpoint because the UTBus provides 16 bits of data in parallel and no suitable clock. Section 2.1.6.3 describes the hardware solution which interfaces the UTBus with the serial control port.

A detailed discussion of the serial control port is given in the AD9912's datasheet, including multiple timing diagrams. Here we summarize the essential elements.

The serial control port of the AD9912 consists of four pins: a clock (SCLK), an I/O pin (SDIO), an active-low control pin which gates the I/O cycles (Chip Select Bit (CSB)) and an output pin (SDO). SDO is unnecessary for our application and has been left unconnected on the board<sup>5</sup>.

Control of the AD9912 is established through the writing of binary data to various registers. Each register has a unique 13-bit address and some functionality which is documented in the datasheet. For example, the DDS output frequency can be controlled by writing to the 48-bit register containing the FTW. Note that all registers are not equal in size.

Each communication cycle consists of two parts: the writing of a 16-bit instruction word and the reading of or writing to a register. Table 2.1 shows the 16-bits of the instructions words mapped to their corresponding bits in the UTBus. The instruction word contains a 13-bit register address (A12,...,A0), two bits indicating the length of the coming data transfer (W1 and W0, see Table 2.2) and a single bit indicating whether the transfer is to be a read or a write (R/ $\overline{W}$ ). Note that our device supports only one- and two-byte transfers and does not support reads. Writing to registers larger than two bytes will require multiple communication cycles.

Table 2.1: Serial control port instruction word bit functionality. D0,...,D15 correspond to DAT0,...,DAT15 in our design and schematics (see Figures A.3 and A.5). The last row corresponds to the 16 bits of the instruction word. Adapted from the AD9912 datasheet[3].

MSB															LSB
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
R/ $\overline{W}$	W1	W0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Table 2.2: Decoding of the W1 and W2 bits in an instruction sent the AD9912's serial control port. These two bits control the number of bytes to be transferred in the current communication cycle and describe the number of bytes transferred in this command cycle, excluding the 2-byte instruction. W1 and W0 correspond to the DAT14 and DAT13 data bits on the UTBus, respectively. Note that the AD9912 DDS device does not support all byte lengths. Reproduced from the AD9912 datasheet[3].

W1	W0	Bytes to Transfer	Supported?
0	0	1	Yes
0	1	2	Yes
1	0	3	No
1	1	Streaming mode	No

The CSB must be held low in order for the AD9912 to recognize data on the SDIO. Accordingly, the CSB should be held low during writing of the instruction word. Afterwards, the CSB can remain low and data transfer can begin immediately. Alternatively, the CSB can be brought high to disable the serial control port until the user is ready to transfer data. Data transfer is similar: the CSB must be held low during the writing of each byte of data. Between each byte, the CSB can be brought high to pause the transfer if desired<sup>6</sup>.

<sup>5</sup>Actually, the pin itself is connected to a trace leading away from the AD9912 IC and to a via. This is to facilitate testing.

<sup>6</sup>Streaming mode is an exception to this; during streaming mode, a rising edge on the CSB indicates the end of the communication cycle.

Some registers on the AD9912 are buffered so that writing to these registers does not affect the device output until an I/O update operation is performed to transfer the data from the buffer registers to the control registers. This can be accomplished by toggling the IO\_UPDATE pin or by writing a 1 to the register update bit. To simplify the design of the interface between the UTBus and the serial control port, the IO\_UPDATE pin is disabled on our devices, and so the latter method will be used in practice. In practice, the CSB will be brought high between commands sent on the UTBus in order to stall the communication cycle and allow time for the UTBus to send the next command.

### 2.1.6.3 Parallel-to-Serial Converter

Schematics for the parallel-to-serial converter are shown in Figures A.3, A.4 and A.5.

An 8-bit comparator is used to compare bits A7 to A2 of the UTBus address bits (the lower 2 bits are not used as addresses) against the board address. The board address, which can be set using a Dual In-line Package (DIP) switch, is a 6-bit address which should be unique for each device connected to the UTBus. If the address bits match the address set on the DIP switch, a custom arrangement of flip flops listens for a rising edge on the strobe bit. When this happens, a pulse is generated that latches the 16 bit command into two SN74HC166 8-bit shift registers. These 8-bit shift registers are daisy-chained together to form a 16-bit shift register.

Once the data is loaded in, the shift registers output the UTBus data into the AD9912's serial port one bit at a time beginning with DAT0. The number of data bits clocked into the AD9912 is an option set by the UTBus address bus bit 1 (A1), renamed to SZ in our schematics. The SZ bit switches between using all 16 bits of the data bus (SZ=0) or only the lower 8 bits of the data bus (SZ=1). The SZ bit will be critical when programming the AD9912; see Section 2.1.6.4.

To implement the switch between 8 and 16 bits, the DDS device design takes advantage of the CSB pin on the AD9912. Since the AD9912 can only be programmed when the CSB is held low, the DDS device ensures that the CSB is only held low for either 8 or 16 bits. This is accomplished by using a mirrored set of SN74HC166 8 bit shift registers. These second set of shift registers are loaded with either all logic low, or 8 bits of logic low followed by 8 bits of logic high. The output from these shift registers is directly connected to the CSB and is clocked out at the same time as the shift registers containing the command. This ensures that the AD9912 is only able to receive data on the serial port for exactly the time it takes to clock in one of 8 or 16 bits.

Parts of this circuit have been prototyped and tested; see Section 2.5. A timing diagram is presented in this section using the data collected; see Figure 2.19.

### 2.1.6.4 Programming

Programming the DDS device consists of sending a series of commands on the UTBus. On each command, 8 or 16 bits of data on the UTBus are clocked into the DDS one bit at a time beginning with DAT0. The UTBus address bit A1 (renamed to SZ in our schematics) controls the length of the data transfer (low for a 16-bit transfer). Thus (see Section 2.1.6.2), each communication cycle with the AD9912 requires two commands to be sent on the UTBus. The first command sent will always be 16-bits and tells the AD9912 which register is to be written to as well as how much data is to be written (8 or 16 bits; see Table 2.2). The second command can be either 8-bits or 16-bits and is the actual data to be written to the register addressed previously.

If the register being written is a buffered register (see Section 2.1.6.2), an additional register must be written to update the DDS output. This can be done immediately or after multiple registers have been written to.

If the register to be written to is larger than 16-bits, multiple communication cycles are required, as illustrated in the example below.

The following is an example of a series of commands to set the FTW to 68DB8BAC7<sub>16</sub><sup>7</sup> (FTW controls the output frequency; see Section 2.1.2). With  $f_s=1\text{GHz}$ , this sets the AD9912 output to 100MHz. The FTW is 48 bits, and so requires 3 communication cycles to completely overwrite. The

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<sup>7</sup>68DB8BAC7<sub>16</sub> = 0000 0000 0000 0110 1000 1101 1011 1000 1011 1010 1100 0111<sub>2</sub>

fourth communication cycle shown below is a write to the I/O Update register, which causes the output frequency to be updated. The address and strobe bits are not shown.

Table 2.3: Sample DDS Device Commands to set the output frequency to 100MHz and subsequently update the output. The first 6 commands set the FTW to the value required for at output frequency of 100MHz, while the last two commands tell the AD9912 to update the output.

SZ	Data				Description
	0-3	4-7	8-11	12-15	
0	0010	0001	1010	1011	Send (0) the next two bytes (01) of data to register 01AB <sub>16</sub> (000110101011 <sub>2</sub> ), the register containing the top 8 bits of the FTW
0	0000	0000	0000	0110	Write 00000000 <sub>2</sub> to register 01AB <sub>16</sub> and 00000110 <sub>2</sub> to register 01AA <sub>16</sub>
0	0010	0001	1010	1001	Send (0) the next two bytes (01) of data to register 01A9 <sub>16</sub> (000110101001 <sub>2</sub> )
0	1000	1101	1011	1000	Write 10001101 <sub>2</sub> to register 01A9 <sub>16</sub> and 10111000 <sub>2</sub> to register 01A8 <sub>16</sub>
0	0010	0001	1010	0111	Send (0) the next two bytes (01) of data to register 01A7 <sub>16</sub> (000110100111 <sub>2</sub> )
0	1011	1010	1100	0111	Write 10111010 <sub>2</sub> to register 01A7 <sub>16</sub> and 11000111 <sub>2</sub> to register 01A6 <sub>16</sub> , bits 15:8 of the FTW
0	0000	0000	0000	0101	Send (0) the next byte (00) of data to register 0005 <sub>16</sub> (0000000000101 <sub>2</sub> ), the IO.UPDATE register that tells the AD9912 to update the output
1	1000	0000	0000	0000	Write 1 to the 1 bit IO.UPDATE register

### 2.1.7 Power Management

The AD9912 has stringent power requirements to ensure the highest-performance operation. Both 3.3V and 1.8V power supplies are needed. While it would be possible to implement an AD9912-based device using only two power rails, the datasheet highly recommends isolation between each group of power supplies on the AD9912. The extent to which isolation is required depends on the requirements of the application. See *Power Supply Partitioning* in the AD9912 datasheet for a detailed description of which pins can be grouped together and which should be isolated.

The isolation between power supply groups can be achieved by using separate regulators for each group or by placing a ferrite bead between a common regulator and each rail. Separate voltage regulators provide better isolation but require more PCB area, increase the cost of the device<sup>8</sup> and increase the power consumption of the device<sup>9</sup>. Our design uses four regulators, two at each of 1.8V and 3.3V, each separated into the broad groups analog and digital. Five ferrite beads are then used to isolate five power supply groups, each sourcing from the 1.8V analog regulator. See the schematics shown in Figures A.7 and A.8.

The CMOS clock driver power supply (VDD.CMOS) can either be connected to the analog 3.3V regulator through a ferrite bead (F4) or to the analog 1.8V regulator through a 0 $\Omega$  jumper (W14)<sup>10</sup>, depending on the desired CMOS output voltage level.

All power pins on the AD9912 and digital logic ICs have a 0.1 $\mu$ F bypass capacitor connected as close as possible to the supply connection. Bypass capacitors serve as power reservoirs, providing instantaneous power to the IC. They prevent that power from needing to travel over a long connection to the voltage regulator, introducing delays due to parasitic inductance of the traces involved. Instead

<sup>8</sup>The cost of each high-performance Low-Dropout (LDO) voltage regulator used was about \$4.50.

<sup>9</sup>This is not a significant concern for this application.

<sup>10</sup>See the datasheet for more information on the CMOS power supply recommendations. W14 uses the same 0805 package as the ferrite beads, allowing a ferrite bead to be used instead of a jumper if desired.

the power comes directly from the capacitor, which is placed as close as possible to the IC in order to minimize parasitic inductance. This capacitor is then recharged by power from the voltage regulator at a speed much closer to DC.

## 2.2 PCB Layout Considerations

Major sources of inspiration were the AD9912 evaluation board and Todd Meyrath's AD9852 design[9] (shown in Figure 1.1). Here we discuss the components chosen for the DDS device, the considerations needed for power management, techniques for managing heat and how trace widths were chosen to ensure signal integrity.

### 2.2.1 Components

All parts and components used on the DDS device were selected and sourced, beginning by considering the components used on either the AD9912 evaluation board or Todd Meyrath's AD9852 design[9]. Many of these parts were re-used, as reflected in the complete Bill of Materials, which is given in Appendix D.

For this application, Surface-Mount Devices (SMDs) were preferred to through-hole components due to reduced inductances and the possibility of higher component density, which is ideal for high frequency design[10]. For these reasons (and following the example of the AD9912 evaluation board and the old AD9852 DDS), most components on our board are surface-mount. There are only three through-hole components: the 50-pin Molex UTBus connector, the 3-pin Molex power connector (5V) and the 10-Pos switch (sets the board address and the AD9912 start-up configuration). Component choice for the UTBus and power connectors is compatible with those used in previous generation devices.

Most common passive components use either 1206 (3.2mm×1.6mm) or 0402 (1.0mm×0.51mm) surface-mount packages. The 1206 package is preferred for its larger footprint<sup>11</sup>, but 0402 is preferred near the AD9912 IC in order to shorten the trace lengths between the AD9912 IC and its bypass capacitors<sup>12</sup>.

Most components are placed on the top side of the board. Bottom-side components are limited to resistors, capacitors and ferrite beads.

The BNC connectors are mounted to the enclosure and solder directly to 2.54×6.35mm pads on the PCB. This design is identical to that used in Todd Meyrath's AD9852 design[9].

The linear regulators used for this board (Texas Instruments TPS78633 and TPS78618) were selected due to their proven use in Todd Meyrath's AD9852 design[9]. These are fixed-voltage 1.5A LDO voltage regulators suitable for use with a 5V supply. Four regulators are used. See Section 2.1.7 for more information.

### 2.2.2 Power Plane

The third layer of the 4-layer PCB is a dedicated power plane, shown in Figure 2.7. This power plane was split into five regions. Around the outside perimeter of board is a 5V plane which is supplied by the 3-pin external power connector. A 470μF tantalum capacitor near the connector stabilizes this supply and ensures constant voltage levels. The 5V supply is used by the four on-board linear power regulators which power the remaining four regions.

The left side of the power plane (labelled Digital 3.3V) is used to supply a 3.3V signal to the digital components which provide the digital interface between the UTBus and the AD9912. The Digital 3.3V power plane also provides power for the AD9912's serial control port.

The three other power planes (Digital 1.8V, Analog 1.8V and Analog 3.3V) provide power to the appropriate sections of the AD9912 IC. These are all required to be independently supplied and

<sup>11</sup>The small 0402 footprint requires a steady hand and some skill in order to install manually.

<sup>12</sup>To reduce Electromagnetic Interference (EMI), a Texas Instruments white paper recommends that the length-to-width ratio of traces between an IC and its voltage source should not exceed 3:1[10].

there are stringent requirements on bypass capacitors and ferrite beads, as listed by the AD9912 datasheet. These recommendations have been followed wherever practical.

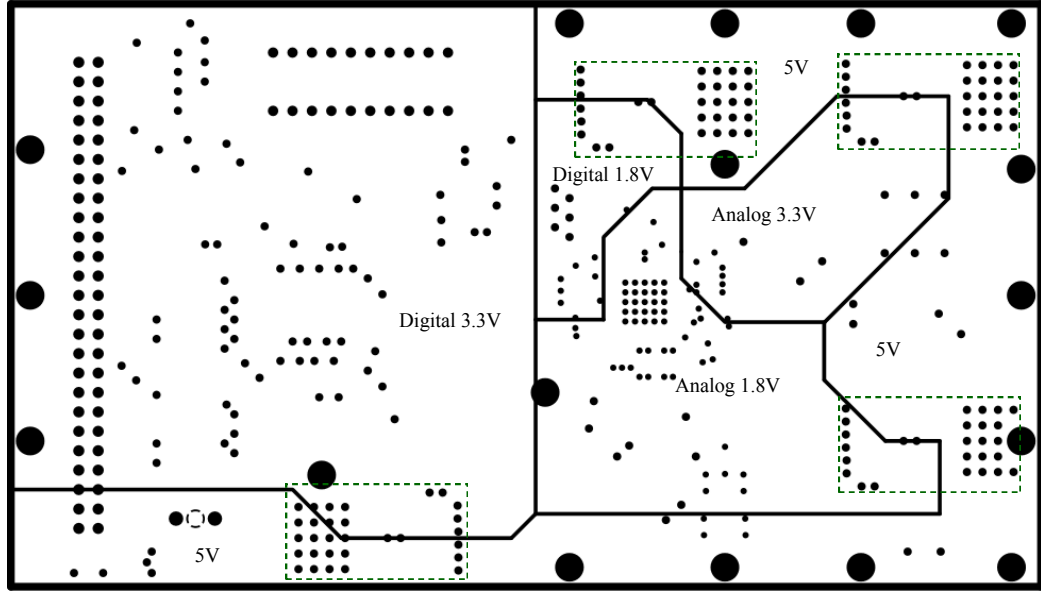


Figure 2.7: The PCB power plane design. This is a negative fabrication image; black areas indicate removal of copper. The plane is split into five regions, labelled in the figure. There are analog and digital 1.8V and 3.3V power planes as well as a 5V plane which serves to supply the four on-board LDO voltage regulators. The PCB areas taken up by each voltage regulator and bypass capacitors are shown outlined in dashed green lines.

### 2.2.3 Heat Dissipation

Power dissipation is an important consideration for the voltage regulators and the AD9912. Both ICs have grounded thermal contacts which are to be soldered directly to copper fills on the top side of the PCB. As recommended by both ICs' datasheets, an array of thermal vias is located under each of these pads and serves to conduct heat away from the ICs. All empty areas on the bottom side of the PCB are ground-filled and this serves to increase the heat capacity. Areas on the bottom layer which are to be in contact with the aluminium enclosure have the insulating soldermask removed, increasing heat transfer to the enclosure (as well as grounding the enclosure). Figures 2.10 and 2.11 show the full PCB layout from the top and bottom sides.

### 2.2.4 Characteristic Impedance and Trace Width

Characteristic impedance is the instantaneous impedance of a PCB trace. It is the impedance that a high-speed signal will encounter as it propagates along a trace, charging up the metal of the trace as it goes. This charging is essentially charging a capacitor where the signal trace is the top of the capacitor, the PCB prepreg is the dielectric and the ground plane is the bottom of the capacitor<sup>[1]</sup>. As the signal's edge travels along the trace, it charges the trace itself before encountering any other electrical components.

If the trace impedance is different from the source or destination impedance, it is possible that the signal's energy will not be completely transferred, with some of the energy returning back through the trace. This can cause constructive or destructive interference, resulting in a less accurate signal.

To avoid this, our design ensured that high-frequency signal traces were  $50\Omega$ .  $50\Omega$  is a common standard and matches the input impedance of the amplifier that the RF output is intended to drive. All other components along these signal paths should be  $50\Omega$  as well, including the RF transformers, BNC connectors and coaxial cables.

Equation 2.6 gives a formula for calculating the characteristic impedance of a rectangular trace[5], where  $W$ ,  $T$  and  $H$  are in common units.  $\epsilon_r$  is the dielectric constant of the PCB prepreg. This equation is an approximation and it most accurate for  $Z_0$  between 50 and  $100\Omega$ [5]. It is the same equation that Altium Designer uses by default for calculating the characteristic impedance of traces.

$$Z_0(\Omega) = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \frac{5.98H}{0.8W + T} \quad (2.6)$$

Figure 2.8 shows the trace geometry assumed by Equation 2.6. This trace geometry is referred to as a microstrip.

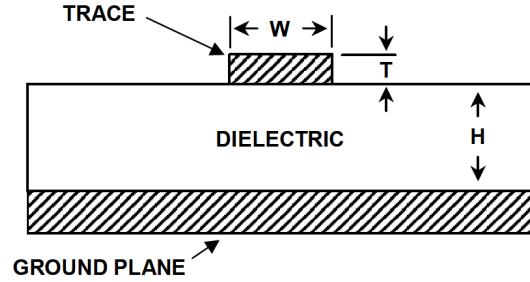


Figure 2.8: Diagram of microstrip trace geometry. Use this figure for characteristic impedance calculations following Equation 2.6. Reproduced from [5].

The situation is slightly more complicated for differential signals. Equation 2.7 can be used for differential signals [6].  $S$  is the spacing between the two traces carrying the differential signal.

$$Z_{diff} = 2Z_0(\Omega)[1 - 0.48e^{-0.96\frac{S}{H}}] \quad (2.7)$$

An alternative trace geometry is referred to as the stripline, and is shown in Figure 2.9. Striplines have the advantage of having lower impedance than the equivalent microstrip and of providing natural shielding for high-frequency signals, thus reducing emissions and reducing interference from incoming signals[5]. Emissions and external interference is not a significant concern for us, as the boards are to be enclosed in a solid aluminium enclosure. Also, striplines are not accessible from the exterior of the board, making testing more difficult. We do not use striplines on our board.

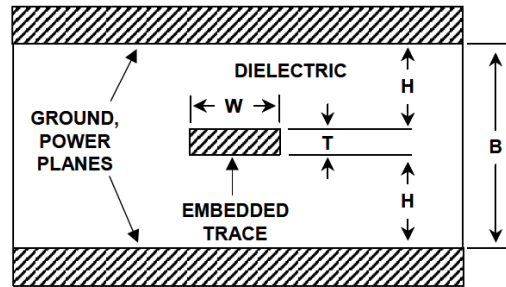


Figure 2.9: Diagram of stripline trace geometry. This figure is shown for comparison only; striplines do not appear on our device. Reproduced from [5].

Using Equations 2.6 and 2.7 and the following parameters,

$$\begin{aligned}\epsilon_r &= 4.350 \text{ (FR-406 dielectric material)} \\ T &= 2.8 \text{ mils (0.071 mm or the thickness of 2 oz/ft}^2 \text{ copper)} \\ H &= 9.6 \text{ mils (0.244 mm)} \\ S &= 9.0 \text{ mils (0.229 mm)}\end{aligned}$$

trace widths giving  $50\Omega$  were calculated as 14.75mils (0.375mm) for single-ended signals and 26.5mils (0.673mm) for differential signals. Wherever practical<sup>13</sup>, these widths were used in the design.

## 2.3 Design and Fabrication Methods

This section describes the methods used in designing and fabricating the PCB and enclosure.

### 2.3.1 Schematic Design

Altium Designer was the software tool used to design the new device, both for a connectivity-level schematics to the generation of layer-by-layer PCB fabrication files.

Due to similarities, the design was largely based upon the AD9912 reference board schematic. This included the schematic for the DDS output, including the Reconstruction Filter, but did not include digital input or power designs. These additional designs were based upon Todd Meyrath's AD9852 design[9] but were extensively modified due to the differences between the AD9912 and the AD9852.

All schematic diagrams are shown in Appendix A.

### 2.3.2 PCB Design

As mentioned, Altium Designer was the software tool used design the PCB layout. Once the design was complete, Altium was used to generate layer-by-layer PCB fabrication files (Gerber files) and drill files. Printouts of these Gerber files are shown in Appendix B. The drill files instruct the PCB manufacturer on the size and location of all holes to be drilled.

Section 2.2 discusses several considerations which influenced the PCB design.

Figures 2.10 and 2.11 show the full PCB layout from the top and bottom sides. Figures 2.13 and 2.12 show assembly diagrams for the PCB. The top and bottom pastemasks and silkscreens are shown above the enclosure and IC mechanical drawings.

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<sup>13</sup>Very close to the AD9912 it is nessessary to reduce the width of the traces, due to the small pin spacing of the IC.



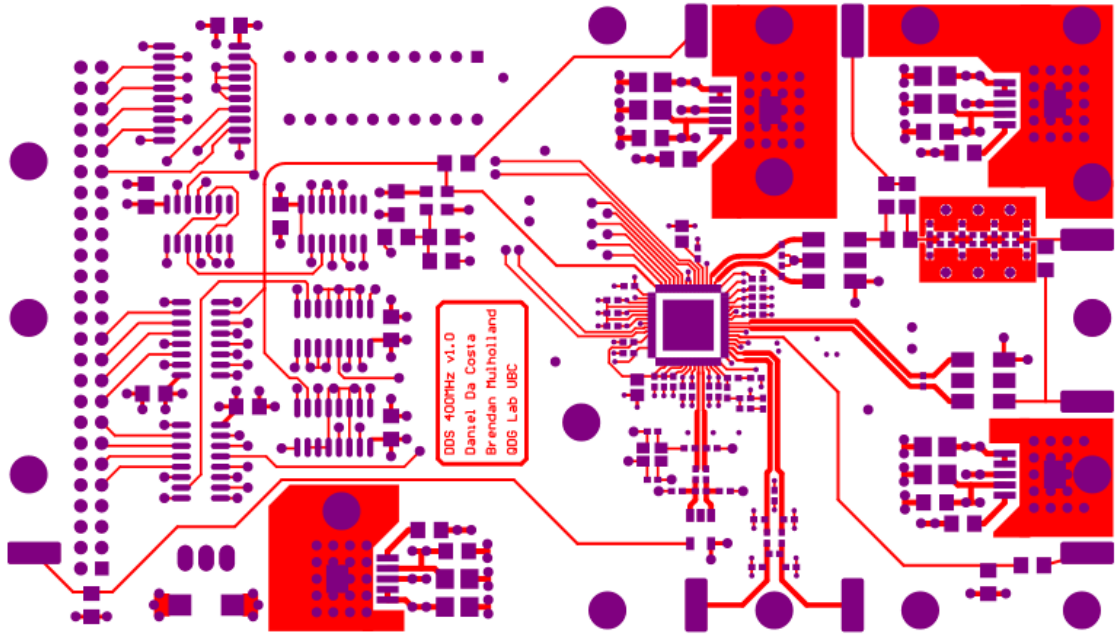


Figure 2.10: Top Side PCB layout. The top copper layout is shown in red. The top pastemask is shown in purple (shown on top of the copper layer).

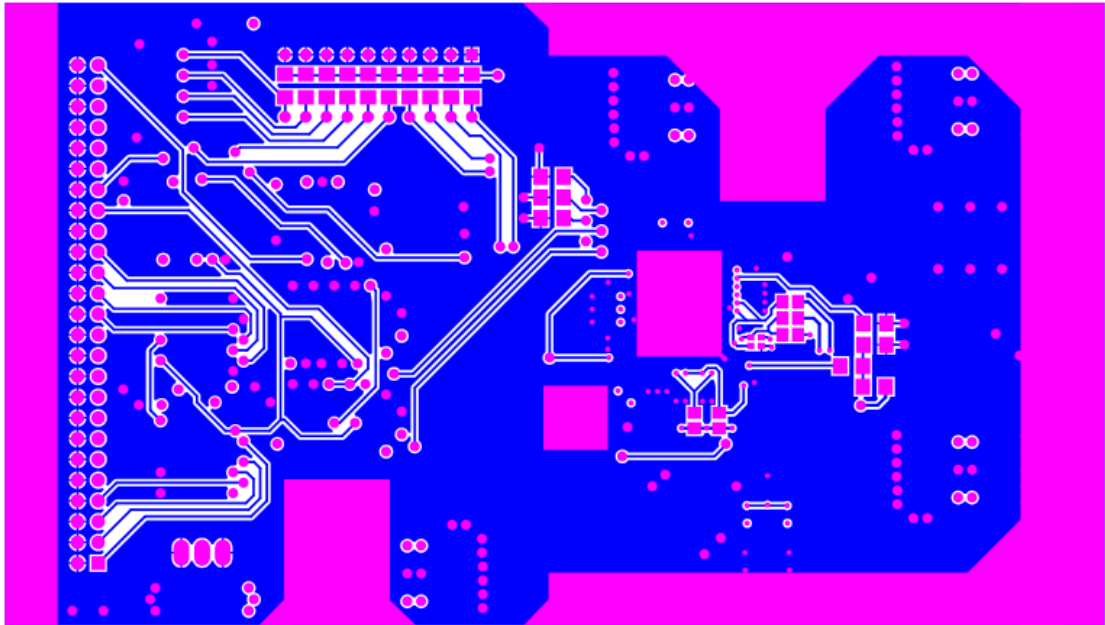


Figure 2.11: Bottom Side PCB layout. The bottom copper layout is shown in blue. The bottom pastemask is shown in pink (shown on top of the copper layer). Notice the bottom of the PCB is ground-filled and that large areas of this ground fill have been exposed (see pink areas). These regions are located along the edges of the PCB and below the AD9912 IC and the voltage regulators. They allow the PCB to be grounded to the enclosure and improve heat dissipation.

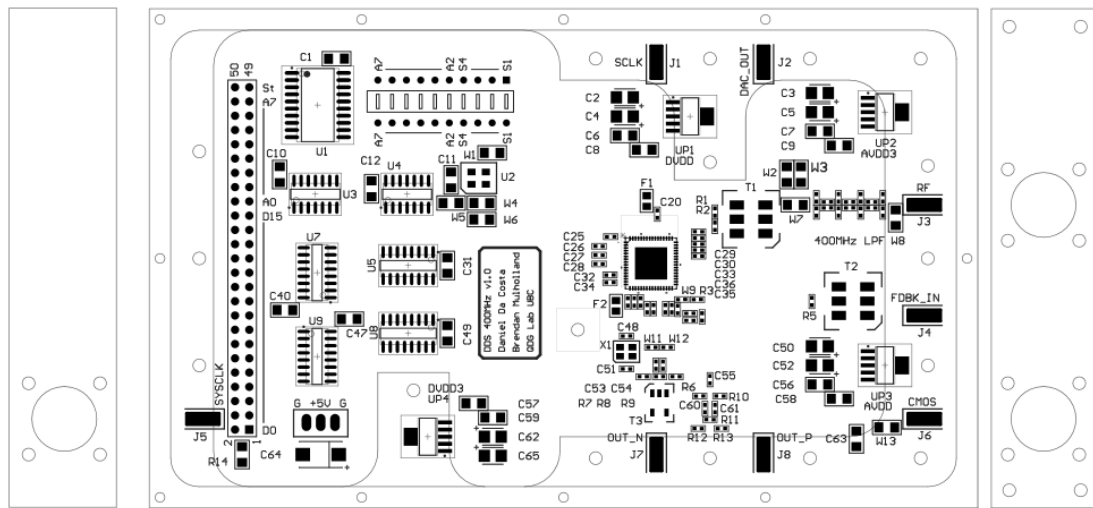


Figure 2.12: Assembly diagram showing the top pastemask and silkscreen above the enclosure and IC mechanical drawings.

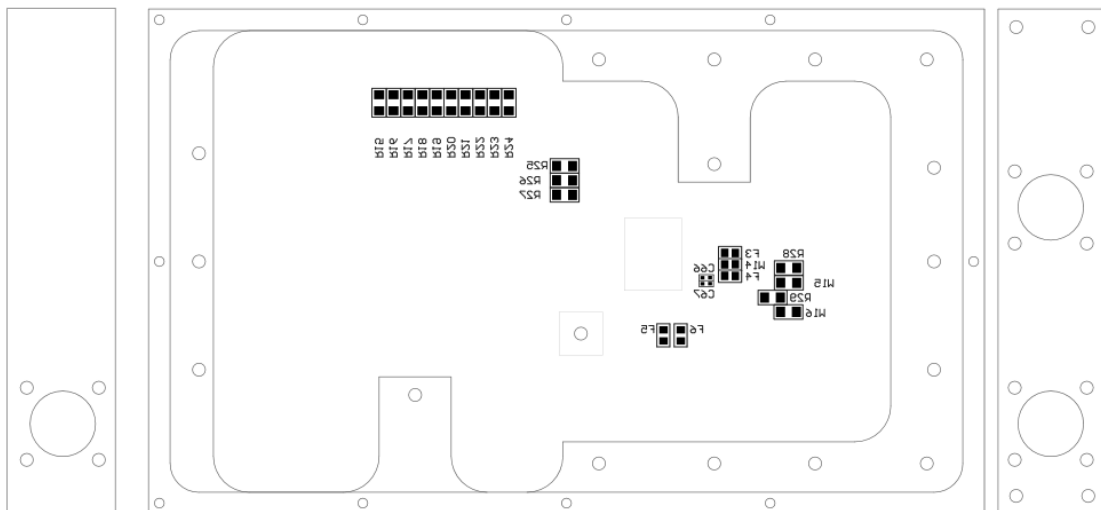


Figure 2.13: Assembly diagram showing the bottom pastemask and silkscreen above the enclosure drawings.

### 2.3.3 PCB Fabrication

The PCB layout design was used to generate fabrication files. There is a drill file, eleven Gerber files and a README file with basic fabrication instructions. The eleven Gerber files are shown in Appendix B.

The boards are  $5.3'' \times 3''$ , which is the same size as the previous generation DDS devices. They are four-layer boards (top signal, ground, power, bottom signal), which is again the same as the previous generation DDS devices. They were fabricated using FR-406 dielectric material (4.350 dielectric constant, 9.6 mils (0.244 mm) thick). Each side of the board is protected and insulated with a green solder-mask and is annotated with a white silkscreen. The PCBs were fabricated by Advanced Circuits. An electrical test was also performed by Advanced Circuits.

Most components were sourced by our team and ordered from Newark. At time of writing, the Department of Physics and Astronomy (PHAS) electronics shop was in the process of assembling a single prototype device. The device is expected to be complete within two or three days of the submission of this report. We provided them with all necessary parts (except ferrite beads) and assembly instructions.

Figures 2.14 and 2.15 are photos of the top and bottom of the PCBs. These photos were taken after the assembly process had begun. Several components are installed, including the AD9912 IC itself.

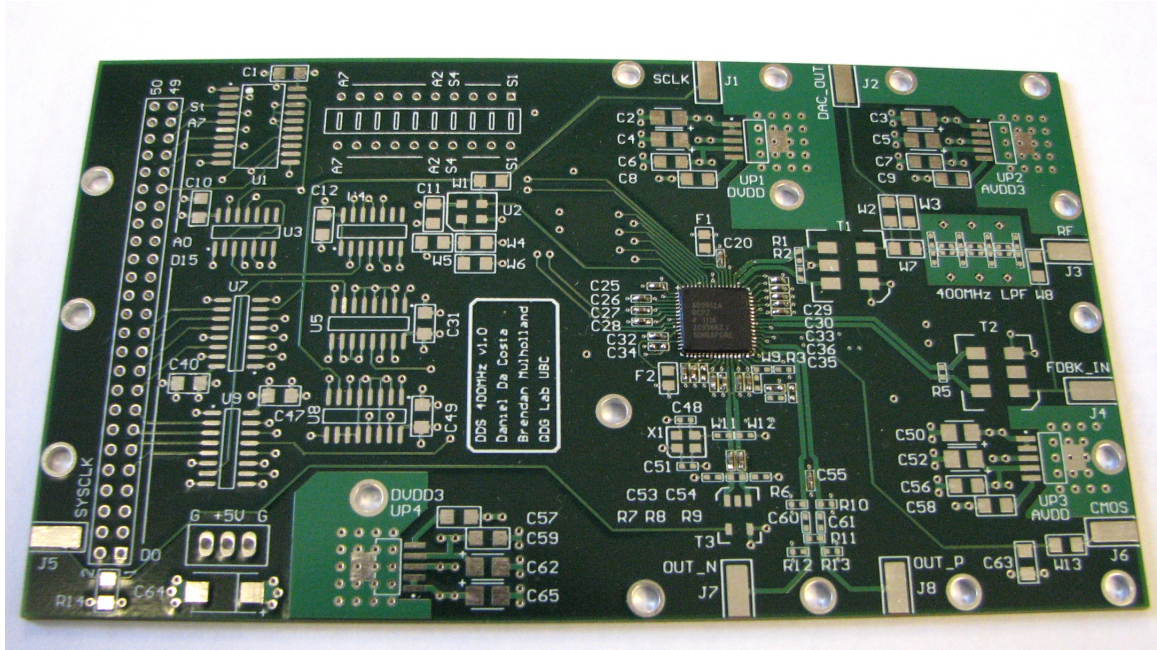


Figure 2.14: Photo of the PCB, top side. Some components have been installed.

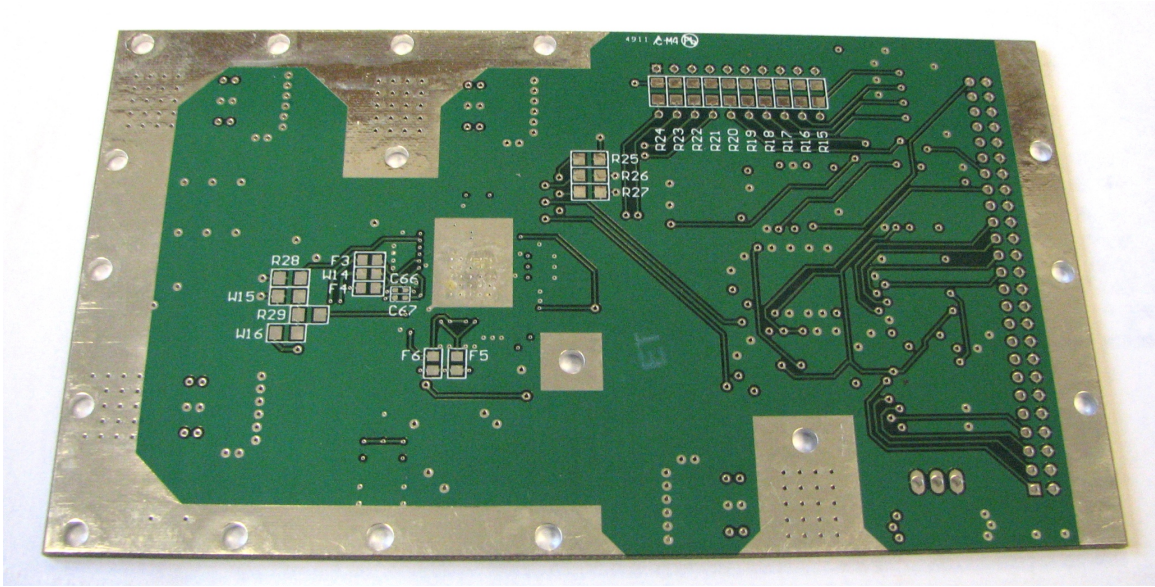


Figure 2.15: Photo of the PCB, bottom side, no components.

### 2.3.4 Enclosures

The enclosure is made of aluminium and has two pieces: a body and a lid. The enclosure design was based upon Todd Meyrath's work[9]. Due to the increased complexity of our design, it was found that the original enclosures would short many of the PCB vias. Avoiding these shorts through changing the PCB was found to be impractical due to space constraints. For this reason, the original enclosure was modified to minimize the metal surface in contact with the PCB while maintaining structural integrity. The decreased contact area provided adequate area for the vias.

The enclosure was grounded in a number of ways. The primary method of grounding is through the screws attaching the PCB to the enclosure, which ensures both a tight fit and adequate return paths. However, the areas of the bottom of the PCB in direct contact with the enclosure were also ground filled and exposed to allow for further contact. This grounding is particular important, as the BNC connectors used obtain their ground only from the enclosure itself.

The New Jersey-based on-line machine shop company eMachineShop was chosen as the supplier ([www.emachineshop.com](http://www.emachineshop.com)). eMachineShop was the supplier for the enclosures used for the AD9852-based DDSs (upon which the new design is based). The enclosures were designed using eMachineShop's proprietary software, also called eMachineShop. Fifteen enclosures have been ordered from eMachineShop and are expected to arrive within two to three weeks of the submission of this report.

Figure 2.16 is a labelled diagram of the enclosure body, shown from the top. Green dotted lines indicate the approximate outlines on the PCB of the four LDO voltage regulators and the AD9912 IC. Shown are ten 4-40 threaded holes and fourteen 8-32 threaded holes, used for mounting the enclosure lid and the PCB, respectively. Gray dotted lines indicate sixteen 4-40 threaded mounting holes, twelve of which are for mounting three BNC receptacles and four of which are for mounting the enclosure to a rack.

The lid is unchanged from the previous design and is shown in Figure 2.17. Shown are twelve 4-40 clearance holes, used to mount the enclosure lid onto the body (two of these holes will be unused as they have no matching hole in the body). Two spaces are cut into the lid to allow for the 50-pin data and 3-pin power connectors.

Designs for rack mounting brackets also exist. Each bracket allows up to eight DDS devices to be mounted to the electronics racks in the QDG lab. The design was modified slightly from an existing design; the spacing of mounting holes were changed to be compatible with the intended

racks. Five<sup>14</sup> brackets have been ordered. At time of writing, the rack mounting brackets have already been fabricated and are in transit.

Figure 2.18 shows a 3D rendering of the enclosure, created using eMachineShop software.

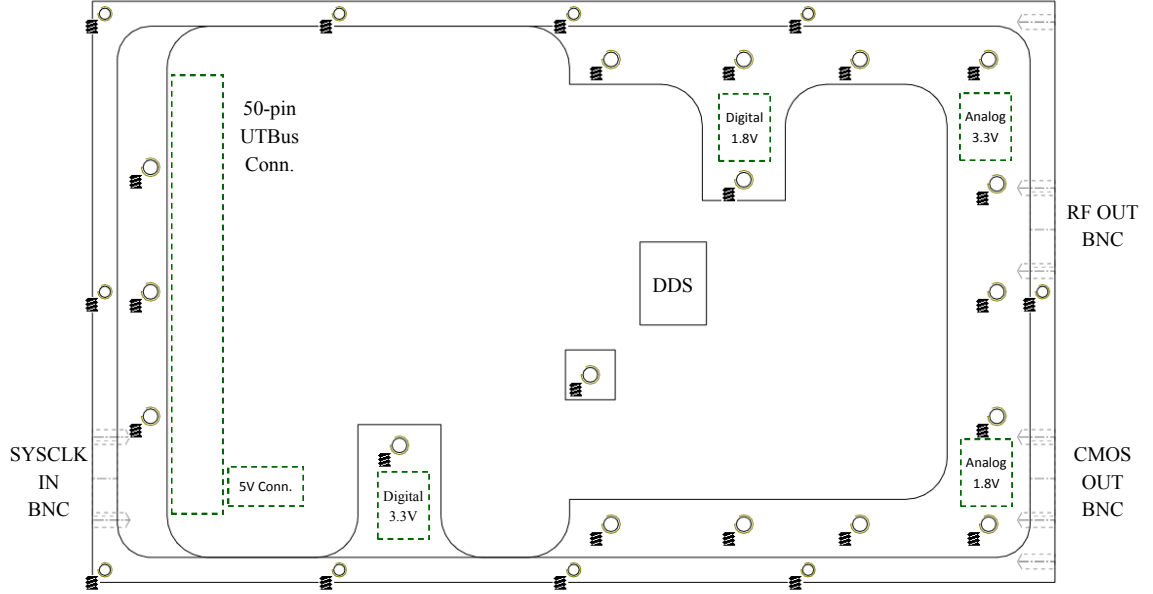


Figure 2.16: Labelled diagram of the enclosure body (top view). Green dotted lines indicate the approximate outlines on the PCB of the four LDO voltage regulators and the AD9912 IC.

<sup>14</sup>Not all of these brackets are intended for this project. Extra brackets were ordered at the request of the QDG lab.



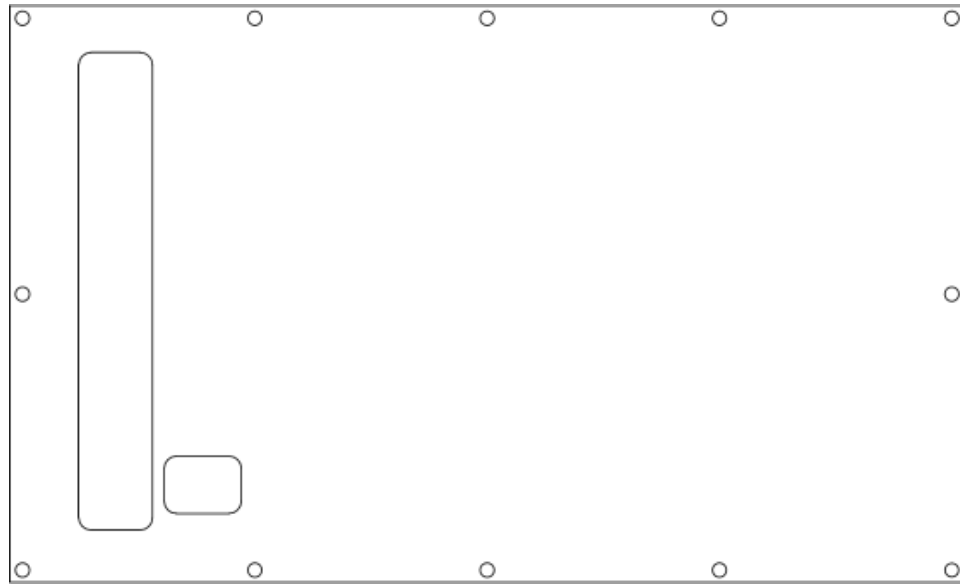


Figure 2.17: Diagram of the enclosure lid (top view). This design is unchanged from the design used for the previous generation DDS devices at the QDG lab.

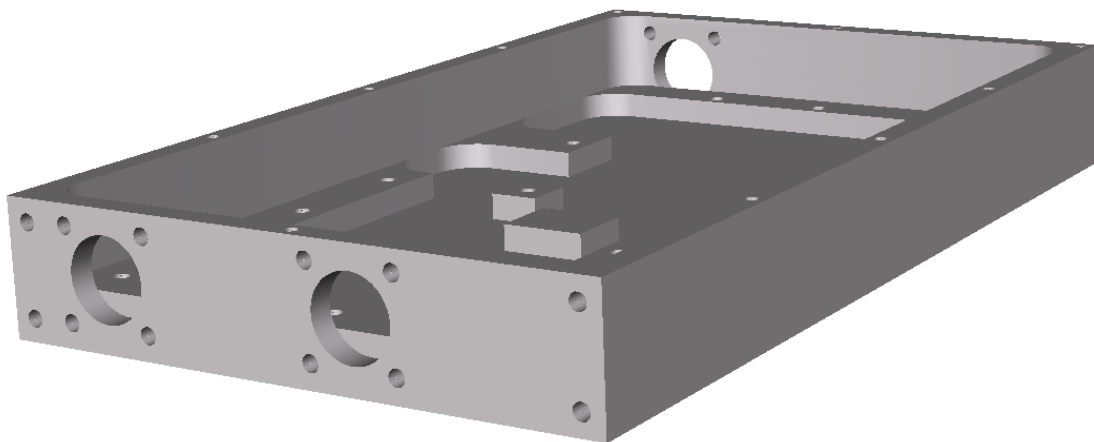


Figure 2.18: 3D rendering of the enclosure, created using eMachineShop software.

## 2.4 Board Features

This section will begin by discussing the device’s available inputs and outputs, the 10-position switch used to specify the board address and AD9912 start-up configuration, and the possible configurations which are possible when the device is assembled.

### 2.4.1 Inputs and Outputs

Table 2.4 lists the connection pads available on the PCB for BNC Connector mounting. Note that only J3, J5 and J6 are intended for mass production, and the enclosure design reflects this (see Section 2.3.4).

Table 2.4: List of connection pads available on the PCB designed for BNC Connector mounting. Note that only J3, J5 and J6 are intended for mass production, and the enclosure design reflects this.

Designator	Name	Mass Production?	Description
J1	SCLK	No	digital control clock input
J2	DAC_OUT	No	unfiltered RF signal, or input to reconstruction filter for debugging
J3	RF	Yes	filtered RF output signal
J4	FDBK_IN	No	input to the AD9912’s on-chip comparator
J5	SYSCLK	Yes	main clock input
J6	CMOS	Yes	programmable clock output (CMOS-level)
J7	OUT_N	No	differential programmable clock output (negative)
J8	OUT_P	No	differential programmable clock output (positive)

### 2.4.2 DIP Switch

A 10-position DIP-package single-pole single-throw switch is shared between the six board address bits and the four AD9912 start-up configuration bits (S1,S2,S3 and S4). Each switch is labeled on the silkscreen on the top side of the PCB. With the switches closed, the connections are grounded. With the switches open, the connections are pulled to the 3.3V digital rail through 10k $\Omega$  resistors.

The AD9912 start-up configuration bits on the AD9912 allow control of the default start-up output frequency and the system clock input mode (PLL enabled or bypassed). A decoding of the configuration bits is reproduced from the AD9912 datasheet in Table 2.5[3].

### 2.4.3 Configuration Options

The DDS device has various functionality and options that may be enabled, disabled or switched between by placing or not placing various components. Here we summarise all options of the board and provide details on how to use them. Table 2.7 summarizes the key options and gives details on specific components which need to be omitted for each option.

#### 2.4.3.1 SYSCLK

The DDS device is intended to be clocked with an external clock source on BNC connector J5. However, the option is provided to use an onboard crystal oscillator.

In the QDG lab, the off-board SCLK will originate from a 10MHz rubidium clock with another DDS being used to increase the frequency as needed (the CMOS clock driver of the AD9912 or AD9852 equivalent are possible). For more information, see Section 2.1.5.2.

Table 2.5: Options for Power-Up Default Frequencies on the AD9912, for 1GHz System Clock. Adapted from the AD9912 datasheet[3]. These options can be changed on the device by toggling four PCB-mounted switches.

S4	S3	S2	S1	SYSCLOCK Input Mode	Output Frequency (MHz)
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

#### 2.4.3.2 SCLK

It is possible to use either a clock oscillator or an external clock source to drive SCLK. The intention is to use an on-board clock oscillator (nominally 25MHz, but this will be determined after testing). For more information, see Section 2.1.5.1.

#### 2.4.3.3 SCLK Enable Pin

If the on-board clock oscillator is to be used, one of W4, W5 and W6 must be installed in order to enable the clock oscillator.

The board provides jumpers allowing the SCLK enable pin to be connected to ground (W4), 3.3V (W5) or the address comparator output<sup>15</sup> (W6). The address comparator output is LOW when the address matches.

#### 2.4.3.4 CMOS Clock Driver Voltage

The CMOS clock driver output voltage can be configured to be either 1.8V or 3.3V, depending on the supply voltage present on the VDD\_SCLK pin. The board provides two 0805 footprints (F4 and W14) allowing a jumper or ferrite bead to connect the pin to either voltage rail. For more information, see Section 2.1.1.

#### 2.4.3.5 PLL

When the PLL is enabled, follow Table 2.6 when choosing values for the loop filter components. See the circuit schematic shown in Figure A.6 for context. The PLL can be enabled or bypassed on the AD9912 by writing a 0 or 1 to Register 0x0010, Bit 4[3]. The default can be controlled through startup pin S4. The N-divider should also be set (Register 0x0020, bits 4:0); see the AD9912 datasheet for more information. This N divider will be half of the PLL multiplier; since N is restricted to  $2 < N < 33$ ,  $4 < \text{PLL multiplier} < 66$ . For more information, see Section 2.1.5.3.

<sup>15</sup>We aren't really sure if this is useful, but we thought it might be, so we included it. The idea is that the clock oscillator will turn off if the board isn't being talked to by the UTBus. This would reduce power usage and possibly noise, but may introduce new complication during programming.



Table 2.6: Recommended Loop Filter Values for a Nominal 1.5MHz SYSCLK PLL Loop Bandwidth. Adapted from the AD9912 datasheet[3]. Designators have been taken to match actual designators in PCB design. See the circuit schematic shown in Figure A.6.

Multiplier	R4	Series C46	Shunt C45
8	390 $\Omega$	1nF	82pF
10	470 $\Omega$	820pF	56pF
20	1k $\Omega$	390pF	27pF
40 (default)	2.2k $\Omega$	180pF	10pF
60	2.7k $\Omega$	120pF	5pF

#### 2.4.3.6 RF Path

It is desirable to be able to characterise the reconstruction filter. To do so, the board provides an option to connect BNC connector J2 directly to the input of the reconstruction filter. To use this option, place jumper W3 and do not place jumpers W2 or W7. To monitor the pre-filter single-ended AD9912 DAC output on BNC connector J2 instead, place W2. For normal operation, place only W7.

The jumper W8 can be used to connect the filtered DAC output to the AD9912 FDBK\_IN inputs (these drive the clock drivers). If either clock driver is to be used, install W8. If the clock drivers are not used, W8 should be omitted, and T2 and R5 are unnecessary.

Table 2.7: List of all device configuration options. In general, all components should be installed except those listed beside the desired options.

Option	Components to omit
SYSCLK	
(1) XTal	C53 C54 R7 R8 R9 R14 T3 W15 <sup>1</sup>
(2) External	W11 W12 X1 C48 C51 W16 <sup>1</sup>
SCLK	
(1) Clock Oscillator <sup>2</sup>	W1
(2) External	U2 W4 W5 W6
CMOS Voltage	
(1) 1.8V	F4 <sup>1</sup>
(2) 3.3V <sup>3</sup>	W14 <sup>1</sup>
PLL	
(1) Disabled	C45 C46 R4 W10
(2) Enabled <sup>4</sup>	R3 W9
RF Signal Path <sup>5</sup>	
(1) Clock Drivers Disabled	C55 C60 C61 C63 R5 R6 R10 R11 R12 R13 T2 W2 W3 W8 W13
(2) Clock Drivers Enabled	W2 W3

<sup>1</sup> These components are located on the bottom side of the PCB.

<sup>2</sup> The clock oscillator used has an enable pin that could be either active high or active low; see Section 2.1.5.1.

<sup>3</sup> W14 uses the same (0805) package as the ferrite beads, allowing a ferrite bead to be used instead of a jumper if desired. See Section 2.1.7

<sup>4</sup> If PLL is enabled, the loop filter components must be chosen according to Table 2.6

<sup>5</sup> These are the conventional options are for normal operation. There are several other possible configurations available; see Section 2.4.3.6.

## 2.5 Breadboard Testing

In order to verify functionality of the parallel to serial converter, the circuit was constructed and tested on a breadboard. The PHAS electronics shop provided 8-bit shift registers (CD74HCT165E) and flip-flops (74HCT74N) in DIP packages for testing. The components used are functionally similar to the SN74HC166 shift registers and SN74HC74 flip-flops, which are the intended components. However, the HCT165E shift registers have an asynchronous load while the SN74HC166 have a synchronous load. The slight difference in shift register functionality does not fully compromise the test, however it does lead to some undesirable output as discussed below.

Switches were used to statically simulate the address comparator output, the strobe and 16-bit data input (arbitrarily set to 1010 1010 1001 0101<sub>2</sub>). The outputs were monitored with an oscilloscope. Results are shown in Figure 2.19. Note that, as expected, the CSB was held low while the data was clocked out on SDIO.

The undesirable output is indicated graphically on the SIO and CSB subplots of Figure 2.19. Both signals responded too soon to the  $\overline{SH}/\overline{LD}$  signal due to the asynchronous load of the HCT165E shift registers.

The DDS device is designed to use the SN74HC74 shift registers, which have a synchronous load. The result will be that the output will not respond to a change in the  $\overline{SH}/\overline{LD}$  signal until a rising edge of the clock. The red lines shown in Figure 2.19 indicate the desired output.

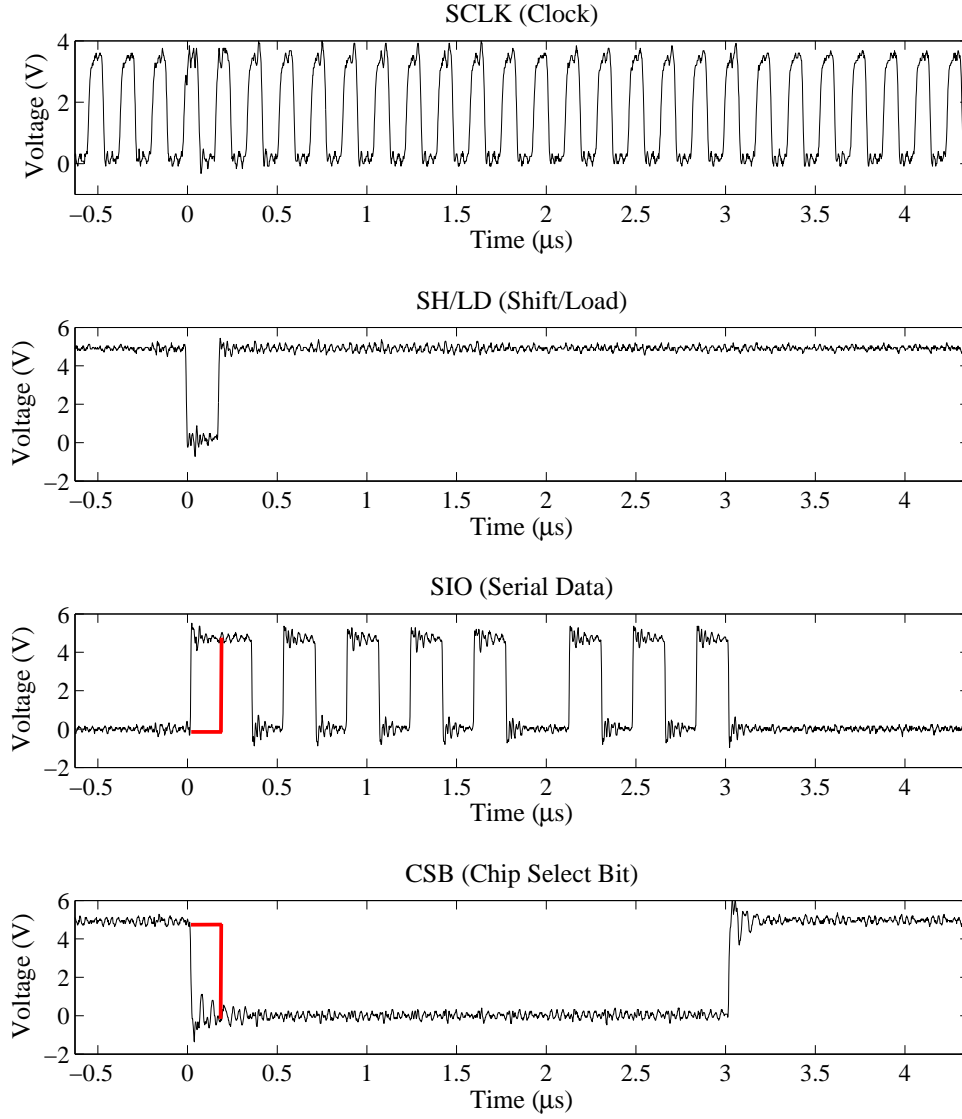


Figure 2.19: Parallel-to-serial converter breadboard test results. This test simulates the writing of the (arbitrarily chosen) 16-bit number  $1010\ 1010\ 1001\ 0101_2$  to the AD9912 serial control port. The top graph shows the clock, which was operating at 5.642MHz. A function generator was used. Below this, the  $SH/\overline{LD}$  graph illustrates the functioning of the load pin. When this signal is low, the 16-bits of data on the UTBus are latched into two 8-bit shift registers on the DDS device. When high, shift register contents are clocked into the AD9912. Second from the bottom, the SIO data plot illustrates the data output from the shift registers. The results are not as desired, but this is expected due to using parts not from the design (CD74HCT165E shift registers were used in place of SN74HC74). The red lines illustrate the desired behaviour. The bottom graph shows that the CSB, which is implemented identically to the SIO and demonstrates the same issue.

## 3

# Conclusions

This report studied the operation of the AD9912 and described in detail the elements of its operation which are relevant to the project.

A conceptual design satisfying the project requirements has been created and presented. As required, the design is compatible with the existing UTBus control interface and is designed to provide a sinusoidal output signal at frequencies from 8 to 400MHz.

The reconstruction filter design was borrowed from the design given for the AD9912 evaluation board, Rev. B. This design has been verified through a SPICE simulation and the resulting theoretical transfer function has been presented. This transfer function meets the desired performance specifications: 400MHz cut-off frequency, a roll-off within 100MHz and a minimum of 60dB of attenuation in the stop-band.

Altium Designer was used as the software tool in creating connectivity-level schematics and PCB fabrication files. The new PCB design uses the same board dimensions, I/O connectors and layer stack-up as Todd Meyrath's AD9852 design.

The functionality of the parallel to serial converter design has been verified through a physical breadboard test. Unfortunately, the exact components specified by the design were not available at the time and so substitutes of similar functionality were used instead. This did lead to some undesirable output, however it did not fully compromise the test. The difference between the desired output and actual output was minor and easily predictable given the functionality of the devices as described in their datasheets.

Twenty PCBs have been fabricated by Advanced Circuits and are now in the possession of the QDG lab.

Enclosures for the devices were designed using eMachineShop's proprietary software. The design is a modification of the previous generation AD9852 enclosure design. It is not conveniently compatible with the previous generation devices. Fifteen enclosures have been ordered from eMachineShop and are expected to arrive within two to three weeks of the submission of this report. Five rack mounting brackets have been ordered, each supporting up to eight DDS devices. The rack mounting brackets have already been fabricated and at time of writing are in transit.

At time of writing, the PHAS electronics shop was in the process of assembling a single prototype device. The device is expected to be complete within two or three days of the submission of this report. Our team provided them with all necessary parts<sup>1</sup> and assembly instructions.

Since the prototype device was not complete at time of writing, no testing has been done. As such, no claims are made regarding the actual functionality and performance of the device. Our team intends to test the prototype device and either verify correct basic operation or identify any serious issues. Part II to this report will document testing procedures, testing results and all recommendations. It will be submitted January 9, 2012.

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<sup>1</sup>With the exception of ferrite beads.

## 4

# Project Deliverables

At time of writing, a single PCB is in the PHAS electronics shop being assembled. The board is expected to be complete during the week of January 9, 2012. Our team will test the device in order to verify correct basic operation of the device or detect any serious issues. No extensive performance characterization will be performed. A Part II to this report will be submitted on January 20, 2012, documenting the testing procedures, the results and all recommendations.

## 4.1 List of Deliverables

The following is a list of the deliverables given in the original proposal for this project, *Proposal to Construct a Direct Digital Synthesizer*. The description of each deliverable is copied verbatim. For each deliverable the current state is described.

- The results of the SPICE simulation of the low-pass filter. In particular, a plot showing the transfer function of the circuit will be provided.
  - The simulation is complete and shows that the filter should work as desired.
  - The design was borrowed from the design given for the AD9912 evaluation board, Rev. B.
  - Electronic copies of the files used for testing and the results will be provided.
- Schematic diagram of the DDS device and a full parts list.
  - The schematics are complete and all parts have been chosen and sourced.
  - Electronic copies of the schematics, parts list and a working Bill of Materials will be provided electronically.
- PCB layout of the DDS device.
  - The PCB layout is complete and has been used to build a PCB with no issues during manufacturing.
  - The PCBs will be left in the drawer the QDG lab has provided for DDS parts.
- Detailed description of testing procedures and results. Performance of the device will be quantified wherever possible.
  - The testing has not yet been completed due to time constraints.
  - An assembled board should be received on January 9, 2012 and testing will begin then.
  - Details of testing procedures and results will follow this report in a Part II.
- The functioning prototype device.

- The prototype device is expected to be received the week of January 9, 2012.
- Once testing is complete, the prototype device will be left in the DDS board drawer in the QDG lab.
- Modified enclosure design, if required.
  - Enclosures for the devices were designed.
  - The design is a modification of the previous generation AD9852 enclosure design and is not conveniently compatible with the previous generation design.
  - Fifteen enclosures as well as rack mounting brackets have been ordered from eMachineShop and are expected to arrive within two to three weeks of the submission of this report.
- Eight or more finished DDS devices, ready for integration into the QDG labs electronic experiment control system.
  - Due to time constraints, this milestone was not and will not be accomplished as part of this ENPH 479 project.
- Engineering recommendation report.
  - This document, submitted January 9, 2012, is the Engineering recommendation report.

## 4.2 Financial Summary

See Table 4.2 for a brief financial summary of the project. See Table 4.2 for a breakdown of the enclosure costs.

Table 4.1: Summary of costs associated with this project. Enclosure costs do not include front panels. Extra PCBs were ordered since the marginal cost is very low. The evaluation board was ordered because it should be a useful benchmark during performance characterization.

Description	Quantity	Vendor	Unit Cost	Total Cost
PCBs	20	Advanced Circuits	\$44.92	\$898.30
Enclosures	15	eMachineShop	\$60.59	\$908.85
AD9912	15	Analog Devices	\$50	\$750
Other Components	15 sets	Newark, Mouser, Digikey	\$43.35	\$650.26
Evaluation Board	1	Analog Devices	\$500	\$500

Table 4.2: DDS Enclosure Costs. All parts were ordered from eMachineShop. Note that only 2 of 5 front panels are intended for the AD9912 DDS devices.

Description	Quantity	Unit Cost	Total Cost
Lid	15	\$10.87	\$163.05
Enclosures	15	\$49.72	\$745.73
Front Panels	5	\$67.29	\$336.47

# References

- [1] Advanced Layout Solutions, Ltd., *Control Impedance*. 2009.
- [2] Analog Devices CMOS 300 MSPS Complete DDS, *Analog Devices 9852*. 2007.
- [3] Analog Devices, *Analog Devices 9912 1 GSPS Direct Digital Synthesizer with 14 Bit DAC*. 2010.
- [4] Analog Devices, *AD9912 Evaluation Board, Rev.0*. 2008.
- [5] Analog Devices, *Microstrip and Stripline Design*. 2009.
- [6] Douglas Brooks, *Differential Impedance*. Miller Freeman, 1998.
- [7] Keith Ladouceur, *Experimental Advances toward a Compact Dual-Species Laser Cooling Apparatus*. 2008.
- [8] Sanaz Footohi, *Control System of Quantum Degenerate Gases Laboratory*. 2006.
- [9] Todd P. Meyrath, *Digital RF Synthesizer: DC to 135 MHz*. 2005.
- [10] Texas Instruments, *PCB Design Guidelines For Reduced EMI*. November 1999.

# Appendix A

## Schematic Diagrams

This section contains the full schematic diagrams for the DDS circuit. Altium Designer was used to create these figures.

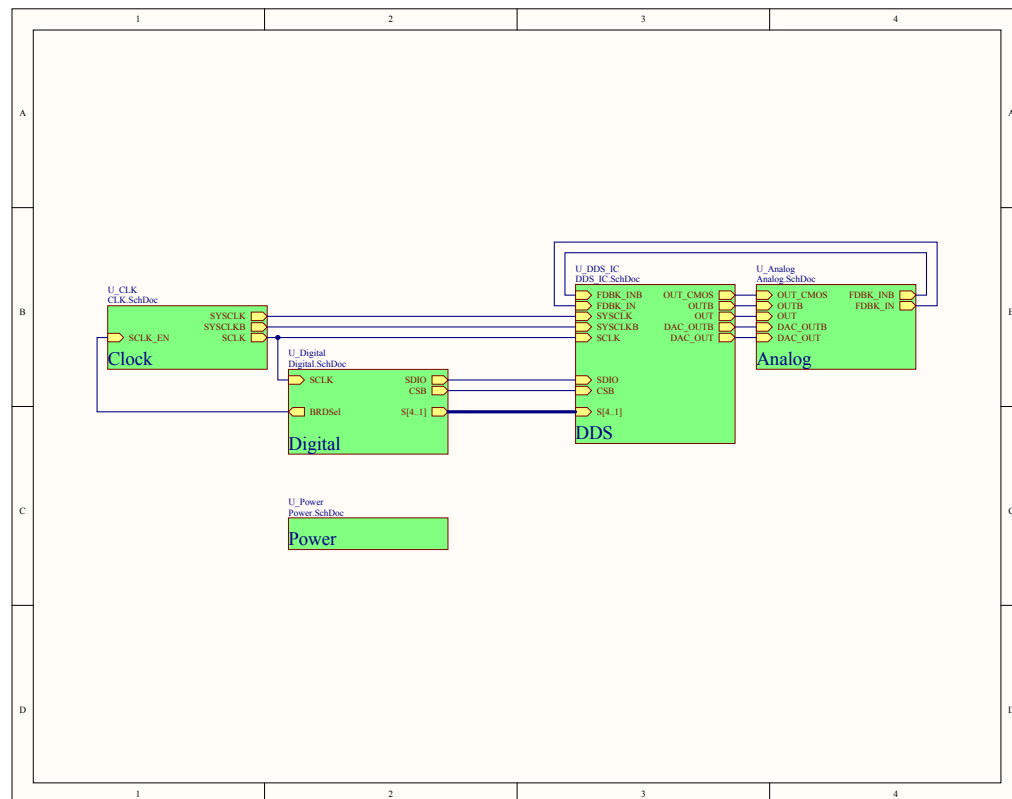


Figure A.1: Schematic diagram, top level. Top\_Level.SchDoc



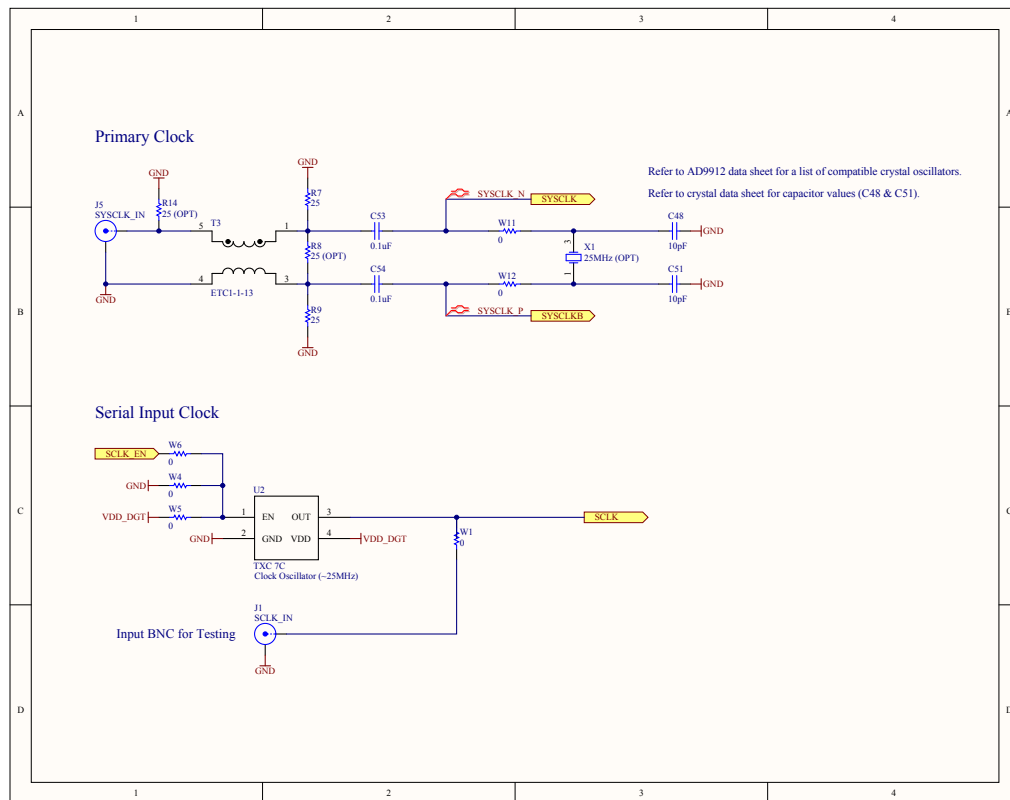
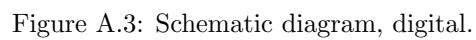


Figure A.2: Schematic diagram, clocks. CLK.SchDoc



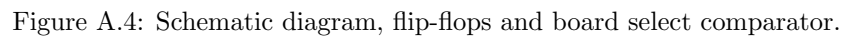


Figure A.4: Schematic diagram, flip-flops and board select comparator.

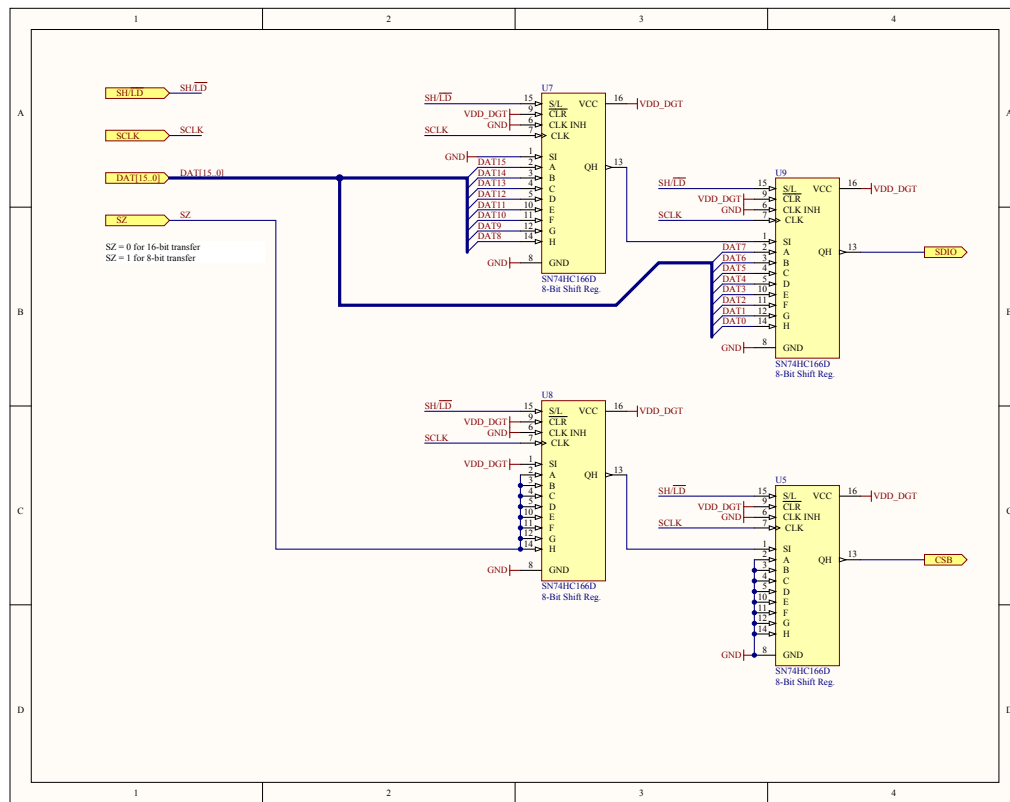


Figure A.5: Schematic diagram, parallel-to-serial converter.

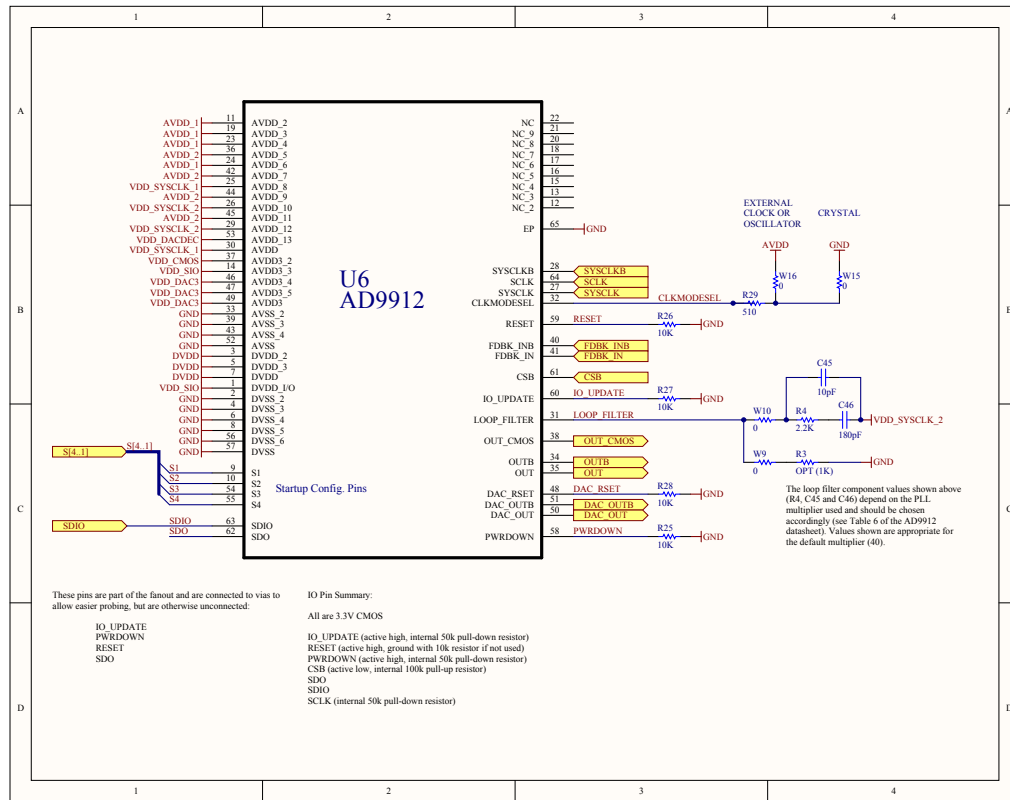


Figure A.6: Schematic diagram, AD9912.

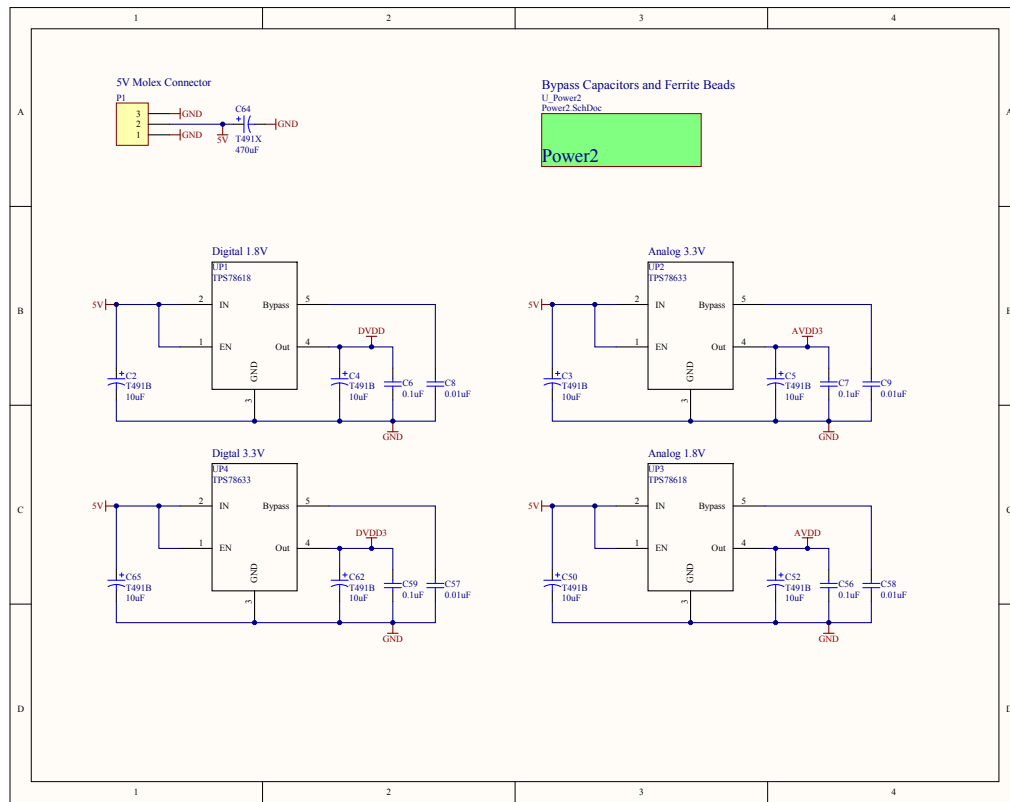


Figure A.7: Schematic diagram, power 1 (voltage regulators).

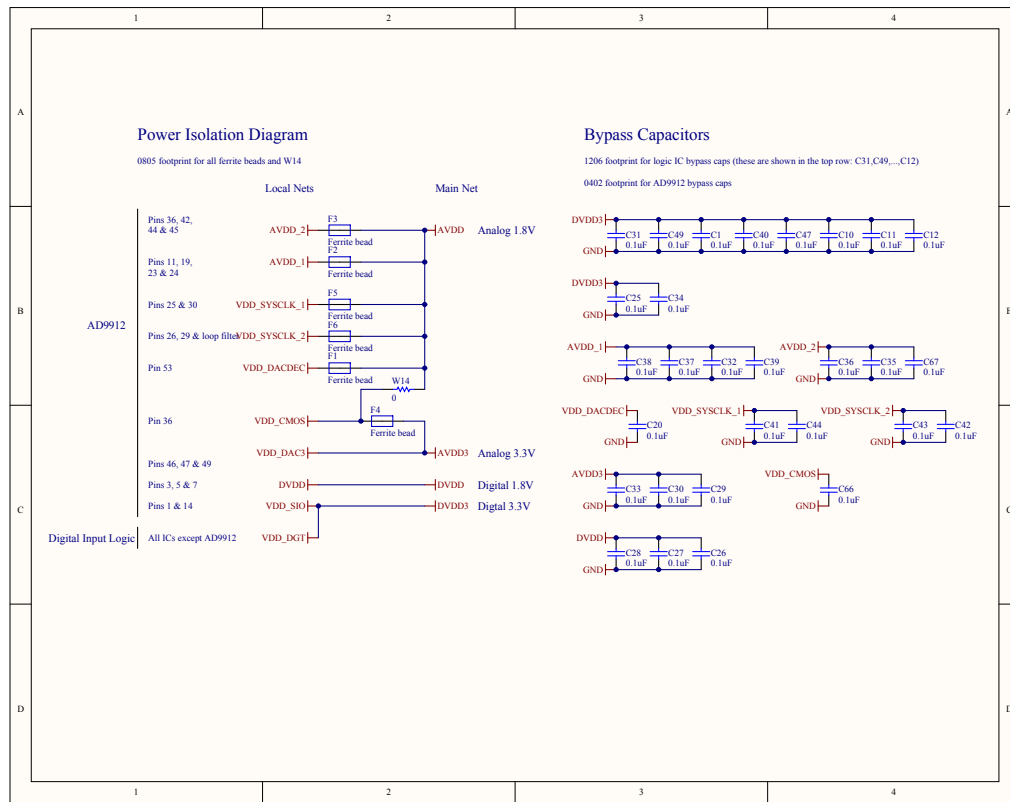
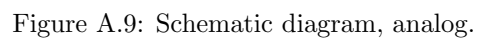


Figure A.8: Schematic diagram, power 2 (bypass capacitors and ferrite beads).





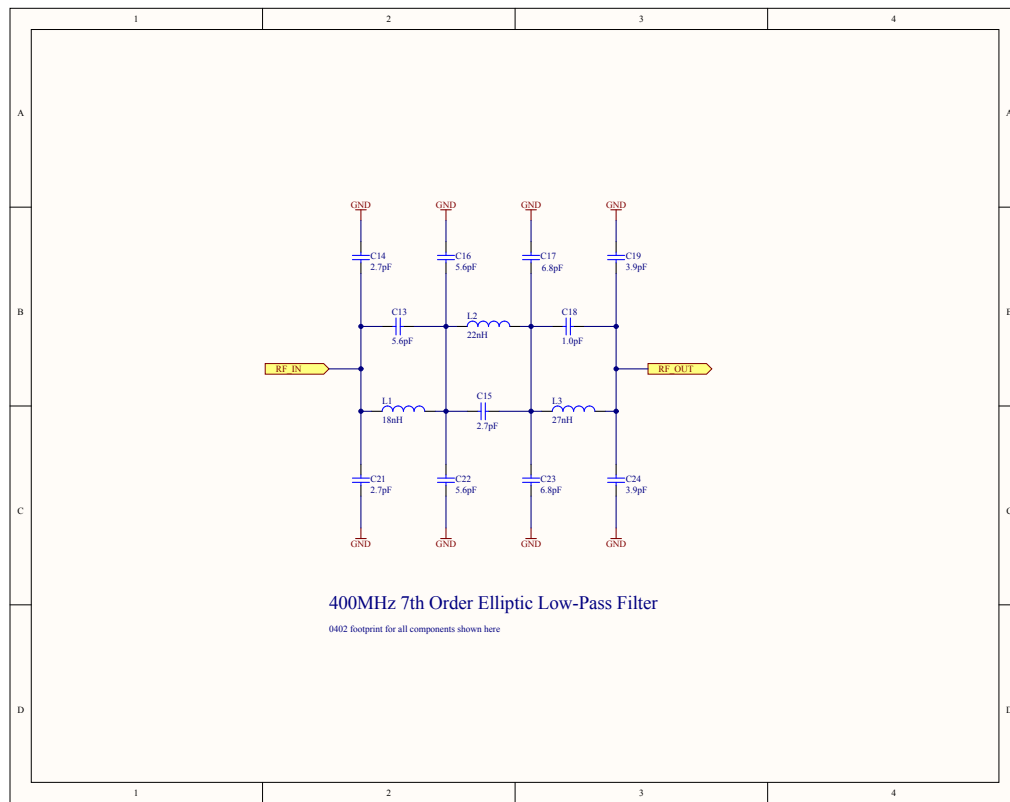


Figure A.10: Schematic diagram, reconstruction filter.

## Appendix B

# PCB Fabrication Drawings

This section contains printouts generated from the Gerber files used for PCB fabrication. These files, along with hole/via drilling information provide the PCB manufacturer with most of the information needed to construct the boards. Unless noted in the caption, the Gerber files shown are positive, meaning that dark areas indicate that material should be present (either copper, the insulating soldermasks or the silkscreens). The ground and power plane files are negative, meaning that dark areas indicate that material should be removed.

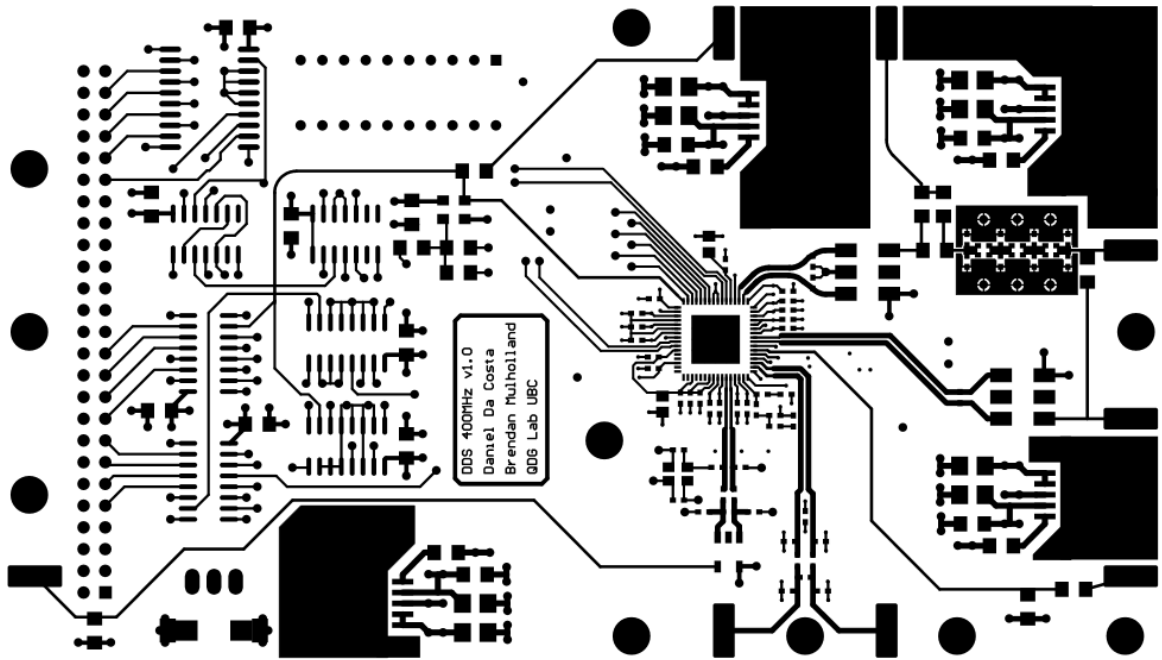


Figure B.1: Fabrication Drawings, top copper layer.

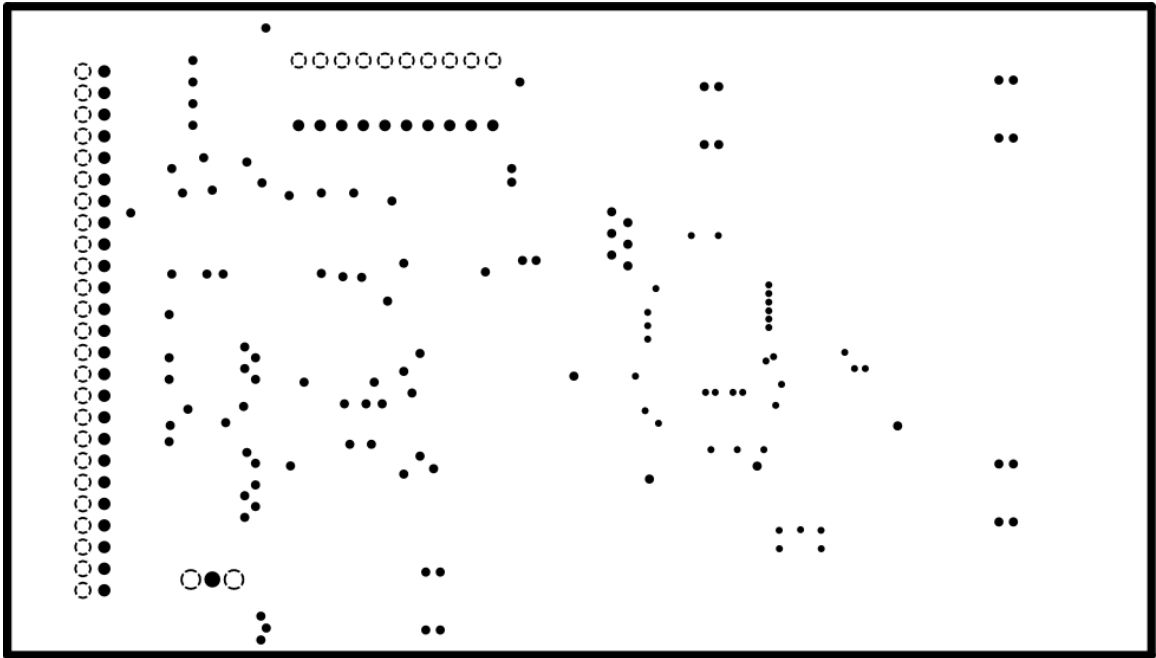


Figure B.2: Fabrication Drawings, ground plane (negative).

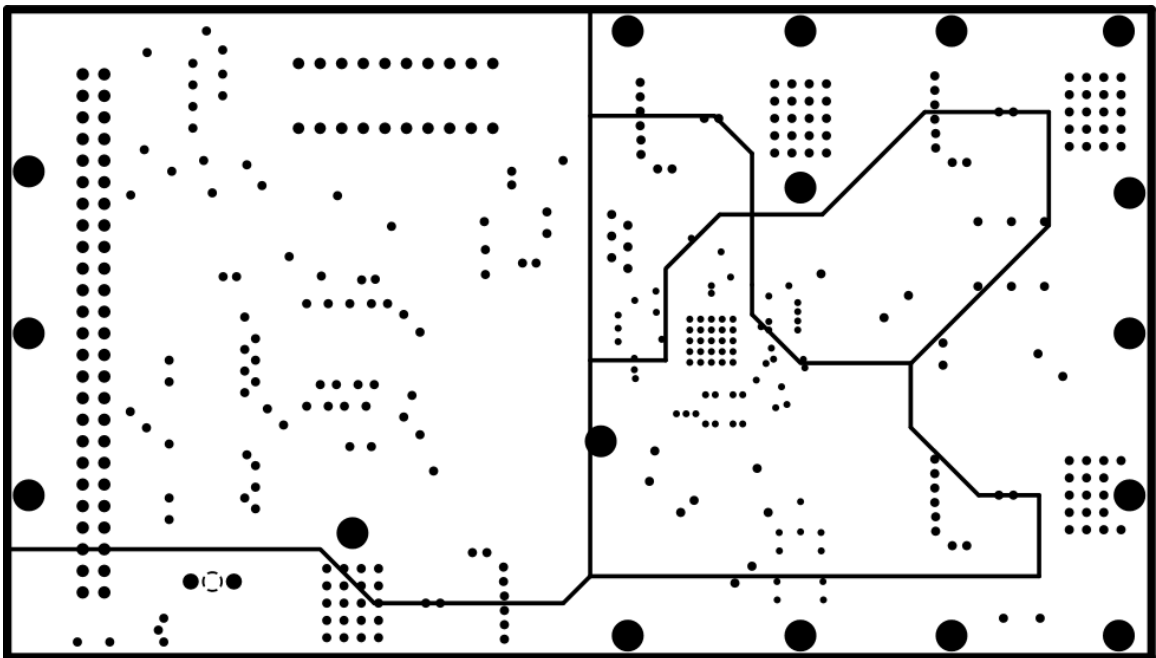


Figure B.3: Fabrication Drawings, power plane (negative).

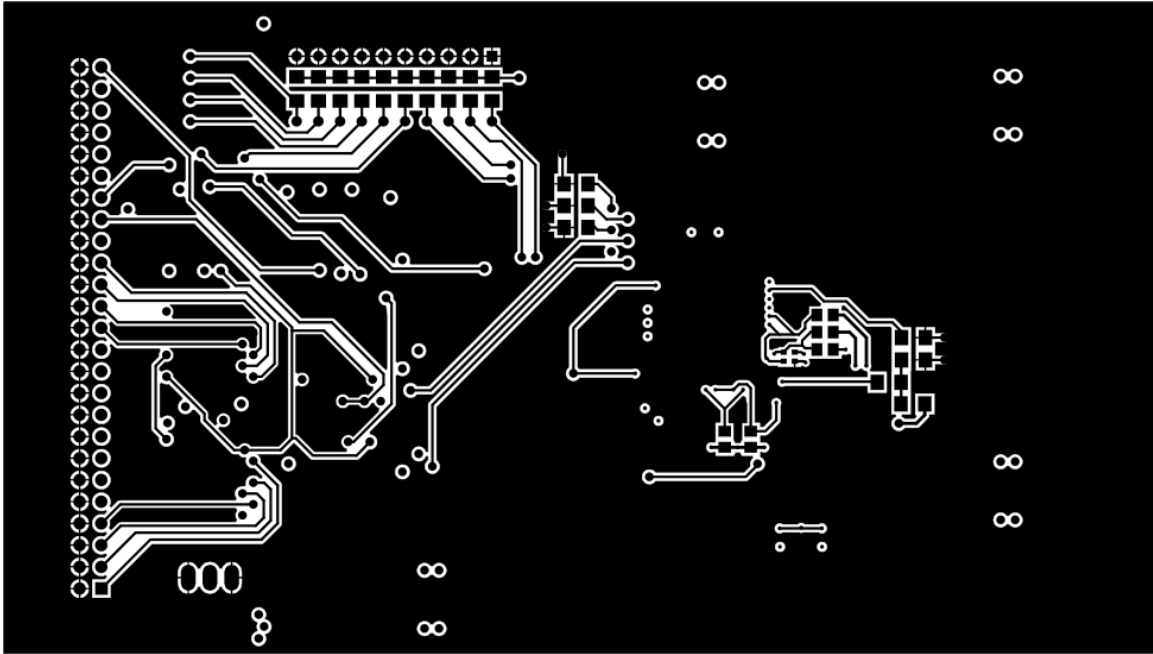


Figure B.4: Fabrication Drawings, bottom copper layer.

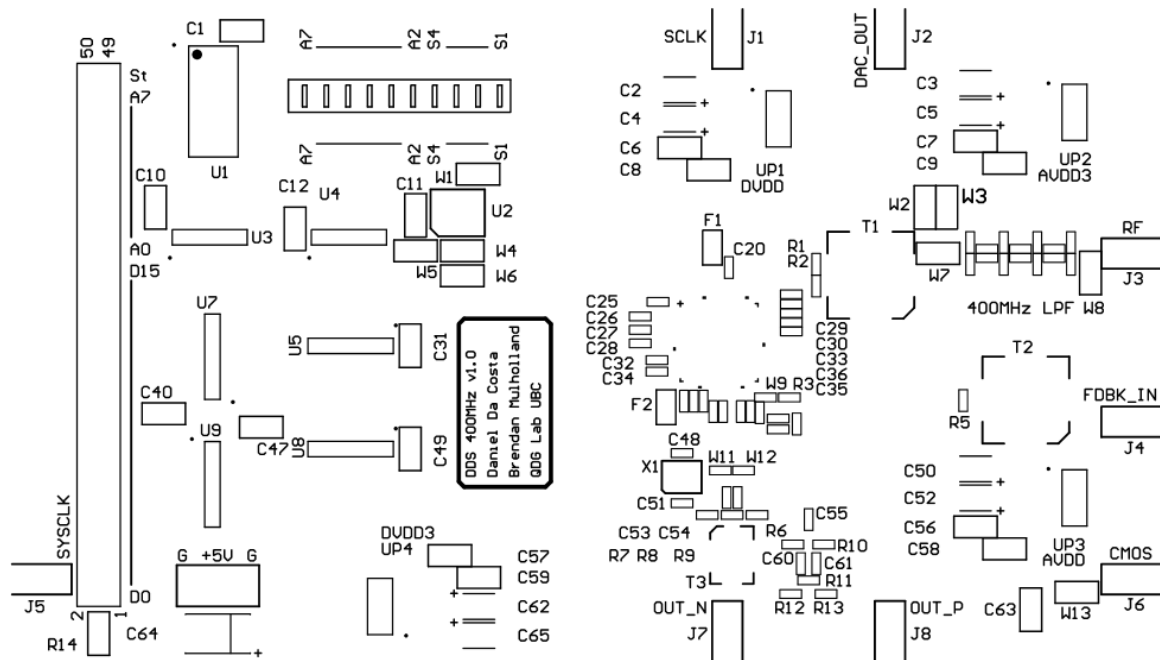


Figure B.5: Fabrication Drawings, top silkscreen.

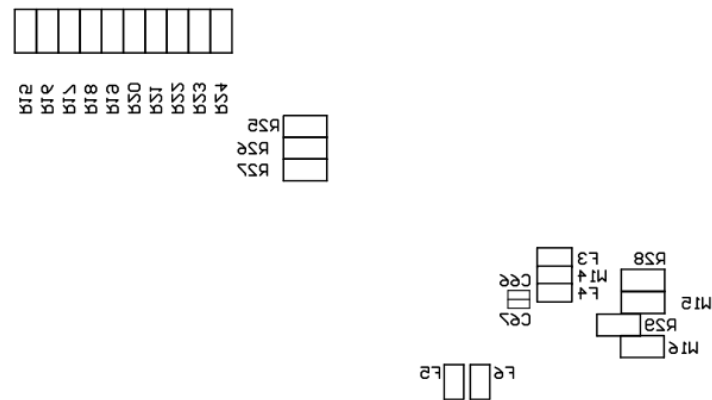


Figure B.6: Fabrication Drawings, bottom silkscreen.

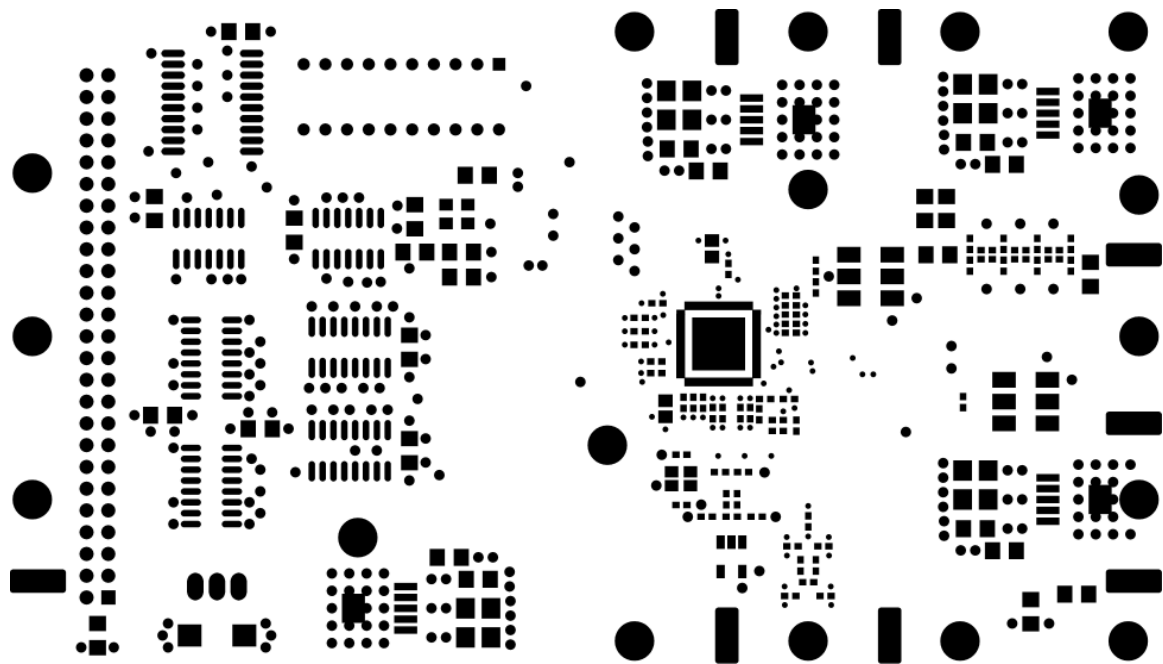


Figure B.7: Fabrication Drawings, top soldermask.

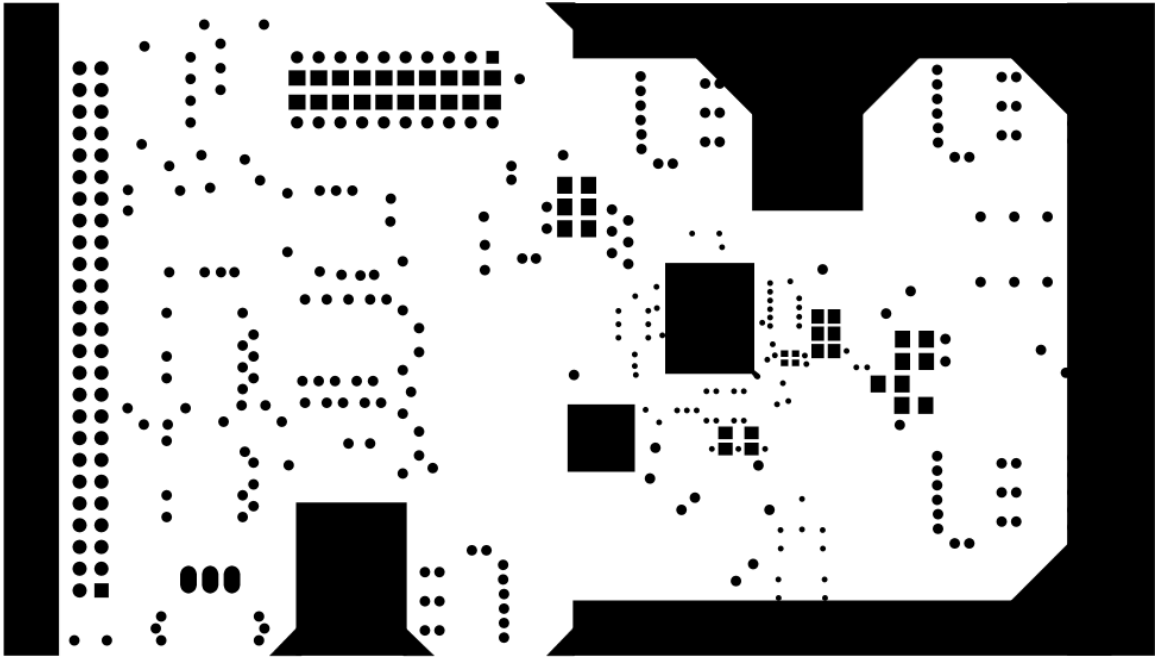


Figure B.8: Fabrication Drawings, bottom soldermask.

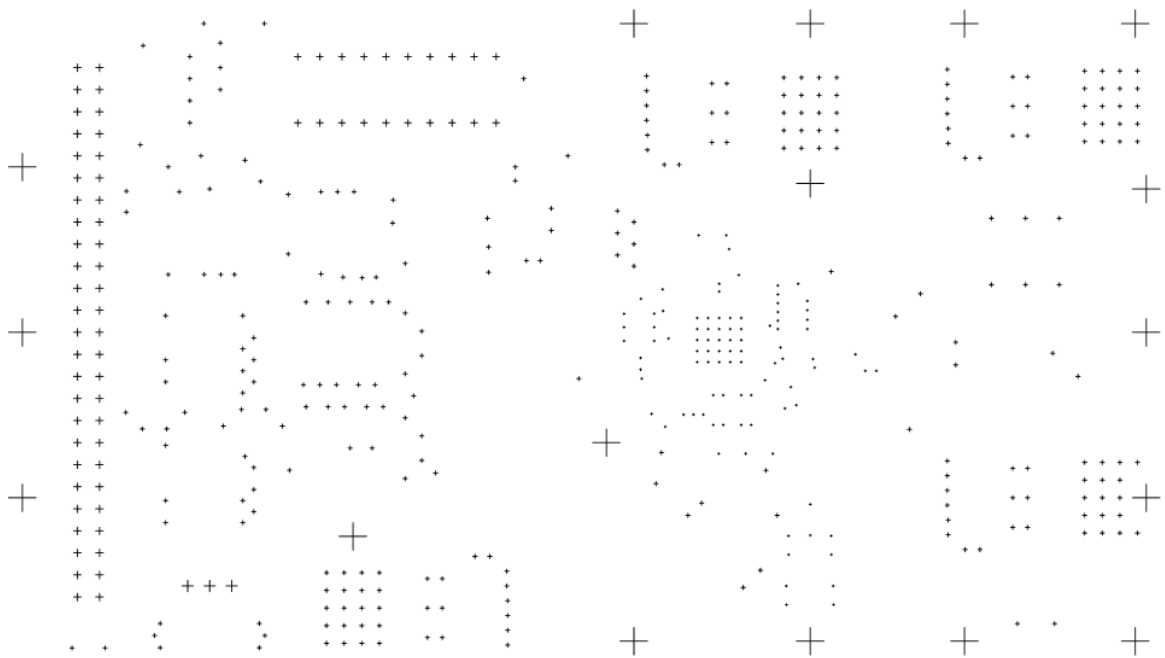


Figure B.9: Fabrication Drawings, drill drawing.

## Appendix C

### 3D PCB Renderings

This section contains 3D renderings of the top and bottom of the PCB. Altium Designer was used to create these figures. Figures C.1 and C.2 use a somewhat realistic colour scheme.

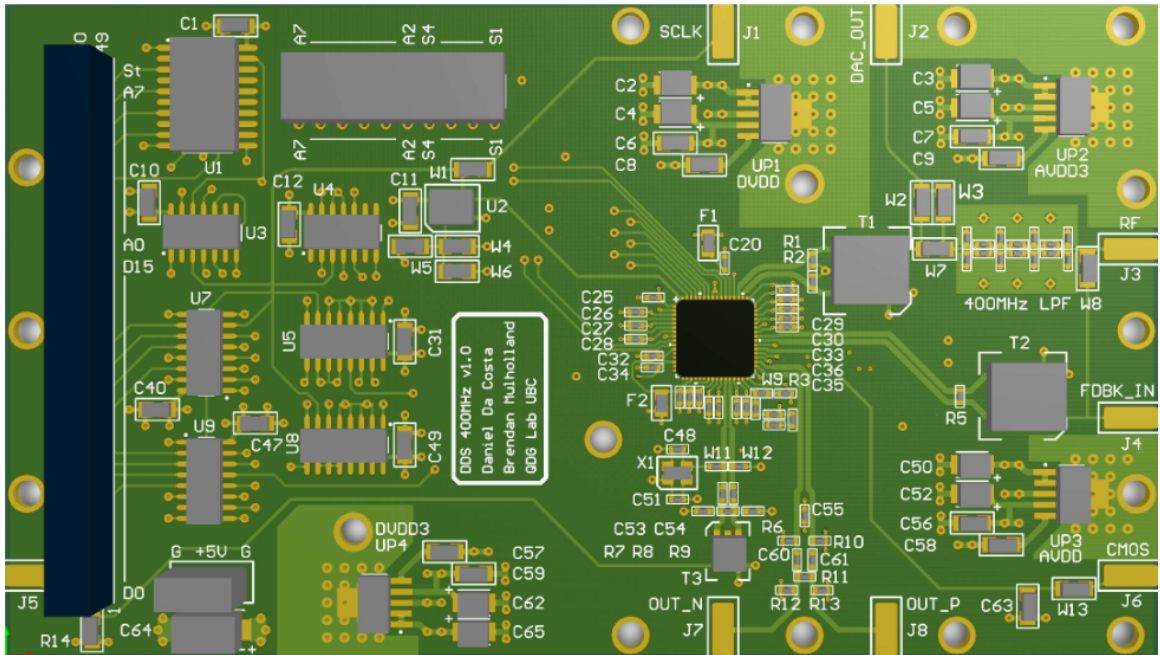


Figure C.1: 3D Rendering of the DDS, top view. Created using Altium Designer.

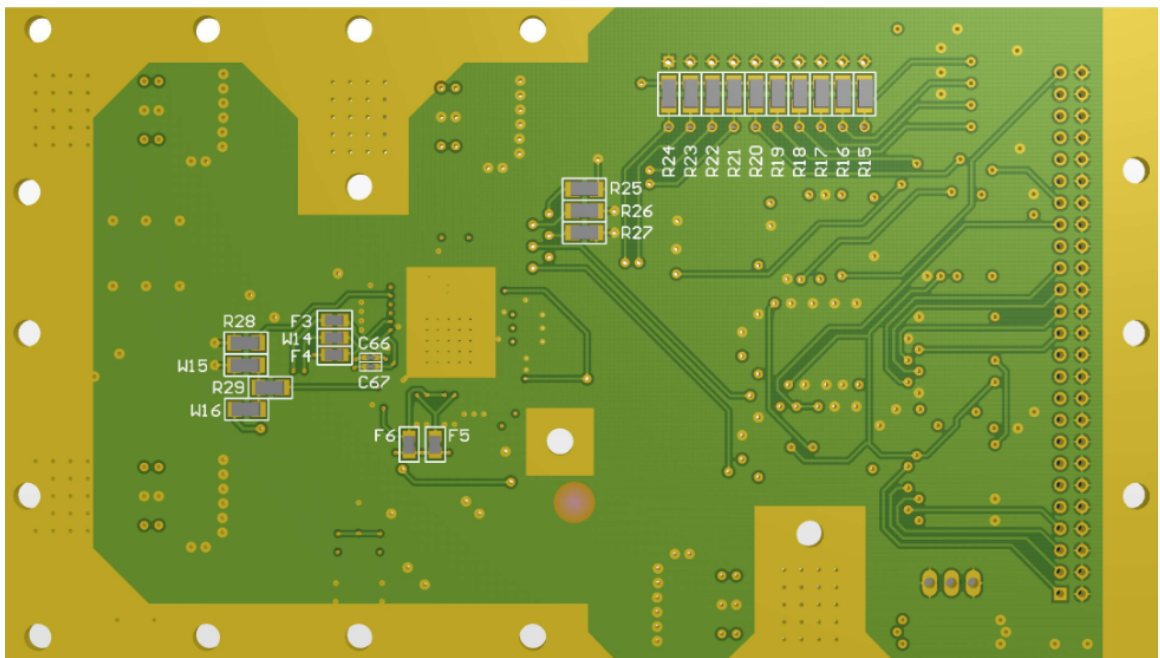


Figure C.2: 3D Rendering of the DDS, bottom view. Created using Altium Designer.



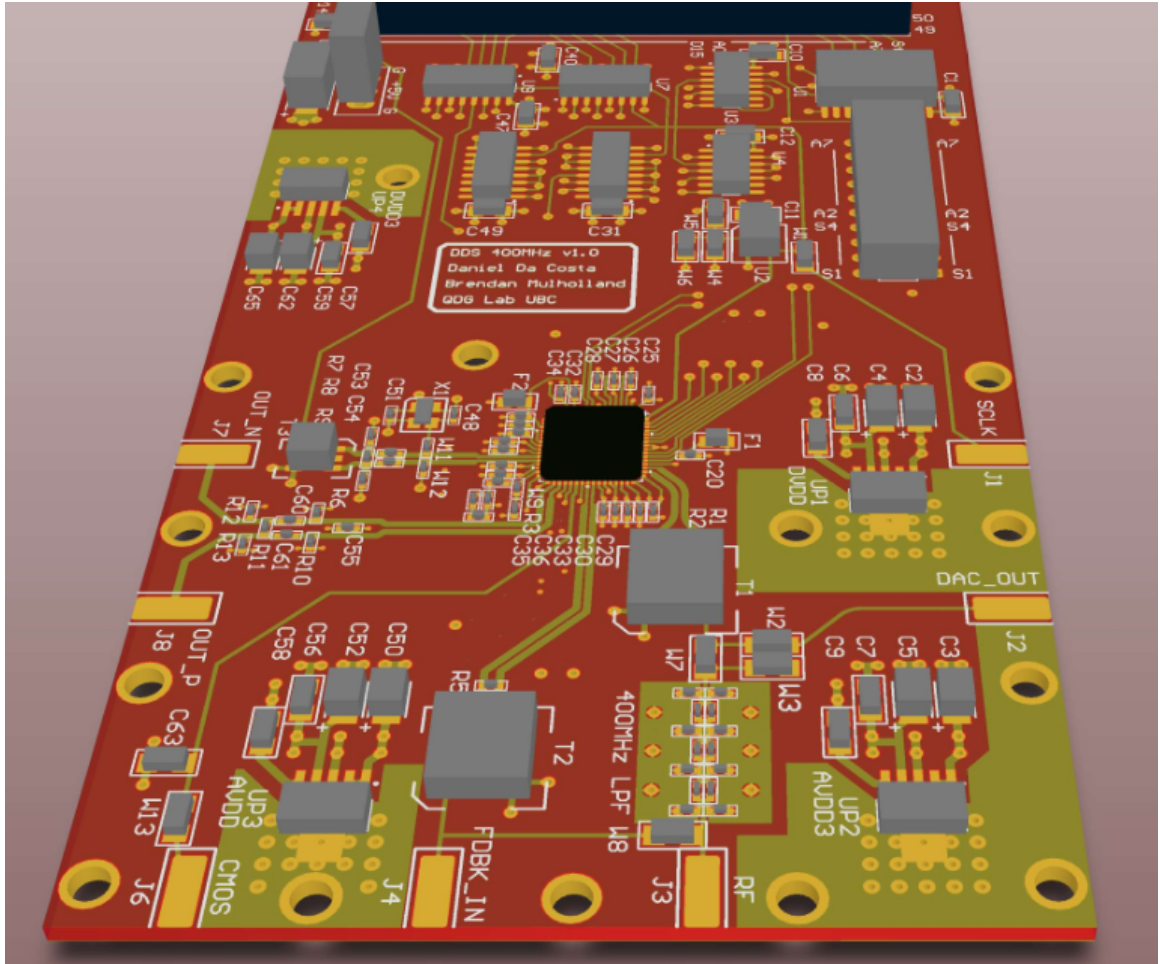


Figure C.3: 3D Rendering of the DDS, angled view. Created using Altium Designer.

## Appendix D

# PCB Parts List

Table D.1: Bill of Materials

Comment	Description	Footprint	Designator
0.1 $\mu$ F	Capacitor	1206	C1, C6, C7, C10, C11, C12, C31, C40, C47, C49, C56, C59
T491B	Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade	B	C2, C3, C4, C5, C50, C52, C62, C65
0.01 $\mu$ F	Capacitor	1206	C8, C9, C57, C58
5.6pF	Capacitor	0402	C13, C16, C22
2.7pF	Capacitor	0402	C14, C15, C21
6.8pF	Capacitor	0402	C17, C23
1.0pF	Capacitor	0402	C18
3.9pF	Capacitor	0402	C19, C24
0.1 $\mu$ F	Capacitor	0402	C20, C25, C26, C27, C28, C29, C30, C32, C33, C34, C35, C36, C37, C38, C39, C41, C42, C43, C44, C66, C67
10pF	Capacitor	0402	C45, C48, C51
180pF	Capacitor	0402	C46
0.1 $\mu$ F	Capacitor	0402	C53, C54, C55
10nF	Capacitor	0402	C60, C61
OPT	Capacitor	1206	C63
T491X	Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade	X	C64
Ferrite bead	Ferrite Bead	0805	F1, F2, F3, F4, F5, F6
SCLK_IN	BNC Elbow Connector	BCN Pads	J1

Comment	Description	Footprint	Designator
DUT OUT/FILTER IN	BNC Elbow Connector	BCN Pads	J2
DUT FIL- TER OUT	BNC Elbow Connector	BCN Pads	J3
FDBK_IN	BNC Elbow Connector	BCN Pads	J4
SYSClk_IN	BNC Elbow Connector	BCN Pads	J5
CMOS OUT	BNC Elbow Connector	BCN Pads	J6
OUTB	BNC Elbow Connector	BCN Pads	J7
OUT	BNC Elbow Connector	BCN Pads	J8
18nH	Inductor	0402	L1
22nH	Inductor	0402	L2
27nH	Inductor	0402	L3
70543-0107	Header, 3-Pin	Power Header	P1
Header 25X2	N2550-5002RB	UTBUS	P2
50Ω	Resistor	0402	R1, R2
1kΩ	Resistor	0402	R3
2.2kΩ	Resistor	0402	R4
100Ω	Resistor	0402	R5
10kΩ	Resistor	0402	R6, R10, R12, R13
25Ω	Resistor	0402	R7, R9
25Ω	Resistor	0402	R8
1kΩ	Resistor	0402	R11
25Ω	Resistor	1206	R14
10kΩ	Resistor	1206	R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28
510Ω	Resistor	1206	R29
SDA10H0KD	C&K SDA Series Low Profile DIP Switches, 10 Pos	DIPSW20	SW1
ADT2-1T- 1P+	6-Pin Transformer	CD542	T1, T2
ETC1-1-13	E-Series RF 1:1 Trans- mission Line Trans- former, 4.5-3000MHz	SM22	T3
SN74HC688DW8	8-Bit Identity Com- parator	DW020_M	U1
TXC 7C	TXC Clock Oscillator (SCLK)	4-pin SMD	U2

Comment	Description	Footprint	Designator
SN74HC74D	Dual D-Type Positive-Edge-Triggered Flip-Flop with Clear and Preset	D014_N	U3, U4
SN74HC166D	8-Bit Parallel-Load Shift Register	D016_N	U5, U7, U8, U9
AD9912	Direct Digital Synthesizer	64-pin SMD	U6
TPS78618	Texas Instruments 5-Pin Voltage Regulator	SOT223-6M	UP1, UP3
TPS78633	Texas Instruments 5-Pin Voltage Regulator	SOT223-6M	UP2, UP4
0 $\Omega$	Jumpers	1206	W1, W2, W3, W4, W5, W6, W7, W8, W13, W15, W16
0 $\Omega$	Jumpers	0402	W9, W10, W11, W12
0 $\Omega$	Jumpers	0805	W14
Fox HC49SDF	25MHz Crystal Oscillator (SYSCLK)	4-pin SMD	X1