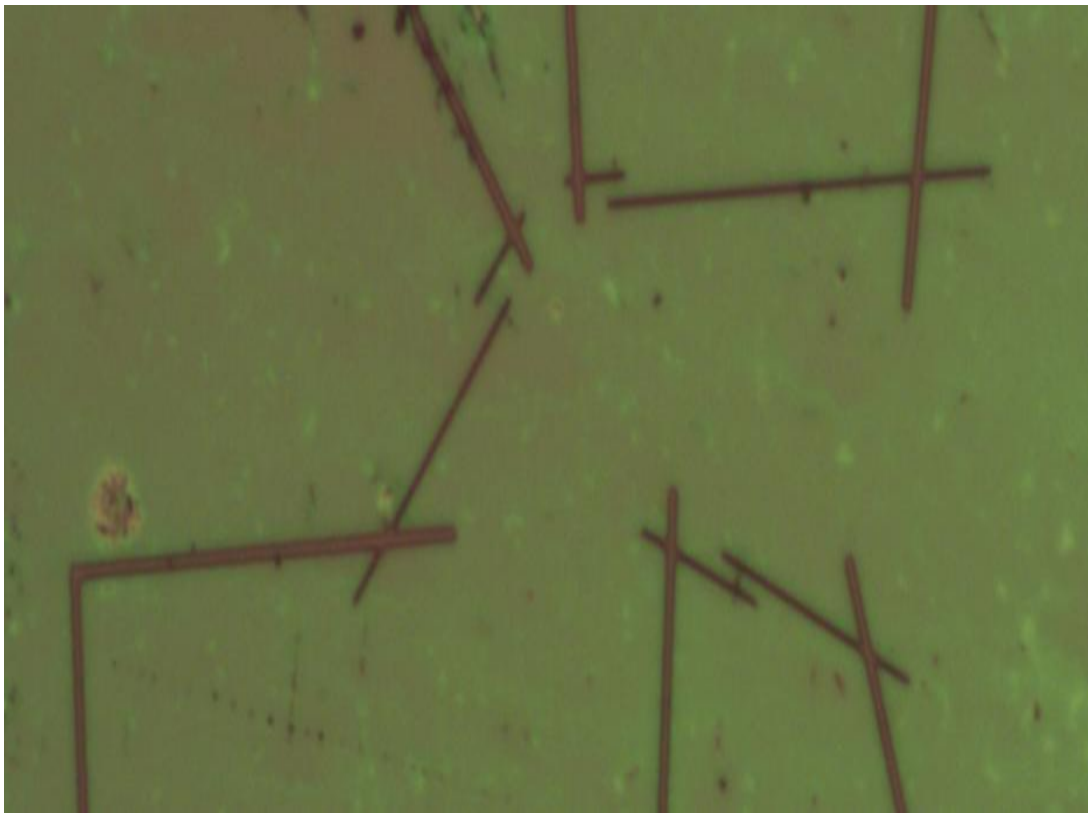
DEVISING A RECIPE TO SYNTHESIZE INDIUM ANTIMONIDE SINGLE-NANOWIRE FIELD EFFECT TRANSISTORS WITH OHMIC CONTACTS



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Project 1119
Applied Science 459
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EXECUTIVE SUMMARY

The goal of this project was to deliver functional nanowire FETs made with Indium Antimonide nanowires to our sponsor Dr. Mario Beaudoin. To create nanowire FETs, first we created a grid of Ti/Au bonding pads on an oxidized silicon wafer using photolithography. InSb nanowires, provided by our sponsor, was then deposited onto the grid, after which they were mapped using scanning electron microscope. Lengthy (~10 μm), un-clumped nanowires were chosen and then Ti/Au contact lines between nanowires and their nearest bonding pads were drawn using electron-beam lithography. The final step was performing a Voltage-current measurement on the nanowire FETs in order to examine whether the nanowires made ohmic contacts with the contact lines. The measurement results showed that our method of fabrication accurately produced functional contact lines at desired locations; however the results were regrettably inconclusive in revealing whether the contacts were ohmic.

The two possible reasons for the inconclusive results were low break-down voltage of the nanowires (~10 milli-volts) and insufficient resolution of the probe station. Due to the nanowires' high resistance (~10^6 ohm), the maximum current allowed before the break-down of the nanowires was in the order of nano-amperes, which was the limit of the current source's resolution. Therefore, resulting voltage-current curve showed an atypical behavior that does not correspond to either ohmic or non-ohmic contacts. After discussion with the project sponsor, it was decided to end the project at this point since a probe station with sufficient resolution was not available. More meaningful voltage-current curve might be observed in a low-temperature measurement as the resistance of the nanowires decreases significantly at a very low temperature, but such measurement was outside the scope of this project.

For future projects, we have a few recommendations that could improve the synthesis process. First, a new set of more-closely-spaced alignment markers should be introduced in order to accommodate smaller nanowires because much time had to be spent finding sufficiently big nanowires that can work with the current pattern. Also, by beginning the training session sooner and making it more customized and structured for this project, the time required to produce first successful nanowire FETs can be shortened.

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1. INTRODUCTION

Indium Antimonide (InSb) is a group III-V semiconductor. It is a promising candidate for high-speed low voltage transistors due to the fact that it has high bulk mobility (7 x 10^4 cm^2/V/s) and a narrow energy bandgap (0.17 eV) [17] compared to other members of group III-V semiconductor materials such as Si, GaAs, and InAs [1]. It also has high electron mobility (8 x 10^4 cm^2/V/S) and the largest electron magnetic moment (g = 51) [11].

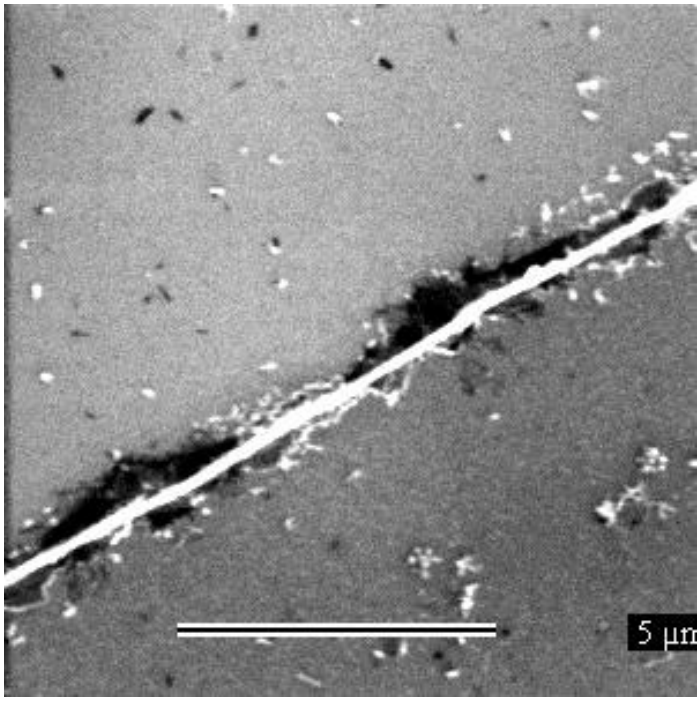


Figure 1. A Scanning Electron Microscope Image of Nanowire at x7500 (on an Oxidized Silicon Wafer)

In this project, the nanowires that are used are made from InSb. Nanowires are cylindrical solids that are on the order of nanometers in diameter and can have any length. Typically, however, nanowires are on the order of micrometers in length. Nanowires are of great interest in both research and industry. Because they exhibit semiconductor characteristics and are small, they are potentially the perfect candidates for nanoscale field effect transistors.

They are also of interest in research. Due to their small size, it is possible to construct spin-orbit nanowire transistors using nanowires. Electrons inside the nanowires are confined so that they can only move in one dimension, which is along the wire. Due to spin blockade, an electron in the nanowire can only propagate when its spin is opposite to the spin of the electron beside it due to the Pauli exclusion principle. Thus, the current flowing through the semiconductor nanowire is controlled through manipulating the spin

of the qubits inside the nanowire.

The objective of this project is to devise a recipe to synthesize nanowire field effect transistors (FETs) with ohmic contacts. Using the transistor units created from our recipe as an intermediate step, our sponsor wishes to ultimately create spin-orbit nanowire transistors. In addition, measurements made on the nanowire field effect transistors will be used to determine the electrical characteristics of the InSb nanowires that he fabricated.

Nanowire field effect transistors have been fabricated in the past. The type of spin-orbit nanowire transistors that our sponsor wishes to create has already been fabricated. However, these spin-orbit nanowire transistors used nanowires made from Indium Arsenide (InAs) [10]. In addition, those nanowires were synthesized using a very expensive method, and thus, the crystal structure of the nanowires used was very pure [10]. The rationale for our project stems from the use of nanowires made from Indium Antimonide (InSb) instead, which has better conductivity than InAs. In addition, our sponsor's InSb nanowires are synthesized using template-assisted electrochemical deposition, which is a cheaper method to create nanowires. Thus, the motivation of our project is to determine whether or not spin-orbit nanowire transistors can be made from cheaply fabricated nanowires. If this method can produce functioning results, then it is possible for our sponsor to mass-produce these transistors at a relatively low cost.

To understand the context of this project, the concepts involved in the operation of spin-orbit nanowire transistors are essential. The two major concepts that the spin-orbit nanowire transistors rely on are spin blockade and Coulomb blockade, both of which will be discussed in the "Theory" section of the report. Another set of concepts essential to understanding the scope of the report is the theory of ohmic contacts vs. rectifying (Schottky) contacts. They too will be explained in detail in the "Theory" section of the report.

In this project, the I-V curves that are generated from the nanowire field effect transistors that were synthesized using our recipe will be examined. These curves will not only determine the conductivity and electron mobility of the nanowires, but they will also determine whether or not ohmic contacts at the metal-semiconductor interfaces were successfully created. Room-temperature measurements will be performed on the transistors using a two-probe device that produces I-V curves. This will most likely be done in the AMPEL cleanroom. We have received permission from Dr. Jon Nakane to extend our project into the summer, and so, this step will be performed in the summer term after final exams.

There are also several factors in regards to the nanowires that were not considered. First, the purity of the nanowires was not considered because we were not involved in the synthesis of the nanowires and thus had no control over its fabrication. In addition, we will not be taking low-temperature measurements of the currents through the nanowires across varying source-drain voltages while inside a magnetic field. Although results from those measurements are the most valuable in determining single-electron behavior in the nanowires, due to lack of equipment and time-constraints, these measurements will be

done after our project is finished. The apparatus needed to perform low-temperature measurements are only available in Josh Folk's lab and special training is needed to operate the device. Thus, our report will not contain those results.

This report is divided into five main sections: Discussion, project deliverables, recommendations, appendices, and references.

In the discussion, the theory needed to understand the scope of the project will be discussed in detail. Then, the methods and testing protocol used to achieve our project objective and create our project deliverables will be discussed. The experimental equipment section will provide figures and descriptions of all the equipment used. In addition, a flow diagram will be provided in order to provide a "big picture" of the exact procedure that was taken in order to produce the transistors. The results, discussion of results, and the conclusion will not be in this report because we have yet to perform any measurements. The measurements will be done during the summer term after final exams, after which we will submit an addendum to this report whose content will complete this report.

In the project deliverables, a list of the project deliverables will be provided. A financial summary outlining any major costs for this project will also be provided, and finally, a detailed outline of the ongoing commitments by team members during the summer will be given.

A list of recommendations will also be included. These recommendations will help the project sponsor expedite the synthesis process.

The appendices will give the exact parameters of the processes that were required to synthesize our transistors such as photolithography, electron-beam lithography, and measuring the depth of PMMA on the silicon wafers.

2. DISCUSSION

2.1 THEORY

As mentioned in the introduction, InSb is an ideal candidate for creating spin-orbit nanowire transistors because it has the largest electron magnetic moment g among all type III-V semiconductor materials [11]. The g-factor is crucial due to the fact that the energy difference between a spin-up and a spin-down electron is proportional to g. The equation (given to us by our sponsor) for the difference in energy needed to change an electron from spin-up to spin-down is:

$$\Delta E = |g * \Delta\mu * B|$$

where g is the g factor, $\Delta\mu$ is the change in the magnetic dipole moment of the electron as it changes from spin up to spin down or vice versa, and B is the external magnetic field that is applied to the electron. Because InSb has a large g-factor, a low external magnetic field is required to switch the electrons from spin up to spin down.

There are two concepts that are essential to the operation of a spin-orbit nanowire transistor: spin blockade and Coulomb blockade. These two concepts are important in understanding the ultimate goal of what our sponsor wishes to achieve but they are not explicitly used in our project.

Spin blockade is evident when two quantum dots are beside each other and are separated by a potential barrier. Usually, the electron from one quantum dot will have a finite probability of tunneling into the second quantum dot [4]. However, since both of the electrons have the same four quantum number n, l, m, and m_l, there is zero probability of either electron tunneling from one quantum well into another due to Pauli's exclusion principle, which states that no two electrons with the identical quantum numbers can occupy the same quantum dot [4]. This phenomenon is called spin blockade because the spin of the electrons determines whether or not the electrons can tunnel. Once the spin of one electron is switched, the two electrons will have a non-zero probability of tunneling from one quantum dot to another. Spin blockade is essential in order to control when tunneling occurs [10].

Coulomb blockade is also phenomenon that prevents electrons from two adjacent quantum dots separated by a potential barrier from tunneling [10]. When there is the existence of a quantum dot, there is a capacitive energy barrier between one quantum dot and the quantum dot that the electron is to tunnel into in the case of spin-orbit nanowire transistors and thus, energy is required in order for a quantum dot to accept another electron [3]. Because this energy barrier is small, Coulomb blockade is only evident when the thermal energy of the electron is smaller than the capacitive energy [3]. Thus, this is only evident at temperatures of several Kelvin [3]. However, if there is a variable gate voltage that can vary the potential of the quantum dot such that adding one electron into the quantum dot requires no energy, then an electron can tunnel into the desired quantum dot [3]. In equation form, Coulomb blockade restricts the tunneling of an electron into a quantum dot until this equation is satisfied:

$$E(N+1, Vg) = E(N, Vg) \quad [12]$$

Where E is the energy of the quantum dot in which the electron is to tunnel into, N is the number of electrons that the quantum dot had, N+1 is the number of electrons that the quantum dot will have after tunneling, and Vg is the gate voltage which controls the potential of the quantum well. Note that the energy required to add an electron depends on the number of electrons in the quantum well and the gate voltage [12].

The next important theory is the concept of ohmic contacts vs. rectifying (Schottky) contacts. This concept is significant in our project because the results from our FETs will depend on whether our metal-semiconductor contacts are ohmic or rectifying. The effects of both ohmic contacts and rectifying contacts occur between the contact junction between the source-drain leads and the semiconductor channel. Because there is a discontinuity of materials at the contacts, there is an energy barrier between the metal and the semiconductor through which the electrons from one material must tunnel into the other (either metal to semiconductor or semiconductor to metal).

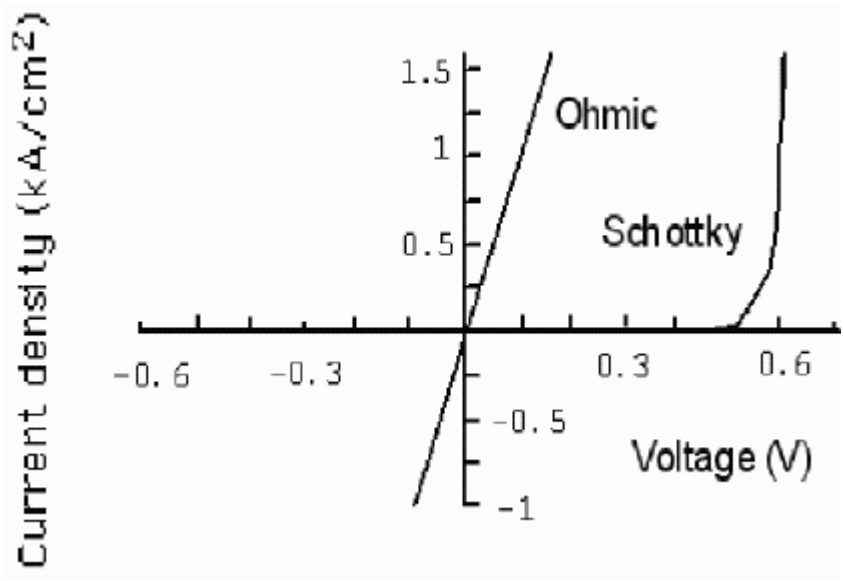
Ohmic contacts are contacts that are formed such that the energy barrier is low enough such that the barrier resistance caused by the energy barrier is negligible to the performance of the transistor [15], and it is type of contacts that is desired for the nanowire FETs. The current vs. source-drain voltage curves of transistors with ohmic contacts will be lines with constant slopes because in ohmic devices, the source-drain voltage needed to obtain certain currents dominate the voltage needed to overcome the energy barrier, thus, the current is directly proportional to the voltage [15]. Fig. 2 shows how the current flowing through the semiconductor under varies linearly with the gate voltage.

One method of forming ohmic contacts is to heavily dope the semiconductor material. The amount of electrons that tunnel from a heavily doped semiconductor will then dominate the effects of the energy barrier between the metal and semiconductor [15]. However, our sponsor did not increase the doping of the nanowires when they were fabricated, so this method cannot be used.

The second method of forming ohmic contacts is to minimize the energy barrier between the metal and the semiconductor. This is the method that was used in this project in order to create ohmic contacts. Since the energy barrier is the difference between the work function of the metal and electron affinity of the semiconductor [15] and the electron affinity of InSb is fixed, a metal with a suitable work function must be chosen.

Rectifying (Schottky) contacts are contacts that are formed such that the energy barrier is now large enough such that the voltage needed for the electron to tunnel from one material to the other at the contact junctions is not negligible compared to the source-drain voltage needed to obtain certain currents, unlike ohmic contacts. Rectifying contacts exhibit the behavior of a diode that is operated with reverse bias. A certain bias voltage is needed to in order for current to flow. Once the voltage applied is greater than the required bias voltage, the slope of the current is much greater than the current in ohmic contacts. This behavior is seen on the Schottky I-V curve in figure 2, where the

current is zero up until the source-drain voltage is equal to a certain voltage. Once the source-drain voltage exceeds a certain voltage, the current will reach its maximum at the



diode voltage.

Figure 2. Current Density vs. Source-drain Voltage of Transistors. This figure shows the current density vs. the source-drain voltage of the transistor. When the metal-semiconductor contact is ohmic, the current across the semiconducting material is linearly proportional to the source-drain voltage, thus it exhibits ohmic behavior. For the rectifying contact, however, the current-voltage characteristic is similar to that of a diode under reverse bias. The current is zero until the source-drain voltage reaches the diode voltage, where the current then reaches its maximum value in a small voltage interval [16].

2.2 METHODS

As mentioned in the introduction, the ultimate goal of the project sponsor is to create spin-orbit nanowire transistors (shown in Figure 3). However, fabricating such a complex structure was not feasible given the scope of APSC 459.

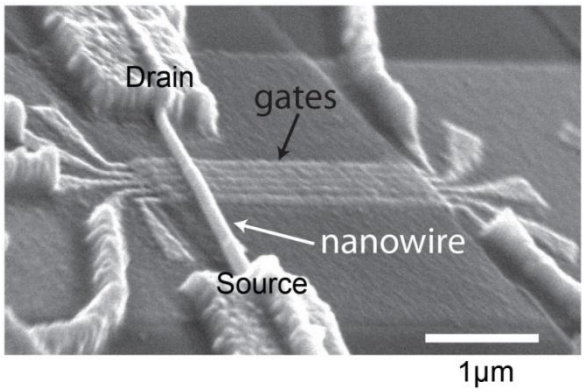


Figure 3. A Scanning Electron Microscope Image of a Spin-orbit Nanowire Transistor [18].

Therefore, instead we aimed for an intermediate structure, namely, single-nanowire field-effect-transistor (SNW-FET). A diagram of this structure is shown in Figure 4. Even though this structure is missing the quantum dot gates (the lines running perpendicular to the nanowire in Figure 3) required for spin-orbit nanowire transistors, it was still a suitable end-point because the quality of electrical contacts we fabricated as well as electron mobility of nanowires could be measured. SNW-FET is also a standard structure that was successfully implemented by many research groups such as Duan et el. and Liu et el [6][9]. Considering the limited time available, lack of expertise in the field of nanofabrication, and most of all, its proven success record, we decided to not pursue an alternative design.

Figure 4. A Diagram of Single-nanowire Transistor (S is source; D is drain; and G is gate) [13].

At AMPEL, voltage-current measurement, required for testing spin-orbit nanowire transistors and electron transport measurement, could only be performed if nanowires were connected to a customized Integrated Circuit(IC) socket, shown in Figure 5.

Figure 5. Integrated Circuit Socket Compatible with the Wire-bonding Machine at AMPEL

Nonetheless, equipment at AMPEL was not capable of directly connecting nanowires to the pins due to their small size. Alternatively, a wafer (3'' p-doped silicon wafer with an oxidized surface; see Figure 6) with a grid of titanium/gold bonding pads (dimensions: 100 μm by 100 μm by 110nm) was utilized. These pads were sufficiently small for direct connections to nanowires and simultaneously large enough to be wire-bonded: a thin gold wire is welded onto the bonding pads and IC socket pins, connecting them together. Therefore, the objective of this project was to create single-nanowire field-effect-transistors (SNW-FETs) on such a wafer and then connect their drains and sources to neighboring bonding pads. This section describes the various nanofabrication processes that were employed to fabricate this structure.

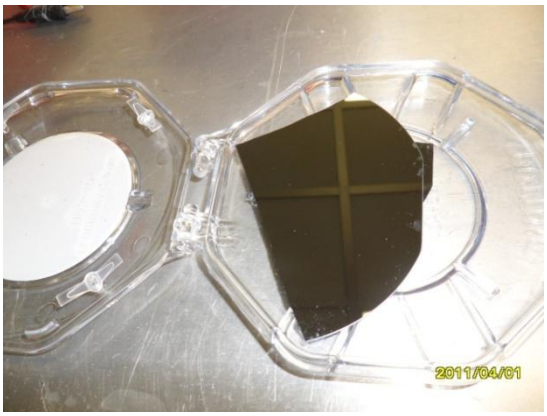


Figure 6. Pieces of Silicon Wafer Used for This Project (the ceiling is reflected on the wafer).

2.2.1 Fabricating Bonding Pads

In order to fabricate bonding pads, two processes were required: photolithography and electron beam physical vapor deposition (EBPVD). Through photolithography, a removable mask on top of the wafer was produced with a hollow grid pattern (i.e. the mask had holes where we wanted bonding pads to appear). Then, using EBPVD, a thin film of titanium and gold atoms was deposited on the mask wafer. Upon removal of the

mask, those deposited on the mask were also removed along with it, and those deposited directly on the wafer (through the holes in the mask) formed bonding pads.

2.2.1.1 Photolithography

Photolithography is a fabrication process that covers a wafer with a removable layer made of a chemical called photoresist and then "carves out" a desired pattern from the layer. Photoresist (specifically, positive photoresist) is a chemical that becomes soluble to developing solution once exposed to UV light [7].

Photoresist (AZ4410) was applied on the wafer using a programmable spinner (Headway PWM32) to obtain a uniform coating. First, drops photoresist were applied until ¾ of the wafer was covered. Then, it was spun at high revolution-per-minute, which spread the photoresist evenly by centrifugal force. The thickness of the resulting photoresist layer depended on the following parameters of Spinner: acceleration, acceleration duration, spin-revolution-per-meter, and spinning duration. For exact values of these parameters and those for later processes, please refer to Appendices. Using the parameters listed in Appendix A resulted in a thickness of 12 μm. After spinning, a soft-bake is performed by putting the wafer on a hot plate to 1) eliminate any moisture in the resist, 2) improve its adhesion to the wafer, and 3) anneal the shear stress resulting from spinning [7]. Any process involving chemicals was done on a wet bench.

After the soft-bake, Ultra-violet light exposure was carried out using Karl Suss Aligner (name of the UV exposure machine). This step transferred a desired pattern from a physical mask to the photoresist layer. The physical mask was provided by the project sponsor, and contained rectangular holes for bonding pads and smaller circular holes for alignment markers. The role of alignment markers is elaborated upon in the Alignment section. The physical mask was placed on top of the wafer to selectively expose parts where the pattern was to be transferred. The exposure strength was increased to 30 light integral from the suggested value of 12 light integral in Standard Operating Procedure because alignments markers and edges were not defined clearly when the latter was used. Afterwards, the wafer was placed in a developing solution (AZ400k) that dissolved exposed parts, leaving the mask pattern on the photoresist. Before moving onto Electron Beam Physical Vapor Deposition, the wafer was inspected under an optical microscope to see if all the features came out clearly. If they did not, the photoresist layer was removed with acetone, and the procedure was repeated.

2.2.1.2 Electron Beam Physical Vapor Deposition (EBPVD)

EBPVD (here forth referred to as Evaporation) is a technique to deposit a film of desired metal on a wafer and is performed using a machine called Evaporator. Typically, Evaporator consists of a high-vacuum chamber and tungsten filaments which produces electron beams via thermionic emission. Electrons are accelerated towards a crucible containing a desired metal, and their kinetic energy is converted into heat upon collision. Metal atoms on the surface of the metal turn into a gaseous state and condense on all surfaces inside the chamber, coating them with a thin film of the metal. The advantage of

this system is that, using high energy electron beams, metals with high boiling points such as gold (2807 ℃) can be easily evaporated [18].

Evaporator at AMPEL could evaporate up to five metals in a single process and was equipped with a thickness monitor which controlled the thickness of deposited metal films. A film of titanium (10nm), for which gold has good adhesion, was deposited first before gold (100nm) because unlike titanium gold does not stick on silicon dioxide well. Chromium was also considered for this purpose because it has good adhesion as well, but at the time of this project, chromium was not properly stored and as a result oxidized, which rendered it useless.

After Evaporation, the entire wafer was covered with the titanium/gold film. To produce the grid pattern, the remaining photoresist needed to be removed using acetone. This removal process is called lift-off. During lift-off, the parts of the Ti/Au film deposited on top of photoresist were washed away along with the photoresist, and only parts that were deposited directly on the wafer remained. For a successful lift-off, it was important to ensure that the photoresist layer (12 μm) is thicker than the metal film (110 nm) so that the parts of the film deposited on the wafer were not attached to those on the photoresist. After the lift-off, the fabrication of bonding pads was completed. After examining for any visual defects under an optical microscope, the wafer was then cleaved into smaller pieces (50mm by 50mm) to be able to fit into the IC socket.

2.2.2 Nanowire Deposition

Nanowires, provided by the project sponsor, were stored in a bottled solution of de-ionized water. They were deposited by applying a few droplets of the solution on the wafer and evaporate boiling away the solvent with a hot plate. Unfortunately, the exact concentration of nanowires in each bottle was unknown and also varied for each bottle. Therefore, the concentration of nanowires in the bottle had to be found out first by checking the resulting density of nanowires for a single droplet using Scanning Electron Microscope. When the concentration was found to be too high, the solution was diluted with more DI water, and for the opposite case, more droplets were applied. The ideal concentration was found to be five to ten nanowires within a square area formed by four alignment markers (see Figure 7). Once the solvent was dried, nanowires glued very strongly to the wafer, and all the subsequent processes described in this section did not change their position. Due to the nature of this method, nanowires were dispersed randomly on the wafer, and needed to be mapped using Scanning Electron Microscope. In addition, it was found that placing the bottle in an ultra-sonic bath for 20 minutes before deposition help reduce the number of clumped nanowires.

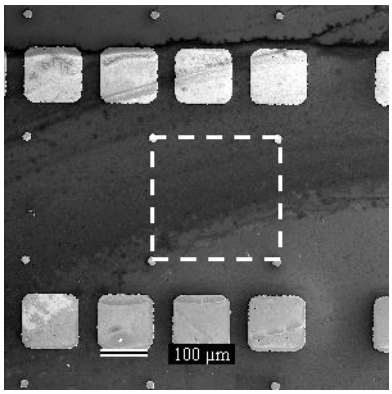


Figure 7: An Image of the Wafer after Photolithography to Illustrate the Square Formed by Four Alignment Markers (inside the dashed square).

2.2.3. Mapping Nanowires

The dimensions of nanowires were quite close to the resolution limit of a low-powered optical microscope available at AMPEL (1000x). If the exact locations of nanowires were known beforehand, it was still possible to find them under an optical microscope; nevertheless, mapping nanowires was not because they could not be differentiated from other impurities when viewed under the optical microscope. Therefore, Scanning Electron Microscope, which offered much higher resolving power (300,000x) was used to map nanowires for this project.

2.2.3.1 Scanning Electron Microscope

Scanning Electron Microscope (SEM) uses a beam of electrons in order to image. Because electrons have much shorter wavelength (about 100,000 times) than visible light, SEM can achieve much greater resolution than an optical microscope. Electrons interact with atoms at the surface of the sample and produce signals such as secondary electrons, back-scattered electrons, electromagnetic waves, and by analyzing these signals, SEM can image the sample's surface topography [8].

When searching for nanowires, magnification from 500x to 1000x was selected. The reason was that at this magnification scanning the wafer in a timely manner was possible, and at the same time nanowires could be still be distinguished. Nanowires appeared as a short string of white specks as shown in Figure 8. They had a characteristic shape at higher magnification; therefore, it was possible to distinguish them from other impurities such as dusts. In addition, care was taken not use any wires that were clumped together to build single-nanowire field-effect-transistors as voltage-current measurements were accurate only for a single nanowire.

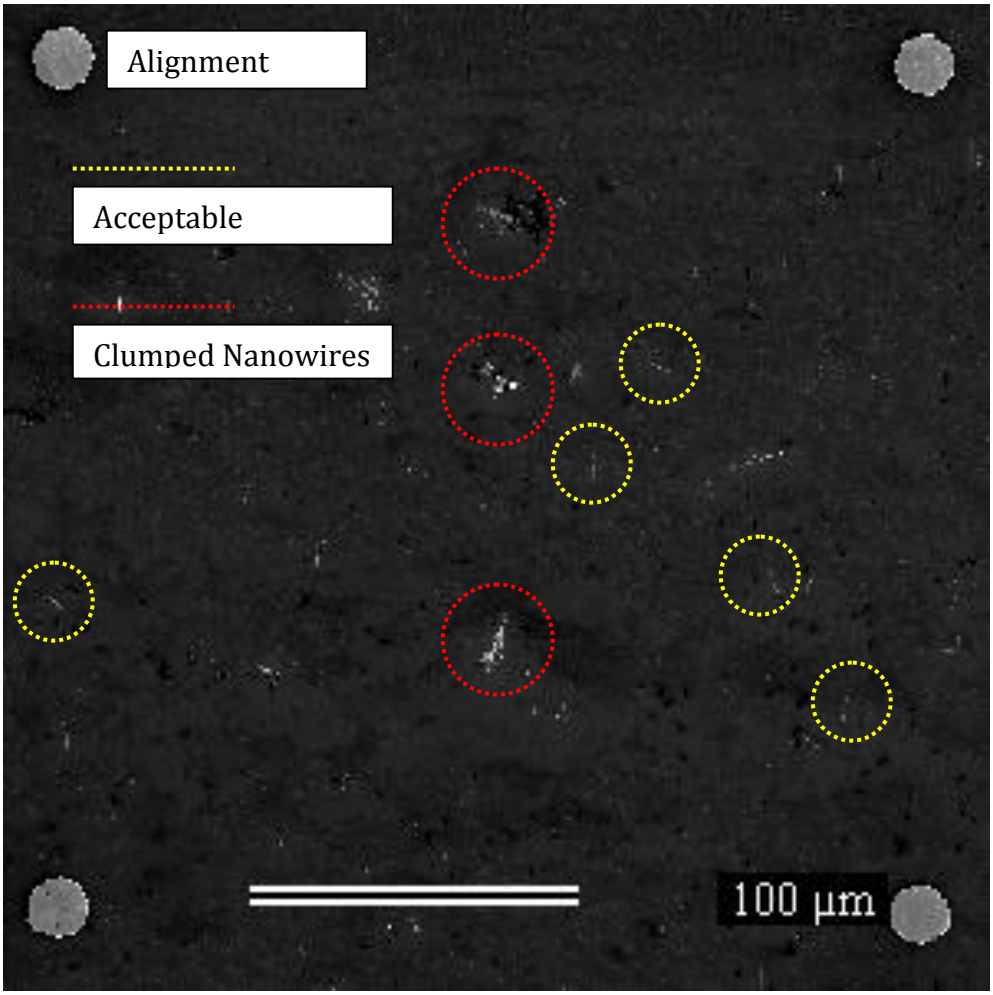


Figure 8. A Scanning Electron Microscope Image of the Wafer after Nanowire Deposition; Magnification x270; Yellow dotted Circles Show Nanowires of Acceptable Length; Red Dotted Circles Show Clumped Nanowires Which Should Be Not Used.

Before loading the wafer into the scanning electron microscope, it was important to note the orientation of the wafer relative to the sample-holder and also to use the same orientation for subsequent steps. The orientation could be determined by different features including the overall shape and visible defects. A small scratch near one corner was used for this project. After loading, we looked for an area with the appropriate area-density of nanowires. Another characteristic to look for was the length of the nanowires since the longer the nanowires were, the less likely it was to fail in subsequent steps. A picture at 270x was taken (Figure 8). This magnification is the highest magnification at which all four alignment markers could be captured, all of which are necessary for alignment. The picture was then opened using the software Microsoft Paint. The pixels of both ends of nanowires and the center of alignment markers were recorded. These values were required for next step. Once all the pixels were recorded, the wafer was prepared for electron beam lithography.

2.2.4. Connecting Nanowires

2.2.4.1 Electron Beam Lithography

Electron beam lithography works in a similar way as photolithography except for two differences: 1) instead of using light and photoresist, electron beam lithography uses electron beams and PMMA (a chemical that becomes soluble when exposed to electron beams); and 2) no physical mask is utilized. Electron beam lithography can fabricate features of size much smaller than photolithography (about 100 times) due to small wavelengths of electron beams, but fabrication speed is much slower. Because PMMA is sensitive to electron beams, a scanning electron microscope (emits electrons) cannot be used to look closely at a wafer after spinning PMMA (PMMA A4 is the exact brand used) on it. The dose (exposure strength) increases with time and magnification; therefore, it is imperative that electron beam lithography is done as quickly as possible in order to avoid unwanted exposure or over-exposure (results in insolubility)[2]

Similar to photolithography, first a resist layer was applied using Spinner. Nonetheless, the spin parameters were not readily available and had to be found out by testing. Using the data sheet of PMMA A4, an approximate spin revolution-per-minute that would yield a thickness of 200nm was found. Because the thickness was much less than the photoresist layer (12 μm), it was necessary to confirm the exact thickness. Otherwise, parts of the resist layer deposited directly on the wafer could have been attached to those on the resist layer and been washed off during lift-off, Using the data sheet, we could approximate revolution-per-minute that produced approximately 200nm thick resist layer. The exact thickness measured using Filmmetrix F20 was 188.31nm, and this thickness worked fine during lift-off.

Next step was electron beam writing, which is analogous to UV exposure. The purpose was again to expose parts that needed to be removed (for Evaporation). However, since unlike in photolithography a physical mask was not used, the parts to be exposed had to be specified using a CAD program, which directed the electron beam.

2.2.4.2 Transformation Matrix

Prior to drawing in the CAD program, first a transformation matrix that converted pixels in Microsoft Paint into coordinates in the CAD had to be computed. The transformation matrix could be found using the following formula (given by the project sponsor):

$$\vec{C} = \begin{bmatrix} Cx \\ Cy \\ 1 \end{bmatrix} = [T] \times \vec{P} = \begin{bmatrix} Px_{align,1} & Px_{align,2} & Px_{align,3} \\ Py_{align,1} & Py_{align,2} & Py_{align,3} \\ 1 & 1 & 1 \end{bmatrix} \times \begin{bmatrix} Px \\ Py \\ 1 \end{bmatrix}$$

where $\vec{C}$ is a point (in coordinates) in the CAD;

$[T]$ is the transformation matrix;

$\vec{P}$ is a point (in pixels) in Microsoft Paint.

The alignment markers were separated by 280 µm from each other. Since their relative positions were known in both the CAD and in Microsoft Paint, they could be used to derive the transformation matrix. Using this matrix, nanowires could be drawn on the CAD file by converting their end points in pixels to coordinates.

When drawing in the CAD program, bonding pads and alignment markers were drawn first. Their dimensions and relative distances were already known because these were determined by the photolithography mask. Then the nanowires were drawn using their transformed end points. These structures worked as a guide when deciding where to draw contact lines. Next, contact lines with a width of 1 µm were drawn from each end of nanowires to the edges of the window at 270x. Then the window size was zoomed out to 100x and these 1µm-wide contact lines were connected to the nearest pads with 2µm-wide contact lines while ensuring that the two ends of each nanowire were connected to two different pads. It was possible to do this process in one step at 100x to save time, but it would have been at the expense of accuracy in the positions of contact lines; therefore, the two-step method was chosen. A finished CAD drawing is shown in Figure 9.

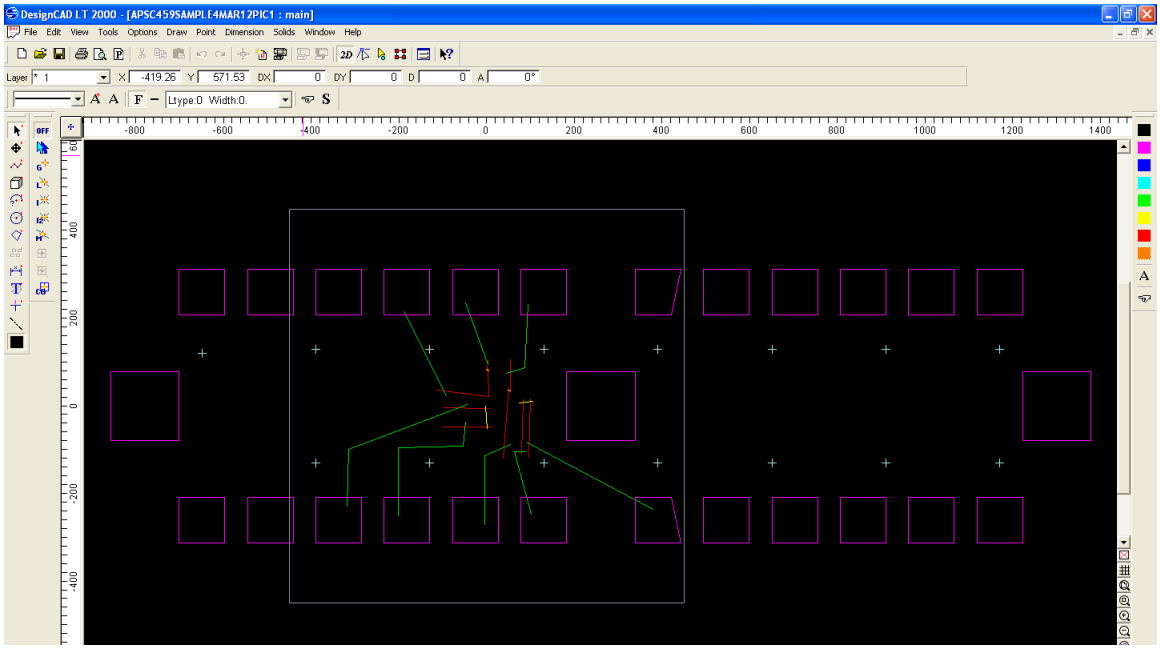


Figure 9: An Example of a Finished CAD file. Purple Squares Indicate Gold Pads; Crosses Indicate Alignment Markers; Yellow Lines Indicate Nanowires; Red Lines Indicate 1 µm-wide Contact Lines; Green Lines Indicate 2 µm-wide Contact Lines.

2.2.4.3 Alignment

After completing the CAD drawing, an aligning program was created. Because the wafer was never in the exactly same orientation (eye-balling is not sufficient during nano-fabrication), the electron beam lithography machine needed to know what the

orientation of the currently loaded wafer was in order to make the right adjustments. The alignment program essentially created a transformation matrix that converted the coordinates in the CAD program to new coordinates that compensated for the difference in orientation. Following executing the alignment program, e-beam writing was carried out using the CAD file.

2.2.4.4 Finishing steps (Development, Evaporation, and Lift-off)

At this point, the parts of PMMA where electrical lines would be located were exposed to the electron beam and became soluble to the developing solution. The same steps as photolithography were followed. Upon development to remove exposed parts of the PMMA layer, a film of titanium (10nm) and gold (100nm) was evaporated onto the wafer. Their thickness was set below the thickness of the PMMA layer (200nm) to ensure that the electrical contact lines were not washed away during lift-off. After the lift-off, the fabrication of single-nanowire field-effect-transistors (SNW-FETs) was finished at last. The SNW-FETs were checked under the optical microscope for any defects, and those that appeared functional were recorded for voltage-current measurements.

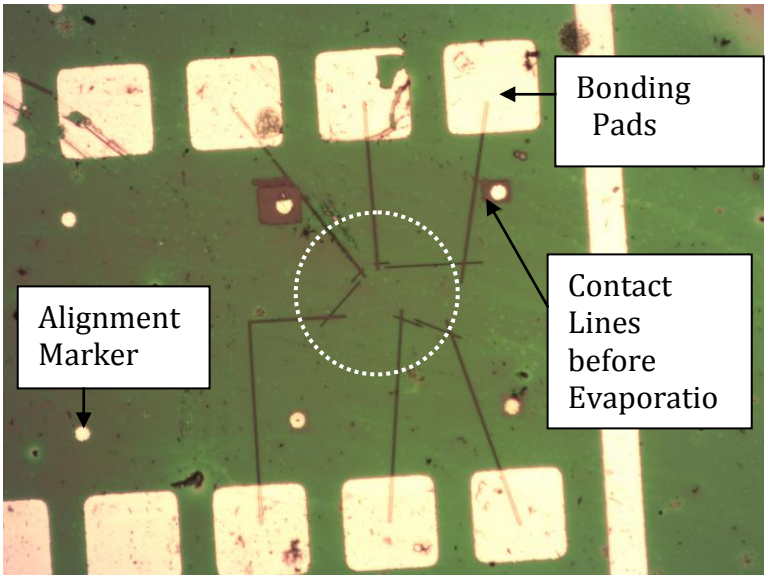


Figure 10: An Optical Microscope Image of the Wafer after Development. Nanowires Are Located at the Small Gaps (Circled).

2.2.5. Voltage-Current Measurement

Before performing voltage-current measurement, the SNW-FETs that showed no defects were annealed at 350 degrees Celsius for 7 minutes in order to improve the crystalline quality of the nanowires and the adhesion of titanium to the silicon dioxide layer. The wafer was then placed on a probe station at Dr. Lukas Chrostowski's laboratory, which was equipped with a current source and a voltmeter. It should be noted that the current source's finest increment was a nano-ampere since the resolution was a limiting factor as discussed later. In addition, each probe was thin enough to be

contacting only the desired bonding pad. Although previously not mentioned to avoid any confusion, several control gold contact lines were drawn directly connecting pairs of bonding pads. Voltage-current measurement was first performed on these contact lines to prove that the fabricated contact lines acted only like small resistors as expected. A diagram describing the measurement procedure is shown in Figure 11. After the measurement, the same procedure was followed for the chosen SNW-FETs.

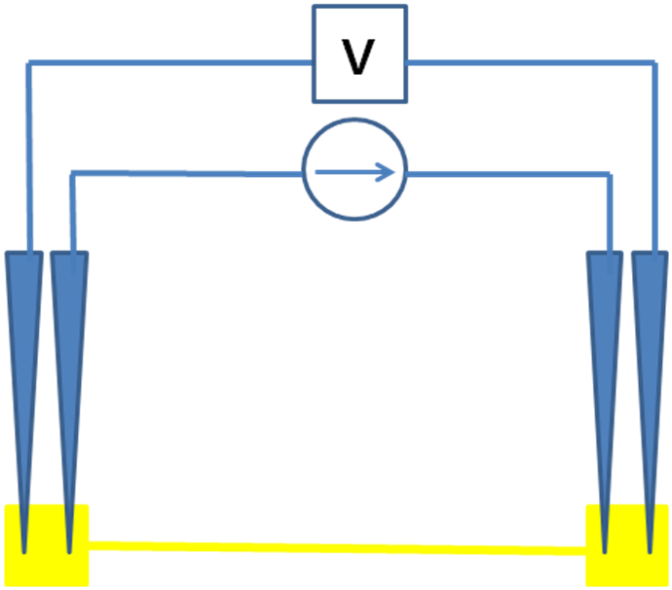


Figure 11: Voltage-Current Measurement Procedure

2.3. EXPERIMENTAL EQUIPMENT

Figure 12. Headway PWM32 (Spinner) Used to Apply a Uniform Layer of Photoresist (right: the sample is held in place in the middle by a vacuum pump; left: the programmable controller for Spinner).

Figure 13. Karl Suss Aligner (used for UV exposure)

Figure 14. Evaporator at AMPEL (right: vacuum chamber; left: control panel)

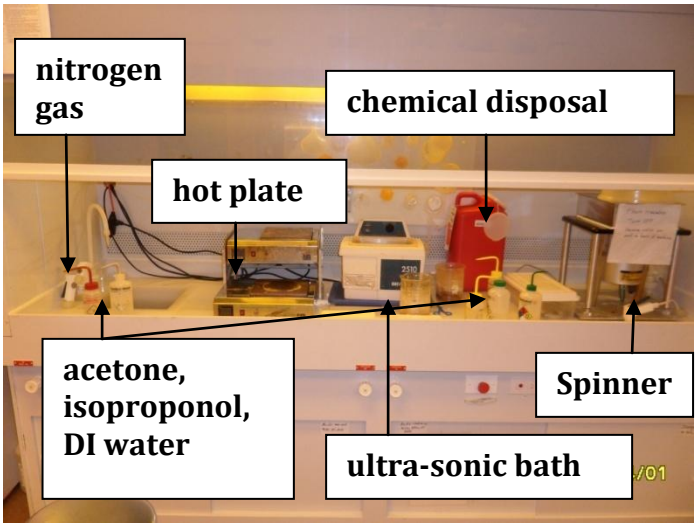


Figure 15. Wet Bench at AMPEL

Figure 16. Scanning Electron Microscope at AMPEL (equipped with electron beam lithography functionality). Left: Control Panel; Right: Microscope

Figure 17. Sample Holder for Scanning Electron Microscope at AMPEL

Figure 18. Filmmetrix F20 (measures PMMA thickness)

Figure 19. Optical Microscope at AMPEL (max magnification 1000x)

Figure 20. Wire-bonding Machine

Figure 21. Rapid Thermal Annealing Machine

2.4FLOW DIAGRAM

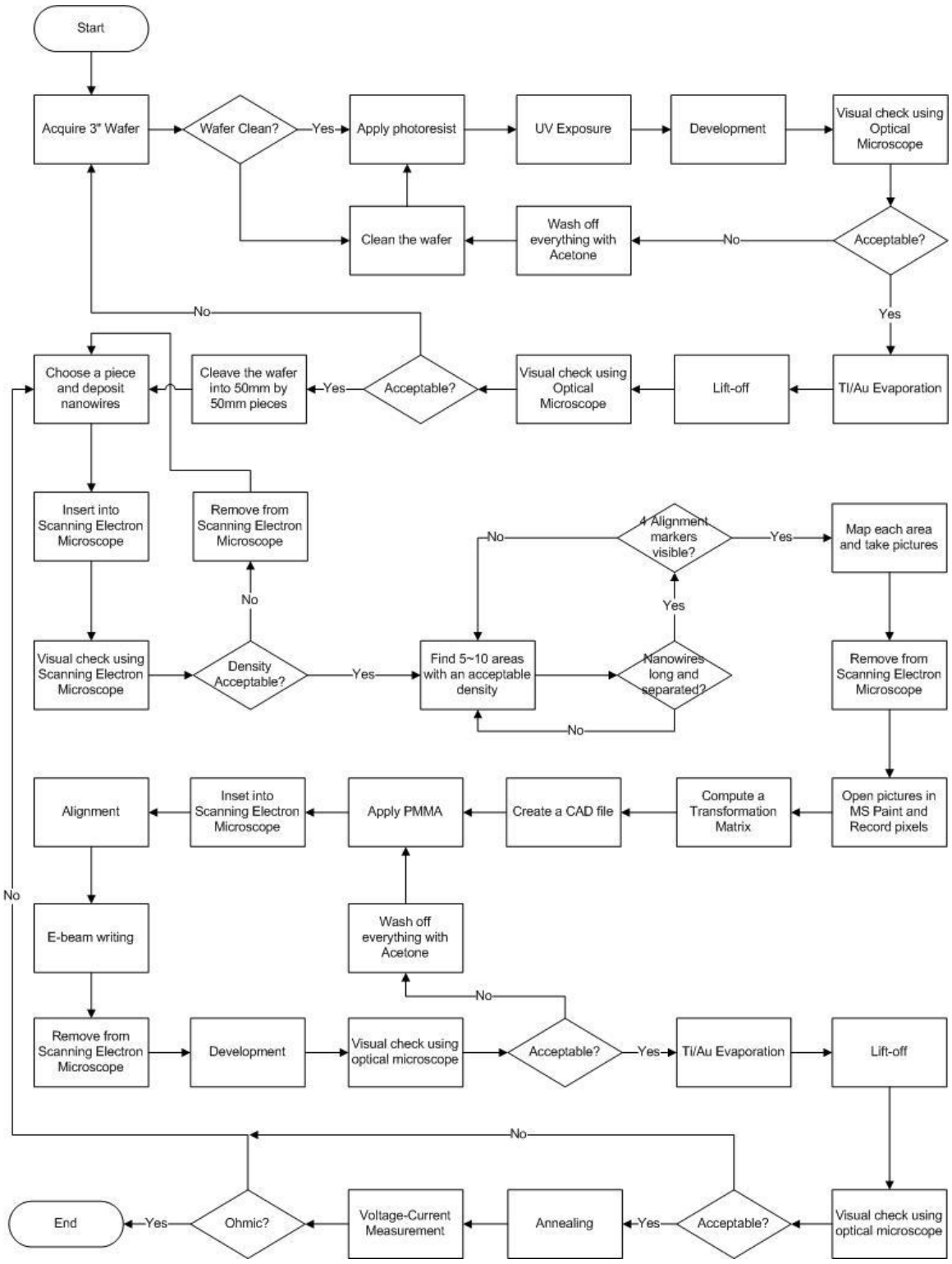


Figure 22. Flow Diagram for Single-Nanowire Field-Effect-Transistor Fabrication

2.5 Discussion of Results

2.5.1 Gold contact line

To verify that the steps described in the "Methods" sections were successful in synthesizing functional electrical contact lines, a control gold contact line was created between two contact pads. As gold is a pure conductor, the voltage-current curve was expected to be linear, with the slope of the curve equal to the resistance of the gold contact line.

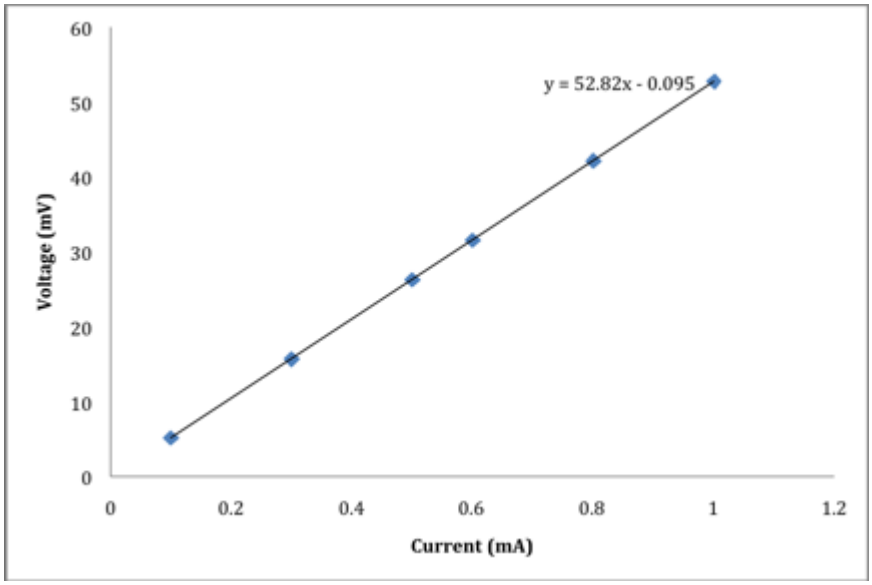


Figure 23. Voltage over a Control Gold Contact Line under Varying Current

Figure 23 shows that the curve is indeed linear and that the resistance of the gold was approximately 52.82 ohms. From the calculations in Appendix D, the calculated value of resistance of the gold contact line was 35.38 ohms. Although the measured resistance is greater than the calculated resistance, the two values were still within order of magnitude of each other. The calculated value was lower most likely because it was assumed that the cross-sectional area along the gold line was uniform and that the purity of the gold was 100%.

However, since the behavior of the measured resistance of the gold contact line was ohmic and the resistance was still within magnitude of the calculated resistance, it is safe to conclude that the electrical contacts that were drawn following the "Methods" section were indeed functional.

2.5.2 Nanowire field-effect transistor (FET)

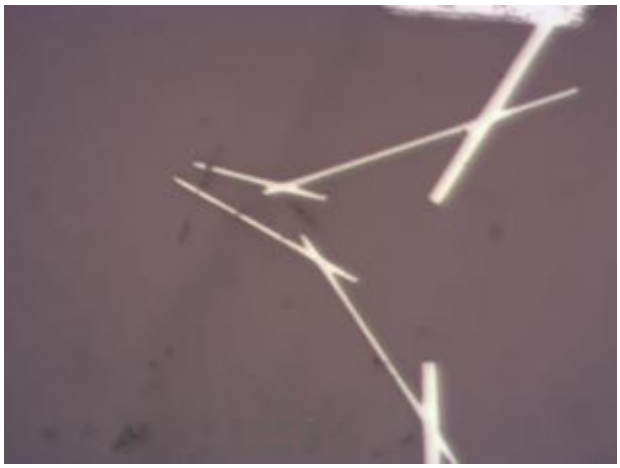


Figure 24 Nanowire and Contact Lines

From figure 24 it is evident that two gold contact lines both touch the same nanowire but do not overlap, successfully creating a SNW- FET. Next, the current under varying voltages between two contact pads that were attached to two ends of a nanowire (i.e. the current through a SNW-FET) was measured. The curve in figure 25 that was obtained from the measurement did not exhibit field-effect transistor behavior.

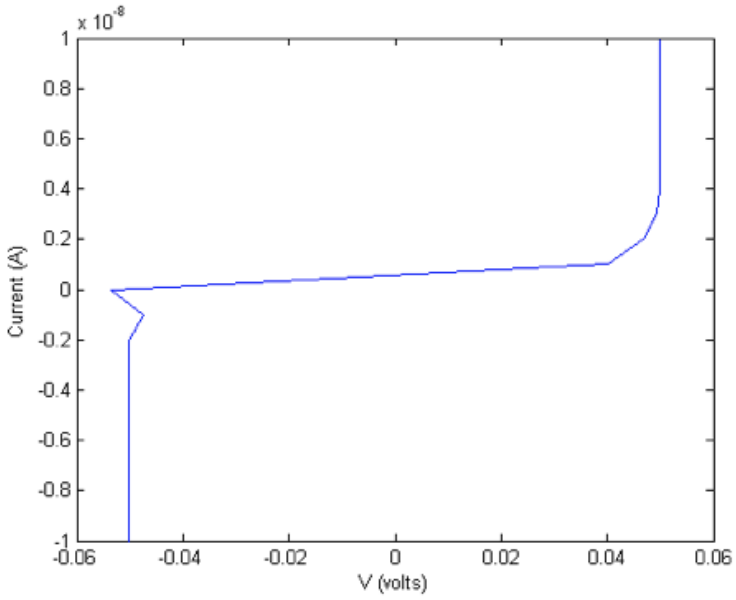


Figure 25 Voltage-Current curve for a SNW-FET

According to Liu *et al.* (2008), the current vs. voltage curve for a SNW-FET should be linear at a given temperature, which is shown in figure 26.

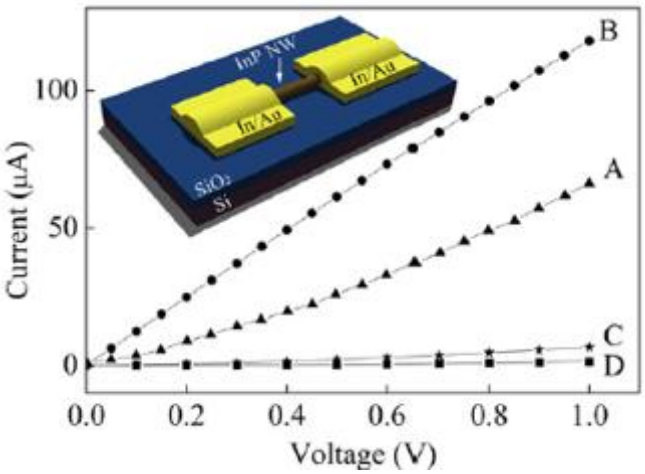


Figure 26. A curve of current vs. voltage for InP nanowire field-effect transistor from Liu et al. (2008). These four curves are the I-V characteristics of four different types of InP nanowires at room temperature

The shape of the measured I-V characteristic does not match the shape of the correct I-V characteristic shown above. With help from our sponsor, the main source of this discrepancy was identified to be low break-down voltage of InSb nanowires.

A limitation of performing room temperature probe measurements was that the allowable range of source-drain voltage was very low because the breakdown field of InSb is approximately 1000 V/cm. The longest nanowires were only 10 μm, which meant that the upper limit of the magnitude of source-drain voltage that could be applied across the nanowire was only 10 mV. If the voltage applied exceeded 10 mV, the nanowire would break down.

The calculated resistances of the nanowires were in the order of megaohms (10^6 Ω), as shown in Appendix E. Because of the high resistance of the nanowire at room temperature, the current flowing through the nanowire would be on the order of nanoamperes when the applied voltage was few milli-volts. Unfortunately, the current source connected to the probe was incapable of generating such low current with great accuracy; thus, it was unlikely that the correct changes in current under varying voltages were observed. At this point, there were not any alternative experiments that would give further insight into the process because a probe station with a finer resolution was not available. Perhaps low-temperature measurements will yield more useful results because at low temperatures (several degrees K), the resistance of the nanowire decreases, and changes in current due to variations in voltage are more evident under those temperatures. Nevertheless, such an experiment was outside the scope of this project.

3. CONCLUSION

From the voltage vs. current curve of the gold contact line in figure 23, the first conclusion that could be drawn was that functioning gold contact lines were synthesized. The thickness of the titanium and gold that were evaporated onto the sample was sufficient to create a conducting contact line while the temperature and duration of time under which the sample underwent rapid thermal annealing was successful in creating strong adhesion between the titanium and the silicon dioxide layer underneath. The linear relationship between voltage and current confirmed that the lines were conducting as expected.

The second conclusion drawn from our measurements was that it was still unconfirmed whether ohmic contacts were successfully synthesized between the gold contact line and the nanowire. The current vs. source-drain voltage measurement did not confirm or disprove whether or not ohmic contacts were formed because the measured I-V curve did not exhibit typical I-V characteristics. This was due to the fact that it was impossible to generate a sufficiently small current at which the nanowire would not undergo break-down with the current source at the probe station.

From the image from the optical microscope, we could at least conclude that our method of mapping nanowires and writing with e-beam lithography was successful in tracing a path from the contact pads to the nanowires because it is evident in figure 24 that the gold contact lines overlap the nanowire at the two ends without shorting. This overlap was true for all the nanowires that were fabricated.

4. PROJECT DELIVERABLES

4.1 LIST OF DELIVERABLES

In the proposal, the project had only one deliverable, which was a single-nanowire field-effect transistor that is electrically connected to a special IC socket.

It turned out, however, that what the sponsor truly wants is the recipe with the exact parameters for creating functioning spin-orbit nanowire field-effect transistors with ohmic contacts so that he can create the FETs. Thus, our final deliverables will consist of:

1. The exact recipe for creating the transistors along with any parameters for each of the machines that we used.
2. The CAD design file that serves as the template for e-beam writing on the silicon wafer. This CAD file is special in that the relative locations of the square pads and the align marks are exactly the same as the pattern on the mask used to create the silicon wafer pad.
3. The CAD design file that serves as the alignment program for 270x magnification and 100x magnification. The alignment program is responsible for generating a transformation matrix so that the alignment marks on the CAD file for the template is mapped onto the same alignment marks on the actual sample.
4. One 50mm-by-50mm (approximate) silicon wafer that contains approximately ten complete and functional nanowire transistors.
5. The room temperature I-V curves of the completed nanwire transistors.

However, we have yet to create a functional transistor, and so, with Dr. Jon Nakane's permission, we are extending this project into the summer after final exams. In the summer, we will create a fully functional transistor and we will do room temperature measurements of I vs. source-drain voltage and I vs. gate voltage in order to obtain the electrical characteristics of the nanowires. Because we are completing our project in the summer, we will not be giving any of our deliverables to our sponsor in April. We are extending our project until mid-May, so we expect to be able to hand over all of our deliverables at that time.

4.2 FINANCIAL SUMMARY

A financial summary will not be included in this report due to the fact that all the materials used for this project were provided by the project sponsor, and we did not purchase anything on our own.

4.3 ONGOING COMMITMENTS BY TEAM MEMBERS

There are no ongoing commitments by team members anymore.

5. RECOMMENDATIONS

In this section, changes that could be made in order to allow students to complete project objectives more easily and to create even smaller SNW-FET's are explained.

5.1 Structured Training and Certification

A bulk of time spent in this project was receiving training on various machines in order to be certified. The safety policies of the AMPEL did not allow an uncertified person to operate any machinery in the clean room, so until at least one team member was certified in several machines, little progress was made. For this project, certification in the following machines was required before the project could take off: Scanning Electron Microscope, Wet Bench, Spinner, and Evaporator. Each of these machines required few training sessions, which needed to be individually scheduled with the project sponsor or experienced users at AMPEL, adding on extra time. Therefore, for future clean room projects, it is recommended that the sponsor creates a structured training regime to be done in the first semester, and only students who will be available for the training should apply for clean room projects. The training regime should include any machines that will be frequently used. The expected outcome of this change is a much faster progress allowing the students to deal with unforeseen problems and complete the project within the expected date of completion.

5.2 Designing a new photolithography mask containing smaller, closer together alignment markers and numbers for each bonding pad

The project sponsor eventually hopes to build SNW-FETs with nanowires of shorter diameters. Smaller nanowires require a higher magnification to accurately draw electrical contact lines to them; however, the highest magnification possible is limited by alignment markers because all four must be visible on the screen for the alignment process, which is a crucial step in Electron Beam Lithography. With the current mask, x270 is the highest magnification possible, at which magnification nanowires of 150nm diameter are just about the limit. Therefore, a new mask with closer together, smaller alignment markers is necessary. The size of the alignment markers should be also decreased accordingly so that they do not fill the whole screen at higher magnifications. With a newly designed mask, building smaller SNW-FETs will be possible. It is also recommended that each bonding pad is numbered by adding numbers to the design of the mask. numbers are added to the design of the mask. This change will expedite the process of mapping nanowires and furthermore allow inexperienced students to perform e-beam lithography more quickly, which is important to prevent over-exposure and unwanted exposure.

Regarding confirming whether the contact lines made an ohmic contact with the nanowires, not much could be done within the scope of this project as a probe station that has a current source with a sufficient resolution is not available to the project sponsor, and a high-resolution probe station is the only way to perform such a delicate measurement. Currently, low-temperature measurement is thought to be the only method which could reveal the nature of the contact between the contact lines and the nanowires.

6. APPENDICES

6.1 Appendix A: Photolithography

This is the original recipe for photolithography. The design on the silicon wafer that resulted from this recipe did not have well-defined corners and alignment marks.

Photoresist
AZ4410

Photoresist Spinning Parameter
Acceleration: 425 rpm
Speed: 2000 rpm for 40 seconds

Photoresist Baking Parameter
Bake at 90 ^{o}C for 12 minutes

Photoresist Exposure Parameter
Karl Suss Aligner
Expose at UV light of wavelength 320 nm for 1.5 minutes

Photoresist developing solution: AZ400k

Post-processing cleaning
1. Wash with DI water followed by blow-drying.

Figure 27. Underdeveloped silicon wafer.
This figure shows the underdeveloped electrical pads when the silicon wafer was made using the recipe above. Note also that no alignment marks appeared after development.

This is the modified recipe for photolithography. The design on the silicon wafer that resulted from this recipe had well-defined corners and all of the alignment marks were present.

Photoresist
AZ4410

Pre-processing cleaning
1. Wash with acetone for 10 minutes
2. Wash with propanol for 10 minutes
3. Wash with DI water for 6 minutes

Photoresist Spinning Parameter
Acceleration: 425 rpm
Speed: 5000 rpm for 40 seconds

Photoresist Baking Parameter
Bake at 100 ^{o}C for 10 minutes

Photoresist Exposure Parameters
Expose at UV light wavelength for 320 nm (Integ 30)

Photoresist developing solution: AZ400K
Post-processing cleaning
1. Wash with DI water followed by blow-drying.

6.2 Appendix B: Electron-Beam lithography

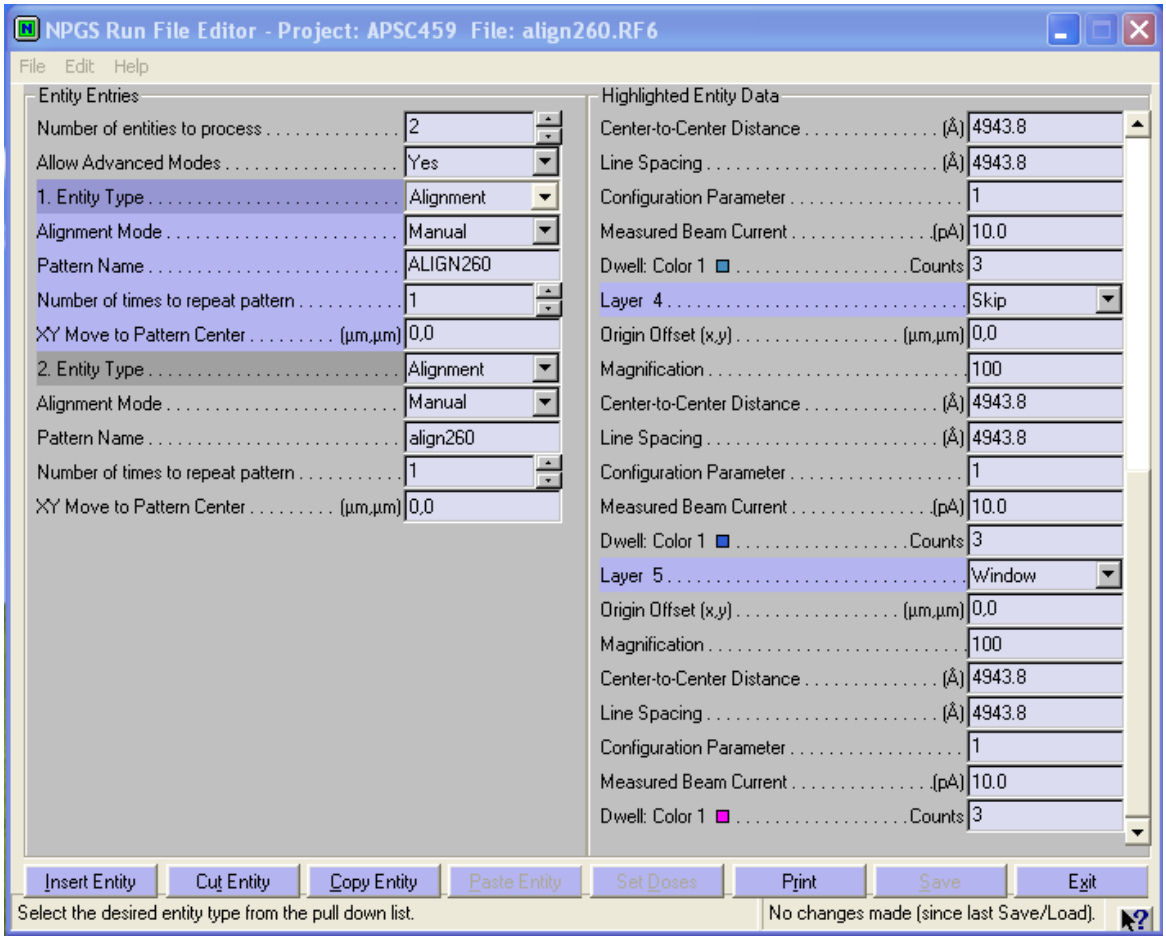


Figure 28. 100x mag. Alignment file Part I.
This is the first portion of the alignment run file at 100x magnification. When this portion is executed, the top right alignment mark among the four alignment marks used is aligned with its position on the CAD file. Only layer 5 is used because layer 5 is the actual circle on the CAD file. The squares surrounding the four alignment marks are used in the second step when all four alignment marks are aligned. All of the parameters used are shown in this screenshot.

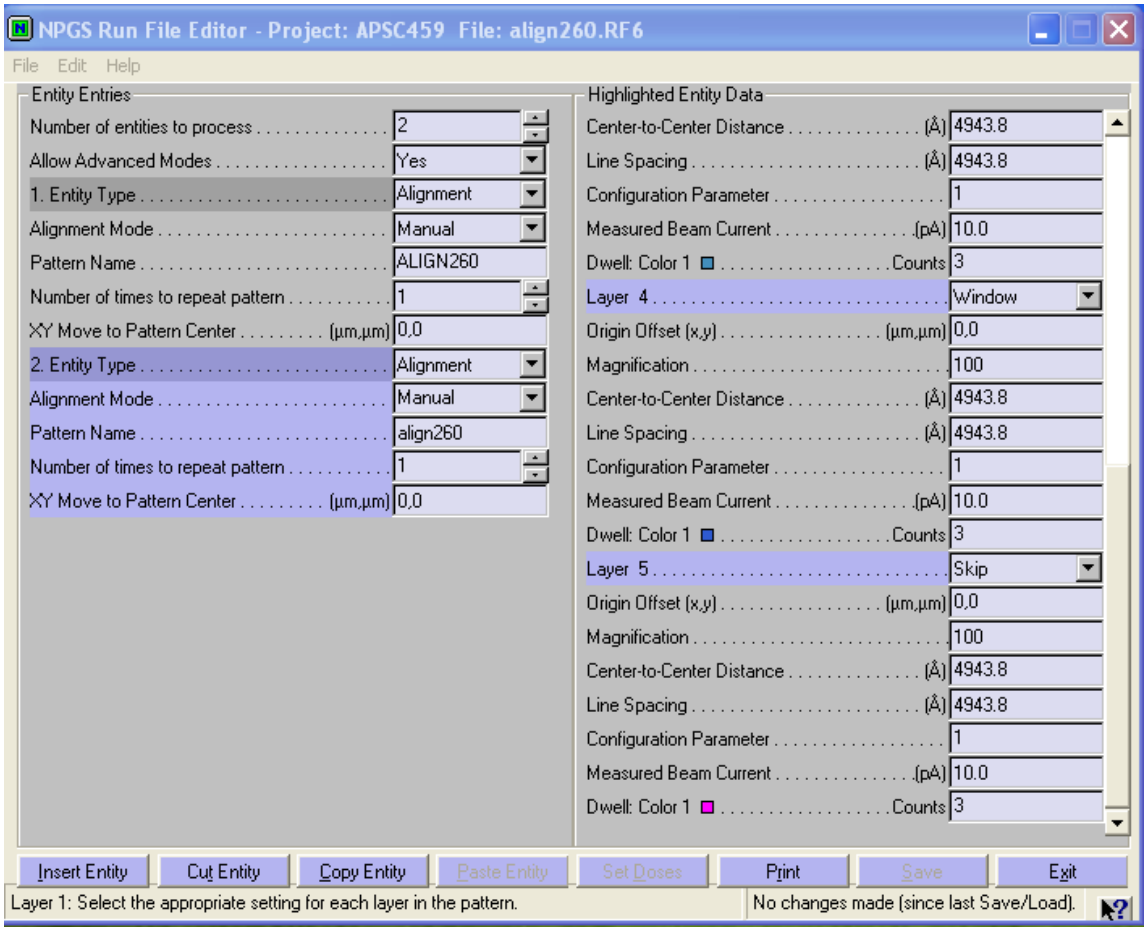


Figure 29. 100x mag. Alignment file Part II.
This is the second portion of the alignment run file at 100x magnification. When this portion is executed, all four alignment marks are used and they are aligned with their corresponding positions on the CAD file. All four layers are used in this file because the squares that surround the circles are used in this step. Only the circle (layer 5) is skipped. All of the parameters used are shown in this screenshot.

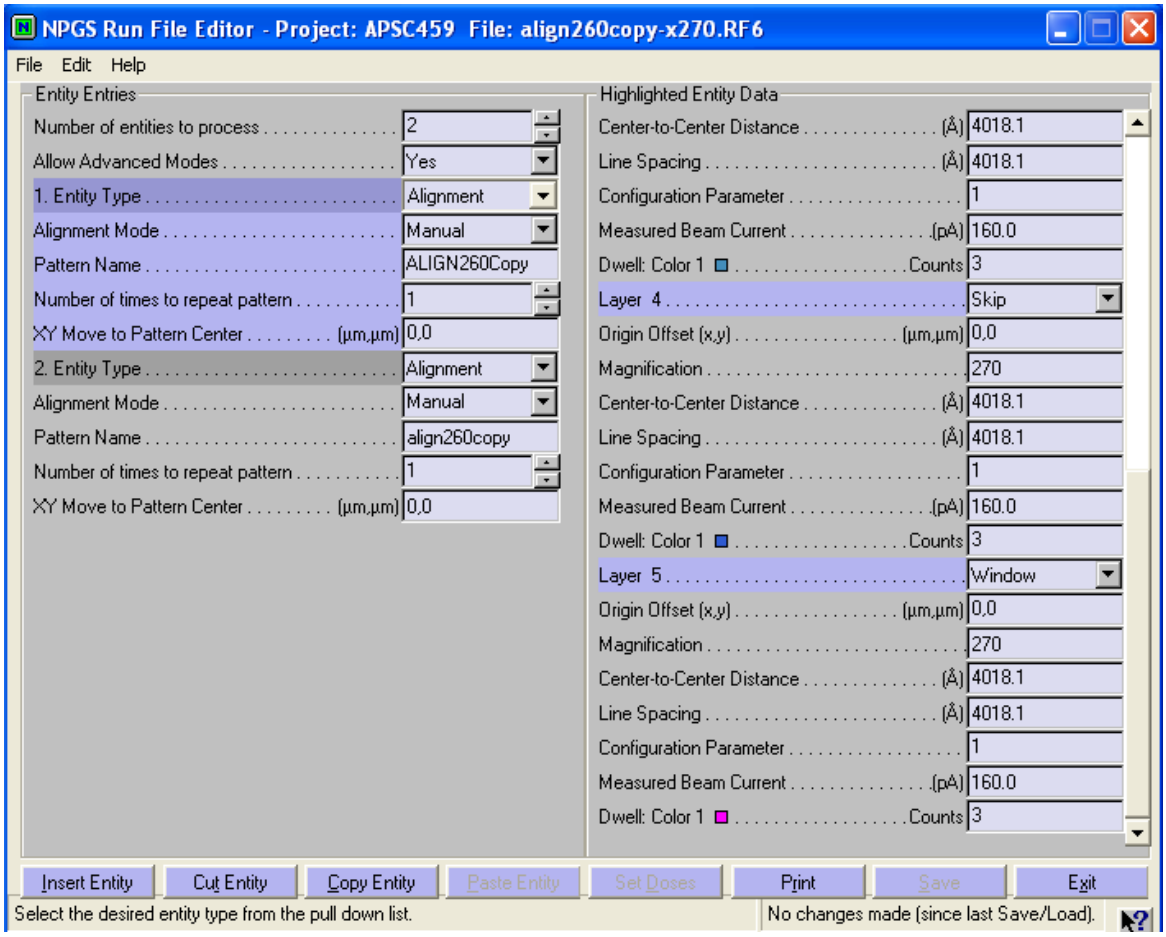


Figure 30. 270x mag. Alignment File Part I

This is the first portion of the alignment run file at 270x magnification. When this portion is executed, the top right alignment mark among the four alignment marks used is aligned with its position on the CAD file. Only layer 5 is used because layer 5 is the actual circle on the CAD file. The squares surrounding the four alignment marks are used in the second step when all four alignment marks are aligned. All of the parameters used are shown in this screenshot.

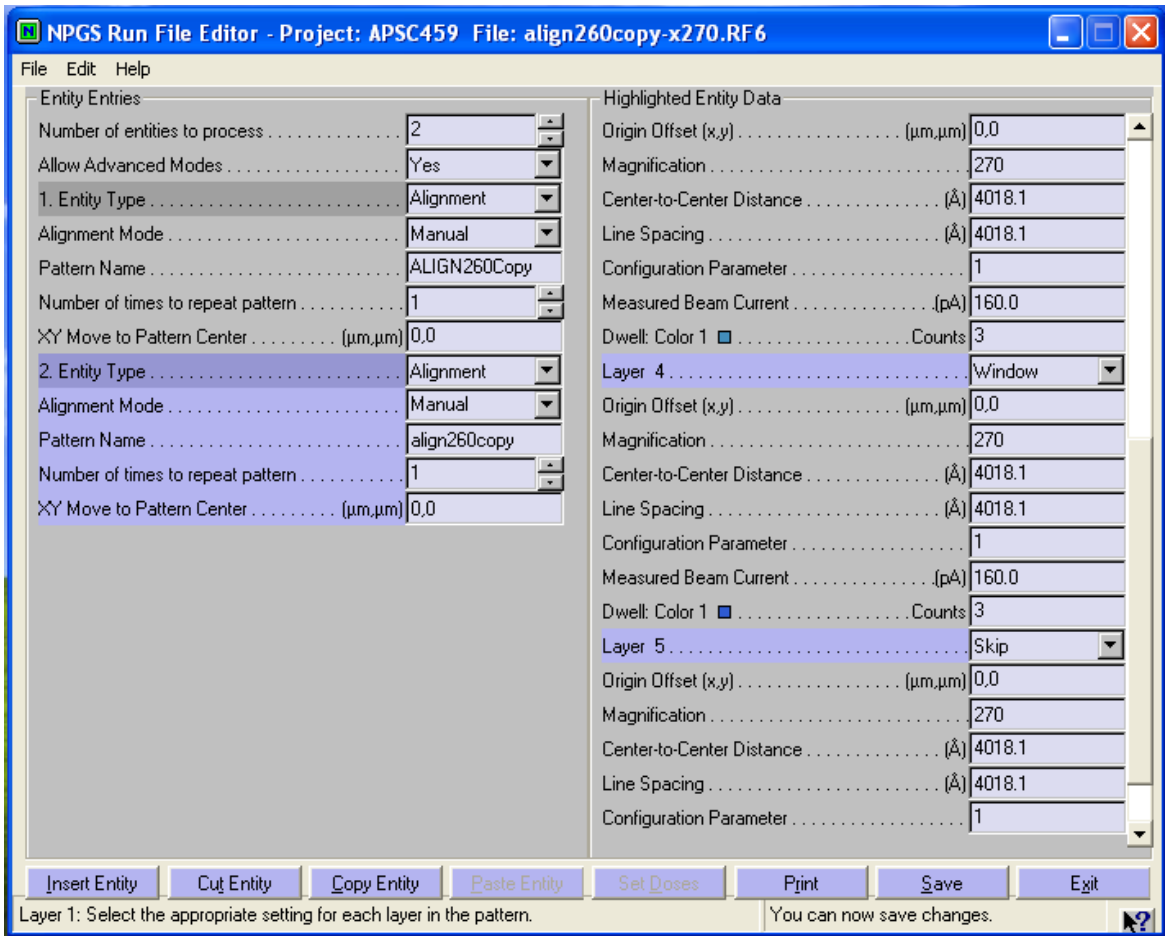


Figure 31. 270x mag. Alignment File Part II.
This is the second portion of the alignment run file at 270x magnification. When this portion is executed, all four alignment marks are used and they are aligned with their corresponding positions on the CAD file. All four layers are used in this file because the squares that surround the circles are used in this step. Only the circle (layer 5) is skipped. All of the parameters used are shown in this screenshot.

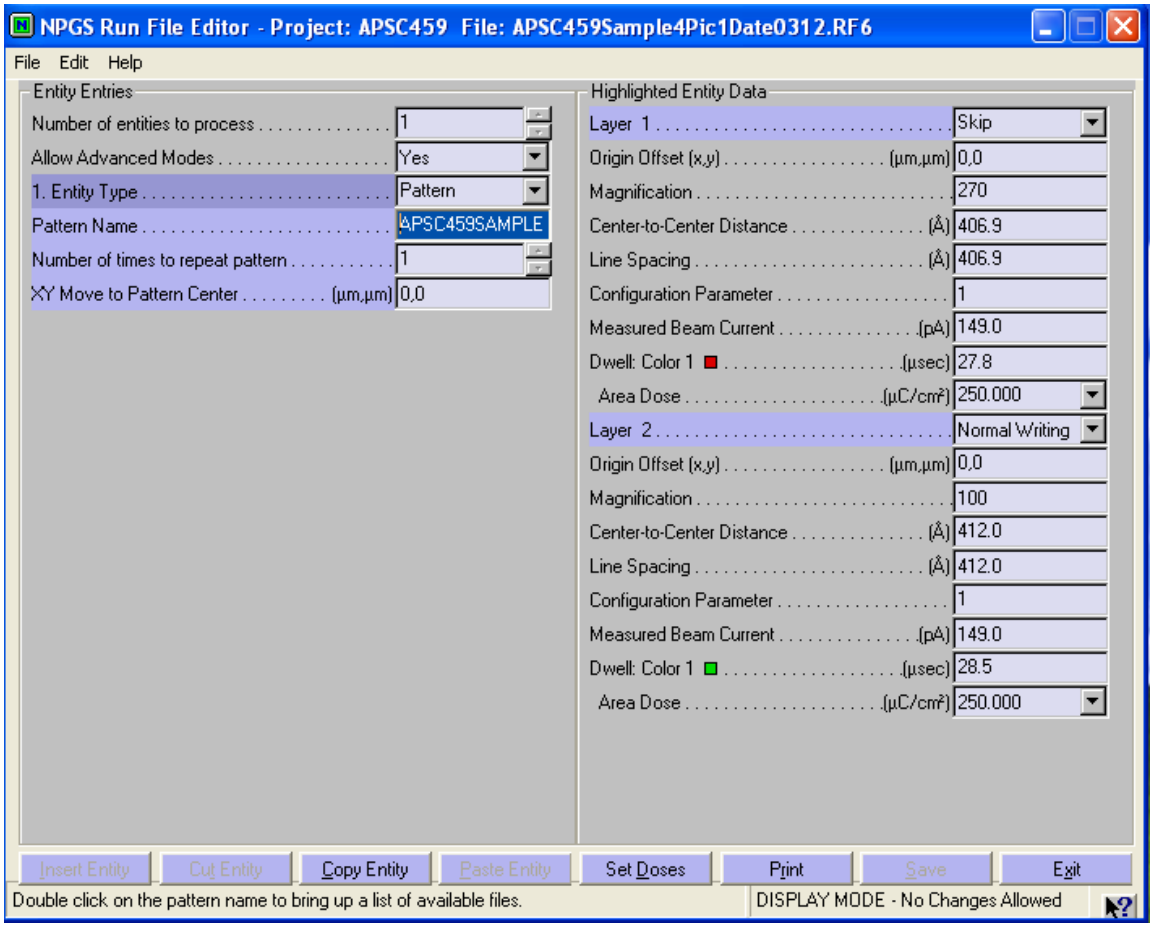


Figure 32. Run File for E-Beam Writing.

This is the run file that contains the parameters for the actual e-beam writing. This run file is used when writing at 100x magnification and at 270x magnification. The only changes needed are to switch from “Skip” to “Normal Writing” in layer 1 and layer 2.

6.3 Appendix C: PMMA DEPTH

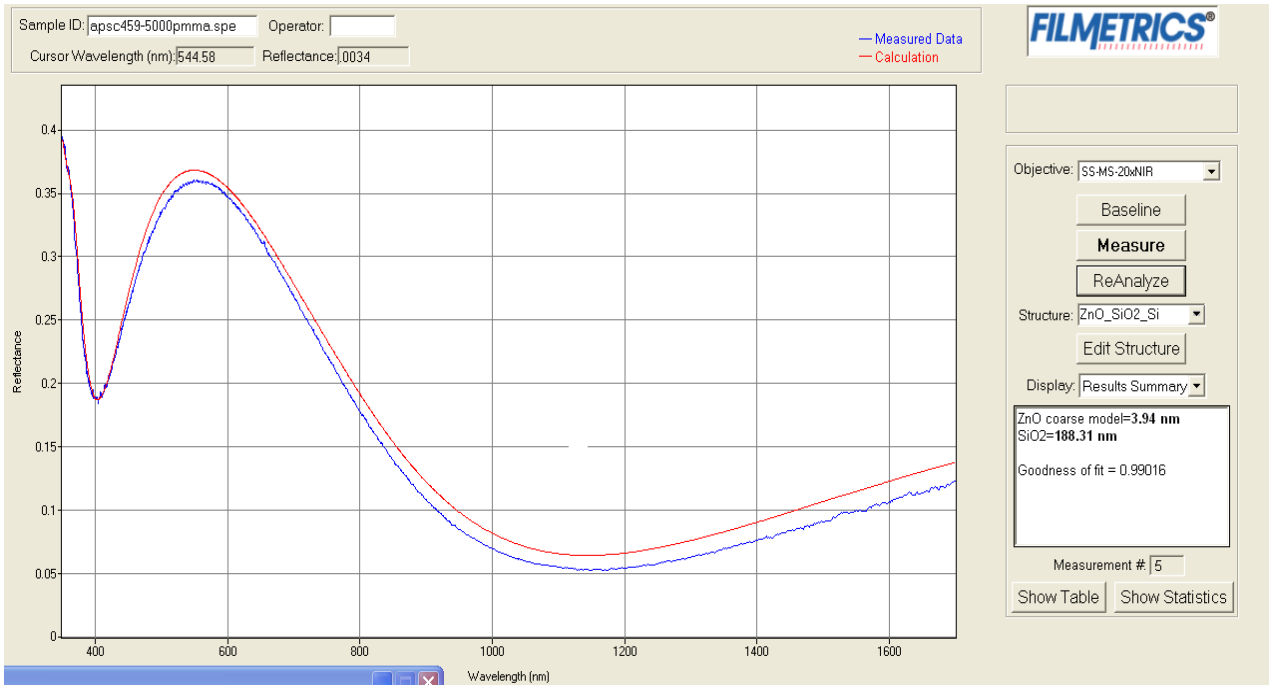


Figure 33. PMMA depth at 5000 RPM.
This figure shows the graph that is generated by the program that measures PMMA depth. The depth is measured by the reflectance of the different wavelengths of light. The depth of PMMA was found to be 188.31 nm (given in the box on the right; ignore the name). The PMMA on this sample was spun at 5000 rpm.

6.4 Appendix D: Calculated Resistance of Gold Contact Line

(Note: all of the equations were given to us by the project sponsor)

$$R = \rho \, l / A$$

where ρ is the static resistivity of gold (2.44×10^{-8} ohm-meters @ 20 ^{o}C), l is the length of the gold line (meters) and A is the cross sectional area of the gold contact line.

The length of the gold line was approximated as the center-to-center distance between the two contact pad, which was 406 μm (l); the width of the gold contact line was 2 μm (chosen arbitrarily); and the height of the gold contact line was 140 nm (determined by the sponsor when he performed evaporation). From these numbers the cross sectional area was calculated to be 2.8×10^{-13} m^2.

Thus, the calculated value of resistance (from the parameters of the gold contact line) was 35.38 ohms.

$$R = 2.44 \times 10^{-8} * 406 \, \mu m / 2.8 \times 10^{-13} \, m^2$$

6.5 Appendix E: Calculation of Resistance of InSb nanowire

(Note: All of the parameters, equations, and the assumed carrier densities were given to us by the project sponsor)

Properties of InSb

Breakdown field $\approx 10^3$ V cm^{-1} (given by our sponsor)

Mobility of Electrons (μ_e) $\leq 7.7 \cdot 10^4$ cm^{2}V^{-1}s^{-1} (given by our sponsor)

Mobility of Holes (μ_P) ≤ 850 cm^{2}V^{-1}s^{-1} (given by our sponsor)

$R = \rho \, l / A$ (given by our sponsor)

where ρ is the static resistivity, l is the length of the nanowire, and A is the cross sectional area of the nanowire.

The length of the longest nanowires (l) was approximately 10^{-3} cm and the radius of the nanowires was approximately 75 x 10^{-7} cm. Thus, A was equal to 1.77 x 10^{-10} cm^2.

Next, we need the equation for ρ:

$\rho = 1/(n \, q \, \mu_e)$ for n-doped

where n is the n-dopant density

$\rho = 1/(p \, q \, \mu_P)$ for p-doped

where p is the p-dopant density

q = elementary charge = 1.6 x 10^{-19} C

With these equations, we could calculate the resistance of the InSb nanowires (under the assumption that they were perfectly crystalline, which was unlikely). Thus, the calculated values should be the lowest values of resistance at room temperature.

Since the sponsor did not know whether the nanowires were n-type or p-type, the values of R was calculated for both n-type and p-type nanowires. In addition, the sponsor did not know the exact carrier density (knew only the range), so we calculated a total of 6 resistance values, each for n-type and p-type using three different carrier densities.

n (cm^{-3})	ρ (V cm s / C)	R (Ω)	p (cm^{-3})	ρ (V cm s / C)	R (Ω)
10^{14}	8.12	4.6 x 10^7	10^{14}	74	4.2 x 10^8
10^{15}	81.2	4.6 x 10^6	10^{15}	7.4	4.2 x 10^7
10^{16}	812	4.6 x 10^5	10^{16}	0.74	4.2 x 10^6

7. REFERENCES

1. Candebat, D. "InSb nanowire field effect transistors." Accessed from http://web.ics.purdue.edu/~dcandeba/

2. *Cornell Nanoscale Science and Technology Facility.* Cornell University. Web. 30 March 2011. http://www.cnf.cornell.edu/cnf_spietoc.html

3. *Coulomb Blockade in a Quantum Dot.* Semiconductor Group. Department of Physics, University of Cambridge. Web. 31 March 2011.

4. Danon, J., and Nazarov, Y. V. "Pauli spin blockade in the presence of strong spin-orbit coupling." *Physical Review* 80 (2009): 041301-1 – 041301-4. Web. 30 March 2011.

5. Delft University of Technology (spin-orbit nanowire transistor) http://www.tnw.tudelft.nl/live/pagina.jsp?id=2136915a-f72a-441a-8783-b0b0e91cb48f&lang=en. Web. 30 March 2011.

6. Duan, X., Huang, Y., Cui, Y., Wang. J, and Lieber, C. "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices." *Letters to Nature* 409 (2001): 66-69. Web. 30 March 2011.

7. Georgia Technical College of Engineering. Web. 30 March 2011. http://www.ece.gatech.edu/research/labs/vc/theory/photolith.html

8. Keith, C., and Shields, J. CBIO 8050: University of Georgia. Class website. 30 March 2011. http://www.uga.edu/caur/semindex.htm

9. Liu, C., Dai, L., You, L. P., Xu, W. J., and Qin, C. G. "Blueshift of electroluminescence from single In-P nanowire/p-Si heterojunctions due to Burstein-Moss effect." *Nanotechnology* 19 (2008): 1-5. Web. 30 March 2011.

10. Nadje-Perge, S., Frolov, S. M., Bakkers, E. P. A. M., and Kouwenhoven, L. P. "Spin-orbit qubit in a semiconductor nanowire." Provided by Dr. Mario Beaudoin

11. Nilsson, H. A., et al. "Giant, level-dependent g Factors in InSb nanowire quantum dots." *Nano Lettters* 9.9 (2009). 3151-3156. Web. 30 March 2011.

12. Nygard, J. Niels Bohr Institute. University of Copenhagen. Accessed on 31 March 2011.

13. Park, W. I., Kim, J. S., and Yia, G. "Fabrication and electrical characteristics of high-performance ZnO nanorod field-effect transistors". *Applied Physics Letters* 85. 21 (2004)

14. Swapp, Susan. “Scanning Electron Microscopy (SEM).” *Geochemical Instrumentation and Analysis.* Science Education Resource Center at Carleton College. Web. 30 March 2011. http://serc.carleton.edu/research_education/geochemsheets/techniques/SEM.html

15. Sze, S. M. *Physics of Semiconductor Devices*. New York: John Wiley & Sons, Inc., 1981.

16. *The Metal-Semiconductor Junction. Schottky Diode. Ohmic Contacts*. 6 June 2006. Web. 31 March 2011.

17. Wang, J. “Co-op term report”. University of Waterloo, 2009. Web. 30 March 2011.

18. Wolfe, D., J. Singh. *Surface and Coatings Technology*. **124**. pp. 142–153. (2000).