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Research paper

Special Focus on Optical Wireless Communication

Undersampled differential phase shift on-off keying for optical camera communications

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Abstract: OCC (Optical Camera Communication) has been proposed in recent years as a new technique for visible light communications. This paper introduces the implementation and experimental demonstration of an OCC system. Phase uncertainty and phase slipping caused by camera sampling are the two major challenges for OCC. In this paper, we propose a novel modulation scheme called undersampled differential phase shift on–off keying to encode binary data bits without exhibiting any flicker to human eyes. The phase difference between two consecutive samples conveys one-bit information, which can be decoded by a low-frame-rate camera receiver. Error detection techniques are introduced to enhance the reliability of the system. We present the hardware and software design of the proposed system, which is implemented with a Xilinx FPGA and a Logitech commercial camera. Experimental results demonstrate that a bit-error rate of 10^{-5} can be achieved with 7.15 mW received signal power over a link distance of 15 cm.

Keywords: image sensor, light-emitting diode, optical camera communication, undersampled differential phase shift on-off keying, visible light communication

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1 Introduction

In recent years, the LED (Light-Emitting Diode) has become the light source of choice for sustainable illumination. LEDs are quickly replacing incandescent lamps, given their improved brightness, lower energy consumption, and longer lifespan. It is estimated that by replacing all existing light sources with LEDs, the world electricity energy consumption can be dramatically reduced by 50%[1]. The development of LED illumination technology also offers great opportunities for data transmission. Relevant research of VLC (Visible Light Communication) with LEDs originated in Japan around 2003 with the establishment of the VLCC (Visual Light Communication Consortium). Since then, VLC has attracted significant research and development interests.

The first VLC standard, IEEE 802.15.7, was initiated in 2008 and completed in 2011. However, VLC products have not emerged into the marketplace to any great extent. This perhaps largely results from the need to integrate VLC systems into existing portable smart devices. OCC offers a means for this integration[2,3]. Given the significant potential for OCC, an amendment is being made to the VLC standard by the IEEE 802.15.7r1 OWC task group. This revision is expected to be published by 2018. There is an immense interest to integrate OCC technology into billions of existing smart devices, without requiring significant hardware modification.

It should be noted, however, that challenges still

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exist for OCC. First, the sampling rate of a commercial camera is typically 30 frames/s, which is considered low for communications. Second, the flicker of LED lighting may induce a biological human response. For this reason, it is suggested that flicker in the 3-70 Hz range should be avoided[4]. Thus, a flicker-free OCC transmitter must blink at frequencies that exceed the camera's frame rate, and the receiver has to undersample the transmitted signals. Third, the transmitters and the receivers are typically unsynchronized, so it becomes challenging to track and compensate for the phase difference between signal transmission and reception. Because of this, the received OOK (On-Off Keying) waveform slowly slips in time, with respect to the sampling point[5], which leads to bit errors and degenerated system performance.

Demodulation of OCC is more challenging than that of non-imaging VLC systems. Several modulation techniques have been proposed for OCC in recent years[6-11]. First, PAM (Pulse Amplitude Modulation) and QAM (Quadrature Amplitude Modulation) were proposed and demonstrated for OCC[9,10]. These techniques typically use more than two amplitude levels; however, it is necessary to correct for the nonlinearity in the applied image sensors. This is achieved with gamma correction, which must be applied before demodulation[12], and it is necessary to introduce a special frame head sequence. This sequence is used to detect the camera sample phase and obtain the gamma curve. Second, UFSOOK (Undersampled Frequency Shift On-Off Keying) was also proposed and demonstrated for OCC[8]. It uses a pair of discrete OOK frequencies to transmit logic ones and zeros. Different symbols present different patterns to the camera. The demodulator then uses two image frames to decode one bit. Because of this, the bitrate cannot exceed half of the camera sample rate. To be more specific, if UFSOOK is applied to a typical 30-frames/s camera receiver, the data rate is limited to 15 bit/s. Third, UPSOOK (Undersampled Phase Shift On-Off Keying) has also been proposed and demonstrated for OCC[11]. It is a dual-LED modulation technique that can accomplish higher transmission speeds. This modulation relies on different combinations of the ON/OFF status of two LEDs. Thus, the demodulator is required to know the exact sampled phase of the camera. To do so, the authors designed a special frame head sequence that is examined before every frame is demodulated. If an incorrect sample phase is detected, all sampled values in the same data frame are inverted. Fourth, a space–time forward error correction scheme with UFSOOK was proposed and demonstrated[5]. Such a scheme can mitigate the effects of ambient light and asynchronous frequencies between the transmitter and the receiver to improve the BER (Bit-Error Rate) performance. The same authors used multiple-phase sampling to detect and correct the erroneous sample phase. This requires the transmitter to repeat the same data frame three times, either spatially or temporally, which will reduce the communication rates.

In this paper, we propose a novel modulation scheme called UDPSOOK (Undersampled Differential Phase Shift On-Off Keying) to overcome the phase uncertainty problem as well as the low data rate problem. The benefit of the proposed scheme is that it does not require the sampling phase of the camera to be known. Furthermore, the scheme uses a new error detection mechanism that can reduce the error bits caused by phase slipping. The results from a full experimental characterization are presented to demonstrate the feasibility of the proposed OCC system.

2 Modulation/Demodulation

To prevent human eyes from photobiological hazard, OCC systems are required to exhibit no flicker to users with different dimming requirements. The ideal blinking frequency of an OCC transmitter is between 90 Hz and 1 000 Hz[8]. Assuming that the frame rate of a commercial camera is f_s and the frequency of the OOK square wave carrier is f_c, we can always find an integer n for UDPSOOK to ensure

$$f_c = n \times f_s, \quad 90 \text{ Hz} < f_c < 1\,000 \text{ Hz}. \tag{1}$$

The transmitted UDPSOOK signal $s(t, \theta)$ can be expressed as

$$s(t, \theta) = \text{sgn}[\sin(f_c t + \theta)], \tag{2}$$

where f_c is chosen according to (1), θ is the phase of the OOK carrier, and the sgn function is defined as

$$\text{sgn}(x) = \begin{cases} 1, & x \geqslant 0, \\ 0, & x < 0. \end{cases} \tag{3}$$

At every $1/f_s$ s, the modulator changes the value of θ depending on the binary bit to be transmitted. When a "1" bit is transmitted, the modulator adds a π phase shift to the current signal. When a "0" bit is transmitted, the modulator adds a 0 phase change to θ. In other words, one bit of information is represented by a change of phase between two consecutive frames.

Fig. 1 illustrates the modulated waveform of binary sequence "110". In the figure, we assume that f_s is the camera sampling rate and $n = 4$ so that $f_c = 4f_s$. Every frame consists of 4 cycles of the OOK carrier. Dashed lines define the $1/f_s$ second interval. The phase of the square waveform has been toggled twice in the first two $1/f_s$ s to transmit two logical ones. In contrast, the phase remains unchanged for the last frame to send a logical zero. The red lines represent the sampling moments of the receiver.

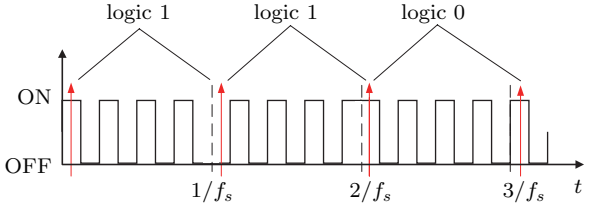


Figure 1 Modulated UDPSOOK symbols

At the demodulator, received bits are determined by comparing the phase between two consecutive samples. The demodulation rule can be simply expressed as

$$\theta_k - \theta_{k-1} = \theta_\Delta = \begin{cases} 0, & \text{"0"}, \\ \pi, & \text{"1"}, \end{cases} \tag{4}$$

where θ_k is the carrier phase of the kth sampling. This rule can be implemented by using an exclusive OR operation as

$$b_{k-1} = s_k \oplus s_{k-1}, \tag{5}$$

where s_k is the kth sampled value of the camera. We map s_k to "1" when the LED is on and s_k to "0" when the LED is off. The structure of the demodulator can be simplified as shown in Fig. 2.

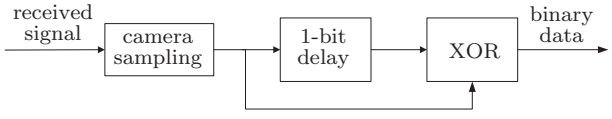


Figure 2 UDPSOOK demodulation

UDPSOOK transmits signals by controlling the phase difference of two consecutive samples so that n camera frames carry $n - 1$ bits of information. The theoretical maximum data rate $R_{\max}$ can be obtained by

$$R_{\max} = f_s \times \lim_{n \to \infty} \frac{n-1}{n} = f_s, \tag{6}$$

which has been doubled compared to the maximum achieved data rate in Ref. [8].

It should be noted that it is generally difficult to predict the sampling phase of a camera in a practical OCC system, because the sampling can occur at any position on the timeline. But UDPSOOK does not require the relationship between the camera sampling points and the received signal waveforms to be known because the demodulation is based solely on the phase difference between two frames. Fig. 3 illustrates how UDPSOOK is immune from the camera phase uncertainty. In Fig. 3, the time difference between two consecutive arrows with the same color is $1/f_s$. Different colors indicate different sampling phases. The sampled result of the red arrows is an LED status sequence [ON,OFF,ON,ON], which indicates the bit sequence "110". If the sampling takes place at the green positions, which have a π phase shift from the red arrows, the sampled values will be fully inverted as [OFF,ON,OFF,OFF]. However, the UDPSOOK demodulator still obtains the bit se-

quence "110" from the green samples. This is because the phase difference between two consecutive frames does not change.

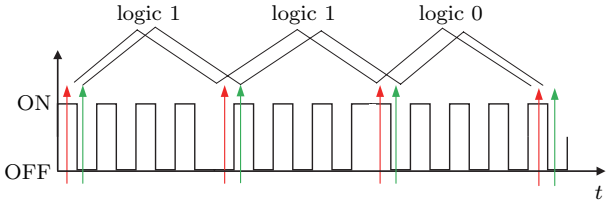


Figure 3 Different sampling timing for UDPSOOK

UDPSOOK also supports dimming control. The LED brightness can be changed by increasing or decreasing the duty cycle of the OOK signal. A fixed 50% duty cycle is not always practical[5]. Assuming a logical "1" is transmitted by UFSOOK and UDPSOOK, as shown in Figs. 4(a) and 4(b), respectively, it is seen that UFSOOK is more likely to have an erroneous sampling result (as seen by the green arrows) when the duty cycle is greater than 50%, but UDPSOOK can adapt to any different duty cycle.

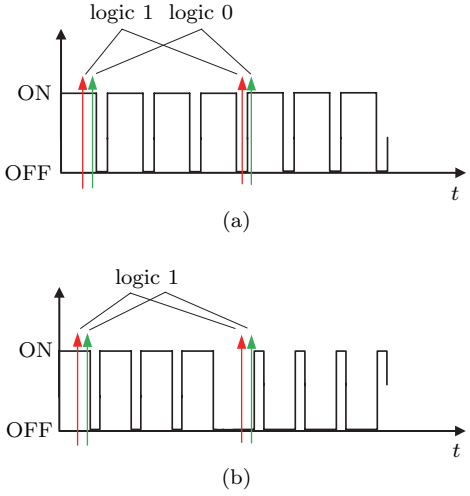


Figure 4 Non-50% duty cycle demodulation with (a) UDPSOOK and (b) UFSOOK

Another problem introduced by image sensors is phase slipping. For a typical OCC system, because the receiver and the transmitter are not strictly synchronized, the sampling points are gradually slipping with respect to the OOK waveforms. A sampling error occurs repeatedly as phase shift accumulates. In our experiment, we found phase slipping to be a major source of bit errors. With this in mind, we propose an error detection technique for UDPSOOK to reduce the system BER. In this proposed system, two LEDs are employed. We use one LED to accomplish data transmission and the other LED to carry out error detection. The LED designated for data transmission is a UDPSOOK transmitter, and the LED designated for error detection continues sending bit zeros during the data transmission. A zero UDPSOOK bit sequence triggers no phase toggling, so the demodulator observes no phase difference on received image samples. Because these two LED suffer from the same channel noise and phase slipping problem, if any sampling error occurs, the error detection LED can precisely indicate the incorrect samples by looking for a sudden phase change. The demodulator then corrects the sampling errors by simply flipping the erroneous sampled values.

Fig. 5 shows the implementation of UDPSOOKED (UDPSOOK Error Detection) sampling. The red arrows indicate a correct sampled sequence [ON, OFF], which is decoded as a bit "1". When a phase error occurs, the second red sampling point slips to the green arrow position and results in an incorrect sampled sequence [ON, ON], which will be decoded as a bit "0". This error can be observed by the receiver owing to the sampled phase change of the error detection LED. On the error detection LED, any status change indicates a bit error.

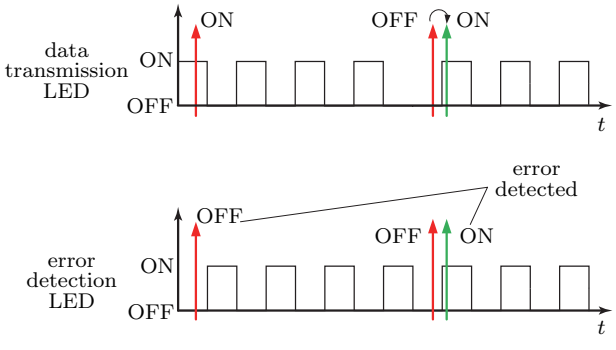


Figure 5 UDPSOOKED sampling and error detection

The demodulator will invert the second sampled value to obtain the correct decoded bit.

It should be noted that UDPSOOKED doubles the overhead of a single LED OCC system by introducing an extra transmitter. However, the efficiency can be significantly improved when multiple LEDs can share a common error detection LED in a MIMO (Multiple-Input Multiple-Output) system. In this case, two or more data transmission LEDs are used. Fig. 6 illustrates one of the possible MIMO schemes for UDPSOOKED. In the figure, LED 1 to LED 4 are data transmission LEDs, and only one LED (LED 5) is used for error detection.

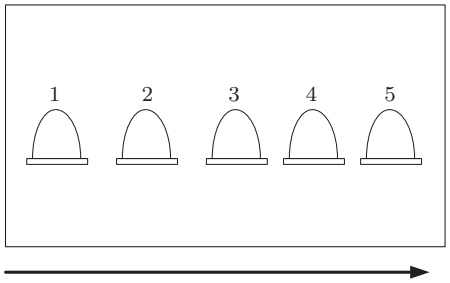


Figure 6 A MIMO scheme for UDPSOOKED

The rolling shutter effect should be considered when a rolling shutter image sensor is used in a UDPSOOKED MIMO system. A rolling shutter image sensor captures a picture by scanning the scene vertically or horizontally rather than recording the entire scene at a single instant. Because most CMOS image sensors arrange pixels in rows, and those rows are activated sequentially in one exposure, the rolling shutter effect may lead to a skewed image when capturing a moving object[6]. In a MIMO system as shown in Fig. 6, LED 5 is designated for error detection, and the arrow indicates the shutter rolling direction of the receiver. LED 5 may fail to detect error samples with a rolling shutter receiver that has a horizontal scan direction because LED 1 is exposed earlier than LED 5 in one snapshot as shown in Fig. 6. The exposure time difference depends on the shutter speed of the receiver. A slower shutter speed means higher probability of bit errors. For this reason, we suggest placing LEDs in a line and maintaining the camera rolling direction perpendicular to the transmitters. Global shutter cameras do not have this problem.

3 Framing structure

To detect the start of transmission, the UDPSOOK data are preceded by an SFD (Start Frame Delimiter). An extra bit is added to the end of the payload for parity check to further enhance the system reliability. Such a data frame is shown in Fig. 7.

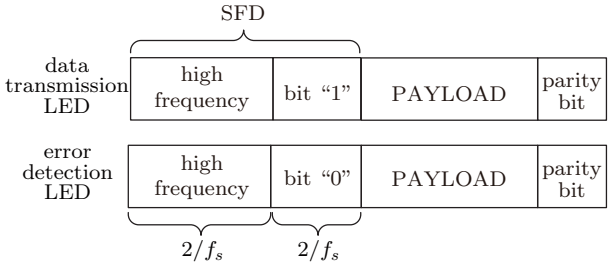


Figure 7 Frame structure of the proposed OCC system

An SFD consists of two parts. The first part is a high-frequency OOK symbol that lasts for two frames. This high frequency must be greater than the cutoff frequency of the receiver so that this status can be recognized neither as fully ON nor as fully OFF. Instead, the camera extracts the average intensity[8] and interprets this status as half ON assuming a 50% duty cycle is used.

The second part of the SFD for a data transmission LED is a UDPSOOK bit "1" (Fig. 7). If a logical "1" is not observed during the decoding of an SFD, the data frame might have been corrupted and should be discarded. The error detection LED has a different second part of SFD. After the first $2/f_s$ s, it starts to transmit a bit "0"; i.e., two frames of OOK signals that have identical phases. In this way, an SFD not only starts a frame but also helps the receiver distinguish between the two different functional LEDs. If a receiver observes a logical "0" after the $2/f_s$ s with half ON, it will recognize this LED as an error detection transmitter.

Following the SFD is the payload of the data frame. The data frame ends when the receiver detects another SFD. The last bit of a data frame is a parity bit used to detect the possible transmission errors. The receiver calculates the number of "1"s when a full data frame is received. When par-

ity check fails, all data in the current frame will be discarded.

4 Experimental setup

Fig. 8 demonstrates our experimental setup. A Xilinx FPGA is used to modulate information and carry out logical operations for transmitters. As shown in the figure, a breadboard provides connections between the evaluation board and the Digilent PmodLED LED module, which is powered by 2 mA 3.3 V FPGA I/O (Input/Output) pins. A camera receiver continuously records videos on the other side. Image processing is then performed off-line in MATLAB.

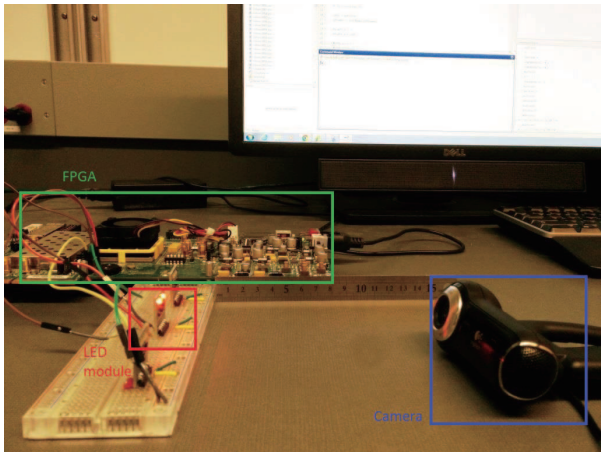


Figure 8 Experimental setup for the proposed OCC system

The finite state machine in Fig. 9 shows the transmission process. When transmission starts, the modulator first sends a high frequency signal as part of the SFD. A UDPSOOK bit "1" follows; i.e., two frames of OOK with π phase difference. The modulator then changes the phase of the carrier every $1/f_s$ s according to the next input bit. At the end of the transmission, a parity bit will be calculated and added to the end of the frame. This modulation for the finite state machine is implemented in Verilog HDL (Hardware Description Language). Xilinx Vivado Design Suite performs RTL (Register-Transfer Level) synthesis, timing analysis, etc., and the in-built simulator provides reliable behavioral verification before testing on hardware. The simulation result is shown in Fig. 10. An *enRead* pulse reads one bit from the memory, and *LED_En* enables the I/O ports on and off according to the modulation rules. Note that the time scale has been shrunk by 1 000 times to improve simulation efficiency and Fig. 10 demonstrates only the initial 300 s after reset.

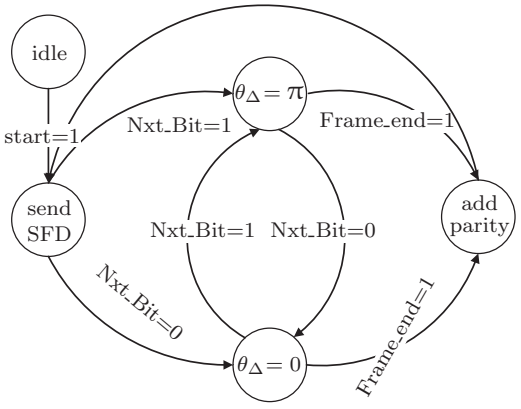


Figure 9 The transmission control of finite state machine

An LED driver circuit can supply sufficient power to match the electrical characteristics of the LEDs. We select the Digilent PmodLED LED module for our transmitters. The PmodLED LED module integrates four high-brightness monochrome red LEDs with the necessary driver circuits. Those low-power-consumption LEDs can be driven by less than 1 mA of current.

At the receiver, videos are recorded by a Logitech Pro 900 camera. The camera is connected to a PC where captured images are processed via MATLAB. Demodulation is performed off-line after the frames are captured. The process starts with monitoring the first SFD, which indicates the beginning of a new data frame. After an SFD is found, the demodulator begins to compare two consecutive samples to determine the transmitted bit. This process repeats until the next SFD is detected. We must check the parity bit before proceeding to the next data frame. For UDPSOOKED, assuming the decoded bit sequences on two LEDs are $\{R_{d0}, R_{d1}, R_{d2}, \cdots, R_{dk}\}$ and $\{R_{e0}, R_{e1}, R_{e2}, \cdots, R_{ek}\}$, the final decoded sequence is given by

$$B_k = R_{dk} \oplus R_{ek}. \tag{7}$$

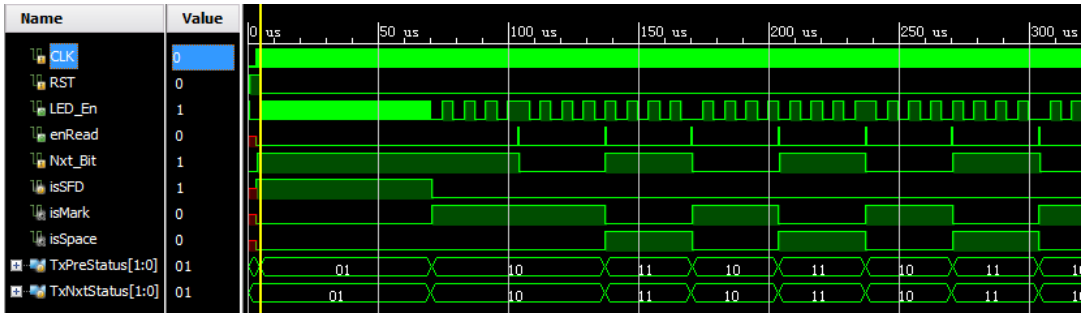


Figure 10 The simulation results in the Xilinx Vivado simulator

5 Experimental results

5.1 Received optical power

Because the LED electrical power consumption is only on the order of 1 mW, one of our central concerns is how much optical power has reached the camera. Fig. 11 shows the experimental setup used to measure the optical power at the receiver. In the figure, d is the transmission distance, and f is the focal length of the 1-in-diameter lens. We employ a high-speed photodetector (Thorlabs DET36A) for the measurement. The voltage difference across the load resistor R_L is directly measured in the experiment. We select a 10 MΩ resistor because a low generated photocurrent can be expected. Tab. 1 gives the voltage results over three different transmission distances.

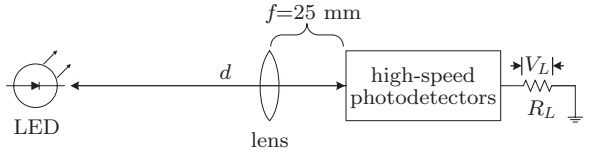


Figure 11 Optical power measurement setup

Table 1 Received optical intensity I

distance	voltage	current	incident power	intensity
15 cm	2.36 V	2.36 µA	7.15 µW	1.41 µW/cm^2
50 cm	220 mV	22 nA	66.67 nW	13.16 nW/cm^2
100 cm	60.8 mV	6.08 nA	18.42 nW	3.64 nW/cm^2

The responsivity curves of the selected photodetector can be obtained from the product specification as shown in Fig. 12[13]. The PmodLED module emits only red light (with a wavelength in the vicinity of 650 nm), so we select the responsivity of $R = 0.33$ A/W. Because the responsivity of a photodiode is defined as a ratio of the photocurrent to the incident light power at a given wavelength, to calculate the received optical power, we use

$$P_{\text{inc}} = \frac{I_{\text{PD}}}{R}, \tag{8}$$

where P_{inc} is the incident power, and I_{PD} is the photocurrent. The photocurrent can be calculated from

$$I_{\text{PD}} = \frac{V_L}{R_L}, \tag{9}$$

where V_L is the voltage across the load resistor R_L. The result is also shown in Tab. 1. As expected, the received power dramatically drops when we increase the transmission distance.

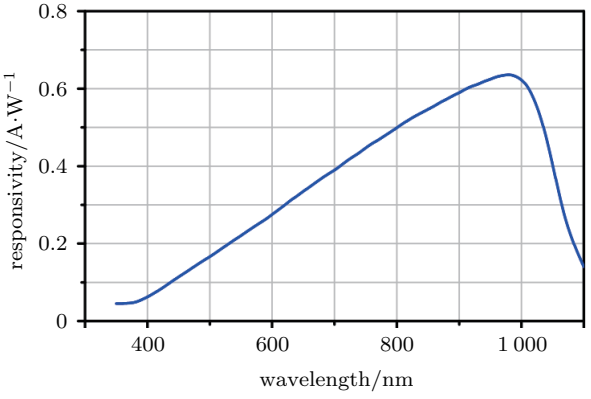


Figure 12 DET36A responsivity

Using the area of a 1-in-diameter lens as $\pi \times (25.4 \text{ mm}/2)^2$, the signal intensity at the receiver can be estimated. Over the distance of 1 m, we have

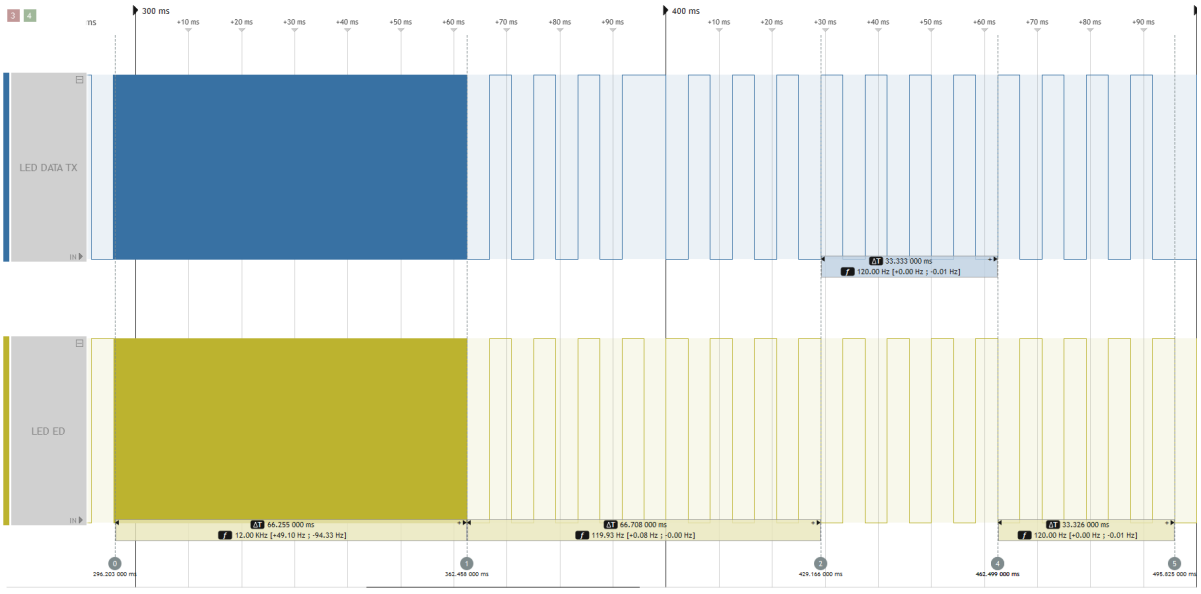


Figure 13 Captured waveforms from the logic analyzer

a signal intensity of

$$I_{d=1\mathrm{m}} = \frac{(P_{\mathrm{inc}})_{d=1\mathrm{m}}}{A} = \frac{18.42\ \mathrm{nW}}{\pi \times (25.4\ \mathrm{mm}/2)^2} \approx 3.64\,\mathrm{nW/cm^2}. \quad (10)$$

Similarly, we can calculate the signal intensity for 15 cm and 50 cm, which is shown in Tab. 1. Our experimental results show that the ambient intensity is on the order of $0.1\,\mathrm{nW/cm^2}$, so we have approximately 10 dB of dynamic range.

5.2 BER and bitrate

In our experiment, the modulator has been implemented on a Xilinx VC707 evaluation board. It should be noted that the modulation logic can be implemented on any entry-level microcontroller or FPGA because of the low requirement for resources. We use a logic analyzer to verify the modulated signals. The captured waveforms are shown in Fig. 13. The blue waveform represents the data transmission channel, and the yellow waveform represents the error detection channel. In Fig. 13, a new data frame starts at 296 ms. A bit "1" has been transmitted between 362 ms and 429 ms on the blue channel as part of the SFD, which is followed by UDPSOOK payloads. As we can see from the figure, there is no phase change on the error detection channel.

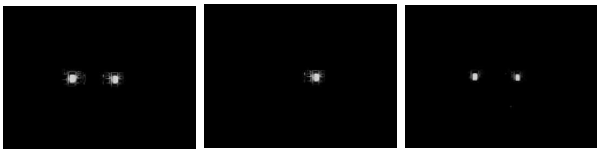
For the experimental tests, we use the modulated electrical signals to drive the LED circuits. The Digilent high-brightness LEDs can function with low power requirements. In our experiment, for each LED, the electrical power consumption is 3.30 V × 2.45 mA = 8.10 mW.

At the receiver, videos are recorded. The camera is set up in a normal indoor environment with typical levels of ambient light. We set the frame rate as 30 frames/s and collect images for processing by MATLAB. In the experiment, auto white balance and other optimization options have been disabled. With proper configurations, the influence of ambient light can be reduced, so the camera can identify the transmitted image with a lower error rate. Key experimental parameters are shown in Tab. 2. We collect approximate 20 000 frames for each measurement.

Table 2 Key experimental parameters

parameter	value
camera frame rate	30 frames/s
resolution	640 × 480
saturation	0
LED DC offset	1.65 V
LED peak-to-peak voltage	3.3 V

Fig. 14 demonstrates the different LED statuses captured by our camera within a data transmission. In each subfigure, the left hand side is a data transmission LED, and the right hand side is an error detection LED. Fig. 14(c) presents an SFD symbol, in which the intensity of the two LEDs is shown as half ON. In Fig. 14(a), the data transmission LED is fully ON, and in Fig. 14(b), the data transmission LED is fully OFF. As one might expect, the status of the error detection LED remains unchanged during the bit transmission.



(a) (b) (c)

Figure 14 UDPSOOKED symbols captured: (a) ON; (b) OFF; (c) SFD

We have tested four different communication distances for both UDPSOOK and UDPSOOKED. The BER results are shown in Tab. 3. UDPSOOK provides acceptable BER performance for all four distances considered, whereas UDPSOOKED can lower the BER, especially for the distances of 15 cm and 50 cm. The result also shows that when the transmission distance is increased, the system BER also increases, as expected.

Table 3 BER performance

modulation	UDPSOOK	UDPSOOKED
15 cm	2.48×10^{-4}	4.96×10^{-5}
50 cm	4.25×10^{-4}	6.08×10^{-5}
80 cm	7.29×10^{-3}	1.81×10^{-3}
100 cm	8.15×10^{-3}	1.88×10^{-3}

The measured data rates are shown in Tab. 4 and Fig. 15. It is shown that when communication distance increases, data rate decreases. This is because the received optical intensity decreases with increasing link distance as expected in Tab. 1.

Table 4 Data rate performance/bit·s^{-1}

distance	15 cm	50 cm	80 cm	100 cm
UDPSOOK	23.02	22.05	15.60	14.30
UDPSOOKED	15.02	13.87	9.70	8.95

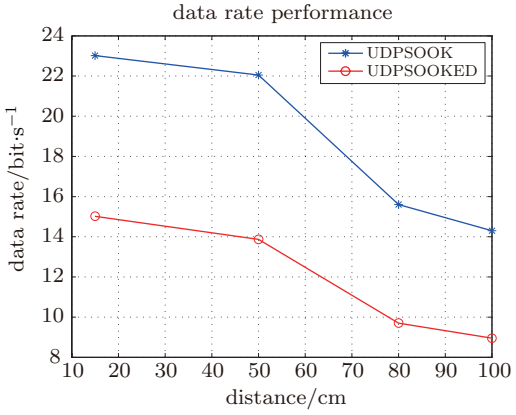


Figure 15 Data rate performance

6 Conclusion

In this paper, we proposed a novel modulation technique named UDPSOOK for OCC. We also designed an error detection scheme, using a second LED as a detector of phase slipping errors. This scheme mitigates the asynchronization problem of OCC. An experimental communication link was implemented by using monochrome LEDs and a low-cost commercial camera. Experiments demonstrated that a BER of 10^{-5} can be achieved with low overheads.

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