

Undersampled Differential Phase Shift On-Off Keying for Optical Camera Communications with Phase Error Detection

Niu Liu*, Julian Cheng[†] and Jonathan F. Holzman[‡]

School of Engineering, The University of British Columbia
Kelowna, BC, Canada V1V 1V7

Email: *niu.liu@alumni.ubc.ca, [†]julian.cheng@ubc.ca, [‡]jonathan.holzman@ubc.ca

Abstract—This paper introduces the design and implementation of an optical camera communication (OCC) system. Phase uncertainty and phase slipping caused by camera sampling are the two major challenges for OCC. In this paper, we propose a novel modulation scheme to overcome these problems. The undersampled differential phase shift on-off keying is capable of encoding binary data bits without exhibiting any flicker to human eyes. The phase difference between two consecutive samples conveys one-bit information which can be decoded by a low frame rate camera receiver. Error detection techniques are also introduced to enhance the reliability of the system. Furthermore, we present the hardware and software design of the proposed system. This low-cost communication system has been implemented with a Xilinx FPGA and a Logitech commercial camera. Experimental results demonstrate that a bit-error rate of 10^{-5} can be achieved with 7.15 microwatts received signal power over a link distance of 15 centimeters.

I. INTRODUCTION

In recent years, with the increasing concerns regarding energy consumption and environmental protection, the light emitting diode (LED) has become the choice for sustainable illumination. LEDs are now gradually taking the place of incandescent lamps. This green technology offers more brightness, lower energy consumption, and longer lifespan, making it well-suited for architectural decoration, traffic control, general lighting etc. The development of illumination technology also offers great opportunities for transmitting data by LEDs. Relevant research of visible light communication (VLC) originated in Japan around 2003 with the establishment of the Visual Light Communication Consortium (VLCC). After that, VLC has been attracting growing interest worldwide.

Initiated in 2008 and completed in 2011, IEEE 802.15.7 was the first VLC standard. After years of waiting, there are few commercialized VLC products on the market. Due to the increasing popularity of portable smart devices, some researchers [1] believed that camera communication is much closer to the market than photodiodes. More interest has been attracted to utilize embedded commercial cameras as VLC receivers [2]. Considering camera data reception is a necessary and significant amendment to the VLC standard, a revision to 802.15.7 is currently being undertaken by IEEE 802.15.7r1 OWC task group. This revision is expected to be published by 2018. Engineers are looking forward to extending OCC

technology to billions of existing smart devices with the new VLC standard, without requiring any hardware modification.

However, challenges and technical problems still exist for OCC. Firstly, the sample rate of a commercial camera is typically 30 frames per second (fps). As LED lighting flicker may induce biological human response, it is suggested that flickering in the 3 Hz to 70 Hz range should be avoided [3]. So a flicker-free OCC transmitter has to blink at frequencies that exceed the camera's frame rate, and the receiver has to undersample the transmitted signals. In addition, the transmitters and the receivers are not strictly synchronized, and it is difficult to know the phase difference between the transmitted signal and the camera receiver, so the received on-off keying (OOK) waveform slowly slips with respect to the sampling point [4]. The phase slipping problem can cause more error bits and degenerate the system performance. For these reasons, demodulation of OCC is more challenging than that of non-imaging VLC systems. Several modulation techniques have been proposed for OCC in recent years [5]–[9].

Undersampled frequency shift on-off keying (UFSOOK) [6] uses a pair of discrete OOK frequencies to transmit logic ones and zeros respectively. Different symbols present different patterns to the camera. The demodulator uses two image frames to decode one-bit information. Because of this, the bit rate could not exceed half of the camera sample rate. To be more specific, if UFSOOK is applied to a 30 fps camera receiver, the data rate was limited to 15 bits per second (bps).

The authors in [7] and [8] introduced pulse amplitude modulation (PAM) and quadrature amplitude modulation (QAM) into OCC. Image sensors are not linear devices. The operation of encoding and decoding luminance values, which is known as gamma correction, is nonlinear [10]. As more than two amplitude levels are used in [7] and [8], the nonlinearity introduced by gamma correction had to be taken into consideration. Received images need to be compensated before demodulation in order to mitigate the non-linear effect. A special frame head sequence was introduced to detect the camera sample phase and obtain the gamma curve.

Undersampled phase shift on-off keying (UPSOOK) [9] is a dual-LED modulation technique that can reach a higher transmission speed. The modulation relies on different combinations of the ON/OFF status of two LEDs. Thus, the

demodulator is required to know the exact sample phase of the camera. To do so, the authors designed a special frame head which is examined before every frame is demodulated. If an incorrect sample phase is detected, all sampled values in the same data frame have to be inverted.

OCC is sensitive to ambient light. Sunlight or other background noise can degrade the system performance. In addition, a disturbing problem that can increase the system bit-error rate (BER) is that the transmitters and receivers are at asynchronous frequencies. To the best of our knowledge, only a small number of error detection techniques have been proposed for OCC. The authors in [4] proposed a space-time forward error correction scheme based on USFOOK when dimming control was required. Multiple-phase sampling was employed to detect and correct the erroneous sample phase. This requires the transmitter to repeat the same data frame three times, either spatially or temporally, which will reduce the communication efficiency.

In this paper, a novel modulation scheme undersampled differential phase shift on-off keying (UDPSOOK) is proposed to overcome the phase uncertainty problem and increase the data rate. The UDPSOOK demodulator is not required to know the sampling phase of the camera. Furthermore, a new error detection mechanism is proposed to help reduce the error bits caused by phase slipping. In addition, the experimental setup and results are introduced in Section V.

II. MODULATION/DEMODULATION

To prevent human eyes from photobiological hazard, OCC systems are required to exhibit no flicker to users with different dimming requirements. The ideal blinking frequency of an OCC transmitter is between 90 Hz and 1,000 Hz. Assuming the frame rate of a commercial camera is f_s and the frequency of the OOK square wave carrier is f_c , we can always find an integer n for UDPSOOK to ensure

$$f_c = n \times f_s, 90Hz < f_c < 1000Hz. \quad (1)$$

The transmitted UDPSOOK signal $s(t, \theta)$ can be expressed as

$$s(t, \theta) = \text{sgn}[\sin(f_c t + \theta)] \quad (2)$$

where f_c is chosen by (1), θ is the phase of the OOK carrier, and sign function is defined as follows:

$$\text{sgn}(x) = \begin{cases} 1 & x \geq 0 \\ 0 & x < 0 \end{cases} \quad (3)$$

Every $1/f_s$ seconds the modulator changes the value of θ depending on the binary bit to be transmitted. A bit “1” is transmitted by adding 180° phase shift to the current signal, while a “0” is transmitted by adding 0° to θ . In other words, one bit of information is represented by a change of phase between two consecutive frames.

Figure 1 illustrates the modulated waveform of binary sequence “110”. In the figure, we assume f_s is the camera sample rate and $n = 4$ so that $f_c = 4f_s$. Every frame consists of 4 cycles of the OOK carrier. Dashed lines represent $1/f_s$

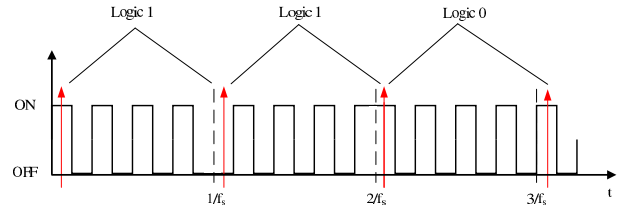


Fig. 1. Modulated UDPSOOK symbols.

seconds interval. The phase of the square waveform has been toggled twice in the first two $1/f_s$ seconds in order to transmit two logic ones. Similarly, the phase stays unchanged for the last frame to send a logic zero.

The red lines represent the sampling moments of the receiver. At the demodulator, received bits are determined by comparing the phase between two consecutive samples. The demodulation rule can be simply expressed as

$$\theta_k - \theta_{k-1} = \theta_\Delta = \begin{cases} 0 & \text{“0”} \\ \pi & \text{“1”} \end{cases} \quad (4)$$

where θ_k is the carrier phase of the k th sampling. This rule can be implemented by using an exclusive OR operation as

$$b_{k-1} = s_k \oplus s_{k-1} \quad (5)$$

where s_k is the k th sampled value of the camera. We map s_k to “1” when the LED is on and s_k to “0” when the LED is off. The structure of the demodulator can be simplified as shown in Fig. 2.

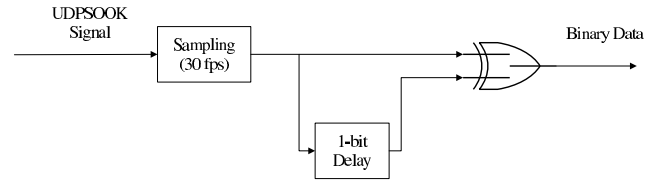


Fig. 2. UDPSOOK demodulation.

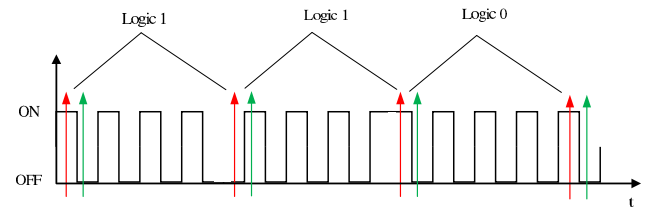


Fig. 3. Different sampling timing for UDPSOOK.

UDPSOOK transmits signals by controlling the phase difference of two consecutive samples, so that n camera frames carry $n - 1$ bits information. The theoretical maximum data rate R_{max} can be obtained by

$$R_{max} = f_s \times \lim_{n \rightarrow \infty} \frac{n-1}{n} = f_s \quad (6)$$

which has been doubled compared to the maximum achieved data rate in [6].

On the other hand, in a practical OCC system, it is difficult to predict the sampling phase of a camera as the sampling can occur at any position regarding the timeline. But UDPSOOK does not need to know the relationship between the camera sampling points and the received signal waveforms since the demodulation is solely based on the phase difference between two frames. Fig. 3 illustrates how UDPSOOK is immune from the camera phase uncertainty. In the figure, the time difference between two consecutive arrows with the same colour is $1/f_s$. Different colour indicates different sampling phase. In Fig. 3, red arrows indicate one set of possible samples for the bit sequence “110”. If the sampling takes place at the green positions, which have a π phase shift from the red arrows, the sampled values will be fully inverted. However, the UDPSOOK demodulator obtains the same bit sequence “110” from the green samples because the phase difference between two consecutive frames does not change.

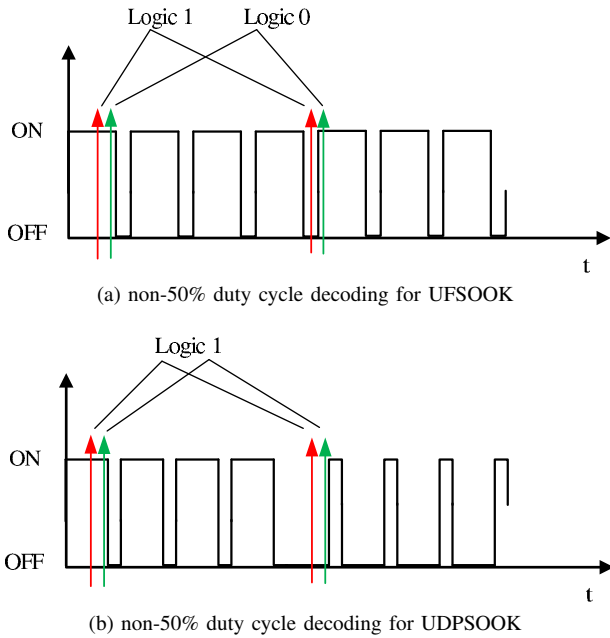


Fig. 4. Non-50% duty cycle demodulation

UDPSOOK also supports dimming control. The LED brightness can be changed by increasing or decreasing the duty cycle of the OOK signal. A fixed 50% duty cycle is not practicable in reality. Assuming a logic one is transmitted by UFSOOK (Fig. 4a) and UDPSOOK (Fig. 4b) respectively, it is shown that UFSOOK is more likely to have an erroneous sampling result (green arrows) when the duty cycle is greater than 50%, but UDPSOOK can adapt to any different duty cycle.

Another problem introduced by image sensors is phase slipping. For a typical OCC system, as the receiver and the transmitter are not strictly synchronized, the sampling points are gradually slipping regarding the OOK waveforms. A sampling phase error occurs when a π phase shift comes. In our experiment, phase slipping is a major source of error bits, so we propose an error detection technique for UDPSOOK

to reduce the system BER. In this proposed system, two LEDs are employed. We use one LED to accomplish data transmission and an extra LED to carry out error detection. The data transmission LED is a UDPSOOK transmitter, and the error detection LED keeps sending bit “0” during the data transmission. As a “0” UDPSOOK bit sequence triggers no phase toggling on the LED, the demodulator expects to see no phase difference on received image samples. Since this LED suffers from the same channel noise and phase slipping problem, if any sampling error occurs, it can precisely indicate the incorrect samples by looking for a sudden phase change. Then the demodulator corrects the sampling errors by simply flipping the erroneous sampled values.

As shown in Fig. 5, the red arrows indicate a correct sampled sequence [ON, OFF], which is decoded as a bit “1”. When a phase error occurs, the second red sampling point slips to the green arrow position and gives rise to an incorrect sampled sequence [ON, ON], which will be decoded as a bit “0”. This error can be observed by the receiver due to the phase change of the error detection LED. The demodulator will invert the second sampled value to get the correct decoded bit.

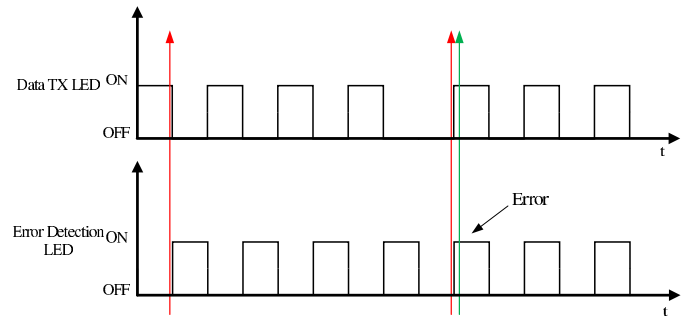


Fig. 5. UDPSOOKED sampling.

III. FRAMING STRUCTURE

In order to detect the start of a transmission, the UDPSOOK data is preceded by a start frame delimiter (SFD). An extra bit is added to the end of the payload for parity check to further enhance the system reliability. A data frame is shown in Fig. 6.

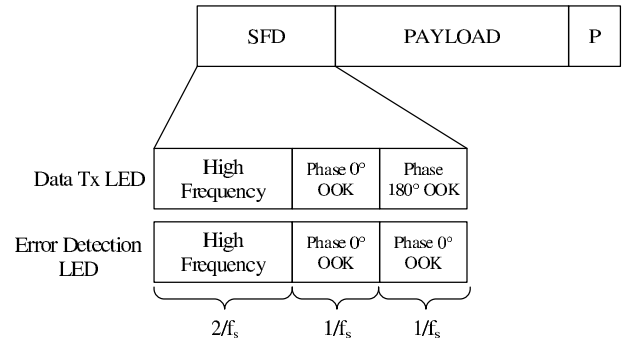


Fig. 6. Frame structure of the proposed OCC system.

An SFD consists of two parts. The first part is a high-frequency OOK symbol that lasts for two frames. This high frequency is required to be greater than the cutoff frequency of the receiver so that this status can be recognized neither as fully ON nor as fully OFF. Instead, the camera extracts the average intensity [6] and interprets this status as half ON assuming a 50% duty cycle is used.

The second part of SFD for a data transmission LED is a UDPSOOK bit “1” (Fig. 6). If a logic “1” is not observed during the decoding of an SFD, the data frame might have been corrupted and should be discarded. The error detection LED has a different second part of SFD. After the first $2/f_s$ seconds, it starts to transmit a bit “0”, i.e. two frames of OOK signals which have identical phase. In this way, an SFD not only starts a frame but also helps the receiver distinguish between the two different functional LEDs. If a receiver observes a logic “0” after the $2/f_s$ seconds half ON, it will recognize this LED as an error detection transmitter.

Following the SFD is the payload of the data frame. The data frame ends when the receiver detects another SFD. The last bit of a data frame is a parity bit used to detect the possible transmission errors. The receiver calculates the number of “1”s when a full data frame is received. When parity check fails, all the data in the current frame will be discarded.

IV. EXPERIMENTAL SETUP

The modulation algorithm is implemented on a Xilinx Virtex-7 FPGA. A finite state machine (FSM) is shown in Fig. 7 to describe the transmission process. When transmission starts, the modulator first sends a high frequency signal as part of the SFD. Followed is a UDPSOOK bit “1”, i.e. two frames of OOK with π phase difference. The modulator then changes the phase of the carrier every $1/f_s$ seconds according to the next input bit. At the end of the transmission, a parity bit will be calculated and added to the end of the frame. This modulation FSM is implemented in Verilog hardware description language (HDL). Xilinx Vivado Design Suite performs register-transfer level (RTL) synthesis and timing analysis etc., and the in-built simulator provides reliable behavioral verification before testing on hardware. The simulation result is shown in Fig. 8. An *enRead* pulse reads one bit from the memory and *LED_En* enables the I/O ports on and off according to the modulation rules. Note that the time scale has been shrunk by 1000 times to improve simulation efficiency and the figure only demonstrates the initial 300 us after reset.

An LED driver circuit can supply sufficient power to match the electrical characteristics of the LEDs. We select the Digilent PmodLED LED module as our solution for transmitters. The PmodLED LED module integrates four high-bright monochrome red LEDs with the necessary driver circuits. Those low power consumption LEDs can be driven by less than 1 mA current.

At the receiver, videos are recorded by a Logitech Pro 900 camera. The camera is then connected to a PC where captured images are processed via MATLAB. Demodulation is performed off-line after frames being captured. It starts with

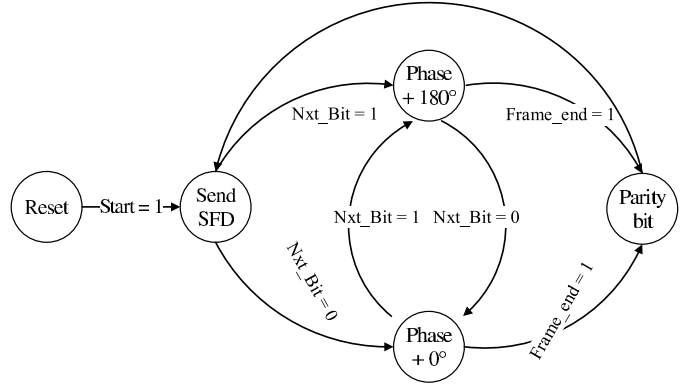


Fig. 7. The transmission control finite state machine.

monitoring the first SFD, which indicates the beginning of a new data frame. After an SFD is found, the demodulator begins to compare two consecutive samples to determine the transmitted bit. This process repeats until the next SFD is detected. We have to check the parity bit before proceeding to the next data frame. For UDPSOOKED, assuming the decoded bit sequences on two LEDs are respectively $\{R_{d0}, R_{d1}, R_{d2}, \dots, R_{dk}\}$ and $\{R_{e0}, R_{e1}, R_{e2}, \dots, R_{ek}\}$, the final decoded sequence is given by

$$B_k = R_{dk} \oplus R_{ek}. \quad (7)$$

V. EXPERIMENTAL RESULTS

A. Received Optical Power

As the LED electrical power consumption is only on the order of mW, one of our central concerns is how much optical power has reached the camera. Fig. 9 shows the experimental setup used to measure the optical power at the receiver. In the figure, d is the transmission distance and f is the focal length of the one-inch-diameter lens. We employ a high-speed photodetector (Thorlabs DET36A) for the measurement. The voltage difference across the load resistor R_L is directly measured in the experiment. We select a 10 M Ω resistor since a low generated photocurrent can be expected. Table I gives the voltage results over three different transmission distances.

TABLE I
RECEIVED OPTICAL INTENSITY FOR THE PROPOSED OCC SYSTEM

Distance	Voltage	Current	Incident power	Intensity
15 cm	2.36 V	2.36 μ A	7.15 μ W	1.41 μ W/cm ²
50 cm	220 mV	22 nA	66.67 nW	13.16 nW/cm ²
100 cm	60.8 mV	6.08 nA	18.42 nW	3.64 nW/cm ²

The responsivity curves of the selected photodetector can be obtained from the product specification [11]. The PmodLED module only emits red light (wavelength in the vicinity of 650 nm), and accordingly, we select a responsivity of $R = 0.33A/W$. As the responsivity of a photodiode is defined as a ratio of the photocurrent to the incident light power at a given wavelength, to calculate the received optical power, we use

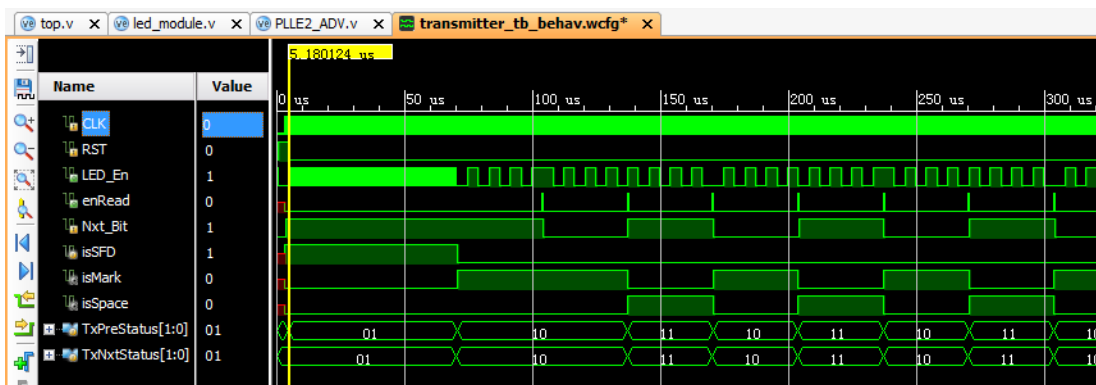


Fig. 8. The simulation results in Xilinx Vivado simulator.

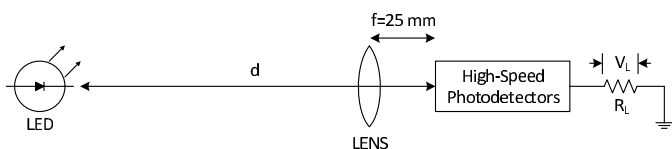


Fig. 9. Optical power measurement setup.

$$P_{inc} = \frac{I_{PD}}{R} \quad (8)$$

where P_{inc} is the incident power and I_{PD} is the photocurrent, which can be calculated from

$$I_{PD} = \frac{V_L}{R_L} \quad (9)$$

where V_L is the voltage across the load resistor R_L . The result is also shown in Table I. As expected, the received power dramatically drops when we increase the transmission distance.

Using the area of a one-inch-diameter lens as $\pi \times (25.4\text{mm}/2)^2$, the signal intensity at the receiver can be estimated. Over the distance of 1 meter we have signal intensity of

$$Int_{d=1m} = \frac{(P_{inc})_{d=1m}}{A} = \frac{18.42 \text{ nW}}{\pi \times (25.4\text{mm}/2)^2} \approx 3.64 \text{ nW/cm}^2. \quad (10)$$

Similarly, we can calculate the signal intensity for 15 cm and 50 cm, which is shown in Table I. Experiment shows that the ambient intensity is on the order of 0.1 nW/cm^2 , so we have approximately 10 dB of dynamic range.

B. BER and Bit Rate

The modulator has been implemented on a Xilinx VC707 Evaluation board. We use a logic analyzer to verify the modulated signals. The captured waveforms are shown in Fig. 10. The blue waveform represents the data transmission channel and the yellow waveform represents the error detection channel. In the figure, a new data frame starts at 296 ms with a 66 ms 12 kHz high frequency. A bit "1" has been transmitted

between 362 ms and 429 ms on the blue channel as part of the SFD, which is followed by UDPSOOK payloads. As we can see from the figure, there is no phase change on the error detection channel.

Then we use the modulated electrical signals to drive the LED circuits. Digilent PmodLED offers high-brightness LEDs with low power requirements. In our experiment, for each LED the electrical power consumption is $3.30\text{V} \times 2.45\text{mA} = 8.10\text{mW}$.

At the receiver, videos have been recorded. The camera has been set up in a normal indoor environment with noise from sunlight outside the room. We set the frame rate as 30 fps and all collected images are processed by MATLAB. In the experiment, auto white balance and other optimization options have been disabled. With proper configurations, the influence of ambient light can be reduced, so that the camera can identify the transmitted image with lower error rate. Key experimental parameters are shown in Table II. We collect approximate 20,000 frames for each measurement.

TABLE II
KEY EXPERIMENTAL PARAMETERS

Parameter	Value
Camera frame rate	30 fps
Resolution	640×480
Saturation	0
LED DC offset	1.65 V
LED peak-to-peak voltage	3.3 V

We have tested three different communication distances for both UDPSOOK and UDPSOOKED. The BER results are shown in Table III. It is suggested that UDPSOOK provides acceptable BER performance under all three distances considered, and UDPSOOKED can lower the BER efficiently, especially for the distances of 15 cm and 50 cm. The result also shows that when transmission distance increases, the system BER increases.

We have also implemented UFSOOK in the same experimental environment. The data rate comparison is shown in Ta-

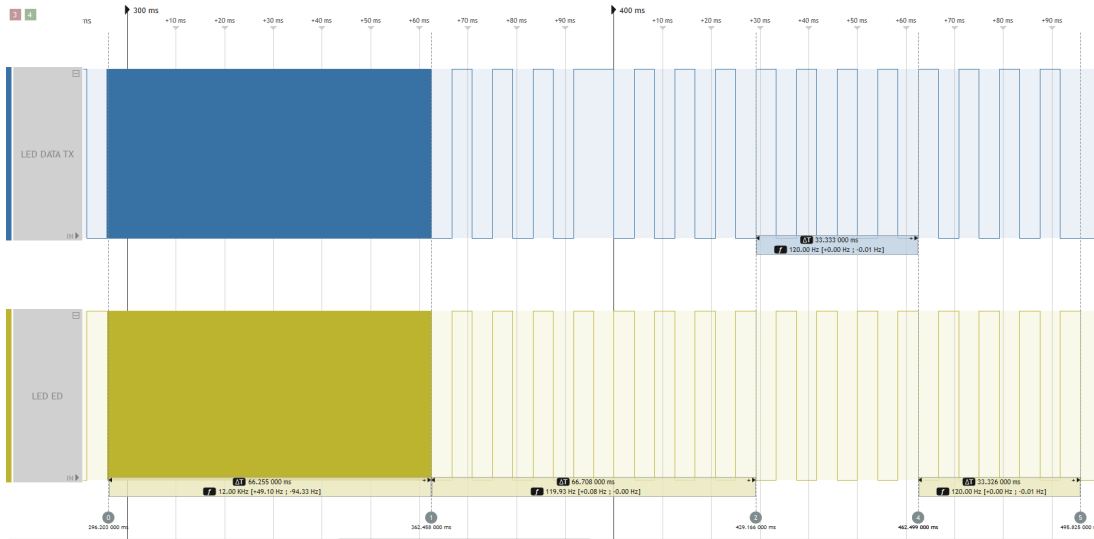


Fig. 10. Captured waveforms from the logic analyzer.

TABLE III
EXPERIMENTAL RESULTS I

Distance	Modulation	BER
15 cm	UDPSOOK	2.48×10^{-4}
15 cm	UDPSOOKED	4.96×10^{-5}
50 cm	UDPSOOK	4.25×10^{-4}
50 cm	UDPSOOKED	6.08×10^{-5}
1 m	UDPSOOK	8.15×10^{-3}
1 m	UDPSOOKED	1.88×10^{-3}

ble IV. The experimental results demonstrate that UDPSOOK has indeed doubled the data rate of UFSOOK as expected.

TABLE IV
EXPERIMENTAL RESULTS II

Distance	Modulation	Data Rate (bps)
15 cm	UFSOOK	11.06
15 cm	UDPSOOK	23.02

VI. CONCLUSION

In this paper, we have proposed a novel non-flicker modulation technique called UDPSOOK for OCC. We have also designed an error detection scheme for UDPSOOK, using a second LED as a detector of phase slipping errors. This method mitigates the asynchronization problem of OCC that other researchers are concerned with. An experimental communication link has been established by using monochrome LEDs and an inexpensive commercial camera. Experiments have demonstrated that a BER of 10^{-5} has been achieved with low overheads. Experimental work shows that UDPSOOKED can provide excellent robustness and reliability for OCC systems.

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