Real-Time Hardware-in-the-Loop Simulation and Control of Totem Pole PFC Converter

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***Abstract*— High efficiency totem pole power factor correction (PFC) converters have attracted a significant attention in recent years. State of the art wide band gap (WBG) devices make continuous conduction mode (CCM) totem pole PFC feasible for medium to high power applications. However, higher costs and complex control are the main barriers to widespread industrial adoption of this topology. Control challenges including current spikes during zero crossings, DC component in AC mains current and AC voltage drop handling are investigated in this paper. Appropriate control measures are utilized to address these challenges. Additionally an accurate low cost DC current reduction method is proposed. The effectiveness of the proposed control is verified through real-time hardware-in-the-loop simulation of a 1450 W interleaved totem pole PFC converter.**

Keywords—Real-Time, Hardware-in-the-Loop, Simulation, Control, AC-DC Power Conversion, Power Factor Correction, Totem Pole

I. Introduction

Wide band gap (WBG) based totem pole power factor correction (PFC) converters operating in continuous conduction mode (CCM) demonstrate promising efficiency and power density improvements in medium to high power applications. Relatively low levels of electromagnetic interference (EMI) make the totem pole structure stand out among bridgeless PFC topologies. However, higher costs and requirements for advanced control are limiting factors for industrial use.

Control challenges such as spikes during voltage zero crossings, DC component in the AC mains current, and susceptibility to sudden AC voltage drops are inherent to bridgeless totem pole PFC structure shown in Fig.1. In this section, these control challenges are described.

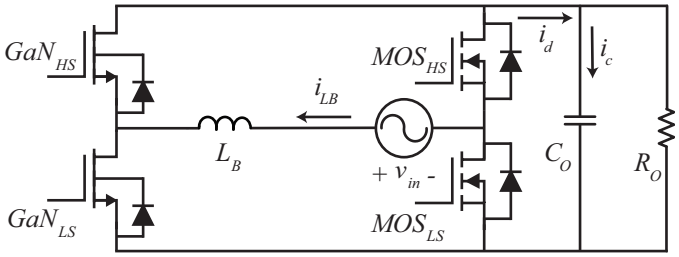

Fig. 1 Totem pole bridgeless PFC with synchronous rectification

A. Current Spikes During Zero Crossings

In Fig.1, MOS_{HS} remains on during the negative half cycle and MOS_{LS} blocks the DC voltage. At the same time GaN_{HS} operates as a boost switch and GaN_{LS} acts as synchronous rectifier. In the positive half cycle however, MOS_{HS} and GaN_{HS} change roles with MOS_{LS} and GaN_{LS}, respectively. During the transition from negative to positive half cycle as shown in Fig.2, the input voltage amplitude is very small and the output capacitor of the lower synchronous FET is not yet discharged. During zero crossing the duty cycle of GaN_{LS} suddenly jumps from near zero close to one. As a result, the output capacitance of MOS_{LS} is suddenly discharged which in turn creates inductive current spikes and generates additional common mode (CM) noise [1], [2].

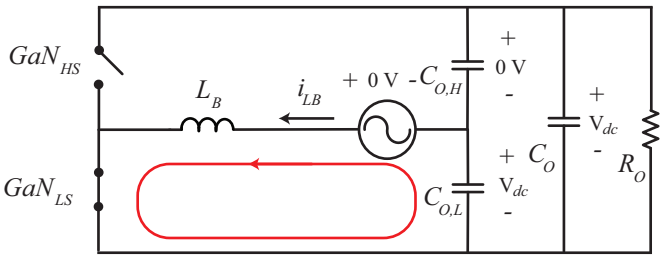

Fig. 2 Totem pole PFC equivalent circuit immediately after negative to positive zero crossing when GaN_{LS} has a duty cycle close to one

B. DC Component in the AC Mains Current

Unlike conventional boost PFC, two different circuits are used in a totem pole structure for shaping the input current. Therefore asymmetries in sensing and manufacturing tolerances may result in noticeable DC component in the AC mains current. [3]-[5]. The cumulative effect of DC current from multiple power converters, for instance in server farm or EV fleet applications, can potentially lead to saturation of distribution transformers [6]. This issue has been recently investigated for transformer-less grid connected distributed energy resources (DERs). IEEE standard 1574-2003 [7] and Italian standard CEI 0-21 [8] place a limit on the DC current at AC mains of DERs to 0.5% of the full rated device current. To detect and compensate the DC current, the use of magnetic elements has been proposed, such as a 1:1 transformer, a mutual inductor or a sensing reactor to decouple the bulk AC component of current

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from the DC component [6], [9]-[14] However, suitable magnetic elements are heavy and bulky and often do not provide the desired accuracy. Detecting the DC current by passing the switching voltage through a low pass filter was proposed in [15], [16]. However, filtering the line frequency component results in significant attenuation of the DC component. Calibration of current sensors during the zero-current period was proposed in [17], [18]. However, this method limits the maximum pulse width. Extracting DC component of AC mains current from the DC link voltage or current was investigated in [19], [20] but complex control and insufficient accuracy are limiting factors.

C. AC Voltage Drop Issue

When the input voltage of a totem pole PFC suddenly drops due to load switching or faults in the grid, the controller is not able to detect the issue instantly. During the time between the voltage drop and detection of a reduction in voltage, which depends on the method of root mean square (RMS) value calculation for the input voltage, the synchronous high frequency GaN switch discharges the output capacitance. This in turn results in large currents in reverse direction.

With recent advances in real-time simulation tools, control challenges can be identified and addressed before the actual prototype is built, reducing time to market. In this paper, Typhoon HIL real-time simulator is used to verify effective measures to address totem pole PFC converter control issues illustrated in the introduction. Section II of this paper elaborates the implementation details of these control measures. Additionally, an accurate, low cost DC current detection and reduction method is proposed in this section. In section III, real-time hardware-in-the-loop (HIL) simulation results are presented to verify the effectiveness of the proposed control. The conclusion forms the final section of the paper.

II. PROPOSED CONTROL FOR TOTEM POLE PFC CONVETRER

The proposed control is based on a multi-thread software structure where time critical tasks are performed in a fast interrupt service routine, repeated every switching cycle. Other tasks are placed into slower control loops. Table I outlines the structure of the proposed control software.

TABLE I. OUTLINE OF THE PROPOSED CONTROL STRUCTURE

Software execution rate	Control functions
Every switching cycle	• Reading ADC channels • Fault handling • Current loop control • PWM pattern update
Every 10 switching cycles	• Input voltage RMS calculation • Converter operation state update • Voltage loop control
Every line cycle	• DC current detection/reduction

The first task in the fastest control routine is reading the sampled value of inductor current as well as input and output voltages. For better accuracy and to eliminate the effect of sampling inconsistencies, signals are sampled eight and two times within every switching cycle for currents and voltages, respectively. The average of these samples are used for control tasks. Next, the converter is monitored for any potential fault. Fig.3 shows the state machine used for monitoring faults. In addition to over voltage, over current and AC voltage brownout protections, the unique totem pole structure requires AC voltage drop protection. An AC voltage drop is detected when the current suddenly drops and the input voltage and current have opposite signs [21]. During this period, the output capacitor is being discharged. When an AC voltage drop is detected, all switching is stopped until the next zero crossing of input voltage. The converter is only allowed to resume operation if the input current has a very small value.

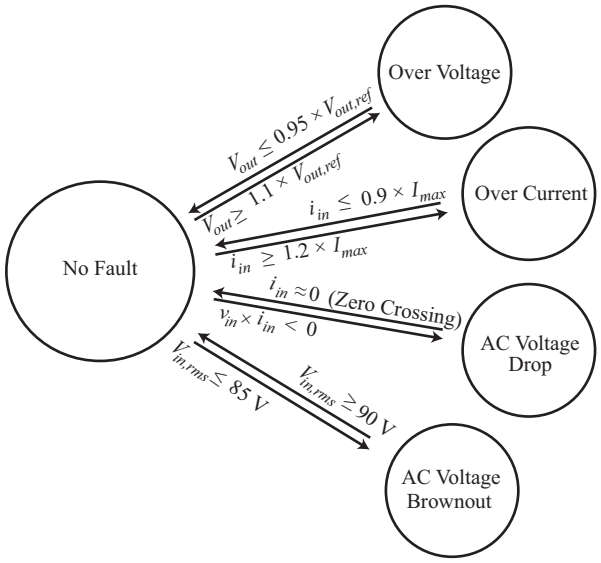

Fig. 3 Fault handling state machine

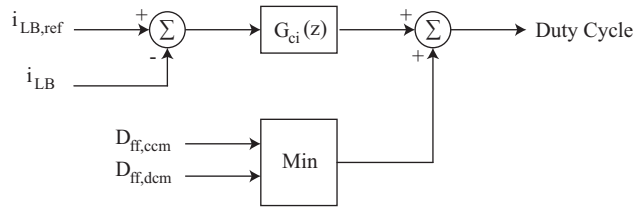

Fig. 4 Current Control loop for digitally controlled totem pole PFC

One of the main objectives of a PFC converter is to regulate input current and minimize its harmonic content. Often up to the 40th harmonic (2.4 kHz in a 60 Hz system) of current needs to be attenuated. Therefore, the bandwidth of the current control loop is usually set to 6-10 kHz. However, due to the delay in a digitally controlled system, a phase drop occurs at higher frequencies in the Bode plot of the transfer function of the boost converter. Therefore, achieving sufficiently high bandwidth for the current controller is challenging. Fig. 4 shows the implemented current control loop. In this implementation a duty ratio feed-forward branch is added to the output of current compensator based on the design in [22]. In order to achieve the desired performance in continuous conduction mode (CCM) as well as discontinuous conduction mode (DCM), a duty feed-forward value is calculated separately for these two modes and the minimum value is utilized in every switching cycle [23].

$$D_{ff,ccm} = 1 - \frac{v_{in}}{V_{out}} \tag{1}$$

$$D_{ff,dcm} = \sqrt{\frac{2G_eL}{T_{sw}}\left(1 - \frac{v_{in}}{V_{out}}\right)} \quad (2)$$

The duty ratio feedforward for CCM and DCM modes is defined in (1) and (2), respectively. In the latter, G_e is the equivalent conductance of the PFC unit in Siemens, L is the boost inductor value and T_{sw} is the switching period. Fig. 5 shows a typical transition between the CCM and DCM duty feed-forward calculations. As a result of these smooth transitions during a line cycle, current distortions are minimized in the inductor.

In order to prevent large current spikes during zero crossings, the PWM pattern state machine shown in Fig. 6 was implemented. During the positive half cycle, GaN_{LS} acts a boost FET and is controlled with duty cycle (D), determined by the current control loop. GaN_{HS} on the other hand, operates as a synchronous FET and is switched in a complementary manner to GaN_{LS}. During positive to negative zero crossing, the roles of these two devices are swapped. First, switching is inhibited for five cycles to account for any zero crossing detection errors. Next, in order to prevent large current spikes, the duty cycle of GaN_{HS} is gradually increased from zero to the value determined by the current control loop. At the end of this process, the output capacitance of MOS_{HS} is discharged and the FET is turned on. A similar process is employed for the negative to positive half cycle transition.

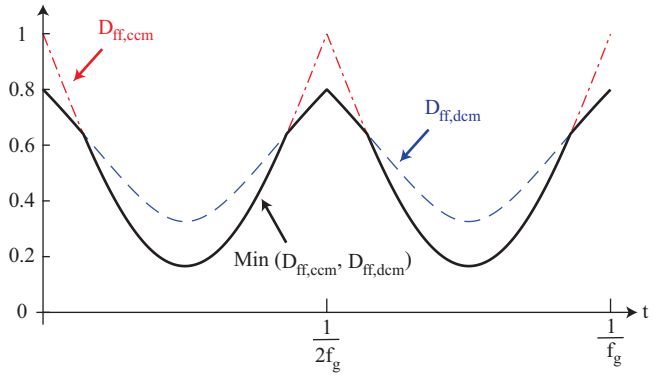

Fig. 5 Illustration of a typical transition between CCM and DCM duty ratio feedforward calculations

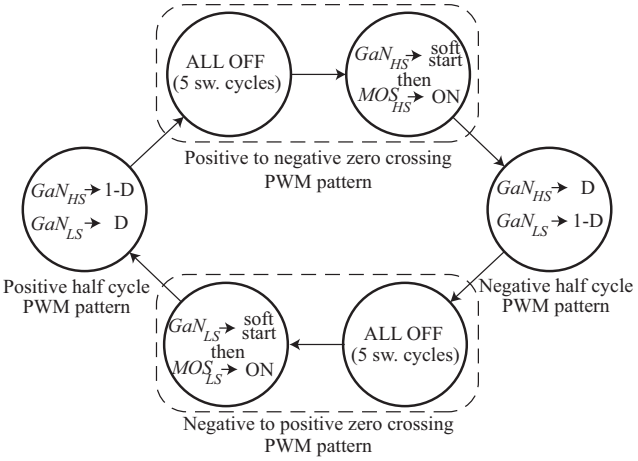

Fig. 6 PWM pattern state machine to implement zero crossing soft start

Fig.7 shows the converter operation state machine implemented in the slower control routine which is performed every 10 switching cycles. In the idle state, the software calculates the RMS value of the input voltage to verify that this value is between 90 V and 260 V. If the input voltage is within the specified range, the converter enters the "AC voltage in range" state. In this state, the output capacitors are being charged through an inrush current limiter. When they are sufficiently charged and the output voltage reaches to a predetermined value between 35 % to 40 % above the input voltage RMS value, the inrush limiter is bypassed through a relay and the reference setting for output voltage is gradually increased from the current output voltage level to the desired output voltage (390 V or 400 V). In this state, the input current is regulated and the output voltage is increased in a controlled manner. Once the output voltage level reaches the desired value, the PFC unit can start operating in the normal mode and the desired load can be applied at the output terminals.

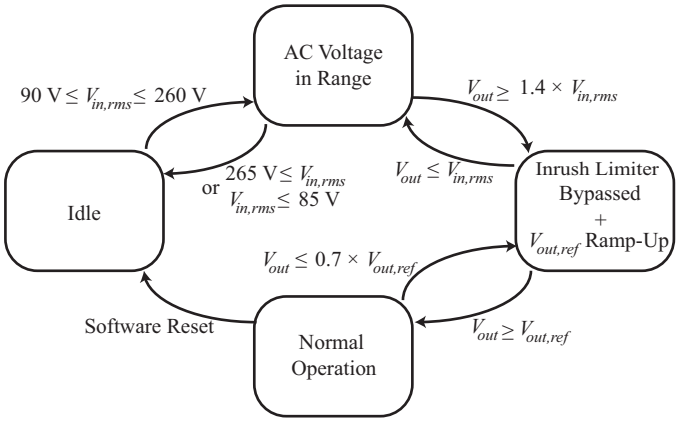

Fig. 7 Converter Operation state machine

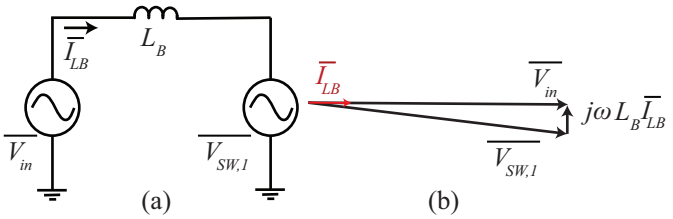

Fig. 8 Phasor relationship between PFC's input voltage and inductor current

DC current detection and reduction is performed in the slowest control routine, which is executed every line cycle, to reduce the risk of interference between control loops. In a boost derived PFC converter, the boost inductor (L_B) is relatively small resulting in a small voltage drop at the line frequency (ω). As a result, the first harmonic of the switch node voltage is approximately equal to the grid voltage as shown in Fig. 8.

$$\overline{V_{sw,1}} = \overline{V_{in}} - L_B j\omega \overline{I_{LB}} \simeq \overline{V_{in}} \quad (3)$$

$$v_{in}(t) = V_p \sin(\omega t) \quad (4)$$

V_p is the peak of the sinusoidal input voltage which is the reference phasor. By defining the switching function $s(t)$ as

$$s(t) = M \sin(\omega t) \quad (5)$$

Where the modulation index, M, is defined as

$$M = \frac{V_p}{V_{dc}} \tag{6}$$

We can derive the expression for the first harmonic of the switch node voltage in (7). V_{dc} represents the DC link voltage.

$$v_{sw,1}(t) = V_{dc}s(t) = MV_{dc}\sin(\omega t) \tag{7}$$

In a PFC converter, the input current is ideally a sinusoidal current in phase with the input voltage. However, a DC component can be present in the boost inductor current in totem pole structures due to inductor current sensing inconsistencies in the positive and negative half cycles.

$$i_{LB}(t) = I_p\sin(\omega t) + I_{dc} \tag{8}$$

I_p is the peak of the first harmonic of the inductor current. The inductor current flows to the DC side during the periods when the boost switch is turned off. As a result, the expression for the first harmonic approximation of the current flowing to the DC side is derived.

$$i_d(t) = i_{LB}(t)s(t) \tag{9}$$

$$i_d(t) = \frac{I_pM}{2} + \frac{I_pM}{2}\sin\left(2\omega t + \frac{3\pi}{2}\right) + I_{dc}M\sin(\omega t) \tag{10}$$

Only the alternating component of i_d flows to the output capacitor (C_o). As a result, the alternating voltage component of C_o is

$$v_{co}(t) = \frac{I_pM}{4C_o\omega}\sin(2\omega t + \pi) + \frac{I_{dc}M}{C_o\omega}\sin(\omega t - \frac{\pi}{2}) \tag{11}$$

It can be seen in (11) that the amplitude of line frequency ripple on the DC link voltage is an indicator of the DC component of input current.

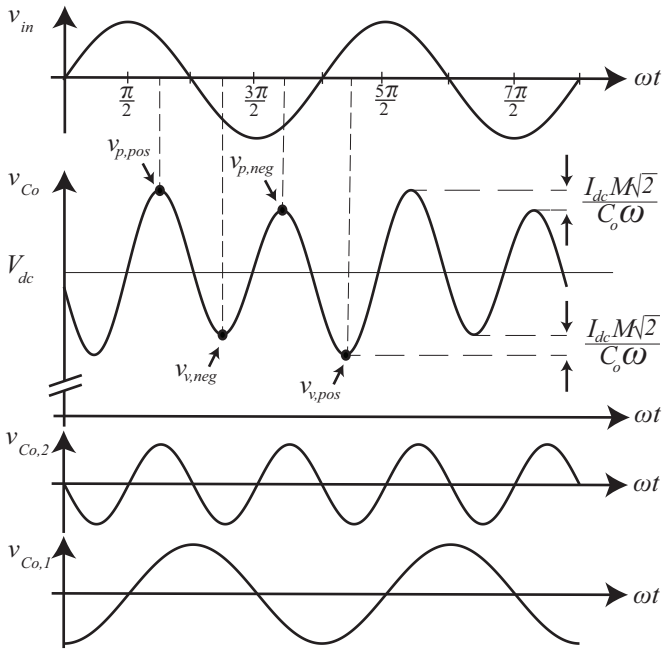

Fig. 9 Phase relationship between input voltage, first and second harmonic of DC link voltage

Fig.9 shows the phase relationship between the input voltage, first harmonic (v_{co1}) and second harmonic (v_{co2}) of DC link voltage when there is a positive DC component in input current. The first harmonic of the DC link voltage is lagging the input voltage by π/2. With a positive DC component in input current, the DC link voltage has higher peak points ($v_{p,pos}$) and lower valley points ($v_{v,pos}$) during positive half cycles compared to peak and valley points ($v_{p,neg}$ and $v_{v,neg}$) during negative half cycles.

By sensing on DC link voltage ripple as well as the input voltage and comparing consecutive samples, the local minimum and maximum points are detected and stored during the positive ($v_{p,pos}$ and $v_{v,pos}$) and negative ($v_{p,neg}$ and $v_{v,neg}$) half cycles. These values together with the input voltage information are then used to detect the sign of the DC current as shown in Fig. 10. To detect the sign of a very small DC component in input current, the voltage across the output capacitors is passed through a high pass filter (HPF), implemented in the hardware model in the HIL, before being fed to I_{dc} sign detection block. Capacitors with voltage ratings in the DC link range (400 V) are inexpensive and the choices are abundant. Additionally, the size and weight of an RC high pass filter is negligible compared to the filters in other methods. Therefore using a HPF is a low-cost solution which increases the sampling resolution of the DC link voltage ripple and improves the DC current detection accuracy.

Fig. 11 shows the block diagram of the DC current reduction method. When the sign of the DC component of current is detected, the proposed method is able to reduce the DC component by applying an adaptive bias k (initially set to zero) in the samples of the sensed inductor current, canceling the undesired bias in the sensor.

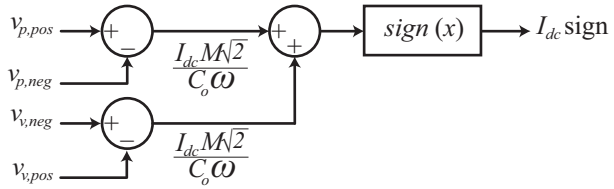

Fig. 10 The proposed DC current sign detection unit block diagram

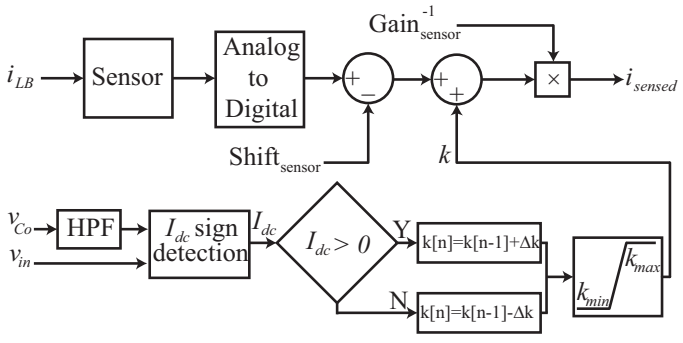

Fig. 11 DC current reduction method block diagram

III. Real-Time Hardware-in-Loop Simulation Results

To verify the effectiveness of the proposed control, a Typhoon HIL real-time simulator, shown in Fig. 12, was used to simulate an interleaved totem pole PFC converter shown in Fig. 13. A three phase inverter block was used to model the three switching legs. The specification of the simulation is listed in Table II.

Fig. 14 shows output voltage soft start-up for low line voltage (115 V_{rms}). The output capacitor starts to charge through the inrush current limiter as soon as the AC source is connected. When it is charged to a predetermined value, the inrush limiter is bypassed and the output voltage is gradually increased toward the reference. The converter enters normal operation mode and full loading (1450 W) is applied after the output voltage reaches 390 V. In this way, excessive start-up current stress is avoided.

TABLE II. SPECIFICATIONS OF REAL-TIME SIMULATED INTERLEAVED TOTEM POLE PFC CONVERTER

Parameter	Value	Parameter	Value
Rated output power (P_o)	1450 W	Inrush current limiter (R_{inrush})	54 Ω
Input voltage (v_{in})	85 ~ 265 V_{rms}	Boost inductors (L_{B1} and L_{B2})	450 µH
Output voltage (v_o)	390 V_{DC}	Output capacitor (C_o)	600 µF
Switching frequency(f_{sw})	2×65 kHz	High-pass filter (C_f and R_f)	320 µF, 10 kΩ

Fig. 12 Typhoon HIL real-time simulator

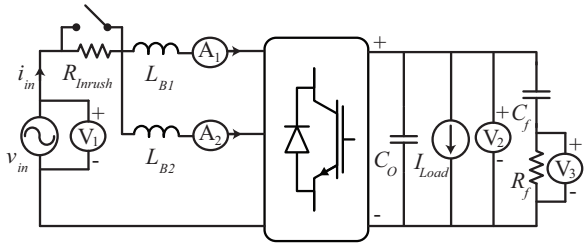

Fig. 13 The real-time simulation model of interleaved totem pole PFC

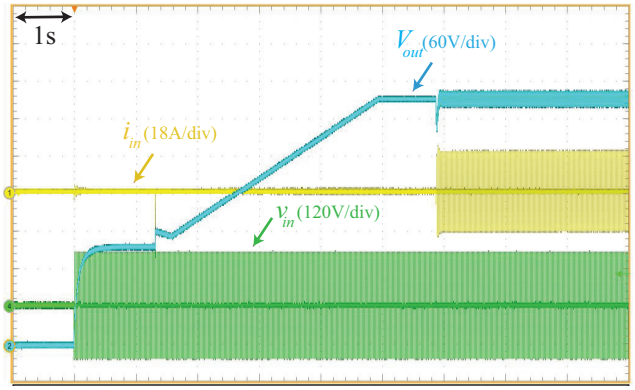

Fig. 14 Output voltage soft start-up for low line voltage (115 V_{rms})

Fig. 15 and 16 show the full load steady state waveforms at low and high line voltages, respectively. In both cases, the current control loop compensator and duty ratio feed forward branch cooperate to regulate the current and reduce the harmonic components. As shown in Fig. 16, a smooth transition occurs between DCM and CCM mode and the current remains under control during this transition.

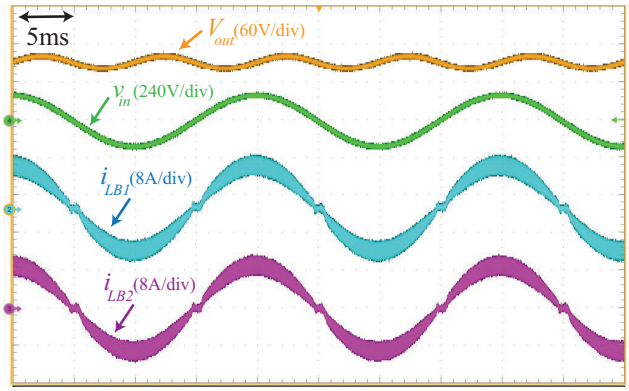

Fig. 15 Low line voltage (115 V_{rms}) full load (1450 W) steady state operation

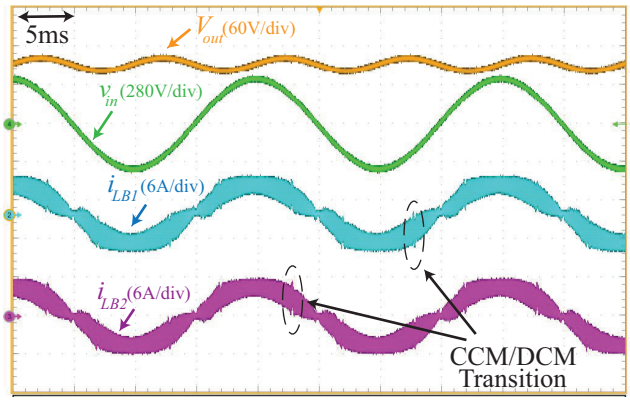

Fig. 16 High line voltage (115 V_{rms}) full load (1450 W) steady state operation

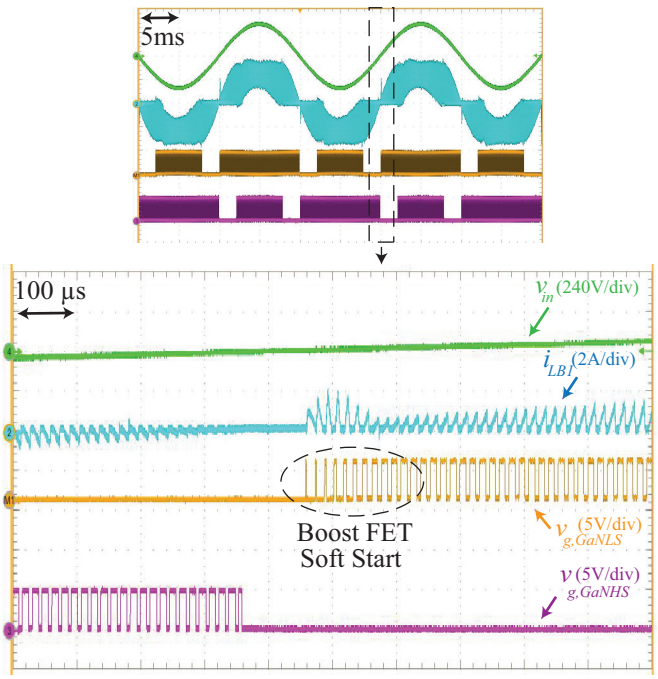

Fig. 17 High line voltage (230 V_{rms}) Boost switch zero crossing soft start

Fig. 17 shows the performance of the negative to positive zero crossing PWM pattern for high line input voltage (230 V_{rms}). In this simulation, an effective 500 pF capacitor is modeled across MOS_{LS}. As can be observed from the waveform, immediately after zero crossing there is a period of no switching which lasts for five switching cycles to account for any potential error in zero crossing detection. Next the low side GaN device goes through a soft start procedure in which the duty cycle of GaN_{LS} is increased gradually. During this period, each time GaN_{LS} is turned on the current in the inductor increases as a fraction of the energy stored in the output capacitance of MOS_{LS} is transferred to the inductor. The energy stored in the inductor is then transferred to the output capacitance of MOS_{HS} when GaN_{LS} is turned off and the current in the inductor decreases back to zero. Without the soft start, the energy transfer would happen in a single step and the peak inductor current would be much larger.

Fig. 18 shows the performance of the AC voltage drop protection when the input voltage suddenly steps from 230 V_{rms} to 115 V_{rms} at the valley of the sinusoidal wave. The current magnitude in both phases drops quickly, and when the voltage and current have opposite signs an AC voltage drop is detected. As a result, all FETs are disabled until the next zero crossing when the converter resumes operation provided that the current is reduced to a small value.

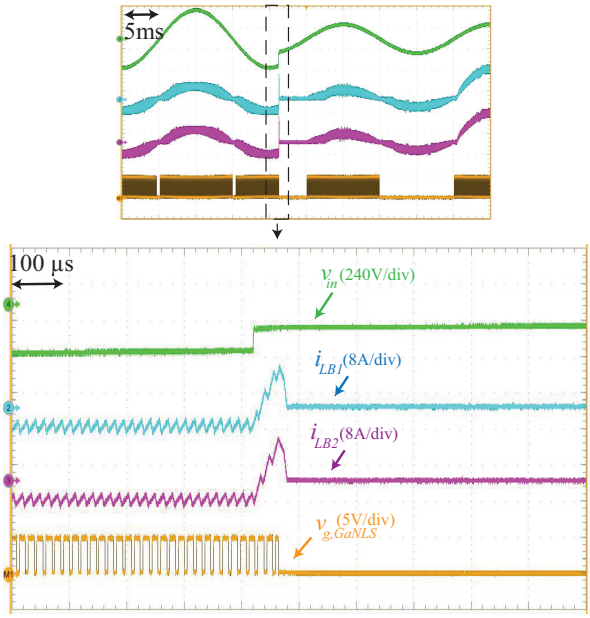

Fig. 18 High (230 V_{rms}) to low (115 V_{rms}) line voltage drop and AC drop protection performance

In order to test the effectiveness of the proposed DC current reduction method. An example of a practical manufacturing tolerance in the output of the current sensors was simulated. In two simulation test scenarios, offsets of +5 mV and -4 mV were intentionally applied in the readings from ADC module to emulate the extreme cases for manufacturing tolerances in Hall-effect sensors like [24]. Fig. 19 and Fig 20 show the full load simulation waveforms at low input voltage in presence of +5 mV offset in the current sensor output without and with the proposed DC current reduction method, respectively. A significant amount of negative DC input current creates a large line frequency ripple on the DC link voltage in Fig. 19. The proposed method effectively detects and reduces the DC component which results in almost zero DC link voltage line frequency ripple in Fig. 20.

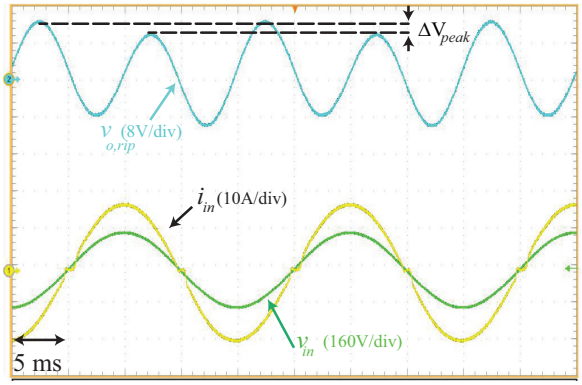

Fig. 19 Waveforms at 1450 W output and 115 Vrms input without the proposed method in presence of +5 mV offset in current measurement

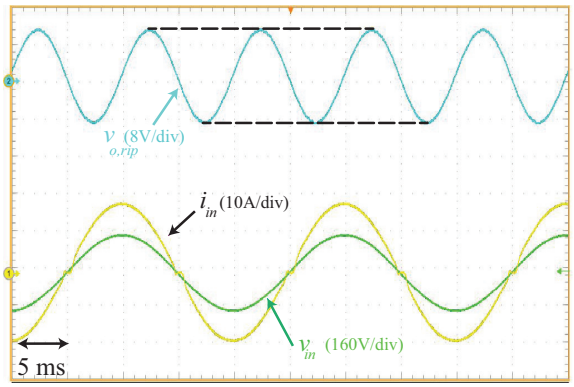

Fig. 20 Waveforms at 1450 W output and 115 Vrms input with the proposed method in presence of +5 mV offset in current measurement

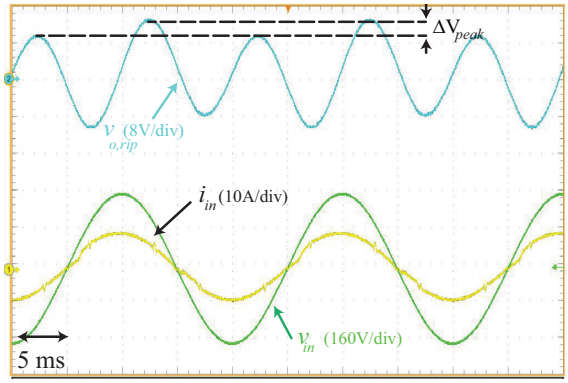

Fig. 21 Waveforms at 1450 W output and 230 Vrms input without the proposed method in presence of -4 mV offset in current measurement

The proposed method also performs well in detection and reduction of positive DC input current at high input voltage and full load as a result of -4 mV of offset in the current sensor's output. The large line frequency ripple in Fig. 21 indicating a

significant amount of positive DC input current is almost fully eliminated in Fig. 22 using the proposed method.

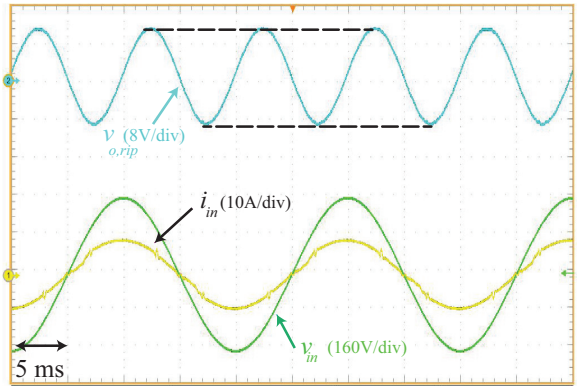

Fig. 22 Waveforms at 1450 W output and 230 Vrms input with the proposed method in presence of -4 mV offset in current measurement

IV. Conclusion

In this paper, control challenges for totem pole PFC converters are investigated. Appropriate control measures are employed to address current spikes during zero crossings and AC voltage drop handling issues. Additionally, a low cost method was proposed for detection and reduction of DC input current was proposed based on time domain analysis of DC link voltage. The proposed control was validated on a 1450 W interleaved totem pole PFC converter through real-time hardware-in-the-loop simulation on Typhoon HIL simulator. The results verify that the proposed control can effectively address the control challenges in totem pole PFC converter.

References

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