Instrumentation and Fabrication Techniques for Semiconductor-Based Quantum Technologies

by

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B.Sc., Sharif University of Technology, 2019

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Applied Science

in

THE FACULTY OF GRADUATE AND POSTDOCTORAL STUDIES
(Electrical and Computer Engineering)

The University of British Columbia
(Vancouver)

February 2022

The following individuals certify that they have read, and recommend to the Faculty of Graduate and Postdoctoral Studies for acceptance, the thesis entitled:

Instrumentation and Fabrication Techniques for Semiconductor-Based Quantum Technologies

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Abstract

Large-scale quantum computers have the potential to perform calculations that are otherwise impossible, a capability that could power exciting advances in fields such as materials design and optimization. Building large-scale quantum computers with spin qubits is appealing because they have long coherence times and can be fabricated on silicon chips using an industrial process amenable to scaling. State-of-the-art spin qubit systems are still small, having only just reached the 2-qubit and 4-qubit scale, and their performance and scalability are not optimized yet. Connecting large numbers of spin qubits on chips remains a challenge. In this thesis we demonstrate a simplified fabrication process using a single layer of gates to realize hole spin qubits, anticipated to be easier to scale up than conventional approaches, based on quantum dots formed in a germanium quantum wells on silicon substrates. We also devised a novel approach to reduce contact resistance to the quantum well. Using this process we successfully built quantum dots, as evidenced by Coulomb blockade spectroscopy. Future work will demonstrate quantum bits using this process.

Optimization of qubits based on quantum devices requires cooling them down below 4 Kelvin and connecting them to microwave control and measurement circuits. Designing a high frequency control and measurement apparatus is challenging since it requires suppression of stray resonances and crosstalk in the setup. Typically each research group designs its own apparatus, or purchases an expensive apparatus that is not possible to customize. In this thesis, we design and test an apparatus for controlling and measuring few-qubit devices using low-frequency and microwave electrical signals, that can be used to optimize qubit devices. Our setup has -40 dB cross-talk with no resonances up to 7 GHz, and has the advantage

of being small in size ($<$ 44 mm diameter) so it fits within the bore of a small electromagnet or cryostat. We share our apparatus and design freely with the research community, enabling new groups to more quickly build and customize an apparatus to test their chips. These results will help the quantum computing research community to fabricate and test advanced quantum computing devices faster.

Lay Summary

Quantum computers are machines that store and process information quantum mechanically and have the potential to revolutionize what can be computed. Building a large-scale quantum computer that can tackle problems that cannot be solved on classical computers is a major challenge. Spin qubits are a promising system to make a large scale quantum computer as they are stable and easy to manufacture. To date, 2 and 4 qubit processors have been demonstrated, but they are not optimized yet and scaling them presents several challenges.

In this thesis, we devise and demonstrate a simplified fabrication process to make a scalable hole-spin quantum dot processor. We also design an apparatus for testing small quantum processors. Our design is compact, making it compatible with small cryostats and electro-magnets. We open-source our apparatus to the quantum computing research community so that new groups can more readily test their chips.

Preface

This thesis is based on a research project conducted by myself under the supervision and guidance of Dr. Joe Salfi.

All devices described in this thesis were fabricated in the UBC nanofabrication facility. The wafers that the devices are built on in chapter 2 were supplied by the group of Dr. Giordano Scappucci at TU Delft. This is the convention in the research field. Groups that synthesize materials generally do not develop the capability to build advanced devices, much less perform advanced experiments on them, since the methodologies are so dissimilar. I contributed to the development of the fabrication process for the devices in chapter 2 in a team environment led by a PhD candidate (Mukhlasur Tanvir) and Postdoc (Dr. Ebrahim Sajadi) in our group, as it customary in the research field.

The measurement and analysis of the devices presented in chapter 2 were carried out by me, with input from the team described above. The nanofabrication process along with a a set of experimental results on similar devices are the subject of a paper in preparation by Dr. Sajadi and Mr. Tanvir, of which I am a co-author.

I led the design, optimization, measurement, and analysis of the sample carrier in chapter 3. The sample carrier designed and tested in chapter 3 is the subject of a manuscript that has been prepared and submitted that I am first author of that paper.

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Acknowledgments

First, I would like to express my deep gratitude to my supervisor, professor Joseph Salfi, for his patient guidance, enthusiastic encouragement, and helpful critiques of this research work. I thank him for providing me with an excellent research opportunity in his lab and his nonstop supports to provide an excellent learning atmosphere in his research group. Every single conversation with him was inspiring lesson for me and made me being able to think outside the box, from multiple perspectives to form a comprehensive study. I am deeply thankful for your wisdom and all the life lessons you taught me during my thesis and would never forget them.

Second, I am very fortunate and grateful to have excellent colleagues who offered me genuine and friendly support and assurance to carry out my research. I should particularly thank Ebrahim Sadjadi and Mukhlasur Tanvir whom they contributed and helped to make this research work possible. I appreciate them for very helpful meetings and discussions we had. My special thanks to Mohammad Khalifa for helpful discussions and feedback on my research project. I appreciate him for all his encouragement during the planning and development of this research work. My great appreciation to Amin Ghasemazar for sharing with me his valuable experiences generously and dedication of his time for instructive discussions about my research.

I also gratefully acknowledge the UBC Quantum Materials Institute for providing us with nanofabrication facilities, the group of Dr. Giordano Scappucci at TU Delft for supplying us the wafers that made chapter 2 possible, and funding provided by the NSERC Create Quantum Computing Program.

My last but foremost and deepest thank to my family, whom they always believ-

ing in me and without them I was never able to get through tough times of my life. My deep and sincere gratitude to my parents whom I am profoundly indebted to, for their unconditional love, support, and blessings. Special thanks to my brother, Amin, and my sister, Helia, for their support and encouragement throughout my study.

Dedication

This thesis is dedicated to my parents, Babajoon and Maman Fathieh.

For their endless love, devotion, and unconditional support.

Chapter 1

Motivation and Background

Nature isn't classical, dammit, and if you want to make a simulation of nature, you'd better make it quantum mechanical, and by golly it's a wonderful problem, because it doesn't look so easy. — Richard P. Feynman

1.1 Motivation

The building blocks of quantum computers are quantum bits (qubits). Unlike a classical bit, which can be either "0" or "1', a qubit can be in a linear superposition of both a $|0\rangle$ state and a $|1\rangle$ state. This, combined with the ability to entangle multiple qubits into multi-qubit superposition states, gives a quantum computer enhanced computational power compared to a classical computer [65]. However, there are many challenges that must be overcome to make powerful quantum computers. Quantum states are intrinsically fragile and their state can be corrupted through a process called decoherence as a result of unwanted interactions with the environment. When a qubit is completely isolated from its environment, its coherence is preserved. However, unwanted interactions of qubits with the environment is difficult to avoid, because a qubit used in a calculation must be controlled by an apparatus, so it is not completely isolated.

After years of progress, qubits can now be manipulated with error rates from decoherence below 1% per operation [6, 38]. Error rates and system sizes have

now reached the point at which calculations can be done that are deemed classically intractable on a superconducting quantum processor [6] or using a photonic system [116]. However, these calculations are contrived to suit this purpose, and have no practical applications. Quantum computers having around 50 to 100 qubits and error rates around 1% per operation have been termed noisy intermediate-scale quantum (NISQ) computers [77]. Using error correction schemes and fault tolerant circuit diesng, the use of thousands of physical qubits per single logical qubit (millions of physical qubits for useful quantum computers), errors can effectively be eliminated entirely from quantum computers. Reducing errors so that NISQ era quantum computers can outperform classical computers, and scaling to millions of qubits required for fault tolerance, are open challenges in the field. Find an ideal quantum hardware platform to scale up will be very challenging.

Many different quantum hardware platforms exist. Quantum dot spin qubits [55] are amongst these, and are appealing partly due to their similarity to the classical transistor which is well understood in the semiconductor industry, and also because of their long coherence times, which help minimize errors. The very small (100 nm$\times$100 nm) footprint and inherent compatibility with conventional semiconductor circuits are very appealing for scaling beyond thousands of qubits [98]. Initial research focused on the group III-V semiconductor GaAs, however, the spins of the nuclei in the GaAs host crystal fluctuate, forming a noisy environment for the spin qubit, resulting in rapid decoherence. Research focus thus shifted to group-IV materials more familiar to the semiconductor industry, where the nuclear spin environment can be eliminated using isotope purification, resulting in very long coherence times. Ge/GeSi heterostructures studied in this thesis allow for the confinement of holes. The hole spin experiences a strong spin-orbit coupling compared to the electron spin, facilitating control of qubits electrically, rather than magnetically, as for electron spin. This is anticipated to be highly beneficial for the fabrication of large arrays of spin qubits. Small scale spin-based quantum processors have recently emerged with 2 and 4 qubits [35, 36]. However, the devices have yet to be optimized, and a clear pathway to scaling them awaits demonstration. Hole spin qubits are an advantages route for this, because the architectures for overcoming noise and making long distant interconnects for hole spin qubits while maintaining long coherence times have recently been proposed in Si and Ge

[82, 104], and demonstrated experimentally in Si[46]. These recent advances make hole spin qubits an appealing candidate for scalable quantum computers.

In Chapter 2 of this thesis, we demonstrate the first Ge/GeSi quantum dot devices, and novel single-layer gate process for their fabrication. We demonstrate the key functionality of the devices, the ability to manipulate the number of charges in the device one by one, through single-hole transport spectroscopy. We characterize the key parameter of the system, the addition energy, and the coupling to the gates. In Chapter 3 of this thesis, we demonstrate a simple apparatus that will enable in the future the control and measurement of a system of a few qubits on a chip. The apparatus consists of a copper box and two-layer PCB that can be cooled to the base temperature of a dilution refrigerator and has 8 microwave control lines and 24 low-frequency control lines suitable for forming, controlling, and measuring a handful of Ge/GeSi hole spin qubits. We characterize the apparatus and show that it has very low cross-talk and no electromagnetic resonances up to 7 GHz, making it suitable for cryogenic quantum device research. Typically, research groups develop their own apparatus, which is time consuming, or purchase expensive ones that are difficult to customize from a small number of vendors. We make the apparatus available to the research community to lower the barrier of entry to the field for new research groups.

1.2 Quantum Computation

Over the past few years, quantum computing has attracted significant attention as the prospective technology for solving complex problems in different fields, such as condensed matter physics, quantum chemistry and machine learning. Quantum algorithms addressing hard problems, such as Shor's algorithm for factoring large numbers, have been proposed [87], and some of them have already been demonstrated on small quantum systems [99]. The power of these quantum algorithms becomes more evident as the size of the problem gets bigger, and requires a larger quantum computer. The reason computing power scales rapidly as the quantum computer gets bigger is because quantum computers process information in a space of 2^n complex numbers defined by n qubits. This becomes possible through the interesting property of quantum superposition in quantum mechanics. In quan-

tum computers, information is represented in a fundamentally different way than in classical computers. Instead of the classical binary encoding in either "0" or "1", information is encoded in a superposition of both "0" and "1", simultaneously. The elementary unit that carries information in a quantum computer is called qubit, and its state is represented by $\alpha|0\rangle + \beta|1\rangle$, where the complex coefficients α and β represent the information stored in the qubit. When a qubit is measured, its state collapses to one of the classical basis, "0" or "1", with probabilities $|\alpha|^2$ and $|\beta|^2$, respectively. In a system of many qubits, two or more qubits can be entangled (i.e. correlated), where their states cannot be described separately from each other, and measuring one of them affects the state of the others. A universal quantum computer [21] is required to perform four kinds of operations: 1) qubit initalization, 2) single-qubit operations, 3) two-qubit operations and 4) readout operations. There is yet another requirement, which is 5) that the quantum states resist decoherence, the process by which the environment corrupts the quantum states inside the quantum computer through unwanted interactions with the qubits.

For an n-qubit system, the state is at any time corresponds to a point in a 2^n-dimensional space. A computation can be performed with a quantum circuit, which transforms the state of the system, which includes the inputs to the calculation, from one point to another within the 2^n-D space. Any quantum circuit can be decomposed into a finite sequence of single- and two-qubit operations (also called quantum gates) [7]. Quantum algorithms exploit these properties to provide faster computations, compared to classical algorithms, where the speedup can be exponential in certain cases. Qubits are noisy, which introduces errors to quantum computations. However, a scheme called quantum error correction (QEC) has been invented to correct errors. The combination of quantum error correction and fault-tolerant circuit design enable arbitrarily accurate computation if the physical qubits have errors below a below certain threshold. Applying QEC, however, requires encoding the information of one logical qubit in many physical qubits. Because reducing errors from decoherence is so challenging, thousands of physical qubits are required for one logical qubit, which is far more qubits than are available in current technologies. Today's quantum computers therefore do not yet have error correction, are are termed noisy intermediate scale quantum (NISQ) computers[77]. Current research in quantum computing focuses on finding suitable

applications for the NISQ systems on the short term, as well as optimizing QEC approaches for large-scale quantum computers on the long term. On the experimental side, the goal is to develop quantum systems that are as insensitive-to-noise as possible, in order to expedite the realization of fault-tolerant quantum computing, and enhance the capabilities of NISQ systems as well, where spin qubit systems offer potentials for the pursuit of this goal.

1.3 Quantum Simulation

Quantum simulators are special purpose quantum computers enabling simulation of physical systems that are hard or impossible to simulate on classical computers [29]. One of the expected applications of quantum simulators is to simulate condensed matter physics and eventually design novel materials at scales impossible on classical computers. Many types of quantum information systems have been proposed for quantum simulation including superconducting circuits, nuclear spins, and trapped ions [29]. Qubits based on silicon electronic devices have major advantages for this pursuit: the devices can be industrially fabricated and host electron spin based qubits which have among the longest coherence times available [16, 30].

The properties of spin qubits make them especially suitable for simulation of materials. Most importantly, the motion of spins in semiconductor mimic the behaviour of electrons in materials when they exchange their positions (exchange statistics) [57], unlike superconducting qubits or trapped ions [8], which allows for efficient material simulation. Spin-qubits hold their quantum state for up to a million times longer than do qubits made from superconducting circuits [64, 100], are simple to manipulate [16], and are sub-micron scale, allowing huge numbers to be placed on each chip, compared to today's superconducting qubits [30].

In the Section 1.4 we review different type of hardware available for quantum computers to better understand why hole-spin qubits could potentially be a successful platform for quantum computation.

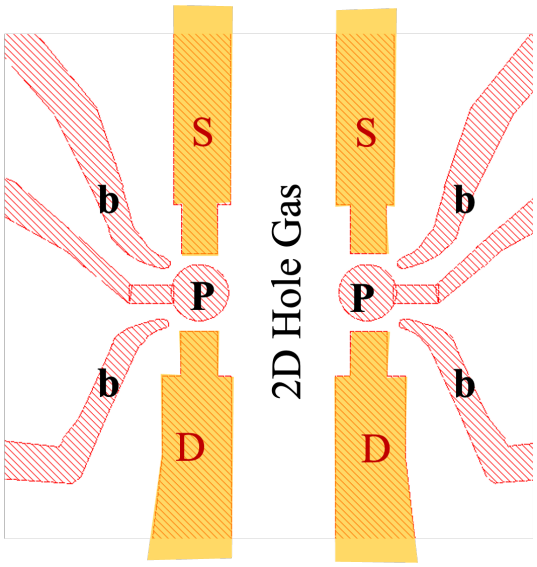

Figure 1.1: Schematic of two quantum dot devices formed by gates. The quantum dot is defined under the top gate plunger gate (P) and its occupancy can be controlled by changing the voltage of the plunger. Controlling the voltage of the barrier gates (b), define the tunnel rate of the charge (hole) into and out of the quantum dot from a reservoir (S and D).

1.4 Hardware of a Quantum Computer

David DiVincenzo defined five criteria for constructing a practical quantum computer that are still used to this day [24]. These criteria are:

1. **Scalability**: a scalable physical system with well-characterised qubits,
2. **Initialisation**: the ability to initialise the state of the qubits to a simple fiducial state,
3. **Coherence time**: long coherence times, much longer than the gate operation time,
4. **Quantum gates**: a 'universal' set of quantum gates, and
5. **Measurement**: the ability to measure the qubits in the basis $|0\rangle$ and $|1\rangle$.

Based on the above-mentioned criteria, there exist different hardware which a quantum computers can be built based on. We explain the technologies and challenges of superconducting qubits, trapped ion qubits, and spin qubits in quantum dots, which is the focus of this thesis.

1.4.1 Superconducting Qubits

While single electrons are the basic charge carriers in normal conductors, pairs of electrons, called "Cooper pairs", are the charge carriers in superconductors. Cooper pairs are bosons as their total spin is an integer as they consist of two half-spin electrons. Unlike fermions with the same quantum numbers that they cannot occupy the same quantum energy level, cooled bosons are allowed to occupy a single quantum energy level which is known as Bose-Einstein condensate. A complex probability amplitude is a measure for condensate wave function at every point of a superconducting electronic circuit that describes the charge flow. The condensate is a macroscopic quantum mechanical state but behaves similarly to microscopic quantum systems. For example, only a discrete number of magnetic flux quanta penetrates a superconducting loop, similarly to the discrete atomic energy levels in the Bohr model. In both cases, the quantization is a result of the complex amplitude continuity. Differing from the microscopic quantum systems used for implementations of quantum computers, macroscopic superconducting circuits can often be described by dissipationless capacitive and inductive circuit elements, where the inductances possess a non-linearity. A key element for superconducting qubits is the Josephson Junction, a superconductor-insulator-superconductor junction. Because of the nonlinearity of the Josephson inductance, superconducting qubits can be described as anharmonic oscillators.

This platform offers devices with little dissipation, large-scale-integration, and a family of classical electronics that could be used for qubit control [6]. One problem with superconducting qubits is that the anharmonicity of the oscillator is weak, so that it is possible to excite the system out of the $|0\rangle$ and $|1\rangle$ states. The macroscopic size of the qubits is a disadvantage for scalability, and they are difficult to miniaturize without compromising coherence times. The coherence times of superconducting qubits have seen great improvements recently, but are still lower than

for many other approaches.

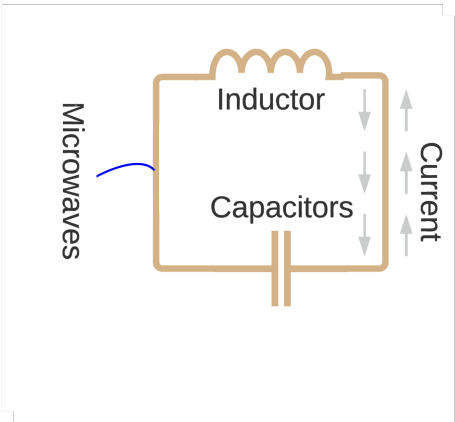

Figure 1.2: Schematic of a superconducting circuit in which current oscillates back and forth with no resistance. Injected microwave signal excites the current into superposition states.

1.4.2 Trapped Ion Qubits

Ions can be confined and suspended in free space using electromagnetic fields. Qubits are stored in stable electronic states of each ion, and quantum information can be transferred through the collective quantized vibration of the ions in a shared trap. Moreover, lasers are used to induce coupling between the qubit states or coupling between the internal qubit states and the external vibrational states. The fundamental operations of a quantum computer have been demonstrated experimentally with the currently highest accuracy in trapped ion systems [66]. Subsequently, trapped ion qubits could be promising schemes to be scaled as they can be transported to spatially distinct locations like in an array of ion traps and still be entangled via photonically connected networks of remotely entangled ion chains [62]. The main challenges facing trapped ion quantum computing are the initialization of the ion's vibrational states, and the relatively brief lifetimes of the vibrational states [17]. Large numbers of lasers are required to manipulate trapped ion systems, and each qubit occupies a large area, compromising the scalability of trapped ion quantum computers.

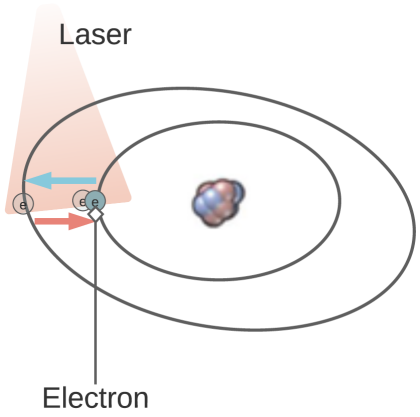

Figure 1.3: Schematic of trapped ions, electrically charged atoms, or ions have quantum energies that depend on the location of electron. Adding tuned laser to the system, cool ions and trap them and put them in superposition state.

1.4.3 Spin Qubits

Spin qubits are based on the same core technology of transistors and integrated circuits that powered the classical information revolution. A transistor works by forming a conductive channel underneath a gate through which current can flow. A spin qubit can be made using a quantum dot, whose operation principal is very similar. In fact, that gate can locally attract or repel electrons, depending on the polarity of the voltage applied to it. Using a very small attractive gate, we can isolate a small puddle of electrons. This puddle of electrons is called a quantum dot, and it is routine within the research field for the puddle to be reduced down to a single electron. This single electron possesses a spin, a two-level quantum mechanical system that can be manipulated using microwaves [52].

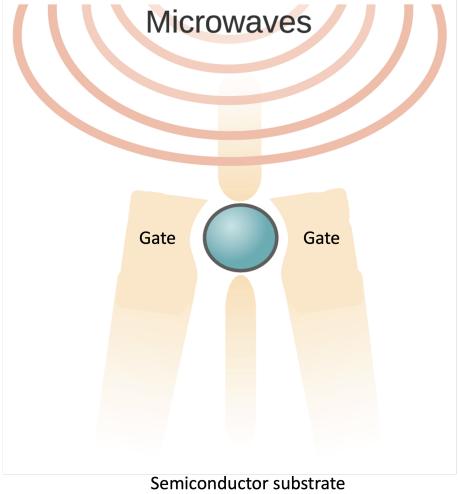

Figure 1.4: Schematic of spin qubit system, based on the charge confinement using gates on an appropriate semiconductor substrate. State of the qubit can be controlled using microwave signal.

Recently, two and four electron spin-based quantum processors have been demonstrated [35, 36]. The small $\sim$ 100 nm size of quantum dots offers the prospect of integrating millions of qubits within a single chip, which is important, since a useful error-corrected quantum computer would require roughly this many qubits. In the case of semiconductor spin qubits, the long-term vision for quantum computing relies on long coherence times recently demonstrated in silicon-based devices. Compared to superconducting and trapped ion qubits, spin qubits are relative newcomers to quantum computing hardware. The best method to scale spin-qubit based processors up is not yet known, but the prospects for the technology are very exciting due to the small qubit size, industrial manufacturability, and stability of the qubits.

1.5 Quantum Dots as Spin Qubits

One of the first proposed approaches for quantum computation dates back to 1997 which is the use of the spin of isolated electrons in quantum dots to form spin qubits, in the Loss-DiVincenzo (LD) proposal[55]. In this architecture, spin of an electron ($\uparrow$ and $\downarrow$) trapped within the quantum dot defines the qubit basis states.

Arbitrary single-qubit control around the Bloch sphere is achieved using electron spin resonance (ESR) techniques where a large static magnetic field B_0 is used to produce the energy separation between the $|0\rangle$ and $|1\rangle$ basis states (via the Zeeman interaction). A smaller oscillatory field $B_1(t)$, applied perpendicularly to B_0, drives rotations of the qubits which form the single-qubit logic. The two-qubit logic is suggested to be implemented using the exchange interaction resulting from tunnelling processes of electrons on adjacent quantum dots [55] that leave the electron numbers of each quantum dot fixed. Combined with the single-qubit control, this allows for a universal set of one and two qubit gates [35].

The ability to measure individual quantum states is a critical step in any form of quantum information processing. Ideally this is done rapidly (relative to the system dynamics) and with a high fidelity. In spin qubit architectures this might seem a challenging task, as the magnetic moment of an electron or hole spin is very small, making it difficult to measure directly. However, using protocols that correlate a spin state with a corresponding charge state, known as spin-to-charge conversion [26], we can transform this task into the more simple requirement of determining the number of electrons in each quantum dot.

1.5.1 Spin Qubit Implementation: Materials

Early quantum dot research were focused on gallium-arsenide (GaAs) heterostructures with very high charge carrier mobilities. GaAs has has low level of disorder allowed the study of spins in single [26, 33], double [47, 74] and larger arrays of quantum dots [78, 88]. However, the nuclear spin bath present in group III-V materials and the interactions between the spin qubit causes rapid decoherence. This is why the focus of quantum dot spin qubit is now towards the group IV material such as silicon and germanium, where mostly the net nuclear spin is zero [39], and the nuclear spin can be removed entirely using isotope purification [39, 40]. Quantum dot spin qubit of group IV materials are shown to have long coherence times [100, 113]. Moreover, scientists have shown one-qubit gate fidelities of over 99.9% using electronic pulses [111], and two-qubit gates have been studied [73, 115], with fidelities up to 98% [38]. This enabled implementation of quantum algorithms, such as Grover's search algorithms in two-qubit systems [61], as well as

tomography of multi-qubit entangled states [94, 105].

In parallel, research efforts focused on the integration of spin qubits with circuit quantum electrodynamics (QED) elements, that form the basis of the superconducting qubit platform. Coupling the spin state to a microwave photon [50, 61, 83] could define a way to couple distance qubits which cannot be realized by exchange interaction. As a first step to the integration of spin qubits with classical electronics two-qubit logic at temperatures as high as 1 K has been demonstrated [72, 112].

It has been shown recently that hole states in germanium could be a potential candidate for quantum information technology [14, 15]. Germanium also mostly has zero nuclear spin. Not only germanium has low degree of disorder [27, 84], it relatively has small effective mass [54, 108], which enables the definition of fully gate-defined quantum dots, such that the quantum dot properties can be well-controlled [34]. Importantly, as mentioned earlier, Germanium can be isotope purified to eliminate the nuclear bath, promising long coherence times of hole spin. Moreover, hole valance band states in germanium has the advantage of not having valley degeneracy comparing to electron state in silicon. Furthermore, hole valance band states in germanium potentially has large splitting between the ground and excited state of the qubit [34, 95]. The strong spin-orbit coupling enables fast, all-electrical control of the spin state [15], eliminating the need for microscopic elements such as micromagnets [105, 115] or striplines [101]. Finally, the Fermi level in germanium aligns with the valence band edge, enabling the integration of ohmic metal contacts and opening up the path to hybrid semiconductor-superconductor systems.

As it is evident from what we already discussed, quantum dot spin qubits are not limited to the state of the electron in conduction band. Around the time when the first demonstrations of electron spin qubits were shown [47], theoretical studies predicted that also unfilled valence band states (holes) could be promising candidates for spin qubits [14]. The experiments in this thesis are all based on valence band holes in germanium quantum wells.

1.6 Scalable Quantum Computing

In this section, we will discuss requirements for scalable quantum computer that are needed for useful quantum computation.

One of the important applications of a quantum computer is factoring of large numbers using Shor's algorithm [87]. The most efficient known classical factoring algorithm needs exponential time to solve this problem. A quantum computer running Shor's Algorithm, could allow factoring to be achieved in polynomial time. The bigger the size of the problem become, the more evident the strength of this algorithm would be and that is where a quantum processor becomes so exciting to be achieved. Moreover, there are other high impact problems such as protein folding [71] and quantum chemistry simulations [51, 107] where quantum speedups using only a limited number of qubits have been predicted.

A factor that increases the number of qubits required for quantum computers to outperform classical ones is quantum error correction (QEC) is likely to be necessary in order to perform useful computations [86, 91]. In quantum error correction, a large number of physical qubits, a few thousand or more, are required to build one reliable logical quantum bit. The large overhead comes from the relative high error rate of around 1% to 0.1% of even the best physical qubits. This also implies that millions of qubits are likely needed to build useful quantum computers [6, 111].

1.7 Quantum Experiment

The apparatus of quantum computers is very different from classical computers, and is influenced by the following factors

- **Cryogenic environment**: Spin qubits and superconducting qubits are operated at low temperatures of around 100 mK to 1K, and 20 mK, respectively. The chip containing the qubits and the components to interface them to qubit control systems must be cooled down far below room temperature.

- **Space**: Cryogenic systems can cool down a limited mass of material, and have limited space. The quantum processor and all of the components that need to be at base temperature need to fit in a volume typically not much bigger than 300 mm in diameter and 100 mm in height. The electrical com-

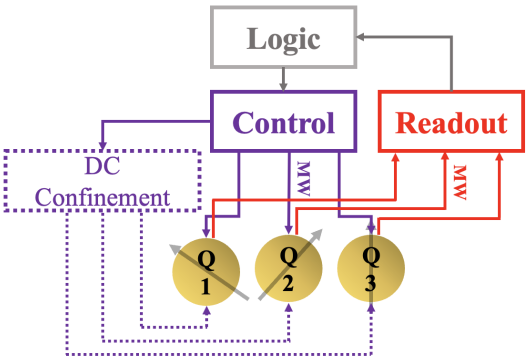

Figure 1.5: A general multi qubits processor diagram, including low level logic, DC signal lines for charge confinement, MW signal lines for control and readout qubits.

ponents and cables must be small enough so they all fit in the limited space available.

- **Magnetic fields**: Spin qubits typically require high magnetic fields of order 1 T to define the qubit levels. The magnetic fields are typically created by superconducting solonoids. These solenoids have typically accomodate objects with a 50 mm to 100 mm diameter, restricting the available volume further. The use of high magnetic fields also limits the choice of the materials to ones that are not magnetic.

- **Signal fidelity**: The quantum states in qubits can be corrupted by very low levels of noise. To reduce errors, the signals must have very low noise levels, and be protected from stray electromagnetic waves and thermal electromagnetic radiation.

- **Signal number**: The number of microwave signals required to both control and read out qubits grows linearly with the number of qubits. Low-frequency signals are also required to control qubits. For exampe, the formation of spin qubits requires voltages applied to gates that do not need to be rapidly changed. These voltages shape the electric potential that confines the electron or hole.

The scaling up of quantum computers require solving major scientific challenges, as well as technical advances for qubit readout, control, and mitigating noise.

1.8 Qubit Control Technique

In the context of quantum information processing, 'control' refers to the ability to implement quantum logic gates, in order to implement quantum circuits and quantum algorithms. Analogous to classical logic, quantum logic can be synthesized from a finite set of gates [22]. The implementation of quantum control control depends on the type of the quantum hardware. Photonic qubits are manipulated with beam splitters and phase shifters [45], trapped ions are controlled with lasers and microwaves[17], and superconducting and spin qubits are controlled with shaped microwave pulses [109].

1.8.1 Microwave

Microwaves quantum logic gates in spin qubit architectures require the control of energy levels via nanosecond voltage pulses applied to the gate electrodes of the single-electron devices. These can serve to modulate the exchange interaction between spin qubits [74]. Modulated microwave signals at the spin transition frequency enable single-qubit quantum logic [47]. The broadband nature of these signals necessitate the use of coaxial microwave waveguides, for NISQ era systems.

1.9 Qubit Readout Techniques

Quantum computation requires the ability to measure qubits. An ideal measurement should be done with high fidelity and rapid enough so it is faster than the dynamics of the system.

For spin qubits, this might seem a challenging task, as the magnetic moment of a charge spin is very small, making it difficult to measure directly. However, using protocols that correlate a spin state with a corresponding charge state, known as 'spin-to-charge' conversion (Section 1.9.1) [32, 42], we can transform this task

into the simpler requirement of determining the number of charges in each quantum dot. The way it works is that the different spin states will be projected onto different charge states. These charge states can in turn be measured using a nearby charge sensor that is the subject for Section 1.9.2, Section 1.9.3, and Section 1.9.4.

1.9.1 Spin to Charge Conversion

Two of the methods for spin-to-charge conversion that have experimentally demonstrated include energy-selective readout and tunnel-rate-selective readout. In both methods, a magnetic field is applied to split the spin-up and spin-down energy state by Zeeman energy splitting.

In the energy-selective scheme, as it is shown in Figure 1.6-a the dot potential is tuned so if the electron has spin-down it will leave the state and transfers the the reservoir, whereas it will stay on the dot if it has spin-up. In this case any charge detection refers to the spin-down tunneling of the charge on to and out of the dot. No charge detection refers to the spin-up state of the charge.

Alternatively, in tunnel-rate-selective scheme as it is shown in Figure 1.6-b, spin-to-charge conversion can be achieved based on the different tunnel rates of spin-up and spin-down to the reservoir. The general concept for the scheme is that we have two charges with different spin state. For the charge with higher coupling to the reservoir, the tunneling rate is higher (singlet and triplet spin state have different wave functions that causes different coupling to the reservoir [49] which is out of the scope of the material we discuss in this thesis). Different tunneling rate causes within short time window that has the value between the time each of the charges require to tunnel to the reservoir, the charge with higher tunnel rate has higher probability to tunnel and be transferred. Measuring the number of the charge transferred through the dot reveals the original spin state.

1.9.2 Charge Detection with Quantum Point Contact

A narrow conducting channel called a quantum point contact can be used as a charge sensor. The width of the channel can be modified by varying the voltage applied to surface electrodes, as shown in Figure 1.7. The conductance through the QPC is controlled using voltages applied to the same gates, and is quantized

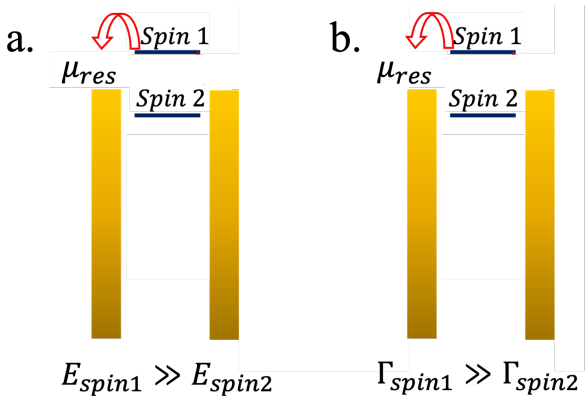

Figure 1.6: Energy diagrams for two methods of spin-to-charge conversion, a- energy-selective readout, b- tunnel-rate-selective readout where Γ is the tunnel rate of the charge to the reservoir.

in units $2e^2/h$. At low temperatures, the transition from one plateau of quantized conductance to another is a sharp function of gate voltage. This makes the QPC being very sensitive to its local electrostatic environment and able to measure very small amounts of charge quickly. In particular, small changes in the number of electrons on a quantum dot, N, can result in large changes in the current through a nearby capacitively coupled channel.

Experimentally this technique is well understood and has been exploited to determine the number of electrons in single [90] and coupled quantum dots [25] down to the single-electron regime.

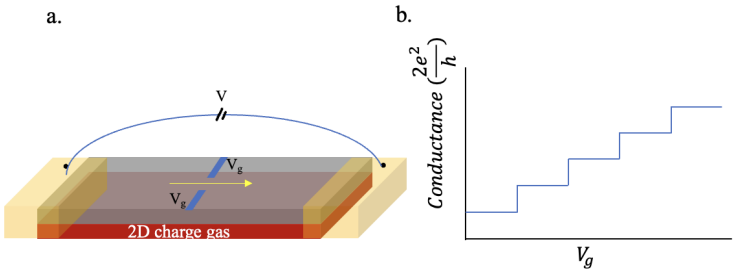

Figure 1.7: a- Schematic of a QPC, split gates on a 2D electron/hole gas, b- QPC conductance at multiples of $2e^2/h$ as a function of gate voltage.

1.9.3 Charge Detection with Single Charge transistor

Another method of sensing a charge is to use another quantum dot or single electron/hole transistor (SET or SHT). The current that flows through an SET is zero for gate voltages in the Coulomb blockade regime, and non-zero in between those regions. At low temperature, the transition from Coulomb blockade to the non-blockaded region is a sharp function of gate voltage. Like the QPC, this makes the SET or SHT very sensitive to its local electrostatic environment and able to measure small amounts of charge quickly. In particular, small changes in the number of electrons on a quantum dot, N, can result in large changes in the current through a nearby SET or SHT.

1.9.4 RF Reflectometery

The electrical wiring that connects devices at the base temperature of a cryostat to the outside world is typically 2 meters long. To maintain high bandwidth of measurement and low noise, 50-ohm coaxial cables are used to transmit the microwave signals, which are also amplified at low temperature using a cryogenic low-noise amplifier with a noise temperature typically around 2 K. The QPC or SET/SHT used in the measurements are then placed inside an impedance matching circuit, because their impedance cannot be less than $2e^2/h \sim 10\ k\Omega$ for fundamental reasons. Using these techniques, single-electron detection has been demonstrated [81, 114].

Chapter 2

Quantum Dot Device: Ohmic Contacts and Coulomb Blockade

Solid-state quantum computing is actively pursued using superconducting and semiconducting materials [10, 74]. In this regard, the group-IV semiconductors silicon (Si) and germanium (Ge) come with central advantages for the realisation of spin quantum bits (qubits). Not only does there exist a mature classical technology for Si and Ge, but they also have isotope with zero nuclear spin [39, 40], enabling spin qubits to reach extremely long coherence times [89, 100] and high fidelity [113] not found in the compound semiconductors or in superconducting devices. These properties have led to demonstrations of two-qubit logic gates [101, 115] and quantum algorithms [105].

Hole quantum dots are particularly promising in Si and Ge. Holes can be manipulated electrically, making hole qubits [59, 106], more scalable than electron qubits, which are manipulated magnetically[100]. In spite of this, extremely long coherence times have been recently demonstrated for holes in silicon [46]. For hole qubits, Ge has certain advantages over Si. Ge has the highest hole mobility of all known semiconductors [75], reaching values up to $\mu = 1.5 \times 10^6 \ \frac{cm^2}{Vs}$ in doped heterostructures[27], which is important since qubits require high quality heterointerfaces, and high mobility is an indicator of high interface quality. Long coherence times have been recently been predicted to be possible in Ge, like Si [104]. Recently, a four-qubit process has been demonstrated in Ge [36]. Furthermore,

the valence band in Ge have no valley degeneracy which results in quantum levels with larges spacing comparing to electrons [110]. All above-mentioned properties makes the Ge/SiGe a potential platform for scalable quantum computation.

Here, we demonstrate the formation of quantum dot in a planar Ge quantum well via a demonstration of a single-hole transistor defined by a plunger gate to induce charge carrier underneath, barrier gates to create tunnel barriers, and accumulation gates to define the source and drain reservoirs of the device. Our wafer is nominally undoped, so the device works by applying negative voltages which accumulate a hole gas in the reservoir and accumulate individual holes under the plunger gate. Our accumulation mode device is created using a novel single-layer process with advantages over previous work which utilized a two-layer gate process[34]. Our process has the advantage of requiring one fewer lithography step, which is less work and does not require alignment of the second layer to the first. Both of these advantages improve yield in devices fabricated in university cleanroom. The main trade-off is that the reservoir must be slightly farther away from the quantum dot, to accommodate the tunnel barriers between them. We find that tunnel are sufficiently transparent (can readily be tunneled through by single holes) to observe the hallmark of quantum dot formation, hole transport in the Coulomb blockade regime[32].

In this chapter we discuss the ability to manipulate the number of charges in the quantum dot one by one, and characterization of the key parameters of the system, the addition energy, and the coupling to the gates.

2.1 Gate Defined quantum dots

The proposal to use the spin of a quantum dot as a qubit was made by Daniel Loss and David DiVincenzo about two decades ago [55]. A quantum dot is a system where charges are confined in a very small three dimensions volume. Because of the small volume, charges that are confined in the quantum dot experience a size quantization in their energy levels. Charges occupy the quantized energy levels. The spectrum of the energy levels resembles that of electrons in atoms, due to the size quantization. That is why quantum dots are also called artificial atoms. In semiconductor systems, the confinement is usually achieved through a combination

of material engineering and electric field potentials. In our work, confinement is achieved in the vertical direction via the heterostructure, and in the lateral direction through electric potentials applied to gate electrodes deposited on top of the wafer, around ~ 50 nm above the quantum well. Without the lateral gates, the stacking of materials with different band gaps, combined with the present of an electric field (provided by a gate called plunger) can give rise to the formation of a two-dimensional plane of charges: a two-dimensional electron or hole gas (2DEG and 2DHG respectively). Using lithographically defined metal gates on the 2DHG and applying right voltage to them, charges can be laterally confined as well, creating the quantum dot.

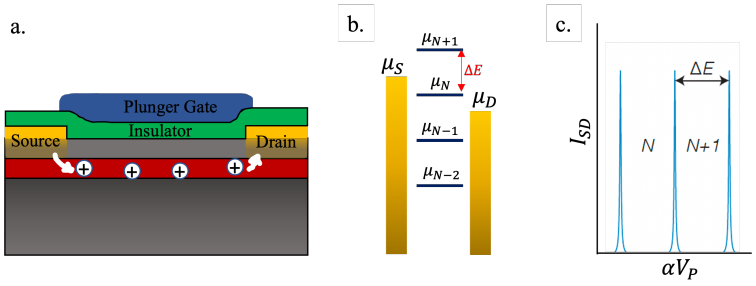

Figure 2.1: a- Schematic representation of a single quantum dot coupled to two ohmic reservoirs. White spheres indicate the charges (holes) on the quantum dot, b- Energy diagram of the quantum dot system. μ_S and μ_D indicate electrochemical potentials of the source and drain respectively. The level spacing ΔE, or the addition energy, in the quantum dot is defined by the charging energy E_C and the orbital spacing $E_{orbital}$. c- When the source-drain current is measured as a function of the plunger gate potential energy Coulomb peaks can be observed.

Figure 2.1-a shows a schematic of an accumulation-mode quantum dot device from a previous report[34]. The device has two close-by (~ 100 nm) reservoirs (source and drain) defined by Aluminum metals deposited on top of the well. A separate top gate is used to define the potential well and also to modulate the quantum dot electrochemical potential. Barrier gates (not shown) are used to control the tunneling rate of the charge into and out of the quantum dot.

To understand the transport properties (between source S and drain D) of this system, we first need to look at the energy levels available in the quantum dot.

Two separate effects are important. First, the classical Coulomb repulsion between charges on the island. As a result, adding another charge to the island will require a charging energy of $E_c = e^2/C$, where e is elementary charge and C the total quantum dot capacitance. Figure 2.2 shows a simple capacitance model of a quantum dot. The total quantum dot capacitance in this simple model is the addition of the capacitance that each of the gates introduce to the quantum dot [96]. Since C is proportional to the quantum dot size (the cubic root of its volume), the charging energy is larger for smaller quantum dots. Second, as a result of the spatial confinement of the wave function of the hole, similar to the particle in a box quantum mechanical problem, its energy levels are quantized (Figure 2.1b). To add an extra charge to the quantum dot, an energy difference of $E_{add} = E_c + E_{orbital}$ is needed, where the second term is zero for degenerate orbital states. The discrete level spacing can only be observed if the level broadening of both the reservoirs and the dot is smaller than the addition energy E_{add}. The first requirement can be achieved by cooling the system down such that $E_{add} > k_B T_e$, where T_e is the electron or hole temperature and k_B the Boltzmann constant. Using the barrier gates, the quantum dot is decoupled from the leads such that $E_{add} > h\Gamma$, where h is the Planck's constant and Γ is the tunnelling rate between the quantum dot and the leads. Transport through the quantum dot is now only possible when a QD energy level aligns between the electrochemical potentials μ_S and μ_D of the source and drain, respectively. Using the plunger gate, the electrochemical potential of the quantum dot can be modulated, thus shifting the energy levels with respect to $\mu_{S,D}$. When the transport current I_{SD} through the quantum dot is measured as a function of the plunger gate voltage V_P, a narrow peak in current (Coulomb peak) can be observed for each quantum dot level (Figure 2.1c) passing through the bias window $|\mu_S - \mu_D|$. The spacing between these peaks is equal to $\alpha \Delta V_P$, with $\alpha = C_{gate}/C$ the lever arm of the gate in meV/mV, which indicates how strongly a gate is coupled to the quantum dot. Our gates are based on a novel single layer deposition of metal through which we can control the transform of the hole in and out of our quantum dot that is discussed in Section 2.2.5.

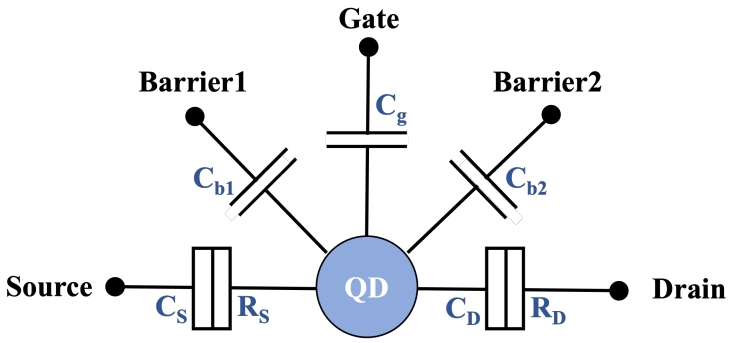

Figure 2.2: A simple capacitance model of a single charge transistor or a single quantum dot coupled to two ohmic reservoirs. Each of the gates define a capacitance to the quantum dot where C_S and C_D are the capacitance between the source and drain to the quantum dot. C_{b1}, C_{b2}, and C_g are the capacitance between the quantum dot and top defined plunger and barrier gates. The total capacitance of the quantum dot is $C = C_{\text{gate}} + C_{\text{source}} + C_{\text{drain}} + C_{\text{barrier1}} + C_{\text{barrier2}}$ in this simple model.

2.1.1 Coulomb blockade

Charge transport through a quantum dot can occur when the chemical potential of the quantum dot is between the Fermi energy of the source (μ_S) and drain (μ_D). The charge can then tunnel from the source onto the dot, and then tunnel off the dot to the drain without losing or gaining energy (elastically). For energies within this bias window, the electron states in one reservoir are filled, while the corresponding states in the other reservoir are empty. If the size of this window is smaller than the addition energy (E_{add}), no levels of the dot are available to the charge to tunnel so the number of charges on the dot remains fixed there is no current flow through the dot. This is known as 'Coulomb blockade' [11]. As we discussed, due to thermal effects, this behaviour can only be observed when the temperature of the systems is below the temperature T defined by $k_B T = E_{\text{add}} = E_C + E_{\text{orbital}}$, which depends on how small the quantum dot is. Coulomb blockade can be lifted by changing the potential of the dot relative to these reservoirs (effectively shifting the whole ladder of potential levels up or down) using capacitively coupled gate electrodes. Whenever a level falls within the bias window, Coulomb blockade is lifted and current flows through the dot. By sweeping the gate voltage and measuring the

transport current we can precisely tune the number of charges on the quantum dot.

2.1.2 Ohmic Contacts

A Schottky barrier is a potential energy barrier for charge transfer at a metal semiconductor junction. This barrier has a contact resistance which can hamper charge transfer from the metal to the semiconductor and vice versa, especially at liquid helium temperatures where electrons do not have enough thermal energy to pass over typical Schottky barrier heights, energetically. This problem can often be resolved, even at low temperatures, by defining local regions of high doping [5, 53], which effectively reduces the width of the Schottky barrier, making it penetrable by tunneling, and therefore less resistive. Germanium is a material that does not require significant doping for formation of low-resistance metal-semiconductor contacts, which is usually attributed to the energetic position of the Fermi level being pinned close to the valence band edge at the surface, which makes the barrier very small [23, 67]. As a result, germanium/metal contacts tend to have a lower resistance compared to almost all other semiconductor/metal contacts, for example, silicon/metal contacts. Alleviating the need for local implantation simplifies the fabrication of Germanium devices. In this work, we develop a method for ohmic contacts on our Ge chips with low contact resistance through which the charge can flow. We discuss the results in Section 2.2.4.

2.2 Experimental Methods

The device fabrication and measurement setup for the experiment are discussed in this section.

2.2.1 Device Fabrication Process

The field-effect transistor (FET) and quantum dot based single-hole transistors (SHTs) measured in this thesis are fabricated using a process with a single ohmic contact layer, a single gate dielectric, and a single gate layer. We fabricated the devices in the UBC Nanofabrication facility, using the wafer nominally identical to the one in reference [34]. Full details for the fabrication process can be found in Appendix A. Both the ohmic contact and the gate layer structures contain

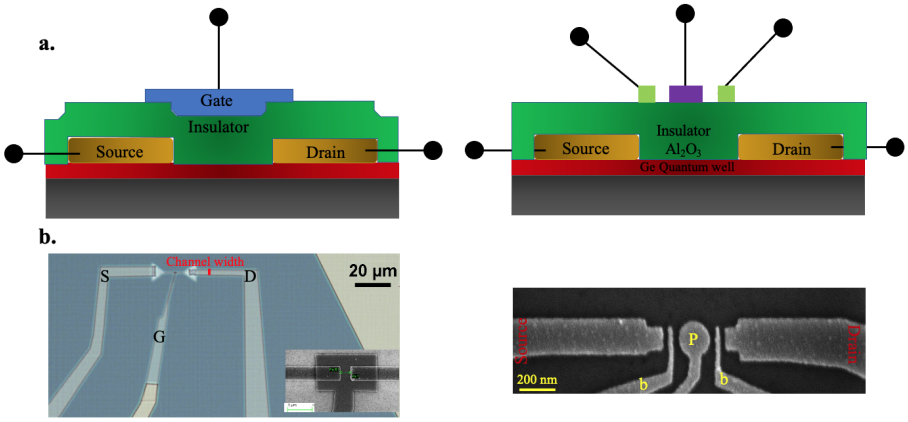

Figure 2.3: a- Side view of schematic representation of a field effect transistor (left) and a single quantum dot coupled to two ohmic reservoirs(right) on Ge quantum well with top gates on an insulator, b- Optical and SEM image of one of our fabricated FETs showing source, drain and the top gate (left), scanning electron microscopes image of one of one of our single quantum dots showing source and drain channels, and plunger and barrier gates.

nanoscale features, so they are created using a lift-off process employing electron beam lithography and physical vapour deposition using the electron beam evaporation technique. The dielectric deposition step is carried out using atomic layer deposition (ALD) of alumina (Al_2O_3) at a temperature of 250 °C. The first step is the ohmic contact deposition step (Aluminum), followed by dielectric deposition (Al_2O_3), and followed by gate metal deposition step (Palladium with a thin layer of Titanium underneath to improve adhesion). Prior to the deposition of Aluminum for ohmic contacts, the chip is dipped in buffered hydrofluoric acid, to remove a thin native oxide on the chip surface that hampers ohmic contact formation. Gate bond-pad are being made on the fine gates and as the last step we etch the dielectric from the ohmic bond pads. After the gate deposition, a layer of Pd bond pads are deposited, that will allow electrical connections to be made from the chip to a carrier PCB.

2.2.2 Device Design

The design of the field effect transistor (FET) is as follows. The source and drain ohmic contacts are defined by aluminum metal deposited on top of the wafer. Both the source and drain have a width W which is varied from less than 1 μm, to around ten μm, and are separated from each other by a distance L, the channel length. After deposition of the dielectric by atomic layer deposition, the gate is deposited between the source and drain, so as to overlap both, which enables the channel to be formed as close as possible to the source and drain. Due to the dielectric deposited on top of the source and drain ohmic contacts, but isolated electrically from them via the gate dielectric.

The design of the single hole transistor (SHT) is illustrated in the false colour scanning electron microscope (SEM) image in Figure 2.7-a . The Ti/Pd accumulation gates which generate the source and drain reservoirs for single hole tunneling are coloured in yellow. They overlap the alumina dielectric and the aluminum ohmic contacts, which are deposited directly on top of the wafer, like the ones used in the FETs. The Ti/Pd barrier gates are coloured in green and the Ti/Pd plunger gate is coloured in purple. All three of these gates are deposited in the same step, as discussed previously. Ohmic contacts are not in the SEM image. As illustrated in Figure 2.7, the ohmic contacts are further from the plunger gate.

The plunger gate has the shape of a "lolly pop", featuring a circular part with diameter $d \sim 150$ nm. The circulate shape of the plunger gate will induce a roughly circular puddle of holes. The smaller width of the metal wire connected to the plunger gate ensures that as the voltage on the plunger decreases, holes are accumulated first under the circular part of the gate. The plunger gate is located between the two barrier gates. The barrier gates are used to electrically control the tunneling barrier between the quantum dot and the ohmic reservoirs. Voltages applied to them can be used to adjust the tunneling rate. Decreasing the voltage of the accumulation gates will, for a small enough accumulation gate voltage, cause an accumulation of a reservoir of holes, which form the source and drain regions of the SHT.

2.2.3 Measurement Setup

Figure 2.4 shows a schematic of our low frequency measurement setup. The chip is cooled down to the $\sim$ 100 mK base temperature of a dilution refrigerator (DR). We apply DC voltages to the device's gates and measure the DC current flow from one ohmic contact to another using electronics at room temperature, through dedicated wiring for low-frequency signals in the DR. Voltages are supplied by a 24 channel digital to analog converter (DAC), with $\sim 1\ \mu V$ accuracy. Voltages created by this DAC pass through a custom-made low-pass filter mounted on the mixing chamber of the dilution refrigerator. The low pass filter block thermal radiation above around 3 GHz that comes from the room temperature electronics. The applied voltage causes a current flow in the device, from one ohmic contact to another, where it is measured by a low-noise current pre-amplifier with a measurement precision better than $\sim$ 1 pA. The pre-amplifier converts the current to voltage that can be measured using a data acquisition card.

2.2.4 Ge FET measurement

We fabricated chips with many FET devices on it with different channel length L and channel width W. The important metric we are looking to establish is whether or not a voltage applied to the gate can control the current from the source to the drain, and whether or not our metal source and drain electrodes can supply charge, i.e. operate as ohmic contacts, to the quantum well, as desired. This test is performed inside a Helium dewar at a temperature of 4 K. Establishing whether or not this works requires two tests. First, we verify that the gate dielectric is electrically insulating, by measuring the current that flows directly from the gate to the source and drain. Ideally this is zero, but a small current always flows. As long as the current that flows from the gate to the source and drain is much less than the current I_{ds} from the source to the drain, I_{ds} can be used to understand the formation of a conducting channel of holes underneath the gate. Once this is verified, we apply a small bias $V_{ds} \sim k_B T$ (or less) to measure the current I_{ds} in the linear regime, and sweep the gate voltage starting from a positive value to a negative value. Figure 2.5 shows a measurement of the conductance $G_{ds} = I_{ds}/V_{ds}$ inferred from the measured current I_{ds} for one of the FET devices with the channel

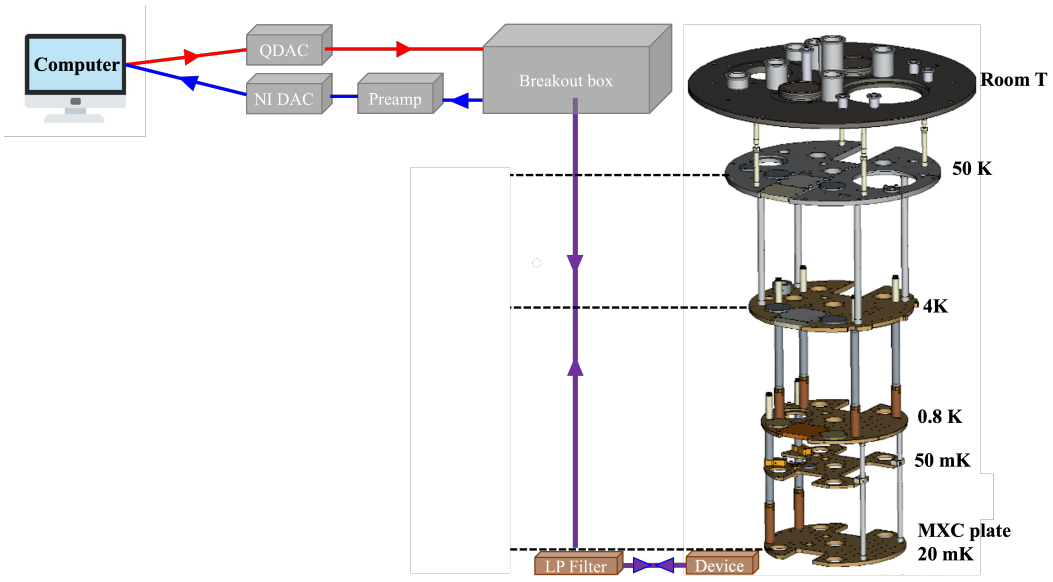

Figure 2.4: Schematic of the low frequency measurement setup, DC voltage applies through QDAC with μV accuracy and those channels we want to apply voltage through, are connected to the breakout box. Breakout box directly send the DC signal towards the DC filter (mounted on the MXC plate) through the DC wiring on the fridge including paired loom wire at low temperature. Right after the thermal radiation that can be transferred through wires are filtered, the DC signal is being sent to the sample. The signal induce a current in the sample that can be detected through the same DC wiring of the fridge that then go to the amplifier and NI DAC.

length and width of 1 μm. The device turns on abruptly at a voltage around -3.8 V, and the conductance saturates at around 40 μS. This measurement was taken with an applied bias of 200 μV.

The current I_{ds} and conductance $G_{ds} = I_{ds}/V_{ds}$ could easily be detected for contact widths W of 0.5 μm and higher. However, devices with widths W of 0.2 μm and 0.1 μm did not turn on. Interpreting the saturation of the conductance in the linear regime with drain-source bias as the access resistance of the source and drain to the channel, we have extracted the contact resistance R_c of the FETs. We plot the contact resistance R_c together with R_cW in Figure 2.6. For the devices with mea-

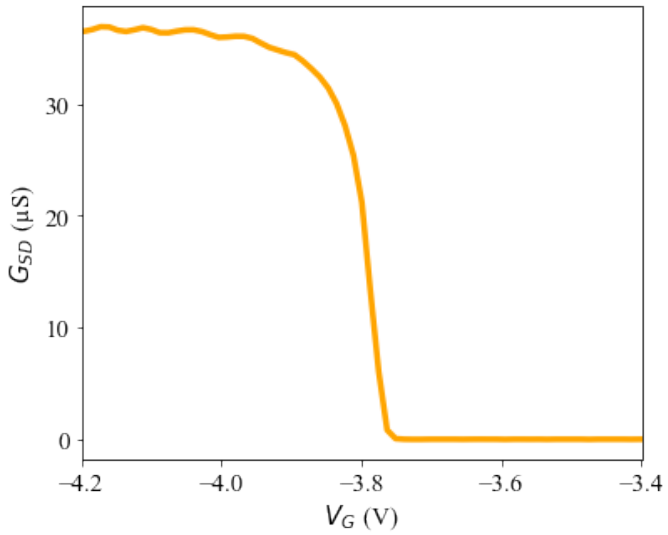

Figure 2.5: Source-Drain conductance vs. gate voltage for field effect transistors with 1 μm channel length (L_c) and channel width (W_C), turns on at around -3.8 V. This measurement was taken with the 200 μV applied bias and measured at 4 K.

surable currents, $R_c \times W$ is a constant, as expected, and R_c increases as $\frac{1}{W}$. Since our current preamplifier, which has a noise floor around 0.5 pA should easily resolve the current if R_cW remains constant, even for $W = 0.1$ μm and $W = 0.2$ μ m, we interpret the result that current cannot be detected in devices with 0.1 and 0.2 μm values for W. We attribute this to the inability for form small low-resistance ohmic contacts. One systematic difference between our process and the process in reference [34] is that annealing of the ohmic contacts, which takes place during the deposition of our insulating Al_2O_3 layer, was performed at 250 °C, the maximum temperature allowed in our atomic layer deposition system at UBC, while 300 °C was used in reference [34]. At these temperatures, Al atoms diffuse into the substrate, causing a p-doped area to form. Doping reduces the width of the Schottky barrier that carriers at low temperature experience at the semiconductor/metal interface, reducing the contact resistance. The lower temperature of our process therefore might result in a higher resistance contact.

SHTs require conductive reservoirs having a width W similar to the $\sim$ 100 nm

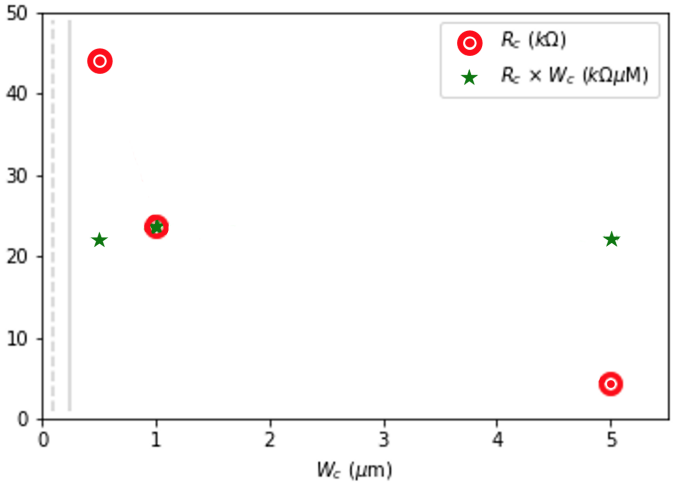

Figure 2.6: Average contact resistance (R_C) vs channel width (W_C). The channel length (L) is the same as the channel width for all devices that are measured at 4 K. Devices with $W_C = 5$, 1, and 0.5 μm show current with expected $R_c \times W_c$ behavior while devices with smaller channel width such as 250 nm and 100 nm didn't turn on. As the red dots on the graph (R_C) suggests, as the channel width decreases, the contact resistance increases.

plunger gate width. Since our nanofabrication process does not seem to produce low-resistance Aluminum ohmic contacts for $W \sim 100$ nm, we devised an alternate scheme for building $W \sim 100$ nm reservoirs using $W \sim 1$ μ m Aluminum ohmic contacts. The scheme employs an reservoir induced by an accumulation gate (Figure 2.7-b). In this scheme, an accumulation gate produces a narrow ($\sim$ 100 nm wide) conducting channel that acts as the reservoir.

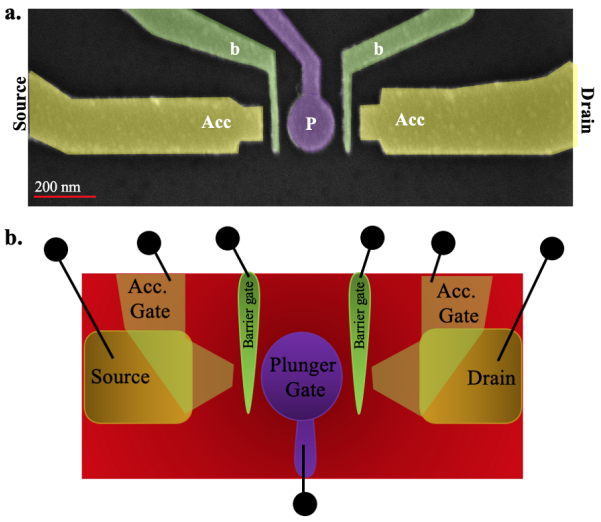

Figure 2.7: a-False-coloured SEM image of the quantum dot device with accumulation gates. The quantum dot is defined under the plunger gate P and its occupancy can be controlled by the plunger gate P. Source and drain are out of the scale of the image but they have overlap with accumulation gates from the their top layer.Barrier gates,are the green gates beside the dot for additional control. Scale bar is 200 nm, b- Schematic of the accumulation gate device, it includes wide ohmic contact and narrow accumulation gate on top of it that is placed on the same layer as the rest of the fine gates including the plunger and barriers.

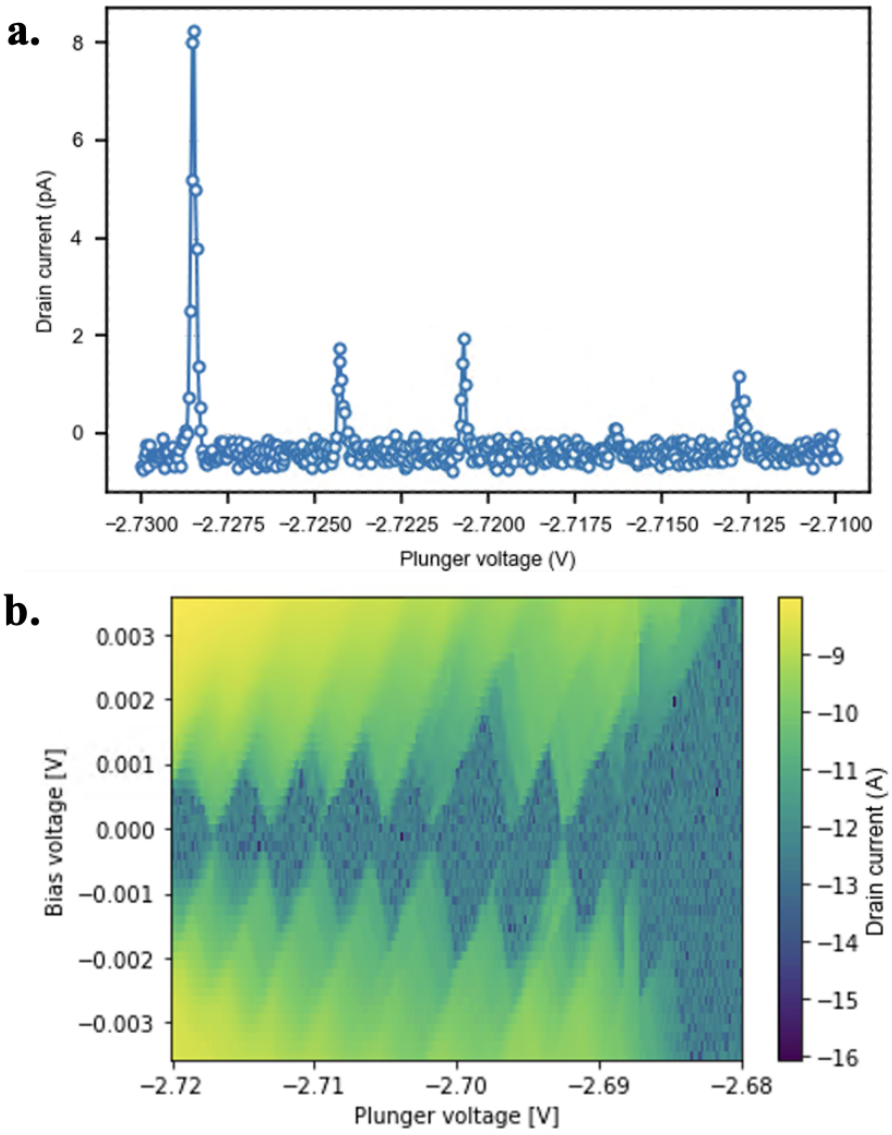

Figure 2.8: a- Transport measurements showing Coulomb oscillations as a function of voltage of the plunger gate, with $V_{acc} = -3.2V$, $V_b = -2.6V$ at low bias. Measurement has been done at 100 mk, b. Coulomb diamonds, colour plots of bias spectroscopy as a function of V_P with $E_C = 1.5meV$.

2.2.5 Ge SHT measurement

Here we present electrical transport measurements of SHT devices deviced by gate electrodes illustrated in Figure 2.7-a and b, taken at a temperature of 100 mK in a dilution refrigerator. The ohmic contacts in our design make a direct contact to the wafer, and have a width of 1.7 μm. The accumulation gates are in the same layer as the barrier and plunger gates. We verified that the gate layer is electrically isolated from the source and drain layer by the Al_2O_3 dielectric. Measurements of the current flowing in the device were performed using so-called 1D and 2D sweeps. In 1D sweeps, one voltage is varied, and current flowing from source to drain is measured. In 2D sweeps, two voltages are varied independently, and the current is measured.

Our aim with these measurements is to find the Coulomb blockade regime, where charges flow through the quantum dot one hole at a time[32]. In this regime, the current has discrete peaks, when the quantum dot level lines up in between the source and drain chemical potentials, and when a two dimensional sweep is performed, the so-called Coulomb diamonds appear[32]. However, it is not *a priori* known what voltages should be chosen on the accumulation gates, barrier gates, and plunger gates to observe Coulomb blockade. Hence, we used the standard approach to search for the Coulomb blockade regime. In this approach, a small fixed electrical bias $V_{ds} \sim k_B T$ is applied from source to drain, and a common voltage applied to the plunger, barrier, and reservoir gates are swept. Performing this sweep, we could immediately identify Coulomb oscillations, indicating the formation conducting reservoirs, and control of the charge one-at-a-time underneath the plunger. Once this regime is found, the reservoir gates, plunger gates, and barrier gates can be adjusted independent of each other to change the reservoir charge density, the tunneling barriers, and the number of charges in the SHT, respectively.

Figure Figure 2.8-a is a plot of the measured current I_{ds} as a function of the plunger gate voltage. It shows peaks of current that occur reproducibly when the quantum dot chemical potential aligns between the source and drain potentials, when they are held at bias $V_{ds} \sim k_B T$. These are the so-called Coulomb oscillations. The current peaks, and their near-uniform spacing in voltage, are a clear indication of the formation of a quantum dot. The regularity of the peaks indicates a single

quantum dot has formed and we can load an additional hole into the quantum dot with each oscillation. When the top gate voltage is increased and the quantum dot is depleted, the amplitude of the observed peaks is reduced and eventually vanishes. This observation can be explained with two different scenarios: one is, as the tunnelling rates to source and drain reservoirs drop too low, we can't detect the current anymore. Second, the last hole has been removed, so further reduction in gate voltage cannot remove anymore. These two scenarios can be distinguished using a charge sensor, though that is outside the scope of this thesis.

We also observed the Coulomb diamonds by performing a two dimensional sweep of the plunger gate voltage V_P and the source drain bias V_{ds}. The measurement is presented in Figure 2.8-b. We observe sequences of diamond-like regions, approximately periodic in the plunger gate voltage, where no current flow through the device can be detected. In this region, the number of charges on the device is fixed, so no current flows. This is the Coulomb blockade region. Above and below the diamonds, a non-zero current flows of order 1 pA to 1 nA. In this region, a net current flows through the SHT by sequential tunneling of holes onto the quantum dot, from a reservoir, and off the quantum dot, to the opposite reservoir.

By looking at the geometry of the Coulomb diamonds, we can characterize the key parameters of the system, the addition energy that must be supplied to place an additional hole into the quantum dot, and the coupling of the energy of the quantum dot to the voltage on the gates. The coupling is defined by a lever arm $\alpha = \frac{C_{gate}}{C}$ in $\frac{meV}{mV}$, where C_{gate} is the capacitive coupling between the gate and the quantum dot, and C is self-capacitance of the quantum dot, that is, the sum of its capacitances to all other electrical conductors in the system as it is shown in Figure 2.2. The lever arm indicates how strongly the plunger gate is coupled to the quantum dot. Moreover α has the relation of $\alpha\Delta V_P = \Delta E$ [33, 49] where ΔE is the addition energy. Looking at Figure 2.8-a, it shows the 1D scan of the plunger gate that we can deduce ΔV_P from. Figure 2.8-b shows a 2D scan of the plunger gate and the source-drain voltage that gives us α_P. From the height and width of these diamonds, the lever arm of the corresponding gate α can be extracted. In the regime shown here ($V_{acc1} = V_{acc2} = -3.2V$ and $V_{b1} = V_{b2} = -2.6V$), we find $\alpha_P \approx 0.3$ and from the Coulomb oscillations, and using the calculated valued of the α, $\Delta E \approx 1.5meV$. While our charging energy ΔE is similar to previous reports, our

lever arm is almost ten times larger than in previous reports [34]. Additional studies would be required to deduce why our coupling is higher than previous reports. One possible explanation for the larger coupling of our plunger gate to the formed quantum dot is a reduced capacitance of the quantum dot to the reservoirs, which could be caused by two effects. First, the accumulated reservoir could have a lower density of holes than the diffused reservoirs, which could lower capacitance of the quantum dot to the reservoirs. Second, the presence of the barrier gates between the plunger and the accumulated reservoirs in our single-layer gate design could reduce the capacitance to the source and drain.

2.3 Conclusion

We devised an accumulation mode quantum dot based single-hole-transistor (SHT) on an undoped germanium quantum well wafer, with all of the gates in a single layer. This is advantageous because it is simpler to build than the previously reported accumulation mode devices, which had two layers of gates [34]. This was accomplished by placing the barrier gates in the same layer as the plunger gates and reservoirs, instead of placing them on the second layer. The trade-off is that the reservoir and gate layers are slightly farther apart within the single layer, however, this is somewhat mitigated because having all of the gates on the same layer means that no errors from layer alignment are incurred. We find that the device functions as a quantum dot with appropriate tunneling barriers to observe Coulomb blockade and electronic transport, at low temperature. Our devices have a stronger coupling of the gate to individual holes in the SHT, compared to a previously reported two-layer design for SHT devices on identical Ge wafers. The single gate layer design is advantageous because it has fewer processing steps and there is no requirement to align one gate layer to another.

Chapter 3

Cryogenic High-Frequency Readout and Control Platform for Few-Qubit Devices

The perfect purity of the air, the unequaled beauty of the sky, the imposing sight of a high mountain range, the quiet and restfulness of the place—all around contributed to make the conditions for scientific observation ideal. — NIKOLA TESLA

3.1 Introduction

Electronic devices enabling coherent manipulation and readout of quantum information encoded in spin degree of freedom of single electrons have recently gained momentum as a promising platform to build scalable quantum computers [20, 33, 44, 55]. These devices are operated at cryogenic temperatures below 4 K, where trapping single electrons in devices and manipulating their spin can now readily be accomplished, and qubit coherence times are suitably long. Operation of these devices further requires low-frequency voltage control, fast voltage pulses with $\sim$ 100 ns to $\sim$ 10 ns duration, modulated microwave signals to control qubits with carrier frequencies typically between 4 to 20 GHz, depending on the technology, and modulation bandwidths around 100 MHz[47, 74]. In addition to this, ei-

ther modulated radio-frequency ($\sim$ 500 MHz) or modulated microwave-frequency (4 GHz to 8 GHz) microwave tones are used for qubit readout. At present an evolution is underway from single-qubit circuits that have demonstrated state preparation, qubit control[28, 47, 70, 74], and qubit readout [4, 9, 32, 63], to multi-qubit devices needed to entangle qubits, which is require to perform computation via the parallel operation of several quantum gates [36, 56, 69, 97, 105].

Scaling from single to few qubits, in addition to the presenting scientific challenges, also requires technical advances such as the development of new apparatus for qubit readout, control, and noise mitigation [19, 37]. The electronic devices, once fabricated on chips, are diced and glued to a printed circuit board (PCB) having both low-frequency connector and high-frequency 50-ohm connectors such as SMA or SMP connectors. The PCBs can be mounted within a shielded metal enclosure (box), and for certain technologies, the box should not have electromagnetic modes in the range of operation frequencies of the qubit, which can present new modes for dissipation and decoherence[85] that are detrimental for device operation. Another problem that must be avoided is microwave crosstalk between the control lines, since it would reduce the accuracy of qubit manipulation. Both the cross-talk and suppression of the resonant modes must be maintained as the number of low-frequency and microwave lines increases[58], requiring careful engineering of the PCB and enclosure. The presence of resonant modes can make it hard to identify the resonance of cavities used for qubit readout. The sample holder box and PCB should be small enough in size to be mounted within typical cryogenic operating environments, such as within the bore of a superconducting magnet mounted in a dilution refrigerator that reaches 0.1 K, or within a compact cryostat for reaching 4 K.

Crosstalk between control signals presents a challenge for few qubit devices because it has the effect of increasing error rates for single qubit operations and opening new channels for decoherence in multi-qubit circuits. Crosstalk causes a signal intended to control just a single qubit to leak onto the control line of another qubit, and influence its behaviour. This crosstalk must be avoided both for the fast voltage pulses with nanosecond rise-times, and modulated microwave tones; the presence of both of these signals somewhat resembles a mixed-signal environment in which digital logic circuits can interfere with sensitive analog systems

[92]. Maintaining a high degree of readout and control signal fidelity under these conditions is necessary so that qubit circuits can be manipulated with sufficiently low errors required for quantum computer operation, and in the future, error corrected quantum computation[76]. Today, a clean design for the sample enclosure and PCB is essential to characterize quantum hardware.

Many of these technical challenges are not unique to quantum devices and are common place in the context of commercial monolithic microwave integrated circuit (MMIC) implementation and packaging. In contrast however, interconnect solutions for spin-qubit device development require cryogenic and high magnetic field operation together with a flexibility that allows for the many iterations of a design, fabrication, and measurement cycle. For instance, interconnects are required to accommodate the regular changing of sample chips of different size and bonding configuration. Quantum coherent circuits are also different to typical MMIC architectures in the sense that they can be sensitive to very broadband noise and interference (hertz to terahertz) which increases the device temperature and, when strong enough, can artificially drive transitions between qubit energy levels [31], lead to photon assisted tunnelling [48], or create bias currents from rectification [93]. For spin qubits, even small amplitude noise or crosstalk (of the order of 100 nV) reduces the fidelity of quantum gate operations by introducing uncontrolled fluctuations of the electron potential defined electrostatically using metallic surface electrodes.

Here we report a chip carrier, including a sampler holder PCB and enclosure, with the necessary connectors to control and read out up to four qubits at cryogenic temperatures. Our PCB is a simple 2-layer design that a diced chip containing the qubit devices can be mounted on. The PCB has 24 low frequency lines, whose bandwidth is defined by filters located elsewhere in the cryostat, as well as microwave signal lines implemented as grounded coplaner waveguides (grounded-CPW) with 50 Ω impedance; recall that grounded CPWs have a centre conductor, a ground layer in the plane, and a separate ground plane. The centre conductor of the waveguides are isolated from eachother using vias from the top to the bottom ground plane. Using ground planes and a dense array of vias we try to manipulate the crosstalk between the MW lines. The PCB is mounted on the oxygen-free copper holder (cold finger) that is also operating as a shield to reduce radiation

incident on the sample. The shielded carrier itself has a small 3D cavity inside it with dimensions 1.9 cm $\times$ 3.5 cm $\times$ 0.7 cm, whose first resonant frequency is above $\sim$7 GHz, and which can be shifted further by a small conducting insert. Such resonances might be excited by narrowband radiation incident from the microwave connectors, or broadband Johnson noise emitted by amplifiers or sources. Our cryogenic holder is small enough, with physical dimensions 3.1 cm $\times$ 2.2 cm $\times$ 8.1 cm to fit within the bore of a 50 mm diameter superconducting solenoid. This is advantageous for qubits that require applied magnetic fields, such as spin qubits, or Majorana qubits. Our design also fits within smaller liquid He cryostats. This is advantageous because it is desired to screen devices within a simple cryostat, which typically have a small sample space, before a long measurement is carried out in a dilution refrigerator.

Importantly, we have made the design for the enclosure, two-layer PCB, and parts list freely downloadable on the internet [1]. The aim of doing this is to reduce the barrier to entry for other research groups who are transitioning to multi-qubit devices. We note that while commercially available holders exist from start-up quantum computing companies such as QDevil [2] , the commercially available holders do not have all of the following properties of interest for spin qubit research with superconducting components. These are: many low-frequency lines, small footprint to fit within a small cryostat or solenoid, large numbers of microwave lines, management of microwave modes in a 3D cavity, and importantly, they are not customizable by the user.

The first planned use of our carrier outside our own group's experiments is as the test fixture to be used by $\sim$ 25 participants in a workshop on the design, fabricate, and test superconducting circuits in a commercial foundry. This workshop [3] , held in July 2021, was organized by the Canadian Microelectronic Consortium, the University of British Columbia, The University of Victoria, and The Université de Sherbrooke, as part of NSERC collaborative research, training, and education (CREATE) grants in quantum computing. To our knowledge, this was the world's first workshop where students design, fabricate, and test superconducting circuits, and it resulted in the creation of the world's first superconducting multi-project wafer.

Characterizing our carrier, we present microwave scattering parameter mea-

surements to determine the level of crosstalk and the frequency of the lowest resonance both at room temperature and cryogenic temperatures, losses of the simple FR4 PCB at low temperature, and in addition, room-temperature measurements of the enclosure without the PCB. We anticipate that the results reported here are of general interest for experiments that involve high-frequency measurements of nanoscale devices at cryogenic temperatures.

In Section 3.2 we further discuss the importance of reducing crosstalk. We then discuss our design, and present the above described measurements, in Section 3.3.1 and Section 3.3.2.

3.2 Crosstalk and Resonances

One common source of errors within a quantum processor is the unintended manipulation of qubits through crosstalk. Because crosstalk comes from signal leakage, rather than a random process, it can be particularly problematic for certain error correction protocols which assume that qubit errors are not spatially correlated [18, 68]. When crosstalk is unmitigated or uncompensated, it compromises the accuracy of quantum control and readout, degrading the ability to precisely control a qubit's trajectory around the Bloch sphere [88]. Suppressing crosstalk through the use of established electronic engineering techniques must be a key consideration in the design of any quantum processor if it is to reach the low hardware error thresholds required for quantum error correction [79].

Crosstalk typically results from unmitigated electromagnetic coupling between electrical lines and thus becomes increasingly problematic as the number of qubit interconnects is increased or where their density is necessarily high. Crosstalk can occur on the chip itself, and the printed circuit board that holds the chip. Here we focus on the design of the PCB, where high and low frequency signals travel, eventually reaching bond pads, and which may also incorporate filtering or other functionality such as bias tees and matching circuits [60, 81]. Design of chips for low crosstalk is not studied in this thesis. While technical improvements in control pulse transmission [12] and dynamically corrected gate operations [103] may allow increased control accuracy crosstalk, they are also outside the scope of this thesis, and they add an undesirable complexity burden.

3.3 Measurement Setup

Figure 3.1 shows the schematic of our measurement setup for the carrier, including the low-frequency lines in the cryostat (red, blue and purple lines) and the high frequency lines (green lines) for control and measurement. Here, we use this setup to characterize the carrier.

We characterize the microwave performance of the carrier using a vector network analyzer (VNA). Signals generated by the VNA are attenuated by 50 dB to suppress thermal radiation. The microwave switches enable us to test different combinations of SMP connectors on the carrier, in the signal path shown in Figure 3.1, which has a low noise amplifier (Low Noise Factory) operating from 4 GHz to 8 GHz with a gain of 40 dB and a noise temperature of around ~ 2 K, mounted on the 4 K stage. We have two circulators (configured as isolators with one port terminated on 50 Ω) for the output line on the mixing chamber to prevent the thermal noise coming from the low noise amplifier (LNA). After amplification by the LNA, the signal is collected by the VNA.

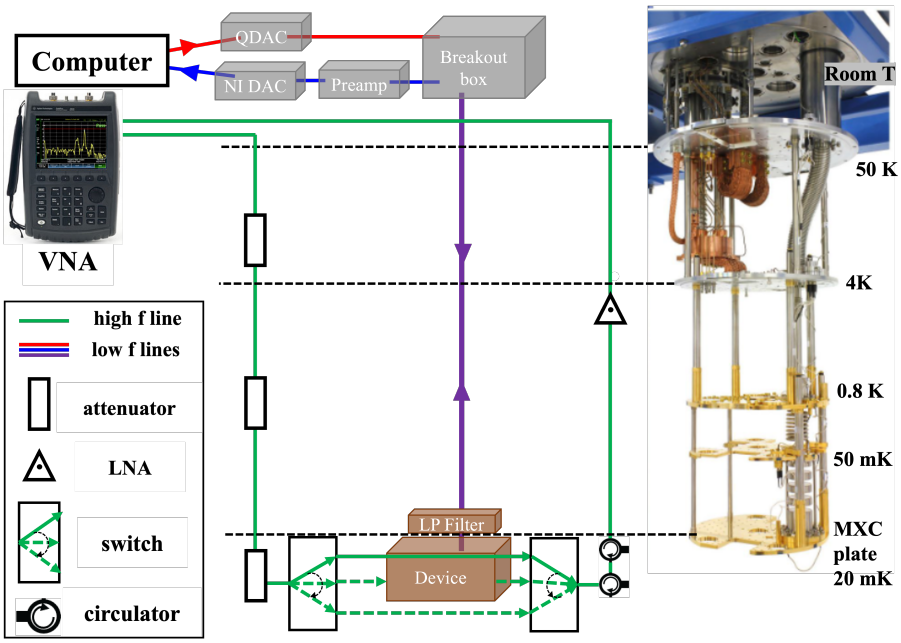

Figure 3.1: For the high frequency measurement setup, to characterize the MW performance of the carrier. The VNA generates a signal at room temperature which is attenuated by 50 dB using attenuators on each stage of the dilution refrigerator to suppress noise from broadband thermal radiation. Then the signal propagates through switches that enable testing different combination of SMP connectors on the sample carrier mounted on the MXC plate. The output signal of the sample holder is sent to circulators at MXC to prevent the thermal noise coming from the LNA. This signal is amplied by the LNA at 4K and is collected by the VNA at room temperature. Voltages with low signal bandwidth are generated by a high-accuracy low-noise digital to analog converter with $\sim 1\mu V$ accuracy. The current flowing through the device is measured by a low-noise high-accuracy current pre-amplifier, whose output is digitized by an analog-to-digital converter. Both the applied voltages and current are combined into a single multi-conductor cable using a breakout box. The low-frequency is a loom of twisted pairs, and the signals on it pass through a low-pass filter (mounted on the MXC plate) with a bandwidth of $\sim$ 100 kHz to remove broadband thermal noise, before reaching the connector of the sample carrier.

In the next few sections We discuss the details of the design and report the

performance of this platform, including signal integrity, crosstalk measurements, and characterization of resonances.

3.3.1 Design

For the enclosure, we choose the material Oxygen Free Copper which is commonly used in ultra-low temperature experiments because of its very high electrical and thermal conductivity at ultra-low temperatures. The high thermal conductivity is important in order to achieve excellent thermal anchoring of the sample to the mixing chamber. The enclosure has a bottom plate, that the PCB is mounted on using M2 brass machine screws. The top plate screws onto the bottom plate using M4 brass machine screws, and the action of tightening these screws presses the PCB against both the bottom and top plates, to improve thermal anchoring. That carrier has 8 SMP microwave connectors that work up to 18 GHz and with 50-ohm impedance. For the low-frequency connector, we use for convenience a micro-D connector with 25 pins, because it mates with the stock wiring of our cryostat and our home-made low-pass filters. The bias tees has thin film capacitors and metal film resistors that work well at low temperatures. This accommodate the needs to add a microwave signal to one of the gates that is designed for low frequency signal around the qubit if needed.

As mentioned earlier, the inside of the enclosure is actually a 3D cavity with dimensions 35 mm $\times$ 19 mm $\times$ 7 mm, highlighted in red in Figure 3.2. Assuming the enclosure acts like a rectangular cavity with perfectly conducting walls and lossless dielectric, Equation 3.1 gives its resonant frequencies, where a, b, and d are the dimensions of the cavity, and integers m, n, and p denote the mode number.

$$f_c = \frac{1}{2\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2 + \left(\frac{p}{d}\right)^2} \tag{3.1}$$

Here, μ and ε are the permeability and permittivity of vacuum. The choice of $m = n = 1$ and $p = 0$ gives the first resonance at 8.9 GHz. We compare this to the measured value of the resonance. This result could also been studied and compared to electromagnetic simulation of maxwell's equations for the box with all its geometrical features included.

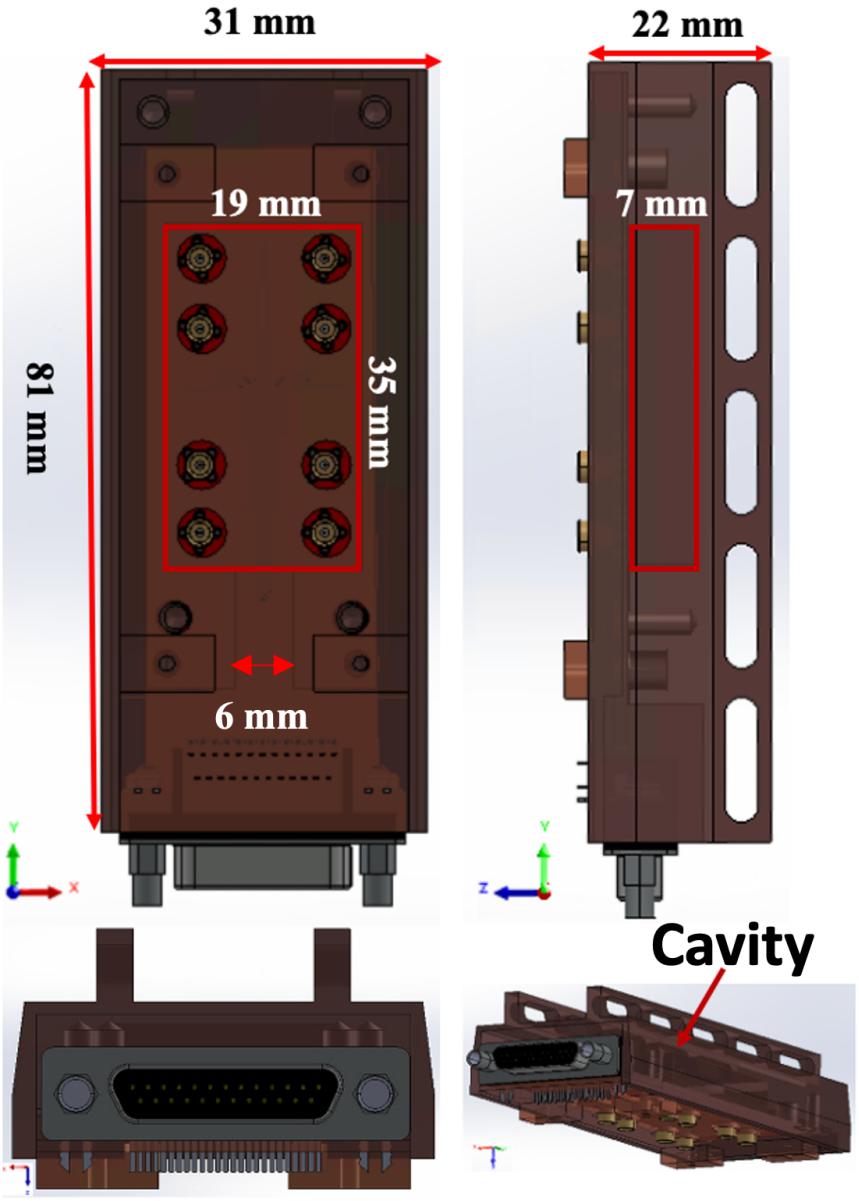

Figure 3.2: Image of the cold finger design, with capacity of carrying 8 MW and 24 DC lines including a small 35 mm $\times$19 mm $\times$ 7 mm cavity and 6 mm width, 1 mm tall gap for routing DC signals.

Table 3.1: Parts list for the PCB. SMT = surface mount

Part Name	Manufacturer	Part Number
1Mohm SMD thin film resistor	Vishay Beyschlag	MCS04020C1004FE000
100 nF SMD ceramic capacitor	KEMET	C0402C104K8PAC7867
Micro D Sub connector (25 pin)	NorComp	381-025-112L565
SMP male thru hole	Pasternack	PE44966

3.3.2 Printed Circuit board

For simplicity, we chose FR4 for the PCB material. While FR4 is lossy at room temperature, it can be adequate at 1 K and lower temperature. MW pads were distributed symmetrically around the device (Figure 3.4). To obtain a 50 Ω impedance, we assumed a relatively dielectric constant of 4.4 for the FR4, and used a width of $W = 0.8$ mm and spacing of $s = 0.127$ mm for the grounded CPW with the 1.0 mm thick PCB. These dimensions are readily achieved by low-cost PCB manufacturers. As is appears from Figure 3.3, the dimensions of the PCB are 72 mm $\times$ 24 mm.

To reduce crosstalk as much as possible, we distributed the SMP connectors and the waveguides symmetrically almost equidistantly from each other and routed the waveguides as short and as straight as possible from the SMP connectors to the bond pads, and maximizing the distance from the waveguides to the DC lines. In order to suppress parasitic modes between the ground planes on the top and bottom of the PCB, we used 0.25 mm diameter copper vias with 0.4 mm spacing to connect the top and bottom ground planes periodically.

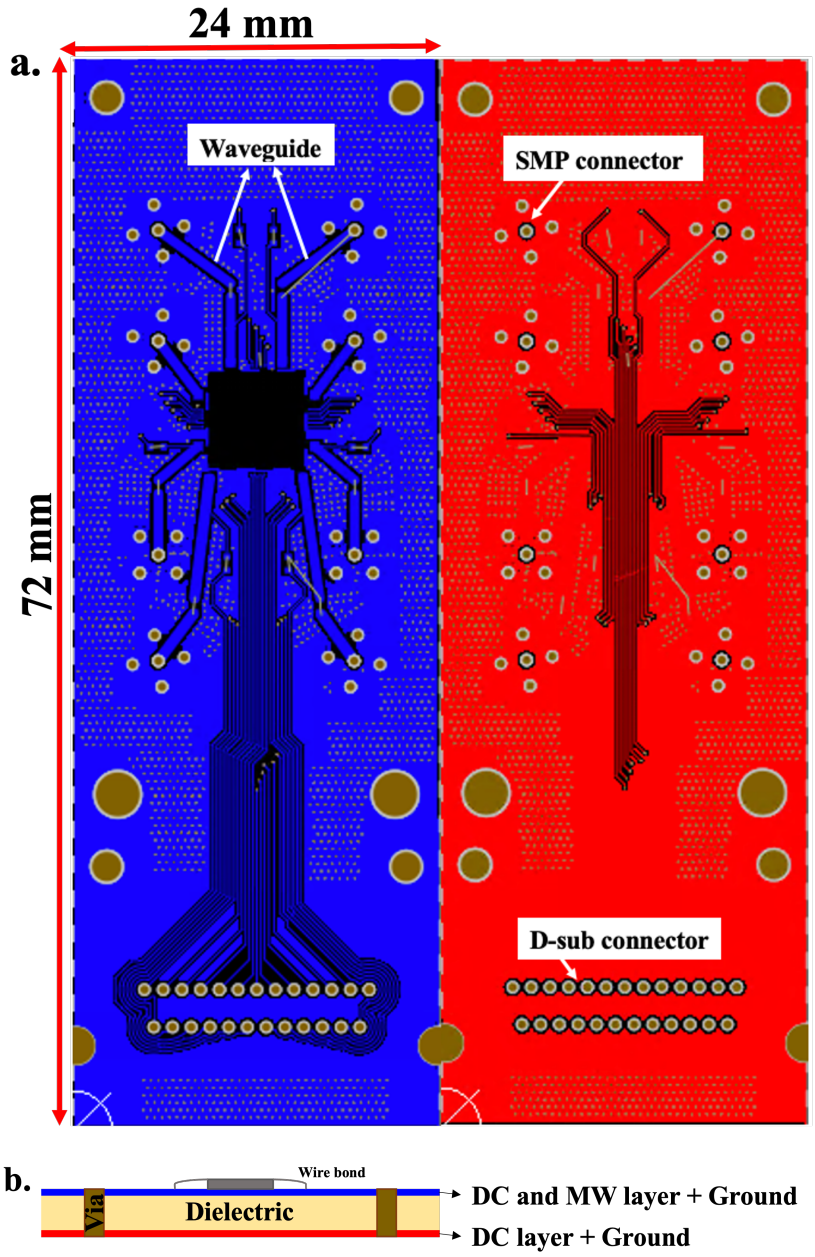

Figure 3.3: a- Two layer 2.4 $\times$ 7.2 cm^2 PCB with 8 microwave and 24 DC signal lines that are equally spread around the central area where the chip mounts, b- Schematic of signal layers of PCB including DC and MW signal and their corresponding ground layers with vias and the chip area.

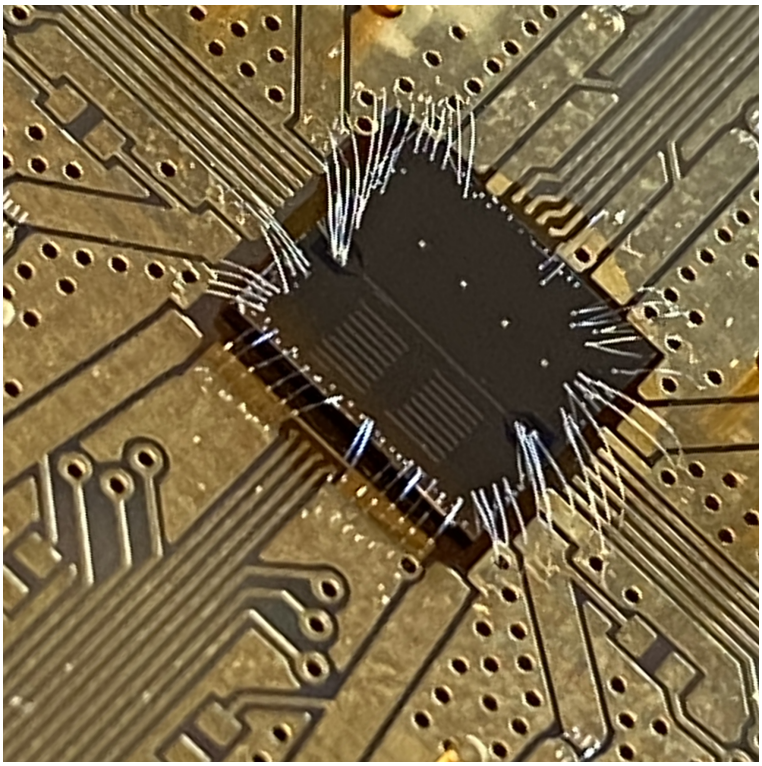

Figure 3.4: Two layer PCB with 8 microwave and 24 DC signal lines that are equally spread around the area where the chip mounts, with a mounted and wirebonded test chip containing 5 GHz microwave resonators.

3.4 Resonant modes of the Enclosure with no PCB: Room Temperature

We now present room temperature measurements of the resonant modes of the enclosure obtained using a VNA. The enclosure itself does not have SMP connectors on it, since the SMP connectors mount directly to the PCB. Consequently, there only ~ 5 mm holes on the enclosure where the SMP connectors would be, if the PCB was mounted. The resonance frequency of the enclosure was measured by carefully inserting a male SMP cable into the hole of the enclosure. We find that the first resonance happens at 6.7 GHz (Figure 3.5) that is in reasonable agreement with the calculations in Section 3.3.1.

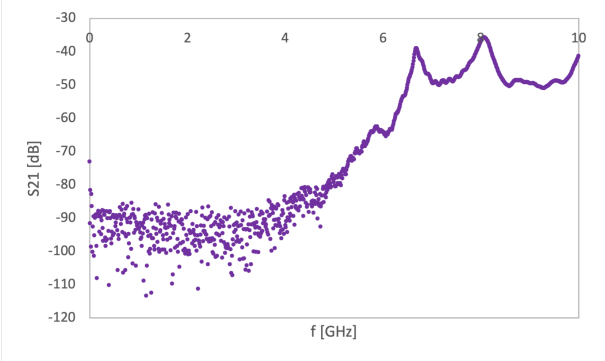

Figure 3.5: Room temperature resonance frequency detection using an S_{21} measurement for two coax cables inserted to the box through the holes designed for SMP connectors number one and two. First resonance appears at around 6.7 GHz, with a small shoulder resonance at around 6 GHz.

3.5 Crosstalk and Transmission Measurements: Room Temperature and 100 mK

With the PCB mounted inside the enclosure, the crosstalk between pairs of lines was measured using a VNA. Representative room temperature data for two of the 8 lines is shown in Figure 3.6, which remains below -40 dB for up to 8 GHz and below -30 dB up to 15 GHz. Compared to crosstalk for the box alone, the

crosstalk for the PCB and box has weak resonances between 3 GHz and 8 GHz that do not exceed -40 dB. By measuring separately the PCB, not inside the box, we found PCB resonances in this frequency range. Importantly, placing the PCB inside the box suppresses these resonances, keeping them below -40 dB, for frequencies below 8 GHz.

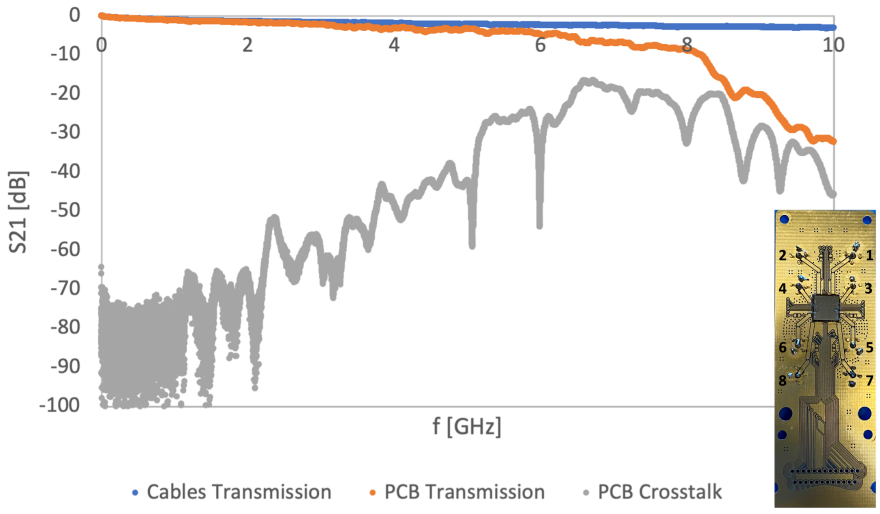

Figure 3.6: Room temperature crosstalk measurement on enclosure and PCB, between waveguides 3 and 7. Crosstalk remains below -40 dB for up to 5 GHz and below -20 dB up to 6.5 GHz. Unused ports are open circuit. Measurements on other ports showed similar behaviour. b- Image of the PCB layer. The blue line is transmission of the coaxial lines, obtained by connecting a pair of coaxial cables. The orange line is transmission of a pair of MW lines number 6 and 8 on the PCB that is obtained by connecting the MW bond pads together using multiple aluminium wire bonds.

For low temperature measurements, the PCB was mounted in the enclosure and the whole assembly was mounted inside a dilution refrigerator at base temperature. Several measurements were taken using the setup shown in Figure 3.1, using the microwave switches.

Data for crosstalk between waveguides 3 and 7 (grey curve) is shown in Figure 3.7, as observed at the VNA. The raw crosstalk measured this way is between

-50 dB and -60 dB between 3.5 GHz and 8.5 GHz which is the approximate operating frequency range of the low noise amplifier. This cross-talk must be compared to the round-trip loss of a signal to the bottom of the dilution fridge, and back out of the fridge, which was determined by removing the sample carrier from the measurement circuit and replacing it with a short section of SMA cable, using the microwave switches. We found the round-trip loss (blue curve, Figure 3.7) to be around 20 dB. This includes 10 dB of loss from CuNi semi-rigid cables and SMA connectors, and around 10 dB loss because of the difference in intentionally placed attenuators (50 dB) and the gain of the low-noise amplifier (40 dB). The actual crosstalk between lines 3 and 7 can therefore be determined by subtracting the crosstalk and round-trip loss (Figure 3.7-b): it is found to be around -30 dB and -40 dB up to 6.5 GHz, similar to the room temperature measurements. This demonstrates the effectiveness of two simple approaches of eliminating crosstalk: via fencing and manipulation of resonances by using a 3D cavity resonances. Indeed, similar strategies can be employed on-chip, where employing ground shielding between microwave signal transmission lines can reduce crosstalk [13, 92].

For completeness, the transmission through a grounded CPW on our FR4 PCB of length 2 cm (Figure 3.7 orange line) was determined through a separate measurement. In this separate measurement, waveguides 6 and 8 were shorted to eachother using multiple aluminium wirebonds, and S_{21} was measured through this circuit. Though the wire-bonds introduce an impedance discontinuity and reflections, and the PCB has losses, the transmission through the grounded CPW is difficult to distinguish from the round-trip loss of the coaxial cables in the fridge, up to around 6 GHz. We find that two relatively simple approaches of via fencing and shifting of the 3D cavity resonances enable a window of -30 dB to -40 dB of suppression of crosstalk to above 6 GHz. Indeed, similar strategies can be employed on-chip, where employing ground shielding between microwave signal transmission lines can reduce crosstalk [13, 92].

3.6 Conclusion

In conclusion, we have described a simple microwave/low frequency sample carrier based on a two layer PCB suitable for testing chips with a few spin qubits. We find

that two relatively simple approaches of via fencing and shifting of the 3D cavity resonances enable a window of -30 dB to -40 dB of suppression of crosstalk to above 6 GHz. Our design is made publicly available. The platform is well suited for the chips with different geometries and performs well at cryogenic temperatures and in the presence of magnetic fields. Crosstalk is strongly suppressed below -40 dB up to 8 GHz for transmission lines by making use of a double-layer PCB, fencing-vias, and mounting the PCB inside an enclosure that makes our design suitable for high quality microwave resonators as well. Further improvements to the crosstalk would require a better understanding of what mechanism dominates; this could be investigated by electromagnetic simulation of Maxwell's equations for the PCB and enclosure design.

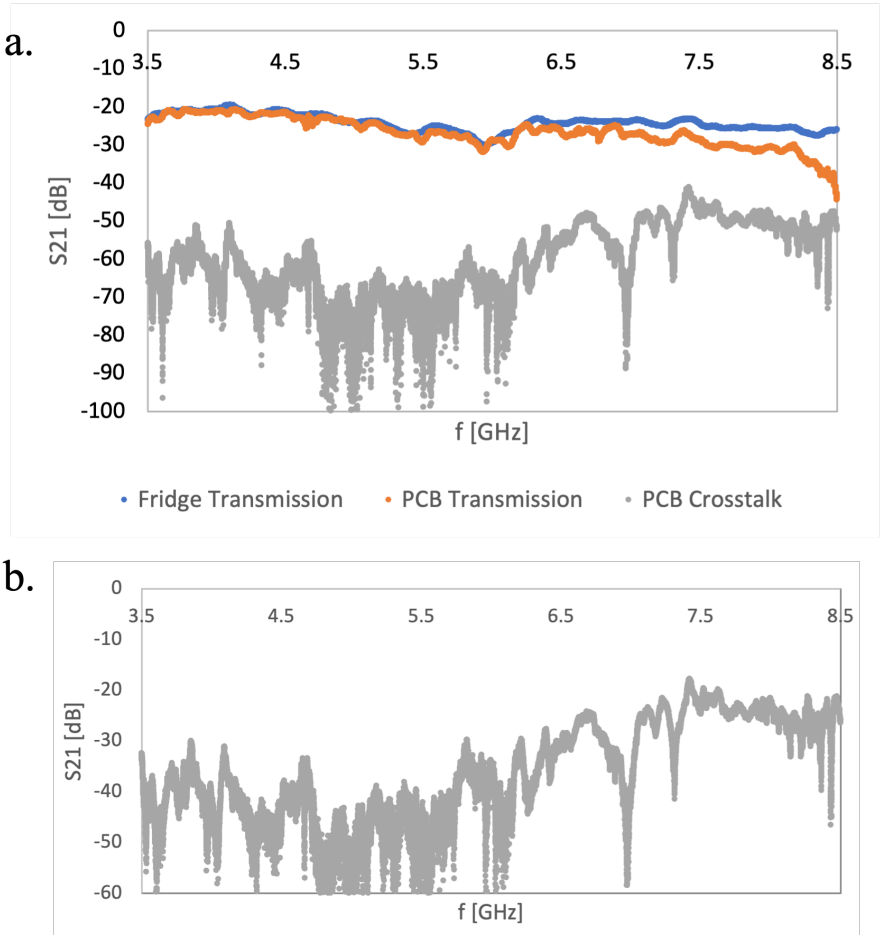

Figure 3.7: a- Crosstalk measurement at base temperature of the dilution refrigerator. The blue line is transmission of the fridge coaxial lines, obtained by connecting a pair of coaxial cables in the fridge. The orange line is transmission of a pair of MW lines number 6 and 8 on the PCB that is obtained by connecting the MW bond pads together using multiple aluminium wire bonds. Grey line is crosstalk between pair 3 and 7 of the MW signal tracks on the high-frequency layer of the PCB (image of the PCB layer shown as an inset). Crosstalk remains below -40 dB for up to 8.5 GHz that is the range of the operation of the low noise amplifier. b- Pure crosstalk graph, fridge transmission is subtracted.

Chapter 4

Conclusion

Quantum computers have the potential to perform calculations that are impossible on classical computers [66]. However, there are many challenges in the field that must be overcome to realize this goal. To date, qubits can be manipulated with error rates below 1% [6, 111]. Quantum supremacy has been shown through calculations on superconducting quantum processor who they have around 50 to 100 qubits [66] or using non-universal photonic boson samplers [116] that are deemed classically intractable. However, these NISQ computers have not yet been used to perform useful calculations that are impossible to do on classical computers. They only do small calculations that are easy to do on classical computers such as variational algorithms to calculate ground state energies for small molecules [43]. The ideal quantum hardware platform is anticipated to require quantum error correction, which, even for state-of-the-art estimates, requires scaling to around one million qubits[80, 102] or more.

There is a huge gap between one million qubits and today's 100 qubit systems, and building a quantum computer with 1 million qubits is an open challenge. Many different quantum hardware platforms exist, one of which is based on silicon technology.The technology of spin qubits based on silicon technology, that we study in this thesis, is appealing because fabrication of the devices can be accomplished with industrial fabrication processes, because the qubits have very long coherence time, and because the qubits have a very small footprint that make them scalable beyond thousands of qubits [98].

The state of the art for silicon-based qubits is two and four qubit circuits [36, 105]. However, we do not yet know the best way to scale this technology to 100 qubits and beyond. Some challenges include overcoming the impact of electric noise on single-qubit and multi-qubit circuits, and making large qubit arrays where each qubit can be individually manipulated. Hole spin qubits studied in this thesis are an attractive route for this, because they offer a number of advantages for building multi-qubit circuits. Architectures for overcoming noise and making long distant interconnects for hole spin qubits while maintaining long coherence times have recently been proposed in Si and Ge[82, 104], and demonstrated experimentally in Si[46]. A four qubit processor in Ge was recently demonstrated[36]. These recent advances make hole spin qubits an appealing candidate for scalable quantum computers.

In this work we design and test a single-layer process for hole spin qubit devices. We show that the device works, and characterize its basic properties. We also design a low-frequency and high-frequency sample carrier to test future devices. We characterize the basic properties of the apparatus.

Our nanofabrication process for the device is novel: we build an accumulation mode quantum dot device on an undoped germanium quantum well wafer, with all of the gates in a single layer. We demonstrate Coulomb blockade through a single hole quantum dot to establish its functionality, the ability to control the occupation of holes, by one hole at time. In previous work, accumulation mode quantum dot devices were implemented with a double layer gate design[34, 36]. Depletion mode devices more commonly use the single layer design for Germanium[41], so our design is as simple as the depletion mode design from a fabrication perspective.

This is advantageous as it makes the fabrication simpler and requires fewer fabrication process steps. Quantum dot devices are very sensitive systems where every fabrication step damages slightly the underlying wafer. For instance, each electron beam lithography step irradiates the chip with high energy electrons, and can cause a damage to it. As a result, reducing the number of fabrication step offers a safer route towards making a processor. Using a single layer reduces the fabrication complexity. It reduces the total number of fabrication steps and eliminates the need to align nanometer-scale gates to each-other with nanometer-scale accuracy. Our design also uses an accumulation mode reservoir, which differs from previous

work[34, 36].

We characterize the two properties of our quantum dot device, that are the addition energy and the lever arm of the plunger gate. The addition energy show the amount of energy required for changing the number of the charges inside the dot, and the lever arm of a gate shows how that gate is capacitively coupled to the quantum dot. our measurements show the addition energy of $\Delta E \approx 1.5meV$ similar to precious studies and the lever arm for the plunger gate to be high ($\alpha_P \approx 0.3$) compared to previous reports [34]. This can be beneficial as it offers a stronger coupling of the gate to individual holes in the SHT which makes the number of charges inside the quantum dot controllable.

Optimizing few qubit chips and scaling beyond them requires technical advancements such as the development of new apparatus for qubit control and readout. The function of the apparatus is to enable the testing of qubit chips that are fabricated on small semiconductor chips, enabling them to be mounted to a PCB that allows both low-frequency and high frequency signals to control and measure the devices. The PCBs is mounted within a shielded metal enclosure (box). The box should not have electromagnetic modes in the range of operation frequencies of the qubit or readout resonators, since those are detrimental for device operation.

Commercially available sample holders have either lots of DC and RF signal lines and with no MW line, or lots of MW lines and no Dc. Neither of the available options are customizable. This work offers a PCB and a holder box that are customizable and are publicly available. Our sample carrier has 8 MW waveguides implemented as grounded-CPWs isolated from eachother using via fences, and 24 DC signal lines. The number of DC lines could be increased using a high density connector. The design is based on simple two-layer PCB suitable for testing chips with a few spin qubits. It is a small 2.4 mm $\times$ 7.2 mm PCB with the commonly used FR4 as its dielectric material known to have adequate microwave performance to around 10 GHz at low temperature. Our holder box is a 8.1 cm $\times$ cm 3.1 $\times$ 2.2 cm with a small 3.5 cm $\times$ 1.9 cm $\times$ 0.7 cm cavity. The material for the holder box is oxygen free copper which is a good electrical and thermal conductor. Our carrier was designed to fit inside a small solenoid or a compact cryostat. Often the same chip is measured in two different cryostats. For instance, one can be measured quickly to screen if the basic capabilities are there, in a simple cryostat, and

then moved to a dilution refrigerator on for longer-term experiments. It is highly desirable if the same chip carrier can be used in both cases.

We measure the 3D electromagnetic resonances for the enclosure, at around 6.7 GHz and resonances for the PCB at around 8 GHz. When our PCB is mounted within the the enclosure, we observe a crosstalk between waveguides of around -40 dB for frequencies 3.5 GHz to 8.5 GHz, which is adequate for quantum experiments. Future improvements could involve ? Box part: metal insert that makes the cavity directly around the chip, with openings for the waveguides, to shift the modes. Lower crosstalk on PCB: investigate where the crosstalk originates from using electromagnetic simulation of maxwell's equations. However, this is a very demanding simulation, because of properties of the metal, NbTiN, complex geometry of the printed circuit board with via array of vias inside the coldfinger box. As a result, the apparatus is well suited for qubit control and for high quality microwave resonators for measurement at cryogenic temperatures and in the presence of magnetic fields.

Adopting the proposed methodology for quantum dot fabrication, future work will evaluate the properties of single qubit and double qubit devices. This would involve experiments demonstrating fast and accurate readout, and fast and accurate qubit control. This could result in a scaled simulator hardware that could effectively be used for simulating quantum materials. The sample carrier that we have designed can be scaled to larger number of qubits, possibly up to 10 or 20. However, beyond 10 to 20 qubits, a completely different design might be necessary.

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Appendix A

Device Fabrication

A.1 Fabrication Process Overview

In this appendix, we describe the detailed fabrication process for a single quantum dot on Germanium heterostructure shown in Figure A.1.

A.2 Chip Preparation

Sample chips are cleaved from a large wafer using a dicer machine to 6×6 small chips.

Next step is chip cleaning so to make sure that the surface is free of junk that includes following steps:

- 10 minutes in 70°C acetone
- 3 seconds sonication
- Nitrogen blow dry

A.3 Marker Layer

Marker layer is required as our fabrication process include multiple steps that they require to be aligned. Fabricating this layer includes following steps:

- Spin-coat: bi-layer A4-495, and A2-950 at spin coater with 4000 rpm speed, and 1000 rpm/sec acceleration for 45 seconds, and finally baking it at 180°C for 4 min
- Electron beam lithography, with dose 1200 $\frac{mJ}{cm^2}$
- Developing sample at room T for 40 seconds in IPA+DI water (7:3 ratio)
- 10 seconds oxygen plasma
- Deposit: 5/55 nm Ti/Pd nm with the rate 1.2/2 $\AA$/s using DeeDirector
- Liftoff: 10 min in acetone at 70°C, 2 seconds sonication, IPA rinse, and blow dry

A.4 Ohmic Layer

- Spin-coat: bi-layer A4-495, and A2-950 at spin coater with 4000 rpm speed, and 1000 rpm/sec acceleration for 45 seconds, and finally baking it at 180°C for 4 min
- Electron beam lithography, with dose 1200 $\frac{mJ}{cm^2}$
- Developing sample at room T in IPA+DI water (7:3 ration) for 50 seconds with agitation, and blow dry
- 30 seconds oxygen plasma
- Etching in buffer HF for 15 seconds and then 5 minutes in DI water, and next blow dry it
- Deposit: 30 nm Al with rate 2 $\AA$/s using AJA
- Liftoff: 5 minutes in NMP at 70°C, 5 min in acetone 70°, 3 seconds ultrasound, IPA rinse, and blow dry
- Deposit 20 nm Al_2O_3 at 150°C using ALD

A.5 Fine Gates Layer

- Spin-coat: bi-layer 495 PMMA A2 at spin coater with 5500 rpm speed, and 2000 rpm/sec acceleration for 45 seconds, and baking it at 180°C for 4 min, then 950 PMMA A1 at spin coater with 3300 rpm speed, and 2000 rpm/sec acceleration for 45 seconds, and baking it at 180°C for 4 min
- Electron beam lithography, with dose 2000 $\frac{mJ}{cm^2}$
- Developing sample at 4°C for 40 seconds in IPA+DI water (7:3 ratio), and then blow dry it
- Deposit: 4/16 nm Ti/Pd nm with the rate 1.3/1.3 $\AA$/s using DeeDirector
- Liftoff: 15 min in acetone at 70°C, 5 seconds sonication, IPA rinse, and blow dry

A.6 Large Gates Layer

- Spin-coat: bi-layer A4-495, and A2-950 at spin coater with 4000 rpm speed, and 1000 rpm/sec acceleration for 45 seconds, and finally baking it at 180°C for 4 min
- Electron beam lithography, with dose 1000 $\frac{mJ}{cm^2}$
- Developing sample at room T for 30 seconds in IPA+DI water (7:3 ratio), and then blow dry it
- Deposit: 5/80 nm Ti/Pd nm with the rate 1.2/2.2 $\AA$/s using DeeDirector
- Liftoff: 12 min in acetone at 70°C, IPA rinse, and blow dry

A.7 Bond-Pad Etching Layer

- Spin-coat: bi-layer A4-495, and A2-950 at spin coater with 4000 rpm speed, and 1000 rpm/sec acceleration for 45 seconds, and finally baking it at 180°C for 4 min

- Electron beam lithography to open a $95 \times 95\ \mu^2$ window on the ohmic bond-pads with dose 1000 $\frac{mJ}{cm^2}$
- Developing sample at room T for 30 seconds in IPA+DI water (7:3 ratio), and then blow dry it
- Oxygen plasma
- Etching in buffer HF for 60 seconds and then 3 minutes in DI water, 5 minutes in acetone at 70°C, 2 minutes in IPA at 70°C, and finally blow drying the sample.

Now the sample is stored and can be mounted on the PCB to wirebond on the chip and cooling it down and measuring it.

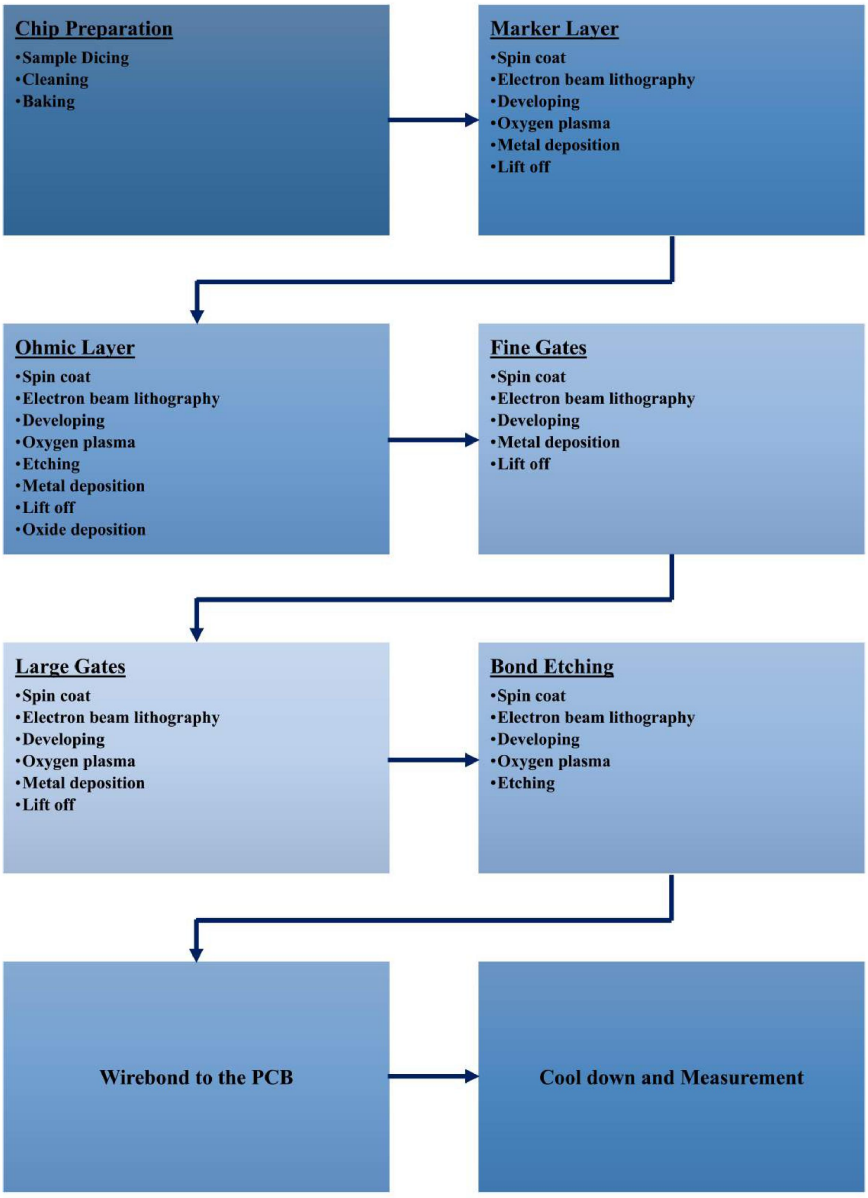

Figure A.1: The overall process of fabricating a quantum dot device.