On the Design of Low-Power Low-Voltage Circuits for Smart Stents

by

Ziyu Wang

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The following individuals certify that they have read, and recommend to the Faculty of Graduate and Postdoctoral Studies for acceptance, the thesis entitled:

On the Design of Low-Power Low-Voltage Circuits for Smart Stents

submitted by **Ziyu Wang** in partial fulfillment of the requirements for the degree of **Doctor of Philosophy** in **Electrical and Computer Engineering**.

Examining Committee:

Shahriar Mirabbasi, Electrical and Computer Engineering, UBC
Supervisor

Sudip Shekhar, Electrical and Computer Engineering, UBC
Supervisory Committee Member

Kenichi Takahata, Electrical and Computer Engineering, UBC
Supervisory Committee Member

Mu Chiao, Mechanical Engineering, UBC
University Examiner

Purang Abolmaesumi, Electrical and Computer Engineering, UBC
University Examiner

Peter Lian, Electrical and Computer Engineering, York University
External Examniner

Abstract

The main focus of this work is on the analysis and design of low-power low-voltage complementary metal-oxide-semiconductor (CMOS) integrated circuits for wirelessly powered implantable systems, in general, and with an emphasis on "Smart Stent" applications. In the context of smart stents the goal is to collect and transmit sensory data from an stent, for example the one that is implanted inside an artery or inside the ureter, for clinical diagnosis. The power for the electronic blocks on the "Smart Stent" is harvested from an optimized external radio-frequency (RF) source that enhances the local power density surrounding the implanted stent. As a proof-of-concept design, a commercially available coronary stent is used as the power receiving antenna for the circuits embedded on the implant, and the system functionality is fulfilled by customized circuit blocks implemented in a CMOS technology. Low-power low-voltage circuit blocks are designed to minimize the power consumption of the overall system, and the interface between the stent and the CMOS die is co-designed for improving the *in-vitro* power transfer efficiency. A CMOS rectifier with fully on-chip transformer-based tunable matching network is designed in a 0.13-μm CMOS process and the measurement results show that it can generate more than 500 mV DC voltage on a 2 kΩ load when the available power received by the stent is greater than -2 dBm, corresponding to 34% power conversion efficiency (PCE). An output capacitor-less low-dropout regulator (LDO) topology that can operate from a 0.58-to-0.9-V supply is also designed in the same 0.13-μm CMOS process. Furthermore, a low-power 5 GHz Class-D VCO is implemented. With 0.2-V supply voltage, only 280 μW is required by the oscillator core, and a figure of merit (FoM) of 192.5 dBc/Hz can be achieved. To validate the presented circuits and the design methodology, the operation of the

complete system that consists of a proposed multi-port external RF source and the "Smart Stent" (stent and the proposed chip) is demonstrated *in-vitro*. The results of the wireless power transfer experiments show that with 480 mW transmitting power and 53 mm separation distance, more than 350 μW is delivered to the implanted system.

Lay Summary

The main focus of this work is on the design of efficient circuits for wirelessly powered implantable systems with an emphasis on "Smart Stent" applications. The power for the electronic blocks is received from an optimized external radio-frequency (RF) source that enhances the local power density surrounding the implanted stent. As a proof-of-concept prototype, customized circuit blocks implemented using complementary metal-oxide-semiconductor (CMOS) technology are added to a commercially available coronary stent where the stent also acts as the power receiving antenna of the implant. The functionality of the system that consists of an external RF source and the "Smart Stent" (stent and the proposed chip) is demonstrated *in-vitro*. Although the proof-of-concept is validated using a coronary "Smart Stent", the systematic design methodology and the circuit design techniques are general and can be used for other types of wirelessly powered implantable systems.

Preface

All the content presented in this dissertation are original, independent work conducted in System-on-Chip (SoC) lab by the author, Ziyu Wang. The proposed techniques described in Chapter 2, 3 and 4 were designed by Ziyu Wang. Canadian Microelectronic Corporation (CMC Microsystems) provided access to the computer-aided design tools as well as access to the technology and chip manufacturing. The research was my own work and I performed the research and wrote the associated manuscripts under the supervision of Professor Shahriar Mirabbasi.

A version of Chapter 2 has been published in the following conference and journal paper:

- Z. Wang and S. Mirabbasi, "CMOS Rectifier with on-chip Transformer Coupled Tunable Matching Network for Biomedical Implants.", *in proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, May 2018.*

- Z. Wang and S. Mirabbasi, "A Low-Power CMOS Rectifier with On-Chip Matching Network and a Magnetic Field Focused Antenna for Wirelessly Powered Medical Implants." *in IEEE Transactions on Biomedical Circuits and Systems, vol.13, no.3, pp.554-565, June 2019.*

I was the leading investigator in developing the concept, designing the circuits and performing all the chip measurements. Professor S.Mirabbasi was the research supervisor and provided feedback on the work and assisted with preparing the manuscript. The work also resulted in the following journal paper:

- M. Cai, Z. Wang, Y. Luo and S. Mirabbasi,"An RF-Powered Crystal-Less Double-Mixing Receiver for Miniaturized Biomedical Implants.", *in IEEE*

Transactions on Microwave Theory and Techniques, vol. 66, no. 11, pp. 5129-5140, Nov. 2018.

Dr. Cai was the leading researcher on this work and my contributions were in theoretical analysis, helping with the design, simulation and measurement of the chip.

A version of Chapter 3 has been published in the following journal paper:

- Z. Wang and S. Mirabbasi, "A 0.58-to-0.9-V Input 0.53-V Output 2.4-μW Current-Feedback Low-Dropout Regulator with 99.8% Current Efficiency." *in IEEE Solid-State Circuits Letters, vol.3, no.3, pp.1-4, 2020.*

I was the leading investigator in developing the concept, designing the circuits and performing all the chip measurements. Professor S. Mirabbasi was the research supervisor and provided feedback on the work and assisted with preparing the manuscript.

Table of Contents

List of Tables

List of Figures

Acronyms

BGR Bandgap Reference. xvii, 13

CMOS Complementary Metal–Oxide–Semiconductor. xvii, 4

EIRP Equivalent Isotropically Radiated Power. xvii, 9

EM Electromagnetic. xvii, 8

GBW Gain-Bandwidth Product. xvii

IC Integrated Circuits. xvii, 11

IL Insertion Loss. xvii

ISF Impulse Sensitivity Function. xvii, 14

ISS Impedance Standard Substrate. xvii

LDO Low-Dropout Regulator. xvii, 12

PCB Printed Circuit Board. xvii, 11

PCE Power Conversion Efficiency. xvii, 9

PDL Power Delievered to Load. xvii

PSD Power Spectral Density. xvii

RF Radio Frequency. xvii

SAR Specific Absorption Rate. xvii, 6

SOLT Short-Open-Load-Thru. xvii

SR Slew Rate. xvii

TRL Thru-Reflect-Line. xvii

UGF Unity-Gain Frequency. xvii, 13

VCO Voltage Controlled Oscillator. xvii, 17

VNA Vector Network Analyzer. xvii

WPT Wireless Power Transfer. xvii

Acknowledgments

First and foremost, I would like to express my sincere gratitude to Prof. Shahriar Mirabbasi, for his tireless guidance and patience through my Ph.D. research and study. I couldn't have found a better supervisor anywhere in the world, and I am grateful to have had the opportunity to learn so much from him, professionally and personally.

I would like to thank Prof. Robert Sobot, for his teaching, for his encouragement and advice, and for supporting my research during the first two years in Canada.

I would also like to thank some of other incredible faculty and staff members in SoC Lab who have shaped my experience in UBC. I am grateful to Prof. Sudip Shekhar, for his teaching, for his advice, and for serving on my committee. I am especially thankful to Dr. Roberto Rosales, for helping me set up all the lab equipment and giving me advice regarding RF measurements. I also wish to thank Roozbeh Mehrabadi, for supporting all CAD tools and network.

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Finally, I would like to thank my wife, Xuejing, for her constant love, support and understanding. I would like to express my thankful to my parents, grandparents and the rest of my family. I would never have had the courage to discover a different life and pursue my dream without your love and support. This thesis is especially dedicated to my grandma, you are never far away from my heart and mind, R.I.P.

Chapter 1

Introduction

Radio Frequency (RF) telemetry has been used in implantable medical devices for monitoring crucial physiological data and transmitting information to and from the implant to an external unit for clinical diagnosis. For example, cardiovascular disease (CVD) is a group of heart and vasculature conditions which are the leading form of mortality worldwide. Blood vessels can become narrowed, restricting blood flow, and drive the majority of hearts attacks and strokes. Reactive surgical interventions are frequently required; including percutaneous coronary intervention (PCI) as shown in Fig. 1.1 and coronary artery bypass grafting (CABG). Despite successful opening of vessels and restoration of blood flow, often in-stent restenosis (ISR) and graft failure can still occur, resulting in subsequent patient morbidity and mortality. A new generation of cardiovascular implants that have sensors and real-time monitoring capabilities are being developed to combat ISR and graft failure. Self-reporting stent/graft technology could enable precision medicine-based and predictive healthcare by detecting the earliest features of disease, even before symptoms occur. Bringing an implantable medical device with wireless electronic sensing capabilities to market is complex and often obstructive undertaking [3]. The development of wireless power transfer (WPT) in the context of biomedical implants has been driven by the demand of removing (bulky) batteries to make the systems more suitable for the *in-vivo* environment as well as avoiding surgical replacement of the battery or implant when the battery life ends. However, the implementation of wirelessly powered system as illustrated in

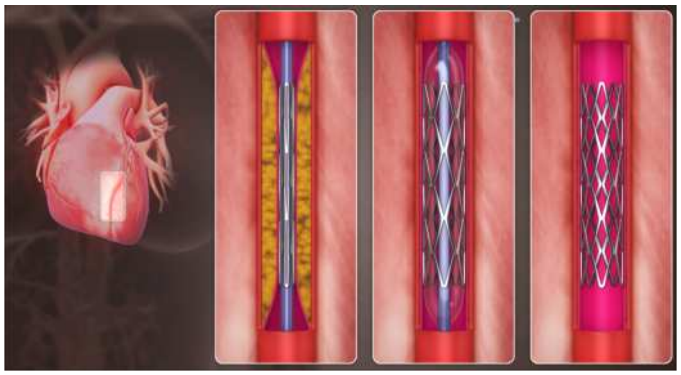


Fig. 1.1. Coronary angiogram showing stent in a coronary artery. Source: https://www.scientificanimations.com/wiki-images

Fig. 1.2 is difficult given constrains in space and energy consumption. This is par-

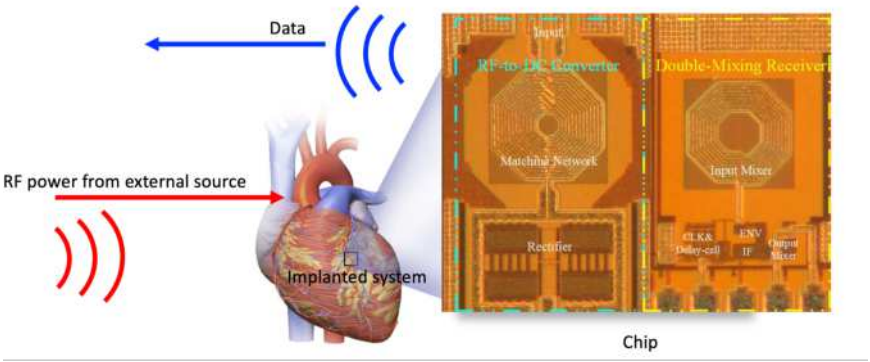


Fig. 1.2. A wirelessly powered RF telemetry implantable system. The chip micrograph is from[1].

ticularly true for coronary or other type of implantable systems that in deep-tissue, which require longer power transfer distance and the receivers at the implanted side are small.

The coupled mode theory [2, 4, 5] has been used to formalize the WPT between a source and a receiver, and the transfer phenomenon can be described by

the following equations:

$$\frac{da_S}{dt} = (j\omega_S - \gamma_S)\, a_S + \kappa a_R + F, \tag{1.1}$$

$$\frac{da_R}{dt} = (j\omega_R - \gamma_R - \gamma_L)\, a_S + \kappa a_S, \tag{1.2}$$

where a_S, a_R are normalized amplitude that are related to source and receiver, respectively. Furthermore, F represents the external excitation, κ is the coupling coefficient, ω_S and ω_R are the source and the receiver resonant frequencies, γ_S and γ_R are the intrinsic decay rates of the source and the receiver, and γ_L is the work extraction rate of the load at the receiver. If the source and the receiver are in resonance, that is $\omega = \omega_S = \omega_R$, the power transfer efficiency which is defined as the ratio of the power dissipated in the load to the total power dissipated by the system, is given as [4]:

$$\eta = \frac{\dfrac{|\kappa|^2}{\gamma_S \gamma_R} \cdot \dfrac{\gamma_L}{\gamma_R}}{(1+\dfrac{\gamma_L}{\gamma_S}) \cdot \dfrac{|\kappa|^2 + 2\,\mathrm{Re}(\kappa)^2}{\gamma_S \gamma_R} + (1+\dfrac{\gamma_L}{\gamma_S})^2}. \tag{1.3}$$

If $|\kappa| \ll 1$ the system will work in weakly-coupled region. For example, this is the case when one wirelessly transfers power to a small implant, especially if it is implanted deep inside the body (i.e., under deep biological tissues). In such cases, Eq. (1.3) can be simplified to:

$$\eta \approx \frac{|\kappa|^2}{\gamma_S \gamma_R} \cdot \frac{\dfrac{\gamma_L}{\gamma_R}}{(1+\dfrac{\gamma_L}{\gamma_R})^2} = \eta_c \cdot \eta_m, \tag{1.4}$$

where η_c is the coupling efficiency and η_m is the matching efficiency at the receiver side [5]. From Eq. (1.4) it can be seen that η_m is mainly determined by the self impedance of the receiving antenna Z_R, and the load impedance Z_L it drives. The term η_m can be maximized if conjugate matching is achieved at the receiver side. In other words, to satisfy $\frac{d\eta_m}{d(\gamma_L/\gamma_R)} = 0$, the ratio $\gamma_L/\gamma_R = 1$ hence $Z_L = {Z_R}^*$. In contrast to η_m, the coupling efficiency η_c is determined by the external source,

the implanted receiver and the medium in between. For the targeted application in this work, the medium consists of multilayer biological tissues, and the equivalent receiving antenna aperture is on the order of several millimeters. It means that in order to achieve optimum efficiency, η, an external source that yields maximum η_c is essential since the improvements that can be done at the receiving side are limited by the application requirements (for example, in terms of size and available supply voltage and power).

The focus of this research is on the design and optimization of an wirelessly powered implantable system for biomedical applications, the design and optimization problems can be divided into the following sub-categories:

i. External domain: The design and optimization of the external source to enhance η_c.
ii. Implanted domain: The design of the integrated building blocks using Complementary Metal–Oxide–Semiconductor (CMOS) technology. Low-voltage low-power techniques are used to minimize the overall system power consumption. Co-design of receiver (Rx) antenna and the antenna interface circuit to maximize η_m.

It should be noted that the external and implanted design are coupled together, therefore several design iterations are necessary to find the design parameters that will yield to global optimum η.

One type of the most commonly used external source is the wire-wound or planar coil, in which the fields generated by these coil-typed sources are quasi-magneto-static when the operating frequency is low (i.e., hundreds of kHz to tens of MHz). This is considered as an advantage for biomedical applications because magnetic fields do not interact with biological materials, and the tissue heating resulted by non-zero electrical fields are controlled by limiting the operation at low frequencies. There are many studies on WPT systems that operate in the near-field over the air [6][7][8][9][10] or across the tissue [11][12][13][14] using coils as the transmitting antenna. For these low-frequency systems, however, the power transfer efficiency drops significantly as the separation distance between the coils increases. Furthermore, η will be further degraded when the receiver dimension is (much) smaller than its depth inside the biological tissue environment. It was

shown in [5][15][16][17] that for mm-size devices that are implanted in deep tissue, optimum power transfer can be achieved in the *mid-field* (the boundary between the near and far fields) where the energy is exchanged through a combination of inductive and radiative modes. Although a popular point of view is that the higher frequency increases the tissue absorption rate and hence degrades the efficiency, this statement is only true if the displacement current is ignored [15]. However, because biological tissues are better modeled as low-loss dielectrics rather than good conductors, the displacement current in them is significant and cannot be omitted. If the tissue model is taken into account, and given that the coupling efficiency is also related to the physical fields as presented in [5], the equation for η_c in Eq. (1.4) can be re-written as [18]:

$$\eta_c = \frac{|\kappa|^2}{\gamma_S \gamma_R} = \frac{|\int d^3r \mathbf{B}_S^* \cdot \mathbf{M}_R|^2}{[\int d^3r \,\mathrm{Im}\,(\varepsilon_r(\omega))|\mathbf{E}_S|^2][\int d^3r \,\mathrm{Im}\,(\varepsilon_r(\omega))|\mathbf{E}_R|^2]}, \tag{1.5}$$

where $\mathbf{B}_S$, $\mathbf{E}_S$ are the magnetic and electric fields generated by the source, $\mathbf{M}_R$ the induced magnetization due to current in receiving antenna. The term $\varepsilon_r(\omega)$ represents the dielectric permittivity of the biological tissue, and can be expressed as in Debye relaxation model [15]:

$$\varepsilon_r(\omega) = \varepsilon_\infty + \frac{\varepsilon_{r0} - \varepsilon_\infty}{1 - j\omega\tau} + j\frac{\sigma}{\omega\varepsilon_0}, \tag{1.6}$$

where ε_{r0} and σ are the relative permittivity and conductivity at DC. The τ is the relaxation time constant, ε_∞ is the relative permittivity at frequencies $\omega \gg 1/\tau$. An important conclusion in [15] is that for a source and a small receiver separated by distance D with a biological tissue, the operating frequency that optimizes the power transfer efficiency is derived as:

$$\omega_{opt} \approx \sqrt{\frac{c\sqrt{\varepsilon_{r0}}}{\tau(\varepsilon_{r0} - \varepsilon_\infty)D}}, \tag{1.7}$$

and it implies that for typical tissue composition and implant depth, f_{opt} is above 1 GHz for small receiving coil. Therefore, the source need to be optimized at

around f_{opt}, and the field pattern it generates should maximize the RHS of Eq. (1.5). In addition, because RF power will be coupled into the tissue by the external source, the Specific Absorption Rate (SAR):

$$SAR = \frac{1}{V}\int \frac{\sigma(\mathbf{r})|\mathbf{E}_S(\mathbf{r})|^2}{\rho(\mathbf{r})}d\mathbf{r}, \tag{1.8}$$

needs to lower than the IEEE safety threshold (1.6 W/kg averaged over 1 g of tissue). In Eq. (1.8), the term V, ρ are the volume and density of the tissue, respectively. Intuitively, the electrical field component generated by the source, $\mathbf{E}_S$, should be minimized since it has negative contribution on η_c and positive contribution on SAR. Analytically, the surface current distribution $\mathbf{J}_{S,opt}$ that yields the optimum $\eta_{c,opt}$ is derived in [2]

$$\mathbf{J}_{S,opt} = \mathcal{F}^{-1}\{(\int \mathrm{Im}\,\varepsilon\, \mathcal{G}_E^*(\mathbf{k}_s,z)\mathcal{G}_E(\mathbf{k}_s,z)\,dz)^{-1}\mathcal{G}_B^*(\mathbf{k}_s,z_f)\mathbf{n}\}, \tag{1.9}$$

where $\mathcal{F}^{-1}\{\}$ represents the inverse Fourier transform in the transverse coordinates, $\mathbf{k}_s = (k_x, k_y)$, $\mathcal{G}_E(\mathbf{k}_s,z)$ and $\mathcal{G}_B(\mathbf{k}_s,z)$ are the Fourier transform of the Green's function that relates $\mathbf{E}_S$ and $\mathbf{B}_S$ to source current density $\mathbf{J}_S$. The relationship between the Green's function and the corresponding field quantity are given as:

$$\mathcal{F}\{\mathbf{E}_S(\mathbf{r})\} = \mathcal{F}\{\int d^3r'\,\mathbf{G}_E(\mathbf{r},\mathbf{r}')\cdot\mathbf{J}_S(\mathbf{r}')\} = \mathcal{G}_E(\mathbf{k}_s,z)\,\mathcal{J}_S(\mathbf{k}_s), \tag{1.10}$$

$$\mathcal{F}\{\mathbf{B}_S(\mathbf{r})\} = \mathcal{F}\{\int d^3r'\,\mathbf{G}_B(\mathbf{r},\mathbf{r}')\cdot\mathbf{J}_S(\mathbf{r}')\} = \mathcal{G}_B(\mathbf{k}_s,z)\,\mathcal{J}_S(\mathbf{k}_s), \tag{1.11}$$

where $\mathbf{r}'$ is the coordinate of a point source and $\mathbf{r}$ is that of a target point. In fact, the optimal source current distribution given in Eq. (1.9) only shows the theoretical solution, however, does not yield a physical source representation directly. Nonetheless, it gives the insight on how to synthesis the optimal source. Specifically, as shown in Fig. 1.3, if the source has following features:

i. The current has opposite direction with respect to the x-axis;
ii. The dominant current paths have semi-circular shape;
iii. The spacing between the current paths is approximately half wavelength;
iv. The phase difference between adjacent semi-circular current paths is roughly

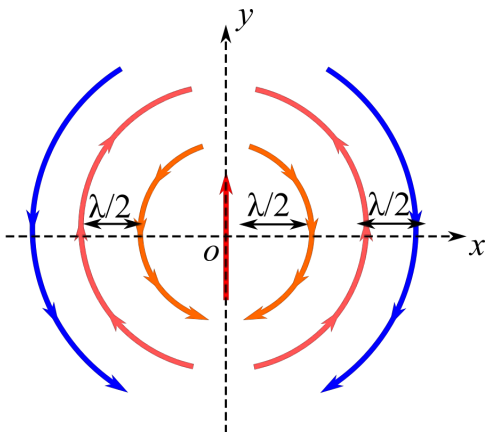


Fig. 1.3. Theoretical optimal source current distribution $\mathbf{J}_{S,opt}$ derived in [2]

180°;

v. The magnitude of the current decays exponentially with radial distance,

the magnetic field component $\mathbf{B}_S$ will be focused around the target point inside the tissue whereas $\mathbf{E}_S$ is suppressed. Although only a simplified version of the optimum source is realized in the form of a four-element slot-array in [2][18], the overall link η is increased by a factor of 4 compared with the conventional coil-based external source.

At the implanted side, the performance of the receiving antenna is usually limited by the small available area and thus it cannot be improved dramatically. Previous works [19][20][21] show the possibility of using a medical stent as the antenna in an implantable "smart stent" system to monitor and potentially prevent restenosis (i.e., re-narrowing of artery at the stent site) [22][23]. Stents are being used in variety of applications. Here, we focus on vascular stents where the stent is placed in the artery as part of a procedure called percutaneous coronary intervention (PCI), also known as coronary angioplasty, to support the inner wall of the artery and keep the lumen open. Other types of stents such as ureteral stents [24, 25] as illustrated in Fig. 1.4 are used to restore the urine flow between the kidney and the bladder in the treatment or prevention of urinary tract obstruction, and pancreatic and biliary stents [26] provide pancreatic and bile drainage from the gallbladder, pancreas, and bile ducts to the duodenum in conditions such as ascending cholangitis due to

obstructing gallstones. Although the topology, material and the size of the stents

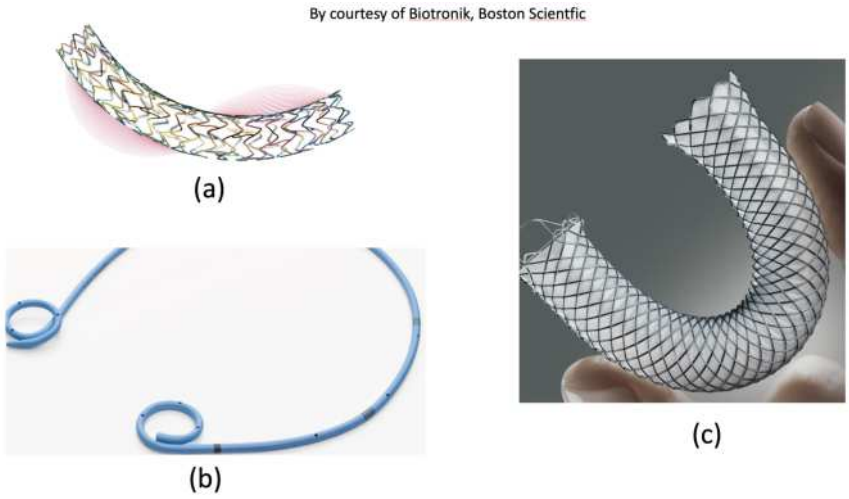


Fig. 1.4. Medical Stents. (a) Coronary stent (b) Ureteral stent (c) Biliary transhepatic stent

are different, the design methodology of the "Smart Stent" system is generic and can be applied to all these stent variations although some modifications may be needed. The objective of the "Smart Stent" or "Active Stent" system is to embed a microelectronic chip along with some sensors on the stent, where the chip is used for communicating sensor data to and from the stent and is powered by an RF signal generated externally. However, the electrical properties such as impedance and radiation patterns of stents are normally not considered by stent designers and thus these parameters are unknown, not well-controlled, and can have significant variations. In addition, because of the complex mesh structure of medical stents, accurate Electromagnetic (EM) models for them are rarely available to the circuit designers which make the design of the circuit that interfaces with the commercially available stents further challenging. For the aforementioned reasons, the system presented in [20][21] is not fully on-chip since discrete RF powering modules are used to connect the stent and the CMOS chip. In this work, a coronary stent will be used as the power receiving antenna for the proposed implantable CMOS chip. In contrast to [20][21], the system including the RF power modules will be fully on-chip and implemented with standard CMOS technology. For

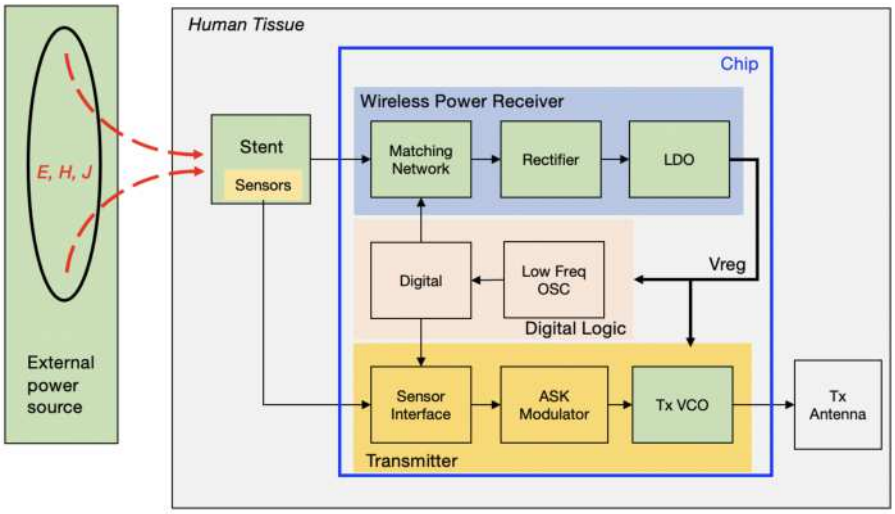


Fig. 1.5. System Overview. The green colored blocks are covered in this work.

both near-field and midfield WPT systems, rectifiers or other types of RF-to-DC converters are used to interface with the antenna as the first stage of a wirelessly powered implant. In the context of *in-vivo* or *in-vitro* biomedical applications, the external Equivalent Isotropically Radiated Power (EIRP) has an upper bound determined by the maximum power level set by the safety regulations. In such cases, the Power Conversion Efficiency (PCE) of rectifiers are crucial to maintain the systems' functionality because of the limited power available to the rectifier. Several techniques have been reported to increase the PCE of CMOS rectifiers by lowering the effective V_{th}, such as active differential V_{th} cancellation [27], lower DC feeding self-body-biasing [28] and self V_{th} compensation [29], to name a few. Nonetheless, the induced voltage at the receiving antenna of the implant, V_{av}, is usually low due to the area constraint as well as significant relaxation losses in the tissue, therefore a high rectifier PCE is difficult to be maintained. In such cases, a matching network that offers passive voltage amplification can be used to generate a higher voltage at the rectifier input [30][31][32]. In addition, the electrical properties of the stent will be affected by its surrounding environment (e.g., fluids, tissues, ...). Previous works [33–35] have characterized losses of ideal electric,

magnetic, and electromagnetic sources in a multilayer spherical phantom tissue. As presented in [36], for a given depth, radiation efficiency of an in-body antenna depends on the dispersive complex permittivity $\varepsilon = \varepsilon' + j\varepsilon''$. The real part of the permitivity, ε' loads the antenna, thus increasing its electrical size $\eta \propto ka$ (where k is the wave-number and a is the antenna circumradius [37].) The imaginary part of permitivity, $\varepsilon'' = \sigma/\omega$, characterize the frequency dependent losses due to tissue conductivity σ and scattering caused by heterogeneity. The effect of $\{\varepsilon, \sigma\}$ on the antenna radiation efficiency losses can be quantified by the approach proposed in [36]. Specifically, the radiation from the phantom in free space $\{\varepsilon_0, 0\}$ is studied to decorrelate the results caused by dielectric resonance by matching the permittivity of the environment to that of the phantom. This enables a more accurate estimate of how the radiation performance of the antenna depends on the EM properties of the surrounding tissues. Then, the computed gain is normalized to its maximum value over $\{\varepsilon, \sigma\}$ so that the results become independent of the specific antenna design. An important conclusion is that the tissues that load the antenna increase its electrical size as $ka \propto \sqrt{\varepsilon}$. The achievable radiation efficiency is proportional to ka for any electrically small antenna [37]. This effect allows for partial compensation of the losses induced by the conductivity. For example, the gain of the antenna operating in the phantom with stomach-equivalent EM properties is about two times higher than when fat-equivalent EM-properties are used. This is despite the fact that the conductivity of stomach is one order of magnitude higher than that of the fat. Moreover, the implanted antenna performance in a realistic environment is analyzed in [35]. It is shown that the antenna detuning caused by the surrounding tissue can be improved if the antenna remains well matched ($|S_{11}| < -10$ dB). Therefore, although for detailed analysis of the smart stent in a realistic scenario and taking into account the effects of the surrounding environment into the performance of the system, further investigations are required which are out of the scope of this work, we have introduced a tunable matching network in this research, which in turn improves the immunity and robustness of the antenna (stent) impedance to the detuning caused by the surrounding environment.

Furthermore, reliable packaging (for biocompatibility) is among the challenging aspects of the "Smart Stent" system design. To reduce the effects of the body reaction to a foreign object, a biocompatible coating and/or packaging is needed

to ensure a correct integration of the stent with the surrounding tissues once the device is implanted. Typically, for such applications it means that apart from having a small footprint, reliability and biocompatibility, the design must conform to constraints imposed by electronic circuit implementation. The vast majority of implant packages are either enclosures made of metal, glass or quartz, or a coating made of biocompatible material (such as medical-grade silicones) [38]. The fabrication of glass and quartz packages increases the overall fabrication time. On the other hand, polymer coatings provide only limited level of barrier against moisture penetration and can suffer delamination problems unless an appropriate thickness is used (typically, several hundreds of microns). Polyurethane, among many other polymers, has been extensively used as an outer membrane to act as a biocompatible interface with the surrounding host tissue. In [39], the realization of the coating/packaging for an implantable device is shown which embeds the sensing platform, the Integrated Circuits (IC) and the powering antenna, for the continuous monitoring of drugs and metabolites in small animals. In another example, the implemented package uses epoxy adhesive (EP42HT-2Med) system to embed the electronic components and the sensing platform in the integrated device. The sensing platform was placed on the top of the Printed Circuit Board (PCB) containing the ICs and the microprocessor. The interconnections between the sensing platform and the electronic components were realized with aluminum wire bonding and were protected with a glob top protection of 0.3 mm. Moreover, hermetically enclosed implant electronics at wafer scale using only narrow seal rings with addition of in silicon feedthourghs have also been gaining popularity [40]. As emphasized in [40], only a few bonding methods exist that do not involve high temperature or toxic materials. Among these, eutectic bonding is well established and can be performed using relatively relaxed environmental parameters, allowing for wafer-scale processing. The concept of using eutectic bonding for medical device packaging relies on a single seal ring in between faces of two planar substrates containing electronic circuitry and wireless communication elements. Both the thickness and width of the joint are in the range of microns, thus allowing for overall size reduction and more design freedom. Such an approach allows for the significant miniaturaization of the package, and could be used in application scenarios such as cochlear and cardiac implants, as well as in future electroeuticals

[41]. For chip-scale devices, AuSn eutectic bonding scheme has been proposed in [40] which offers the possibility of forming compact seals that achieve ultra-low permeability. A key feature is that it can be achieved at process temperature below 350°C, therefore allowing for the integration of sensors and microsystems with CMOS die within a single package. As can be seen from this brief overview, reliable packaging of the smart stent is of pronounce importance and requires further investigations which are outside the scope of this research.

In order to offer a stable power supply to support the operation of the overall system, on-chip voltage regulators are required to generate a fixed global V_{DD} from the prior rectifier stage output. Furthermore, voltage or current reference circuits are indispensable since many circuit blocks need to be biased. Because the available power that will be delivered to the implanted device is relatively low ($\sim$ tens of μW to hundreds of μW), low-power, low-voltage techniques should be used when designing regulators and references. A Low-Dropout Regulator (LDO) is a linear feedback circuit that is used to provide a stable voltage supply rail for the system. Here, the dropout voltage is defined as the difference between the supply voltage of the regulator and its output voltage V_{Reg}. The operating mechanism of LDO is that the output voltage V_{Reg} is monitored by the sensing block and compared with the reference through a negative feedback loop. If the loop gain of the LDO is high enough, the absolute error between the V_{Reg} and V_{REF} is negligible so that V_{Reg} is desensitized from the variation of the supply voltage and I_L. In addition, the output node impedance is low since it is divided by the loop gain of the LDO, so the behavior of the circuit is more closer to an ideal voltage source. LDOs are dynamic feedback systems and traditionally a large off-chip capacitor is required to be connected to the output to stabilize the loop as well as improving the load transient response [42, 43]. However, the off-chip components and the interconnections are problematic for SoCs, especially for implantable systems. Recent developments of output-capacitor-less LDO (OCL-LDO) make the full integration of these building blocks possible by eliminating the large external output capacitor [44–50]. Although the OCL-LDO topology is attractive, two issues have to be resolved: the instability and slow load transient response. A typical LDO feedback loop consists of an error amplification block (can be either single stage or multiple stages) and a pass transistor, where the size of the pass transistor is proportional to the maxi-

mum load current requirement. There are multiple poles in an LDO loop, but the two poles at relatively lower frequencies are p_o at the output of the LDO and p_g at the gate of pass transistor. For most of the OCL-LDOs, $p_o > p_g$, and hence the system is referred to as an "internal-pole" dominated topology. The stability of LDOs is affected by the load current variation. Specifically, p_g is proportional to square root of the load current I_L, and the p_o is proportional to I_L [44]. Large load currents push the output pole to higher frequencies well past the internal pole because it has faster change rate. Therefore, for LDOs that internal pole dominates the response, the loop usually has adequate phase margin when the load current is higher than certain level or in "heavy load" condition. However the stability of the loop should be carefully examined at "no load" and "light load" conditions, which refer to the cases where the load current is zero or very small. The quiescent biasing current of the pass transistor is expected to be as low as possible, so when I_L is small or zero, the pass transistor will be in cut-off or weak-inversion region. In this case, the Miller effect can be ignored since the pass transistor gain is very small so the internal pole moves up to higher frequency, on the other hand, the output resistance of the pass transistor increases so that the output pole moves backwards to lower frequency. The two poles can be placed fairly close which can lead to instability. For low-speed and low-power applications, a "Miller compensation" capacitor is often introduced to ensure the worst case stability of the LDO, but the Unity-Gain Frequency (UGF) will be significantly reduced.

Conventionally, the Bandgap Reference (BGR) [51] is one of the most popular solutions to generate process, voltage, temperature (PVT) independent voltage for integrated circuits. However, because the output voltage V_{REF} is the sum of junction diode built-in potential Φ_0 and the thermal voltage kT/q multiplied by a constant, the value of V_{REF} is around 1.25 V. Therefore, it is challenging to implement the conventional BGR topology when the supply voltage and the desired output voltage is low. In [52], a sub-1V output BGR is proposed by using current domain summation to generate V_{REF} and achieves comparable performance with traditional BGR topology. Nevertheless, the supply voltage cannot below the built-in potential Φ_0. For example, if the *pnp* transistor is used for V_{CTAT} generation, the junction built-in potential or its base-emitter voltage V_{EB} is around 0.7 V. It means that the minimum required supply voltage for BGR using *pnp* transistor

should be no less than 0.75 V, since even without cascoding the current mirror on top of the *pnp* transistors requires at least 50 to 100 mV V_{DS} to work in saturation mode. To further lower the required supply voltage, all-MOSFET reference topologies have been investigated and presented in [53–56]. The basic idea is that to use diode-connected MOSFETs which are biased in weak-inversion region to replace the *pnp* transistors, since the threshold voltage, V_{th}, of MOSFETs is typically in the range of 0.3 to 0.5 V, the required V_{GS} is much lower than V_{EB} of the *pnp* transistor, hence the supply voltage can be reduced. The major drawback of the all-MOSFET topology is that it is more sensitive to process variations, especially V_{th} variation due to the exponential relationship between drain current and gate-source voltage. Nonetheless, the all-MOSFET solution still offers decent performance for low-voltage applications.

Typically, the oscillator is one of the power-hungry circuit blocks of the system, especially when the oscillation frequency is beyond GHz range. In fact, the implementation of a low-voltage, low-power voltage-controlled oscillator with good phase-noise (PN) and tuning range is always challenging. For low-power applications, *LC*-oscillators are preferred due to lower power consumption at higher frequencies. Previous works [57–59] presented the design and optimization method of oscillators based on the Impulse Sensitivity Function (ISF) to achieve optimum phase noise performance. The desired ISF can be synthesized by "engineering" the oscillators' output waveforms, which can be achieved by weighting the harmonic contents.

1.1 Survey on wirelessly-powered micro-implantable systems

In recent years, there are many works focus on transfer wireless power to small implantable systems. In [30], a mm-sized implantable power receiver are proposed. Specifically, the power receiver was implemented in 0.13-μm CMOS and bonded to a 2×2 mm^2 loop antenna with controlled bond wire length. A 2×2 cm^2 loop was used as the transmit antenna and the antennae were separated by 15 mm of bovine muscle tissue. Regulator output of 1.2 V is maintained as the current load varies from 15 μA to 120 μA. A 3.5 dB gain is achieved by adaptive matching for

a receiver at 1 mm range displacement plus 1 mm of axial mis-alignment. In [15], the tradeoff between received power and tissue absorption are examined against different frequencies. The results show that the optimal frequency is in the GHz range for mm-sized antenna and shifts to the sub-GHz range for cm-sized antenna. In [60], a wirelessly powered and controlled implantable device capable of locomotion in a fluid medium is presented. The wireless prototype occupies 0.6 mm $\times$ 1 mm in 65 nm CMOS with an external 2 mm $\times$ 2 mm receive antenna. It receives 500 μW from a 2 W 1.86 GHz power signal at a distance of 5 cm. Asynchronous pulse-width modulation on the carrier allows for data rates from 2.5-25 Mbps with energy efficiency of 0.5 pJ/b at 10 Mbps. The received data configures the propulsion system drivers, which are capable of driving up to 2 mA at 0.2 V and can achieve speed of 0.53 cm/s in a 0.06 T magnetic field. In [5], the optimal transmitter for wireless power transfer to small receiver embedded in multiple planar layers of tissue is studied. The optimal source distribution achieves the highest power transfer efficiency at the low-GHz range. At higher frequencies, the optimal current distribution is shown to include fields that exhibit focusing. The effects of constructive and destructive interference substantially improves the power transfer efficiency and reinforces operation in the low GHz range. The optimal transmitter establishes an upper bound on the power transfer efficiency for a given implant and provides insight on the design of the optimal transmit antenna. In [18], a wireless powering method that can power micro-implants at nearly any location in the body is demonstrated. With exposure levels below human safety thresholds, milliwatt levels of power can be transferred to a deep-tissue (>5 cm) micro-implant for both complex electronic function and physiological stimulation. The approach developed enables new generations of implantable systems that can be integrated into the body at minimal cost and risk. In [61], a fully integrated 2 $\times$ 2 CMOS transceiver at 60 GHz with energy harvesting capability in the transmitter mode and on-chip dipole antennas is demonstrated. The radio supports on-off-keying modulation and a programmable data rate of 38 to 2450 Mbps at BER of less than 5×10^{-4}. The power consumption of the transmitter scales with data rate from 100 μW to 6.3 mW at 5 cm range and from 260 μW to 11.9 mW at 10 cm range. This yields an energy efficiency of 2.6 pJ/b at 5 cm and 4.9 pJ/b at 10 cm. The energy harvesting circuits operate at 2.45 GHz with an average efficiency of 33%.

The harvesting antenna and its matching components are off-chip. The complete transceiver including the energy harvesting block and on-chip antennas occupies 1.62 mm^2 in 40 nm CMOS. In [17], a wirelessly powered 11 μW transceiver for implantable devices has been designed and demonstrated through 35 mm of porcine heart tissue. The prototype was implemented in 65 nm CMOS occupying 1 mm $\times$ 1 mm with a 2 mm $\times$ 2 mm off-chip antenna. The forward link transfers power and data on a 1.32 GHz carrier using low-depth ASK modulation that minimizes impact on power delivery and achieves from 4 to 20 Mbps with 0.3 pJ/b at 4 Mbps. The backscattering link modulates the antenna impedance with a configurable load for operation in diverse biological environments and achieves up to 2 Mbps at 0.7 pJ/b. The device supports TDMA, allowing for operation of multiple devices from a single external transceiver. In [62], a radio system that could be used in millimeter-scale wireless neural implants is presented. The system is RF-powered and demonstrates Mbps data rates required for neuromodulation and recording applications. The radio transmits at 58 Mbps and receives at 2.5 Mbps maximum data rates. The transceiver uses a duplexer to achieve full-duplex communication via frequency-division duplexing at 1.74 and 1.86 GHz for Tx and Rx, respectively. The average power consumption of the transmitter is 93 μW at 58 Mbps, while that of the receiver is 7.2 μW at 2.5 Mbps. The transceiver was fabricated using 40 nm CMOS process and occupies 0.8 mm^2 of die area. Including the off-chip duplexer, the system occupies $2\times1.6\times0.6$ mm^3.

1.2 Organization

In the first part of this thesis, we described our work on designing the interface between the medical stent and the CMOS IC die. The detailed characterization process of the medical stent is elaborated in Chapter 2, and the co-design method of matching network and the rectifier is presented. Next, the external RF source is synthesized based on the method presented in [2, 5, 18, 63]. Finally, the chip with the stent is tested with the synthesized RF source *in-vitro*. As a proof-of-concept design, the implantable system has been shown to be working at 1.1 GHz, with a separation distance of 50 mm and a 30 mm phantom-tissue.

Next, in the second part of the thesis, we focus on the design of the low-power

circuit blocks. In Chapter 3,fundamentals of the low-dropout regulator (LDO) as well as the design challenges have been reviewed and discussed. A novel LDO based-on current feedback is proposed as a solution for ultra-low power applications. The proposed LDO has a current efficiency of %99.8, with an input range of 0.58 V to 0.9 V and achieves a FoM of 0.99 ps. In addition, it has embedded reference hence the BGR is no longer required.

In Chapter 4, the design and optimization of Class-D Voltage Controlled Oscillator (VCO) is elaborated. A low-power, low-voltage Class-D VCO with tail inductor noise-filtering is implemented, which shows a FoM of $-192.5\,\mathrm{dBc/Hz}$. The Fourier coefficients of the ISF is derived from simulation, and the phase-noise predicted by the ISF is in-line with the results from the circuit simulator.

Finally, in Chapter 5 we summarize some of the key design insights and perspectives of the "active stent" system, as well as the design techniques associated with the low-power low-voltage implementation of the circuit blocks. In addition, some potential future research directions to address the challenges of designing wirelessly powered implantable systems and low-power integrated circuits are presented.

Chapter 2

Co-Design of Stent-Chip Interface

In this chapter, the detailed design methodology of stent-chip interface is discussed. Firstly, the characterization procedure of the medical stent is elaborated. Then a rectifier is designed based on the circuit model of the stent to achieve the optimum PCE for the low-voltage condition. As a proof-of-concept design, a fully integrated rectifier with on-chip tunable transformer-coupled matching network is implemented in a 0.13 µm CMOS process. The measurement results show that it can generate more than 500 mV DC voltage on a 2 kΩ load when the available power from the stent is greater than -2 dBm, corresponding to 34% PCE.

2.1 Review of wirelessly-powered implantable system using medical stents

In [19], the authors explored the use of stents as radiating structures to support transcutaneous wireless telemetry. Incorporating stents with a miniature implantable sensory device allows for internal monitoring of nearly any location within the cardiovascular system. Specifically, an implantable stent-based transmitter were assembled by integrating a 2.4 GHz wireless transmitter, battery and two stents configured as a dipole radiator. The *in-vivo* results from various distances (10 cm to 1 m) showed a 33-35 dB power reduction while implanted at a 3.5 cm depth

within the chest. This validates the ability of using stents to wirelessly transmit data from deep within a living body. In [20], a fully wireless cardiac pressure sensing system is presented. Food and Drug Administration (FDA) approved medical stents are explored as radiating structures to support simultaneous transcutaneous wireless telemetry and powering. An application-specific integrated circuit (ASIC), designed and fabricated in 0.13 μm CMOS process, enables wireless telemetry, remote powering, voltage regulation, and processing of pressure measurements from a microelectromechanical systems (MEMS) capacitive sensor. It demonstrates fully wireless-pressure-sensing functionality with an external 35-dBm RF powering source across a distance of 10 cm. Measurements in a regulated pressure chamber demonstrate the ability of the cardiac system to achieve pressure resolution of 0.5 mmHg over a range of 0-50 mmHg using a channel data-rate of 42.2 Kbps. In [64], RF powering techniques to supply wireless-energy for miniature implantable devices used to monitor physical-conditions in real-time are evaluated. The RF rectifier consists of a modified two-stage voltage multiplier which produces the necessary turn-on voltage for standard low power CMOS systems while supplying the required current levels. The rectifier fabricated in 0.13 μm CMOS is integrated with an antenna to quantify wireless performance of the power transfer. *In-vivo* studies performed on New Zealand white rabbits demonstrated the ability of implanted CMOS RF rectifier to produce 1 V across a 27 kΩ load at a distance of 5 cm with a transmit-power of over 1.5 W. Using a pulsed-powering technique, the circuit generates under 0.9 V output with an average transmit-power of 300 mW. The effects of implantation on the propagation of RF powering waves are quantified and demonstrated to be surmountable, allowing for the ability to supply a low-power wireless sensor through a miniature rectifier IC.

2.2 Stent characterization

The stent sample used in this work is Lekton Motion 3.5/18 from Biotronik GmbH & Co.KG. As shown in Fig. 2.1, the measured length and diameter of the stent after expansion are 15 mm and 2.5 mm, respectively. Unlike the design of an antenna, the complex mesh pattern of the stent makes it difficult to be characterized by using a 3-dimensional full-wave electromagnetic (EM) simulation. In this case, the

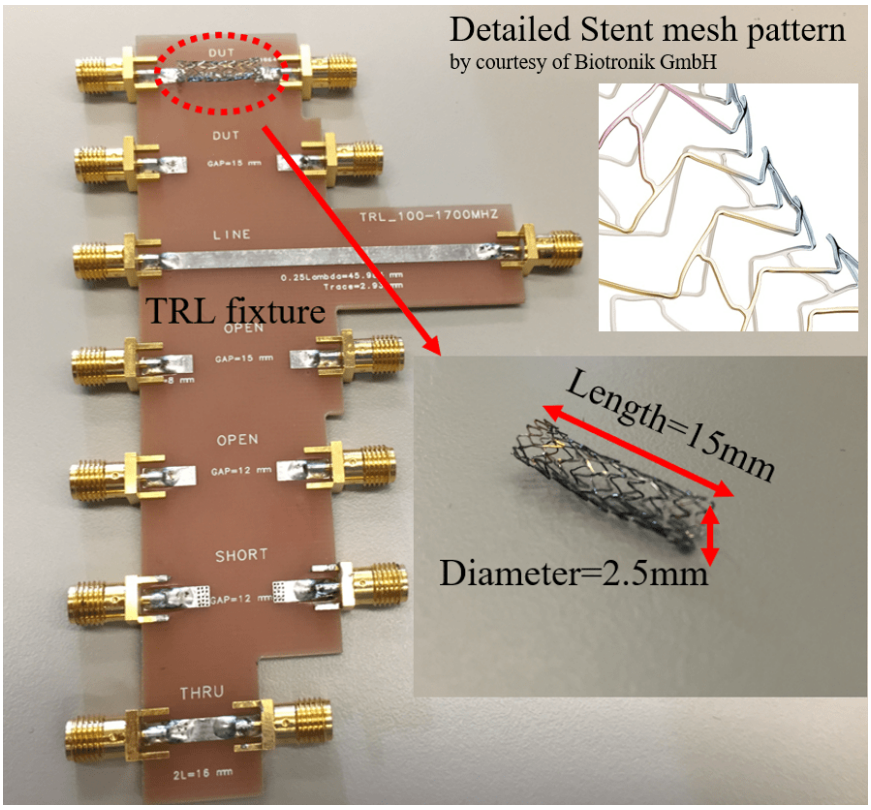


Fig. 2.1. The medical stent and the customized calibration sets used in this work.

modeling of the stent can be performed based on RF-measurements. Specifically, the stent is to be considered as a two-port or differential one-port network, and its Z-parameters can be measured by using **VNA!** (VNA!). One of the major issues has been encountered in RF measurements is that the measured response will deviate from the true response due to the parasitics introduced by test fixtures and interconnections. Ideally, the stent should be directly wire bonded to the bond pads of the bare die without any other fixtures, however, a customized stent is required to make this possible. The parasitics in stent-chip interface have profound impacts on the overall system performance. Nonetheless, the parasitic effects can be explicitly analyzed as long as the intrinsic performance of the stent is known. To calibrate the measurement results, a customized calibration kit as shown in Fig. 2.1 is fabricated

to hold the stent during the two-port impedance measurement, and the parasitics of the test fixture are de-embedded afterwards by using **TRL!** (**TRL!**) calibration technique. After calibration, the differential one-port stent impedance Z_{stent} can be derived as

$$\begin{aligned} Z_{stent} &= Z_{dd0} \cdot \frac{1+S_{dd}}{1-S_{dd}} \\ &= Z_{dd0} \cdot \frac{1+\dfrac{S_{11}+S_{22}-S_{21}-S_{12}}{2}}{1-\dfrac{S_{11}+S_{22}-S_{21}-S_{12}}{2}}, \end{aligned} \tag{2.1}$$

where subscripts 1 and 2 refer to the two single-ended stent terminal ports. Z_{dd0} is the differential reference impedance, which is equal to $100\,\Omega$ in a $50\,\Omega$ measurement environment. We also know Z_{stent} is a function of frequency, as expressed here:

$$\begin{aligned} Z_{stent}(\omega) &= R_{stent}(\omega) + jX_{stent}(\omega) \\ &= R_{rad}(\omega) + R_{loss}(\omega) + j\omega L_{stent}(\omega). \end{aligned} \tag{2.2}$$

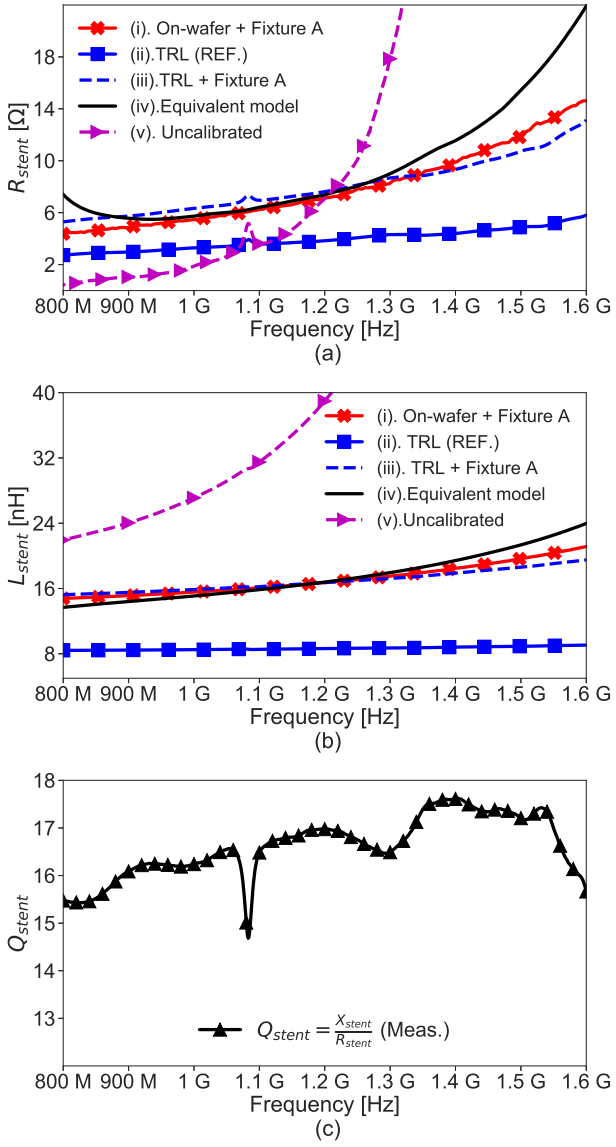


Fig. 2.2. Stent differential resistance (a), inductance (b) and Q-factor (c). i. Measured on-wafer with *Fixture-A* parasitics. ii. Measured and de-embedded with customized TRL standards. iii. TRL results embedded with *Fixture-A* parasitics. iv. Equivalent stent model (50 Ω port+Balun+*Fixture-B*) used for rectifier input power characterization in the 50 Ω environment. v. Measured without TRL calibration.

The real part of $Z_{stent}(\omega)$ consists of two components, the equivalent radiation resistance $R_{rad}(\omega)$ and the ohmic loss term $R_{loss}(\omega)$, and these two terms determine the radiation efficiency of the stent. Measuring the ratio of $R_{rad}(\omega)$ and $R_{loss}(\omega)$, or in other words, the stent radiation efficiency is not straightforward as one can measure the sum of the two parameters but not their individual values. Nonetheless, for frequencies in the range of 800 to 1600 MHz, the ohmic loss can be estimated by only considering skin-effect of the stent. The measured stent differential resistance R_{stent} and inductance L_{stent} are illustrated in Fig. 2.2, from which it can be seen that there is a large difference between impedance, especially the reactance X_{stent} before and after TRL calibration (traces (v) and (ii) in Fig. 2.2, respectively). Without calibrating out the fixture parasitics, L_{stent} will grow much faster with frequency, therefore the resonance caused by parasitics occurs at a frequency much lower than the real self-resonance frequency (SRF) of the stent. In fact, the true stent differential inductance L_{stent} is around 8 nH and the inductance variation ΔL_{stent} from 800 MHz to 1600 MHz is about 0.72 nH or 9%. Therefore, the main uncertainty of the equivalent inductance seen by the circuit is from parasitic inductance caused by the interconnection between the stent and its interface with the peripheral circuit. With respect to the resistance R_{stent}, it can be concluded that R_{stent} increases from 2.7 Ω at 800 MHz to 5.8 Ω at 1600 MHz. The variation ΔR_{stent} is 3.1 Ω and should not be ignored as it is comparable to R_{stent}. The quality factor of the stent is also plotted in Fig. 2.2, and one can see the *Q-factor* is generally at the same level of on-chip inductors. It should be noted that the accuracy of the stent model will be affected by the surrounding environment. For example, when the stent is placed inside a typical *in-vitro* or *in-vivo* environment, the stent impedance will change. This is in part due to the relative permittivity, ε_r, of the surrounding media, for instance, human tissue, where the effective wavelength in the media λ_{eff} will be $\sqrt{\varepsilon_r}$ times shorter than the wavelength in the free space, λ_0. As a result, the physical size of the stent becomes comparable to λ_{eff} so that the radiation resistance can be quite different. Although a more accurate stent model can only be derived by testing the stent *in-vivo*, the presented modeling methodology is still valid and the same methodology can be used for *in-vivo* experiments. In our proof-of-concept design, the variation of the stent impedance caused by the surrounding environment will be partly compensated by the tuning process, and the measured impedance of

trace (ii) in Fig. 2.2 is used as the reference stent impedance.

2.3 Co-design of rectifier and matching network

2.3.1 Analysis of Cross-Coupled Differential Rectifier

The cross-coupled differential rectifier presented in [27][65][66] is an efficient topology at low input power levels. The available power at the output of the stent or at the input of the rectifier circuit is:

$$P_{av} = \frac{V_{oc}^2}{8R_{stent}} = \frac{V_{av}^2}{2R_{stent}}, \tag{2.3}$$

where, V_{oc} is the amplitude of the open-circuit voltage at the output of the stent and V_{av} is the peak available voltage across the load under conjugate-matched condition. Since V_{oc} depends on the equivalent antenna aperture of the stent and the polarization mismatch, high P_{av} and V_{oc} can be achieved only by properly designing the external transmitting antenna.

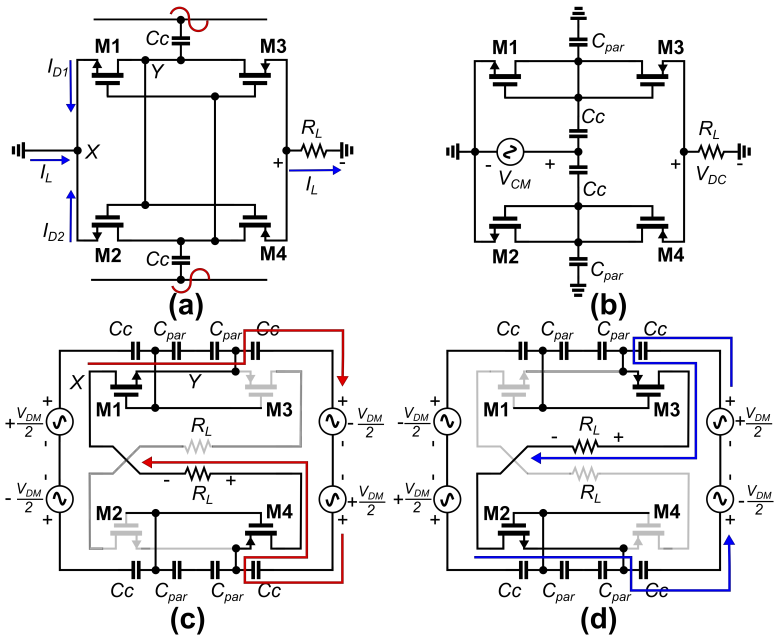


Fig. 2.3. Single stage differential rectifier cell.

The analysis of the cross-coupled rectifier shown in Fig. 2.3 is rather cumbersome due to its strong nonlinearity. The current flow through the load, I_L, will be steered in the same direction during the complementary on-off operation of the two rectifier branches, $M_{1,4}$ and $M_{2,3}$. Assuming the rectifier cell is symmetrical and its p-type transistors are sized such that $\mu_p W_p = \mu_n W_n = \mu_n W$, where $\mu_{n\,(p)}$ is the electron (hole) mobility and W is the width of the n-transistors. Due to the circuit symmetry, it suffices to consider one of the rectifier branches. When a single tone signal $V_{av}\sin\theta$ is applied across the rectifier, and the node X is chosen as the reference node so that $V_X = 0$, then according to Fig. 2.3 (c) the terminal voltages of transistor M_1 can be written as:

$$V_{GX}(\theta) = V_{CM} + \frac{V_{DM}(\theta)}{2} = V_{CM} + \frac{V_{av}\sin\theta}{2}, \tag{2.4a}$$

$$V_{GY}(\theta) = V_{DM}(\theta) = V_{av}\sin\theta, \tag{2.4b}$$

$$V_{XY}(\theta) = \frac{V_{DM}(\theta)}{2} - V_{CM} = \frac{V_{av}\sin\theta}{2} - V_{CM}, \tag{2.4c}$$

where V_{CM} and $V_{DM}(\theta)$ are the common-mode and the differential-mode components of the input voltage. The common-mode component depends on the charge-

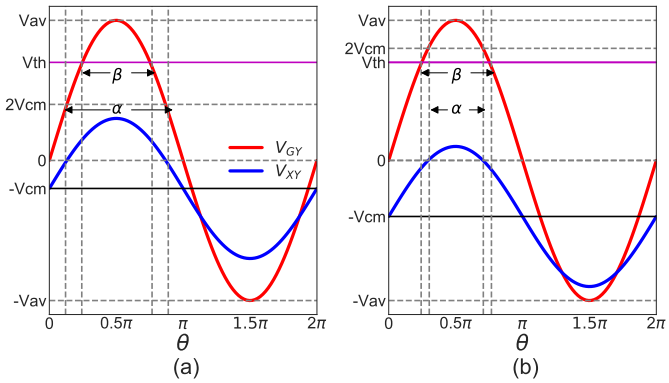


Fig. 2.4. Forward conduction angle α, strong inversion conduction angle β vs. transistor terminal voltages. (a) $\alpha > \beta$. (b) $\alpha < \beta$.

redistribution among the coupling capacitors, output capacitor and the transistors' channels of the rectifier cell. At the beginning of the rectifier start-up phase, the DC output voltage $V_{DC} = 0$ and hence $V_{CM} = 0$. After several periods, V_{DC} rises up because I_L flows through load R_L. As a result, V_{CM} is generated by V_{DC} itself and superimposed on the gate nodes of the transistors. The common-mode behavior can be seen as transistors $M_{1,2,3,4}$ are diode-connected and stacked on top of each other, therefore, for a single stage rectifier cell V_{CM} is half of V_{DC} based on the assumption $\mu_p W_p = \mu_n W_n$. In the steady state, if the forward direction of the drain current I_{D1} is defined as the same as that of I_L, it can be deduced that I_{D1} will be positive or in forward direction when $V_{XY}(\theta) > 0$. Ignoring all secondary order effects, the drain current can be written as:

$$I_D = \begin{cases} I_S \exp\left(\dfrac{V_{GS} - V_{th}}{\xi V_T}\right)\left[1 - \exp\left(-\dfrac{V_{DS}}{2V_T}\right)\right], & V_{GS} \leq V_{th} \\ \\ K' \dfrac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \dfrac{V_{DS}^2}{2}\right], & V_{GS} > V_{th} \end{cases} \tag{2.5}$$

where ξ, V_T, K' are the sub-threshold swing, thermal voltage, and transconductance parameter of the transistor, respectively. The term $I_S = \mu \frac{W}{L} V_T^2 \sqrt{q\varepsilon_{si} N_{dep}/4\phi_F}$ is

technology dependent, where N_{dep} is the channel doping concentration at depletion edge, ϕ_F is the Fermi potential in the bulk and ε_{si} is the permittivity of silicon. To simplify the analysis, the forward conduction angle α is introduced and defined as

$$\alpha = \pi - 2\arcsin(\frac{2V_{CM}}{V_{av}}), \tag{2.6}$$

hence for $\theta \in (\frac{\pi-\alpha}{2}, \frac{\pi+\alpha}{2})$, $I_{D1}(\theta) > 0$. In this case, node X is the drain of M_1 and node Y is the source. The load current is $I_L(\theta)$ which equals to $I_{D1}(\theta)$, and its magnitude will be determined by the overdrive voltage $V_{GS1}(\theta) - V_{th}$. To keep the notation consistent, conduction angle β is introduced to define the boundary of the strong inversion and the weak inversion and is given as:

$$\beta = \pi - 2\arcsin(\frac{V_{th}}{V_{av}}), \tag{2.7}$$

so that the transistor operates in strong inversion region for $\theta \in (\frac{\pi-\beta}{2}, \frac{\pi+\beta}{2})$. It should be noted that α and β are not necessarily to be equal since the range of them will be determined by the relationship among the input voltage, output voltage and the threshold voltage. If we assume $V_{av} > V_{th}$ and $2V_{CM} \approx V_{DC}$ for a single-stage rectifier cell in normal operation, the drain current of one of the n-transistor, e.g. M_1, can be found in following two situations:

a). $\alpha > \beta$

If the forward conduction angle α is greater than β, the drain current $I_{D1}(\theta)$ contains both strong inversion and weak inversion currents during forward conduction, whereas the reverse current contains only sub-threshold component as indicated in Fig. 2.4 (a). The load current $I_L(\theta)$, which equals to $I_{D1}(\theta)$ for half of a period, can

be derived by substituting (2.4)(2.6)(2.7) into (2.5) and is written as:

$$I_L(\theta) = \begin{cases} \text{if } \theta \in [0, \dfrac{\pi-\alpha}{2}] \cup [\dfrac{\pi+\alpha}{2}, \pi] : \\ -I_S \exp(\dfrac{V_{av}\sin\theta - V_{th}}{\xi V_T})[1-\exp(\dfrac{2V_{CM}-V_{av}\sin\theta}{2V_T})], \\ \\ \text{if } \theta \in [\dfrac{\pi-\alpha}{2}, \dfrac{\pi-\beta}{2}] \cup [\dfrac{\pi+\beta}{2}, \dfrac{\pi+\alpha}{2}] : \\ +I_S \exp(\dfrac{V_{av}\sin\theta - V_{th}}{\xi V_T})[1-\exp(\dfrac{2V_{CM}-V_{av}\sin\theta}{2V_T})], \\ \\ \text{if } \theta \in (\dfrac{\pi-\beta}{2}, \dfrac{\pi+\beta}{2}) : \\ +K'\dfrac{W}{L}(\dfrac{3V_{av}^2 - 8V_{CM}^2 + 16V_{CM}V_{th}}{16} \\ \qquad -\dfrac{V_{CM}+V_{th}}{2}V_{av}\sin\theta - \dfrac{3}{16}V_{av}^2\cos 2\theta) \end{cases} \tag{2.8}$$

where the "+" sign indicates the forward current direction and the reverse current is labeled with "−" sign.

b). $\alpha < \beta$

In the case of $\alpha < \beta$, all forward current is generated when the transistor is operating in the strong inversion region, whereas the reverse current consists of both strong inversion and sub-threshold currents. By using the same notation, the load

current can be written as:

$$I_L(\theta) = \begin{cases} \text{if } \theta \in [0, \dfrac{\pi-\beta}{2}] \cup [\dfrac{\pi+\beta}{2}, \pi]: \\ -I_S \exp(\dfrac{V_{av}\sin\theta - V_{th}}{\xi V_T})[1-\exp(\dfrac{2V_{CM}-V_{av}\sin\theta}{2V_T})], \\ \\ \text{if } \theta \in [\dfrac{\pi-\beta}{2}, \dfrac{\pi-\alpha}{2}] \cup [\dfrac{\pi+\alpha}{2}, \dfrac{\pi+\beta}{2}]: \\ -K'\dfrac{W}{L}(\dfrac{3V_{av}^2 - 8V_{CM}^2 + 16V_{CM}V_{th}}{16} \\ \qquad -\dfrac{V_{CM}+V_{th}}{2}V_{av}\sin\theta - \dfrac{3}{16}V_{av}^2\cos 2\theta), \\ \\ \text{if } \theta \in (\dfrac{\pi-\alpha}{2}, \dfrac{\pi+\alpha}{2}): \\ +K'\dfrac{W}{L}(\dfrac{3V_{av}^2 - 8V_{CM}^2 + 16V_{CM}V_{th}}{16} \\ \qquad -\dfrac{V_{CM}+V_{th}}{2}V_{av}\sin\theta - \dfrac{3}{16}V_{av}^2\cos 2\theta). \end{cases} \tag{2.9}$$

The DC load current for both cases can be calculated as:

$$I_{DC} = \frac{1}{\pi}\int_0^{\pi} I_L(\theta)\,\mathrm{d}\theta. \tag{2.10}$$

From preceding analysis it can be found that the current in the reverse direction has a negative contribution on V_{DC}, and hence, the reverse current when the rectifier transistors are operating in strong inversion should be avoided as the magnitude of the drift current is much greater than that of the diffusion current. Therefore, the condition $\alpha > \beta$ is preferred and can be further reformulated as $V_{th} > 2V_{CM}$. For a single-stage rectifier cell, however, it means that the output voltage V_{DC} is lower than V_{th} if $\alpha > \beta$. In order to have a higher V_{DC} while keeping the reverse current low, N stages can be cascaded to pump up V_{DC}, and also scale down the V_{CM} across each transistor gate to $V_{DC}/2N$. As a result, the DC output voltage V_{DC} only needs to be smaller than NV_{th} to satisfy $\alpha > \beta$. The closed form analytic solution of (2.8) and (2.10) cannot be obtained since the common-mode voltage V_{CM} in (2.6) and (2.8) is determined by $I_{DC}R_L/2N$. Nonetheless, equation (2.8) and (2.10) can be

solved iteratively by using numerical methods so that for a given V_{av}, V_{DC}, optimum W/L and N can be found that yield maximum I_{DC}. However, it should be noted that because the stent impedance Z_{stent} is within the range of $2.7 + j42$ to $5.8 + j91\ \Omega$, the V_{av} generated by the stent at low P_{av} is much less than V_{th}. Therefore, the input signal has to be amplified by a matching network to meet the condition $V_{av} > V_{th}$. The overall power conversion efficiency at the implanted side, η_{Rx}, with load R_L, is defined as:

$$\eta_{Rx} = \frac{P_{DL}}{P_{av}} = \frac{P_{in}}{P_{av}} \cdot \frac{I_{DC}^2 R_L}{P_{in}} = (1 - |\Gamma|^2) \cdot PCE, \tag{2.11}$$

where P_{in} is the actual power into the rectifier cell, $|\Gamma|^2$ is the power reflection coefficient at the rectifier input. To improve η_{Rx}, $|\Gamma|^2$ and PCE need to be co-optimized since $|\Gamma|^2$ and rectifier PCE are both functions of W/L and N as will be discussed in following sections.

2.3.2 Transformer Design

There are many topologies for on-chip matching networks. In this work, a transformer-based matching network is proposed to achieve voltage amplification while keeping the **IL!** (**IL!**) low. Ideally, the passive voltage gain of the transformer G_{VX} is governed by its turn ratio n,

$$G_{VX} = \frac{V_S}{V_P} = \sqrt{\frac{L_S}{L_P}} \approx n, \tag{2.12}$$

where, L_S and L_P are the self-inductance of the secondary and primary windings, respectively, and can be measured by having the other winding open-circuited. The coupling coefficient, k_{ps}, indicates the magnetic coupling strength between the primary and secondary windings and can be expressed as

$$k_{ps} = \frac{M_{ps}}{\sqrt{L_P L_S}} = \frac{\mathrm{Im}(Z_{21})}{\sqrt{\mathrm{Im}(Z_{11})\,\mathrm{Im}(Z_{22})}}, \tag{2.13}$$

where, ports 1 and 2 are defined as transformer's primary and secondary differential ports, respectively, M_{ps} is the mutual inductance between the primary and secondary winding. The ratio of the power delivered to the load R_2 at secondary winding P_2 to the total power into the transformer primary winding P_1 is given by

[67]

$$\eta_X = \frac{P_2}{P_1} = \frac{R_2/n^2}{(\frac{\omega L_P/Q_S + R_2/n^2}{\omega k_{ps} L_P})^2 \cdot \frac{\omega L_P}{Q_P} + \frac{\omega L_P}{Q_S} + R_2/n^2} \tag{2.14}$$

and the minimum insertion loss IL_{min} is defined as

$$\begin{aligned} IL_{min}(dB) &= -10\lg(\eta_{X,\,max}) \\ &= -10\lg[1+2(x-\sqrt{x^2+x})], \end{aligned} \tag{2.15}$$

where $\eta_{X,\,max}$ is the maximum transformer efficiency and $x = 1/(k_{ps}^2 Q_P Q_S)$.

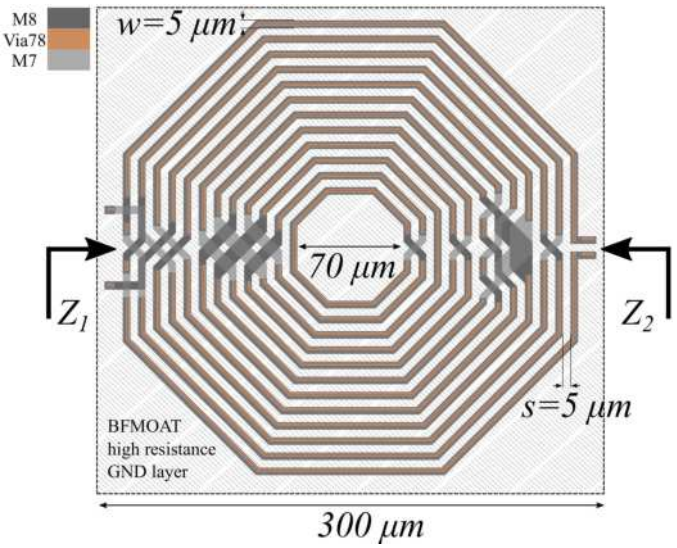


Fig. 2.5. Proposed transformer layout. The region underneath the transformer is a BFMOAT implant blocking layer to lower the substrate conductivity.

Eqn. (2.14) indicates that the minimum insertion loss IL_{min} of the transformer is not a function of its load R_2 and is a monotonically decreasing function of x. In order to achieve low IL_{min}, the term $k_{ps}^2 Q_P Q_S$ needs to be maximized. Although the transformer IL_{min} can be optimized without considering the loading conditions, it should be noted that $IL = IL_{min}$ will only be achieved when the primary and secondary termination impedances are simultaneously matched to the associated input and output impedances of the transformer Z_1, Z_2.

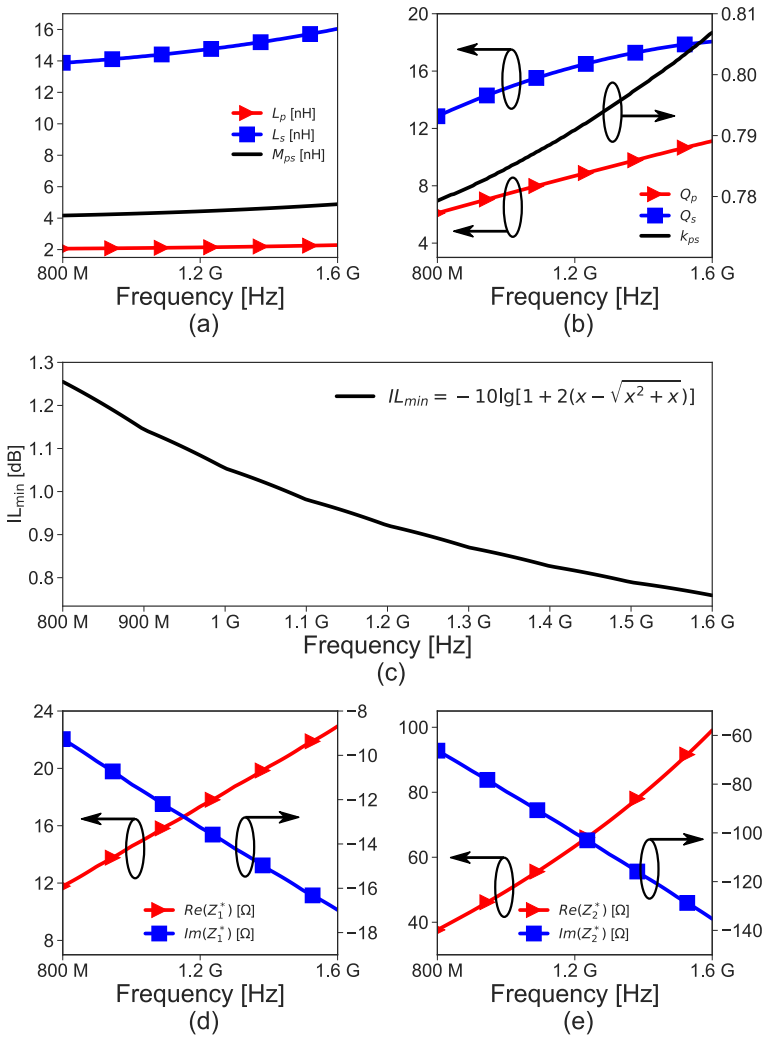


Fig. 2.6. Transformer performance. (a) Self and mutual inductance. (b) Q-factor and coupling coefficient. (c) Calculated theoretical minimum insertion loss. (d)-(e) Required differential termination impedance at primary/secondary port to realize IL_{min}.

The primary termination impedance is determined by the stent and the tuning network while the secondary termination impedance will be determined by the rectifier topology and the load R_L. The optimization is an iterative process because only Z_{stent} and R_L are known parameters, therefore, to achieve the global maxi-

mum PCE, the tuning network should convert Z_{stent} to Z_1^* and the rectifier with load R_L should be designed to have input impedance $Z_{rect} = Z_2^*$ to realize IL_{min}. In this work, a transformer with minimum IL_{min} and maximum G_{VX} at the desired operating frequency is designed first and the output/input impedance of the tuning network and rectifier are designed to approach the optimum transformer termination impedance accordingly. The physical layout of the proposed fully differential transformer is illustrated in Fig. 2.5, the 3-turn primary winding is interleaved into 9-turn secondary winding, and the stacked traces, consisting of the two available thick metal layers, are used in both primary and secondary windings to enhance Q and k_{ps}. The design and simulations are performed by 2.5-D EM solver Sonnet, and the simulated results are shown in Fig. 2.6. By using Eqn. (2.12) and the results shown in Fig. 2.6 (a), the calculated value of G_{VX} is around 2.6. As predicted by Eqn. (2.15) the IL_{min} is between 0.8 and 1.3 dB within the range of 800 MHz to 1.6 GHz, and the required optimum transformer termination impedance $Z_{1,2}^*$ are derived and plotted in Fig. 2.6 (d)-(e).

2.3.3 Co-optimization of Rectifier and Matching Network

Given the nonlinear behaviour of the rectifiers, large-signal S-parameter (LSSP) based analyses should be used to evaluate the rectifier impedance at different input power levels and frequencies. The optimization goal is to achieve more than 500 mV DC voltage on a 2 kΩ load at the rectifier output when its input voltage is $V_{av} \cdot G_{VT} \cdot G_{VX}$, where G_{VT} is the voltage gain of the tuning network. This corresponding to $I_{DC} \approx 250\,\mu A$. On the one hand, larger I_{DC} requires larger W/L. On the other hand, as W/L becomes larger, the rectifier input impedance Z_{rect} will be reduced accordingly, which may conflict with the desired optimum termination impedance at the transformer secondary port Z_2^*. As the LSSP results shown in Fig. 2.7, Z_{rect} varies with different input power. Furthermore, Z_{rect} is also a function of transistor size W, number of stages N, frequency f and available power P_{av}, namely, $Z_{rect} = Z_{rect}(W, N, f, P_{av})$. By properly designing W, N of the rectifier, the optimum value Z_2^* can be approached. As discussed in Section 2.3 B, simultaneous conjugate matching is required to realize transformer IL_{min}, so the tuning network should also be designed to transform Z_{stent} to Z_1^*. It is important to consider the par-

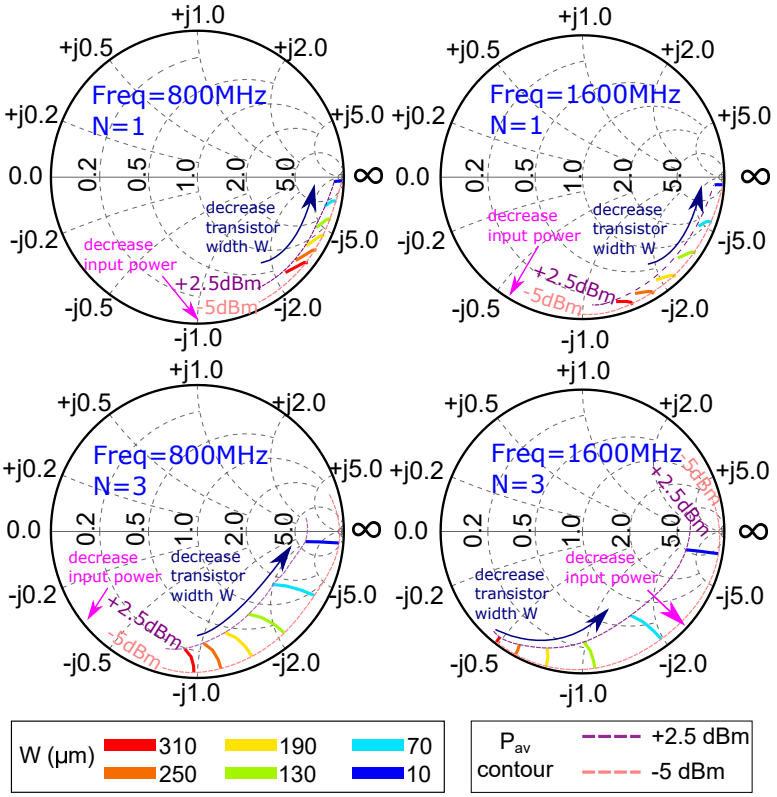


Fig. 2.7. Simulated large signal rectifier differential input impedance on 50 Ω Smith-Chart. P_{av} of a 50 Ω source is swept from −5 dBm to +2.5 dBm in the range of 800 MHz to 1600 MHz and a 2 kΩ R_L is connected at the output. The width of PMOS and NMOS is W_P=2W_N=2W, where W is swept from 10 µm to 310 µm for the case of $N = 1$ and 3.

asitic effects caused by the electrostatic discharge (ESD) devices, bond-pads, bond-wires and any printed circuit board (PCB) interconnections at the stent-rectifier interface when designing tuning network since the parasitics are comparable with the circuit parameters. The parasitic capacitance of ESD devices and bond-pads are extracted from post-layout simulation, the bondwire inductance and interconnection inductance are estimated by using 1 nH/mm and $Q \approx 27$. The design procedure is summarized in Fig. 2.8, several optimization iterations are needed to find design parameters that will use the lowest P_{av} to generate $V_{DC} > 500$ mV on a 2 kΩ load.

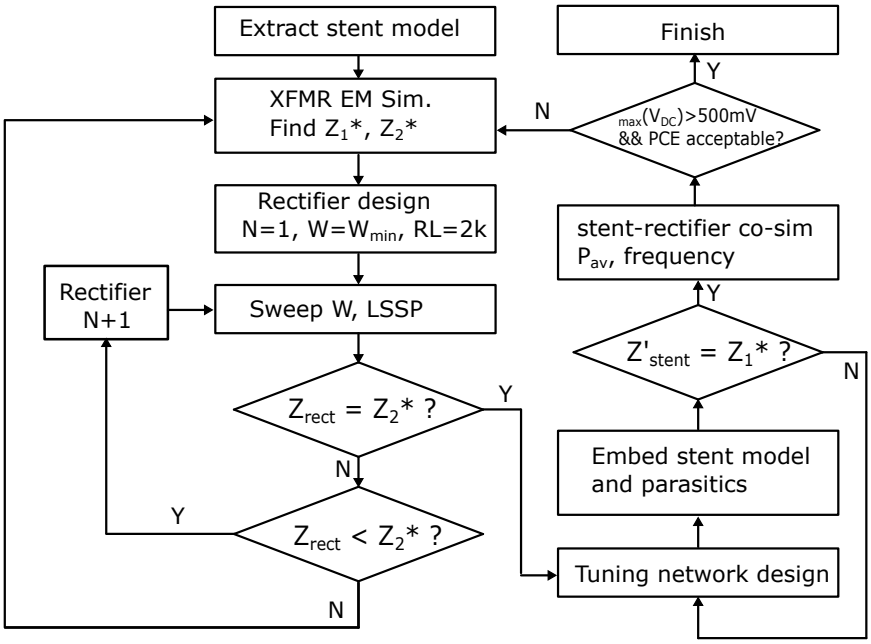


Fig. 2.8. Optimization flowchart.

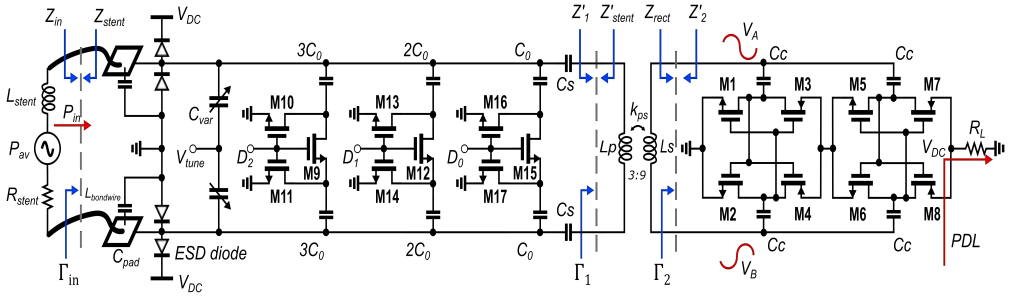


Fig. 2.9. Co-designed rectifier with monolithic transformer-coupled tunable matching network. Γ_{in}, Γ_1 and Γ_2 are the power wave reflection coefficient at CMOS die input, transformer input and rectifier input respectively.

The proposed rectifier with transformer-coupled network is shown in Fig. 2.9. Low-threshold voltage (LVT) transistors are used in this design to enhance the PCE at low P_{av}, and the body of all NMOS transistors are connected to chip ground hence a triple-well process is not required. Transistors M_1 to M_8 will be turned on when the amplitude of the input voltage is close to or greater than V_{th}. Transis-

tors M_9 to M_{17}, capacitors C_0 to $3C_0$ are used for 3-bit coarse tuning and varactors C_{var} are used for fine tuning. The compromise between small switch R_{on} and large capacitance variation ΔC should be taken into consideration when sizing the aspect ratio of M_9 to M_{17}. The stent impedance along with all the interconnection parasitics are transformed to Z'_{stent} as shown in Fig. 2.10 (a) at the transformer primary winding port by the tuning network and the coupling capacitor C_S. The secondary winding of the transformer and a two stage rectifier forms a resonator that is strongly coupled to the stent network. The ESD diodes at the input is biased by the rectifier DC output voltage hence no external supply is required. Because the source impedance presented to the rectifier is complex, the concept of power waves presented in [68] is most suited to evaluate the power efficiency. The power reflection coefficient at the primary transformer port $|\Gamma_1|^2$ and the rectifier input port $|\Gamma_2|^2$ which are annotated in Fig. 2.9, are given as

$$|\Gamma_1|^2 = |\frac{Z'_{stent} - Z'^{*}_1}{Z'_{stent} + Z'_1}|^2, \;\; |\Gamma_2|^2 = |\frac{Z'_2 - Z^*_{rect}}{Z'_2 + Z_{rect}}|^2 \tag{2.16}$$

where Z'_{stent} is the tuning network output impedance with its input port terminated with Z_{stent} and parasitics, Z'_1 and Z'_2 are loaded transformer primary and secondary impedances, respectively. As shown in Fig. 2.10, simultaneous conjugate matching condition is satisfied at frequency where both $|\Gamma_1|^2$ and $|\Gamma_2|^2$ are minimum.

Table 2.1: RECTIFIER DESIGN PARAMETERS.

$M_{1,2,5,6}$	$M_{3,4,7,8}$	M_9	M_{12}	M_{15}
220 μm	330 μm	50 μm	40 μm	30 μm
$M_{10,11,13,14,16,17}$	C_S	C_0	C_C	C_{var}
0.96 μm	1.1 pF	60 fF	30 pF	75 to 160 fF

According to the definition of insertion loss and power waves, the actual transformer *IL* can be estimated by the ratio of input and output powers, namely $10\lg[(1-|\Gamma_1|^2)\cdot\eta'_X\cdot(1-|\Gamma_2|^2)]$. Fig. 2.11 shows simulated voltage and current waveforms of M_1 in the rectifier cell, and it can be seen that the simulated $I_{D1}(\theta)$ and $I_L(\theta)$ are in line with the results calculated by (2.8), where the reverse current has sub-

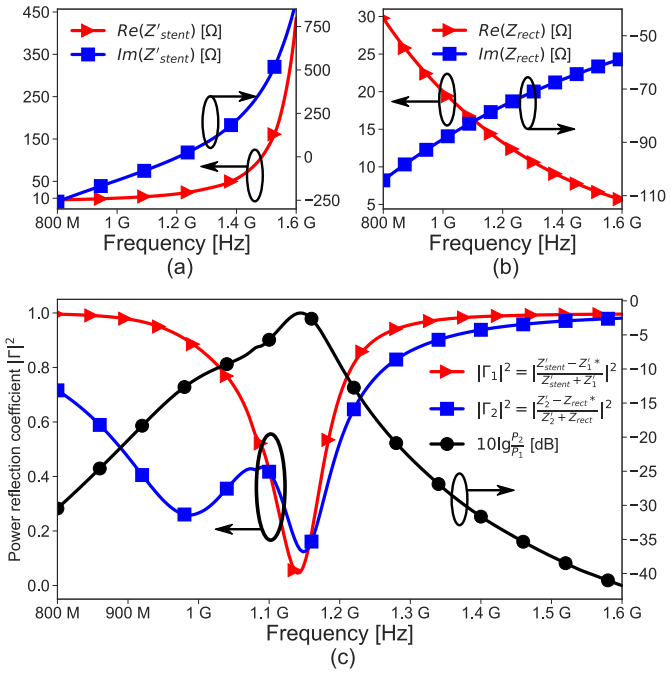


Fig. 2.10. (a) Output impedance of tuning network Z'_{stent} when its input port is terminated with stent model and parasitics. (b) Rectifier input impedance Z_{rect}. (c) Power reflection coefficient $|\Gamma|^2$ and the insertion loss calculated by $10\lg\frac{P_2}{P_1} = 10\lg[(1-|\Gamma_1|^2)\cdot\eta'_X\cdot(1-|\Gamma_2|^2)]$, where the power into the transformer primary is P_1 and the power out of transformer secondary port is P_2.

threshold component only. With all design parameters that are listed in Table 2.1, it is shown in Fig. 2.12 that a V_{DC} greater than 500 mV can be generated at the rectifier output on a 2 kΩ load and requires −2 dBm available power from the stent. The peak rectifier PCE is 34 % at 1139 MHz with $D_2D_1D_0$ all set to '1'. In such a case, 136 µW P_{DL} can be achieved with 403 µW peak input power.

The designed rectifier with the transformer matching network is fabricated in a CMOS 0.13 µm RF process as shown in Fig. 2.13. The die area is $750 \times 1350\,\mu m^2$, however, it can be further reduced by removing the test pads and their ESD blocks after the functionality verification. The rectifier die is tested by using Keysight PNA-X N5242A network analyzer, which supports true-differential mode stimulus

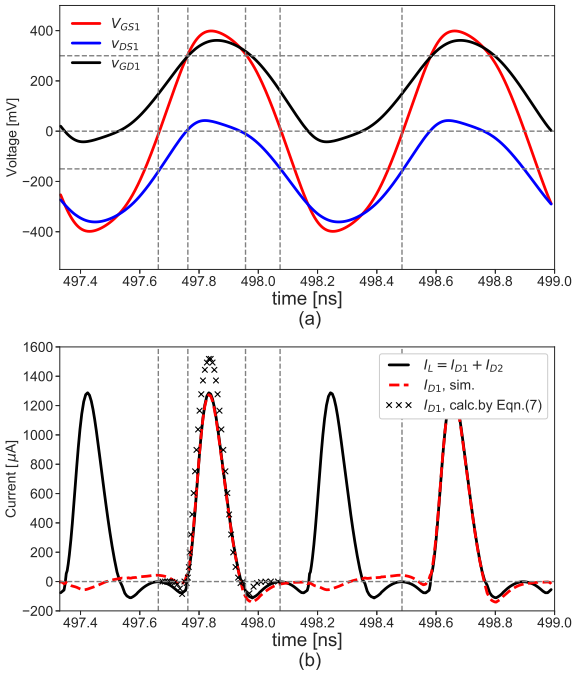


Fig. 2.11. (a) Steady state V_{GS}, V_{DS}, V_{GD} of transistor M_1 and M_2 at 1.2 GHz, $P_{av} = -2$ dBm, R_L=2 kΩ. (b) I_D of transistor M_1 and load current I_L.

in order to measure the mixed-mode S-parameters of the rectifier network. The differential probe (SUSS-Z040-K3N-GSGSG) is calibrated by using **SOLT!** (**SOLT!**) method with an **ISS!** (**ISS!**) first and then circuit input impedance Z_{in} is measured on-wafer. The measured mixed-mode S-parameters is converted to Z-parameters by using Eq. (2.1), and the results are shown in Fig. 2.14. To reproduce the same behavior of a non-50 Ω system in a 50 Ω measurement environment, the same test bench, i.e., same R_S, R_L and P_{av}, is configured in Cadence Virtuoso to validate the measurement results, and in Fig. 2.14 it shows a good agreement between the simulation and measurement.

For this prototype design, the interconnection between the stent and the rectifier die is implemented as shown in Fig. 2.15 (e), where the stent terminals are soldered on PCB trace, and the rectifier chip is connected to the stent in a chip-on-board (COB) configuration. The PCB fixture, is referred to as *Fixture-A*, will introduce parasitic inductance and capacitance on the stent-rectifier interface, therefore, the

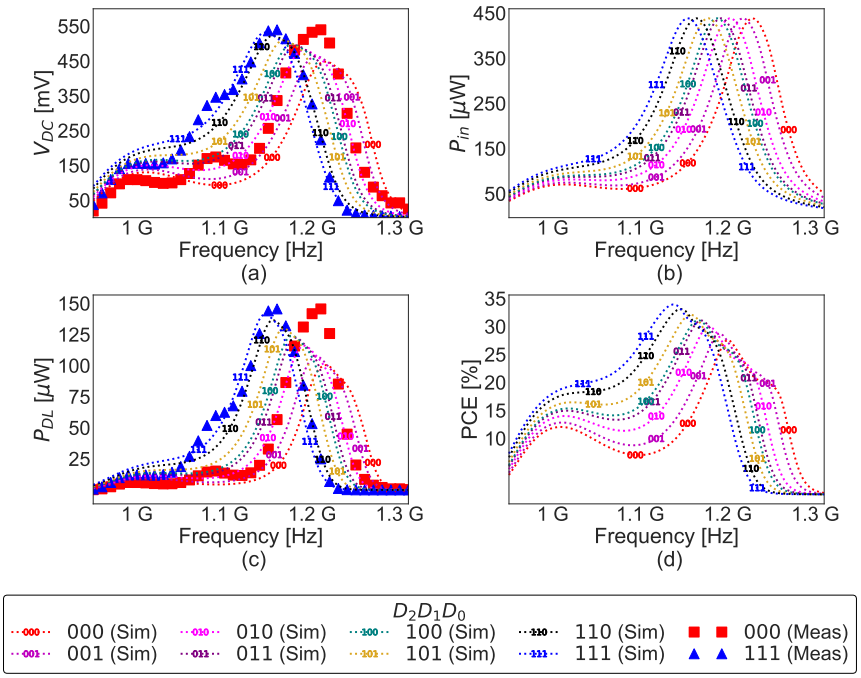


Fig. 2.12. Post-layout simulated and measured results of the rectifier chip with PCB *Fixture-B*, P_{av}=−2 dBm, R_L=2 kΩ. (a) DC output voltage. (b) Input power. (c) Power delivered to load. (d) Rectifier power conversion efficiency.

stent is connected to an additional group of GSGSG pads as illustrated in Fig. 2.15 (b) and measured directly on-wafer to include the parasitic effects that introduced by *Fixture-A*, and the measured stent impedance with PCB parasitics are shown as trace (i) in Fig. 2.2. It can be seen that parasitics shift both R_{stent} and L_{stent} up. Additionally, the parasitic RLC network has been extracted and embedded to the TRL-calibrated Z_{stent} data as shown in Fig. 2.15 (c) , and the simulated response are shown as trace (iii) in Fig. 2.2. From these figures, it can be seen that the simulation results are in good agreement with on-wafer measurements. By using the same technique, the interconnection parasitics can be modeled and de-embedded even with different PCBs or other type of fixtures.

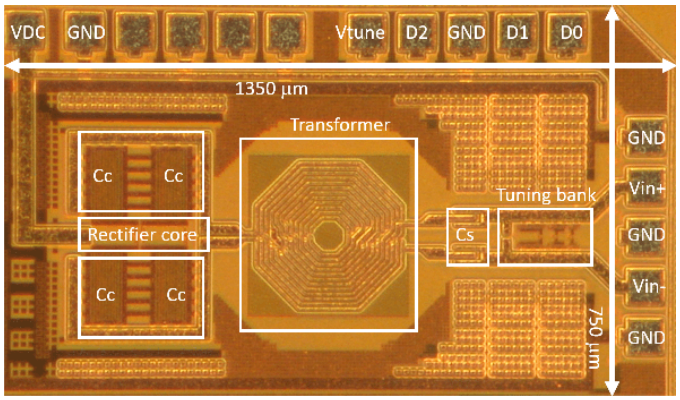


Fig. 2.13. Chip micrograph of the proposed rectifier.

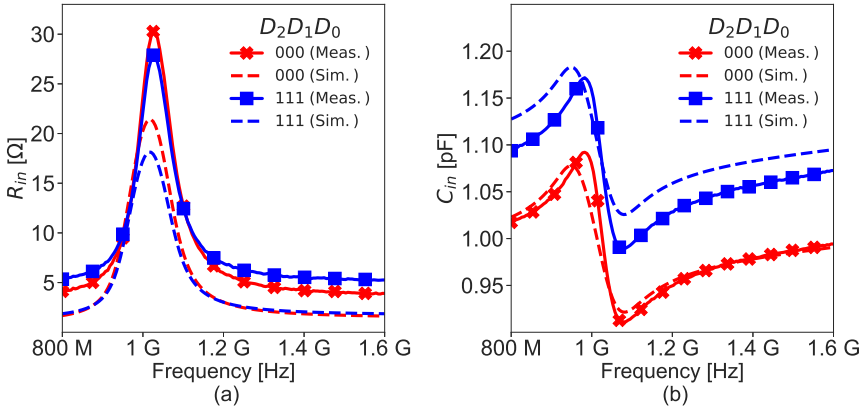


Fig. 2.14. Measured and simulated rectifier chip input impedance Z_{in}, $P_{av} = -5$ dBm, $R_S = 50\,\Omega$.

2.3.4 Rectifier Measurements with Equivalent Stent Model

In order to quantitatively measure the rectifier output voltage V_{DC} for certain P_{av}, an RF signal generator is used to sweep the power and frequency of the rectifier input signal. Sweeping the source available power on different source impedance will lead to different voltage amplitude. However, the response of a non-linear circuit such as the rectifier in this work is highly sensitive to the input voltage level. When using 50 Ω source, it is cumbersome and inaccurate to re-calibrate the power level at the source in order to keep the input voltage amplitude the same as when

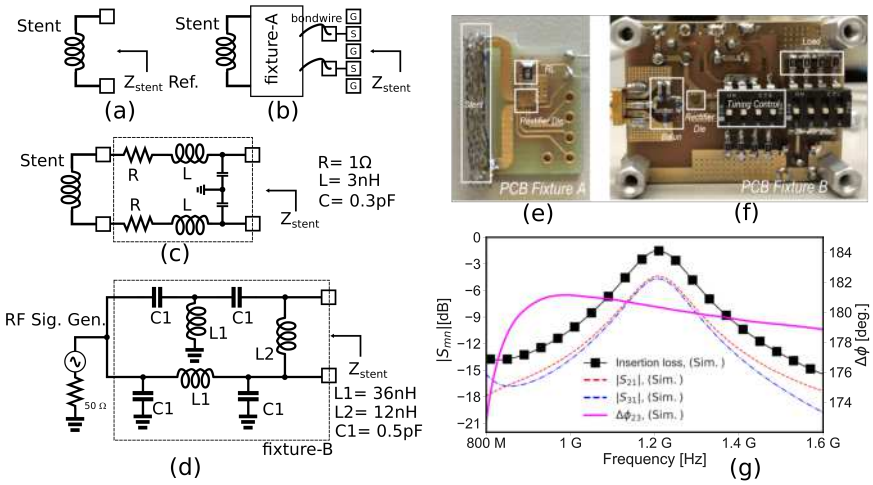


Fig. 2.15. Measurement-oriented stent model. (a) Stent model with TRL calibration. (b) Stent model with *Fixture-A*, measured on-wafer. (c) Stent model with extracted parasitic model of *Fixture-A*. (d) Equivalent stent model used for rectifier efficiency measurement. (e) Stent with *Fixture-A* used for *in-vitro* wireless power transfer experiment. (f) *Fixture-B* used for rectifier power efficiency measurement. (g) Simulated balun response.

the source impedance is not 50 Ω. In this case, additional impedance transformation network is required to measure the true response of the system. Because the stent model is differential and usually the RF signal generator has a single-ended output port, a balanced to unbalanced (Balun) network is designed as shown in Fig. 2.15 (d) to reproduce the Z_{stent} at the output of the source network with its input connected to 50 Ω RF signal generator port. The insertion loss of the balun network is depicted in Fig. 2.15 (g), where the discrete component model (Coilcraft 0603HP inductors, AVX 0603 capacitors) and PCB *Fixture-B* in Fig. 2.15 (f) are co-simulated using ADS Momentum. The output impedance of the balun model, or the measurement-oriented stent model is also depicted as trace (iv) in Fig. 2.2. It shows that the proposed measurement-oriented equivalent stent model fits closely to the on-wafer measurement results. Therefore, this equivalent stent model can be used as a replica of the real stent on *fixture-A* to characterize the rectifier performance in a 50 Ω test environment. The insertion loss of the balun network is de-embedded from the signal generator source power based on the result shown in

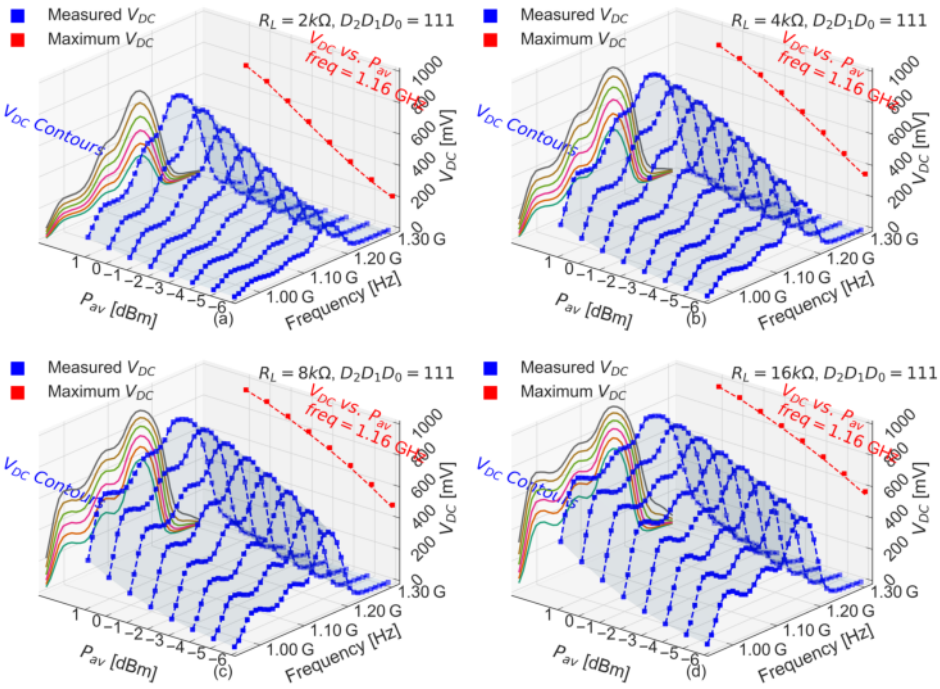


Fig. 2.16. Measured rectifier DC output voltage V_{DC} with the equivalent stent model in Fig. 2.15(d). (a) R_L=2 kΩ. (b) R_L=4 kΩ. (c) R_L=8 kΩ. (d) R_L=16 kΩ.

Fig. 2.15 so that P_{av} becomes more accurate. In the measurements, the logic '1' of the control bits $D_2D_1D_0$ is 500 mV and logic '0' is 0 V. It should be noted that if the control voltage is higher, it will greatly increase the measured rectifier PCE since R_{on} of the switches (i.e., $M_{9,12,15}$ in Fig. 2.9) will be reduced, however, the worst-case scenario should be investigated to guarantee the normal system functionality in a typical biomedical application. Fig. 2.16 shows the measured V_{DC} for different load R_L. The available power is swept from −6 dBm to +1 dBm for 2 kΩ, 4 kΩ, 8 kΩ and 16 kΩ load R_L, the results show that the V_{DC} will increase with R_L especially when P_{av} is low. For higher P_{av}, $\frac{dV_{DC}}{dP_{av}}$ is getting smaller, because the rectifier PCE will be degraded due to the higher reverse current when V_{DC} is greater than $2V_{th}$ as explained in Section 2.3.

2.4 Optimal External Source Synthesis

As discussed in Chapter 1, the optimal frequency of WPT for devices that implanted in deep tissue is in the lower GHz range. For a typical source to load separation of several centimeters, the separation distance is comparable to the wavelength in the tissue so that the power transfer operates in midfield and depends on the diffraction effects in tissue. An analytical bound on the efficiency of wireless power transfer to a weakly coupled implant in deep tissue is presented in [5][63], where the Maxwell's equations are solved in the multilayer tissue structure by using angular spectrum method, and the source current density that yield optimal efficiency is derived in spatial domain by using inverse Fourier transform. It turns out that the optimal source surpasses the performance of coil-type source by a factor of 4, however, the theoretical solution does not yield a physical source representation but only gives the insight on how to approach the optimal source. A source realization is proposed in [63] [18], where a 4-element slot array is synthesized at 2.6 GHz and 1.6 GHz respectively to manipulate the phase of the current in order to approach the theoretical optimal source. However, the implementations are based on a reduced view of the optimal source current density hence are simplified implementations. In this work, a more detailed realization of the optimal source current distribution is proposed at 1.2 GHz as shown in Fig. 2.17.

The phase of the excitation at port 1 and 2, $\phi_{1,2} = 0^\circ$, and $\phi_{3,4} = 180^\circ$ at port 3 and 4, where the magnitude for all the ports are the same. As shown in Fig. 2.17 (b), the current distribution pattern have following features: (i) The dominant current paths are semicircular and symmetric with respect to x-axis. (ii) The spacing between adjacent paths is roughly $\lambda/4$ and out-of phase. (iii) The peak current magnitude appears at roughly $\lambda/2$ away from origin. The above features result in constructively interfering the magnetic fields in the direction of power transfer therefore the local power density is enhanced. The antenna is optimized for $50\,\Omega$ interface, where the port impedance is tuned by sizing the co-planar waveguide (CPW) shunt stub without changing the current pattern significantly. Therefore, no external matching network is required for the antenna. The simulated results in Fig. 2.17 (c) show that, regardless of the presence of the tissue model in Table 2.2, each port is well matched to the $50\,\Omega$ power source. In addition, it can be

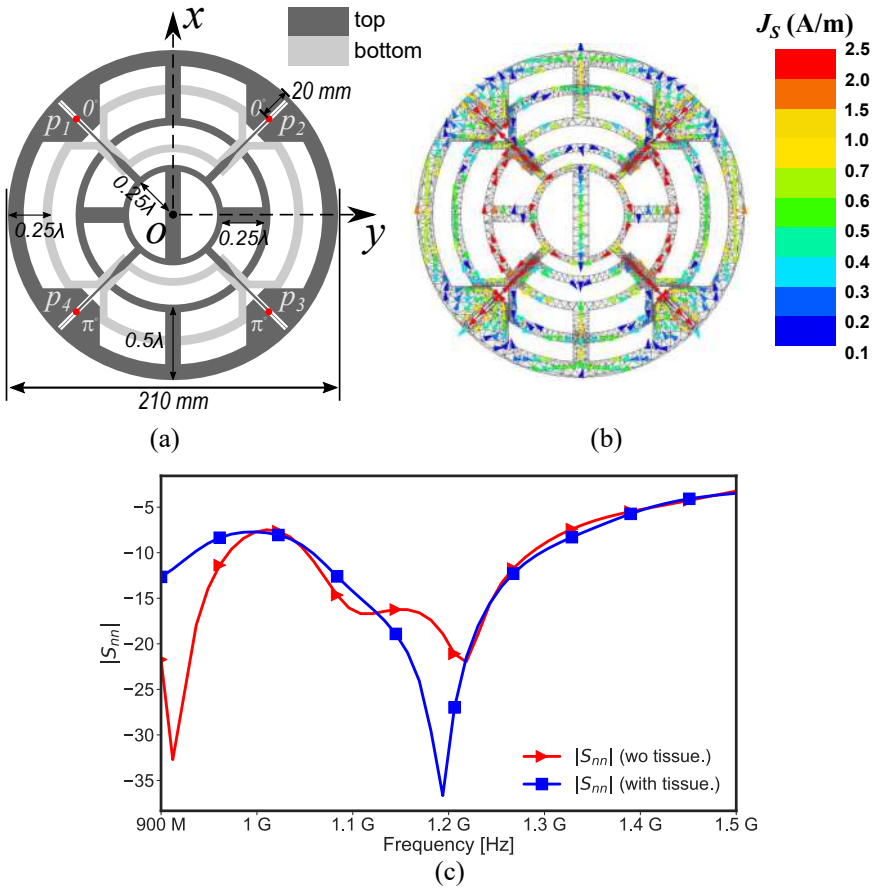


Fig. 2.17. Proposed 4-port antenna. (a) Antenna layout. (b) Simulated current distribution. (c) Simulated $|S_{nn}|$, $n \in [1,4]$.

Table 2.2: MULTI LAYER TISSUE MODEL.

Tissue type	ε_r	$\tan\delta$	thickness (mm)
Skin	35.83	0.158	2
Fat	11.44	0.123	10
Bone	20.19	0.181	16
Muscle	53.74	0.173	8
Heart	53.68	0.120	30

observed that with the presence of tissue the center frequency will shift down since the transmitted power is coupled to tissue. The magnetic field is also illustrated in Fig. 2.18 (a) to (d), where it shows that the fields are focused in -z-direction. The magnetic field intensity at the depth of 50 mm inside the tissue, $|\mathbf{H}|_{(0,\,0,\,0)}$ is attenuated 3∼6 dBs compared with $|\mathbf{H}|_{(0,\,0,\,50)}$ on the tissue surface. The detailed multi-layer tissue model parameters are listed in Table 2.2, and the air gap between the source and tissue surface is 10 mm. Fig. 2.18 (e)-(f) show that the specific ab-

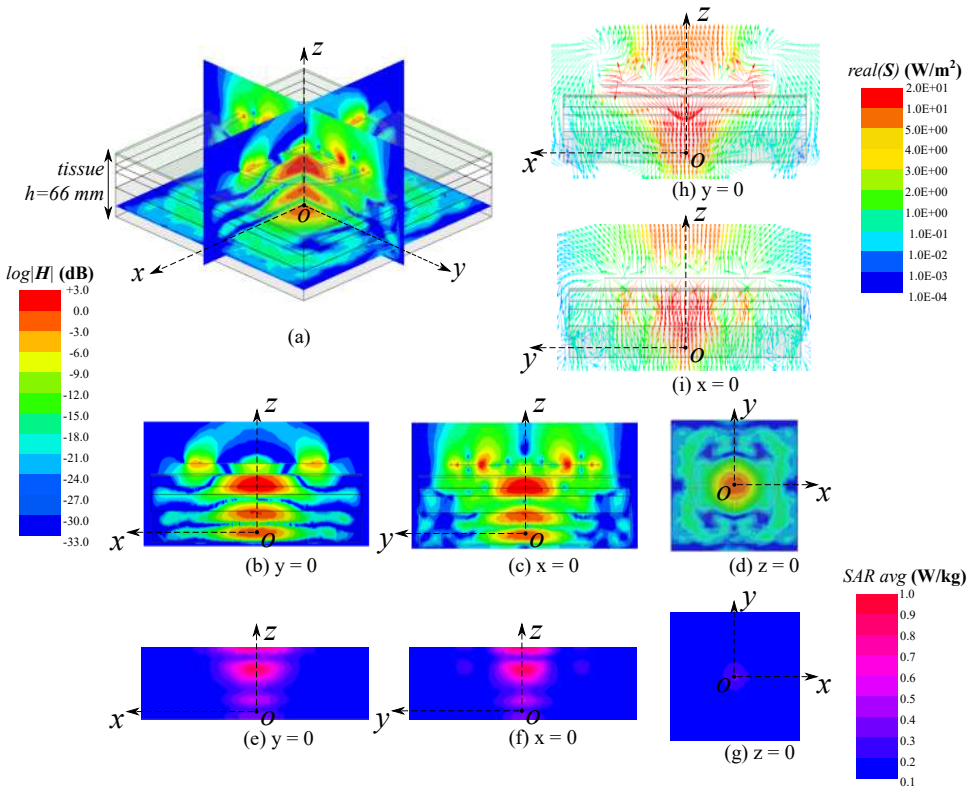


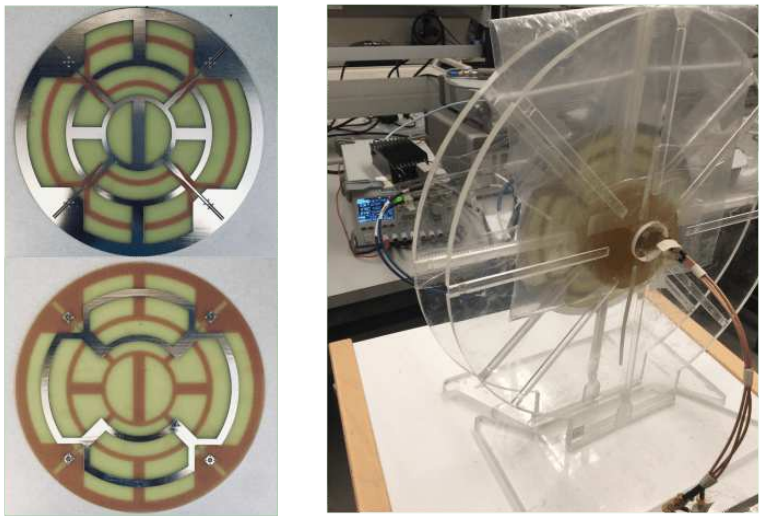
Fig. 2.18. Simulated antenna performance at 1.2 GHz, P_{in}=480 mW. The Maxwell equations are solved by using 3D EM solver HFSS. (a)-(d) Magnetic field intensity. (e)-(g) SAR field, averaged over 1g of tissue. (h)-(i) Poynting vector.

sorption rate (SAR) field averaged over 1 g of tissue is less than 1 W/kg when the total input power is 480 mW (120 mW source power is applied at each of the four ports), which is much less than the 1.6 W/kg SAR safety threshold in North

America. The Poynting vector is also plotted in Fig. 2.18 (h) and (i), from which it can be observed that the proposed antenna generates converging power flow lines inside the tissue.

2.4.1 In-vitro Wireless Power Transfer Experiment

The setup of the *in-vitro* wireless power transfer experiment for the proposed "smart stent" system is shown in Fig. 2.19. The phantom tissue with the thickness of 33 mm is prepared exactly as reported in [69], and the oil percentage of the recipe is 15 % in this work to mimic the muscle tissue. The external antenna is placed 20 mm away from the phantom tissue, and two in-phase and two out-of phase signals are generated by using one two-way 0-180° balun (Mini-Circuit ZAPDJ-2) and two power splitters to feed the four ports of the antenna. The power into the antenna ports $P_{in,\,ant}$ are pre-calibrated by using Agilent E4481B RF power meter to exclude the power loss caused by the power splitter, balun and co-axial cables. At the implanted side, a 2 kΩ resistor is connected to the rectifier output and the DC output voltage of the rectifier is measured by Agilent 34401A multimeter. The



(a) (b)

Fig. 2.19. (a) Fabricated antenna on 1.6 mm FR-4 substrate. (b) *In-vitro* experiment setup.

measured system frequency response is illustrated in Fig. 2.20, from which it shows that for 480 mW external antenna input power $P_{in,\,ant}$ and 53 mm separation distance (20 mm air and 33 mm tissue), the maximum output voltage V_{DC} is 840 mV at 1078 MHz, corresponding to 353 µW **PDL!** (**PDL!**). The results in Fig. 2.20 (a) also show that with only 300 mW external source power is required to achieve more than 500 mV V_{DC} or 125 µW for the worst case scenario (i.e., without changing the tuning code). The performance of the "smart stent" system is summarized and compared with other state-of-the-arts in Table 2.3.

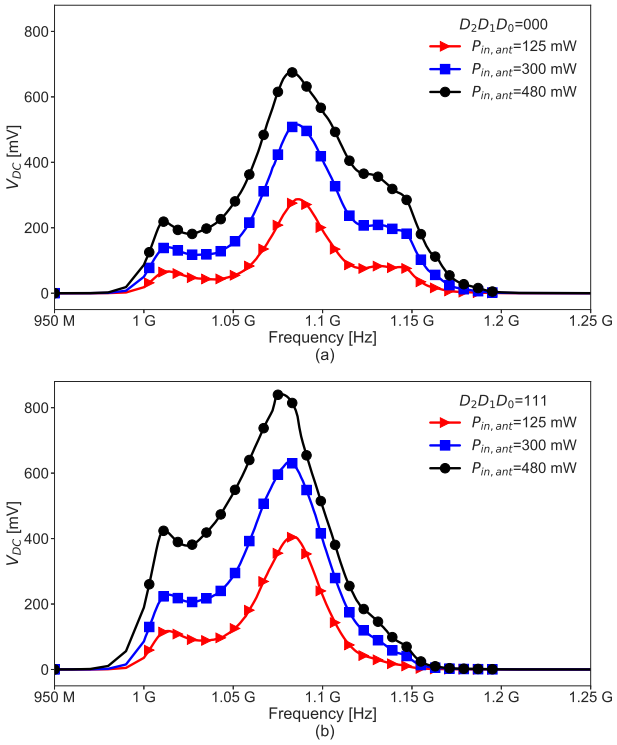


Fig. 2.20. Measured rectifier DC output voltage V_{DC} *vs.* external antenna input power $P_{in,\,ant}$. R_L=2 kΩ, separation distance=53 mm, phantom tissue thickness=33 mm. (a) $D_2D_1D_0 = 000$. (b) $D_2D_1D_0 = 111$.

Table 2.3: PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ARTS.

	This work	ISSCC'09 [30]	ISSCC'17 [31]	TBioCAS'12 [60]	TBioCAS'16 [17]	TCASI'17 [28]	JSSC'14 [32]
Application	Biomedical	Biomedical	Biomedical	Biomedical	Biomedical	RFID	RFID
CMOS Technology	0.13 μm	0.13 μm	0.18 μm	65 nm	65 nm	0.13 μm	90 nm
Frequency	1.1 GHz	915 MHz or 1 GHz	434 MHz	1.86 GHz	1.3 GHz	2 GHz	868 MHz
Rectifier Topology	Cross-coupled	Cross-coupled	Charge-pump	Cross-coupled	Cross-coupled	Differential drive Cross-coupled	Cross-coupled
Rectifier Stages	2	3	4	4	4	3	5
Rx Antenna	15 mm Stent d=2.5 mm	Square loop 2×2 mm	2-turn coil d=2.8 mm	Square loop 2×2 mm	Square loop 2×2 mm	Signal generator 50 Ω port	Square loop 21.9 cm^2
Matching Type	Tuned XFMR	2-element L-network	2-element L-network	2-element L-network	No matching	NA	Capacitor bank
Inter-Antenna Dielectric	20 mm air gap +33 mm tissue	15 mm tissue	5 mm tissue	50 mm	35 mm tissue	NA	27 m in the air
PDL @Tx power	353 μW @480 mW	140 μW @250 mW	48.9 μW	500 μW @2 W	10.7 μW @125 mW	NG	8 μW † @1.78 W
Unregulated Voltage	0.5∼0.84 V	$>$ 1.2 V	1.35 V	0.2 V	0.8∼1.2 V	0.5 V	1.6 V
Rectifier Load	R_L=2 kΩ	R_L=12 kΩ	Resistive	R_L=100 Ω	R_L=48 kΩ	R_L=2 kΩ	R_L=330 kΩ
Rectifier PCE @Rx P_{av}	34% @−2 dBm	65%	15.85%	55% @0 dBm	50% @−17 dBm	25% @−2 dBm	40% @−17 dBm
Chip Area (mm^2)	0.75×1.35	0.75×1.4	0.75×0.75	0.33×0.67	0.4×0.63	0.127×0.23 ‡	0.12×0.24 ‡

† The PDL and 1.6 V V_{DC} are derived from the reported 40% PCE when P_{in}=−17 dBm, R_L=330 kΩ.
‡ The area contains rectifier block only.

Chapter 3

The Design of Low-Voltage Low-Power Low Drop-out Regulator

As discussed and demonstrated in previous Chapter 2, the available power can be delivered to the implanted system is low. Therefore, low power / supply voltage circuit topologies and design techniques are desired to make the RF and analog blocks practical. For low-speed low-power biomedical applications, a suitable voltage regulator design should have following features:

a) High power efficiency The power efficiency η_p can be written as

$$\eta_p = \frac{I_L}{I_L + I_Q} \cdot \frac{V_{DD} - V_{drop}}{V_{DD}} = \eta_i \cdot (1 - \frac{V_{drop}}{V_{DD}}), \tag{3.1}$$

where I_L, V_{DD}, V_{drop} and η_i are the load current, input voltage, dropout voltage across pass transistor and current efficiency of the regulator, respectively. From Eq. (3.1) it can be seen that low V_{DD} value, low V_{drop}/V_{DD} ratio, and high η_i will enhance η_p of the LDO.

b) Wide input range The output voltage of the rectifier stage is highly dependent on the available power at its input and the load current, hence the LDO's input voltage can have a large variation.

c) Fully on-chip implementation No external off-chip capacitor should be used to stabilize the regulator. The output capacitor-less topology should be used to make the design compact.

d) Robust to PVT variation Low voltage analog designs are susceptible to process, supply voltage and temperature variations.

Although digital LDOs (DLDOs) can be used for low supply voltage applications, their transient response is usually slow and they require a clock signal to operate. Moreover, DLDOs have intrinsic output ripple which is due to limit cycle oscillation (LCO) that is induced by the inherent quantization error of the finite resolution ADCs. In this work, an analog LDO is used because of its faster response and lower power.

3.1 Review of low-power low drop-out regulators

In [45], an output-capacitorless low-dropout regulator compensated by a single Miller capacitor is implemented in a 90 nm CMOS process. The proposed LDO makes use of the small transistors realized in nano-scale technology to achieve high stability, fast transient performance and small voltage spikes under rapid load-current changes without the need of an off-chip capacitor connected at the LDO output. Experimental result verifies that the proposed LDO is stable for a capacitive load from 0 to 50 pF and with load capability of 100 mA. Moreover, the gain-enhanced structure provides sufficient loop gain to improve line regulation to 3.78 mV/V and load regulation to 0.1 mV/mA, respectively. The embedded voltage-spike detection circuit enables pseudo Class-AB operation to drive the embedded power transistor promptly. The measured power consumption is only 6 μW under a 0.75-V supply. The maximum overshoot and undershoot under a 1.2 V supply are less than 66 mV for full load current changes within 100 ns edge time, and the recovery time is less than 5 μs. In [70], a digital LDO is designed in 65 nm CMOS achieved 0.5-V input voltage and 0.45-V output voltage with 98.7% current efficiency and 2.7 μA quiescent current at 200-μA load current. In [49], an output-capacitorless LDO with a direct voltage-spike detection circuit is presented. The proposed voltage-spike detection is based on capacitive coupling. The detection circuit makes use of the rapid transient voltage at the LDO output to increase the

bias current momentarily. Hence, the transient response of the LDO is significantly enhanced due to the improvement of the slew rate at the gate of the power transistor. The proposed voltage-spike detection circuit is applied to an output-capacitorless LDO implemented in a standard 0.35 μm CMOS technology. Experimental results show that the LDO consumes 19 μA only. It regulates the output at 0.8 V from a 1 V supply, with dropout voltage of 200 mV. at the maximum output current of 66.7 mA. The voltage spike and the recovery time of the LDO with the proposed voltage spike detection circuit are reduced to about 70 mV and 3 μs, respectively, whereas they are more than 420 mV and 30 μs for the LDO without the proposed detection circuit. In [71], an analog-assisted output-capacitorless digital LDO with tri-loop control is presented. For responding to instant load transients, the proposed high-pass analog-assisted loop momentarily adjusts the unit current of the power switch array, and significantly reduces the voltage spikes. In the proposed LDO, the overall 512 output current steps are divided into three sub-sections controlled by coarse/fine loops with carry-in/out operations. Therefore, the required shift register length is reduced, and a 9-bit output current resolution is realized by using only 28-SR bits. Besides, the coarse-tuning loop helps to reduce the recovery time, while the fine-tuning loop improves the output accuracy. To eliminate the limit cycle oscillation and reduce the quiescent current, a freeze mode is added after the fine tuning operation. To reduce the output glitches and the recovery time, a non-linear coarse word control is designed for the carry-in/out operations. The LDO is fabricated in 65 nm CMOS process. A maximum voltage undershoot/overshoot of 105 mV is measured with a 10 mA/ns load step and a total capacitor of only 100 pF.

3.2 Analysis of Low Drop-out Regulator

3.2.1 Linear model of voltage-feedback LDO

The LDO is designed to maintain a constant output voltage regardless its input voltage and output current variations, in other words, the LDO mimics an ideal voltage source. For small supply voltage V_{DD} and load current I_L change, the operation of the LDO can be analyzed by using classical linear (small-signal) feedback model.

However, the linear model might not be valid for large load variation during a short time slot.

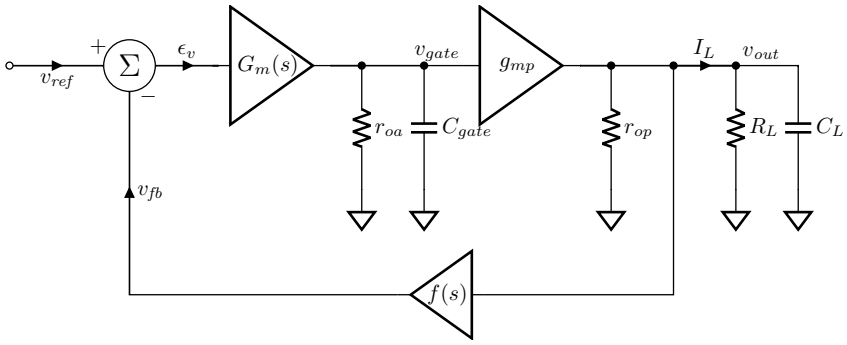


Fig. 3.1. Simplified LDO linear model

The simplified linear model of a typical LDO loop is shown in Fig. 3.1. Assuming the input impedance of the feedback network $f(s)$ is infinity for an ideal voltage feedback topology, the loop transmission $L(s)$ can be derived by breaking the loop at the input of $f(s)$:

$$\begin{aligned} L(s) &= f(s)\cdot G_m(s) r_{oa}\cdot g_{mp}(r_{op}\,||\,R_L)\cdot \frac{1}{1+sr_{oa}C_{gate}}\cdot \frac{1}{1+s(r_{op}\,||\,R_L)C_L} \\ &= f(s)\cdot G_m(s) r_{oa}\cdot g_{mp}(r_{op}\,||\,R_L)\cdot \frac{1}{1+s/p_{gate}}\cdot \frac{1}{1+s/p_{out}}, \end{aligned} \tag{3.2}$$

where the gate pole can be expressed as:

$$p_{gate} = \frac{1}{\tau_g} = \frac{1}{r_{oa}C_{gate}}, \tag{3.3}$$

and the output pole can be written as:

$$p_{out} = \frac{1}{\tau_o} = \frac{1}{(r_{op}\,||\,R_L)C_L}, \tag{3.4}$$

$G_m(s)$, r_{oa} are the stage transconductance and the small-signal output resistance of the error amplifier, g_{mp} and r_{op} are the transconductance and output resistance

of the pass transistor, respectively. All capacitance at the gate node of the pass transistor are lumped into C_{gate}, and the lumped capacitance at the output node is written as C_L. It should be noted that the error amplifier can have more than one stage, or in other words, more than one high impedance node. To make the loop stable, the poles inside $G_m(s)$ have to be at a much higher frequency then p_{gate} and p_{out}, or be compensated by left half plane (LHP) zeros. If assuming all parasitic poles of $G_m(s)$ are at frequency much higher than the unity gain frequency (UGF) of the LDO loop, and the feedback network $f(s)$ is frequency independent, the loop transmission can be simplified and written as:

$$\begin{aligned} L(s) &\approx f(0)\cdot G_m(0) r_{oa}\cdot g_{mp}(r_{op}\,||\,R_L)\cdot \frac{1}{1+s/p_{gate}}\cdot\frac{1}{1+s/p_{out}} \\ &= \frac{L_0}{(1+s/p_{gate})(1+s/p_{out})}. \end{aligned} \tag{3.5}$$

In fact, the LDO is not a static loop due to the movement of p_{gate}, p_{out} and the change of DC loop gain $|L_0|$ that caused by the load current variations, which can be explained as follows. For most commonly used LDO topologies, the pass transistor is usually p-type because the required minimum drop-out voltage is only one V_{dsat}, that is at least one V_{th} lower compared with its n-type counterpart. The output resistance r_{op} is determined by the channel length modulation of MOS transistors, and it is inversely proportional to the drain current:

$$r_{op} = \frac{V_E}{I_D} \approx \frac{V_E}{I_L}, \tag{3.6}$$

where V_E is the Early voltage which is a process dependent parameter. The equivalent load resistance R_L is evaluated by

$$R_L = \frac{V_{out}}{I_L}. \tag{3.7}$$

Therefore, the total resistance at the output node can be derived by using Eqs. (3.6) and (3.7):

$$r_{out} = r_{op}\,||\,R_L = \frac{1}{I_L}\cdot(V_E\,||\,V_{out}). \tag{3.8}$$

Substitute Eq. (3.8) into Eq. (3.4), the output pole can be re-written as:

$$p_{out} = \frac{I_L}{C_L} \cdot \frac{1}{(V_E \,||\, V_{out})}. \tag{3.9}$$

As shown in Eq. (3.9), *for certain output voltage V_{out} and C_L, the output pole p_{out} will be pushed up to higher frequency by increasing the load current.* In addition, Eq. (3.9) also indicates that the location of p_{out} is proportional to the slew rate of the pass device. The small-signal transconductance, g_{mp}, of the pass transistor is also related to I_L, which will result in the change of p_{gate} and $|L_0|$. Depending on I_L, the pass transistor will be operating in different regions. For certain aspect ratio W/L and over-drive voltage V_{ov}, by taking partial derivative of Eq. (2.5) with respect to V_{GS}, the expression of small signal transconductance can be derived as

$$g_{mp} = \frac{\partial I_D}{\partial V_{GS}} \approx \begin{cases} \sqrt{2K' \frac{W}{L} I_L}, & \textit{strong-inversion} \\ \\ \frac{I_L}{\xi V_T} = \frac{I_L}{V_T} \cdot \frac{C_{ox}}{C_{ox} + C_{dep}}, & \textit{weak-inversion} \end{cases} \tag{3.10}$$

where it can be concluded that *the g_{mp} is linearly related to I_L when the load is light, but $g_{mp} \propto \sqrt{I_L}$ when the load is heavy.*

If ignore the output capacitance from the error amplifier, the capacitance at the gate node of the pass MOS transistor can be written as:

$$C_{gate} = C_{gb} + C_{gs} + (1 + g_{mp} r_{out}) C_{gd}\,. \tag{3.11}$$

When the transistor is in saturation and its channel is in strong inversion, the intrinsic portion of $C_{gd} \approx 0$ due to the channel is pinched off at the drain node, but the extrinsic unit length overlap capacitance C_{ov} still plays an important role due to the Miller effect. On the other hand, the intrinsic portion of $C_{gs} \approx 0$ when the transistor is in weak inversion since no channel exists below the surface, hence $C_{gd} \approx C_{gs} \approx W \cdot C_{ov}$. Therefore, Eq. (3.11) can be further formulated by substitut-

ing Eqs. (3.8) and (3.10):

$$C_{gate} \approx \begin{cases} \frac{2}{3}WL \cdot C_{ox} + [1 + (V_E \,||\, V_{out})\sqrt{\frac{W}{L} \cdot \frac{2K'}{I_L}}]W \cdot C_{ov}\,, & \textit{strong-inversion} \\ WL \cdot \frac{C_{ox}C_{dep}}{C_{ox}+C_{dep}} + [1 + \frac{V_E \,||\, V_{out}}{V_T} \cdot \frac{C_{ox}}{C_{ox}+C_{dep}}]W \cdot C_{ov}\,, & \textit{weak-inversion} \end{cases} \tag{3.12}$$

The depletion capacitance C_{dep} is a function of surface potential ψ_s where the detailed analysis can be found in [72]. In weak / moderate inversion, C_{dep} is inversely proportional to ψ_s, or the gate-body voltage V_{gb}, same as the case for the depletion capacitance of a reversely biased *pn* junction. When the boundary between weak / moderate and strong inversion is reached, namely when $\psi_s \approx 2\phi_F$, the depletion width reaches its maximum, results in minimum depletion capacitance hence minimum value of C_{gb}. The unit gate-bulk capacitance C'_{gb} can be written as:

$$C'_{gb,min} = \frac{C_{ox}C_{dep,min}}{C_{ox}+C_{dep,min}} \approx \frac{C_{ox}}{1+(2/\gamma)\sqrt{2\phi_F}}, \tag{3.13}$$

where $\gamma = \sqrt{2q\varepsilon_{si}N_{dep}}/C'_{ox}$ is the body-effect coefficient. By combining the results from Eqs. (3.12) and (3.13), the variation of C_{gate} for different load current values can be depicted in Fig. 3.2. Based on aforementioned discussion, the movement of p_{gate} and p_{out} that caused by I_L is shown as Fig. 3.3. For either p_{gate} dominant (i.e. $p_{gate} > p_{out}$, Fig. 3.3 a) or p_{out} dominant (i.e. $p_{gate} > p_{out}$, Fig. 3.3 b) cases, the separation distance between these two open-loop poles varies for different I_L. However, the smallest pole-separation distance happens at different I_L for these two cases. Specifically, if p_{gate} is the dominant pole, the distance between p_{gate} and p_{out} is smallest when $I_L = I_a$. This is due to C_{gate} has its minimum value at I_a. On the other hand, if p_{out} dominates, the smallest pole-separation distance happens at $I_L = I_b$, correspond to the maximum value of C_{gate} that is caused by the Miller-effect.

By combining Eqs. (3.2) to (3.4), (3.8), (3.10) and (3.12), the DC loop gain

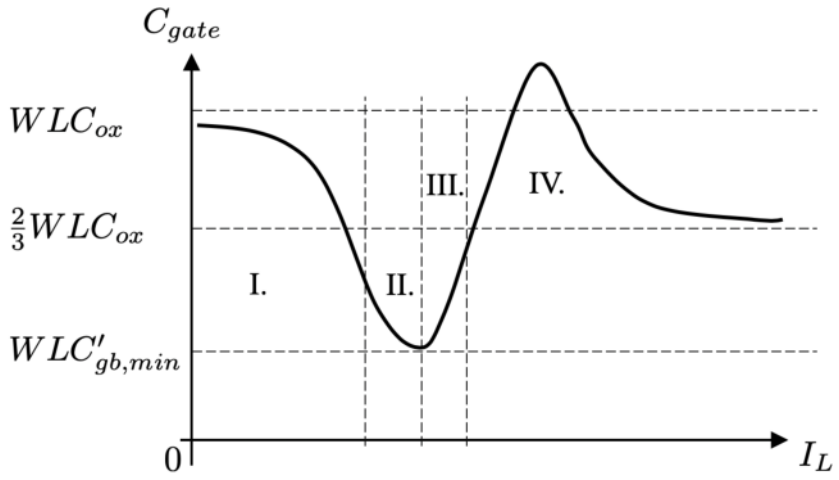


Fig. 3.2. Gate capacitance C_{gate} *vs.* I_L. I. depletion II. weak-inversion III. moderate-inversion IV. strong-inversion

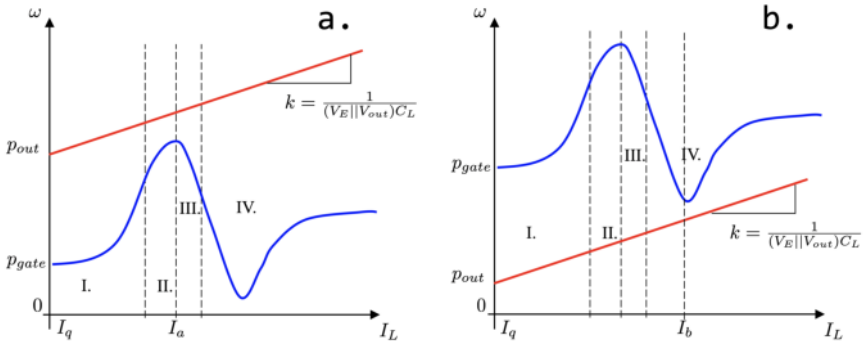


Fig. 3.3. p_{gate}, p_{out} *vs.* I_L. a). p_{gate} as the dominant pole. b). p_{out} as the dominant pole.

$|L_0|$ in Eq. (3.2) can be re-written as:

$$|L_0| \approx \begin{cases} |f(0)G_m(0)|r_{oa} \cdot \sqrt{2K'\dfrac{W}{L}} \cdot \dfrac{V_E \,||\, V_{out}}{\sqrt{I_L}}, & \textit{strong-inversion} \\ |f(0)G_m(0)|r_{oa} \cdot \dfrac{C_{ox}}{C_{ox}+C_{dep}} \cdot \dfrac{V_E \,||\, V_{out}}{V_T}, & \textit{weak-inversion} \end{cases} \tag{3.14}$$

For the weak-inversion case of Eq. (3.14), the impact of I_L on the depletion capacitance C_{dep} can be observed from Fig. 3.2 since the variation of C_{gate} is solely caused by C_{dep}. On the other hand, when the transistor is in strong-inversion, $|L_0|$ is monotonically reduced if I_L is increased.

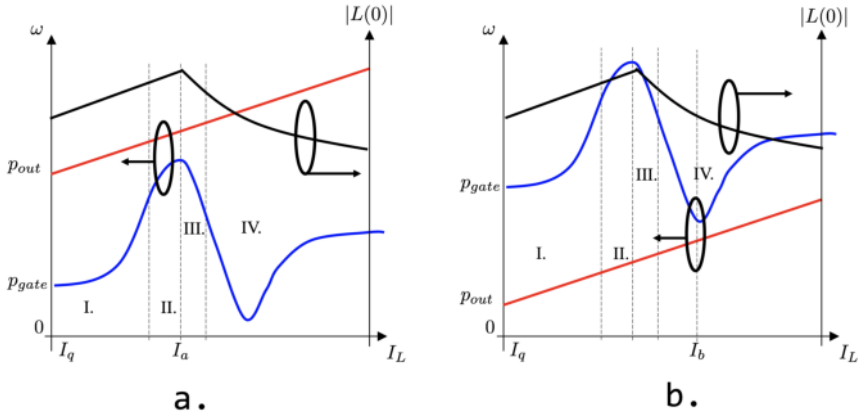


Fig. 3.4. $|L_0|$ *vs.* I_L. a). p_{gate} as the dominant pole. b). p_{out} as the dominant pole.

Based on aforementioned discussion, $|L_0|$ is plotted in Fig. 3.4, from which it can be observed that for p_{gate} dominant case, $|L_0|$ reaches its maximum value when the separation distance between the two poles are smallest. Therefore, the worst phase margin happens at $C_{dep} = C_{dep,min}$ at weak-inversion. However, the worst phase margin appears at a higher load current for p_{out} dominant case, since when $|L_0|$ peaks the pole separation is not at its smallest value.

For voltage feedback LDO topologies, the error voltage $\varepsilon_v = V_{ref} - f \cdot V_{out}$ is amplified to control the V_{sg} of the p-type pass transistor, hence the current flow

through the biasing branch at the output I_b is adjusted to maintain a fixed V_{out}. The "ideal" closed-loop transfer function (i.e., the closed-loop transfer function when the loop gain is infinity) of the LDO at DC, $H_\infty(0)$, can be derived as:

$$H_\infty(0) = \frac{V_{out}}{V_{ref}} = \frac{1}{f(0)}, \tag{3.15}$$

where, it follows that if the DC loop gain $|L_0|$ is sufficiently large and approaches infinity, the negative feedback loop forces V_{OUT} to track V_{REF}, and because $f(0)$ can be made relatively constant by using passive feedback network such as resistive divider, the absolute accuracy of V_{out} mainly relies on V_{ref}. However, $|L_0|$ is bounded to a finite value in reality as shown in Eq. (3.14), and the gain bandwidth product, *GBW*, of the loop is usually proportional to the power consumption. Therefore, there will be a finite error between $f \cdot V_{out}$ and V_{ref}, and the closed-loop error transfer function of can be expressed as:

$$E(s) = \frac{\varepsilon_v(s)}{V_{ref}} = \frac{1}{1+L(s)} = \frac{(1+s\tau_g)(1+s\tau_o)}{1+L_0+(\tau_g+\tau_o)s+\tau_g\tau_o s^2}. \tag{3.16}$$

From Eq. (3.16) it is obvious that the error will be suppressed by the loop gain and hence high loop gain is desired. However, it is not possible to keep such a system stable at all frequencies with high $L(s)$. Instead, a practical negative feedback system only needs to maintain a reasonable high loop gain within the desired frequency band to suppress the in band error below certain value. Since the order of the loop is more than one (the order will be higher than two if the parasitic poles of the error amplifier is also taking into consideration), the stability of the loop should be scrutinized. In fact, the magnitude of loop gain will be eventually limited by the instability. The denominator polynomial of Eq. (3.16) is the characteristic equation of the loop, and can be re-written as standard form:

$$D_e(s) = s^2 + 2\zeta\omega_n s + \omega_n^2. \tag{3.17}$$

where the damping factor ζ is:

$$\zeta = \frac{1}{2} \cdot \frac{1}{\sqrt{1+L_0}} \cdot \frac{\tau_g+\tau_o}{\sqrt{\tau_g\tau_o}} = \frac{1}{2\omega_n} \cdot \frac{\tau_g+\tau_o}{\tau_g\tau_o}, \tag{3.18}$$

and the natural frequency ω_n is:

$$\omega_n = \sqrt{\frac{1+L_0}{\tau_g \tau_o}}. \tag{3.19}$$

The roots of Eq. (3.17) are the poles of the closed-loop transfer function, and can be derived as:

$$p_{1,2} = -\omega_n \cdot (\zeta \pm \sqrt{\zeta^2 - 1}), \tag{3.20}$$

it follows that if $\zeta > 1$, p_1 and p_2 are on the real axis of left half plane, indicating an over-damped system and hence the transient response has no ringing. The unit step response of $\varepsilon_v(t)$ can be derived by using inverse Laplace transform with respect to Eq. (3.16):

$$\varepsilon_v(t) = \mathcal{L}^{-1}\{\frac{\Delta v_{ref}}{s} \cdot E(s)\} = (\,1 - Ae^{-p_1 t} - Be^{-p_2 t}\,) \cdot \Delta v_{ref}\, u(t) \tag{3.21}$$

where the coefficients A and B are calculated by substituting Eqs. (3.18) to (3.20) into Eq. (3.21):

$$\begin{aligned} A =& \frac{p_2}{p_2 - p_1} \cdot [\,1 - p_1(\tau_g + \tau_o) + p_1^2 \tau_g \tau_o\,] \\ =& [\,\frac{1}{2} + \frac{\zeta}{2\sqrt{\zeta^2 - 1}}\,] \cdot [\,1 + 2\zeta(1+L_0)(\zeta - \sqrt{\zeta^2 - 1}) + (1+L_0)(\zeta - \sqrt{\zeta^2 - 1})^2\,] \end{aligned} \tag{3.22}$$

$$\begin{aligned} B =& \frac{p_1}{p_1 - p_2} \cdot [\,1 - p_2(\tau_g + \tau_o) + p_2^2 \tau_g \tau_o\,] \\ =& [\,\frac{1}{2} - \frac{\zeta}{2\sqrt{\zeta^2 - 1}}\,] \cdot [\,1 - 2\zeta(1+L_0)(\zeta + \sqrt{\zeta^2 - 1}) + (1+L_0)(\zeta + \sqrt{\zeta^2 - 1})^2\,] \end{aligned} \tag{3.23}$$

If ζ is smaller than 1, $p_{1,2}$ become a complex conjugate pole pair,

$$p_{1,2} = -\omega_n \cdot (\zeta \pm j\sqrt{1 - \zeta^2}), \tag{3.24}$$

and hence the magnitude of the poles are ω_n, the angle between the pole vector and

the imaginary axis is $\arccos\zeta$. By substituting Eq. (3.24) into Eqs. (3.21) to (3.23) the unit-step response and the coefficient A and B can be rewritten as:

$$\begin{aligned}\varepsilon_v(t) &= [\,1-e^{-\omega_n\zeta t}[(A+B)\cos(\omega_n\sqrt{1-\zeta^2}t)+j(A-B)\sin(\omega_n\sqrt{1-\zeta^2}t)]\,]\cdot\Delta v_{ref}\,u(t)\\ &= [\,1+e^{-\omega_n\zeta t}\cdot L_0\cos(\omega_n\sqrt{1-\zeta^2}t)\\ &\qquad +e^{-\omega_n\zeta t}\cdot\frac{\zeta(L_0+\omega_n+2\omega_nL_0+2)}{\sqrt{1-\zeta^2}}\sin(\omega_n\sqrt{1-\zeta^2}t)\,]\cdot\Delta v_{ref}\,u(t)\,,\end{aligned} \tag{3.25}$$

which shows a decaying sinusoidal waveform. Small ζ values will cause the complex pole-pair moving towards imaginary axis of s-plane hence decreasing the phase margin and increasing overshoot/undershoot in the time domain.

3.2.2 Load transient response of LDOs

Load transient response of the LDOs reflects how fast can the loop take action against the load current variation. In general, for certain load current step ΔI_L with rise (fall) time t_r, the smaller overshoot or undershoot of V_{out} and the shorter the recovery time, the better the load transient performance. However, the step-response in Eqs. (3.21) and (3.25) only valid for small Δv_{ref}. In fact,the load transient response is not only affected by the small-signal loop bandwidth, but mostly related to the slew-rate at the gate of the pass-transistor [49, 73, 74]. Traditionally, a large output capacitor is required to alleviate the undershoot (overshoot) voltage spike problem since the capacitor act as a charge reservoir to offer the instantaneous current during the load transient. However, for fully integrated SoC design it is preferable to put an on-chip capacitor-less LDO adjacent to individual circuit blocks hence the power supply of each circuit block can be optimized independently [75]. As shown in Fig. 3.5, the drain current of the pass transistor I_{ds} is the sum of load current I_L and the biasing current I_b. If the load current changes abruptly like a step function with rise (fall) time Δt, the net charge ΔQ has to be transferred from the output node to load.

$$\Delta Q = \Delta I_L \cdot \Delta t \tag{3.26}$$

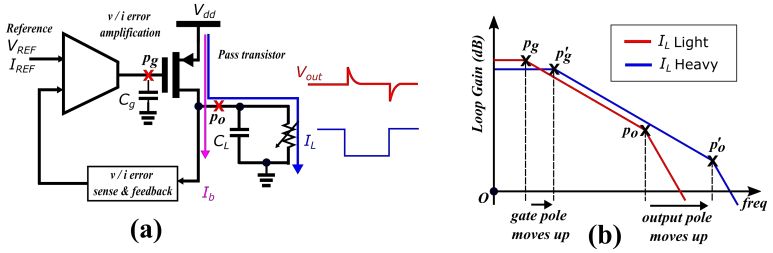


Fig. 3.5. (a) The LDO load transient response (b) The pole locations at different load current

There are two sources of charge available to offer ΔQ, namely the channel charge of M_P, and the charge stored on the capacitance at the output node, including C_L and all the parasitic capacitance lumped together. However, it should be noted that these two sources have different time constant, τ_g and τ_o. For the typical output capacitor-less architecture, the dominant pole is at the gate of M_P rather than at the output. Hence, we have $\tau_o \ll \tau_g$, which means that ΔQ will be transferred from output capacitor first. On the other hand, to change the channel charge of transistor M_P, the surface potential has to be changed by changing the overdrive voltage through the negative feedback loop, but this can only happen after 3 to 5 τ_g for small ΔI_L and even longer for large ΔI_L. Before the channel charge can change, the output voltage drops due to net charge loss on the output node. The output voltage will keep dropping until the feedback increases the overdrive voltage of M_P, more channel charge will be generated to re-charge C_L and the load. The output voltage level will be recovered when the required ΔQ is entirely supplied by M_P, and the recovery time depends on both τ_g and τ_o. From aforementioned qualitative analysis it can be concluded that to achieve undershoot (overshoot)-free response is quite challenging for small load current transition time Δt, if not impossible. More importantly, for large ΔI_L, the relationship between voltage level and charge (discharge) time is no longer exponential but linear, due to the slewing at the gate of M_P and the output node. The slew rate at the gate of M_p, SR_G, and at the LDO output, SR_O, can be written as:

$$SR_G = \frac{dV_{gate}}{dt} = \frac{I_{oa,max}}{C_{gate}}, \tag{3.27}$$

$$SR_O = \frac{dV_{out}}{dt} = \frac{I_L}{C_L}, \tag{3.28}$$

where $I_{oa,max}$ is the maximum current can be sourced (sinked) by the output stage of the error amplifier, C_{gate} is the lumped capacitance at the gate of M_P as shown in Eq. (3.12). To decrease the voltage spikes during the load transient, the *GBW* has to be increased, and SR_G cannot be much less than SR_O. However, since the *GBW* is directly related to the system's natural frequency ω_n, a large *GBW* makes it difficult to achieve a large ζ at the same time, as indicated in Eqs. (3.18) and (3.19). Because C_{gate} is proportional to the aspect ratio of M_P, it is attempting to increase SR_G by decreasing the size of M_P. However, M_P will work at triode region for large I_L if sized too small, and will result in poor supply noise rejection ratio (PSRR). Moreover, the C_{gate} can be much higher if a Miller compensation capacitor is used and lumped into C_{gate}. Therefore, in order to boost SR_G, it generally requires an error amplifier design with high maximum output current sourcing (sinking) ability. The most straightforward way is to use high biasing current at the output stage of the error amplifier. This indeed improves the slew rate but with a price of much higher quiescent power consumption and a lower DC loop gain due to reduced r_{oa}. To overcome the drawbacks of the constant biasing scheme[76], there are many solutions have been proposed including dynamic biasing[77–79], and adaptive biasing[80]. As shown in Fig. 3.6, adaptive or dynamic biasing scheme saves power, because I_{oa} was only boosted either during the load transient event or biased with different I_{oa} for different I_L. Nonetheless, the push-pull output stage in [77, 78] shows class-AB behavior has high supply noise sensitivity, hence the overall power supply noise rejection ratio (PSRR) of the LDO will be degraded. More importantly, these techniques are more effective with respect to reducing the recovery time rather than reducing the absolute value of undershoot (overshoot), this is especially true for the worst-case scenario when the load current changes from 0 to $I_{L,max}$ with small transition time Δt. In general, the limited bandwidth of the error amplifier prevent the effective detection of the output voltage spike within Δt, until the undershoot (overshoot) reaches certain level[49]. For instance, even with the dynamic biasing technique, voltage spikes in the range of tens of mV to several hundreds of mV can be observed for the worst-case load transient response,

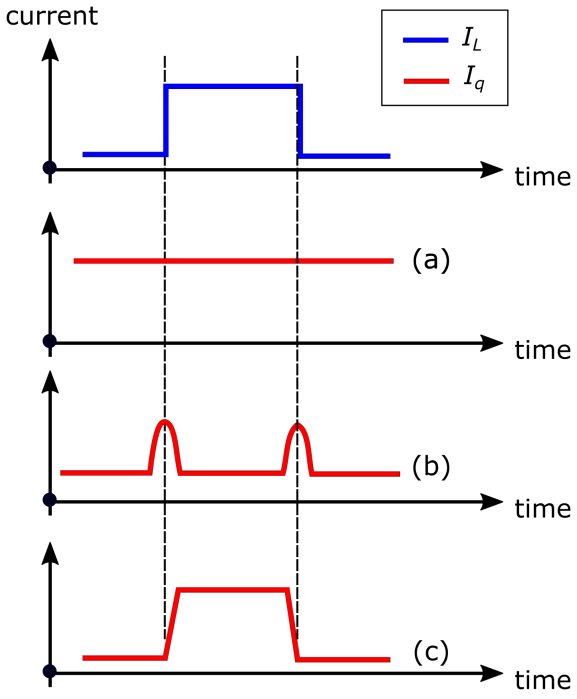


Fig. 3.6. Relationship between the output current and the quiescent current of the LDO (a) constant biasing (b) dynamic biasing (c) current-efficient current buffer

depending on the required ΔQ.

Another issue related to the error amplifier design is the common-mode range at the output and input. For a voltage feedback LDO, it is desirable to have rail-to-rail output range so that a wide range of I_L can be supported. For a supply V_{DD} and p-type power transistor, the output voltage range is roughly from V_{dsat} to $V_{DD} - V_{dsat}$, so that the range of the overdrive voltage of M_P will be from $V_{dsat} - |V_{th}|$ to $V_{DD} - V_{dsat} - |V_{th}|$. Therefore, when I_{ds} is low, the gate voltage of M_P should not be higher than $V_{DD} - V_{dsat}$, and should not be lower than V_{dsat} for high I_{ds}. As V_{DD} is getting closer to V_{th}, it is difficult to drive M_P into strong-inversion region, hence the g_{mp} is lower. In [49], a direct voltage spike detection technique is used to boost the bias current only at the transient instant. Compared with the adaptive and dynamic biasing scheme, the detection circuit is not in the main LDO loop, therefore the undershoot (overshoot) detection is no longer limited

by the *GBW* of the LDO. Specifically, the spike detection and compensation circuit directly senses the output voltage spike, and inject current impulse of which the magnitude is proportional to the high frequency content of the undershoot (overshoot) into the gate of M_P. Therefore, the response time is shorter since the main error correction path in the loop is bypassed. By using this technique, the voltage undershoot (overshoot) magnitude and recovery time can be reduced even for V_{DD} as low as 0.75 V [45].

In order to evaluate the load transient response performance of LDOs, the FOM_1 is defined in [45] :

$$\text{FOM}_1 = \frac{k\Delta V_{OUT} I_q}{\Delta I_L}, \tag{3.29}$$

where I_q is the quiescent current of the LDO itself, k is the Δt ratio normalized to the smallest Δt among all designs used for comparison. Another load transient FOM_2 is proposed in [81]:

$$\text{FOM}_2 = \frac{C_{OUT}\Delta V_{OUT} I_q}{(I_{L,\,max} - I_{L,\,min})^2}, \tag{3.30}$$

where the load capacitance at the output node C_{OUT} has been included.

3.2.3 Supply noise rejection of output capacitor-less LDO

One of important features of LDOs is that the supply noise will be effectively suppressed, because the feedback desensitize the output node from variations on the power supply within the closed-loop bandwidth. The performance of power supply noise rejection can be quantitatively characterized with power supply rejection ratio (PSRR). As shown in Fig. 3.7, LDOs typically have fundamental PSR limitations at high frequencies due to the existence of several paths between the noisy supply and the LDO output[46]:

1.) The supply noise modulate the gate voltage of M_P through C_{gs} and C_{gb}.

2.) The supply noise inject into the error amplifier and modulate the gate voltage of M_P due to the noisy error amplifier output.

3.) The supply noise directly transfer to the output node due to the finite output impedance of M_P.

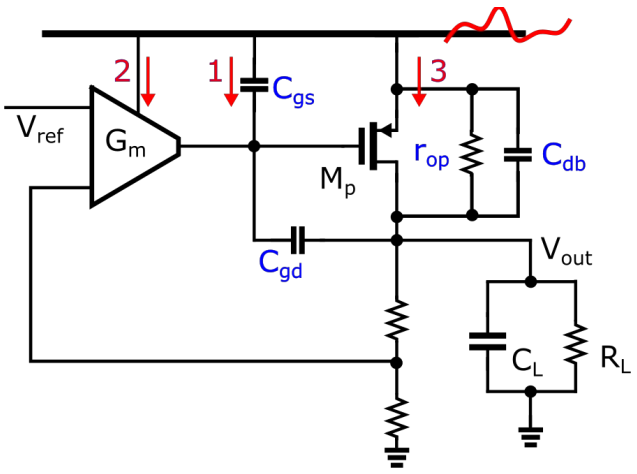


Fig. 3.7. Supply noise transfer path in a conventional LDO.

The supply noise transfer function of the first and second path depending on the size of M_P and the error amplifier topology, whereas the last path sets the ultimate limit for PSR of LDOs, and this can be explained as the following.

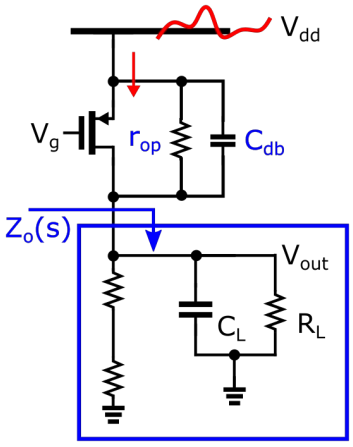


Fig. 3.8. The simplified PSR model of a conventional LDO.

The simplified PSR model for path 3 is shown in Fig. 3.8, the supply noise

transfer function can be written as:

$$H_{vdd}(s) = \frac{v_{out}}{v_{dd}} \approx \frac{Z_{o(s)}}{r_{op} + Z_o(s)} = \frac{1}{1 + r_{op}L(s)/(r_{op}||R_L||\frac{1}{sC_L})}. \tag{3.31}$$

It follows that at low frequencies, $Z_o(s)$ will be suppressed by the loop gain $|L(s)|$. At very high frequencies, $Z_o(s)$ will be attenuated by the output impedance since $sC_L \to \infty$. However, the mid-frequency response is quite different for gate-pole (p_g) dominant and output-pole (p_o) dominant LDO configurations. Specifically, if

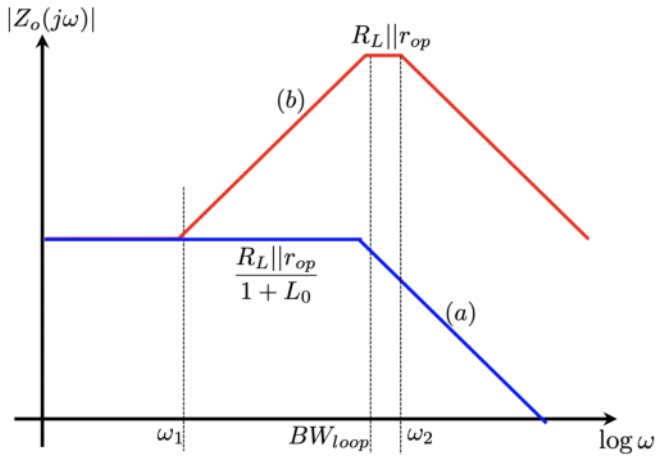


Fig. 3.9. LDO output impedance $Z_o(s)$. (a) output pole dominant, $BW_o = \omega_1$, $BW_a = \omega_2$. (b) internal pole dominant, $BW_a = \omega_1$, $BW_o = \omega_2$.

p_{gate} is the dominant pole, the loop gain $L(s)$ drops as soon as the supply noise frequency surpasses the 3-dB bandwidth of the error amplifier BW_a, hence the output impedance $Z_o(s)$ increases. As shown in Fig. 3.9 (a), the output impedance $Z_o(s)$ peaks between the closed-loop bandwidth BW_{loop} and the output RC network bandwidth BW_o, where its magnitude becomes comparable to r_{op}, hence the attenuation with respect to the supply noise is mainly determined by the divide ratio between r_{op} and $r_{op}+R_L||r_{op}$. After the frequency passes BW_o, the output impedance begins to drop with the roll-off of the output first-order RC network.

On the other hand, the $Z_o(s)$ is different for the output-pole (p_{out}) dominant

LDO topologies, as depicted in Fig. 3.9 (b). When frequency surpasses BW_o, $Z_o(s)$ starts to drop, but the loop gain also drops accordingly due to the reduction on the output impedance of M_p as can be seen from Eq. (3.5). Therefore, $Z_o(s)$ keeps constant initially due to these two effects cancel each other. However, when frequency surpasses BW_{loop} where $|L(s)|=1$ and can no longer drop further to cancel out the impedance drop caused by the sC_L term, $Z_o(s)$ starts to decrease as the first-order roll-off of the output RC network.

Combining Eq. (3.31) and the aforementioned qualitative analysis, the peaking of $Z_o(s)$ is the root cause of the degradation of $H_{vdd}(s)$ for LDOs whose dominant-pole is p_{gate}, which is the case for most of the output capacitor-less LDO topologies. Adding more C_L at the output indeed helps reduce the high-frequency supply noise, but will make the design of a stable LDO more challenging since p_{out} is pushed into p_{gate}.

3.3 The Design of Low-Voltage Low-Power LDO with Current Feedback

In previous sections, the fundamentals of the classical LDO designs with voltage-voltage (shunt-shunt) feedback are elaborated, and the critical performance specifications and design challenges are also analyzed. Clearly, the performance of the LDO based on voltage feedback are limited by the voltage headroom, the *GBW* of the error-voltage amplifier and eventually will be bounded by the total power consumption. Therefore, it may not be the optimum solution for applications require ultra-low power and supply voltage, high power and current efficiencies. For instance, voltage amplifiers are usually used in a voltage feedback LDO to amplify the voltage difference between the reference and the LDO output, then use the amplified version of voltage error to control the gate voltage of M_P. For power-constraint designs, multi-stage designs are common ways to increase the total *GBW* of the error amplifier, where an optimum number of stages and optimum gain per stage exists[82]. However, the number of stages can rarely more than 2 due to complicated compensation scheme for the closed-loop system with many high impedance nodes within the loop. In addition, because the quiescent current need to stay low, the voltage-gain A_v is mainly boosted by the resistance term rather

than the transconductance term to save power, the internal high impedance nodes need longer time to be charged (discharged) hence result in slow response.

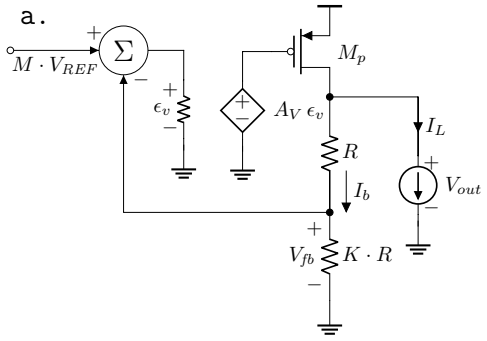


Fig. 3.10. The voltage-voltage feedback LDO

3.3.1 Linear model of current feedback regulators

To achieve better *GBW* for a low power budget and low supply voltage, the error amplifier could be designed in such a way that the output nodes for intermediate stages are low and the only high impedance node is the output of the last stage that directly drives M_P. For such an implementation, the compensation for the internal poles of the error amplifier can be significantly simplified. To make the LDO even faster, the voltage-current (shunt-series) feedback topology can be used, so that the feedback network responses faster because current can change instantaneously at the high impedance RC nodes.

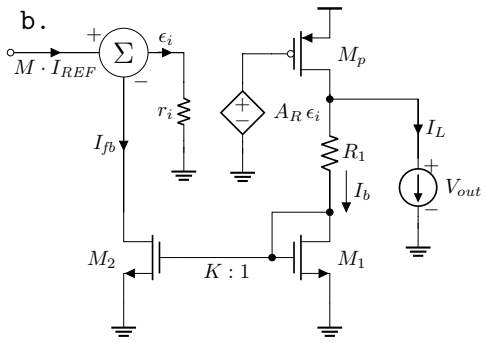


Fig. 3.11. The voltage-current feedback LDO

As shown in Fig. 3.11, a current mirror stage is used to convert the output voltage, V_{out}, to the feedback current $I_{fb} = K \cdot I_b$ (where K is the current scaling ratio of the current mirror). The feedback current $I_{fb} = f_g \cdot V_{out}$ is compared with the scaled reference current I_{ref}. The current mirror offers both DC biasing path and the small-signal feedback path. In this case, the small-signal error current $\varepsilon_i = i_{ref} - f_g \cdot v_{out}$ will be amplified by a trans-impedance amplifier with the gain of A_R, and the output $A_R\varepsilon_i$ will adjust the the overdrive voltage of M_P to force $\varepsilon_i = 0$.

If the loop gain is infinite, the "ideal" closed-loop transfer function can be written as:

$$H_\infty(0) = \frac{V_{out}}{I_{ref}} = \frac{1}{f_g}, \tag{3.32}$$

where f_g is the (conductance) feedback factor at DC. Similar to the conventional LDOs, in practice L_0 is finite and the error current ε_i will be suppressed by $L(s)$:

$$\varepsilon_i(s) = \frac{I_{ref}}{1 + L(s)}. \tag{3.33}$$

Ignoring the second-order effects, the feedback factor can be expressed as:

$$f_g = K \cdot \frac{g_{m1}}{1 + g_{m1}R_1} \approx \frac{K}{R_1}\Big|_{g_{m1}R_1 \gg 1}. \tag{3.34}$$

Therefore, the DC loop gain L_0 can be derived as by substituting the $G_m r_{oa}$ and f_0 terms in Eq. (3.14) with A_R and f_g respectively, and re-written as:

$$|L_0| \approx \begin{cases} |\frac{K}{R_1}A_R| \cdot \sqrt{2K'(\frac{W}{L})_p} \cdot \frac{V_E \,||\, V_{out}}{\sqrt{I_L}}, & \textit{strong-inversion} \\ \\ |\frac{K}{R_1}A_R| \cdot \frac{C_{ox}}{C_{ox} + C_{dep}} \cdot \frac{V_E \,||\, V_{out}}{V_T}, & \textit{weak-inversion} \end{cases} \tag{3.35}$$

where $(W/L)_p$ is the aspect ratio of M_p, A_R is the DC trans-resistance gain of the error amplifier. The loop stability can be analyzed using the same procedure as the voltage feedback LDO, and the results in Eqs. (3.16) to (3.25) can be reused.

Nevertheless, one of the major disadvantages of the topology in Fig. 3.11 is that since the DC biasing and AC feedback path overlapped, the small-signal loop gain

L_0 is coupled with the DC quiescent current. Specifically, the DC output voltage V_{OUT} should satisfy:

$$V_{OUT} = \frac{M}{K} I_{REF} R_1 + V_{GS1}. \tag{3.36}$$

From Eq. (3.35) and Eq. (3.36) it can be observed that a large K value is desired to increase the loop gain, however, a small K is necessary to achieve a relatively high V_{OUT} and lower power consumption. Therefore, high L_0 conflicts with the requirement of high V_{OUT} and low power consumption.

Another challenge is the implementation of the error amplifier with rail to rail output with low quiescent power and high slew rate, DC gain as well as GBW. The previous small-signal analysis assumes all the internal poles of the error amplifier locate at least a decade higher than the closed-loop LDO bandwidth BW_{loop}, which is difficult to realize with low quiescent power.

In addition, the PVT corners need to be carefully considered for low-power design, due to the fact that in weak inversion the transistors' drain current varies exponentially rather than quadratically with respect to the overdrive voltage. One of the solutions is to use "ratio based" or "self-biased" [83] design techniques as much as possible, so that the PVT variations will be partially, if not completely, cancelled out.

3.3.2 Low power implementation of the error amplifier

Two commonly used error amplifier topologies with rail to rail output are the two-stage differential pair (DP) OTA and the current mirror (CM) amplifier, as shown in Fig. 3.12. Previous research show that for a given power budget, no matter how large the current mirror factor K is, the single stage CM amplifier is lagging behind the DP amplifier for most of the performance [84]. Nonetheless, the CM amplifier and its variations are easier to be compensated and can be more efficient in a multi-stage cascaded configuration compared with the DP counterpart.

In [85], a CM amplifier with shunt cur- rent sources was proposed as shown in Fig. 3.13 (a), where the diode-connected transistors $M_{5a,6a}$ are shunt by a pair of fixed current source $M_{3a,4a}$. The current at the output stage $M_{8a,10a}$ are hence reduced accordingly without affecting the biasing current of the input stage $M_{1a,2a}$, therefore, both the G_m of the input stage and r_{out} are enhanced. The drawback of

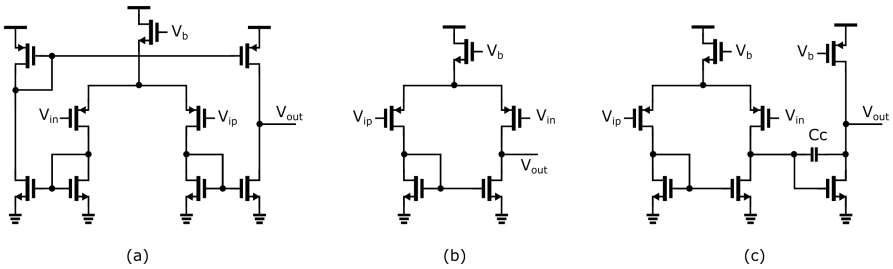


Fig. 3.12. (a). conventional current-mirror amplifier. (b). differential pair amplifier. (c). simple Miller compensation amplifier.

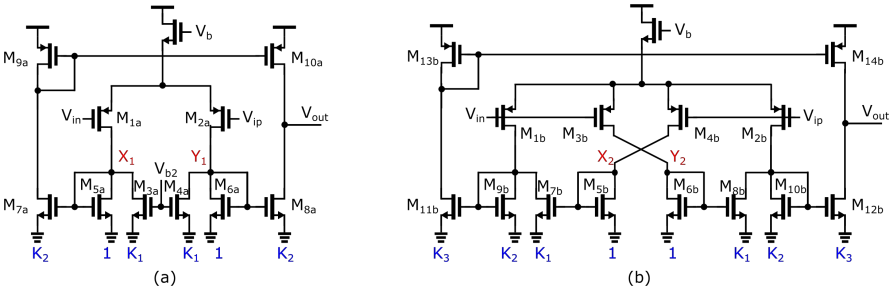


Fig. 3.13. Single-stage amplifiers developed from the current-mirror amplifier: (a) with shunt current sources; (b) with current reuse.

this topology is that the slightly reduced PM due to the parasitics introduced by $M_{3a,4a}$. The key specifications are derived as:

$$G_m = \frac{K_2(K_1+1)}{K_2+K_1+1} \cdot g_{m1}, \tag{3.37}$$

$$r_{out} = \frac{K_2+K_1+1}{K_2} \cdot (r_{o10}||r_{o8}), \tag{3.38}$$

$$SR = \frac{K_2(0.5K_1+1)}{K_2+K_1+1} \cdot \frac{2I_b}{C_L}, \tag{3.39}$$

where G_m is the total stage transconductance, r_{out} is the output resistance, SR is the slew-rate.

The topology in Fig. 3.13 (a) can be further improved by recycling the current of $M_{3a,4a}$, adding another differential pair $M_{3b,4b}$ and cross-coupling to $M_{5b,6b}$, as shown in Fig. 3.13 (b) [86]. Compared with the topology in Fig. 3.13 (a), the G_m will be increased if the current mirror factor K_1 to K_3 are sized properly. Besides, transistors $M_{7a,7b}$ do not need extra bias circuitry, hence the quiescent power is further reduced. Also, the *SR* of this topology surpasses design in Fig. 3.13 (a). The reason is that during large-signal operation, transistor M_{7b} or M_{8b} will be disabled since the node voltage X_2 or Y_2 will be pulled down to ground so that more current will be pushed into the output stage $M_{11b,12b}$. The key parameters are calculated as:

$$G_m = \frac{K_3}{K_2} \cdot \frac{K_2 + 2K_1}{K_3 + K_2 + K_1 + 1} \cdot g_{m1}, \tag{3.40}$$

$$r_{out} = \frac{K_3 + K_2 + K_1 + 1}{K_3} \cdot (r_{o12b} || r_{o14b}), \tag{3.41}$$

$$SR = \frac{K_3}{K_2} \cdot \frac{K_2 + K_1}{K_3 + K_2 + K_1 + 1} \cdot \frac{2I_b}{C_L}. \tag{3.42}$$

It should be noted that the design in Fig. 3.13 (b) has worse PM than the design in [85]. Although introducing two extra current mirrors offers more design freedom to leverage the DC gain, **GBW!** (**GBW!**) and **SR!** (**SR!**), the pole associated with node X_2 (Y_2) along with the left-half-plane (LHP) zero that created by the feedforward path from $M_{1b,2b}$ forms a pole-zero doublet, therefore the stability of the amplifier is degraded [84].

The core idea behind the aforementioned design has been formulated in [84] and [87] as nested current mirror (NCM) technique. As shown in the half circuits in Fig. 3.14, the NCM technique splits the main input device into multiple sub-transistors, with their input cross-coupled to other sub-transistors in the other half of the circuits alternately. All drain-source current of M_1 to M_N are recycled by the current mirror load and combined in sequence. If the current mirror factor K_1 to K_N are sized properly, the effective stage G_m, the output impedance r_{out} will increase concurrently. The DC gain and *GBW* can be increased by adding more CM stages and (or) using large CM ratios, however the number of CM stages and ratios are limited by the PM and transistor mismatches.

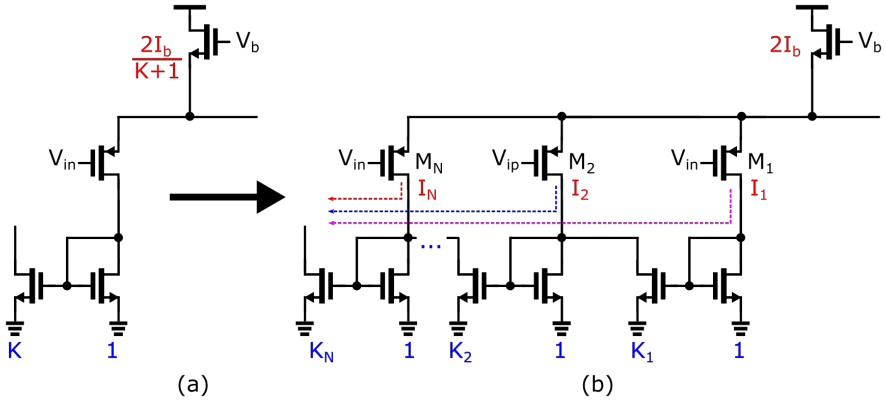


Fig. 3.14. (a) simple Current-Mirror (CM) topology. (b) Nested-Current-Mirror (NCM) topology.

Because of aforementioned features of CM (NCM) amplifiers, they are suitable to be used as the error amplifier in a low-power LDO design. Nonetheless, the designs in [84][85][86] all need the tail current source, so that the minimum required supply voltage has to be $2V_{dsat} + V_{gs}$. In this work, the minimum supply voltage is further reduced by getting rid of the tail current source of the error amplifier. In contrast to conventional pseudo-differential pair amplifiers, by virtue of the proposed current-feedback LDO topology, the pseudo-differential input pair of the error-amplifier is not sensitive to PVT variations.

3.3.3 A low-power LDO implementation using self-biased and current feedback techniques

The idea of using current feedback in a LDO design is illustrated in Fig. 3.11, where a diode-connected transistor is used to sensing the output voltage noise and convert it to error current signal, and can be considered as a NMOS version of "self-biased symmetric" load in [83]. The I-V characteristics of the "self-biased symmetric" load is depicted in Fig. 3.15, from which it can be seen that the equivalent resistance is quite non-linear. Nevertheless, this non-linearity will not affect the output voltage accuracy of the proposed LDO, if the gate biasing voltage will be generated form a replica of the "symmetric" load .

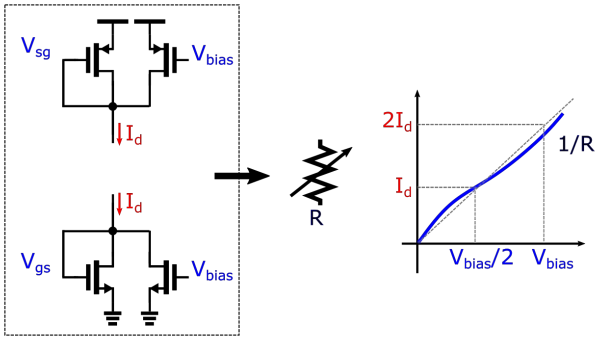


Fig. 3.15. The "self-biased symmetric load".

In this work, a novel LDO topology for ultra-low power biomedical application has been proposed. To make the design suitable for low-voltage operation and insensitive to PVT variations, techniques such as "self-biasing", "replica-biasing" and current-feedback are used. As a result, the design shows both high current and power efficiency as well as good load-transient response.

As shown in Fig. 3.16, a constant-g_m stage offers the biasing voltage of the "symmetric load". Because the feedback loop forces the current at M_{7a} and M_{7b} to be equal, the V_{gs} of M_1 tracks that of M_{3b}. The drain voltage and gate voltage of M_{3d} are set by the gate voltage of M_1 and M_{3b}, respectively. In other words, transistor M_{3d} is "replica-biased" as if it is in a "diode-connection" as M_1 does, due to the tracking of V_{gs3b} and V_{gs1}. As a result, the equivalent resistance that is in series with R_1 is roughly $1/(g_{m1}+g_{m3d})$. The output resistance of the LDO can be re-written as:

$$r_{out} = r_{op} \,\|\, (R_1 + \frac{1}{g_{m1}+g_{m3d}}) \,\|\, \frac{V_{OUT}}{I_L}. \tag{3.43}$$

Additionally, by adding transistor M_{3d}, the conflict between low quiescent power, high output voltage and high loop gain has been resolved. This can be explained as the following. Compared with Fig. 3.11, the proposed LDO topology as shown in Fig. 3.16 decouples $L(s)$ and V_{OUT} by subtracting a portion of DC current from the main feedback path, hence reduces the power consumption and increases $L(s)$ for a given V_{OUT}. Specifically, the current subtraction is implemented

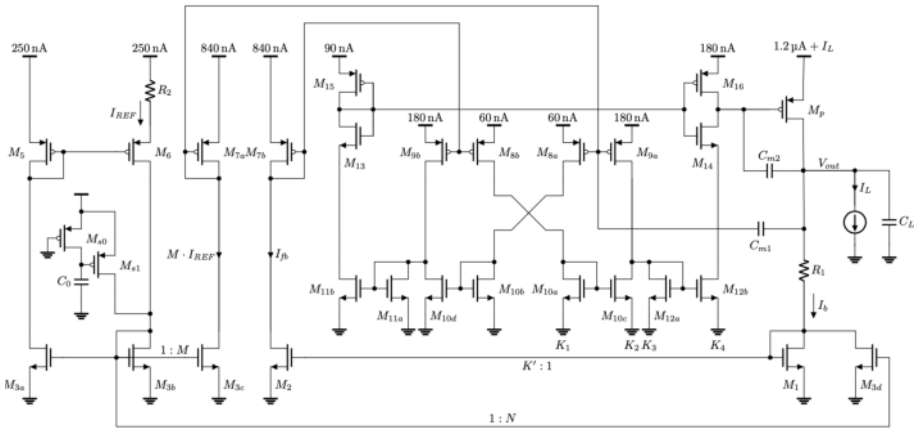


Fig. 3.16. The schematic of the proposed LDO.

by introducing another current mirror branch M_{3d} at the drain node of M_1. With sufficiently high loop gain and assuming that the new current mirror ratio between M_1 and M_2 in Fig. 3.16 is K', the feedback loop forces $M \cdot I_{REF} \approx I_{fb}$. Note that for the low supply voltage design in this work, the current mirror transistors operates in the weak-inversion, the output voltage can be written as:

$$\begin{aligned} V_{OUT} &= (\frac{M}{K'} + N) I_{REF} R_1 + V_{GS1} \\ &= nV_T \cdot [\alpha + \ln(\frac{I_{REF}}{I_{o1}})] + V_{th}. \end{aligned} \tag{3.44}$$

The parameter α can be expressed as:

$$\alpha = (\frac{M}{K'} + N) \frac{R_1}{R_2} \ln(\frac{S_6}{S_5}) + \ln(\frac{M}{K'}), \tag{3.45}$$

where

$$I_{o1} = \mu_n S_1 V_T^2 \sqrt{\frac{q \varepsilon_{si} N_{dep}}{4 \phi_F}} \tag{3.46}$$

is the transistor saturation current, n is the sub-threshold swing parameter, $S_1 = (W/L)_1$ is the aspect ratio of M_1, μ_n the mobility of electrons, ε_{si} is the permittivity of silicon, N_{dep} is the channel doping concentration at depletion edge, ϕ_F is the

Fermi potential in the bulk, $V_T = k_B T/q$ is the thermal voltage defined by Boltzmann constant k_B, absolute temperature T, and the electron charge q. For the same V_{OUT} in Eq. (3.36) and Eq. (3.44), it can be derived that

$$\frac{1}{K} = \frac{1}{K'} + \frac{N}{M} \implies K' > K, \tag{3.47}$$

which indicates that a higher $L(s)$ can be achieved without increasing the total quiescent power.

Another advantage of the proposed LDO topology is that there is no tail current source required for the error-amplifier. The nested current mirror (NCM) technique presented in [87] is used in the forward path trans-impedance error amplifier design to achieve low-power operation. The small-signal feedback current, $i_{fb} = K' \cdot i_{d1} \approx K' \cdot i_b$, is mirrored into a two-stage pseudo-differential NCM amplifier (M_7 to M_{12}) and is amplified to error voltage at the gate of M_p. The cascode transistor M_{14} is used to increase the output impedance r_{oa}. The low-frequency trans-impedance gain and r_{oa} can be expressed as:

$$A_R = \frac{1}{g_{m7}} \cdot G_{ma} \cdot r_{oa} = \frac{1}{g_{m7}} \cdot \left(\frac{K_4 K_2}{K_3 K_1} g_{m8} + \frac{K_4}{K_3} g_{m9}\right) \cdot r_{oa} \tag{3.48}$$

$$r_{oa} = r_{o16} \,\|\, [r_{o14} + (1 + g_m r_{o14}) \cdot r_{o12b}], \tag{3.49}$$

where G_{ma} is the effective stage transconductance of the NCM amplifier, K_1 to K_4 are current mirror ratios as labeled in Fig. 3.16.

To stabilize the loop, the nested Miller compensation technique [88] is adopted to split the dominant pole and the most significant parasitic poles. As shown in the small-signal model of Fig. 3.16, the capacitor C_{m2} splits the pole at the gate of M_p, p_2, and the pole at the output p_3, and the dominant pole p_1 is moved to the gate of M_7 due to C_{m1}. Therefore, the $L(s)$ of the proposed LDO can be derived by Eqs. (3.35), (3.43), (3.48) and (3.49), replacing the term K with K':

$$L(s) = g_{mp} r_{out} A_R \frac{K'}{R_1} \cdot \frac{(1 + s/z_1)(1 - s/z_2)}{(1 + s/p_1)(1 + s/p_2)(1 + s/p_3)} \tag{3.50}$$

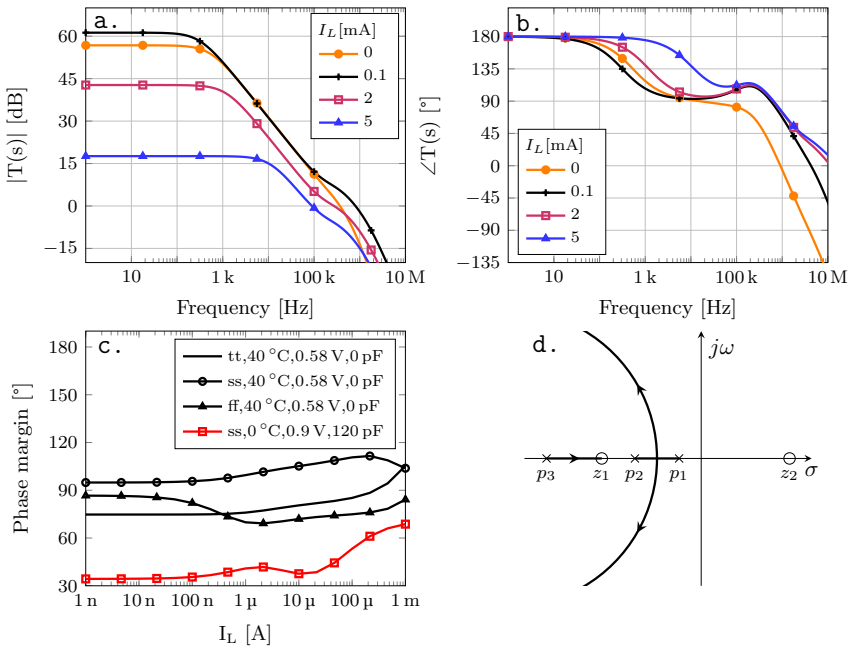


Fig. 3.17. LDO loop transmission $L(s)$. (a) Loop transmission magnitude. (b) Loop transmission phase. (c) Typical and worst-case phase margin. (d) Root locus after compensation (not in scale).

and the dominant pole can be approximately written as:

$$p_1 \approx -\frac{g_{m7}}{(1+G_{ma}r_{oa}g_{mp}r_{out})\cdot C_{m1}} \approx -\frac{1}{g_{mp}r_{out}A_R\cdot C_{m1}} \tag{3.51}$$

and the first two parasitic poles and zeros are:

$$p_2 \approx -\frac{G_{ma}}{C_{m2}}, \qquad p_3 \approx -\frac{1}{r_{out}\cdot C_L}, \tag{3.52}$$

$$z_1 \approx -\frac{g_{mp}}{C_{m2}}, \qquad z_2 \approx +\frac{G_{ma}}{C_{m1}}. \tag{3.53}$$

It should be noted that z_2 is a RHP zero, however, it can be placed at a higher frequency than the unity-gain frequency (UGF) of the loop by letting $C_{m2} \gg C_{m1}$. As shown in the root locus diagram in Fig. 3.17(d), the LHP zero z_1 pulls away the complex pole pair of p_1 and p_2 from the imaginary axis of the s-plane and hence

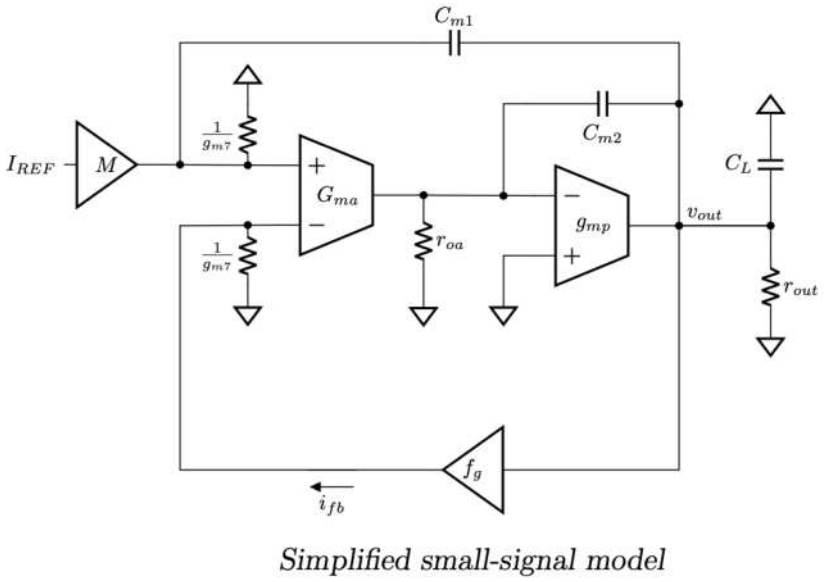


Fig. 3.18. LDO linear model.

improves the phase margin. In addition, p_3 should be located at a much higher frequency than p_1 to further improve the stability. From Eqs. (3.51) and (3.52), $|p_3/p_1| \approx g_{mp}A_R C_{m1}/C_L$, which gives an upper bound for C_L. More accurate loop analysis can be done by a circuit simulator and the simulated loop transmission is shown in Fig. 3.17. It can be seen that L_0 between 40 to 60 dB is achieved as long as the maximum output current $I_{L,\,max}$ is less than 2 mA. Drawing more current than $I_{L,\,max}$ will reduce r_{out} as well as r_{oa} and hence lowers the DC loop gain.

As shown in Fig. 3.16, although the quiescent current at the output stage of the NCM error amplifier is only 180 nA, the proposed LDO design still have good load-transient performance. The SR at the gate of M_p will be dynamically enhanced by virtue of an "embedded" fast loop and the pseudo-differential configuration, as illustrated in Fig. 3.19. The compensation capacitor used in this work is dually used as a part of a faster loop. More specifically, C_{m1} along with $R_1 + 1/(g_{m1} + g_{m3d})$ act as a high-pass filter or a differentiator that connects the output node directly to

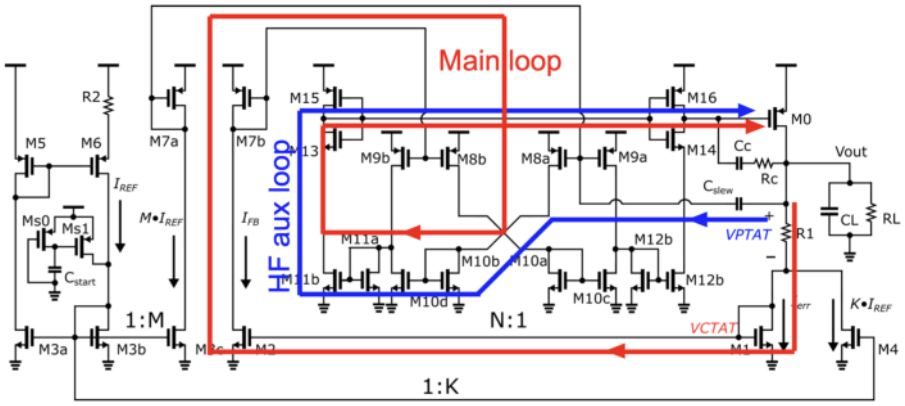


Fig. 3.19

the input of NCM error amplifier. When V_{OUT} undershoots due to abrupt rising edge of I_L, the derivative of the voltage spike pulls down the gate voltage of M_{9a}, and boosts the transient current of M_{12b}, therefore offers a faster discharge path for the gate charge of M_p through $M_{14} - M_{12b}$.

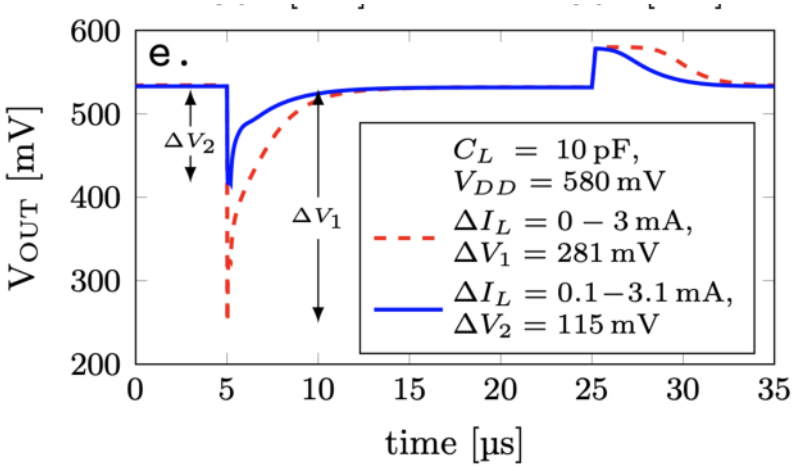


Fig. 3.20. Load transient response for zero minimum load current and 0.1 mA minimum load current. t_r = 200 ns.

To reduce the effects of device mismatch due to local (within-die) variations,

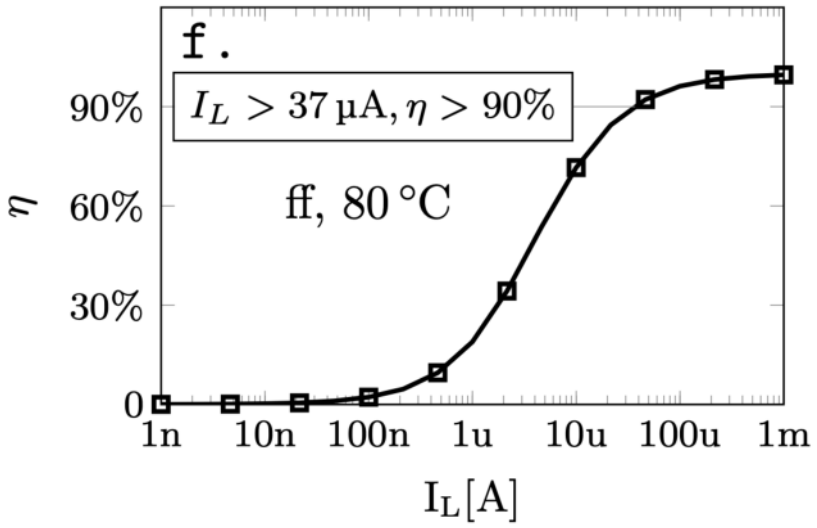


Fig. 3.21. Worst case current efficiency η.

large size transistors are used since device mismatches are inversely proportional to the area of the transistors. Layout techniques such as interdigitate and common-centroid structures are used to minimize the layout-dependent mismatches.

The V_{OUT} variations under different PVT corners are simulated through 1500-point Monte-Carlo simulation (Fig. 3.22). The aspect ratios of the transistors are optimized to make the total standard deviation σ less dependent to transistor mismatches. As can be seen from Table 3.1, global (lot-to-lot, wafer-to-wafer, and die-to-die) variations is the main contributor to the overall variation of σ of V_{OUT}.

Table 3.1: CONTRIBUTIONS OF LOCAL VARIATION OF DEVICES AS WELL AS CONTRIBUTION OF THE GLOBAL VARIATIONS TO σ OF V_{OUT} .

M_{9a}	M_{9b}	M_{8b}	M_{3b}	M_{8a}	other devices
3%	3%	3%	3%	2%	5%
M_{7b}	M_{7a}	M_{10a}	M_5	M_{3a}	Global Variations
2%	1%	1%	1%	1%	75%

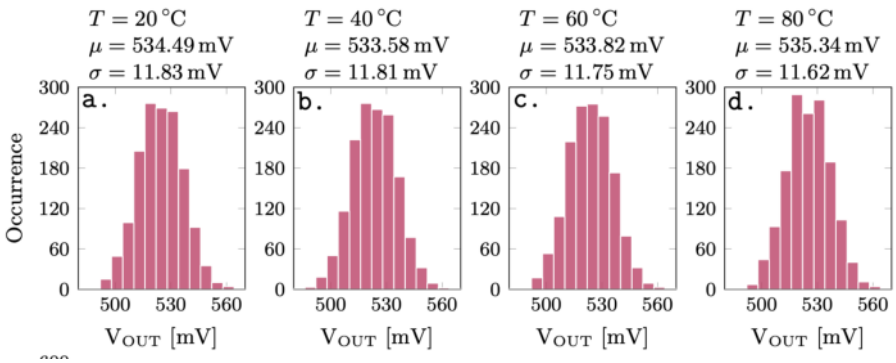


Fig. 3.22. V_{out} distribution of 1500 points Monte-Carlo simulation.

3.3.4 Experimental Results

The presented LDO is designed with standard V_{th} transistors in a 0.13 µm CMOS process and the chip micrograph is shown in Fig. 3.23(a). Two identical LDO cells are designed and laid out on the same die with one of them having a load-transient testbench that is similar to the on-chip loading in [50]. The line (load) regulation and load transient response of the 16 LDOs on 8 dies are measured by a dual channel Keithley source measure unit (SMU) 2604B, the total DC current that is drawn from V_{DD} and the load current I_L are monitored during the measurement. As shown in Fig. 3.23(e), the presented LDO is able to work for a V_{DD} from 0.56 V to 0.9 V, and generates a nominal mean $V_{OUT,\mu}$ of 0.53 V with standard deviation σ of 4.5 mV. The load transient response under full current swing condition (0 to $I_{L,\,max}$) and typical current swing condition ($I_{L,\,typical}$ to $I_{L,\,max}$) are shown in Fig. 3.23(f)-(i), for 0.6 and 0.9 V supply voltages, respectively. The LDO performance is summarized in Table 3.2.

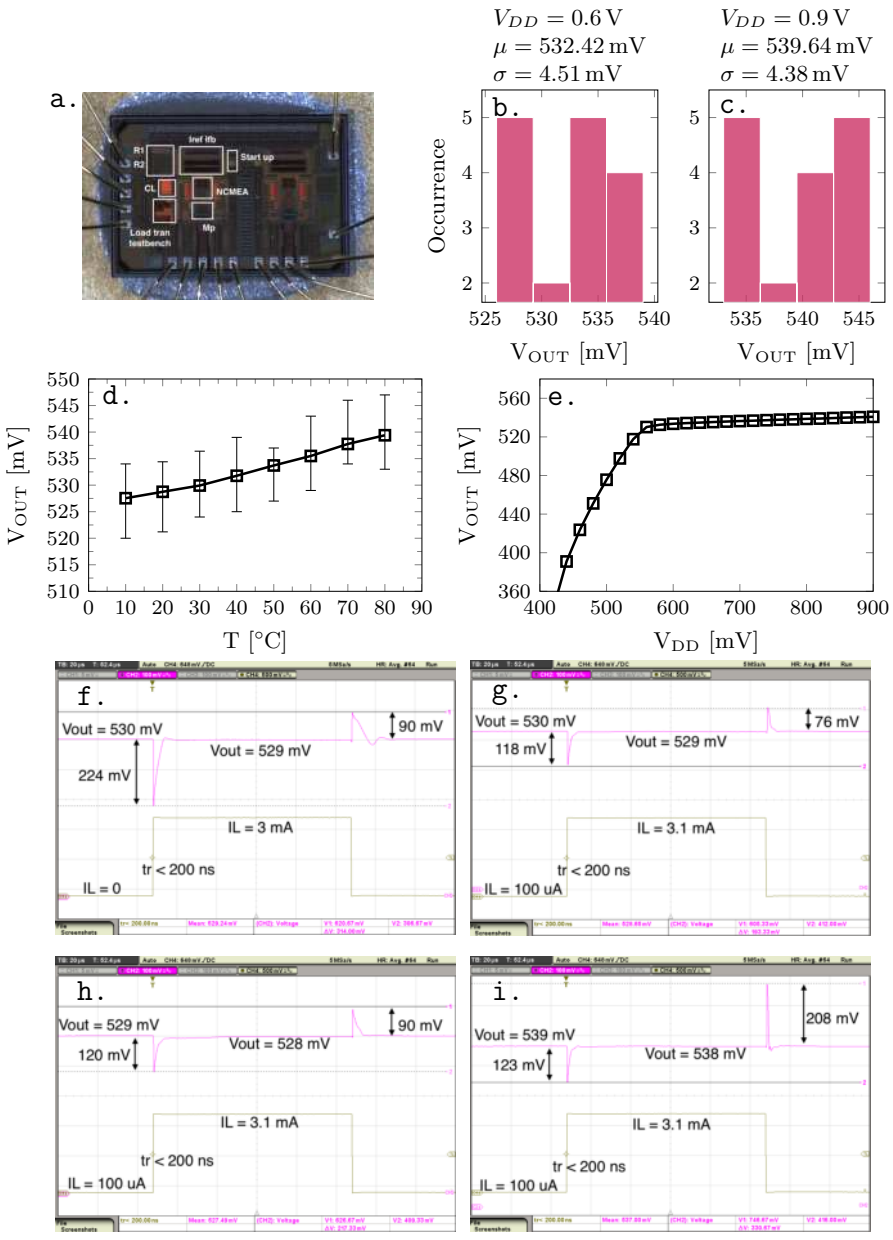


Fig. 3.23. Measured LDO performance.(a) Micrograph. (b-c) V_{OUT} of 16 samples. (d) Temperature dependency of V_{OUT}. (e) Line regulation. (f) $\Delta I_L = 3\,\mathrm{mA} - 0\,\mathrm{mA}$, $C_L = 10\,\mathrm{pF}$, $V_{DD} = 0.6\,\mathrm{V}$, $V_{OUT} = 0.53\,\mathrm{V}$. (g) $\Delta I_L = 3.1\,\mathrm{mA} - 0.1\,\mathrm{mA}$, $C_L = 70\,\mathrm{pF}$, $V_{DD} = 0.6\,\mathrm{V}$, $V_{OUT} = 0.53\,\mathrm{V}$. (h) $\Delta I_L = 3.1\,\mathrm{mA} - 0.1\,\mathrm{mA}$, $C_L = 125\,\mathrm{pF}$, $V_{DD} = 0.58\,\mathrm{V}$, $V_{OUT} = 0.53\,\mathrm{V}$. (i) $\Delta I_L = 3.1\,\mathrm{mA} - 0.1\,\mathrm{mA}$, $C_L = 125\,\mathrm{pF}$, $V_{DD} = 0.9\,\mathrm{V}$, $V_{OUT} = 0.54\,\mathrm{V}$.

Table 3.2: COMPARISON WITH STATE-OF-THE-ARTS.

Design	[71]	[81]	[89]	[90]	This work
Technology	65 nm	65 nm	0.13 µm	65 nm	0.13 µm
Control method	Digital wo Ref	Digital wo Ref	Digital wo Ref	Analog wo Ref	Analog w Ref
V_{DD} [V]	0.5-1	0.5-1	0.5-1.2	0.6	0.58-0.9
V_{OUT} [V]	0.45-0.95	0.3-0.45	0.45-1.14	0.3-0.55	0.53
$V_{dropout\,min}$ [mV]	50	50	50	50	50
I_Q [µA]	3.2	14	24	32	4
$I_{L,\,min}$ [µA]	200	0.1	100	0	0
$I_{L,\,max}$ [mA]	13	2	4.6	50	3
Line Reg. [mV / V]	30	2.3	NA	NA	29
Load Reg. [mV / mA]	2.3	<5.6	<10	NA	1.2
C_L [pF]	100	400-1000	1000	0-40	0-120
Load Tran. Δt [ns]	1	<1	NA	150	<200
Load Tran. ΔI_L [mA]	12-2=10	1.1-0.04=1.06	0.7	10-0=10	3.1-0.1=3
Undershoot ΔV_{OUT} [mV]	105	40	40	133.9	120
Overshoot ΔV_{OUT} [mV]	65	40	NA	115.3	90
Peak current efficiency η [%]	>95.5	99.8	98.3	99.9 *	99.8
Load range with $\eta > 90\%$	0-12 mA	33.6 µA-2 mA	2.9-4.6 mA	0.4-50 mA *	0-3 mA
FOM_1 †[V]	0.000036	0.00028	NA	0.064	0.032 **
FOM_2 ‡[ps]	0.23	56	8571	1.7	0.99 **

† $\text{FOM}_1 = k\Delta V_{OUT} I_Q / \Delta I_L$ as defined in [45]. k is the Δt ratio normalized to the smallest Δt among all designs used for comparison.

‡ $\text{FOM}_2 = C_{OUT}\Delta V_{OUT} I_Q / (I_{L,\,max} - I_{L,\,min})^2$. As suggested in [81], for a valid measurement of FOM_2, Δt should be less than $T_R/10$, where $T_R = C_{OUT}\Delta V_{OUT}/\Delta I_L$ is the response time.

* These numbers are observed from the figures in [90].

** The C_L of 120 pF off-chip and 10 pF on-chip capacitance and corresponding measurement data are used for FOM_1 and FOM_2 calculation, respectively. Note that the LDOs in [71], [90], and the proposed design do not meet $\Delta t < T_R/10$, however, the FOMs are still informative as comparison metrics[71][90].

Chapter 4

The Design of Low-Power Voltage-Controlled Oscillator

The voltage-controlled oscillator (VCO) is one of the major power consumers in modern CMOS IC designs, the trade-offs among power consumption, output phase noise, output voltage swing, and tuning range needs to be thoroughly considered to achieve optimal performance. For the low-power and low-voltage constraints in this work, the Class-D topology[91] is used to achieve low phase noise, high voltage swing and high power efficiency at the same time, but at a price of degraded supply pushing. Nonetheless, the supply pushing issue will be compensated if a regulated supply is used for the Class-D VCO (e.g., in a phase locked loop), so that the overall system power efficiency will be improved without sacrificing the performance.

4.1 Review of low-power voltage controlled oscillators

In [92], a dual conduction class-C CMOS VCO for ultra-low supply voltages is proposed. Two cross-coupled NMOS pairs with different bias points are employed, which realize impulse like current waveform to improve the phase noise in the low supply conditions. The proposed VCO was implemented in a 0.18 μm CMOS technology, which oscillates at a carrier frequency of 4.5 GHz with a 0.2 V supply voltage. The measured phase noise is -104 dBc/Hz@1 MHz offset with a power

consumption of 114 μW, and FoM is -187 dBc/Hz. In [93], a transformer coupled VCO is used in a 2.4 GHz receiver. The transformer feedback VCO requires a 300-mV supply voltage and achieves 3-dB better phase noise compared with standard cross-coupled VCO. In [94], a enhanced swing class-D VCO operates from a supply voltage as low as 300 mV is presented. The proposed VCO have been implemented in a 65 nm RF CMOS process with a 5 GHz VCO oscillation frequency. At a 350 mV supply, the measured phase noise performance for the quadrature VCO with a 5% tuning range is -137.1 dBc/Hz at 3 MHz offset with a power dissipation of 2.1 mW from a 0.35 V supply. The highest resulting FoM is 198.3 dBc/Hz. In [95], a class-D VCO in parallel with a class-C starter is implemented in a 28 nm CMOS process. The VCO oscillates at 2.3 GHz and shows smaller than -113 dBc/Hz phase noise at 2.5 MHz offset. The active power is only 153 μW at 0.18 V supply voltage.

4.2 The linear time-invariant model of oscillator phase noise

The modeling of phase noise and jitter of oscillators have been studied extensively, for instance, the Leeson-Cutler model [96]:

$$S_\phi(\Delta\omega) = S_{\Delta\theta}[1 + (\frac{\omega_0}{2Q\Delta\omega})^2] \tag{4.1}$$

has been widely used for phase noise evaluation. The derivation of Eq. (4.1) is based on the linear time-invariant (LTI) feedback model, where Q is the unloaded open loop quality factor, $S_\phi(\Delta\omega)$ is the power spectral density (PSD) of the phase in frequency domain. Specifically, for a *LC* oscillator with tank resonant frequency $\omega_0 = 1/\sqrt{L_pC_p}$,

$$Q = \frac{R_p}{\omega_0 L_p} = R_p\omega_0 C_p, \tag{4.2}$$

where the tank loss is modeled with R_p. The impedance of the tank at $\omega_0 + \Delta\omega$ can be derived as:

$$\begin{aligned} Z(\omega_0 + \Delta\omega) &= j(\omega_0 + \Delta\omega)L_p || \frac{1}{j(\omega_0 + \Delta\omega)C_p} \\ &= \frac{j(\omega_0 + \Delta\omega)L_p}{1 - \omega_0^2 L_p C_p - 2\omega_0 \Delta\omega L_p C_p - \Delta\omega^2 L_p C_p}. \end{aligned} \tag{4.3}$$

If assuming the frequency offset $\Delta\omega$ is much less than ω_0, and substituting Eq. (4.2) into Eq. (4.3), the tank impedance can be approximately written as:

$$Z(\omega_0 + \Delta\omega) \approx -j \frac{R_p}{2Q} \cdot \frac{\omega_0}{\Delta\omega}. \tag{4.4}$$

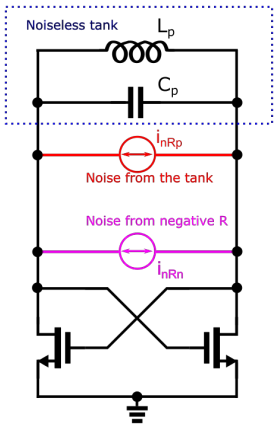


Fig. 4.1. Noise model of LC oscillator, assuming tank resistance R_p is cancelled by the G_m of the active device.

Therefore, if the noise from the tank itself due to R_p and from the negative resistance due to the active circuits are uncorrelated, the output noise voltage mean-

square spectral density can be evaluated by:

$$\begin{aligned}\frac{\overline{v_n^2}}{\Delta f} &= \left(\frac{\overline{i_{nR_p}^2}}{\Delta f} + \frac{\overline{i_{nR_n}^2}}{\Delta f}\right) \cdot |Z(\omega_0 + \Delta\omega)|^2 \\ &= \frac{\overline{i_{nR_p}^2}}{\Delta f}\left(1 + \frac{\overline{i_{nR_n}^2}}{\Delta f} \Big/ \frac{\overline{i_{nR_p}^2}}{\Delta f}\right) \cdot |Z(\omega_0 + \Delta\omega)|^2.\end{aligned} \tag{4.5}$$

The negative resistance generated by the active circuits, $-R_n = -1/G_m$, should precisely cancel the tank loss R_p to maintain stable oscillation, however, the noise of R_n and R_p are not necessarily the same. In practice, the ratio between these two noise spectral density,

$$F(\Delta\omega) = 1 + \frac{\overline{i_{nR_n}^2}}{\Delta f} \Big/ \frac{\overline{i_{nR_p}^2}}{\Delta f} \tag{4.6}$$

is often obtained by measurements as an empirical parameter. The noise current mean-square spectral density of R_p can be expressed as:

$$\frac{\overline{i_{nR_p}^2}}{\Delta f} = \frac{4kT}{R_p}. \tag{4.7}$$

by substituting Eqs. (4.4), (4.6) and (4.7) into Eq. (4.5), the output noise mean-square voltage spectral density can be expressed as:

$$\frac{\overline{v_n^2}}{\Delta f} = 4kTF(\Delta\omega) \cdot R_p \left(\frac{\omega_0}{2Q}\frac{1}{\Delta\omega}\right)^2. \tag{4.8}$$

It should be noted that Eq. (4.8) has both amplitude and phase noise components. According to the equipartition theorem [82], the noise impact will split evenly between amplitude and phase, if the voltage waveform of the oscillator is sinusoidal. This is in general the case for *LC* oscillators. Therefore, the phase noise **PSD!** (**PSD!**) can be written as:

$$S_\phi(\Delta\omega) = \frac{\overline{v_n^2}}{\Delta f}\frac{1}{R_p} = 2kTF(\Delta\omega) \cdot \left(\frac{\omega_0}{2Q}\frac{1}{\Delta\omega}\right)^2. \tag{4.9}$$

It is common to normalize the phase noise PSD with respect to the carrier power

at ω_0 and express the ratio in decibel to characterize the phase noise performance. The signal power of the carrier can be derived as:

$$P_{sig} = \frac{v_{sig,rms}^2}{R_p}, \tag{4.10}$$

hence the phase noise at offset frequency $\Delta\omega$ can be re-written in **dBc/Hz** as:

$$L(\Delta\omega)|_{\mathbf{dB}} = 10\log[\frac{2kTF(\Delta\omega)}{P_{sig}} \cdot (\frac{\omega_0}{2Q}\frac{1}{\Delta\omega})^2]. \tag{4.11}$$

The phase noise expression in Eq. (4.11) has only considered the impact of thermal noise from the tank, however, the uncertainty of the oscillator phase consists of two components: the additive white noise at frequencies around ω_0 and other frequencies mixed into the band of interest by nonlinearities; and noise caused by the parameter variations (such as the flicker noise caused by trapping and de-trapping of charge carriers in traps located in the transistor's gate dielectric). For white additive noise, its PSD will be eventually flatten out with frequency due to the noise floor, rather than keep decreasing quadratically. For the flicker noise, on the other hand, every single trap that is located in the dielectric oxide leads to a Lorentzian noise power spectrum, the Lorentzian spectra add up to give a $1/f$ characteristic if the trap has uniform spatial distribution [97].

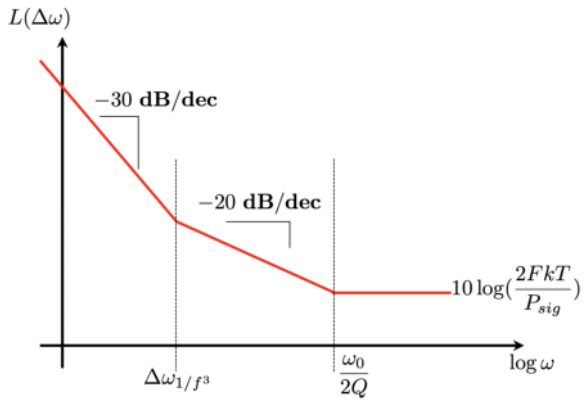


Fig. 4.2. Phase noise predicted by Leeson-Cutler model.

In order to include these two noise components, Leeson [96] modified the

model in Eq. (4.11) with experimental results, added a flat region and $1/f$ region, and assumes $F(\Delta\omega) \approx F$ for all the frequencies hence the model can be written as:

$$L(\Delta\omega)|_{\mathbf{dB}} = 10\log[\frac{2kTF}{P_{sig}} \cdot (1 + (\frac{\omega_0}{2Q}\frac{1}{\Delta\omega})^2) \cdot (1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|})], \tag{4.12}$$

where it shows that the corner frequency between $1/f^2$ region and flat region happens at $\omega_0/2Q$, as shown in Fig. 4.2. It should be noted that although the empirical parameter F is usually called "device excessive noise number", it does not relate to any physical concept. The Leeson-Cutler model also assumes that the boundary between $1/f^3$ and $1/f^2$ noise occurred precisely at the $1/f$ corner of the device. However, this is not always the case. Besides, the frequency at which the noise flattens out is not always equal to half the resonator bandwidth $\omega_0/2Q$ [98].

4.3 The linear time-variant model of oscillator phase noise

Since the oscillators are periodically time-varying systems, the LTI model has limited accuracy if used for modeling oscillators. A more sophisticated and general

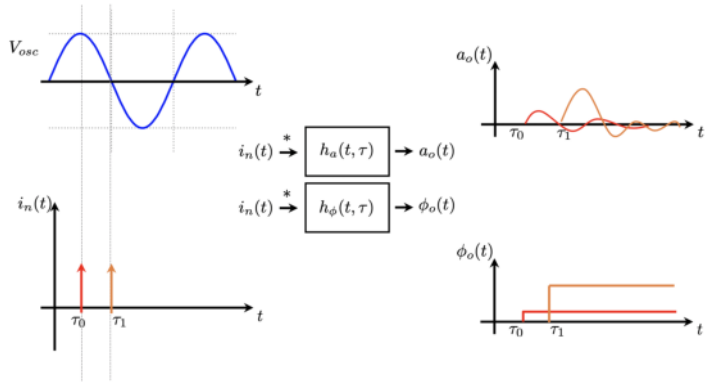


Fig. 4.3. Impulse response of amplitude $a_o(t)$ and phase $\phi_o(t)$.

method of modeling phase noise is proposed in [99], which is based on linear time-variant (LTV) model. In this approach, the impulse response of an oscillator system is evaluated to characterize the output phase deviation for an input current impulse excitation.

As depicted in Fig. 4.3, for an oscillator in steady-state, the impulse responses of output phase $\phi_o(t)$ and amplitude $a_o(t)$ both depend on the time instant τ of the input excitation, $i_n(\tau)$, which demonstrates the time-variant nature of the system. Nevertheless, the system function $h_\phi(t,\tau)$ and $h_a(t,\tau)$ are completely different. On one hand, the limiting mechanism will suppress the amplitude deviation because the system state will eventually approach the closed trajectory in the portrait of oscillator's state-space, regardless of the initial state [100].

On the other hand, $\phi_o(t)$ shows a step change, meaning that the phase deviation will be accumulated or integrated with respect to time indefinitely. In fact, the sensitivity of $\phi_o(t)$ with respect to the time at which $i_n(\tau)$ is injected into the input varies significantly. As illustrated in Fig. 4.4, for a *LC* oscillator, the sensitiv-

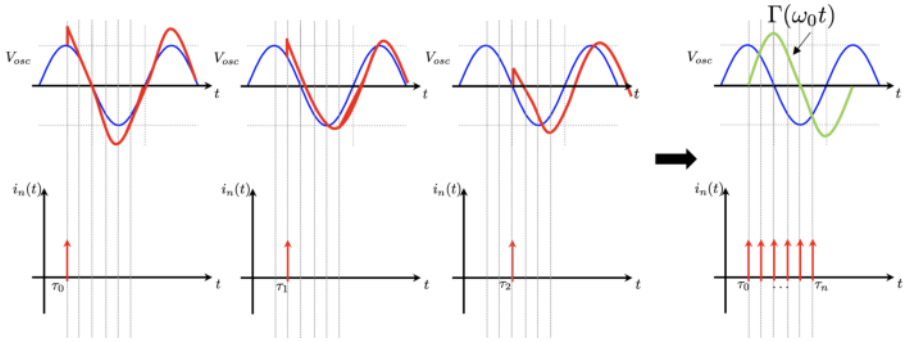


Fig. 4.4. The impulse sensitivity function (ISF).

ity of phase deviation of the output voltage waveform is highest at zero-crossings, or when all energy is stored in the inductor as magnetic energy and zero electric energy left in the capacitor. The sensitivity is lowest when the voltage waveform reaches its peak, or when all energy is stored in the capacitor as electric energy and zero energy left in the inductor. These phenomena make sense because the capacitor is susceptible to abrupt current change while inductor rejects sudden change of current.

To quantitatively analyze relationship between $\phi_o(t)$ and $i_n(\tau)$, the impulse sensitivity function (ISF), $\Gamma(\omega_0\tau)$, is defined in [98, 99]. As shown in Fig. 4.3, the

system function $h_\phi(t,\tau)$ has a step change and can be written as:

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau), \tag{4.13}$$

where $u(t)$ is the unit-step function, $q_{max} = V_{max} C_{total}$ is the maximum charge displacement across the capacitor on the node at which the $i_n(\tau)$ is injected in, V_{max} is the peak value of the voltage signal swing of the oscillator. By normalizing $\Gamma(\omega_0\tau)$ with respect to q_{max}, the ISF's dependency on signal amplitude is eliminated. Therefore, $\Gamma(\omega_0\tau)$ is a dimensionless, amplitude and frequency-independent function with period of 2π that quantifies how much phase deviation $\Delta\phi$ will be caused by applying a unit impulse at different time instant in one period $t = \tau_N$. It can be inferred that ISF is proportional to the derivative of the oscillator waveform, where its magnitude reflects how sensitive the voltage waveform to the injected noise current with respect to the generation of excessive phase.

Having introduced the ISF, the output excess phase $\phi_o(t)$ can be derived by using the superposition integral:

$$\phi_o(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau)\, i_n(\tau)\, d\tau = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_0\tau)\, i_n(\tau)\, d\tau. \tag{4.14}$$

Since $\Gamma(\omega_0\tau)$ is periodic, it can be expressed as *Fourier* series:

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \theta_n), \tag{4.15}$$

where c_n are the real-valued coefficients and θ_n is the phase of the nth harmonic. By substituting Eq. (4.15) into Eq. (4.14), switching the order of integration and summation, and ignoring the parameter θ_n, the excess phase can be re-written as:

$$\phi_o(t) = \frac{1}{q_{max}} \cdot [\frac{c_0}{2} \int_{-\infty}^{t} i_n(\tau)\, d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i_n(\tau) \cos(n\omega_0\tau)\, d\tau]. \tag{4.16}$$

It is more intuitive to draw the diagram of Eq. (4.16) as Fig. 4.5, where it can be seen that the noise at all frequency band will be down converted by the harmonic tones $n\omega_0$, weighted by the corresponding *Fourier* coefficients of $\Gamma(\omega_0\tau)$, and the weighted sum will be integrated and will modulate the output voltage waveform

in a non-linear way, since $V_{osc}(t) = V_{max}\cos[\,\omega_0 t + \phi_o(t)\,]$. For a white input noise

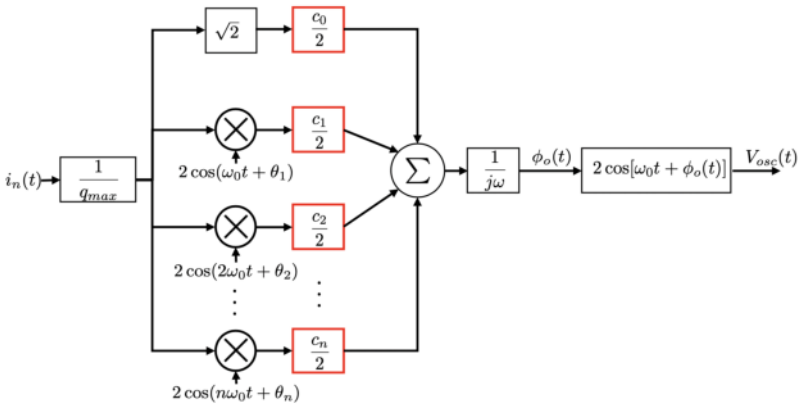


Fig. 4.5. ISF Fourier Series Coefficients.

source $i_n(t)$, the PSD of $\phi_o(t)$ can be calculated as:

$$\begin{aligned} S_\phi(\omega) &= \frac{\overline{i_n^2}}{2\Delta f}\cdot 2(\frac{1}{q_{max}})^2\cdot[(\frac{c_0}{2})^2+(\frac{c_1}{2})^2+\cdots]\cdot|\frac{1}{j\omega}|^2 \\ &= \frac{1}{4\,q_{max}^2\,\omega^2}\cdot\frac{\overline{i_n^2}}{\Delta f}\cdot\sum_{n=0}^{\infty}c_n^2, \end{aligned} \tag{4.17}$$

therefore the total single sideband (SSB) phase noise spectral density below the carrier power per Hertz at frequency offset $\Delta\omega$ can be written as:

$$L(\Delta\omega) = 10\log[\,S_\phi(\Delta\omega)\,] = 10\log[\,\frac{1}{4\,q_{max}^2\,\Delta\omega^2}\cdot\frac{\overline{i_n^2}}{\Delta f}\cdot\sum_{n=0}^{\infty}c_n^2]. \tag{4.18}$$

According to *Parseval*'s theorem:

$$\sum_{n=0}^{\infty}c_n^2 = \frac{1}{\pi}\int_0^{2\pi}|\Gamma(x)|^2\,dx = 2\Gamma_{rms}^2, \tag{4.19}$$

where Γ_{rms} is the root-mean-square value of the ISF. By substituting Eq. (4.19) into Eq. (4.18), it follows that:

$$L(\Delta\omega) = 10\log[\,\frac{\Gamma_{rms}^2}{2\,q_{max}^2}\cdot\frac{\overline{i_n^2}}{\Delta f}\,] - 20\log(\Delta\omega), \tag{4.20}$$

where it predicts that $1/f^2$ region exists in the SSB phase noise power spectrum. In addition, the $1/f$ region as well as the corner frequency can also be analyzed by the ISF. If assuming the $1/f$ noise can be represented by [82, 99]:

$$\overline{i_{n,1/f}^2} = \overline{i_n^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}, \tag{4.21}$$

where $\omega_{1/f}$ is the device $1/f$ corner frequency. Since the $1/f$ noise will only be weighted by c_0 term of the ISF *Fourier* coefficients, the PSD of $\phi_o(t)$ can be derived as:

$$\begin{aligned} S_{\phi,1/f}(\Delta\omega) &= \frac{\overline{i_{n,1/f}^2}}{2\Delta f} \cdot 2(\frac{1}{q_{max}})^2 \cdot (\frac{c_0}{2})^2 \cdot |\frac{1}{j\Delta\omega}|^2 \\ &= \frac{\omega_{1/f}}{4q_{max}^2\Delta\omega^3} \cdot \frac{\overline{i_n^2}}{\Delta f} \cdot c_0^2, \end{aligned} \tag{4.22}$$

and the corresponding $1/f$ phase noise can be written as:

$$L_{1/f}(\Delta\omega) = 10\log[\frac{c_0^2\,\omega_{1/f}}{4\,q_{max}^2} \cdot \frac{\overline{i_n^2}}{\Delta f}] - 30\log(\Delta\omega). \tag{4.23}$$

where it shows that there is a $1/f^3$ region in the phase noise profile. Therefore, the boundary between the $1/f^2$ and $1/f^3$ region, ω_{1/f^3}, can be found at the frequency when $S_\phi(\omega_{1/f^3})$ equals $S_{\phi,1/f}(\omega_{1/f^3})$. Combining Eq. (4.17) and Eq. (4.22), the $1/f^3$ corner frequency can be solved as:

$$\omega_{1/f^3} = \omega_{1/f} \cdot \frac{c_0^2}{2\Gamma_{rms}^2} \approx \omega_{1/f} \cdot (\frac{\Gamma_{dc}}{\Gamma_{rms}})^2, \tag{4.24}$$

where Γ_{dc} is the DC component of $\Gamma(\omega_0\tau)$. An important conclusion based on Eq. (4.24) is that ω_{1/f^3} is not the same as the device flicker noise corner $1/f$, but a scaled version of $\omega_{1/f}$. The scaling factor Γ_{dc}/Γ_{rms} is determined by the waveform of the oscillator, hence by properly engineering the oscillator waveform, e.g., making the voltage waveform symmetric, the term Γ_{dc} or c_0 approaches to zero therefore there will be no up-conversion of flicker noise.

Aforementioned analysis assumes the noise source $i_n(\tau)$ is stationary during

one oscillation cycle. However, $i_n(\tau)$ usually varies periodically, as it depends on the bias conditions of its associated transistors. By introducing the noise modulation function (NMF) $\alpha(x)$, the ISF and LTV model will also accounts for the cyclostationary noise. The cyclostationary noise $i_n(\tau)$ can be written as:

$$i_n(\tau) = i_{n,0}(\tau) \cdot \alpha(\omega_0 \tau), \tag{4.25}$$

where $i_{n,0}$ is the stationary thermal noise source. After introducing the NMF, the effective ISF can be re-written as:

$$\Gamma_{\text{eff}}(\omega_0 \tau) = \Gamma(\omega_0 \tau) \cdot \alpha(\omega_0 \tau). \tag{4.26}$$

The above Eq. (4.26) infers that to minimize $\Gamma_{\text{eff}}(\omega_0 \tau)$, the peak of the NMF should appears at the zero values of $\Gamma(\omega_0 \tau)$, as illustrated in Fig. 4.6. A good example

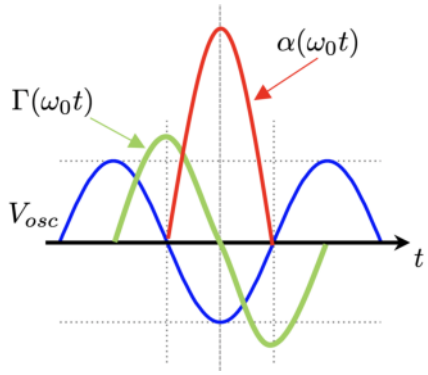


Fig. 4.6. Best placement of current modulation of phase noise.

to support this viewpoint is the *Colpitts* oscillator which is in Class-C operation, i.e. the current conduction angle of the main transistor is much less than 180°. As shown in Fig. 4.7, the peak of the current that being injected to the tank happens at the lowest voltage swing, corresponding to the zero-crossings of the ISF. Therefore, the effective ISF $\Gamma_{\text{eff}}(\omega_0 \tau)$ is optimized by virtue of the shape of $\alpha(\omega_0 \tau)$, so that noise current has minimal impact on the output phase.

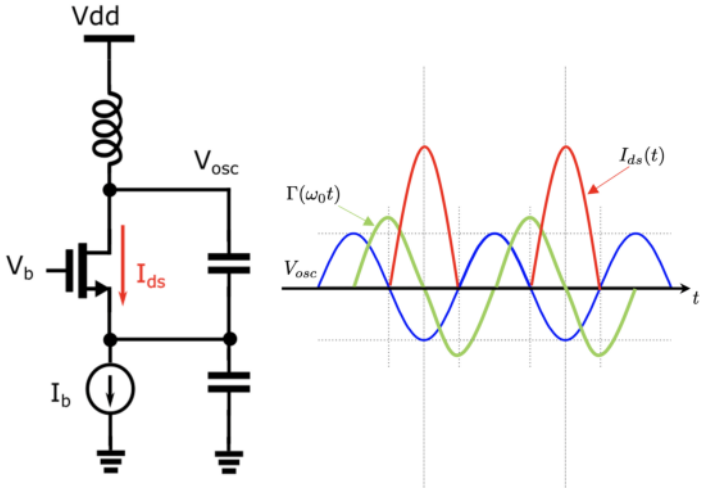


Fig. 4.7. The noise modulation function of Colpitts oscillators.

4.4 The Class-D operation of LC oscillators

So far, the phase noise model of oscillators have been investigated, and the phase noise optimization techniques using ISF and LTV model has been elaborated. Several CMOS *LC* VCOs optimized with Γ_{eff} has been proposed [57–59, 101–103] and the experimental results show good agreement with the LTV model. Nevertheless, the Class-B type VCOs still require a reasonable high supply voltage, which are not suitable for ultra-low-power / voltage applications. Harmonic oscillators such as Class-C VCO has been used for ultra-low-voltage application [92], but the output voltage swing is low due to the supply voltage limitation. The Class-D oscillator

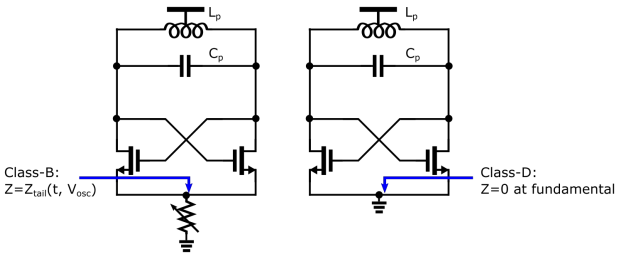


Fig. 4.8. Class-B and Class-D oscillators.

topology that has been proposed in [91, 104] makes the ultra-low-voltage opera-

tion possible without significantly sacrificing the VCO performance. As shown in Fig. 4.8, for certain supply voltage V_{DD}, the peak-to-peak output voltage swing of the Class-D VCO is around $3 \cdot V_{DD}$, while that of the Class-B VCO is around $2 \cdot V_{DD}$. The high voltage swing improves the VCO phase noise and driving strength. More importantly, the Class-D VCOs' power efficiency can beyond 90%, which makes it a promising solution for ultra-low-power applications.

Compared with the conventional Class-B VCOs using differential pair as the cross-coupled negative G_m generator, the cross-coupled transistor pair is pseudo-differential in Class-D topology, and are sized as switches with large aspect ratios. As a result, the *LC* tank of the Class-D oscillator is not time-invariant as the case for Class-B/C oscillators, in contrast the tank configuration has time-dependency. As

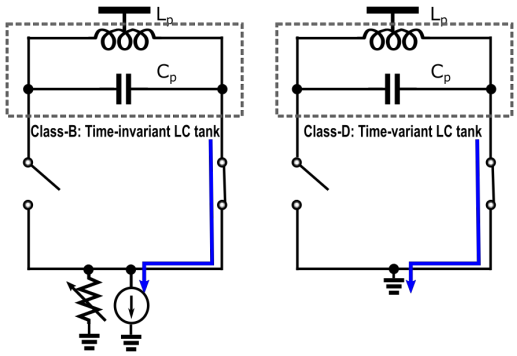


Fig. 4.9. Time-variant LC tank in Class-D oscillators.

can be seen in Fig. 4.9, due to the high output impedance of the tail current source, the inductor and capacitor in the Class-B/C tank are always in parallel, regardless of the status of the transistors. Therefore, the output nodes are isolated from signal ground. In the Class-D tank, however, each of the oscillator output node will be shorted to ground for half of the oscillation period $1/f_{\text{osc}}$ by the switches (i.e. the transistors in triode region), due to the absence of the tail current source. This time-variant *LC* tank hence shapes the voltage and current waveforms in such a way that the product of V_{ds} and I_{ds} of the transistors approaches to zero, therefore the average power dissipated on the active devices in one cycle:

$$P_{avg} = \frac{1}{T_{osc}} \int_0^{T_{osc}} V_{ds}(t) \cdot I_{ds}(t)\, dt \approx 0. \tag{4.27}$$

Therefore almost all power dissipation occurs inside the *LC* tank, which explains the high power efficiency of the Class-D topology.

4.4.1 Current and voltage waveforms of Class-D oscillators

The current flow through the inductor I_{La} is illustrated in Fig. 4.10, where $L_a = L_b = L/2$, $R_{La} = R_{Lb} = R_L/2$, $R_{Ca} = R_{Cb} = R_C/2$. $M_{1,2}$ are the two main transistors act as switches. During the first half of the oscillation period T_1, namely $0 < t < T_{\text{osc}}$,

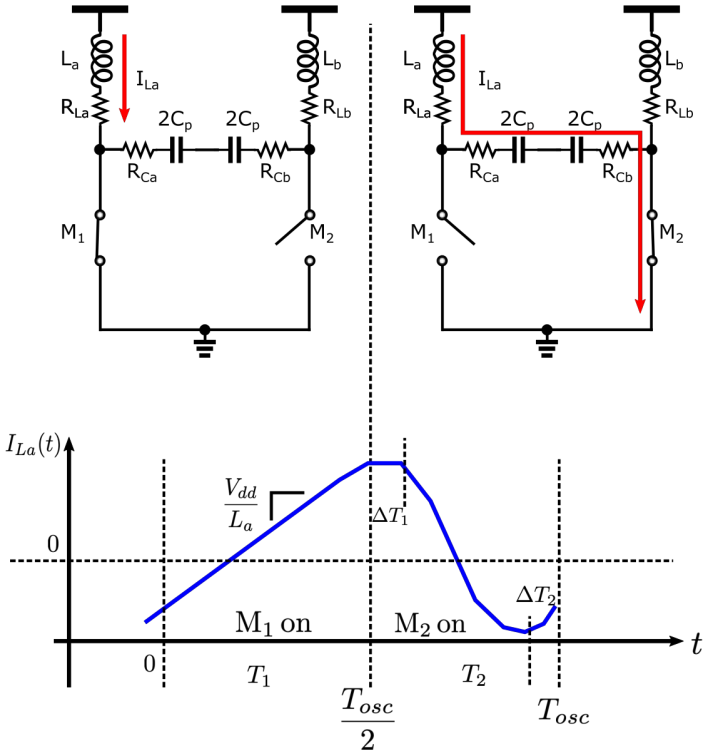


Fig. 4.10. Time domain current waveform of Class-D oscillators.

the switch M_1 is closed and M_2 is opened. The charging current through L_a can be derived as:

$$I_{La}(t) = I_{La}(0) + \frac{V_{dd}}{R_{La}} \cdot (1 - \mathrm{e}^{-t/\tau_1}), \qquad 0 < t < \frac{T_{\text{osc}}}{2}. \tag{4.28}$$

where $I_{La}(0)$ is the initial condition of the tank current, $\tau_1 = L/R_L$ is the time constant associated with the tank inductor. The derivative of $I_{La}(t)$ can be derived as:

$$\frac{dI_{La}(t)}{dt} = \frac{V_{dd}}{L_a} \cdot \mathrm{e}^{-t/\tau_1}, \qquad 0 < t < \frac{T_{\mathrm{osc}}}{2}. \tag{4.29}$$

During the second half of the oscillation period T_2, namely $T_{\mathrm{osc}}/2 < t < T_{\mathrm{osc}}$, the switch M_1 is opened and M_2 is closed. The current $I_{La}(t)$ will be re-directed to ground through L_a and the tank capacitor C, and the corresponding expression of the discharging current can be derived as :

$$I_{La}(t) = I_{pk} \cos[\,\omega_s(t - \frac{T_{\mathrm{osc}}}{2}) - \phi_0\,] \cdot \mathrm{e}^{-(t-\frac{T_{\mathrm{osc}}}{2})/\tau_2} \tag{4.30}$$

where it follows [91]:

$$\phi_0 \approx \arctan(\frac{2}{\pi}\frac{\omega_{\mathrm{osc}}}{\omega_s}) \approx \frac{2}{\pi}\frac{\omega_{\mathrm{osc}}}{\omega_s}, \tag{4.31}$$

$$I_{pk} \approx \sqrt{(\frac{V_{dd}}{L_a}\frac{1}{\omega_s})^2 + (\frac{V_{dd}}{2L_a}\frac{T_{\mathrm{osc}}}{2})^2}, \tag{4.32}$$

$$\tau_2 = \frac{L}{R_L + R_C}. \tag{4.33}$$

The parameter ω_s is the resonant frequency of the series-LC network:

$$\omega_s = \frac{1}{\sqrt{L_a C}} = \sqrt{\frac{2}{LC}} = \frac{2\pi}{T_s}. \tag{4.34}$$

Since the transition time from ΔT_1 and ΔT_2 is non-zero, the time interval T_2 can be written as:

$$T_2 = \frac{1}{2}T_{\mathrm{osc}} = \Delta T_{12} + \frac{1}{2}T_s + \Delta T_{21} = 2\Delta T_{12} + \frac{1}{2}T_s, \tag{4.35}$$

where the transition time $\Delta T_{12} = \Delta T_{21}$ because of the symmetric current waveform during T_2. Combining Eqs. (4.31), (4.34) and (4.35) it can be derived that:

$$T_{\mathrm{osc}} = 4\Delta T_{12} + T_s = 4\frac{\phi_0}{\omega_s} + T_s = \frac{4}{\pi^2}\frac{T_s^2}{T_{\mathrm{osc}}} + T_s, \tag{4.36}$$

hence the oscillation frequency ω_{osc} can be calculated by solving Eq. (4.36) and written as:

$$\omega_{\text{osc}} = (\frac{\pi}{8}\sqrt{\pi^2+16} - \frac{\pi^2}{8}) \cdot \omega_s = \frac{\omega_s}{\alpha} \approx 0.76\,\omega_s. \tag{4.37}$$

From Eq. (4.37) it can be concluded that for the same LC tank, the oscillation frequency of Class-D oscillator is higher than its Class-B/C counterpart by a factor of $0.76 \times \sqrt{2} = 1.08$. The voltage waveforms of the Class-D oscillator is derived

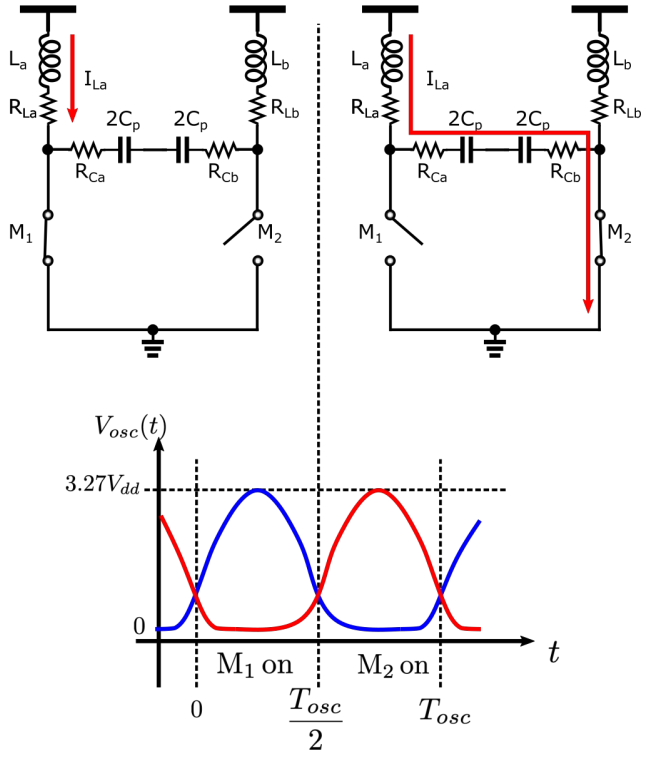


Fig. 4.11. Time domain voltage waveform of Class-D oscillators.

by integrating the current in Eq. (4.30) on the tank capacitance C during T_2:

$$V_{\text{osc}}(t) = \frac{1}{C}\int_{T_{\text{osc}}/2}^{T_{\text{osc}}} I_{La}(t)\,dt = V_{dd} + V_a \cdot \sin[\,\omega_s(t - \frac{T_{\text{osc}}}{2}) - \phi\,], \tag{4.38}$$

where it follows

$$V_a = V_{dd}\sqrt{\frac{\alpha^2\pi^2}{4}+1}, \tag{4.39}$$

so that the peak voltage swing therefore can be calculated as:

$$V_{\text{osc, peak}} = V_{dd} + V_a \approx 3.27\,V_{dd}. \tag{4.40}$$

In practice, $V_{\text{osc, peak}}$ could be slightly lower than the value given in Eq. (4.40) due to tank loss. Nonetheless, the output swing is still much higher than the V_{dd}, and will be set by the supply voltage. This is expected because the lacking of tail-current source makes the Class-D oscillator work in voltage-limiting regime [57, 58] rather than current-limiting regime.

As analyzed in [91], the calculation of current consumption of Class-D oscillators is cumbersome. The DC current is given as:

$$I_{dc} \approx (7.1 - 2\,\frac{\tau_2}{\tau_1}) \cdot \frac{(R_C + R_L)V_{dd}}{\omega_{\text{osc}}^2 L^2}, \tag{4.41}$$

depending on the ratio of τ_2/τ_1, Eq. (4.41) has an error up to 10% compared with more lengthy and exact equations. The more useful insight is that a large τ_2/τ_1 ratio helps reduce the power consumption, or in other words, minimizing R_C and a relative increment of R_L reduce the overall power consumption. This is another difference with respect to the Class-B/C oscillators, where R_L and R_C have the same impact on the power consumption.

4.4.2 Phase noise analysis of Class-D oscillator

The phase noise of Class-D oscillators can be analyzed with the techniques proposed in [105] based on ISF and LTV model. Due to the time-varying nature of the *LC*-tank, the ISFs are derived separately for the inductive and capacitive losses, where the detailed analysis can be found in [91]. For the Class-D oscillators, the

ISFs are given as below:

$$\Gamma_{R_{La}}(\omega_{\rm osc}\tau) = \begin{cases} \dfrac{-\varepsilon}{V_a(1+\varepsilon^2)}\omega_{\rm osc}\,, & \tau \in [0, \dfrac{T_{\rm osc}}{2}] \\ \dfrac{\sin[\,\omega_s(\,\dfrac{\tau - T_{\rm osc}}{2}\,) - \phi_0\,]}{V_a(1+\varepsilon^2)}\omega_{\rm osc}\,, & \tau \in [\,\dfrac{T_{\rm osc}}{2}\,, T_{\rm osc}] \end{cases} \tag{4.42}$$

$$\Gamma_{R_{Lb}}(\omega_{\rm osc}\tau) = \begin{cases} \dfrac{\sin(\,\omega_s\,\tau - \phi_0\,)}{V_a(1+\varepsilon^2)}\omega_{\rm osc}\,, & \tau \in [0, \dfrac{T_{\rm osc}}{2}] \\ \dfrac{-\varepsilon}{V_a(1+\varepsilon^2)}\omega_{\rm osc}\,, & \tau \in [\,\dfrac{T_{\rm osc}}{2}\,, T_{\rm osc}] \end{cases} \tag{4.43}$$

where $\Gamma_{R_{La}}(\omega_{\rm osc}\tau)$ and $\Gamma_{R_{Lb}}(\omega_{\rm osc}\tau)$ are the ISFs of R_{La} and R_{Lb},

$$\Gamma_{R_C}(\omega_{\rm osc}\tau) = \begin{cases} \dfrac{\sin(\,\omega_s\,\tau - \phi_0\,)}{V_a(1+\varepsilon^2)}\omega_{\rm osc}\,, & \tau \in [0, \dfrac{T_{\rm osc}}{2}] \\ \dfrac{-\sin[\,\omega_s(\,\dfrac{\tau - T_{\rm osc}}{2}\,) - \phi_0\,]}{V_a(1+\varepsilon^2)}\omega_{\rm osc}\,, & \tau \in [\,\dfrac{T_{\rm osc}}{2}\,, T_{\rm osc}] \end{cases} \tag{4.44}$$

is the ISF of R_C, $\varepsilon = V_{dd}/V_a$ is a constant around 0.44, as derived using Eq. (4.40). Eqs. (4.41) to (4.43) are plotted in Fig. 4.12, from which it can be seen that the rms ISF value of R_{La} and R_{Lb} is equal. Therefore, the $1/f^2$ phase noise spectral density can be derived as:

$$L(\Delta\omega) = 10\log[2k_BTR_L\cdot\Gamma^2_{R_L,rms} + 2k_BTR_C\cdot\Gamma^2_{R_C,rms}] - 20\log(\Delta\omega), \tag{4.45}$$

and the FoM [106] of the oscillator at frequency offset $\Delta\omega$ can be calculated as:

$$\text{FoM} = L(\Delta\omega) - 20\log[\frac{\omega_{osc}}{\Delta\omega}] + 10\log(V_{dd}\cdot I_{dc}). \tag{4.46}$$

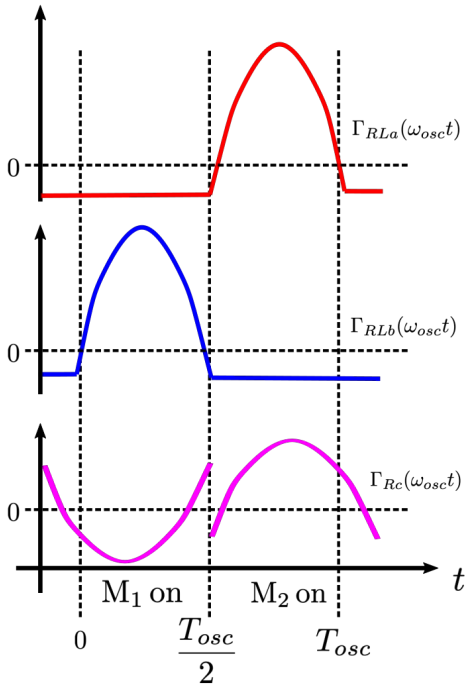


Fig. 4.12. The ISF of R_{La}, R_{Lb} and R_C.

4.4.3 A 4.5-5.4 GHz, 0.2-V, 0.28-mW Class-D VCO

In this work, a Class-D VCO is implemented using a 65-nm CMOS process as shown in Fig. 4.13. The symmetric inductor L with center-tap is used as the tank inductor, and a tail inductor L_T is used for improving the $1/f^2$ and $1/f^3$ noise, by filtering out the second-harmonic content [107]. The inductance and Q-factors of L and L_T are illustrated in Fig. 4.14, where Q_L and Q_{LT} are optimized at 4.8 GHz and 9.6 GHz, respectively.

The tuning of the tank resonant frequency is obtained by both continuous fine tuning using varactor C_{var}, and discrete coarse tuning via a 5-bit binary weighted switch-capacitor bank. It should be noted that by introducing the resonate tail filtering technique, the waveforms of the oscillator's output V_{osc} is different than the V_{ds} of the cross-coupled pair, and this topology is more like a hybrid of Class-B and Class-D. As shown in Fig. 4.15, V_{osc} is similar to the output voltage waveform of the traditional Class-B VCOs, since the resonant tail filter act as a current source

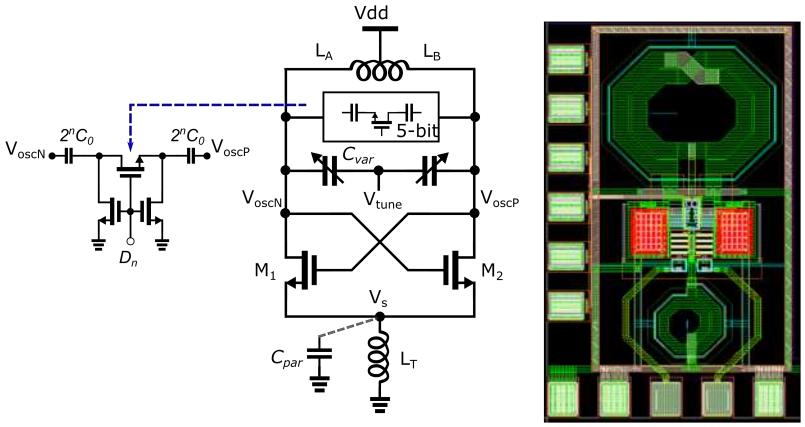


Fig. 4.13. Implementation of Class-D VCO with tail inductor.

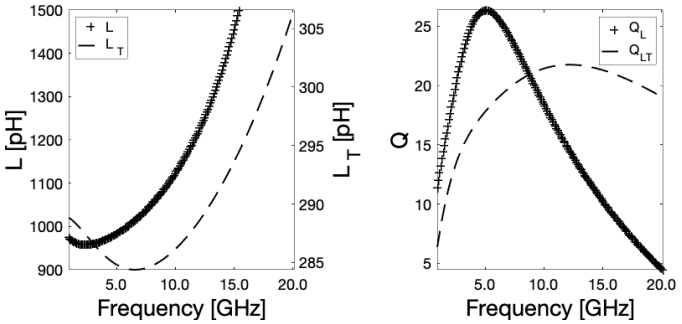


Fig. 4.14. The inductance and Q-factor of the tank and tail inductors.

with zero-voltage headroom. In addition, the source of the cross-coupled pair, V_s, shows high impedance at the vicinity of $2\omega_{\text{osc}}$, which caused by the parallel resonance of L_T and the parasitic capacitance associated with the source node, C_{par}. This parallel $L_T C_{par}$ network at the tail "traps" the second harmonic current inside, therefore prevents the noise current at $2\omega_{\text{osc}}$ flow into the main LC tank. As a result, at $2\omega_{\text{osc}}$, the R_{on} of $M_{1,2}$ will not load the tank as heavily as that of a Class-D oscillator with the source node directly short to ground, hence reduces the second harmonic content and yield largest differential voltage amplitude.

The tuning characteristics of the Class-D VCO implementation is shown in Fig. 4.16, where it shows a 18% tuning range with 5-bit coarse discrete tuning bank. The VCO gain, K_{vco}, shows dependency on the discrete coarse tuning code,

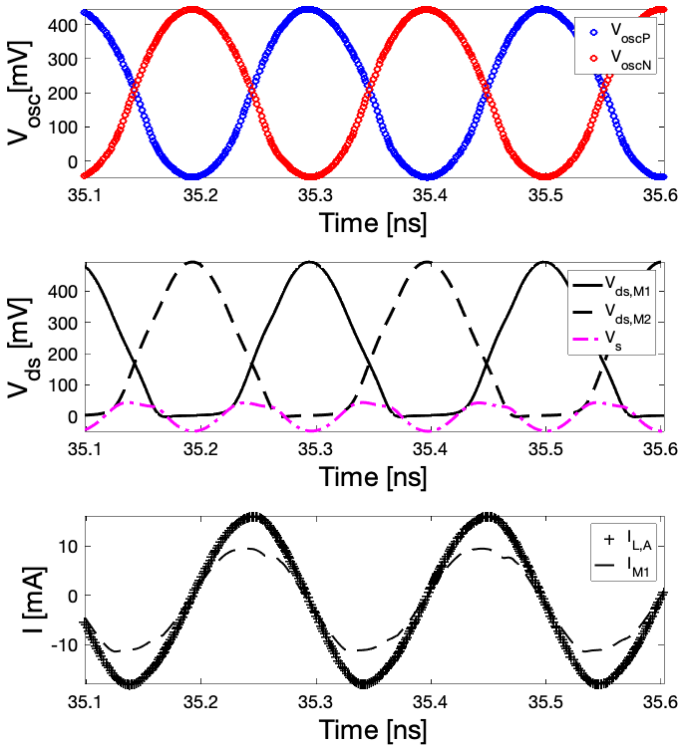


Fig. 4.15. Voltage and current waveforms of the Class-D VCO with tail inductor.

where the $K_{vco,max}$ appears when $D_4D_3D_2D_1D_0 = 5'd0$ and $K_{vco,min}$ appears when $D_4D_3D_2D_1D_0 = 5'd31$. The gap between each coarse frequency band is covered by changing V_{tune} of the varactors from 0 V to 0.5 V.

The ISF function of the Class-D VCO with tail inductor is achieved based on the method proposed in [108, 109] and illustrated in Fig. 4.17. The coefficients of $\Gamma(\omega_0\tau)$ in Eq. (4.15) is derived from periodic steady state (PSS) and periodic transfer function (PXF) simulations with 10 harmonics. Specifically, the oscillator's ISF is derived in the frequency domain rather than in the time domain. A small test current tone $i_{\text{test}}(t)$ at a frequency offset $\Delta\omega$ around the n-th harmonic of the output voltage is injected into the oscillator by connecting an ideal current

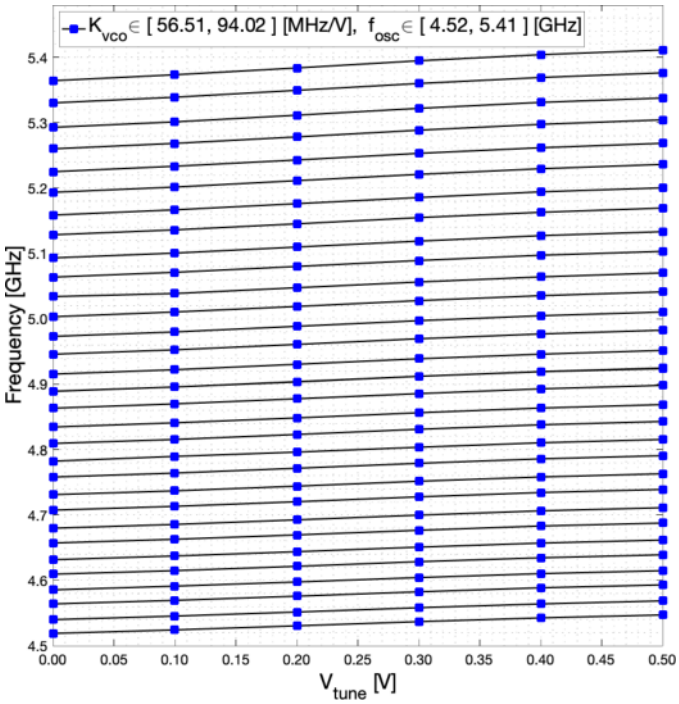


Fig. 4.16. Tuning characteristics of the Class-D VCO implementation.

source across the drain-source of M_1,

$$\begin{aligned} i_{\text{test}}(t) &= i_{\text{test}}[\cos(n\omega_{osc}+\Delta\omega)t] \\ &= i_{\text{test}}[\cos[(\omega_{osc}+\Delta\omega)t+(n-1)\omega_{osc}t]], \end{aligned} \tag{4.47}$$

where $n-1$ is the index of PXF sidebands. The current perturbation causes a phase modulation at $\Delta\omega$ of the output voltage at the fundamental frequency ω_{osc}. According to Eq. (4.16), the excess output phase can be re-written as:

$$\phi_o(t) \approx \frac{c_n i_{\text{test}}}{2\Delta\omega}\sin(\Delta\omega-\theta_n). \tag{4.48}$$

Therefore, the drain-source voltage at fundamental frequency can be expressed as:

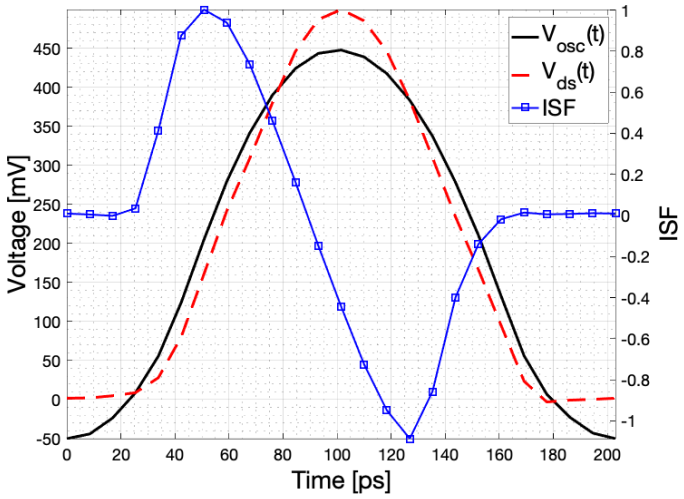


Fig. 4.17. The impulse sensitivity function (ISF) of the Class-D VCO with tail inductor.

$$\begin{aligned} V_{ds}(t) &= A_0 \cos[\omega_{osc} t + \theta_0 + \phi_o(t)] \\ &\approx A_0 \cos(\omega_{osc} t + \theta_0) \\ &+ \frac{A_0 c_n i_{\text{test}}}{4\Delta\omega} \cos[(\omega_{osc} + \Delta\omega)t + \psi_n^-] \\ &+ \frac{A_0 c_n i_{\text{test}}}{4\Delta\omega} \cos[(\omega_{osc} - \Delta\omega)t + \psi_n^+], \end{aligned} \tag{4.49}$$

where θ_0 is the random initial phase of $V_{ds}(t)$, $\psi_n^- = \theta_0 - \theta_n$, $\psi_n^+ = \theta_0 + \theta_n$. Note that Eq. (4.49) has both upper and lower sideband content, since $i_{\text{test}}(t)$ in Eq. (4.47) has upper sideband content at $\omega_{osc} + \Delta\omega$, the periodic transimpedance from $i_{\text{test}}(t)$ at $n-1$ sideband to $V_{ds}(t)$ at $\omega_{osc} + \Delta\omega$ can be computed as:

$$|Z(n-1)| = \frac{A_0\, c_n}{4\Delta\omega}, \tag{4.50}$$

$$\angle Z(n-1) = \psi_n^-, \tag{4.51}$$

where the magnitude $|Z(n-1)|$ and unwrapped phase $\angle Z(n-1)$ can be directly simulated by PXF. The magnitude A_0 and the initial phase θ_0 of $V_{ds}(t)$ at the fun-

damental frequency can be simulated by PSS. Therefore, the coefficients c_n and the phase θ_n of $\Gamma(\omega_{osc}t)$ can be derived as:

$$c_n = \frac{4\Delta\omega|Z(n-1)|}{A_0}, \tag{4.52}$$

$$\theta_n = \theta_0 - \angle Z(n-1). \tag{4.53}$$

The phase noise of the class-D VCO is shown in Fig. 4.18, where the phase noise is

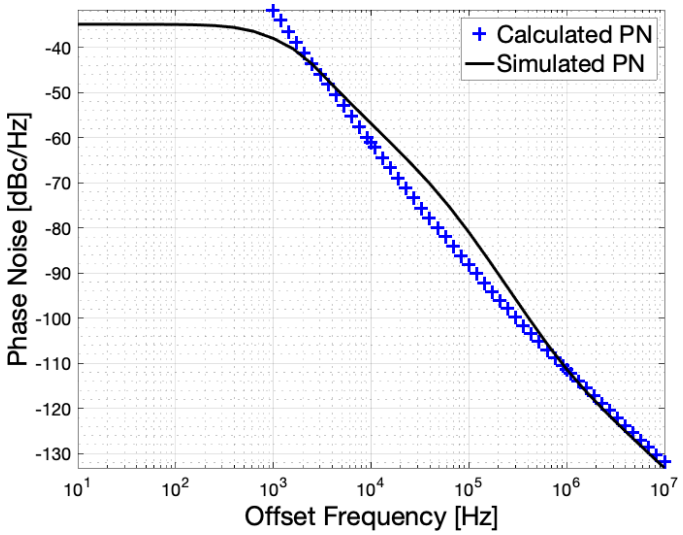


Fig. 4.18. Phase Noise of the Class-D VCO.

calculated by substituting Eqs. (4.52) and (4.53) into Eqs. (4.18) to (4.20), (4.23), (4.25) and (4.26), and is simulated by pnoise of Spectre-RF simulator. Both the calculated and simulated results agree with each other and show a $-113\,\mathrm{dBc/Hz}$ phase noise at 1 MHz offset. The FoM of $-192\,\mathrm{dBc/Hz}$ is calculated by using Eq. (4.46) and the performance is compared with the state-of-the-arts in Table 4.1.

Table 4.1: COMPARISON WITH STATE-OF-THE-ARTS.

Design	[92]	[106]	[103]	[102]	This work
Technology	0.18 µm	0.18 µm	65 nm	0.18 µm	65 nm
Topology	Class-C dual-conduction	Transformer feedback	Class-F	Class-C push-pull	Class-D w tail inductor
V_{DD} [V]	0.2	0.5	1.25	1.8	0.2
Power Consumption [mW]	0.114	0.57	15	2.16	0.28
Frequency [GHz]	4.5	3.8	3.7	6.75	5
Tuning Range [%]	NA	8.4	25	20.8	18
Phase Noise [dBc/Hz]	-104 @ 1MHz	-119 @ 1MHz	-142.2 @ 3MHz	-123 @ 2MHz	-113 @ 1MHz
FoM [dBc/Hz]	-187	-193	-192.2	-191	-192.5
$1/f^3$ Corner [kHz]	200	NA	300-700	200	2

Chapter 5

Conclusions

In this thesis, a few critical building blocks of a "Smart Stent" system are analyzed, designed and implemented. The system is powered wirelessly in the mid-field of an external RF source and *in-vitro* measurements support the viability of integration of a medical stent and CMOS integrated circuits. The essential circuit blocks such as rectifier, LDO, and VCO are implemented with ultra-low-power consumption to reduce the required external source power, by virtue of using the proposed circuit topologies. In addition, an optimum external RF source is designed to enhance the power density around the implanted stent, and to improve the overall wireless power transfer efficiency.

5.1 Future Work

For the proof-of-concept prototype design in this work, the CMOS IC die is not directly embedded on the stent, and we have used chip-on-board (COB) solution. Therefore, the parasitics introduced by the interconnection degrade the system performance significantly. More importantly, COB is not realistic for the application scenario, considering the stent will be put inside the human artery. More advanced packaging or integration solutions should be further investigated to make the "active stent" practical and safe to be implanted.

5.1.1 Stent characterization in in-vitro and in-vivo environments

In this work, the performance of the proposed smart stent has been characterized in the air. A more accurate stent model can be derived by testing the stent *in-vivo*, and the methodology presented in this work can be reused for more elaborate *in-vitro* and *in-vivo* experiments. The electrical properties of the stent will be affected by its surrounding environment. For instance, when the stent is placed inside a typical *in-vitro* or *in-vivo* environment, the stent impedance will change. This is in part due to the relative permittivity, ε_r, of the surrounding media, for example, tissues and blood, where the effective wavelength in the media λ_{eff} will be $\sqrt{\varepsilon_r}$ times shorter than the wavelength in the free space, λ_0. When the physical size of the stent becomes comparable to λ_{eff} the radiation resistance can be quite different. Further experiments are required for proper *in-vitro* or *in-vivo* characterization. Furthermore, the proposed matching network should be designed to cover the stent impedance variation caused by the environment.

5.1.2 System assembly and bio-compatibility

Ideally, the bare IC die and exposed sections of bond-wire, when assembled on the stent, should be covered with a biocompatible coating such as a silicone sealant. The IC die should also be enclosed by a package with metal shield to minimize electrical field coupling. To make the whole system bio-compatible, the overall stent system should be coated with biocompatible material such as urethanes, polycarbonates, silicones, or styrenes. The coating should be non-conductive to reduce the dielectric loss. Furthermore, the mechanical strength of the assembly should be considered since during stent expansion the connections between IC package and stent will be stressed. Therefore, further investigations are required for proper system assembly and biocompatible packaging.

5.1.3 General link efficiency improvement

The external RF source needs multi-phase excitation at its input ports, so that the magnetic field will be focused in the direction pointed to the stent. The multi-phase excitation course should also be calibrated to reach to the peak of the power trans-

fer efficiency. In addition, the matching network and the rectifier will also need to be tuned dynamically to achieve the optimum large-signal input impedance. The adaptive tuning of the external RF source and the implant requires a transmitter (Tx) on the implanted site to send the PDL level back to the external source in real time, and multi-phase generator such as phase mixer or phase interpolator based on phase-locked loops (PLLs) or delay-locked loops (DLLs) can be used to drive the multi-external source. The implementation of the Tx at the implant side should focus on improving the efficiency and lower the quiescent power. More importantly, the full-duplex communication of the Tx and Rx should be investigated for the single-stent (antenna). The multi-phase generation on the external side should focus on increasing the phase resolution and the output power. In addition, the adaptive tuning also requires the necessary processing and control circuits such as a finite-state machine (FSM), which should be monolithically implemented.

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