Enhanced Performance of P-GaN Gate AlGaN/GaN High-Electron-Mobility Transistors for Power Applications

by

Guangnan Zhou

M.A.Sc., The University of British Columbia, 2017

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF

THE REQUIREMENTS FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

in

THE FACULTY OF GRADUATE AND POSTDOCTORAL STUDIES

(Materials Engineering)

THE UNIVERSITY OF BRITISH COLUMBIA

(Vancouver)

October 2021

The following individuals certify that they have read, and recommend to the Faculty of Graduate and Postdoctoral Studies for acceptance, the dissertation entitled:

Enhanced Performance of P-GaN Gate AlGaN/GaN High-Electron-Mobility Transistors for Power Applications

submitted by Guangnan Zhou in partial fulfillment of the requirements for

the degree of Doctor of Philosophy

in Materials Engineering

Examining Committee:

Guangrui Xia, Associate Professor, Department of Materials Engineering, UBC
Co-supervisor

Hongyu Yu, Professor, School of Microelectronics, Southern University of Science and Technology
Co-supervisor

Edmond Cretu, Associate Professor, Department of Electrical and Computer Engineering, UBC
Supervisory Committee Member

William Dunford, Professor, Department of Electrical and Computer Engineering, UBC
University Examiner

Chad W. Sinclair, Professor, Department of Materials Engineering, UBC
University Examiner

Additional Supervisory Committee Members:

David Dixon, Professor, Department of Materials Engineering, UBC
Supervisory Committee Member

Abstract

Gallium nitride (GaN) possesses excellent physical properties, such as a high critical electric field, a high saturation velocity, a high electron mobility, and a good thermal stability. Due to these superior material properties, GaN-based high-electron-mobility transistors (HEMTs) have performances superior to their silicon (Si) counterparts. They can operate at higher voltages, currents, frequencies, and temperatures, making them ideal devices for the next-generation high-efficiency power converters applications, such as phone chargers, electric vehicles, data centers and renewable energy. For switching applications, normally-off transistors are required to provide adequate safety. Due to the positive and stable threshold voltage, *p*-GaN gate HEMT technology is the most promising candidate among many options of normally-off HEMTs. Meanwhile, there are still some problems to be addressed (e.g., low threshold voltage, low gate breakdown voltage, gate reliability) for the *p*-GaN gate technology.

In this dissertation, we present a comprehensive study of *p*-GaN gate HEMTs, including the work on failure mechanisms and three different methods to enhance the device performance. Chapter 1 includes a background review for power devices, GaN material properties and basic AlGaN/GaN HEMT structures. In Chapter 2, a typical fabrication process and test methods for *p*-GaN gate HEMTs are described in detail. Chapter 3 demonstrates a novel measurement and analysis method to identify three different gate failure mechanisms. Based on the baseline process in Chapter 2 and the analysis method in Chapter 3, three different structures aimed at enhancing the *p*-GaN gate HEMTs' electrical performance and reliability are demonstrated in Chapters 3 to

6, including metal/graphene gates, ultra-high-resistance Au/Ti/*p*-GaN junctions, and doping engineering. The three different methods have their unique strengths. Chapter 7 concludes this work and suggests some future directions.

Lay Summary

For decades, silicon (Si)-based transistors have been extremely successful in power applications that help to convert, manage, and control electric power. However, their performances are now close to their theoretical limits determined by the fundamental material properties of Si. GaN power transistors can provide better power efficiencies, faster speeds, and lower system costs.

The leading GaN-based power transistors are *p*-GaN gate AlGaN/GaN high-electron-mobility transistors (HEMTs), though there are still room to improve their performances and reliabilities. This work presents a comprehensive study of *p*-GaN gate HEMTs. It demonstrated a new failure mechanism analysis method and three different methods to enhance the devices' performances.

Preface

Chapter 1. Figures 1.1, 1.5, and 1.15 are used with permission from applicable sources. All the work presented henceforth was conducted at the Southern University of Science and Technology of China by the author. Without the contributions from the collaborators, however, this thesis could not have been accomplished.

The work discussed in Chapter 3 has been published [Zhou, G., Zeng, F., Jiang, Y., Wang, Q., Jiang, L., Xia, G.*, & Yu, H.* (2021). Determination of the Gate Breakdown Mechanisms in p-GaN Gate HEMTs by Multiple-Gate-Sweep Measurements. *IEEE Transactions on Electron Devices*, 68(4), 1518-1523]. I was the lead investigator, responsible for all major areas of concept formation, experimentation, data collection and analysis, as well as the majority of manuscript composition. Fanming Zeng was involved in the mask design and device fabrication. Yang Jiang performed with the SEM characterization. Qing Wang and Lingli Jiang contributed to manuscript composition and edits.

The work discussed in Chapter 4 has been published [Zhou, G., Wan, Z., Yang, G., Jiang, Y., Sokolovskij, R., Yu, H.*, & Xia, G.* (2020). Gate leakage suppression and breakdown voltage enhancement in p-GaN HEMTs using metal/graphene gates. *IEEE Transactions on Electron Devices*, 67(3), 875-880]. I was the lead investigator, responsible for all major areas of concept formation, experimentation, data collection and analysis, as well as manuscript composition. Zeyu Wan was involved in the *p*-GaN gate etching and passivation deposition. Yang Jiang contributed to the sample preparation for transmission electron microscopy (TEM). Prof. Gaiying Yang

performed the TEM characterization and helped analyze the data. Robert Sokolovskij was involved in the early stages of concept formation and contributed to manuscript edits.

The work discussed in Chapter 5 has been published [Zhou, G., Jiang, Y., Yang, G., Wang, Q., Fan, M., Jiang, L., Yu, H.*, & Xia, G.* (2021). Formation of ultra-high-resistance Au/Ti/p-GaN junctions and the applications in AlGaN/GaN HEMTs. *AIP Advances*, 11(4), 045207]. I was the lead investigator, responsible for all major areas of concept formation, experimentation, data collection and analysis, as well as the majority of manuscript composition. Yang Jiang and Mengya Fan contributed to metal deposition and data collection. Qing Wang and Lingli Jiang contributed to manuscript composition and edits. Prof. Gaiying Yang performed the TEM characterization and helped analyze the data.

I was the lead investigator for the projects discussed in Chapters 6, where I was responsible for all major areas of concept formation, experimentation, data collection and analysis, as well as the majority of manuscript composition. Fanming Zeng and Kai Cheng were involved in the early stages of concept formation. They also contributed to the epitaxial wafer growth. Rongyu Gao and Qing Wang contributed to devices fabrication and electrical data collection.

Profs. Guangrui Xia and Hongyu Yu supervised all the above projects. Prof. Xia is the principal supervisor of the author in the PhD program, and Prof. Yu is the co-supervisor. They were also the corresponding authors of the above publications.

Table of Contents

List of Tables

List of Figures

List of Symbols

	Unit	Description
BV	V	Breakdown Voltage
BV_{DSS}	V	Off-state drain to source breakdown voltage
E_A	eV	Activation energy
E_{CR}	V/cm	Breakdown field
E_F	eV	Fermi level
E_G	eV	Bandgap
$F(t_{BD})$		Cumulative failure probability
I_D	mA/mm	On-state drain current
I_{DSS}	mA/mm	Off-state drain leakage current
I_G	mA/mm	Gate leakage current
I_{SAT}	mA/mm	Drain saturation current
L_G	µm	Gate length
L_{GD}	µm	Gate-drain distance
L_{GS}	µm	Gate-source distance
n_s	cm^{-2}	2DEG carrier density
P_{PZ}	cm^{-2}	Piezoelectric polarization
P_{SP}	cm^{-2}	Spontaneous polarization
R_C	Ω•mm	Contact resistance
R_{ON}	Ω•mm	On-state resistance
R_{SH}	Ω/square	Sheet resistance
SS	mV/dec	Sub-threshold swing
t_{BD}	s	Time-to-failure
V_{DS}	V	Drain-to-source voltage
$V_{G\text{-}max}$	V	Maximum Gate Operation Voltages
V_{GS}	V	Gate-to-source voltage
V_{TH}	V	Threshold voltage
W_G	µm	Gate width
Φ_B	eV	Schottky barrier height
Φ_M	eV	Metal work function
χ_S	eV	Electron affinity of the semiconductor

List of Abbreviations

2DEG	Two-Dimensional Electron Gas
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
AlGaN	Aluminum Gallium Nitride
AlN	Aluminum Nitride
BD	Breakdown
CMOS	Complementary Metal Oxide Semiconductor
CTLM	Circle Transmission Line Model
D	Drain
D-mode	Depletion mode
E-mode	Enhancement mode
FET	Field Effect Transistor
FP	Field Plate
G	Gate
GaN	Gallium Nitride

GIT	Gate Injection Transistor
HEMT	High Electron Mobility Transistor
i-GaN	Intrinsic Gallium Nitride
ICP	Inductively Coupled Plasma
LEDs	Light Emitting Devices
MBE	Molecular Beam Epitaxy
MIS-HEMTs	Metal-Insulator-Semiconductor High Electron Mobility Transistors
MOCVD	Metal Organic Chemical Vapor Deposition
MOS	Metal-Oxide-Semiconductor
p-GaN	p-type doped Gallium Nitride
S	Source
S/D	Source/Drain
sccm	standard cubic centimeters per minute
TDGB	Time-Dependent Gate Breakdown
TEM	Transmission Electron Microscopy
u-GaN	Unintentionally-doped Gallium Nitride
WBG	Wide Band Gap

Acknowledgements

My journey towards the scientific discoveries in my PhD program has never been easy. The knowledge, the time, and the collaboration from the wonderful people I met along the journey have been extremely helpful for me. Without all their kind and strong support and guidance, this thesis would not have been possible. Here I would like to express my sincerest gratitude to them.

First and foremost, I would like to express my deepest gratitude to my advisors, Prof. Guangrui Xia and Prof. Hongyu Yu, for their continuous support, guidance, and encouragement throughout my PhD study. They offered me the opportunity to pursue the degree. Prof. Xia helped me in all the time of research and writing of this dissertation. She has always been patient and provides valuable feedback with lots of inspiring questions. My PhD research work highly benefits from her extensive knowledge in the semiconductor field. I would like to thank Prof. Yu for his great support, which allowed me to experience countless trials and errors. Without his support, I couldn't have gone through the most challenging moments in my research. I am also grateful to them for the spirit and attitude they passed on to me towards people and things in life. I could not have imagined having better advisors for my PhD study.

I would like to thank Prof. David Dixon and Prof. Edmond Cretu for being my supervisory committee members and providing valuable feedback for my research. I wish to thank Prof. Willam Dunford and Prof. Chad W. Sinclair for being my thesis examination committee members and providing constructive comments for this work. I would like to offer my deepest gratitude to Prof. Wai Tung Ng for being my thesis examiner. His suggestions are always valuable and inspiring. Without the help and the guidance from my examining committee, I wouldn't have made it. The improvement from them made my dissertation something I can be proud of having written.

The study and research were conducted according to the joint-PhD program agreement between UBC and Southern University of Science and Technology (SUSTech). I wish to thank SUSTech for offering me the scholarships. I wish to thank the Materials Characterization and Preparation Center, SUSTech, for providing me with the necessary facilities. I wish to express my thanks to the technical staff at SUSTech: Xuhang Ma, Rui Zhang, Yao Wang, and Chunzhu Wang.

I cannot finish this thesis work without the strong support and discussions from the GaN-mates as well as my lunchmates: Dr. Fanming Zeng, Mengya Fan, Dr. Weichih Cheng, Yang Jiang, Dr. Robert Sokolovskij, Wenmao Li, Xinpeng Lin, Yongle Qi, Siqi Lei, Jiaqi He, Chuying Tang, Yi Zhang, Minghao He, Xiguang Chen, Qi Ge, Zepeng Qiao, Hongze Zhen, Qiaoyu Hu, Lina Liao, Chenkai Deng, Honghao Lu, Linqi Li, Fangzhou Du, and Kangyao Wen. It is a great pleasure to have a group of such nice people around. Moreover, I would like to thank Prof. Gaiying Yang for her great help with the TEM observation and analysis. I wish to give my special thanks to Prof. Qing Wang. She gave me valuable instructions in not only the semiconductor field and but also lots of life philosophies. I appreciate the help from my friends and colleagues at UBC. Yunlong Zhao, Zeyu Wan, Limin Wang, and Jia Guo are my groupmates, and we had many interesting discussions during group meetings that greatly broadened my knowledge in microelectronics.

I would like to give my deepest thanks to Shunjie Huang for sharing her life with me. In times of happiness and hard, she's always there. Her love and endless support are beyond description, and the words are not sufficient for me to express how I feel for her. Last but not least, special thanks are owed to my parents, who have supported me throughout my years of education, both morally and financially.

Chapter 1: Introduction to GaN Technology for Power Applications

1.1 Background for Power Devices

Electrical power has been one of the major driving forces of mankind's modernization, and is essential in our everyday lives. As core elements in electrical power utilization, power electronics are the electronic circuits used to control, convert, and manage electric currents or voltages or powers. They are widely used in switching power supplies, power converters, power inverters, motor drives, and so on, which are essential to consumer products and the harvesting and utilization of energies (Figure 1.1).

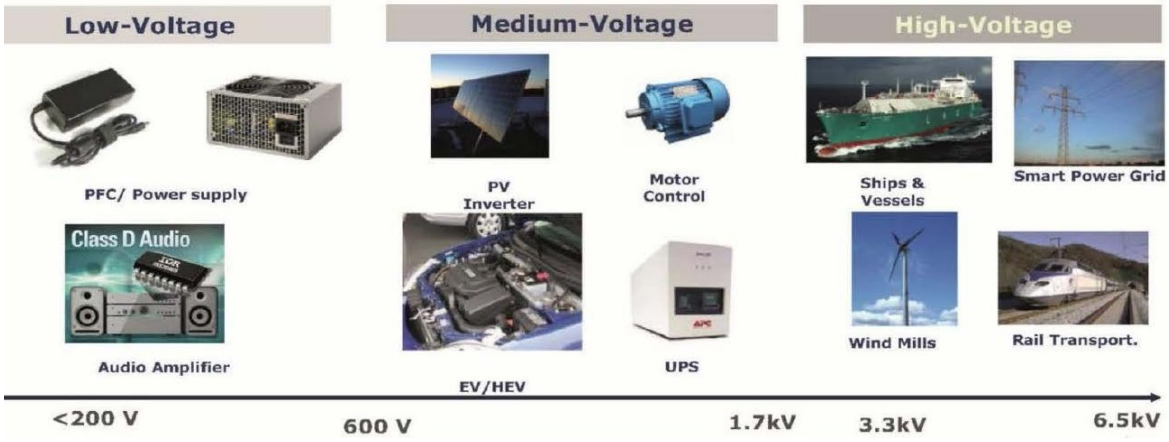


Figure 1.1 Applications of power electronics in power management and control. Figure courtesy of Ref. [1].

A typical power electronic system consists of a power source, a filtering mechanism, a power conditioner, a load, and a control circuit, as shown in Figure 1.2. A power conditioner consists of an arrangement of semiconductor devices operating in the switched mode, which means that the device is switched between the "OFF" state and the "ON" state by the control of the gate driver [2].

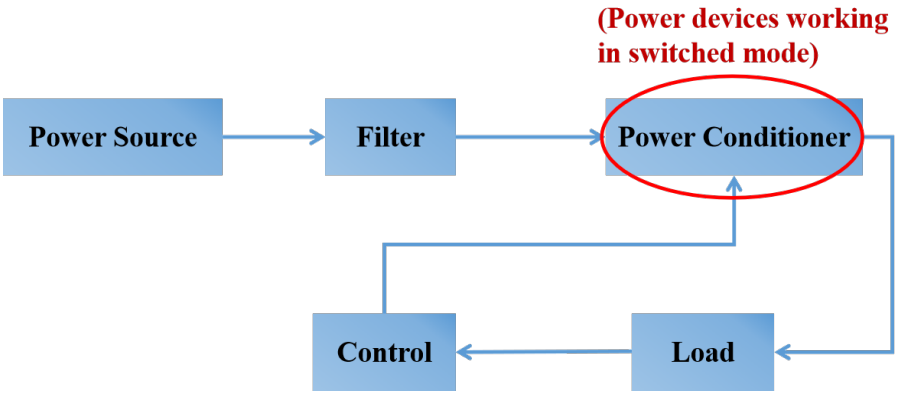


Figure 1.2 Components of a power electronic system and power semiconductor devices in power conditioners.

An ideal switch should feature zero leakage current and have the full voltage drop across it when turned "off" and zero voltage drop when turned "on" (Figure 1.3). In reality, the power devices have resistance in the on-state (R_{ON}) and a leakage current in the off-state. Under common biasing conditions, the voltage across it when off is limited by the off-state drain-to-source breakdown voltage (BV_{DSS}). Thus, to achieve high energy efficiency and reduce conversion losses, a low R_{ON} and a high BV_{DSS} are the most critical characteristics of power devices to achieve.

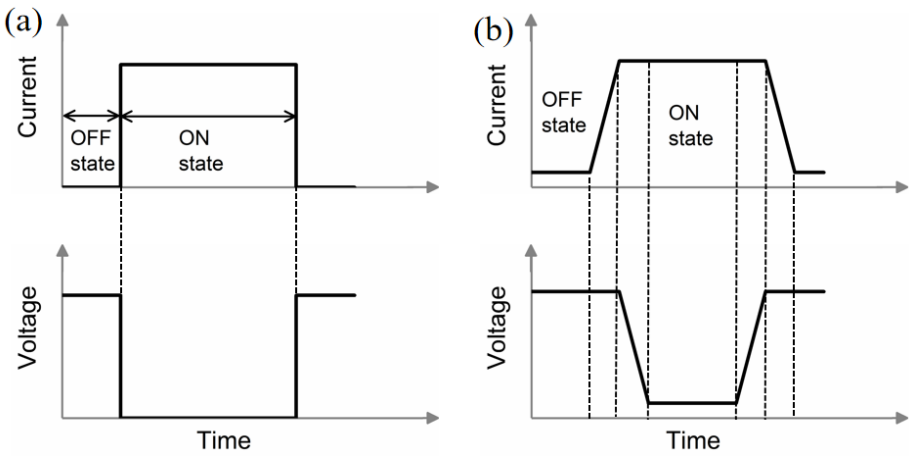


Figure 1.3 The current and voltage across (a) an ideal power switching device and (b) a power switching device in reality.

Due to the low cost and the maturity of processing, Si-based power devices, such as power metal-oxide-silicon field-effect transistors (MOSFETs) and insulated gate bipolar transistors

(IGBTs), have been the dominant transistors in power electronic systems for more than five decades. However, for certain applications that require high frequencies, high currents/voltages, or high working temperatures, Si power devices are limited by its relatively narrow energy bandgap, low thermal stability, and low thermal conductivity, resulting in lower operation currents, lower voltages, lower operation temperature ranges, and lower energy efficiencies. Moreover, the rate of improvement has slowed down as Si power devices have approached their theoretical bounds predicted by its material properties. The continuous demand for higher current/voltage and power density and the need for better energy efficiencies to reduce global energy consumption require new semiconductor technologies in power electronics to overcome the inherent limitations of Si-based devices. Wide bandgap (WBG) semiconductors, such as silicon carbide (specifically 4H-SiC) and gallium nitride (GaN), are considered the best materials for future energy-efficient power electronics [3]. GaN- and 4H-SiC-based power devices have recently become commercially available. Other WBG semiconductors, like β-Ga_2O_3 and diamond, have gained increasing interest and are still in the research stage for power electronic applications [4].

As discussed, the two most important characteristics for power devices are R_{ON} and BV_{DSS}. For power transistors, the switching losses are also impacted primarily by Q_{GD}, known as the miller charge, which controls the voltage rising and falling speed. The switching figure-of-merit is defined as $R_{ON} \times Q_{GD}$, and the lower the better [2]. Low R_{ON} and high BV_{DSS} are highly desired, which translate to low power consumptions, high operation voltages, and high currents. In power transistors, due to the finite critical breakdown electric field of the semiconductor, achieving higher BV_{DSS} requires a longer drift region, which also leads to a larger R_{ON}. Therefore, a fundamental trade-off lies between the R_{ON} and BV_{DSS} (Figure 1.4). Taking the device footprint into

consideration, the theoretical minimal specific on-resistance, defined as the product of R_{ON} and device area, is proportional to the square of BV_{DSS} in both lateral and vertical devices [5], [6]. According to this figure, with the same BV_{DSS}, GaN devices can deliver one order and three orders of magnitude lower R_{ON} than SiC and Si, respectively, owing to their superior material properties.

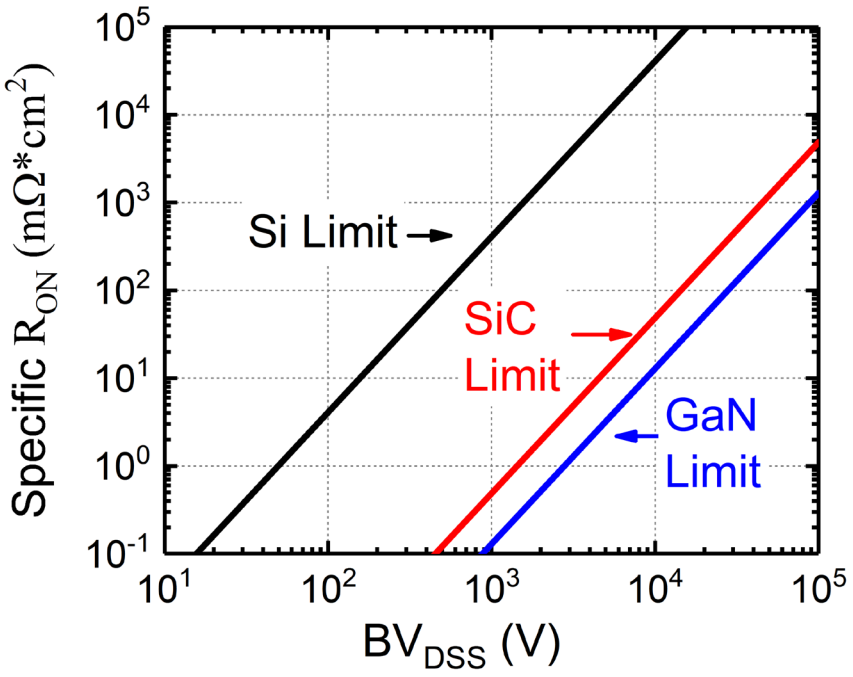


Figure 1.4 Fundamental trade-off relations between specific R_{ON} and BV_{DSS} of Si, SiC, and GaN-based power transistors.

However, in power electronics, GaN is still behind SiC in technology maturity. GaN-based high electron mobility transistors (HEMTs) are the GaN transistors employed as switching devices in high-power applications. As recently reported by several market analysts, GaN is better suited for the low-medium voltage range (200-600 V), including a large portion of the consumer electronic market (e.g., phone chargers, computer power supplies, audio amplifiers, etc.). In this voltage range, GaN is the best candidate to replace the existing Si devices. The 600-900 V voltage range is strategic; it covers the converters for electric vehicles (EVs) and hybrid EVs and inverters

for renewable energy (e.g., photovoltaic). In this voltage range, GaN devices are expected to be in competition or to coexist with SiC. According to recent reports of market analysts [7], a dramatic increase of the GaN power device market is predicted, exceeding $700M in 2025. Besides the superior material properties, presently, there exist two major technical problems for GaN HEMTs: the lack of the realization of normally-off operation and the low reliability, which were the topics of my dissertation work.

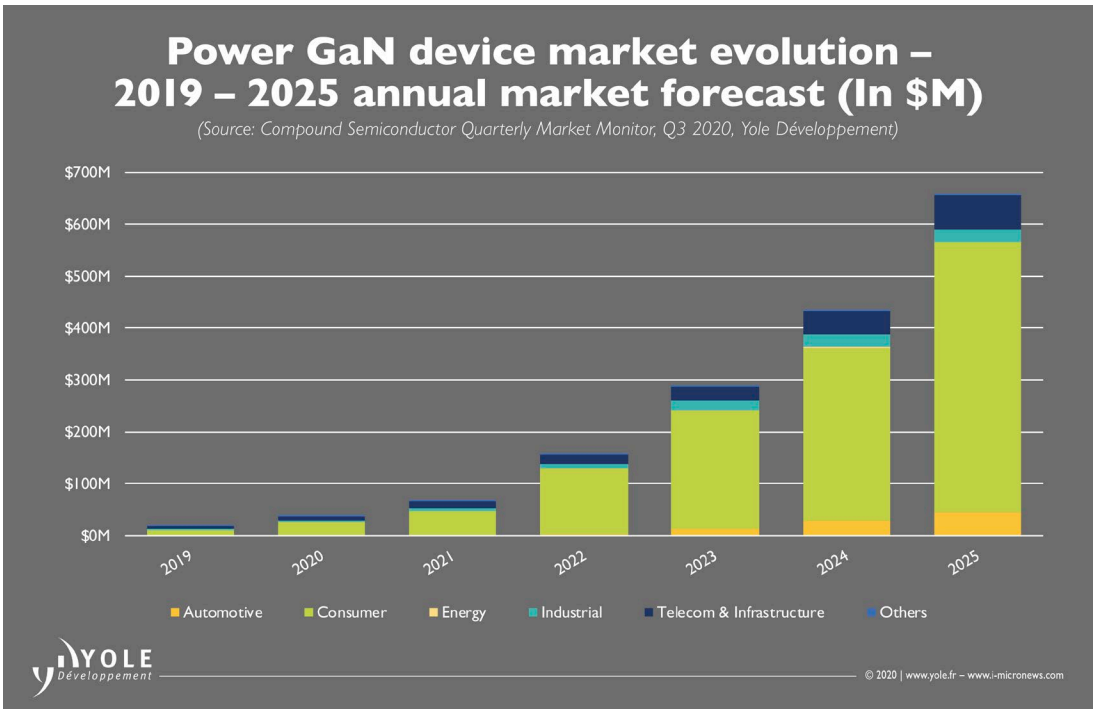


Figure 1.5 GaN power device market size prediction by Yole. Figure courtesy of Ref. [7].

1.2 Material Properties of GaN

1.2.1 Comparison of Different Semiconductor Materials

The relevant material properties of Si, GaN, and SiC, which contend for the power management market, appear in Table 1.1 and Figure 1.6.

- Energy bandgap (E_G): GaN and SiC have two to three times the bandgap of Si. The E_G of a semiconductor is related to the strength of the chemical bonds between the atoms in the lattice. A larger E_G means that it is harder to break the bonding and provide free charge carriers for current conduction, which means that the material is less conductive, and the transistors have less leakage currents and are generally more stable under high temperatures. Compared with Si, GaN and SiC have a much lower intrinsic carrier concentration (n_i). Theoretically, these materials could have a negligible leakage current of up to 500 ^oC.

- Electric breakdown field (E_{CR}): When a material is subjected to a high enough voltage, electric breakdown will occur when the electric field exceeds its E_{CR}. The trade-off between the R_{ON} and BV_{DSS} of a power device is actually related to E_{CR}. The higher E_{CR} of GaN means that GaN devices possess much higher BV_{DSS} than Si devices when their specific on-resistances are comparable.

- Electron mobility (μ) and saturated electron velocity (v_s): Electron mobility measures how fast electrons can drift under an electric field. The high mobility of GaN further reduces the R_{ON}. This allows the use of a smaller device size to achieve a given current. Saturated electron velocity is the maximum velocity that an electron attains in the presence of very high electric fields. The

higher saturated electron velocity of GaN compared to Si means that GaN devices have higher saturation on-current.

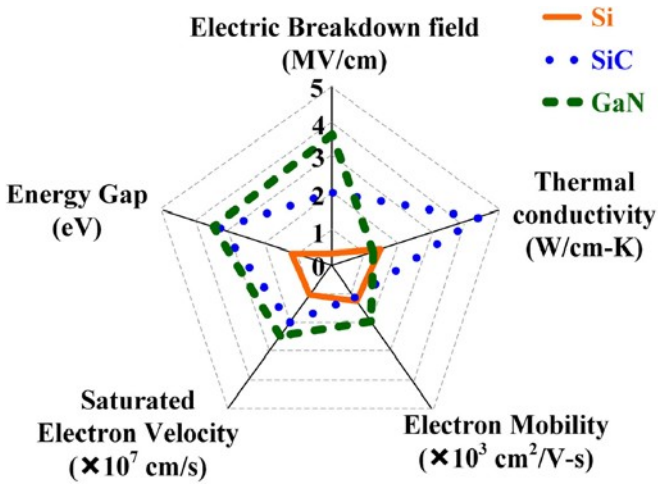


Figure 1.6 Comparison of Si, SiC, and GaN for power semiconductor applications [11], [12].

Property	Si	4H-SiC	GaN
Bandgap (eV)	1.12	3.2	3.4
Electric breakdown field E_{cr} (MV/cm)	0.25	2.1	3.6
Dielectric constant ε	11.8	9.7	9.5
Saturation velocity v_s (10^7 cm/s)	1	2	3
Electron mobility μ (cm^2/Vs)	600	800	1300 (2DEG)
Intrinsic carrier concentration n_i (cm^{-3}) at 300 K	1010	10-7	10-10
Thermal conductivity k (W/cm·K)	1.5	4.9	1.3
BFOM ($\varepsilon\mu E_{cr}^3$) normalized to Si	1	842	3175

Table 1.1 Relevant physical and electronic properties of GaN compared with Si and SiC. The BFOM for power and high-frequency electronics is normalized to Si [11], [12].

In summary, the material characteristics of SiC and GaN are better and more capable of producing transistors with lower RON, higher BVDSS, higher frequencies, higher efficiencies, and smaller sizes than Si [3], [5], [8]-[10]. Although SiC excels in high-temperature applications, the material characteristics of GaN are superior in high power and high-frequency applications.

Table 1 also includes Baliga figures of merit (BFOM) normalized to Si, which is commonly used to quantify the performance of high power and high-frequency devices [5]. The high value of the BFOM, 3175, of GaN indicates its potential advantages over Si devices in high-power and high-frequency applications.

1.2.2 Crystal Structure and Polarization of III-Nitrides

Group III and V elements can form III-V compound semiconductors such as InP, GaN and AlN. III-V semiconductors have two common crystal structures, zinc-blende and wurtzite, as shown in Figure 1.7 [3], [13]. The rock salt (NaCl) lattice structure may also be induced under very high pressures for GaN, AlN, and InN. For GaN, at room temperature, the most thermodynamically stable phase is the wurtzite structure. The wurtzite structure has a hexagonal unit cell. The hexagonal wurtzite structure of GaN has a molecular weight of 83.728 gm/mol and lattice parameters of $a = 3.1892 \pm 0.0009$ Å and $c = 5.1850 \pm 0.0005$ Å at room temperature [14].

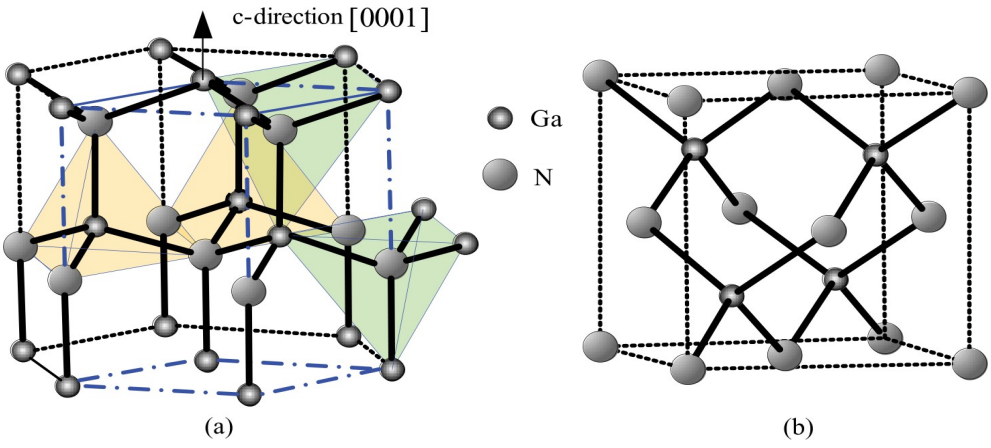


Figure 1.7 Illustration of (a) wurtzite structure and (b) zinc-blende structure [3].

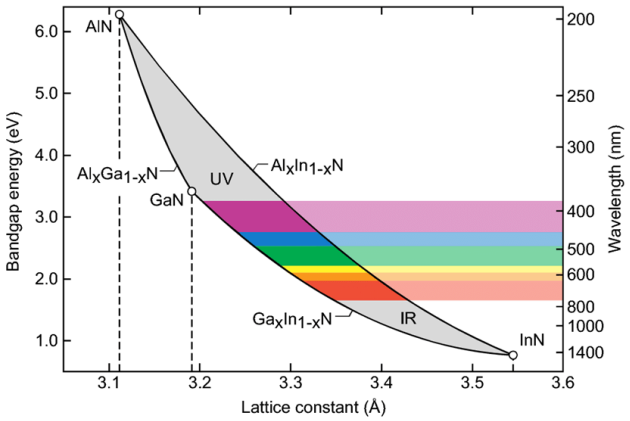


Figure 1.8 Energy bandgap in relation to the lattice constant of III-nitrides [15].

Other III-nitrides, AlN and InN, also have wurtzite structures. The lattice constants and bandgap energies of III-nitrides are compared in Figure 1.8. GaN has a bandgap energy of 3.42 eV [16], AlN has a bandgap energy of 6.13 eV [16], and InN has a bandgap energy reported in the range of 0.7-1.9 eV [17]. The large bandgap energies in GaN and AlN lead to high breakdown electric fields of 3.3 MV/cm in GaN and 11.7 MV/cm in AlN [18]. $Al_xGa_{1-x}N$ is a ternary alloy that has a bandgap energy larger than GaN, and it is commonly used as the insulating material in a GaN-based device. GaN-based devices are mostly composed of heterostructures. Besides GaN, commonly used materials in the heterostructures are AlGaN, InAlN, InGaN, and InAlGaN. The properties of these alloys, such as bandgap energies, electron/hole effective masses, and the dielectric constants, all depend on the alloy compositions. Ternary and quaternary nitride compounds form a continuous range of bandgap energies that make bandgap engineering possible.

In particular, by tuning the Al content in an AlGaN layer, it is possible to tune its bandgap: from 6.2 eV of pure AlN (100% Al) to 3.4 eV of pure GaN (0% Al). GaN, AlN, and its alloy AlGaN have different lattice constants, as shown in Figure 1.8. As discussed next in Section 1.2.3,

the lattice mismatch between GaN and AlGaN is the origin of piezoelectric polarization, when an AlGaN layer is epitaxially grown on top of a GaN crystal.

Moreover, the physical properties of group III-nitrides are influenced by the spontaneous and piezoelectric polarization ($\boldsymbol{P_{sp}}$ and $\boldsymbol{P_{pz}}$). The band structures of the heterostructures and carrier distributions are also affected. The polarization properties are essential for device applications [19].

- Spontaneous polarization $\boldsymbol{P_{sp}}$: Dipoles may form due to the asymmetry of bonding in low-symmetry compound crystals, in which the center of negative charges (electrons) is shifted away from the center of the positive charges (nuclei) [20]. Under this condition, the material will show a built-in spontaneous polarization. The polarization, defined as $\boldsymbol{P_{sp}}$, is the electric dipole moment per unit volume of the material.

For GaN, the z-axis convention is the [0001] axis. As illustrated in Figure 1.7, the polarity is defined as the Ga polarity, when the bonds along the *c*-direction range from cation (Ga) to anion (N) atoms. The direction of the bonds from Ga atoms to N atoms along the *c*-direction is defined as the +*z*-direction. As a result, due to the lack of inversion symmetry along the *c*-axis, the [0001] and $[000\bar{1}]$ directions are not equivalent. In a nitride semiconductor, the electric dipole points from the N atom to the Ga (or Al or In) atom, resulting in a negative polarization value. Polarization is a bulk property, so the polarity of the crystal is not dependent on the termination of the surface layer but is dependent only on the dipole direction [21].

- Piezoelectric polarization $\boldsymbol{P_{pz}}$: Mechanical deformation due to a lack of center of symmetry will cause piezoelectric polarization $\boldsymbol{P_{pz}}$. Highly pronounced polarization effects are observed in the group III-nitride semiconductors. The lack of inversion symmetry leads to piezoelectric effects in nitride semiconductors when strained in the <0001> direction. $\boldsymbol{P_{pz}}$ comprises two components:

the strain from a lattice mismatch and the thermal strain arising from the thermal expansion coefficient differences between the epitaxial layers and the substrate.

Spontaneous and piezoelectric polarization are the mechanisms responsible for forming the two-dimensional electron gas (2DEG) in an AlGaN/GaN heterostructure.

1.2.3 AlGaN/GaN Heterojunction and 2DEG

One of the most unique phenomena in AlGaN/GaN heterostructures is the natural formation of 2DEG, which makes them especially suitable for transistor applications. An AlGaN/GaN heterostructure is formed by epitaxially growing a thin AlGaN layer on top of a thick GaN layer, as depicted in Figure 1.9. Due to the $\boldsymbol{P_{sp}}$ and $\boldsymbol{P_{pz}}$, a 2DEG is subsequently formed at the interface between the AlGaN barrier and the GaN channel, which can be a conduction channel made of very high mobility electrons even without any n-type doping, perfect for transistors. The details are described below.

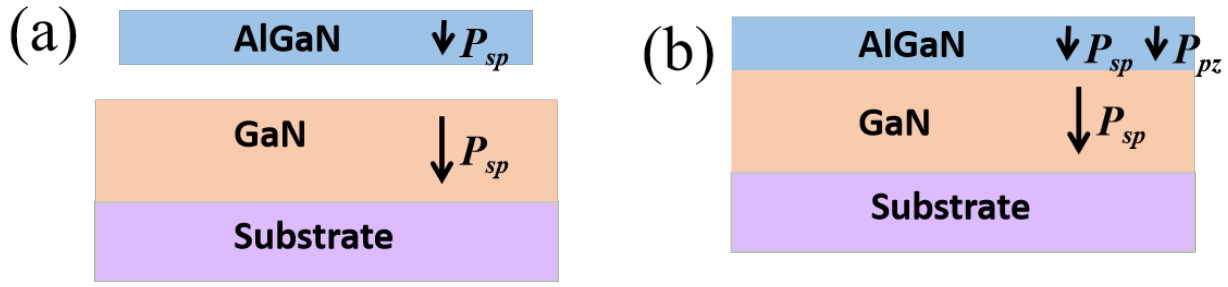


Figure 1.9 Schematic of an AlGaN/GaN heterostructure. On top of a thick GaN layer, a thin layer of AlGaN is epitaxially grown. Due to the lattice mismatch between GaN and AlGaN, a P_{pz} is added to the P_{sp}, as shown in (b).

GaN and AlGaN both present a strong $\boldsymbol{P_{sp}}$. A $\boldsymbol{P_{pz}}$ component appears in GaN, AlN, or AlGaN when the material is strained. The calculation details for $\boldsymbol{P_{sp}}$ and $\boldsymbol{P_{pz}}$ can be found in Ref.

[22]. In an AlGaN/GaN heterostructure, the piezoelectric polarization appears only in the thin AlGaN layer because it is under tensile strain, whereas the GaN layer is much thicker than the AlGaN layer and is almost fully-relaxed. If the AlGaN layer is under tensile strain, $\boldsymbol{P_{sp}}$ and $\boldsymbol{P_{pz}}$ are parallel (Figure 1.9) [23]. The explicit calculation of the $\boldsymbol{P_{sp}}$ and $\boldsymbol{P_{pz}}$ present in a generic $Al_xGa_{1-x}N$ layer when grown on top of a GaN layer is reported in Ref. [24]. The higher the Al content, the larger the $\boldsymbol{P_{pz}}$ component, caused by the larger lattice mismatch with the GaN layer. Consequently, the higher the Al content in the AlGaN layer, the larger the total polarization. A polarization charge density (ρ_p) is associated with a gradient of polarization (P) in space ($\rho_p = \nabla P$). Therefore, at the abrupt interface of AlGaN/GaN, a fixed polarization charge should be induced. Considering the case of AlGaN/GaN, fixed positive induced polarization charges appear at the interface. The positive polarization-induced charges at the interface of AlGaN/GaN attract free electrons even without any n-type doping, resulting in the formation of a 2DEG at the AlGaN/GaN interface (Figure 1.10). It is also possible to analytically calculate the 2DEG carrier density based on the polarization [25]. The results show that the 2DEG density will rapidly increase once the AlGaN thickness exceeds a certain thickness depending on the Al content (usually a few nm). The 2DEG density will gradually saturate when the thickness is 30-60 nm [25].

Although the polarization charges at the interface are fixed, the electrons of the 2DEG are free to move. In addition, due to the band discontinuity between AlGaN and GaN, electrons of the 2DEG are confined in a triangular quantum well, as schematically shown in Figure 1.10.

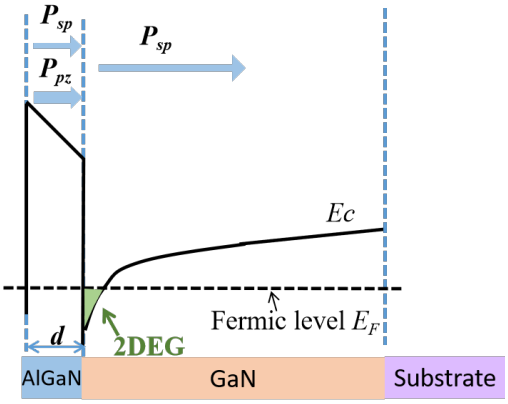


Figure 1.10 Schematic of the band diagram of a heterostructure composed of a thin strained AlGaN layer on a thick relaxed GaN.

From the discussion above, it is clear that the 2DEG density is strongly influenced by the thickness and Al content of the AlGaN barrier. Ideally, growing a thicker AlGaN barrier with a higher Al content would lead to higher 2DEG density (e.g., the extreme case of pure AlN). This would also result in a more significant bandgap discontinuity at the interface, providing better carrier confinement. However, the AlGaN barrier layer starts to relax by dislocations formation when the AlGaN barrier is beyond a critical thickness [26]. This critical thickness is a function of the Al content: the higher the Al content, the larger the lattice mismatch and the lower the critical thickness. This means that the trade-off between the Al content and the final thickness of the AlGaN barrier layer needs to be considered.

Typically, the common Al contents and thicknesses of AlGaN barrier layers are found to be within 15 to 35% and 10 to 30 nm, respectively. Nevertheless, this still results in a considerable 2DEG density (~ 10^{13} cm^{-2}). Such a high carrier density is also routinely measured in state-of-the-art AlGaN/GaN epilayers.

1.3 AlGaN/GaN HEMTs and Electrical Characteristics

1.3.1 Basic Structure of an AlGaN/GaN HEMT

As discussed above, by growing a thin strained layer of AlGaN on top of a thick relaxed GaN layer, the formation of 2DEG naturally happens at the interface. This 2DEG is highly conductive due to the confinement of the high mobility electrons in the quantum well. This confinement increases the mobility of electrons from about 1000 $cm^2/V•s$ in unstrained GaN to 1500-2000 $cm^2/V•s$ in the 2DEG region due to a reduction of surface scattering. The high concentration of electrons with a very high mobility is an ideal transistor channel for the HEMTs, the subject of this work.

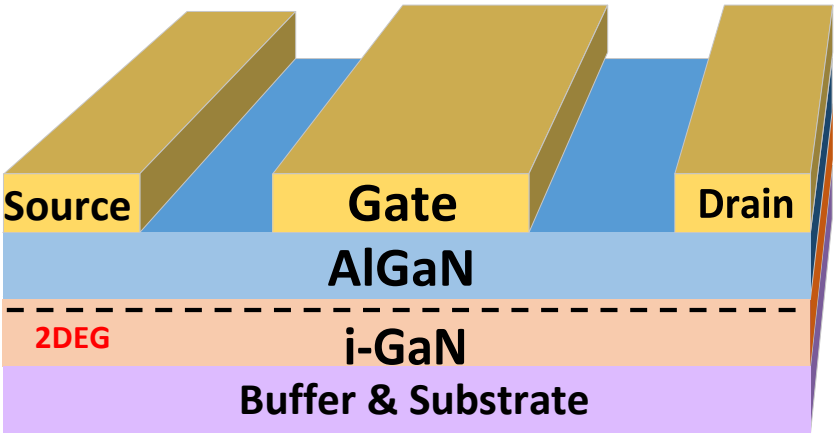


Figure 1.11 The schematic of an AlGaN/GaN HEMT. The dashed line indicates the 2DEG formed at the AlGaN/GaN interface.

A basic AlGaN/GaN HEMT structure is shown in Figure 1.11. As with any power FET, there are gate, source, and drain electrodes. The source and drain metals form ohmic contacts with the underlying 2DEG by annealing by metal spiking through the AlGaN layer (not shown in the figure as a convention in this field). The gate electrode forms a Schottky contact with the AlGaN layer without annealing, which is desirable for obtaining low gate leakage currents. The insulating

AlGaN layer isolates the gate contact from the 2DEG. Any current from the gate to the GaN substrate is considered as a leakage gate current. The AlGaN/GaN HEMT was first demonstrated in 1993 [27], where the 2DEG is present at the AlGaN/GaN interface. The channel is controlled by applying a gate voltage (V_{GS}) and thus a vertical electrical field to either deplete it or enhance it, making the channel less for the off-state or more conductive for the on-state. Later on, groups around the world have increasingly reported high-performance AlGaN/GaN HEMTs for radio frequency (RF) as well as for high-power applications [28]-[30].

As discussed, the 2DEG channel exists at an AlGaN/GaN interface when there is no gate to source voltage bias applied, i.e., V_{GS} = 0 V. This type of HEMT is called a depletion-mode (D-mode), or normally-on, HEMT. This means that an AlGaN/GaN-based HEMT is normally-on and a current between the source to the drain can readily flow. This also means that the threshold voltage (V_{TH}) of this AlGaN/GaN HEMT is less than 0 V, and a V_{GS} is required to deplete the 2DEG and turn off a HEMT. This characteristic, however, is also one of the main challenges for the state-of-the-art AlGaN/GaN HEMTs that are used in high power and high current applications [31]. It leads to many drawbacks in a practical circuit, such as high consumption, potential electrical safety risk, inherent fail-safe operation, and complicated circuit configuration [31], [32]. Therefore, the normally-off operation, or enhance-mode (E-mode) HEMT, is required, and a high and positive V_{TH} is desired.

Besides the V_{TH} requirements, for transistors to be used in power conversion circuits and systems, there are several critical electrical parameters, including off-state breakdown voltage between source and drain (BV_{DSS}) and on-resistance (R_{ON} or $R_{DS(on)}$). These key device parameters will be described in Section 1.3.2-1.3.4 below.

1.3.2 Breakdown Voltage (BV_{DSS}) and Leakage Current (I_{DSS})

A semiconductor transistor with applied biases will break down when any constituent materials' critical electric field is exceeded. A lateral electrical field exists between the source (S) and the drain (D) when a voltage is applied from D to S (V_{DS}) at off-state. The BV_{DSS} of a GaN HEMT describes the off-state breakdown voltage from D to S, which is generally a few hundreds of volts, and the larger, the better. The electrical field distribution is sensitive to the bias conditions, the geometry details, defects, and interfaces. BV_{DSS} is determined by several factors [33] including the fundamental E_{Cr} of GaN discussed in section 1.2.1; the specific design of the device such as the geometry and layout; the specifics of the heterostructure such as the Al content, the quality and thickness of the AlGaN layer; the internal insulating layers in the device structure above the gate, source, and drain electrodes; and the underlying substrate material properties.

The BV_{DSS} is evaluated by applying a positive drain bias to a source, V_{DS}, while the transistor is off with the 2DEG depleted. In an E-mode transistor ($V_{TH} > 0$), the transistor is turned off when $V_{GS} = 0 < V_{TH}$. In a D-mode device ($V_{TH} < 0$), $V_{GS} < V_{TH}$ is required to set the HEMT to the off-state.

A simple analysis, shown in Figure 1.12, illustrates the electric field magnitude distribution in a *p*-GaN gate HEMT when a high V_{DS} is applied. Higher electric fields develop near gate electrodes. When these fields, at any location in the device structure, exceed E_{Cr}, the device will break down and result in a significant increase of the current.

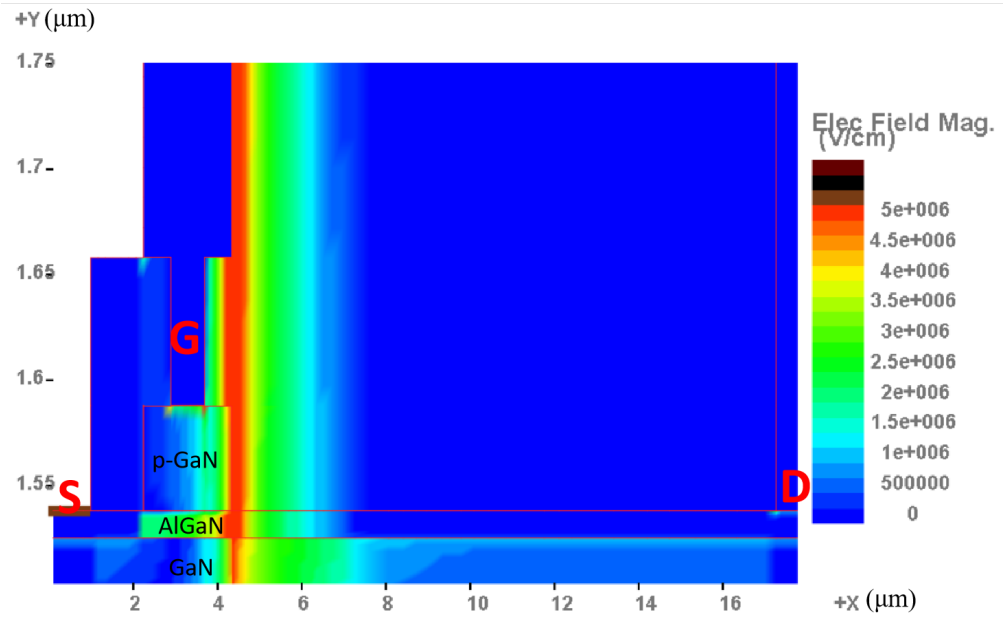


Figure 1.12 The electric field distribution of a HEMT when V_{DS} is applied at off-state.

When a transistor is turned off, there are still some small leakage currents (I_{DSS}). In an HEMT device, the leakage currents can have a few paths, such as from the drain to the source, from the drain to the gate, or from the drain to the substrate. The sum of these three leakage currents will be the total I_{DSS} in the *p*-GaN gate HEMTs in this work and in most common applications, as the G is connected to S. When designing a power conversion system, I_{DSS} can become a significant source of power loss. For example, if a 100 V device has a 100 µA I_{DSS} leakage current, the overall power dissipation due to the leakage current would be 10 mW. In applications requiring low standby powers, this amount of loss could be unacceptable.

1.3.3 On-resistance (R_{ON})

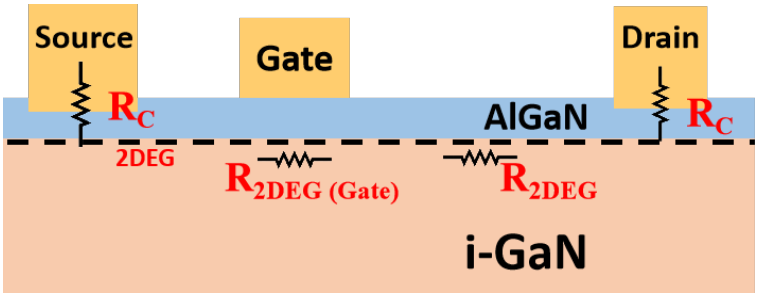


Figure 1.13 Cross-section of a HEMT, showing the major components of R_{ON}.

The R_{ON} of a transistor is the sum of all the resistance elements that are on the current flow route from the D to the S. Figure 1.13 shows the major components contributing to the R_{ON} of the device. The source and drain metals connect to the 2DEG through the AlGaN barrier by having metal spiking through this layer (not shown according to the convention in the field). This component of resistance is called the contact resistance (R_C). Electrons then flow in the 2DEG with a resistance R_{2DEG}. This resistance is determined by the mobility (μ_{2DEG}), the number of electrons (n_{2DEG}) per unit area, and the distance the electrons have to travel (L_{2DEG}). This resistance can be described with the following formula [34]:

$$R_{2DEG} = L_{2DEG} / (q\, \mu_{2DEG}\, n_{2DEG}),$$

where R_{2DEG} is normalized by the device width and are in the unit of Ω·mm. As discussed in Section 1.2.2, the number of electrons in the 2DEG depends on the AlGaN barrier when there is no vertical or lateral electric field. Under the gate electrode, the electron concentration also depends on the type of gate (recessed gate, MOS, Schottky, or *p*-GaN), the fabrication process used, and the V_{GS}. A higher V_{GS} attracts a higher electron concentration in the channel than a lower V_{GS}. Thus, the R_{ON} can be modeled as follows [35]:

$$R_{ON} = 2 \times R_C + R_{2DEG} + R_{2DEG(Gate)},$$

where all the resistances are normalized by the device width and are in the unit of Ω·mm.

1.3.4 Threshold Voltage (V_{TH})

For a transistor, the V_{TH} is the V_{GS} required to form a conducting channel underneath the gate to conduct a lateral current between S and D in the device. For a transistor that conducts currents by electrons, $V_{GS} > V_{TH}$ is needed to turn on this transistor. Therefore, if $V_{TH} < 0$, a transistor is on even when no gate bias is applied as $V_{GS} = 0\ V > V_{TH}$. This type of device is called a normally-on device, which is not desired due to a safety concern. A normally-off device has a positive V_{TH}. Therefore, a sufficient large and stable V_{TH} is highly desired.

For a GaN HEMT, the V_{TH} is when the 2DEG underneath the gate is fully depleted by the voltage generated by the gate electrode, which is the boundary line between the on- and the off-state [36], [37]. This occurs when the voltage of the gate balances the voltage generated by the piezoelectric strain on the AlGaN/GaN barrier. Hence, a HEMT with the structure illustrated in Figure 1.11 is a normally-on device, as a negative V_{GS} is required to deplete the 2DEG.

1.4 Normally-off AlGaN/GaN HEMTs

1.4.1 Techniques to Achieve Normally-off AlGaN/GaN HEMTs

As previously discussed, the unique property of the AlGaN/GaN heterostructure results in the formation of a 2DEG with a high electron density and a high electron mobility without doping, which is ideal as a transistor channel. However, normally-on devices are inconvenient in power conversion applications because a negative bias must be applied to turn them off. For the safety consideration, a normally-off, or E-mode, operation is highly desired. For this reason, both the

academic community and many industrial players (e.g., Panasonic, Infineon, GaNSystems, OnSemiconductors, STMicroelectronics) are currently trying to develop and commercialize reliable normally-off HEMTs [32].

Several different approaches have been proposed and demonstrated to obtain normally-off HEMTs. Among these methods, the *p*-GaN gate cap layer is probably the most promising one and has been successfully commercialized. The mechanism and progress of *p*-GaN gate HEMTs will be discussed in detail in the next section. This section will elaborate on three other popular structures that have been used to create enhancement-mode devices: 1) recessed gate, 2) implanted gate, and 3) cascode hybrid.

1) Normally-off HEMTs with recessed gate

The first solution proposed to realize a normally-off HEMT is the "recessed gate" approach [38], which consists of the local reduction of the AlGaN barrier layer thickness under the gate using plasma etching. This approach requires an accurate control of the AlGaN etching technology because the gate leakage current is due to a tunneling effect that is very sensitive to the barrier layer thickness and uniformity. Moreover, the damage induced by the etching process could lead to an increase in the gate leakage current and to V_{TH} non-uniformity effects [39].

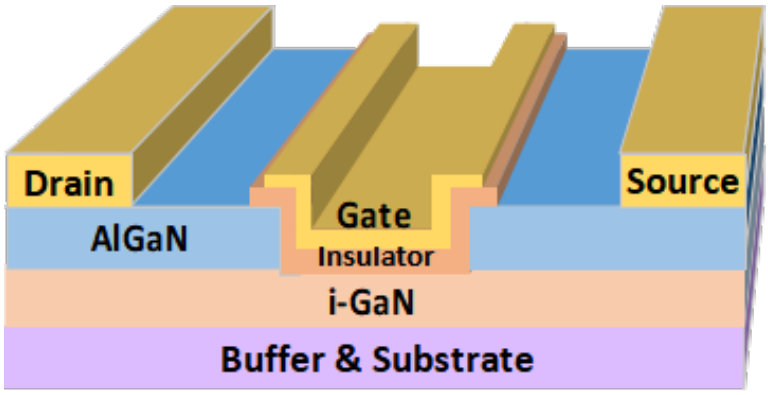


Figure 1.14 Schematic of a normally-off HEMT by a gate recess process.

Some groups have proposed combining the metal-insulator-GaN (MIS) with HEMTs to overcome the gate leakage issues (Figure 1.14). In a MIS-HEMT device, the AlGaN barrier layer is removed below the gate, forming the channel using a MIS system. This kind of MIS-HEMT is beneficial for control the V_{TH} by the recess depth, and the gate leakage current is also suppressed to a low level [40]-[42]. The selection of the insulating dielectric layer is also key for the device performance. MIS-gates explicitly affect both the channel mobility [43], [44] and the V_{TH} stability [45]. Still, the precise control of the AlGaN etching process is required in this approach. In addition, the contamination and damages induced by the etching process need to be considered as they could lead to V_{TH} reliability and instability issues.

2) Normally-off HEMTs with F^- ion implantation

To avoid the dry etching introduced by damages, an alternative approach to achieve the normally-off operation is developed. Due to its strong electron-negativity, F^- ions introduced by ion implantation in the AlGaN layers can effectively raise the electron potential in the AlGaN barrier and deplete the 2DEG channel. Thus, the V_{TH} can be modulated by F^- ions implanted during the plasma treatment. Consequently, the normally-off operation can be fabricated [46]. The method of F^- ion implantation is widely researched, owing to such merits as good repeatability and high saturation current [47]-[50]. However, the V_{TH} stability after high-temperature annealing remains a concern in these devices [51].

3) Normally-off HEMTs with a cascode circuit configuration

A normally-off GaN HEMT can also be realized by applying a “cascode” configuration, which has been previously used in Si transistors [52]. The cascode circuit is schematically shown in Figure 1.15. The terminals indicted by blank fonts are the overall G, S and D terminals of this

package. It consists of a low-voltage normally-off Si MOSFET to turns off the overall D (in black) to S (in black) path and a high-voltage normally-on GaN HEMT connected in series. The two devices are connected in such a way that the output (drain-source in blue) voltage of the MOSFET determines the input (gate-source in red) voltage of the HEMT [53]. The V_{TH} of this configuration is the V_{TH} of the Si MOSFET, which is positive.

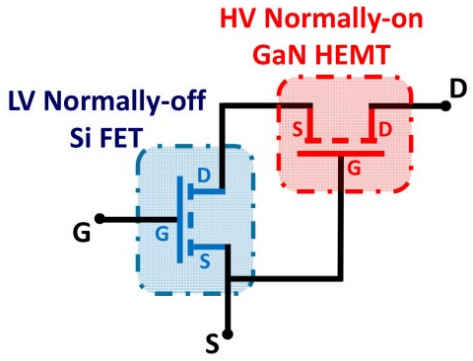


Figure 1.15 Normally-off GaN transistor package by the cascode configuration. Figure courtesy of Ref. [1].

With the cascode configuration, a positive and stable V_{TH} of the overall package can be obtained. At the same time, the system maintains the benefits provided by GaN materials or a low series resistance of the 2DEG in the on-state and a high BV_{DSS} in the off-state.

Normally-off GaN HEMTs using the cascode configuration rated at 600 V are commercially available [32], [53]. However, while the conventional MOSFET can control the cascode configuration, this solution has some drawbacks. For example, the series connection of the two devices increases the packaging complexity and introduces parasitic inductance that affects the cascode configuration's switching performance. Moreover, the high-temperature operation is limited by the presence of the Si device. Hence, the power electronics community continuously pushes toward the development of real normally-off GaN HEMT solutions instead of adopting the cascode configuration.

1.4.2 *p*-GaN Gate AlGaN/GaN HEMTs

The most promising approach to achieve normally-off operation is probably the use of a *p*-GaN (or *p*-AlGaN) layer upon the AlGaN/GaN heterostructure at the gate region, as shown in Figure 1.16 [54], [55]. In fact, it is currently the only normally-off GaN HEMT technology commercially available. This type of GaN HEMTs has received significant attention within the scientific community and the industry.

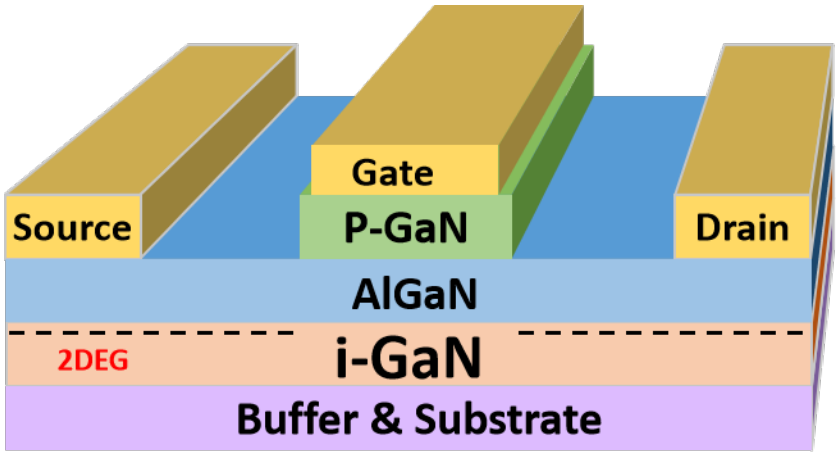


Figure 1.16 Normally-off GaN transistor with the *p*-GaN gate.

The operation principle of the *p*-GaN gate HEMT is schematically depicted in Figure 1.17. With the *p*-GaN cap layer on the AlGaN, the conduction band of the AlGaN is lifted, leading to the depletion of the 2DEG. Hence, the normally-off operation of the device can be achieved [56]. Historically, the normally-off GaN HEMT with a *p*-AlGaN gate was first proposed by Uemoto et al. [55], and it exhibited a V_{TH} of 1.0 V and a BV_{DSS} of 800 V.

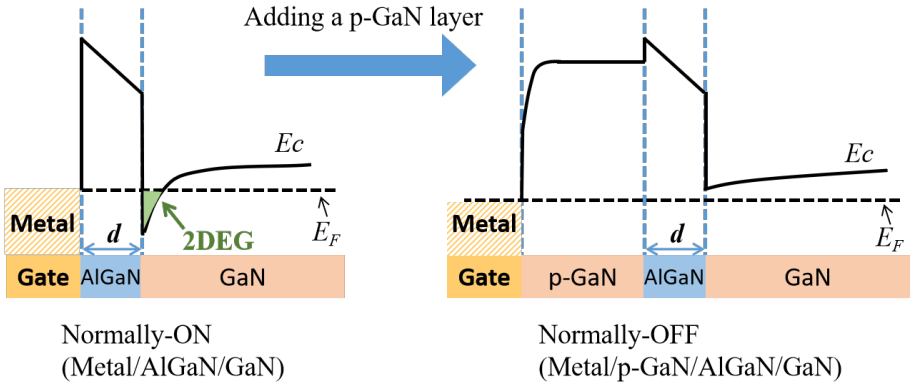


Figure 1.17 The energy band diagram of metal/AlGaN/GaN with and without a *p*-GaN gate under equilibrium.

To achieve an efficient depletion of the 2DEG and a high V_{TH}, the properties of the AlGaN/GaN heterostructure (i.e., the AlGaN barrier thickness and Al concentration) must be appropriately defined [56]-[59]. The AlGaN barrier layer thickness is typically in the range of 10-15 nm, and the Al concentration is in the range of 15-25%. A high doping level of the *p*-GaN layer ($> 10^{18}$ cm^{-3}) is typically required for the efficient depletion of 2DEG [60]. Hence, one of the key elements to increase the V_{TH} for a fixed Mg concentration of the *p*-GaN layer is to increase the Mg electrical activation [61]. However, it is difficult to obtain a high activation of Mg in *p*-GaN due to the high ionization energy (in the range 150-200 meV) of Mg as a p-type dopant, i.e., acceptor [62], [63]. An acceptor concentration of about $2\text{-}5 \times 10^{19}$ cm^{-3} is typically used, around two orders of magnitude higher than the hole concentration. A higher Mg concentration in the *p*-GaN could result in a deterioration of the crystalline quality of the layer and a subsequent decrease in the electrically active acceptors [64]. Hence, it is challenging to achieve a high V_{TH} in *p*-GaN gate HEMTs.

Another relevant aspect in the *p*-GaN gate HEMT is the choice of the gate metals. The V_{TH} and gate leakage currents are related to the metal/*p*-GaN Schottky barrier height. Several papers

in recent years have discussed the influence of metal gate work-function on the electrical behavior of *p*-GaN gate HEMTs [54], [60], [65]-[67]. Meneghini et al. showed that a WSiN- based Schottky gate, rather than a Ni/Au ohmic contact to *p*-GaN, could reduce the gate leakage current [67]. A high gate leakage in GaN HEMTs translates into continuous power consumption and heating of the gate driver. Hence, a good Schottky barrier in *p*-GaN gate HEMTs reduces the leakage current from the gate, enabling lower power consumption. For that reason, the use of a Schottky gate on *p*-GaN is currently preferred over the ohmic gate solution. Several metals have been used as Schottky gate metal contacts to *p*-GaN, including Mo-, Ni-, Ti-, TiN-based metal stacks. Greco et al. [66] demonstrated that a normally-off operation with V_{TH} = 1.5 V could be obtained with a Ti/Al metal gate. However, the structural changes at the Al/Ti/*p*-GaN interface upon thermal annealing (400-800 ^{o}C) lead to a decrease of the Schottky barrier height, which results in an increase of the leakage currents and a reduction of V_{TH}. In this sense, the thermal and electrical stability of the metal/*p*-GaN interface is an essential requirement.

The gate reliability is also an important issue in *p*-GaN gate HEMTs. Due to the relatively low gate BV (usually 10-11 V), the maximum gate operation voltages for *p*-GaN gate HEMTs are usually between 6-8 V in the commercially available products [68]. The gate BV is limited by several factors, including the epi-wafer quality, gate structure, and fabrication process. The mechanism of the gate failure is still very controversial. This maximum gate operation voltages have severely constrained the gate driver design considering the gate voltage swing. Thus, a method to increase the gate BV and enhance the gate reliability is highly desired.

In summary, although the *p*-GaN gate is by far the only practical normally-off HEMT solution that is available on the market, the technology is complex, and the device behavior can be

significantly influenced by device structures and fabrication processing conditions such as the choice of the heterostructures, the selective *p*-GaN etching processes, gate metal contacts, and thermal budgets. There are still some device and reliability issues, such as the low V_{TH}, high gate leakage currents, low gate BV, and the impact of the fabrication processes on the device performance, that require more detailed investigation [56], [67], [69].

1.5 Thesis Objectives and Outline

This work mainly focused on the investigation and realization of the high-performance *p*-GaN gate HEMTs for power electronics applications. Due to the unique characteristics of 2DEG, the AlGaN/GaN HEMTs are intrinsically normally-on. The normally-off characteristics are required for power switching applications to achieve a safe operation and a simple gate drive configuration. Among different approaches to realizing normally-off operation, the *p*-GaN gate AlGaN/GaN HEMT emerged as a leading solution. However, some important aspects of the *p*-GaN gate HEMT technology still need significant improvements in V_{TH}, gate leakage, and gate BV, which were addressed in this work. By designing novel device structures and optimizing the fabrication process, we have developed *p*-GaN gate HEMTs superior to the state-of-the-art products in V_{TH} and gate reliability. The failure mechanisms and reliability issues related to *p*-GaN gate HEMTs have also been investigated.

Chapter 2 discusses the fabrication process and characterization methods for *p*-GaN gate HEMTs in detail. A state-of-the-art *p*-GaN gate HEMT fabrication baseline was developed for the subsequent investigation. In particular, some of the critical fabrication steps, including the *p*-GaN gate etching, the source/drain metal contact formation, the passivation deposition, and the gate

metallization, are discussed comprehensively. The electrical characterizations of the *p*-GaN gate HEMTs are conducted and the key parameters are extracted.

Chapter 3 is on the testing and reliability. We proposed and validated a new novel multiple-gate-sweep-based method to thoroughly examine the gate breakdown mechanisms of *p*-GaN gate AlGaN/GaN HEMTs. Three different breakdown mechanisms have been observed and confirmed by SEM: the metal/*p*-GaN Schottky junction breakdown, the *p*-GaN/AlGaN/GaN junction breakdown, and the passivation-related breakdown. The temperature dependences of the breakdown voltages from the three breakdown mechanisms were measured and compared. In addition, we employed this analysis method for the devices with a different passivation material to show its applicability.

In Chapter 4, we investigate a new interface engineering technique to reduce gate leakage and increase gate BV, where graphene is used as an insertion layer below the gate metal stacks, which form a Au/Ti/graphene/*p*-GaN stack in the middle and a Au/Ti/graphene/SiN_x stack on the two sides. A larger I_{ON}/I_{OFF} ratio, higher $V_{TH,}$ and reduced off-state gate leakage have been achieved by the insertion of graphene. Higher gate BV has also been achieved with graphene, considered to be the result of higher Φ_B, the suppression of Ti/*p*-GaN reaction, and the better graphene/*p*-GaN interfaces.

In Chapter 5, we investigate the processing window and gate contact materials to reduce leakage currents and thus increase the gate BVs. Au/Ti/*p*-GaN Schottky diodes were shown to be highly resistive when annealed within a specific annealing window. This high-resistance junction structure is employed in *p*-GaN gate AlGaN/GaN HEMTs. The gate breakdown voltage is increased with negligible influence on the sub-threshold slope and V_{TH}.

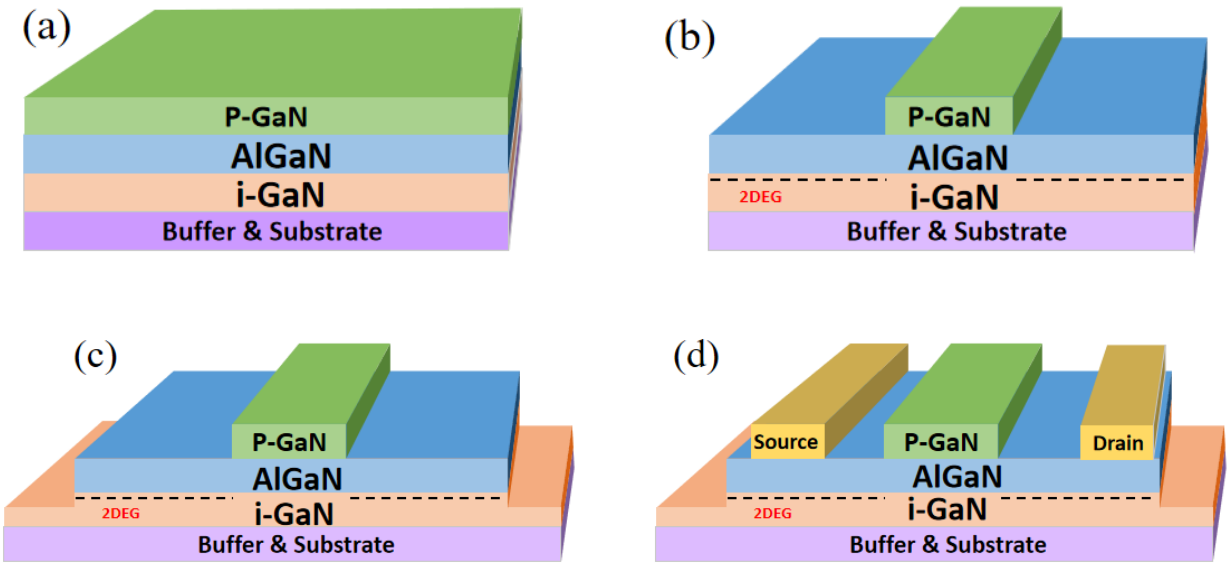
Chapter 6 presents a novel *p*-GaN gate HEMT structure with reduced hole concentration near the Schottky interface by *p*-GaN gate doping engineering, which aims to increase gate BV. By employing the additional unintentionally doped GaN layer, the gate leakage current is suppressed, and the gate breakdown voltage is boosted. Time-dependent gate breakdown measurements reveal that the maximum gate drive voltage increases significantly, effectively expanding the operating voltage margin of the *p*-GaN gate HEMTs.

Finally, Chapter 7 concludes the results achieved in this work. Potential research directions are discussed.

Chapter 2: Fabrication and Characterization of *p*-GaN Gate HEMTs

2.1 Process Flow of the *p*-GaN Gate HEMT Overview

A common *p*-GaN gate AlGaN/GaN HEMT process begins with the epitaxy growth of a series of thin films on a Si substrate. The *p*-GaN epi-wafers (Si wafers with buffer layers and top *p*-GaN/AlGaN/*i*-GaN films) used in this work are commercially available from Enkris Semiconductor Inc. China and NTT, Japan. After that, the fabrication scheme often includes a sequence of (a) wafer cleaning, (b) *p*-GaN gate defining, (c) mesa isolation, (d) ohmic metal deposition and annealing, (e) passivation deposition, (f) gate contact window opening, (g) source/drain contact window opening, (h) gate metal deposition and patterning, and (i) the second passivation deposition and contact metal deposition, as shown in Figure 2.1.



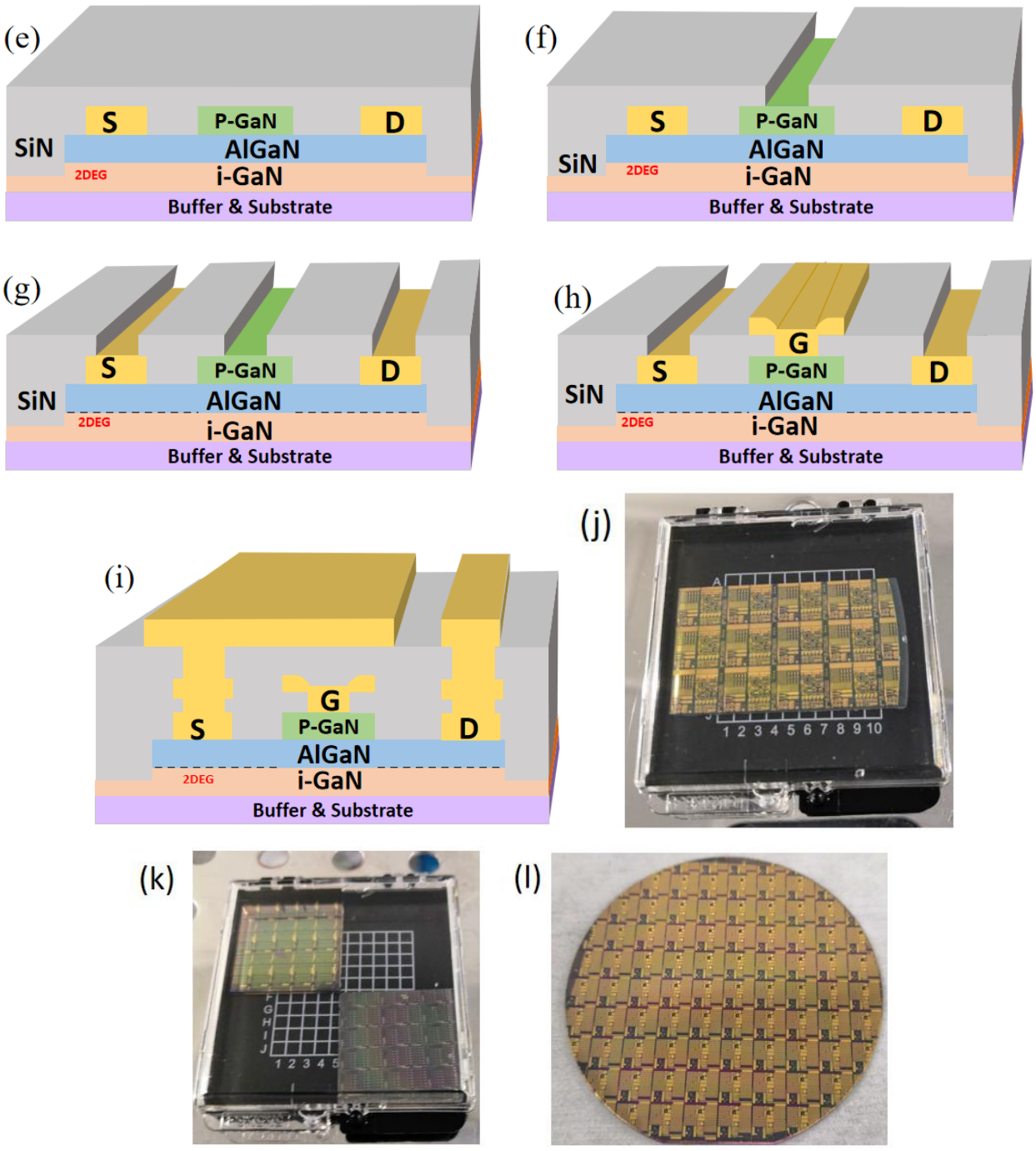


Figure 2.1 A typical fabrication process flow of *p*-GaN gate HEMTs, (a) wafer cleaning, (b) *p*-GaN gate defining, (c) mesa isolation, (d) ohmic metal deposition and annealing, (e) passivation deposition, (f) gate contact window opening, (g) source/drain contact window opening, (h) gate metal deposition, and (i) the second passivation deposition and contact metal deposition. Examples of the as-fabricated wafers appear in (j), (k) and (l).

All the fabrication and testing in this work were performed by the author at the Southern University of Science and Technology of China (SUSTech). The study and research there were conducted according to the joint-PhD program agreement between UBC and SUSTech. The fabrication process was based on standard photo-lithography and lift-off technologies. The detailed instruction of each process will be introduced below. Alignment and exposure are executed with the Karl Suss MA6 Mask Aligner in the hard-contact exposure mode. Unless specified, the photoresists used were RZJ-304 from Ruihong Electronic Chemical Co. and LOR 5A.

For photo-lithography with a single-layer photoresist, the procedure was as follows,

1) spin coat the sample with RZJ-304 at a rate of 3000 rpm for 35 sec;
2) bake it on a hot plate at 100^{o}C for 90s sec;
3) align and expose it with a mask;
4) develop it using RZX-3038 for 30 sec; and
5) rinse it with DI water and dry with nitrogen.

To pattern metals by the lift-off technology, double-layer photoresists were required. The procedure was as follows,

1) spin coat the sample with LOR-5A at a rate of 4500 rpm for 50 sec;
2) bake it on a hot plate at 170^{o}C for 7 min;
3) spin coat the sample with RZJ-304 at a rate of 3000 rpm for 35 sec;
4) bake it on a hot plate at 100^{o}C for 90s sec;
5) align and expose it with a mask;
6) develop it using RZX-3038 for 80 sec;
7) rinse it with DI water and dry with nitrogen;

8) metal deposition by e-beam evaporation or sputtering;

9) soak it with DMSO at 85°C for 30 min; and

10) rinse it with IPA and DI water and dry with nitrogen.

2.1.1 Epitaxial GaN Wafers and Wafer Cleaning

Unless otherwise specified, the *p*-GaN gate HEMTs were fabricated on 100 nm *p*-GaN/15 nm $Al_{0.2}Ga_{0.8}N$/0.7 nm AlN/4.5 µm GaN epi-structure grown on 6-inch Si (111) substrates by metal-organic chemical vapor deposition (MOCVD), as shown in Figure 2.2. There is a 0.7 nm AlN layer between the GaN and AlGaN layer to increase the electron concentration, which is often omitted in our schematics and literature schematics for simplicity. The *p*-GaN layer was doped with Mg to a concentration of 4×10^{19} cm^{-3}.

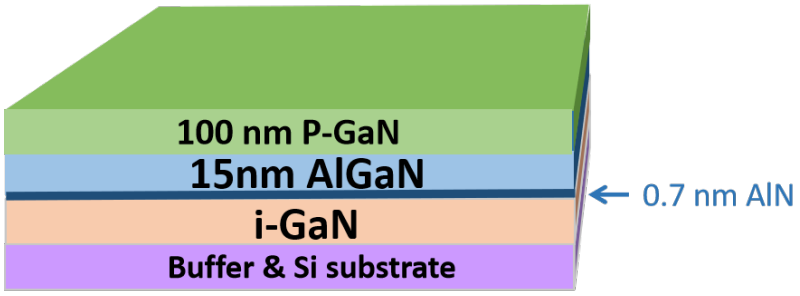


Figure 2.2 The epitaxial structure of *p*-GaN wafers used in the experiments.

The 6-inch wafers were first coated with a photoresist for protection, then diced into smaller pieces (typically 2.5 cm × 2.5 cm). After being cleaned with acetone, the wafers were immersed in a SPM solution (H_2SO_4: H_2O_2 = 4: 1, volume ratio) and heated at 90°C for 10 min, cleaned with deionized (DI) water, and blow-dried using a nitrogen gun to clean any organic residuals.

2.1.2 *p*-GaN Gate Definition

The *p*-GaN gate definition played a critical role during the *p*-GaN gate HEMTs fabrication. In this step, the *p*-GaN layer had to be selectively removed from the access regions by dry etching in an inductively coupled plasma (ICP) system and was left only in the gate regions, as shown in Figure 2.3.

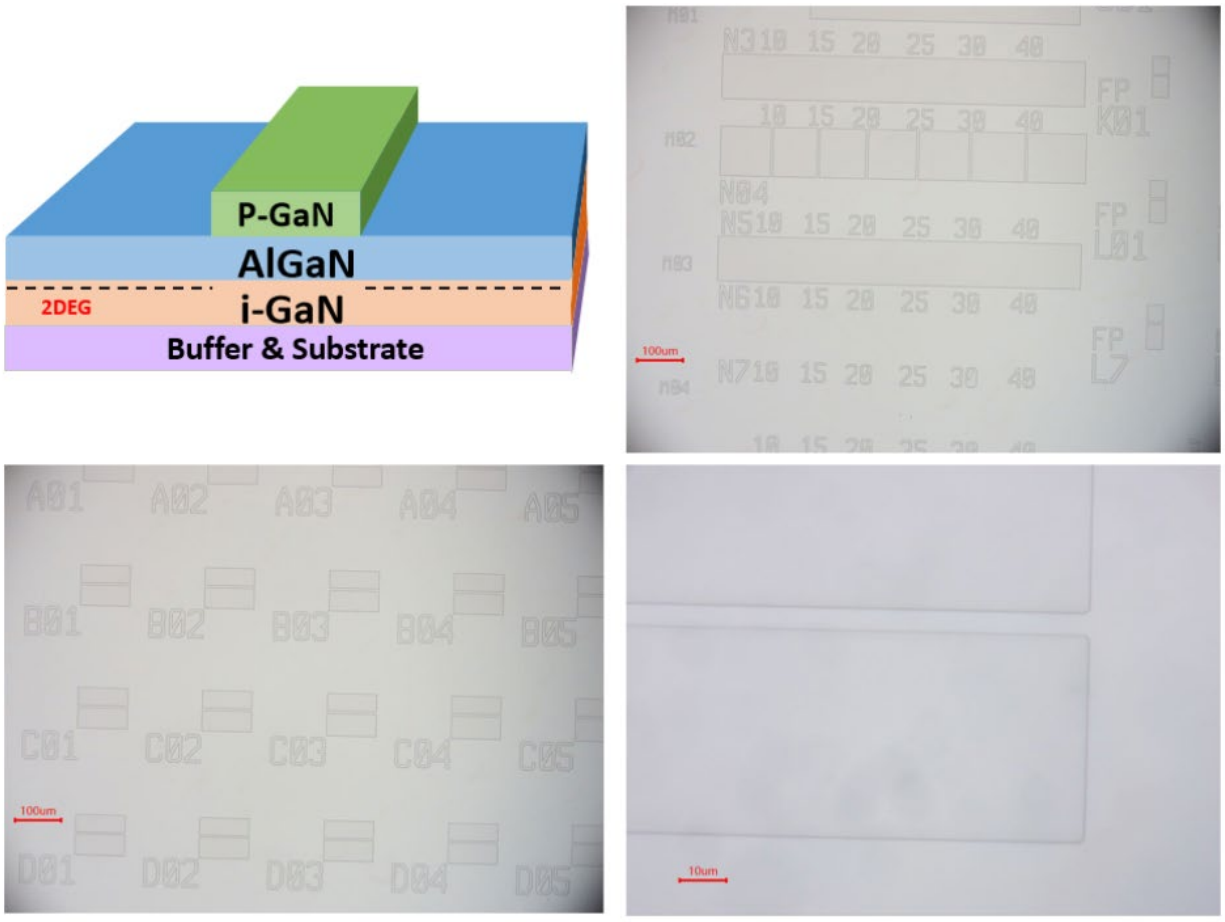


Figure 2.3 Schematic and microscopic view of the devices after the *p*-GaN gate definition.

For this step, several requirements had to be fulfilled, including a smooth surface morphology, low damages towards the AlGaN layer, and a controlled etching rate. As the thickness of the AlGaN layer was only 15 nm, even 2-3 nm over-etching of AlGaN could significantly

degrade the electron density and mobility in the 2DEG channel, leading to an increase of R_{ON}. Meanwhile, any residual of *p*-GaN in the access regions would also cause an increase in gate leakage current and shift the V_{TH} [70]. Hence, the etching rate needed to be accurately controlled. In order to avoid the degradation of the AlGaN surface, having a good selectivity of the *p*-GaN over the AlGaN was also extremely important. The high selectivity can also help to achieve a smooth surface of the AlGaN.

Etching results depend on various parameters, such as the gas chemistry and the ICP/bias power. In our experiments, a Corial 210IL ICP-RIE etching system was used. GaN dry etching is usually based on chlorine (Cl_2) as the main etching agent. Due to the higher binding energy of AlN (11.5 eV) in comparison with GaN (8.9 eV) [71], the affinity of oxygen to Al is higher compared to GaN [72]; the volatility of $AlCl_x$ complexes is lower than $GaCl_x$ complexes [73], [74]. Hence, a selectivity of GaN etching over the AlGaN is expected when using the Cl_2/O_2 gas. It has been demonstrated that the introduction of small amounts of O_2 into Cl_2-based dry etches improves the selectivity through the formation of an etch-resistant layer on the AlGaN surface [75], [76]. Given that the etching rate increases as the ICP/bias power of the process increase, the ICP/bias power must be reduced to allow better control of the etching depth. Meanwhile, the etching rate should not be too slow. Otherwise, the etching time will be unreasonably long. Thus, an etching rate between 0.1-1 nm/sec for GaN is favored. To ensure total removal of *p*-GaN on top of AlGaN, usually a 120% etching time normalized to the nominal etch time was adopted, considering the variations of the epitaxial-layer thickness and the etching rate. Other parameters that can influence the etching results include the chamber pressure and the etching mask. An inappropriate chamber pressure or etching mask can result in an undesired etching profile (e.g., a rough *p*-GaN sidewall

[Figure 2.4(a)] and a faster etching rate at the *p*-GaN gate foot corner removing too much AlGaN [Figure 2.4(b)]).

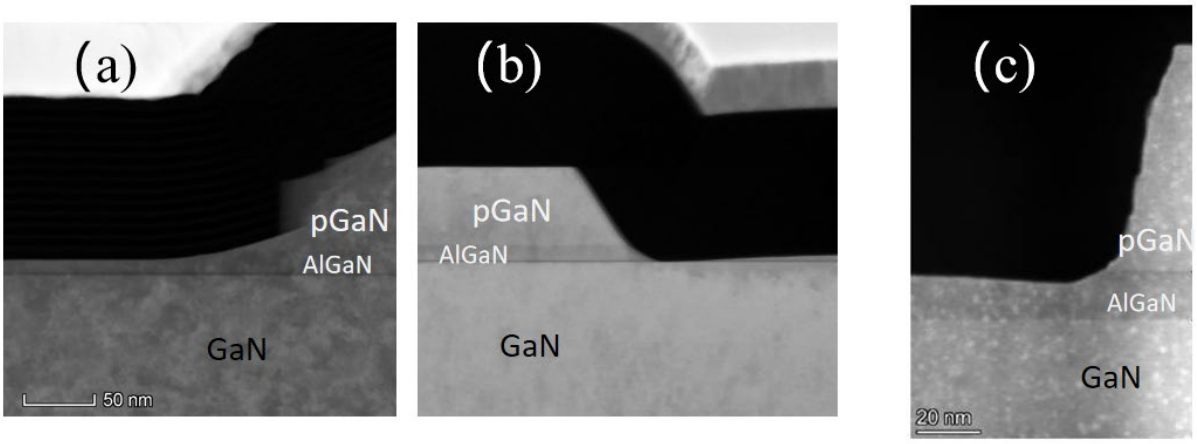


Figure 2.4 Different *p*-GaN gate etching results with different recipes characterized by transmission electron microscope (TEM): (a) undesired results with a rough *p*-GaN sidewall; (b) undesired results with corner etching; and (c) optimal etching results.

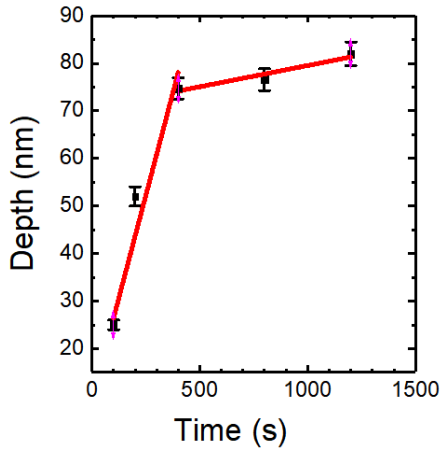


Figure 2.5 AFM measurement results of the step height as a function of the etching time, which were used to measure the etching rate of *p*-GaN and AlGaN.

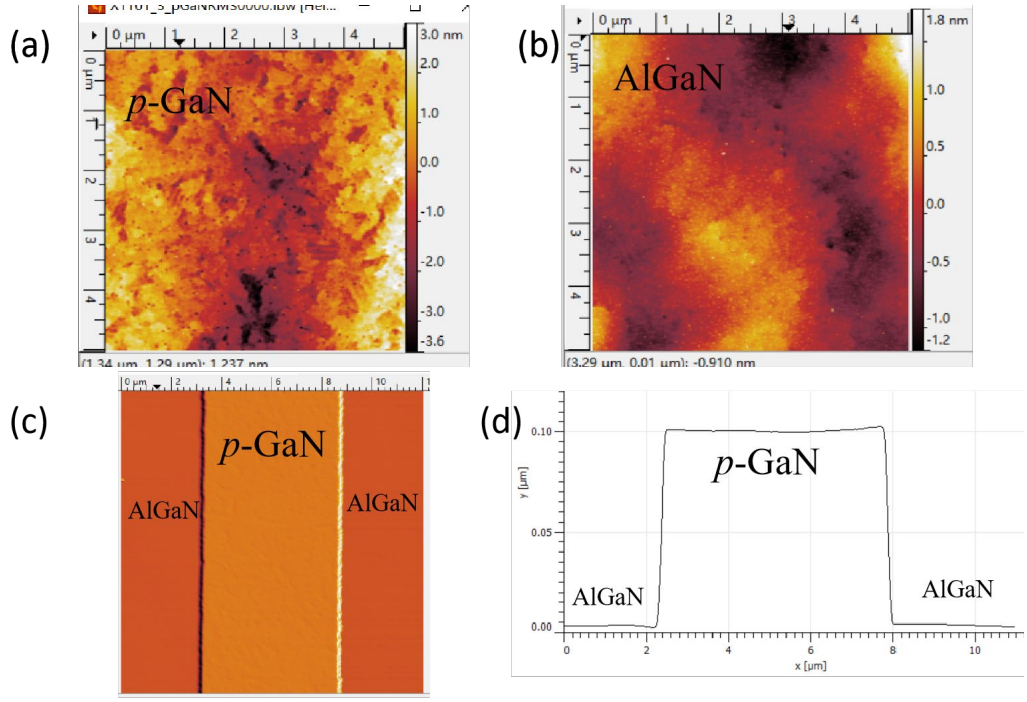


Figure 2.6 AFM characterization of (a) the as-grown *p*-GaN surface; (b) AlGaN surface after *p*-GaN gate definition; (c) the *p*-GaN gate; and (d) the extracted height profile from (c).

Figure 2.4(c) shows that our optimal etching recipe selectively removed the *p*-GaN on the AlGaN, which was characterized by TEM. A low damage recipe with ICP/bias power of 200/20 W was adopted, with the $Cl_2/N_2/O_2$ etching gas at a flow rate of 40/10/2 standard cubic centimeters per minute (sccm) and a chamber pressure of 10 mTorr. The low bias power increases the selectivity of the *p*-GaN etching over AlGaN. The relatively high ICP power is to ensure a reasonable and stable etching of *p*-GaN with enough plasma. The N_2 gas was adopted to improve the uniformity of etching. The selectivity values were also measured with different gas flow rates, and this recipe has the highest selectivity value. A low average etching rate of approximately 0.25 nm/sec was measured by an atomic force microscope (AFM), leading to accurate control of the *p*-GaN etching. To measure the etching rate of AlGaN, a 200% normalized etching time was also adopted on a test sample. As shown in Figure 2.5, the etching depth of AlGaN was smaller than 4

nm, meaning that the etching rate of AlGaN was lower than 0.01 nm/sec and the selectivity of GaN over AlGaN was higher than 25: 1. Thanks to the high selectivity, the morphology of the AlGaN surface observed after the *p*-GaN removal exhibited a root mean square roughness (RMS) of 0.41 nm, even better than the as-grown *p*-GaN surface RMS of 1.1 nm, as shown in Figure 2.6(a) and (b). The profile of the *p*-GaN gate was also well defined with a smooth sidewall and boundary, as shown in Figure 2.6(c) and 2.6(d).

2.1.3 Mesa Isolation

The mesa isolation step is used to isolate individual devices from each other through ICP dry etching, as shown in Figure 2.7. By etching through the AlGaN layer and to a depth in the GaN layer, active regions of the devices were defined and the leakage currents between the devices were minimized.

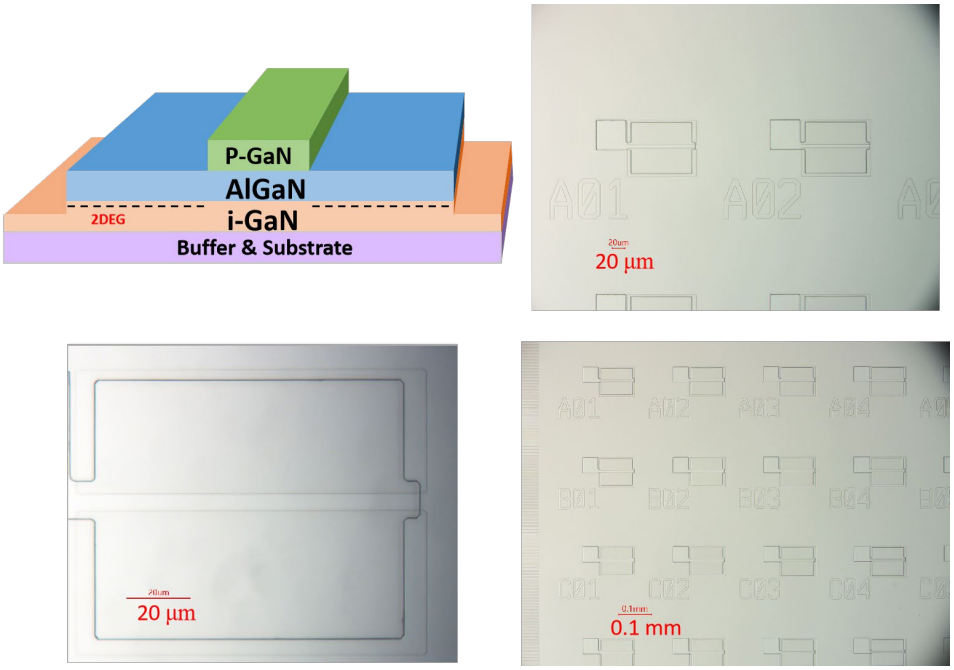


Figure 2.7 Schematic and microscopic view of the device structures after the mesa isolation.

Mesa etching was done with a Naura ICP-GSE200Plus system using a $Cl_2/BCl_3/Ar$ gas mixture with a flow rate of 50/10/10 sccm. The ICP/bias power was 100/20 W, and the chamber pressure was 10 mTorr. According to the calibration of the test samples measured by AFM, the etching rate for AlGaN or GaN was 1.1 nm/s. The samples were etched for 300 seconds to obtain a mesa depth greater than 300 nm.

After the device isolation by dry etching, surface treatment was first done by immersing the wafers in a HNO_3/HF solution for 10 min to clean the possible contaminations off the etched surface. Afterward, rapid thermal annealing was carried out at 500°C in N_2 ambient for 5 min to reduce the defect density induced by the dry etching [75].

2.1.4 Source/Drain Metal Contact Formation

The purpose of the source/drain metal contact formation step was to form good ohmic contacts between the source/drain metals and the 2DEG. A low resistance is highly desired. As shown in Figure 2.8, the ohmic contacts for the AlGaN/GaN heterostructures usually adopted the Ti/Al/*x*/Au metal stacks deposited on the AlGaN surfaces followed by high-temperature annealing, where *x* might be Ti, Ni, Pt, Mo, or Pd [77]. Please note that in the schematics below, the metal stacks are separated from *i*-GaN by AlGaN, which is non-conducting. In reality, the metals form spikes through AlGaN to connect with the conducting 2DEG. The metal spikes are usually not shown as a convention in this field [78].

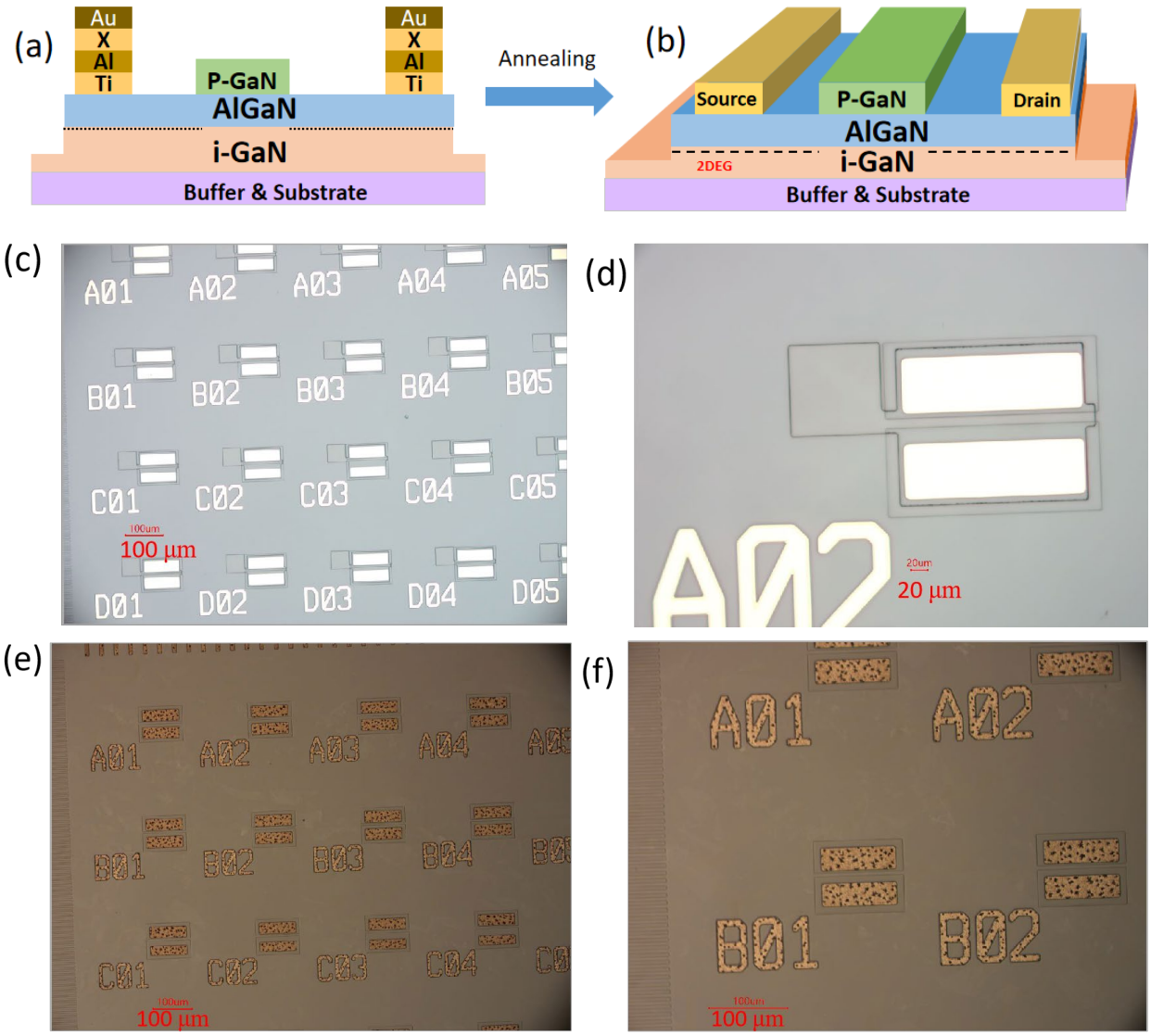


Figure 2.8 Schematics of the device structures with the source/drain metals formation (a) before and (b) after annealing. Microscopic view of the device structures (c) (d) before and (e) (f) after annealing.

Each one of the Ti/Al/*x*/Au layers plays an essential role in the ohmic contact formation. Ohmic contacts to n-type semiconductors are usually favored with a low work function, such as Ti (4.33 eV [79]) and Al (4.28 eV [79]). Besides being a low work function metal, Ti is also highly reactive with GaN upon annealing, and it can form TiN compounds at the interface, making the contacts stable. N vacancies are formed in AlGaN. Those vacancies are also beneficial for the

ohmic contacts since they act as donors and increase the net carriers' concentration below the interface [77]. However, a single Ti metal layer is unsuitable for forming low resistance ohmic contacts to AlGaN/GaN, as the use of Ti alone can also lead to the formation of voids at the interface upon annealing, resulting in a bad mechanical contact [80]. Hence, the preferred alternative metal contacts use Ti/Al bilayers, where the top Al layer allows the formation of stable phases with the underlying Ti layer upon annealing. Although a low contact resistance can be obtained after the annealing of Ti/Al bilayers [81], the oxygen contamination during annealing can cause an increase in the resistance of these metals. Moreover, the upper Al layer tends to ball up during annealing, increasing the roughness of the contact surface [82]. Hence, another metal layer, or the cap layer, is needed to act as a protective layer to minimize the oxidation of the underlying metals, and gold (Au) is commonly used. Due to the ease diffusion of Au, a barrier layer (the third layer counting from the bottom) is generally required to stabilize the multilayers during annealing, limiting the inter-diffusion of the first two metal layers with the upper fourth layer. Thus, the third layer usually has a high melting point (> 1400^{o}C), where Ti, Ni, Pt, Mo, or Pd can be applied. In summary, the Ti/Al/*x*/Au (*x*= Ni, Ti, Ta, Mo, Pt . . .) multilayers scheme is commonly used in ohmic contact formation with AlGaN/GaN. The thicknesses of each layer are usually in the range of 15-30 nm, 60-200 nm, 35-60 nm, and 50-100 nm, respectively [77]. After the metal deposition, a high-temperature annealing step, generally higher than 800^{o}C, is required to achieve the ohmic contact.

In our experiment, Ti/Al/Ti/Au (20/110/40/50 nm) was adopted as the ohmic electrode deposited by an HHV-TF500 e-beam evaporation system. A standard lift-off technology was

implemented with double-layer photoresists. The annealing process was carried out at 830 ºC for 45 sec in an N_2 ambient using a rapid thermal process (RTP) by an Annealsys AS-one 150 system.

The contact resistance (R_C) between the S/D metals and the 2DEG and the sheet resistance (R_{SH}) of the 2DEG can be extracted by the transmission line model (TLM) or the circle transmission line model (CTLM), as illustrated in Figure 2.9. Figure 2.9(b) shows that the TLM test structure consists of more than three contacts [83]. From this linear TLM structure, R_C and R_{SH} can be determined based on the linear relationship between the resistance and the gap spacing between the contacts, where the intercept yields R_C and the slope yields R_{SH}.

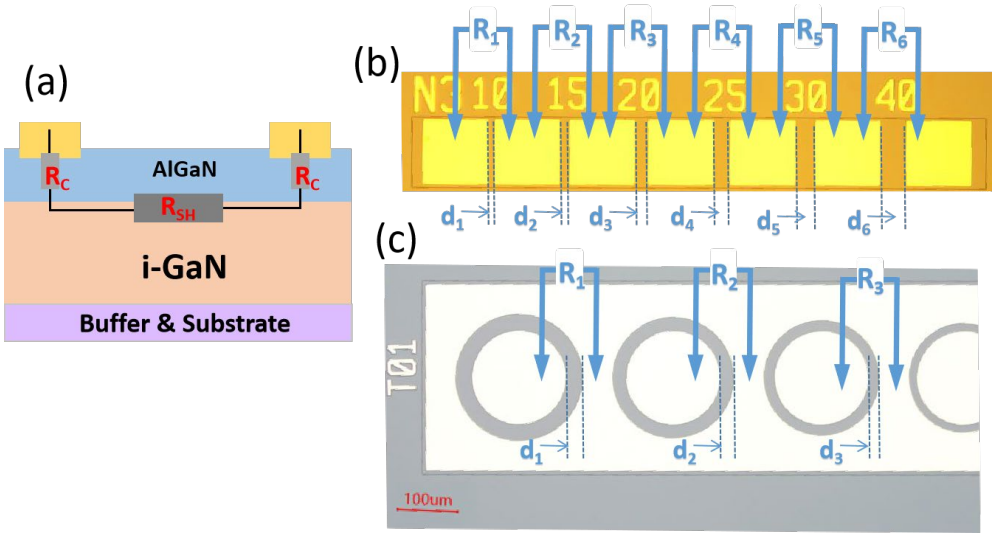


Figure 2.9 (a) Illustration of R_C and R_{SH}; (b) Planar view of as-fabricated TLM test structure; (c) Planar view of as-fabricated CTLM test structure.

However, the linear TLM technique tends to suffer from the spreading of currents from one contact to another due to current crowding at the metal corners [83]. Hence, the CTLM test structure has been developed to overcome the problem. This structure consists of some circular contacts in a large metal pad separated by ring-shaped gaps, as shown in Figure 2.9(c). In our

experiments, the radius of the circular (r_1) was fixed to 80 μm. The gap varied from 5 to 30 μm, with 5 μm per step. The measured resistance increases with larger gap spacing, yielding six different resistance values. For each measured resistance, there was a correlation factor *c*. Plotting *R/c* as a function of the gap spacing yields a typical result, as shown in Figure 2.10. From the linear fit, the intercept with the y-axis and the slope could be obtained. The intercept was $2R_C/2\pi r_1$, and the slope was $R_{SH}/2\pi r_1$. Thus, the R_C between metals and the 2DEG and the R_{SH} of the 2DEG could be extracted.

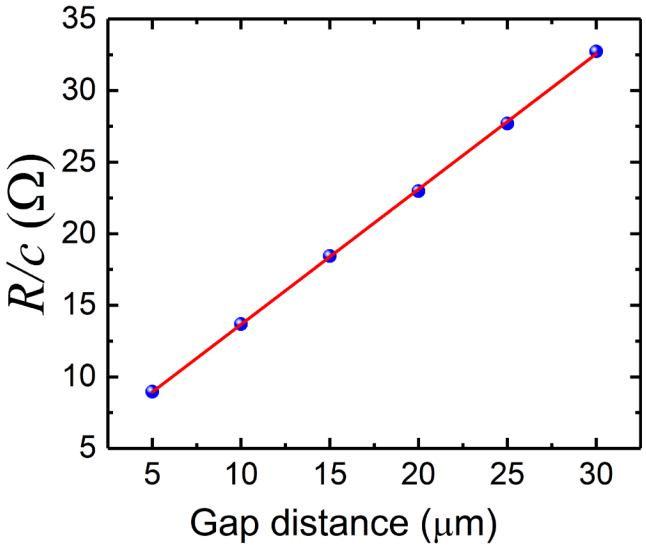


Figure 2.10 Measured resistance with the correction factors applied versus the gap spacing. From the linear fit, R_C was determined to be 0.58 Ω·mm and R_{SH} was determined to be 618.3 Ω/square.

To get the optimized thermal budget, the author tested five different thermal budgets on test wafers with the fixed Ti/Al/Ti/Au thicknesses (20/110/40/50 nm), including 810 ºC 30 sec, 810 ºC 45 sec, 830 ºC 30 sec, 830 ºC 45 sec, and 860 ºC 45 sec, as shown in Figure 2.11. A lower R_C could be achieved at a higher annealing temperature. However, the high temperature can be deteriorated to the 2DEG, leading to an increase of R_{SH} (e.g., 860 ºC 45 sec). Considering that low

R_C and R_{SH} are both required for the HEMTs, the 830 ºC 45 sec annealing condition was chosen as the S/D metal annealing condition in the GaN HEMT fabrication baseline.

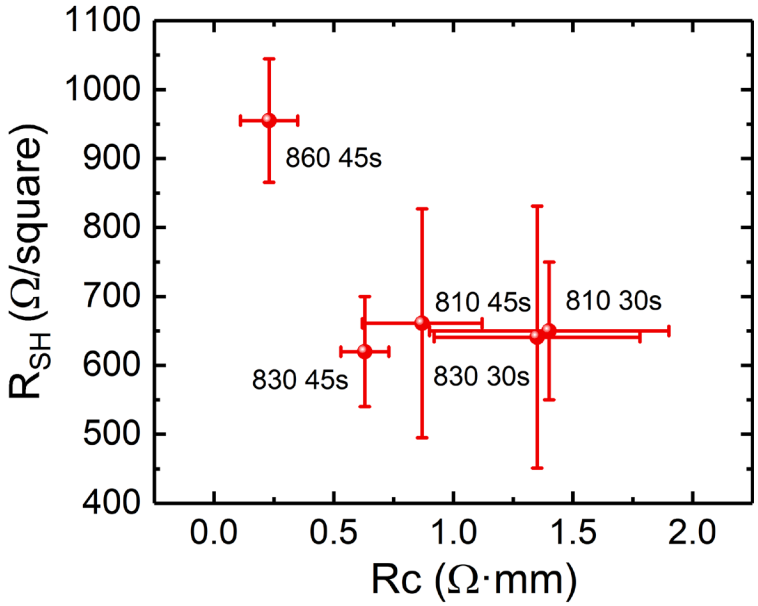


Figure 2.11 The R_C and R_{SH} extracted by the CTLM test structures after different annealing conditions.

2.1.5 Passivation Deposition and Etching

During the passivation step, dielectric films were deposited on the wafers to protect the access regions, as shown in Figure 2.12(a). The dielectric films commonly employed include SiN_x, SiO_2, AlN, and Al_2O_3. After this blanket film deposition step, the dielectric in the gate and source/drain region had to be cleaned to have gate metals deposited and make connections to the contact metals, as shown in Figure 2.12(b).

The surface passivation scheme is necessary for the operation stability and reliability of GaN HEMTs. Green et al. first reported noteworthy passivation effects on the performance of AlGaN/GaN HEMTs using PECVD SiN_x [84]. Owing to the suppression of current collapse, a

significant improvement of microwave output power has been achieved. Nitrogen radicals generated during the PECVD process control the formation of surface defects [85], leading to low-density electronic states at the SiN_x/AlGaN interface.

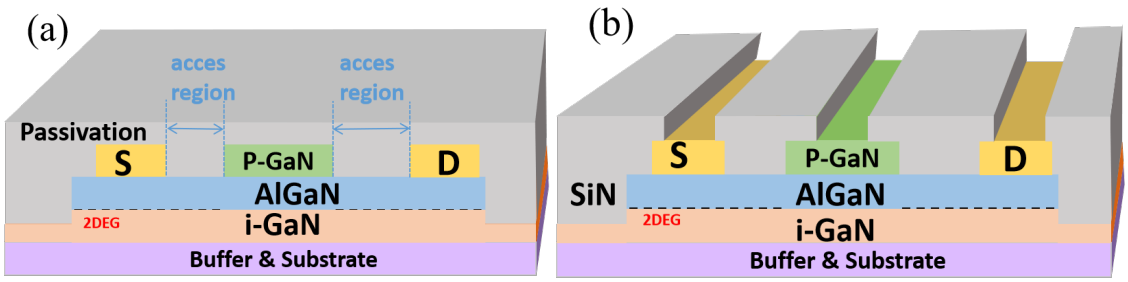


Figure 2.12 Schematic of (a) the passivation deposition step and; (b) the passivation etching step.

In this study, the SiN_x passivation layer was deposited using an Oxford PlasmaPro 80 plasma-enhanced chemical vapor deposition (PECVD) System. The SiN_x was deposited using silane (SiH_4), ammonia (NH_3), and nitrogen (N_2) as the source gases. The SiN_x film properties depend on a variety of parameters, including the bias power, the gas flow rate, and the chamber pressure. Since the SiN_x properties have a dramatic impact on the stress distribution and surface defects originated from dangling bonds and traps of AlGaN surface [86], the SiN_x deposition recipe has a significant influence on the device's electrical properties, including the V_{TH}, I_{ON}/I_{OFF} ratio, and gate leakage current.

Different passivation deposition recipes have been tested, as shown in Figure 2.13. Recipe 1 and 2 have low I_{ON}/I_{OFF} ratios due to the large off-state leakage current via the surface defects caused by the strong ion bombardment in PECVD. Hence, the deposition frequency was adjusted to lower the ion bombardment in recipe 3 and 4. Recipe 3 and 4 have different gas flow rates. Figure 2.13 shows that the device with recipe 3 has a higher V_{TH} and lower gate leakage current

compared to recipe 4. Considering that a high V_{TH}, a high I_{ON}/I_{OFF} ratio, and a low gate leakage current are desired for *p*-GaN gate HEMTs, recipe 3 was selected for the baseline processing. The processing parameters appear in Table 2.1. The thickness of the SiN_x is estimated to be 150 ± 5 nm.

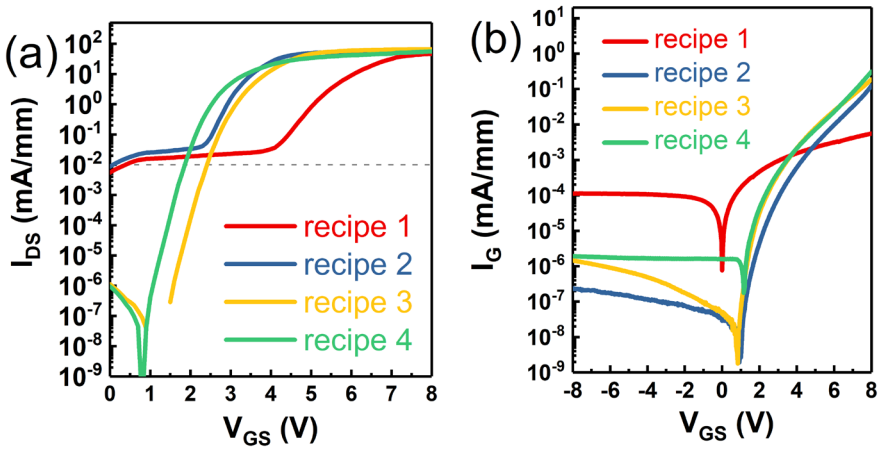


Figure 2.13 Comparison of the electrical performance of the *p*-GaN HEMTs with different passivation recipes: (a) transfer characteristics and (b) gate leakage characteristics.

Frequency (MHz)	Bias Power (W)	Gas Flow Rates $SiH_4/NH_3/N_2$ (sccm)	Chamber Pressure (mTorr)	Deposition Time (sec)	Deposition Rate (nm/sec)
13.56	25	6/4.5/700	5	281	0.533

Table 2.1 The parameters of passivation SiN_x deposition recipe 3 for the baseline processing.

After the SiN_x deposition, the dielectric in the region of the gate and source/drain had to be removed to deposit metal contacts for these three terminals. The dielectric etching was done using a Corial 210IL ICP-RIE etching system using SF_6 and Ar gases. Similar to the *p*-GaN etching step, the SiN_x etching step always requires a smooth surface morphology, low damages to *p*-GaN, and a controlled etching rate. As shown in Figure 2.14, an inappropriate SiN_x etching recipe could

bring in more surface traps on the *p*-GaN gate due to the ion bombardment, increasing the gate leakage current. The process parameters for the baseline processing appear in Table 2.2.

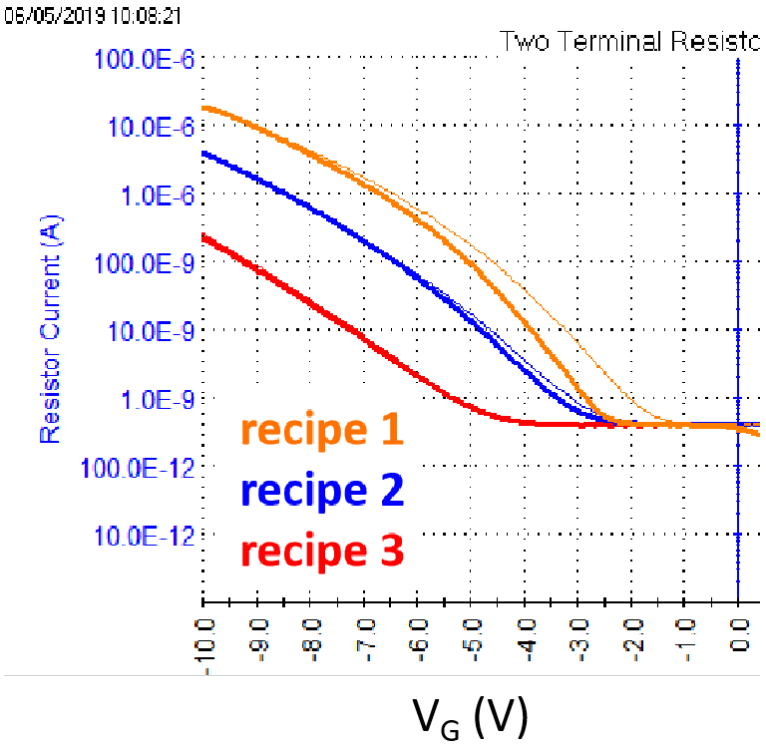


Figure 2.14 Comparison of the gate leakage currents with different SiN_x etching recipes.

ICP power (W)	Bias power (W)	Gas flow rates SF_6/Ar (sccm)	Chamber pressure (mTorr)	Etching Rate (nm/sec)
0	50	25/5	10	0.90

Table 2.2 The parameters of the SiN_x etching recipe for the baseline processing.

2.1.6 Gate Metal Deposition

The metallization for the *p*-GaN gate also plays a critical role, which can form either ohmic contact or Schottky contact. In an ohmic contact structure, where a high work function metal (e.g., Ni, Pd) is typically employed, the gate metal forms an ohmic contact with the *p*-GaN gate after certain temperature annealing. Due to the injection of holes toward the channel, the *p*-GaN gate

HEMTs with ohmic contact gates are also called gate injection transistors (GITs) [55]. Benefiting from the low barrier heights between the metals and *p*-GaN, the GITs usually have exceptionally low sub-threshold slopes and reliable metal/*p*-GaN interfaces. However, the GITs can suffer from their relatively large gate leakage currents. A current-driving design is also required for the GITs, which is less convenient. Compared with the ohmic-type gate scheme, the Schottky-contact scheme yields voltage-driven devices with much lower forward gate leakage currents due to the reverse-biased metal/*p*-GaN Schottky junctions [54]. Hence, the Schottky contact gate structure without gate metal annealing is more popular both in the literature and commercialization, which was also used in this work.

In literature, typical metals used for the Schottky contact gates include Ti, Ni, W, and TiN [56], [65]. According to the Schottky-Mott relation, the metal/semiconductor Schottky barrier height Φ_B for a p-type semiconductor obeys the relation:

$$\Phi_B = E_G - (\Phi_m - \chi_s), \tag{2.1}$$

where E_G is the bandgap of the semiconductor, Φ_m is the work function of the metal, and χ_s is the electron affinity of the semiconductor. Hence, a metal with a lower work function should give a higher Φ_B. Hwang et al. used Schottky contacts in their normally-off HEMTs, showing that a lower work-function metal (W) with a higher Φ_B, allows an increase in the V_{TH} with respect to a higher work-function one (Ni) and, at the same time, enables a reduction of the gate leakage current [54]. Considering that high V_{TH} and a low gate leakage current are desired for *p*-GaN gate HEMTs, a low work function metal should be adopted. However, the metal/semiconductor interface is known for its high-density interface states, which have a big impact on the electrostatics. The exact experimental value of the metal/*p*-GaN barrier height depends not only on the metal-work function

but also on the processing conditions (surface preparation, material defects, annealing, etc.), making its impact more complicated [87]. The effect of the gate metal on the HEMT's performance will be discussed more thoroughly in Chapters 3 and 4.

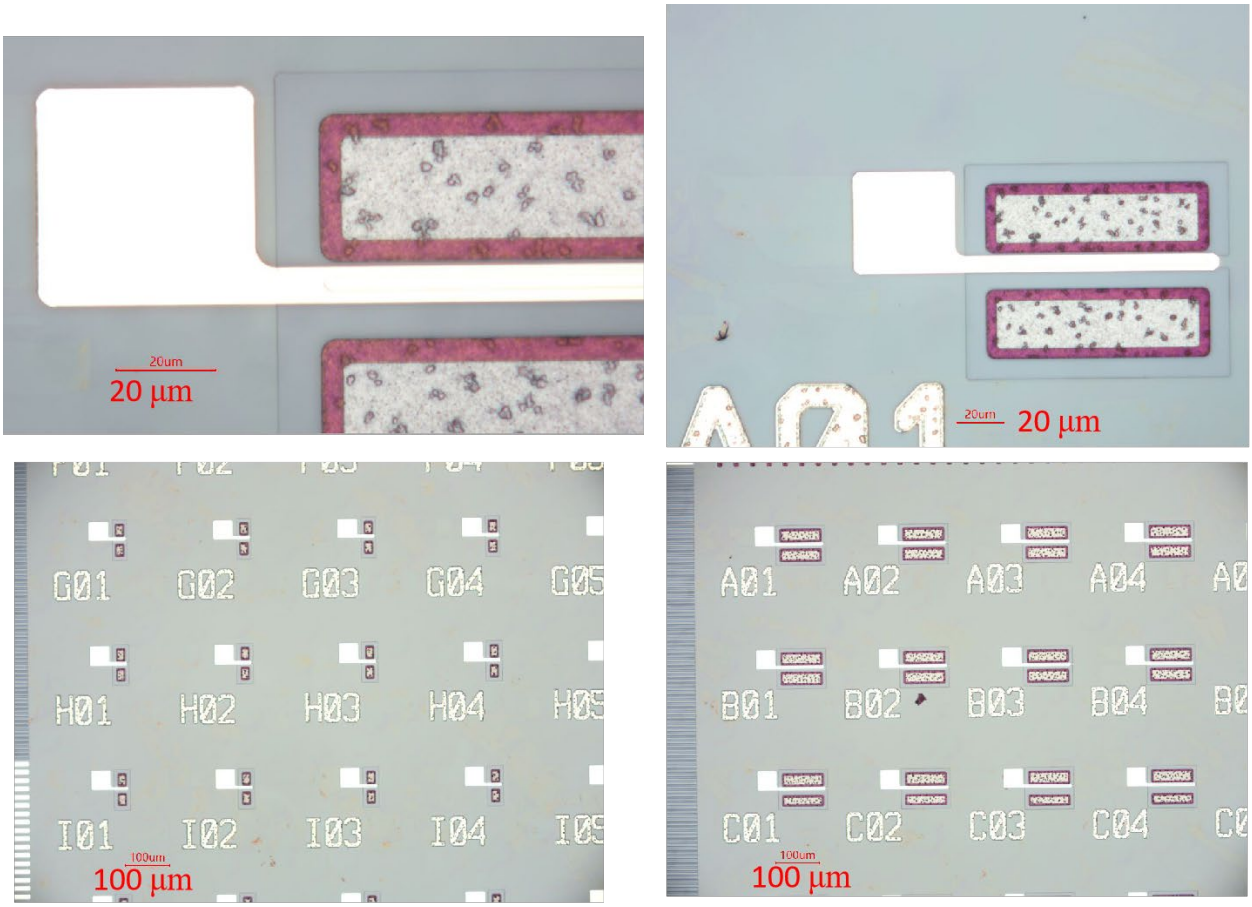


Figure 2.15 Microscopic view of the devices after the gate metal deposition.

In the baseline processing, the author adopted Ti/Au (40/110 nm) as the gate electrode due to its low work function. A standard lift-off technology was implemented with double-layer photoresists. Before the gate metal deposition, the wafers were immersed in the diluted HCl solution (39% HCl: H_2O = 1: 4) for 1 min to remove the native oxide layer. Immediately after rinsing them in DI water and blowing them dry with a nitrogen gun, the wafers were loaded into

an HHV-TF500 e-beam evaporation system. Figure 2.15 shows the devices observed by an optical microscope after the gate metal deposition.

2.1.7 Contact Metal Deposition

Contact metals are not metals directly deposited on the gate or the source/drain of a HEMT. They are metal lines/pads connecting those terminals and the outside environment for measurements or to modify the electrical field to increase the device breakdown voltage, in which case, the metals are called field-plates (FP). In a GaN HEMT, the FP structures are very effective in modifying the electric field distribution and lowering the peak electric field at the gate edge on the drain side [88]-[90]. This is in analogy to the case that the shape of a heat source can impact the temperature distribution. The electric fields in a HEMT with and without FP structure were simulated using Silvaco, as shown in Figure 2.16. The FPs are the overhangs on the source and the gate. Simulation results showed that the peak electric field near the gate edge was lowered by the FP structures. In addition, the reduction of the electric field at the gate edge could also reduce the number of trapped electrons at the AlGaN surface. Thus, the FP structures are effective in suppressing the increase of R_{ON} under high drain voltage. Ando et al. demonstrated that the gate FP significantly reduced current collapse, leading to a high-efficiency power performance of AlGaN/GaN HEMTs under high voltage operation [89].

In the baseline processing, a 200 nm SiN_x deposited by PECVD was used as the second passivation layer. Ti/Au (20/200 nm) were adopted as the contact metals formed by e-beam evaporation. Figure 2.17 shows the device images obtained by an optical microscope after the second SiN_x layer and contact metal deposition.

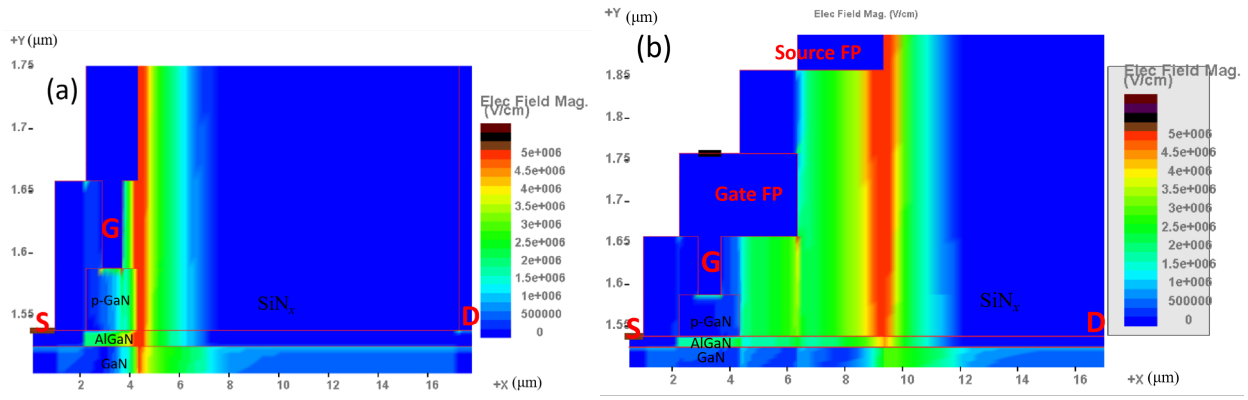


Figure 2.16 The electric field simulation at V_{DS} = 650 V for the HEMT (a) without FP and (b) with FP.

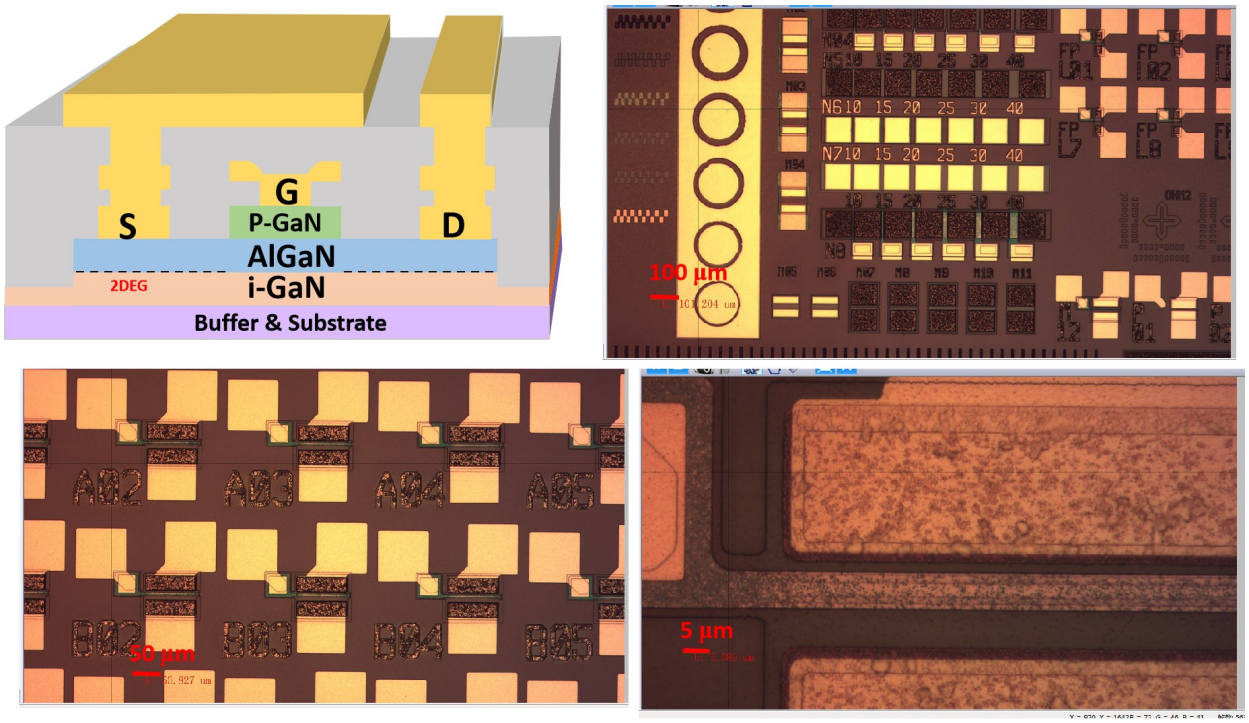


Figure 2.17 Schematic and microscopic views of the devices after the second SiN_x layer and contact metal deposition.

2.2 Characterization of *p*-GaN Gate HEMTs

The electrical characterizations were carried out using a Keithley 4200 Analyzer and a probe station. The *p*-GaN gate HEMTs from the baseline processing featured a gate width (W_G) of 100 μm, a gate length (L_G) of 5 μm, a gate-source distance (L_{GS}) of 3 μm, a gate-drain distance (L_{GD}) of 12 μm, a gate field plate (G-FP) of 1 μm, and a source field plate (S-FP) of 3 μm, as illustrated in Figure 2.18(a). Unless specified, the characterizations adopted the sweep mode under a "normal" measurement speed (0.05 V/step, delay time = 1 ms, measure time = 53.59 ms) with the substrates floating. The measurement temperature was 25 °C. Different parameters of the HEMTs were extracted. The currents were normalized to W_G unless specified.

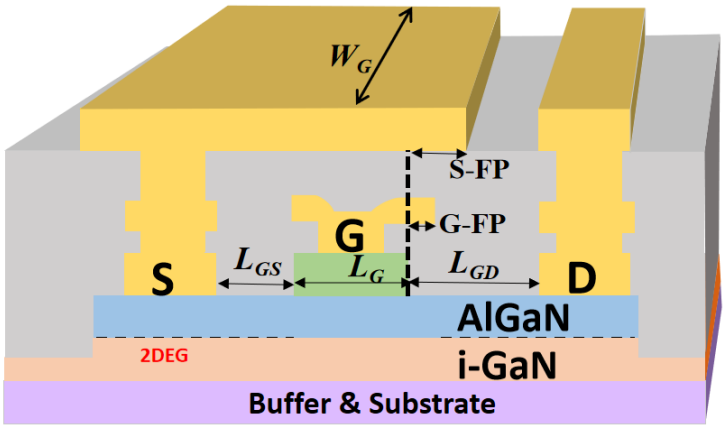


Figure 2.18 Schematic of the baseline *p*-GaN gate HEMTs and the corresponding geometry parameters.

Transfer characteristic (I_D-V_{GS}) measurements were carried out to extract the V_{TH}, hysteresis, sub-threshold swing (*SS*), and I_{ON}/I_{OFF} ratio of the HEMTs. The drain voltage was fixed at V_{DS} = 1 V. The drain current (I_D) was measured as the gate voltage was swept from -4 to 8 V and then swept back to -4 V. There are two different methods to define the V_{TH}: the linear extrapolation method and the current density method. In the early stage of *p*-GaN gate HEMT research, V_{TH} was routinely defined by the linear extrapolation method introduced from the CMOS,

or the gate voltage of the intersection of the linear extrapolation at the maximum slope (maximum transconductance) [55], [58], [59]. However, researchers later found it less convenient to design the gate drivers for power devices using V_{TH} defined by such a method. Besides, the comparison of V_{TH} by different works can be difficult since the values rely on the details (the measurement step, smoothing of the raw data, etc.). The current density method is more recognized now, where V_{TH} is defined as the gate to source voltage where the unit width I_D equals to 0.01 mA/mm or 0.1 mA/mm [65], [75], [92], [93]. The hysteresis is defined as the maximum voltage difference between the sweep-up curve and the sweep-down curve at the same current. I_{ON}/I_{OFF} ratio is defined as the ratio between the maximum $I_{D,ON}$ and the $I_{D,OFF}$, where the transistor is fully pinched off.

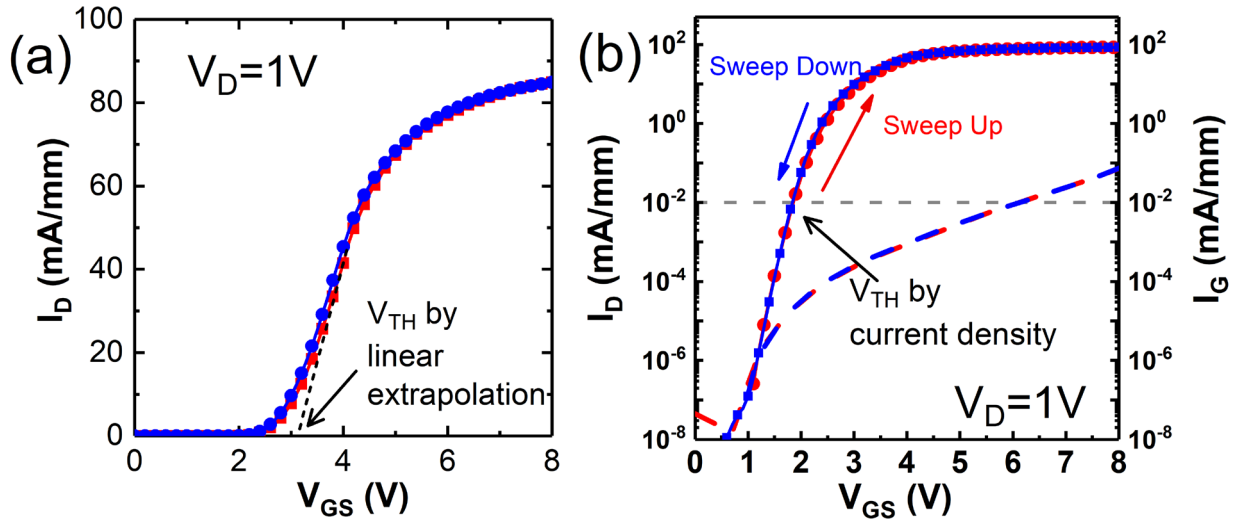


Figure 2.19 Transfer characteristics plotted in (a) linear scale and (b) log scale. V_{TH} is defined by (a) the linear extrapolation method or (b) the current density method at I_D = 0.01 mA/mm.

Transfer characteristics measured from the baseline HEMTs appear in Figure 2.19. V_{TH} was extracted to be 3.05 V by the linear extrapolation method and 1.8 V by the current density

method (0.01 mA/mm). A high I_{ON}/I_{OFF} current ratio of 5×10^8 and a low hysteresis less than 50 mV were achieved. The *SS* was determined to be 148 mV/dec extracted at V_{GS} = 1.2 V.

Output characteristics (I_D-V_{DS}) measurements were carried out to extract the R_{ON} and saturated drain current density (I_{SAT}). For the I_D-V_{DS} measurement, V_{DS} was swept from 0 to 8 V with a constant V_{GS}, and the measurement was repeated at increasing gate voltages. I_{SAT} was extracted as the maximum drain current density. R_{ON} was evaluated according to the I_D-V_{DS} with the maximum V_{GS} in the linear region. As illustrated in Figure 2.20 (a), R_{ON} was extracted to be 13 Ω·mm, and I_{SAT} was extracted to be 295 mA/mm from the baseline *p*-GaN gate HEMTs.

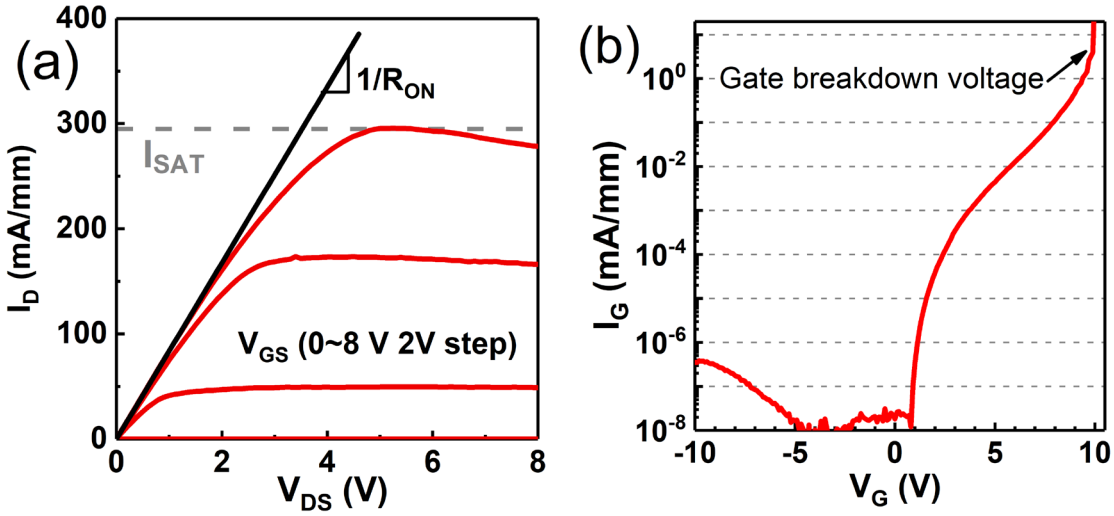


Figure 2.20 (a) Output characteristics of the baseline HEMTs where R_{ON} and I_{SAT} could be extracted; (b) gate leakage characteristics of the baseline HEMTs.

The gate leakage characteristics (I_G-V_{GS}) were carried out to measure I_G with varying V_{GS} (Figure 2.20 (b)). In this measurement, V_{DS} was fixed at 0 V, and voltage bias was applied between the gate and the S/D. The gate breakdown voltage (gate BV) is defined as the V_{GS} when I_G shows a sudden increase, which is the gate breakdown point. For the baseline *p*-GaN gate HEMTs, the gate breakdown voltage was measured to be 10 V.

The off-state drain to source breakdown voltage BV_{DSS} was evaluated by applying a positive V_{DS} with V_{GS} held at 0 V at off-state. As demonstrated in Figure 2.21, BV_{DSS} was extracted to be 700 V. The state-of-the-art GaN HEMTs can provide BV_{DSS} above 1000 V. The extracted DC parameters from the baseline *p*-GaN gate HEMTs appear in Table 2.3.

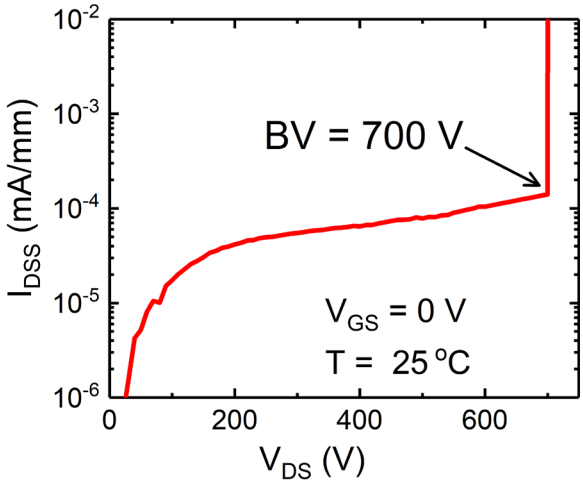


Figure 2.21 Off-state drain leakage current for the baseline *p*-GaN gate HEMTs.

Parameters	Unit	Value
V_{TH} (linear)	V	3.05
V_{TH} (I_D = 0.01 mA/mm)	V	1.8
I_G (V_G = 8V)	mA/mm	~ 1
I_{ON}/I_{OFF}	/	5×10^8
R_{ON}	Ω•mm	13
Gate BV	V	10
SS	mV/dec	148
BV_{DSS}	V	700

Table 2.3 Summary of extracted DC parameters.

Chapter 3: Determination of the Gate Breakdown Mechanisms in *p*-GaN Gate HEMTs by Multiple-gate-sweep Measurements

As discussed previously, among different approaches to realize enhancement mode (e-mode) operation [94]-[97], the *p*-GaN gate AlGaN/GaN HEMT emerged as the leading solution [98], [99]. However, due to the relatively low gate BV (usually 10~12 V), the maximum gate operation voltages for *p*-GaN gate HEMTs are usually 5-7 V [98], [99]. The small gate voltage swing has imposed significant constraints on the gate driver design. Improving the gate BV remains a critical challenge in *p*-GaN gate HEMTs. However, the gate breakdown (BD) mechanisms are still controversial among the available reliability studies [100]-[111]. Some works have proposed that the gate BD originated from the BD of *p*-GaN/AlGaN/GaN junction (PiN) or the AlGaN barrier layer [100]-[104]. Meanwhile, others have ascribed that to the creation of the percolation path in the *p*-GaN/metal interface [105]-[107]. Especially, I. Rossetto et al. found that the peak electric field across the AlGaN would decrease with the positive gate bias, disapproving the BD of PiN or AlGaN layer [108]. Whether the PiN junction is likely to fail remains indeterminate. A method to determine the BD mechanism is still lacking, which is the motivation of the work in this chapter.

A new multiple-gate-sweep-based gate BD mechanism analysis approach was proposed and demonstrated here as an effective and generic method to determine a gate BD mechanism. The multiple-gate-sweep is to induce and decouple the BDs of different device regions. For the first time, three different BD mechanisms have been decoupled and identified from the devices of the same structure: 1) the metal/*p*-GaN junction BD; 2) the PiN junction or AlGaN barrier BD; and 3)

the passivation related BD. The PiN junction BD has been directly observed. The BVs of the different BD mechanisms and their dependences on temperature and passivation technology were also investigated.

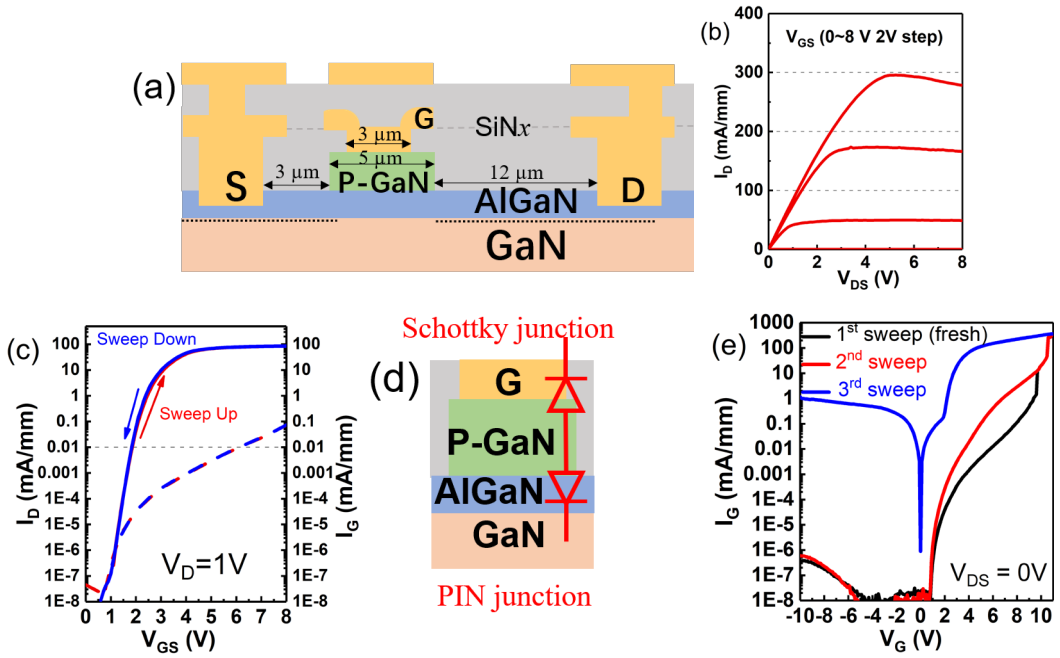


Figure 3.1 (a) Schematic view of the device structure; (b) output characteristics of the *p*-GaN HEMTs; (b) transfer characteristics of the HEMTs under V_{DS} = 1 V; (d) Schematic cross-sectional view of the gate regions and the equivalent circuit; (e) gate leakage characteristics of three gate sweeps with V_{DS} = 0 V showing the first and the second breakdowns.

3.1 Device Structure and Gate Breakdown

The *p*-GaN gate HEMTs were fabricated on 75 nm *p*-GaN/15 nm $Al_{0.2}Ga_{0.8}N$/0.7 nm AlN/4.5 μm GaN epi-structures grown on Si (111) substrates as shown in Figure 3.1(a). The *p*-GaN layer was doped with Mg to a concentration of 4×10^{19} cm^{-3}. The fabrication process is described in detail in Chapter 2. The sheet resistance of the 2DEG was extracted to be 610 Ω/square

using the circular transmission line model (CTLM) measurements. Two SiN_x layers were deposited as the passivation layers by plasma-enhanced chemical vapor deposition (PECVD). A Schottky-type contact was formed between the Ti/Au and the *p*-GaN gate. The devices under test feature a gate width (W_G) of 100 μm, a gate length (L_G) of 5 μm, a gate-source distance (L_{GS}) of 3 μm, and a gate-drain distance (L_{GD}) of 12 μm. On-wafer characterization was performed by a Keithley 4200 Analyer using the sweep mode of "Normal" measurement speed (0.05V/step, delay time = 1 ms, measure time = 53.59 ms) with a floating substrate. Unless specified, the measurement temperature was 25 ^oC.

As shown in Figure 3.1(b) and (c), the V_{TH} is extracted to be 1.8 V at I_D of 0.01 mA/mm. A high I_{ON}/I_{OFF} current ratio of 5×10^8 and a low on-resistance R_{ON} of 13 Ω·mm have been achieved. At V_{GS} = 8 V, the maximum drain current is extracted to be 290 mA/mm. The device exhibited a breakdown voltage larger than 400V, defined at the criteria of I_{DSS} reaching 1 μA/mm.

Figure 3.1(d) shows the equivalent circuit of the gate and the regions below, which consists of a metal/*p*-GaN Schottky junction and a *p*-GaN/AlGaN/GaN PiN heterojunction. The Schottky junction limits the I_G when $V_G > 0$ V, while the PiN does that when $V_G < 0$ V. Figure 3.1(e) illustrates the gate leakage (I_G-V_G) characteristics of a typical measurement using three consecutive gate sweeps. The device shows two abrupt I_G increases in the first and second sweeps, consistent with very recent studies [109], [110], indicating the existence of at least two different BD mechanisms. Huang et al. and He et al. have attributed the first-step breakdown to Schottky junction failure and second-step breakdown to PiN junction failure. In the following text, we will demonstrate that second-step breakdown should be ascribed to passivation-related failure. Moreover, it's found that the PiN failure won't result in an increase of I_G in the positive bias.

3.2 The Metal/*p*-GaN Junction BD in the First Sweep

In Figure 3.1(e), in the first sweep, I_G increases abruptly when V_G reaches 9.2 V, suggesting a hard BD of the gate. However, in the second sweep, the reverse I_G has negligible change compared to the first sweep, indicating that the PiN junction remains functional. The transfer characteristics of the HEMTs before and after the first BD are shown in Figure 3.2(a). The device can still be turned off/ON with a high I_{ON}/I_{OFF} ratio. The "gate control" of the channel is preserved. Besides, the device shows a lower threshold voltage, a lower subthreshold swing and a higher I_D after first-step breakdown after the first BD. These features indicate that the first BD should be attributed to the metal/*p*-GaN Schottky junction failure. The degradation has converted the Schottky junction to an ohmic-like gate. Figure 3.2(b) compares the I_{DSS} before and after the Schottky BD, showing that the off-state leakage blocking capability of the gate stack is maintained.

Although a HEMT cannot function as a normal switch after the first BD, the following BDs in the subsequent sweeps of the HEMTs are still worth investigating: 1) Owing to the device structure and gate technology differences, the first BD mechanism varies in the literature as in Ref. [102], [109]-[112]. Further sweeps and BDs can help to determine the first BD mechanism; and 2) To protect a switch system, it is vital to maintain the off-state blocking capability (i.e., a low I_{DSS}) of the *p*-GaN HEMTs after the gate BD as argued in Ref. [110].

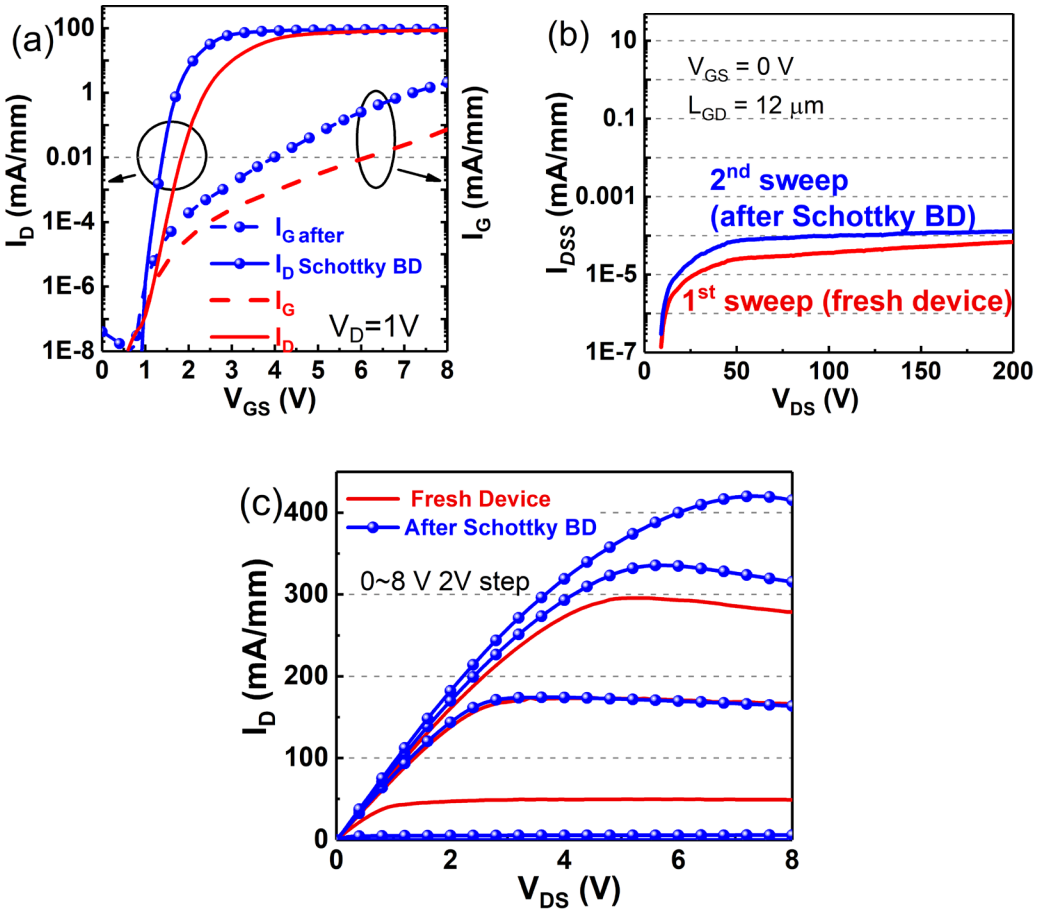


Figure 3.2 The device performances before (red) and after (blue) the Schottky junction breakdown: (a) transfer characteristic; (b) off-state drain leakage; (c) output characteristic.

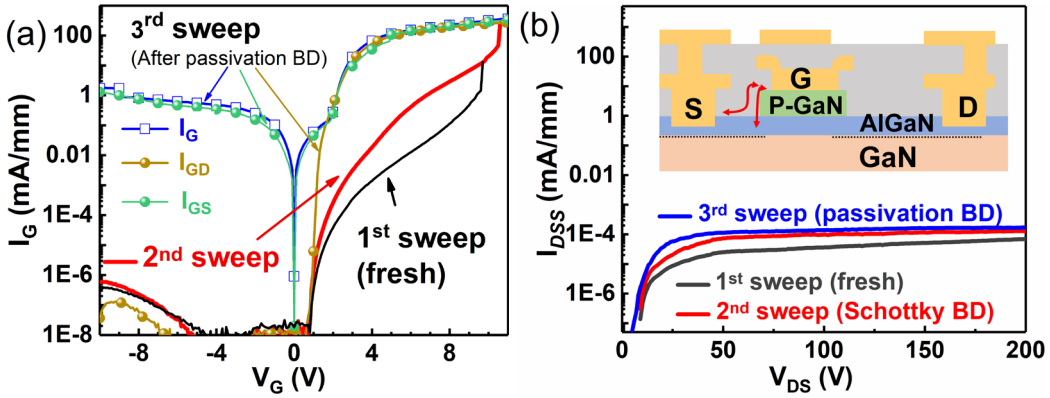


Figure 3.3 (a) The passivation related BD in the second sweep; and (b) I_{DSS} before and after passivation related BD. Inset: illustration of two possible leakage paths responsible for the passivation related BD.

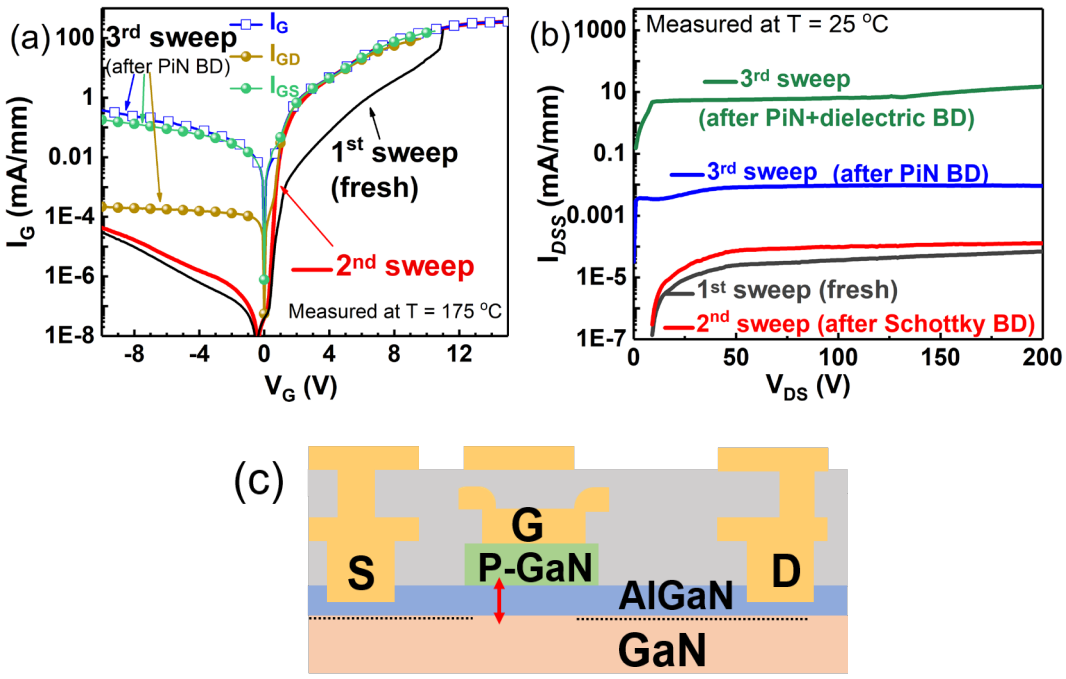


Figure 3.4 (a) The PiN junction BD in the second sweep; (b) I_{DSS} before and after PiN junction failure; and (c) illustration of the leakage path responsible for the PiN junction BD.

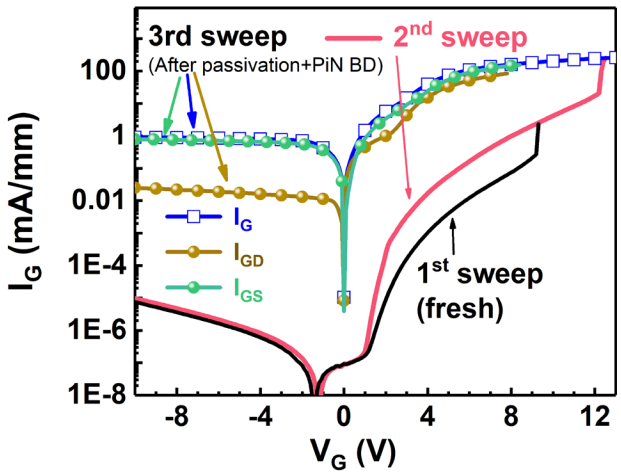


Figure 3.5 Gate leakage characteristics before and after the both breakdown of the passivation and PiN junction.

3.3 Passivation Related BD and PiN BD in the Second Sweep

As shown in Figure 3.1(b), after the second BD, I_G increases significantly under both forward and reverse bias. However, either PiN junction BD or passivation related BD may possibly lead to this phenomenon, which makes it challenging to identify the BD mechanism. In this work, we propose a simple but effective method to determine the mechanism, which is to measure the gate-drain current (I_{GD}) and the gate-source current (I_{GS}) separately. Figure 3.3(a) shows I_G, I_{GD} and I_{GS} after the second BD in the third sweep. The I_{GS} component is very close to I_{GD} when $V_{GS} = V_{GD} > V_{TH}$ (~ 1.4 V), while I_{GS} is approximately seven orders of magnitude higher than I_{GD} when $V_G < V_{TH}$. This I_{GD}/I_{GS} difference can be explained by the failure of the passivation on the source side. A leakage path between the G and S terminals has been created either along the passivation/*p*-GaN left sidewall or through the passivation in the second BD, while the PiN junction below remains intact. The "gate control" of the channel is still preserved. When $V_G < V_{TH}$, the channel under the gate is depleted; thus, I_{GD} maintains at a low level. When $V_G > V_{TH}$, the channel is turned on connecting the S and D terminals, thus I_{GD} is comparable to I_{GS}. This conclusion is confirmed by I_{DSS} in Figure 3.3(b). Despite the large reverse I_G, the I_{DSS} maintains at a low level after the second BD.

Furthermore, the PiN junction or AlGaN barrier BD has been successfully observed at higher temperatures thanks to the multiple-sweep measurement instead of step stress or a constant stress measurement. As illustrated in Figure 3.4(a), in the second sweep at 175 ^oC (red), there is no typical abrupt I_G increase when $V_{GS} > 0$ V as an indication of a BD. However, in the third sweep, I_G increased several orders of magnitude in the $V_{GS} < 0$ V regime without any I_G increased when $V_{GS} > 0$ V. Besides, both I_{GD} and I_{GS} increased when $V_{GS} < 0$ V. The I_{DSS} also increased several

orders of magnitude as shown in Figure 3.4(b). Based on these, we can infer that a PiN junction BD happened in the second sweep. Its failure will not contribute more leakage current when V_{GS} > 0 V. This phenomenon confirms the possibility of the PiN junction failure and reveals that this failure itself will unlikely result in the increase of I_G in the positive bias regime, disapproving the deductions in previous studies [100-102, 108-110]. This feature makes it difficult to observe the PiN junction BD in a stress measurement due to the lack of a typical breakdown feature. To our best knowledge, this is the first report of direct observation of PiN junction failure. The physical origin PiN BD may be closely related to dislocations in GaN/AlGaN. In literature, it's found that the dislocations in GaN diode can increase the reverse-bias leakage current significantly, whereas they have little impact on the forward-bias current [113]. This conclusion is consistent with our finding that the PiN junction breakdown will only increase the reverse-bias leakage current.

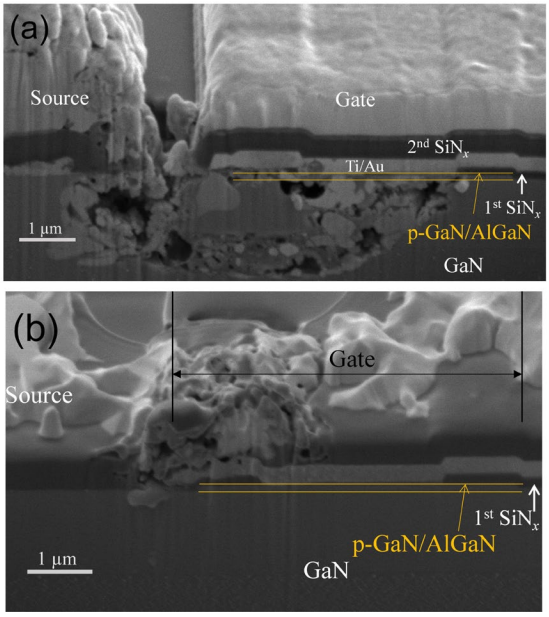


Figure 3.6 Cross-section view of BD damages by SEM: (a) damages mainly caused by a PiN junction failure; and (b) damages mainly caused by a passivation related failure. The two parallel lines indicate the top and the bottom surfaces of the *p*-GaN/AlGaN layer.

	when $V_G > 0V$		when $V_G < 0V$		
	I_{GS}	I_{GD}	I_{GS}	I_{GD}	I_{DSS}
Schottky BD	↑	↑	-	-	-
Passivation related BD*	↑	↑	↑	-	-
PiN BD	-	-	↑	↑	↑
Passivation + PiN BD	↑	↑	↑	↑	↑

*$V_G > V_{TH}$ or $V_G < V_{TH}$ in this case

Table 3.1 Features of different BD

Meanwhile, it's also possible that the passivation related BD and the PiN junction BD happen in the same sweep, as illustrated in Figure 3.5. The features of different BD mechanisms are summarized in Table 3.1, where the "↑" indicating an increase of the leakage current and the "-" indicating no significant change.

When a device is exposed to higher gate voltage, damages are likely to occur due to the heating effect. The cross-sections of the damaged parts have been prepared by focused ion beam etching (FIB) and imaged by scanning electron microscopy (SEM), as illustrated in Figure 3.6. Damages originated from the PiN junction failure are clearly shown in Figure 3.6(a). Meanwhile, the PiN junction remains intact while the passivation was severely damaged in Figure 3.6(b). These observations confirmed our previous deductions that both PiN BD and passivation related BD can happen in *p*-GaN gate HEMTs.

3.4 Simulation and Gate BV Comparisons of the Different BD Mechanisms

The electric field across the gate region has been simulated numerically by Silvaco' Technology Computer Aided Design (TCAD) software as shown in Figure 3.7 [58]. The considered structure is as depicted in Figure 3.1(a). Incomplete ionization of magnesium acceptors

has been taken into account with an ionization energy of 170 meV [114]. The results of the simulations showed that the electric field can be quite high in two regions of the device: the *p*-GaN footing and AlGaN/GaN interface, which are close related to the passivation related failure and PiN junction failure, respectively.

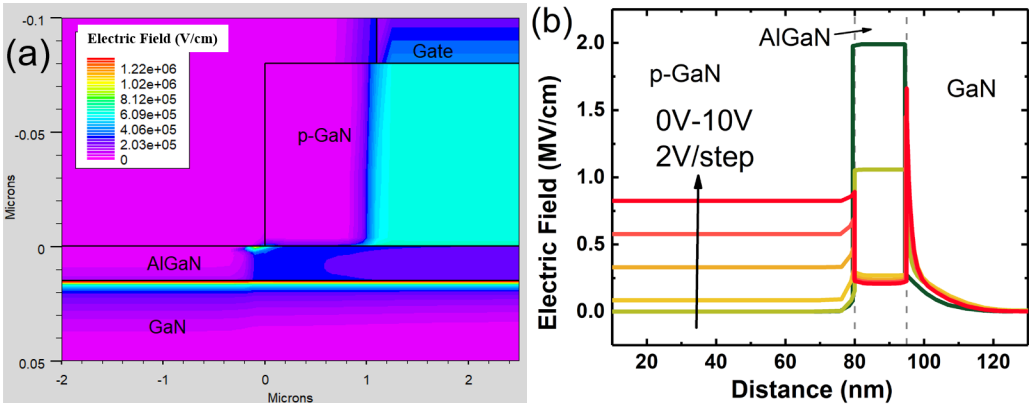


Figure 3.7 TCAD Simulation (Silvaco) of the electric field (a) across the gate region under V_{GS} = 8V; and (b) across the *p*-GaN/AlGaN/GaN layers under different gate bias.

Temperature-dependent measurements were conducted from 25 ºC to 175 ºC with 37.5 ºC per step to get further insights into the BD mechanisms. For each temperature, at least ten devices were measured by multiple-gate-sweep. To extrapolate the BV of PiN junction failure, more than sweep has been carried out. The maximum forward V_G has been increased by 0.1 V in each sweep until the increased reverse I_G was observed. The maximum V_G in the last sweep was then defined as the PiN junction BV. Figure 3.8(a) shows the statistical summary of the gate BVs. The sequence of the BDs depends on the measurement/operation temperature. Schottky BD has the smallest BV, so it happens before others. At a higher temperature, PiN BD is likely to happen prior to the passivation related BD as shown in Figure 3.4, which may not be the case for lower temperatures. The different BD mechanisms show different temperature dependences. The Schottky failure has

very weak temperature dependence, while the passivation related failure and PiN failure clearly have positive temperature dependence. The positive temperature dependence of PiN junction failure is ascribed to a dominant role of impact ionization, as discussed in [115].

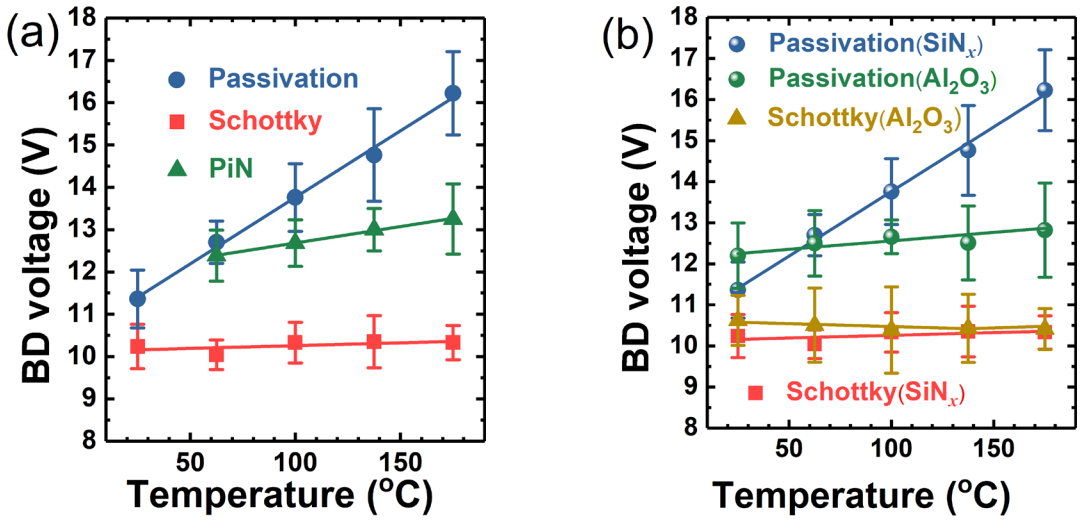


Figure 3.8 (a) BVs of different mechanisms and their temperature dependence (SiN_x as the passivation layers); (b) The Schottky junction and passivation related BVs of the devices with a SiN_x or an Al_2O_3 as the passivation layer, respectively.

Furthermore, the gate BVs with different passivation layers have also been compared. In the comparison group, the device structure and fabrication process are the same as previous except that the SiN_x layer was replaced by a 100 nm Al_2O_3 layer deposited by atomic layer deposition (ALD). As illustrated in Figure 3.8(b), their Schottky breakdown voltages have little difference at different temperatures, which is as expected since the passivation layer is not related to the Schottky junction. On the other hand, the passivation related BV in those devices with Al_2O_3 passivation layers has a much weaker temperature dependence compared to those with SiN_x. These results further valid our BV mechanism determination method discussed above. The "second-step" breakdown should be ascribed to passivation related failure instead of the PiN junction failure as

claimed by Ref. [109], [110]. Otherwise, the different passivation layers should have little impact on the BVs. These results also help to explain the differences in the temperature dependence of the gate breakdown in literature. Therefore, to improve the gate reliability of *p*-GaN gate HEMTs, it's also essential to optimize the passivation technology.

3.5 Chapter Summary

In this work, the gate BD mechanisms of *p*-GaN gate AlGaN/GaN HEMTs were studied thoroughly by the multiple-gate-sweep-based method. Three different BD mechanisms have been observed and confirmed by SEM: the metal/*p*-GaN Schottky junction BD, the PiN junction BD, and the passivation related BD. By measuring I_{GD} and I_{GS} separately and doing I_{DSS} analysis, the BD mechanisms can be successfully identified. This method is generally applicable for *p*-GaN gate HEMTs. Especially, it's demonstrated that the PiN junction failure alone doesn't lead to an increase of I_G at $V_G > 0$ regime disapproving previous literature. Besides, it's demonstrated that the three BD mechanisms have different temperature dependences. The Schottky junction failure has a very weak temperature dependence, while the PiN junction failure has a positive temperature dependence. For the passivation related breakdown, its dependence on temperature is closely related to the passivation technology. We believe the clarification of BD mechanisms and this BD analysis method will shed more light on improving the gate BV and reliability.

Chapter 4: Gate Leakage Suppression and Breakdown Voltage Enhancement in *p*-GaN HEMTs using Metal/Graphene Gates

In this part of work, we tried to utilize a 2D material, graphene, in a HEMT to reduce the gate leakage. Reducing the gate leakage current and increasing the gate breakdown voltage (BV) remain as big challenges for *p*-GaN gate HEMTs [66], [116], [117]. The forward gate leakage current limits the gate voltage swing and causes gate drive losses, while the reverse gate leakage can lead to the off-state power consumption [117]. The low gate BV (usually < 11V) has imposed a significant burden upon gate drive design [118]. Previous studies in MIS-HEMTs revealed that fluorinated graphene (F-Graphene) can serve as a barrier layer between Al_2O_3 and GaN, which suppressed the gate leakage current by two orders of magnitude [119]. While retaining the carbon skeleton of intrinsic graphene (I-Graphene), F-graphene is usually more resistive than I-Graphene due to the existence of a bandgap, contrary to the zero bandgap of I-graphene [120]. Besides, graphene can act as a strong barrier to atom diffusion and saturate the dangling bonds and defects on the surface [121], [122]. However, there had not been any reports on the effectiveness of graphene in *p*-GaN HEMTs, which was addressed in this chapter.

Single-layer intrinsic and fluorinated graphene layers were investigated as gate insertion layers in normally-off *p*-GaN gate HEMTs, which wraps around the bottom of the gate forming Ti/graphene/*p*-GaN at the bottom and Ti/graphene/SiN_x on the two sides. Compared to the Au/Ti/*p*-GaN HEMTs without graphene, the insertion of graphene was found to increase the I_{ON}/I_{OFF} ratio, increase the V_{TH} and reduce the off-state gate leakage. This is considered to be a

result of the increase in Schottky barrier height and the better quality of the Ti/graphene/*p*-GaN and Ti/graphene/SiN_x interfaces. This approach was shown to be very effective in improving the I_{ON}/I_{OFF} ratios and gate breakdown voltages of normally-off GaN HEMTs in this work.

4.1 Device Structure and Fabrication

The *p*-GaN gate HEMTs were fabricated on 100 nm *p*-GaN/15 nm $Al_{0.2}Ga_{0.8}N$/0.7 nm AlN/4.5 µm GaN epi-structures grown on Si (111) substrates as described in Chapter 2. Figure 4.1 shows the schematic cross-section of the devices. 120 nm SiN_x PECVD was used as the first passivation layer. Prior to the deposition of gate metals (40 nm Ti/100 nm Au), single layer graphene grown by chemical vapor deposition (CVD) on Cu foils was transferred to part of the wafer surface via the "polymethyl methacrylate (PMMA)-mediated" wet-transfer approach [123]. The undesired part of graphene was etched away by O_2 plasma after the deposition of the gate metals. Finally, the devices were annealed at 350 °C in N_2 for 5 minutes to improve the Au/Ti/(graphene)/*p*-GaN interface. The devices under test feature a W_G of 100 µm, a L_G of 5 µm, a L_{GS} of 3 µm, and a L_{GD} of 10 µm.

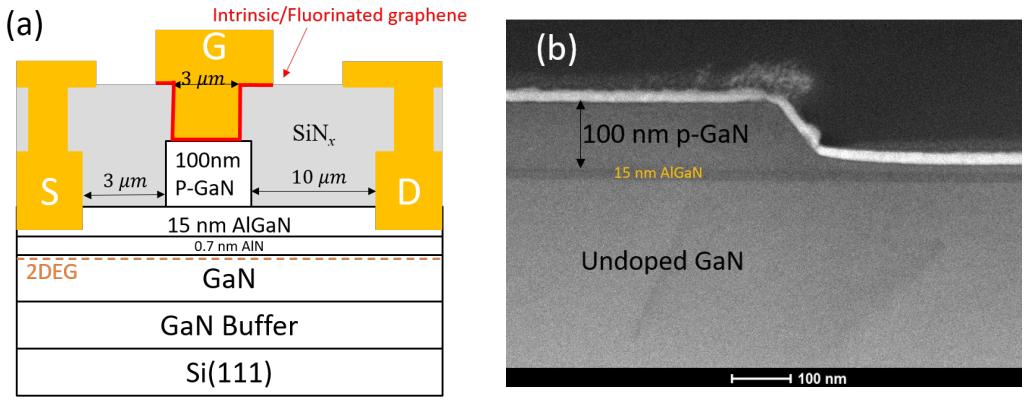


Figure 4.1 (a) Schematic view of the device structure; (b) Cross-section of the device characterized by a scanning transmission electron microscope (STEM) showing the edge of a *p*-GaN gate and the *p*-GaN/AlGaN/GaN structure.

To investigate the impact of graphene's electronic properties on this structure, two types of graphene, I-graphene and F-graphene, were investigated. F-graphene was realized by exposing the I-graphene to SF_6 plasma before the transfer process. In this experiment, the quality and the cleanness of the transferred graphene are crucial, as the metal/semiconductor barrier height heavily depends on the surface states and defects. Especially, the PMMA residuals could introduce considerable unwanted surface states at the metal/graphene/*p*-GaN junction, which would eventually result in nonuniform or unstable performances of these devices [124]. As illustrated in Figure 4.2, the Raman spectra and SEM pictures show that the transferred I-graphene ($I_{2D}/I_G \approx 2$) and F-graphene ($I_D/I_G \approx 1.2$) have high quality with negligible PMMA contaminations [120], [125].

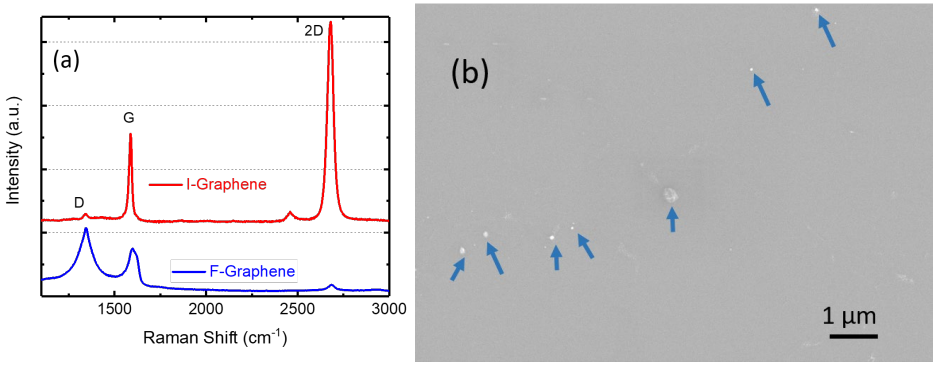


Figure 4.2 The transferred graphene characterized by (a) Raman spectroscopy and (b) SEM, a few PMMA residuals are shown intentionally as noted by the arrows.

4.2 HEMTs Results

The HEMTs with and without graphene are from the same wafer piece. The gate leakage, transfer and output characteristics of the HEMTs are shown in Figure 4.3. Compared to the HEMTs with Ti/*p*-GaN gate structures, those with Ti/I-graphene/*p*-GaN and Ti/F-graphene/*p*-GaN gate

structures have about one order of magnitude lower gate leakage under a forward bias and 50 times lower leakage current under a reverse bias.

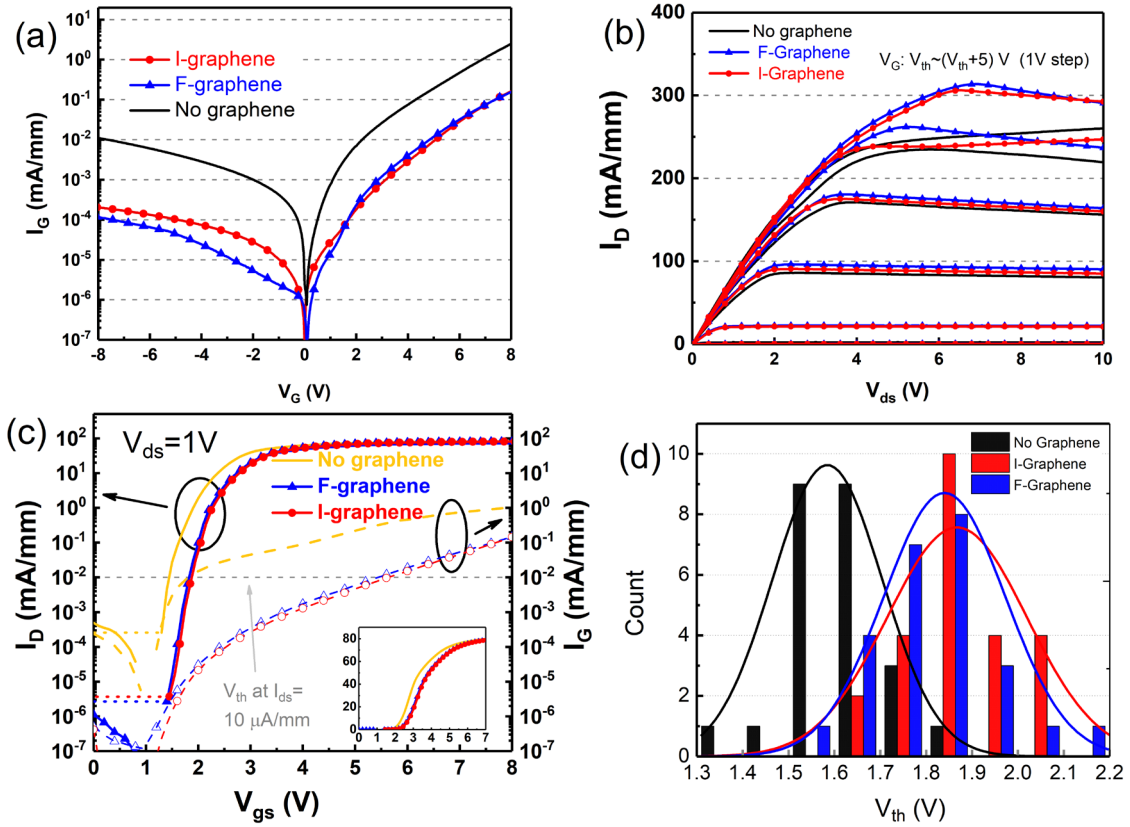


Figure 4.3 Comparison of the device performances of the *p*-GaN HEMTs with I-graphene, F-graphene and without graphene; (a) gate leakage characteristics under V_{DS} = 0 V; (b) output characteristics (V_G from V_{TH} to (V_{TH} + 5V)), 1V step); (c) transfer characteristics under V_{DS} = 1 V, the inset figure is transfer characteristics plotted in linear scale; and (d) V_{TH} uniformity characterization.

Additionally, the HEMTs with graphene have higher V_{TH} defined at I_{DS} = 10 μA/mm (0.32 V higher for I-graphene and 0.28 V higher for F-graphene). More importantly, the insertion of graphene increased the I_{ON}/I_{OFF} ratio by at least one order of magnitude for both types of graphene. Detailed comparison of the extracted DC parameters between the three types of devices is shown in Table 4.1. The statistical data of V_{TH} are shown in Figure 4.3 (d). The average V_{TH} values of the devices without graphene, with I-graphene and with F-graphene are 1.58 V, 1.86 V and 1.84

V, respectively. The increase of V_{TH} should be attributed to the higher Schottky barrier height (Φ_B) and p-type doping in graphene introduced in the "PMMA-mediated" wet-transfer process [123]. In summary, the insertion of graphene reduced the gate leakage current and increased V_{TH} without sacrificing any output performances. The small difference between F-graphene and I-graphene demonstrates that the electronic property of graphene was not the dominant reason for device performance improvement. Instead, those should be attributed to the higher Φ_B and the better interfaces, which will be discussed in the following sections.

Parameters	No graphene	I-Graphene	F-Graphene
I_G (V_G = 8V) (mA/mm)	~ 2	~ 0.1	~ 0.1
I_{OFF} (mA/mm)	2.5×10^{-4}	3.6×10^{-6}	1.2×10^{-6}
V_{TH} (V)	1.54	1.86	1.82
R_{ON} (Ω•mm)	12.4	12.8	11.9
Gate BV (V)	9.8	12.05	12.0
SS (mV/dec)	195	160	160

Table 4.1 Comparison of extracted DC parameters.

4.3 Effects of Graphene during Annealing Treatment

In practice, passivation layers are necessary for metal pad and interconnect protection. This means that the gate metal/*p*-GaN interfaces will commonly experience some low-temperature thermal annealing. For the gate-metal-first process, the interface will undergo an even higher thermal budget for S/D contact annealing [66]. To investigate the effects of graphene during these thermal steps, the gate leakage currents of devices were also been measured before the annealing treatment (350 °C in N_2 for 5 minutes). Figure 4.4 presents the gate leakage characteristics and gate BV before and after annealing.

As illustrated in Figure 4.4, when $V_G > 0$ V, all the devices have a considerable increase in the gate leakages. This should be due to the reduction of Φ_B. After the annealing, the gate BV of the devices without graphene was 9.80 V whereas the devices with graphene broke down at 12.05 V. Figure 4.4(b) summarize the gate BV or maximum gate bias versus V_{TH} for *p*-GaN gate HEMTs fabricated by several groups. Compared with other reported *p*-GaN gate HEMTs, our devices with graphene insertion exhibit the highest gate BV and a relative high V_{TH}. These improvements are crucial for *p*-GaN gate HEMT devices for power switching applications.

To get further insights into the role of graphene on Ti/*p*-GaN interfaces, scanning transmission electron microscopy (STEM) images of the HEMTs were obtained. As shown in Figure 4.5, the Ti/*p*-GaN interface quality was much improved by the insertion of graphene. Both Figure 4.5(d) and (e) are EDS data from small dark regions at the Ti/*p*-GaN or Ti/graphene/*p*-GaN interfaces, which are likely TiN compounds considering the contract difference with Ti. In Figure 4.5(a), at the Ti/*p*-GaN interface, there are many small TiN regions indicated by the arrows, and a void exists illustrated by the very low EDS signal intensity shown in Figure 4.5(c). In Figure 4.5(b), at the Ti/graphene/*p*-GaN interface, there are much less TiN regions and no voids, suggesting a more stable and cleaner interface with the use of graphene.

This means that the graphene interlayer helped to reduce the formation of TiN and interface voids and maintain a more stable Ti/graphene/*p*-GaN interface during annealing, contributing to a lower leakage current and a higher gate BV.

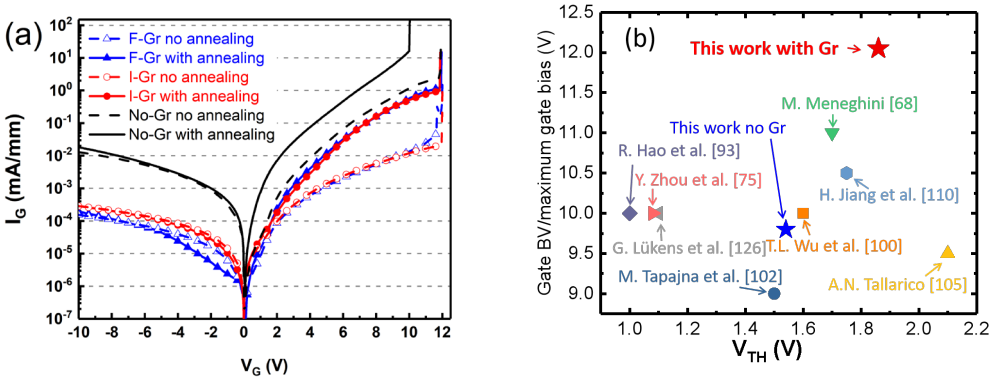


Figure 4.4 (a) Comparison of the gate leakage current and gate breakdown voltage before and after 350 °C 5 min annealing; (b) Gate BV or maximum gate bias versus threshold voltage for *p*-GaN gate HEMTs fabricated by several groups.

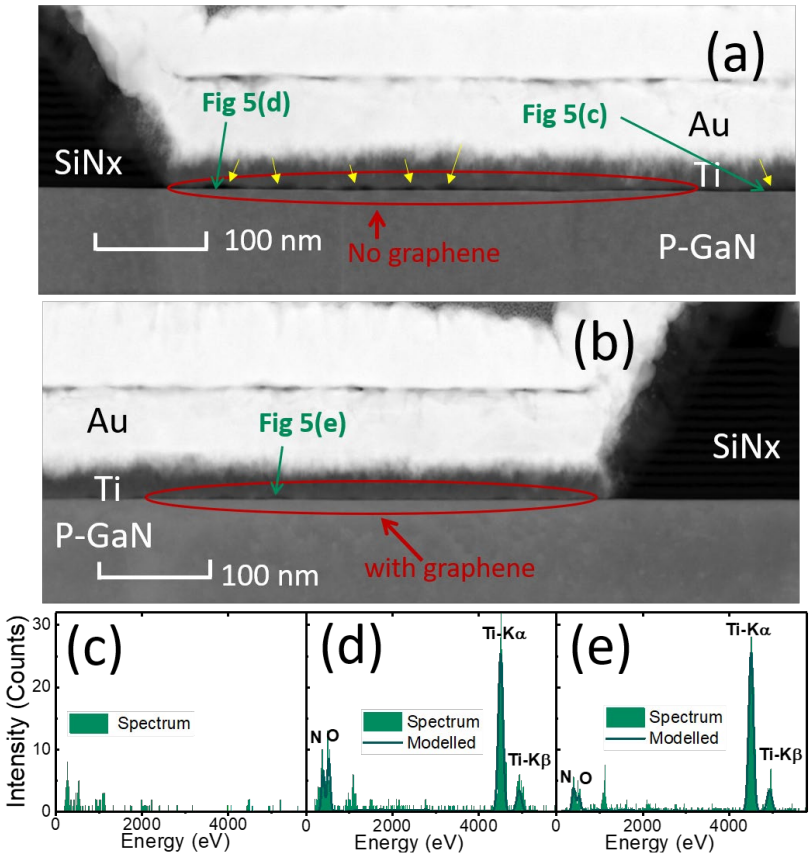


Figure 4.5 Cross-section STEM of the HEMTs after 350 °C 5 min annealing in the gate region (a) without graphene; (b) with I-graphene. The Au/Ti/*p*-GaN interface has been much improved by graphene. EDS shows that the darker regions in (a) are either (c) voids or (d) TiN; (e) EDS in the Ti/graphene/*p*-GaN interface as comparison.

4.4 Mechanism Study with Ti/graphene/*p*-GaN Schottky Diodes

Besides the material analysis, Au/Ti/graphene/*p*-GaN Schottky contacts have been fabricated as seen in the inset of Figure 4.6(a). Considering the fact that the I-graphene and F-graphene had similar effects in the previous experiments, only I-graphene was studied here. This test structure consists of two Schottky contacts back-to-back [127]. The I–V measurements were carried out in the bias range of 0 to 6 V. Before annealing, the systems with and without I-graphene have comparable current density, whereas they are significantly different after 350 ºC 5 minutes annealing.

The temperature dependence of the I-V characteristics has also been studied for these systems to extract Φ_B. Taking the Mg doping concentration of 4×10^{19} cm^{-3} into consideration, the value of E_{00}/kT is in the range between 0.85 and 1.34 in the examined temperature range. This implies that thermionic field emission (TFE) should be the dominant mechanism in our systems. Hence, the expression of the TFE reverse current was used to fit our experimental data [66], [128]

$$I_s = \frac{A_c A^* T \sqrt{\pi E_{00}}}{k} \cdot \sqrt{q(V - V_n) + \frac{q\Phi_B}{cosh^2(\frac{E_{00}}{kT})}} \cdot exp\left(-\frac{q\Phi_B}{E_{00}\, coth\left(\frac{E_{00}}{kT}\right)}\right) \tag{4.1}$$

$$I_{TFE} = I_s \cdot exp\left(\frac{qV}{kT} - \frac{qV}{E_{00}\, coth\left(\frac{E_{00}}{kT}\right)}\right) \tag{4.2}$$

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_A}{m^*\varepsilon}}, \tag{4.3}$$

where V is the applied voltage, A_c is the contact area, A^* is the Richardson constant, q is the elementary charge, k is the Boltzmann constant, h is Planck's constant, T is the absolute

temperature, and ε and m^* are the dielectric constant for GaN and the effective mass for holes, respectively. Φ_B represents the Schottky barrier height of the metal/(graphene)/*p*-GaN interface. In our calculation, we used the values of $\varepsilon = 8.9\ \varepsilon_0$, $A^* = 27.9\ A/cm^2K^2$, and $m^* = 0.81\ m_0$.

The extracted Φ_B from the data (Figure 4.6(b)) is 2.08 eV for the contacts without graphene and 2.09 eV for those with I-graphene, respectively. After annealing the sample at 350 °C in N_2 for 5 min, Φ_B decreased to 1.65 eV (no Gr) and 1.89 eV (with Gr), which results in approximately one order of magnitude smaller current in the sample with graphene. The extracted Φ_B are summarized in Table II. These data are consistent with the experimental value reported in the literature for Ti/*p*-GaN interfaces [66].

It is worth mentioning that this back-to-back Schottky diode experiment was conducted on *p*-GaN wafer without any passivation or etching process. The metal/*p*-GaN interfaces in a HEMT can be more defective due to the ion bombardment during the fabrication process (e.g. passivation deposition and gate dielectric etching).

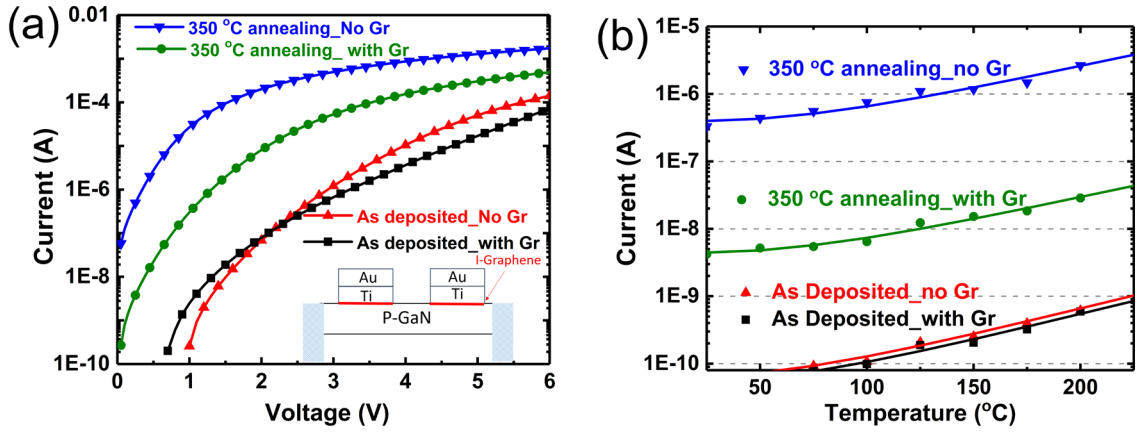


Figure 4.6 (a) I-V characteristics acquired from the back-to-back diodes. Inset: Schematics of the sample structure; (b) Temperature dependence of the current measured at V = +0.2 V in back-to-back Schottky contacts. The symbols are measured data. The lines are the fitting curves.

4.5 Analysis and Modeling of Gate Leakage Current

In this part, the frequency dependent capacitance-voltage (C-V) profiles of the devices with and without graphene will be discussed. Then, the gate current characteristics in Figure 4.4(a) and the corresponding mechanism will be analyzed more thoroughly. The data will be fitted to a physical model from Ref. [129]. The trap depth and the corresponding prefactors of the HEMTs with/without graphene will be extracted.

As illustrated in Figure 4.7(a), the gate-source C-V curves of the devices with graphene are relatively stable when the frequency varies from 2 MHz to 50 kHz while the capacitances of the devices without graphene increase more significantly with the decrease in the measurement frequency (Figure 4.7(b)), suggesting the existence of more interface states at the Ti/*p*-GaN interface. As shown in Figure 4.7(c), the gate structure includes two junctions, i.e. the metal (graphene)/*p*-GaN junction (Schottky junction) and the *p*-GaN/AlGaN/GaN junction (p-i-n junction). The gate leakage mechanisms are different in different gate bias regimes.

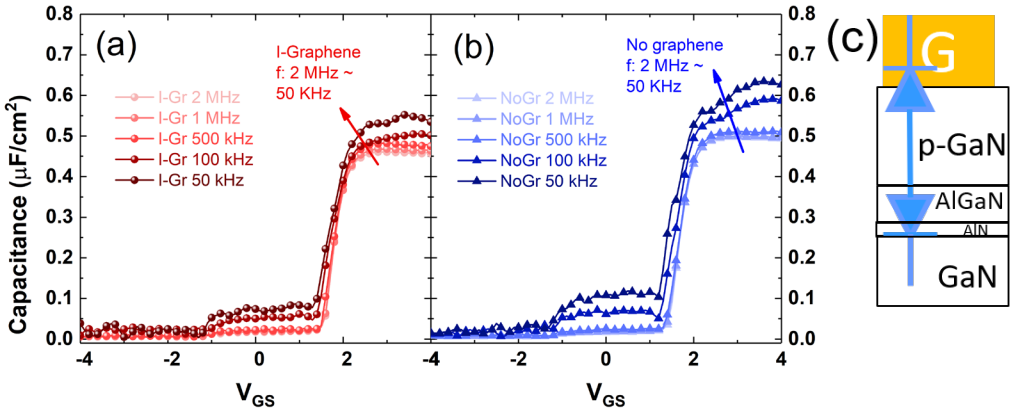


Figure 4.7 Frequency-dependent C-V profiles of the devices (a) with graphene and; (b) without graphene; (c) schematic representation of the *p*-GaN gate region and its equivalent circuit.

In the $V_G < 0$ regime, vertical gate current is blocked due to the reverse bias of the p-i-n junction. An electron current is likely from the Schottky metal near the gate edges through a leakage path along the *p*-GaN sidewall and these electrons are emitted into the 2DEG layer. As shown in Figure 4.4(a), the I_G with/without graphene at reverse bias had negligible change after annealing even though the Schottky barrier changed. This further confirms that the dominant factor for I_G at the negative bias is associated with the surface defects introduced during the fabrication process. A similar conclusion has also been reported for previous *p*-GaN gate HEMTs [117], [129]. According to Ref. [117], [129], the dominant gate leakage mechanism associated with *p*-GaN surface defects is found to be Poole-Frenkle emission (PFE) for the case of $V_G < 0$, which can be described by:

$$J = C\,E \exp\left(-\frac{q\left(\Phi_t - \beta\sqrt{E}\right)}{kT}\right), \qquad (4.4)$$

where $C = qn\mu_n$, $\beta = \sqrt{q/\pi\epsilon}$ is the Schottky factor, k is Boltzmann's constant, $q\Phi_t$ is the trap depth, and $E = V_{GS}/L_{GS}$ is the electric field, with L_{GS} being the shortest distance between the gate and source metal.

The temperature dependent I_G-V_G of the HEMTs after annealing have been measured from 300 K to 450 K. The PFE model has been used to fit the data in the negative bias regime, with the trap depth $q\Phi_t$ and prefactor C as the fitting parameters. The fitting results are illustrated in Figure 4.8, where the fitting curves are plotted as solid lines and symbols represent selected measurement points. The trap depths are $q\Phi_{t,I-Gr} = 0.199$ eV and $q\Phi_{t,no-Gr} = 0.165$ eV, respectively. The prefactor C in the HEMTs without graphene is $\frac{C_{no-Gr}}{C_{I-Gr}} = \frac{585.70}{47.46} = 12.34$ times of that with I-

graphene. This explains why I_G in the HEMTs with/without graphene differ a lot in the as-deposited case even though their Φ_B are comparable extracted in Section 4.4. Graphene layers passivated the *p*-GaN surface resulting in the neutralization of interface states and, consequently, less electron leakage toward the gate foot along the *p*-GaN surface.

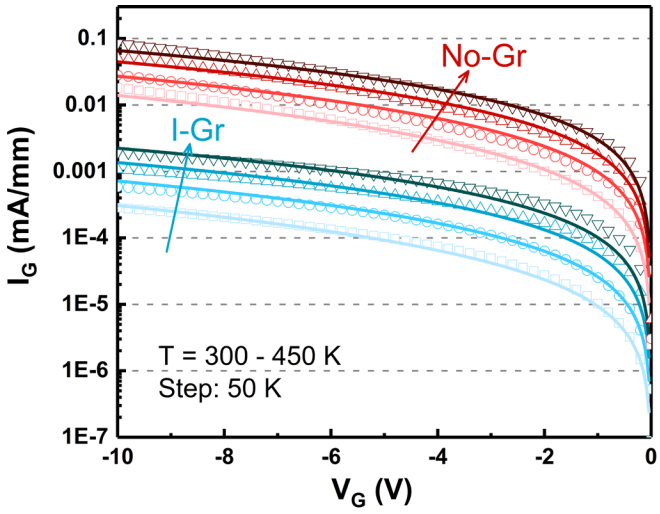


Figure 4.8 Negative gate bias current from T = 300 to 450 K measured on HEMTs with I-graphene and without graphene. The symbols are selected measured data. The lines are the fitting curves using the PFE model.

		As Deposited	350 °C 5 min annealing
Φ_B (eV) in diodes	With I-graphene	2.08	1.89
	No graphene	2.09	1.65
Φ_t (eV) in HEMTs	With I-graphene	\	0.199
	No graphene	\	0.165
C (Ω^{-1}) in HEMTs	With I-graphene	\	4.75×10^{-8}
	No graphene	\	5.86×10^{-7}

Table 4.2 Summary of the gate current modelling of the back-to-back diodes and the HEMTs.

In the $V_G > 0$ regime, the p-i-n junction will be positive biased while the Schottky junction will be reverse biased. In the case of no-annealing, it is found that the I_G are comparable in the regimes of positive and negative gate biases in Figure 4.4(a). We deduce that the vertical gate current is also small since the Schottky barrier is large enough. The graphene contributes to a lower gate leakage by reducing the interface defects similar to the $V_G < 0$ regime. For devices after annealing, the gate leakage current under a positive bias is much larger than that under a negative bias. The dominant current shall be from the vertical gate current due to a lower $\Phi_B$in the Schottky junction. The voltage dropped at the p-i-n junction is large enough to turn on the diode and the dominant conduction mechanism is found to be thermionic field emission. Thus, graphene helps to reduce the gate leakage current by maintaining a more stable interface and a higher Φ_B after annealing as analyzed in Section 4.4.

Based on these evidences, it can be deduced that graphene can help to reduce the interface defects, prevent the Ti/*p*-GaN reaction and maintain a more stable Au/Ti/*p*-GaN interface during annealing. In $V_G > 0$ regime, the larger Φ_B contributes to a lower gate leakage current and the higher V_{TH}. Graphene can also prevent the decrease of gate BV during annealing. In the $V_G < 0$ regime, as the defects at the *p*-GaN surfaces during the fabrication process are the dominant factor for gate leakage, graphene reduces the gate leakage by saturating the defects at the *p*-GaN surface. According to fitting the experimental data, it is found that graphene changes the trap depth $q\Phi_t$ from 0.165 eV to 0.199 eV and reduces the prefactor C by 12.3 times.

4.6 Chapter Summary

In this work, intrinsic and fluorinated graphene were investigated as gate insertion layers in normally-off *p*-GaN HEMTs, which formed Au/Ti/graphene/*p*-GaN interfaces in the middle and Au/Ti/graphene/SiN_x on the two sides. 50 times larger I_{ON}/I_{OFF} ratios, 0.30 V higher V_{TH} increase, 50 times off-state gate leakage reduction have been achieved by the insertion of graphene. 12.1 V gate BV has been achieved with I-graphene for Schottky gate *p*-GaN HEMTs. This is considered to be the result of a 0.24 eV higher Φ_B, the suppression of Ti/*p*-GaN reaction and the better graphene/*p*-GaN interfaces. In the negative gate bias regime, I_G has been fitted to PFE model, which revealed that graphene layers contribute to a 0.034 eV larger trap depth and a 12.3-time smaller prefactor. As single-layer graphene can be prepared in wafer-size areas [130], this approach is mass-production compatible and very effective in improving the I_{ON}/I_{OFF} ratios and increasing V_{TH} and gate BV of *p*-GaN gate HEMTs.

Chapter 5: Formation of Ultra-High-Resistance Au/Ti/*p*-GaN Junctions and the Applications in AlGaN/GaN HEMTs

In this chapter, we report a dramatic current reduction, or a resistance increase, by a few orders of magnitude of two common-anode Au/Ti/*p*-GaN Schottky junctions annealed within a certain annealing condition window (600-700 ºC, 1-4 min). Results from similar common-anode Schottky junctions made of Au/*p*-GaN, Al/Ti/*p*-GaN and Au/Ti/graphene/*p*-GaN junctions demonstrated that all the three layers (Au, Ti and *p*-GaN) are essential for the increased resistance. This high-resistance junction structure was further employed in *p*-GaN gate AlGaN/GaN HEMTs, and was demonstrated to be useful to reduce the gate leakage currents and improve the gate BV in HEMTs due to its high-resistance [131], [132].

Besides power HEMTs, GaN-based devices have been very promising for a wide range of semiconductor device applications, including UV detectors , radio frequency (RF)/microwave electronics [84], [133], gas sensors [134], [135], and high speed and high-power electronics [32]. GaN-based light-emitting diodes (LEDs) and laser diodes (LDs) have already been commercialized for a variety of lighting and display applications [77], [136].

Metal/*p*-GaN junctions are essential in many of these electronic devices. For example, low-resistance and transparent ohmic metal contacts to *p*-GaN are crucial to improve current injection and light extraction efficiency of GaN-based LEDs. For *p*-channel GaN-based transistors, thermally stable and low-resistance ohmic metal/*p*-GaN contacts are highly desired, where Ni-metals are most widely used for its high work function [77], [137]. Meanwhile, for HEMTs with *p*-GaN gate, Schottky type metal/*p*-GaN gate with high Schottky barrier height is preferred to

reduce the gate leakage current and increase the threshold voltage. Ti- or TiN- based metal electrodes are usually adopted due to their low work functions [65], [105]. Even though Ti/Al or Ti/Au metal stacks have been widely used as the *p*-GaN gate metals [65], [66], the impact of metal/*p*-GaN junctions on the HEMTs' performance parameters such as the V_{TH} and the gate BV has seldom been investigated. Only a handful of recent papers discussed the influence of the different metals and fabrication processing conditions on the HEMTs performances. G. Greco et al. demonstrated that the HEMTs with Ti/Al gate showed a considerable high leakage current when subjected to 800 ºC 1 min annealing [66]. The importance of the metal contacts on *p*-GaN still deserves further investigation to optimize the performances of these electronic devices.

In this chapter, we present a detailed investigation of Au/Ti/*p*-GaN junctions, focusing on the impact of annealing thermal budget on the resistance of these junctions. We report that ultra-low current, i.e., ultra-high resistance, can be achieved using Au/Ti/*p*-GaN processed within a particular window, which is contrary to the observations in Ref. [66], [138]. Au/*p*-GaN, Al/Ti/*p*-GaN and Au/Ti/graphene/*p*-GaN junctions were also studied to investigate the current reduction mechanisms. The Au/Ti/*p*-GaN junction were characterized by cross-sectional scanning-transmission electron microscopy (STEM) and Raman spectroscopy. Moreover, this Au/Ti/*p*-GaN scheme has been used in *p*-GaN gate HEMTs to investigate its benefits in device performance. Compared to the conventional metal gate without annealing, the devices with optimized Au/Ti/*p*-GaN gate have shown superior gate breakdown voltages with little changes on the threshold voltages or the sub-threshold slopes.

5.1 Common-Anode Au/Ti/*p*-GaN Schottky Contacts

The 100 nm *p*-GaN/15 nm AlGaN/0.7 nm AlN/GaN buffer epitaxial structures used in the experiments were grown on (111) Si substrates by metal-organic chemical vapor deposition (MOCVD) provided by Enkris Semiconductor Inc. The *p*-GaN layers were doped with Mg to a concentration of 4×10^{19} cm^{-3}. As seen in Figure 5.1, the test structure consists of two common-anode Schottky junctions in series at a distance of 20 µm, with one being forward-biased and the other being reverse-biased [128], [139]. Prior to the metal deposition, the *p*-GaN surfaces were thoroughly cleaned using acetone, ethanol, 1: 4 HCl: H_2O, and then rinsed in DI water with each step lasted for 10 minutes. Au/Ti (100nm/40 nm) layers were deposited by the e-beam evaporator mentioned above and were patterned by a lift-off technique. The metals featured a width of 100 µm and a length of 25 µm. To investigate the annealing effect, the samples were annealed at 400, 500, 600, 700 and 800 °C respectively for 1 min in an N_2 ambient using Rapid Thermal Process (RTP) by an Annealsys AS-one 150 system.

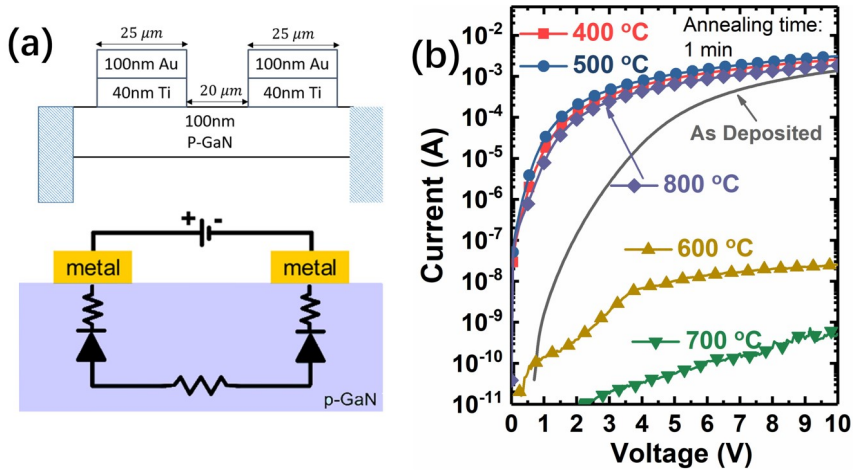


Figure 5.1 (a) Schematics of the investigated common-anode Au/Ti/*p*-GaN Schottky contacts, the measurement setup and its equivalent circuit. (b) I-V characteristics of the common-anode Au/Ti/*p*-GaN Schottky contacts with different thermal annealing conditions: the plain solid line is from the as-deposited sample, and the solid lines with symbols are from the samples annealed at 400 to 800 °C for 1 min.

Current-voltage (I–V) measurements were carried out in the bias range of -10 to 10 V. Figure 5.1(b) shows the I-V characteristics of the two common-anode junctions with and without annealing. The data from -10 to 0 V are not presented due to the symmetry of the I-V curves. As the reverse-biased junction has a much larger resistance than the forward-biased junction, the I-V behavior is determined by the reverse-biased junction, which is the junction on the left in Figure 5.1(a). Annealing commonly leads to a higher current due to the lower Schottky barrier height [66], [138]. Indeed, the I–V measurements showed an increase in the current after the annealing at 400 ºC or 500 ºC, which was as expected. However, when the annealing temperature reached 600 ºC, the current decreased significantly by approximately five orders of magnitude. If the annealing temperature further increased to 700 ºC, the current would further drop (< 10^{-9} A). More interestingly, when the annealing temperature was 800 ºC, the current increased to a level comparable to the case of 500 ºC annealing. In summary, the resistance of this metal/*p*-GaN junction was found to have a very unusual dependence on the annealing temperature.

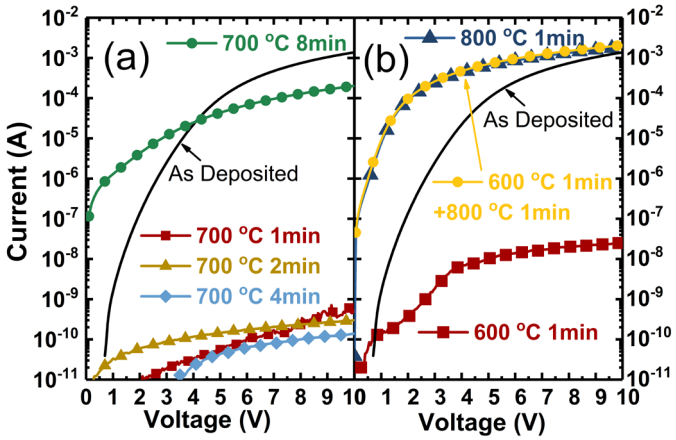


Figure 5.2 I-V characteristics in Au/Ti/*p*-GaN Schottky contacts, (a) for the samples annealed at 700 °C from 1 min to 8 min; (b) for the sample annealed at 600 ºC for 1min followed by 800 ºC 1 min annealing.

To further investigate the current dependence on the annealing thermal budget, some samples were annealed for 1-8 min at T = 700 ºC. As shown in Figure 5.2, the current remained considerably low when the annealing time ranged from 1-4 min, whereas it was back to Schottky-like behavior when the annealing time was 8 min. Furthermore, for the sample annealed at 600 ºC for 1 min, the current surged significantly after a second annealing step at 800 ºC for 1 min, which was finally equivalent to the case of 800 ºC 1 min annealing only. These data demonstrate that the I-V characteristics of the Au/Ti/*p*-GaN Schottky contacts are highly dependent on the annealing temperature and time. Within a certain process window, the Au/Ti/*p*-GaN contacts can be highly resistive. Specifically, after 700 ºC 1-4 min annealing, the current across the Schottky contacts is around six orders of magnitude lower than that in as-deposited contacts at V = 5V.

5.2 Common-Anode Metal/*p*-GaN Schottky Contacts For Comparison

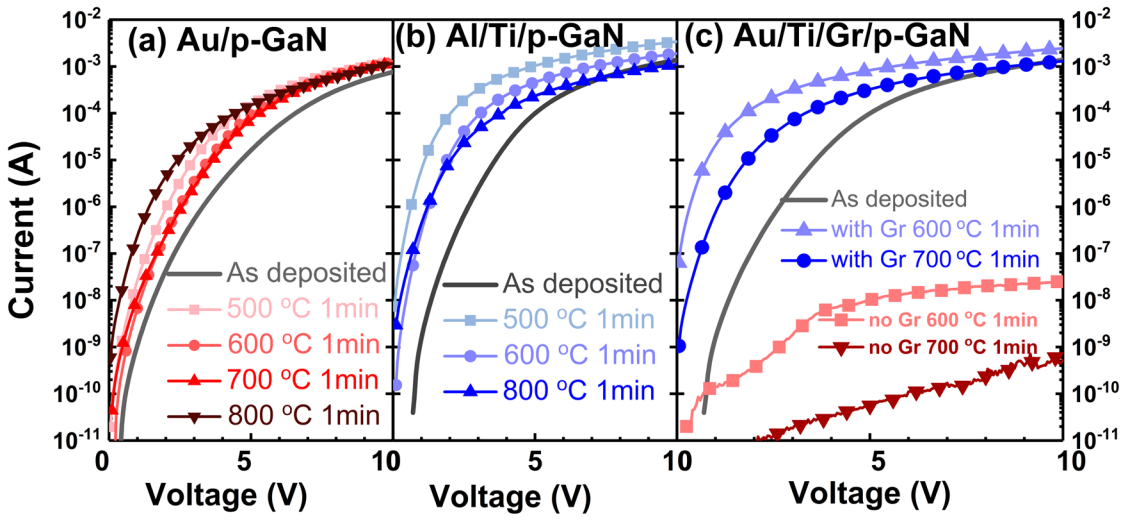


Figure 5.3 I-V characteristics of the common-anode *p*-GaN Schottky contacts with different metals, (a) Au/*p*-GaN; (b) Al/Ti/*p*-GaN; (c) Au/Ti/graphene/*p*-GaN (Au/Ti/Gr/*p*-GaN) compared with Au/Ti/*p*-GaN.

Common-anode diodes with Au/*p*-GaN (no Ti) and Al/Ti/*p*-GaN (no Au) contacts were also fabricated and annealed at 500 to 800 °C for 1 min for comparison. Current reduction after annealing was not observed in either case, as shown in Figure 5.3(a) and 3(b). The testing results are consistent with literature data that the annealing treatments will result in a higher current due to a lower metal/*p*-GaN barrier. Thus, we can deduce that both Ti and Au are necessary to form the high-resistance junction. To assess the role of the *p*-GaN in this process, graphene was inserted between Ti and *p*-GaN as a diffusion barrier. The strong sp2 hexagonal bonding of graphene can act as a strong barrier to atom diffusion and has been utilized as a diffusion barrier in many applications [140-143]. Figure 5.3(c) compares the contact of Au/Ti/graphene/*p*-GaN (Au/Ti/Gr/*p*-GaN) and Au/Ti/*p*-GaN with and without annealing. The current in the as-deposited samples with and without graphene were comparable. After annealing at 600 °C or 700 °C for 1 min, the current in the contact with graphene further increased, contrary to the sample without graphene. The fact that the graphene barrier layer between the metals and *p*-GaN can prevent the current decrease demonstrates that *p*-GaN is also essential to form the high-resistance junction.

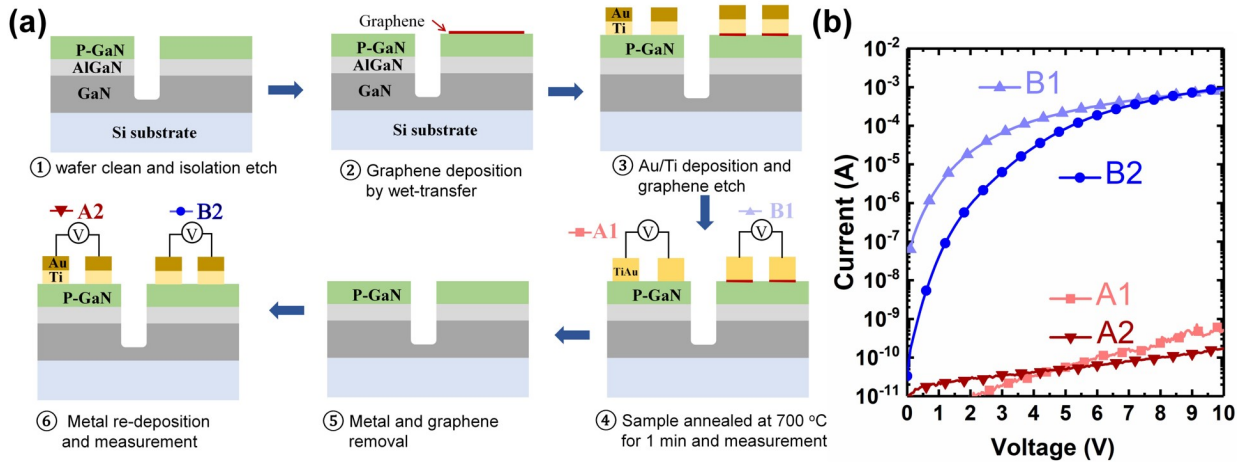


Figure 5.4 (a) Schematics of the process flow of the metal re-deposition experiment; (b) I-V characteristics of the Au/Ti/(graphene)/*p*-GaN Schottky contacts with metal re-deposition.

5.3 Analysis of the Mechanism by Metal Re-deposition

To identify the critical location and analyze the formation mechanism of the high-resistance junction, a metal re-deposition experiment was designed and conducted as illustrated in Figure 5.4(a). The idea was to measure I-V of the diodes with the original annealed Au/Ti/*p*-GaN (A1), remove the metal layers, redeposit new Au/Ti metals, and then measure the I-V of the new Au/Ti/*p*-GaN common-anode diodes (A2). This should reveal the role of the Au/Ti metals. Original Au/Ti/Gr/*p*-GaN diodes (B1) and new Au/Ti/*p*-GaN diodes (B2) were also fabricated on the same wafer and measured for comparison as graphene served as a barrier layer between Au/Ti and *p*-GaN.

Single-layer graphene grown by chemical vapor deposition (CVD) on Cu foils was transferred to part of the *p*-GaN sample surface via the "polymethyl methacrylate (PMMA)-mediated" wet-transfer approach [123], [142]. After the deposition and patterning of 100 nm Au/40 nm Ti, graphene was etched by O_2 plasma using the patterned metals as the self-aligned mask. The sample was annealed at 700 ^oC for 1 min and then I-V measurement was performed on the common-anode diodes without and with graphene (A1 and B1). To completely remove the metals and graphene, the sample was first cleaned by acid, then exposed to O_2 plasma to remove the graphene. Before the re-deposition of Au/Ti, the sample was again cleaned with acid to remove the oxidation layer or any metal residuals. As shown in Figure 5.4(b), the I-V characteristics of the common-anode diodes with the new Au/Ti layers (A2 and B2) were similar to their counterparts with the original Au/Ti (A1 and B1), which indicated that the metal layers are not the key regions to the drastic resistance change. Instead, the high-resistance regions should locate in the *p*-GaN layers that were annealed in contact with Au/Ti without the graphene barriers. One possible

explanation is that the Au/Ti layers can deactivate the Mg in GaN by forming an electrically inactive complex with Mg within this annealing window.

5.4 Material Characterization of the High-resistance Junction

To get further insights into the Au/Ti/*p*-GaN junctions, STEM images were obtained for the Au/Ti/*p*-GaN and Au/Ti/graphene/*p*-GaN diodes with 700 ºC 1 min annealing. As shown in Figure 5.5(a) and 5(b), Ti has diffused into Au. Besides, TiN has formed between the Ti/*p*-GaN interfaces confirmed by energy-dispersive spectroscopy (EDS). However, significant morphology difference that may explain the current reduction phenomenon were not found in the STEM. The samples with and without graphene after annealing have no significant differences according to the EDS analysis.

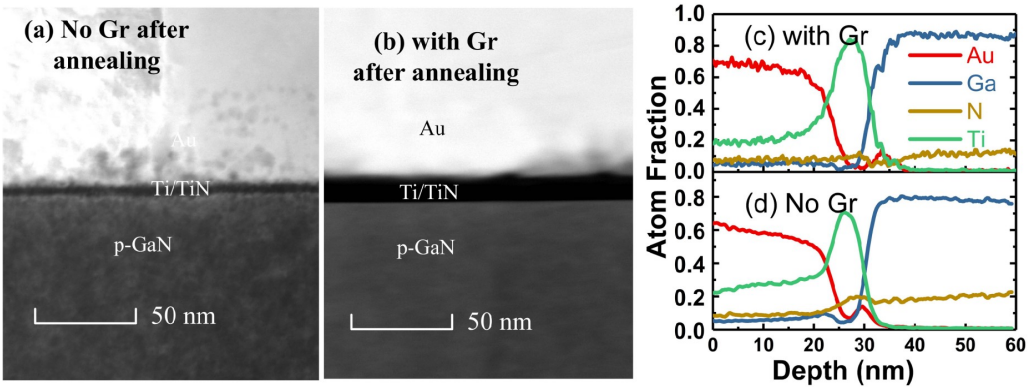


Figure 5.5 Cross-section STEM of the samples after 700 ºC 1 min annealing in N_2: (a) Au/Ti/*p*-GaN and (b) Au/Ti/graphene/*p*-GaN. (c) EDS of the Au/Ti/graphene/*p*-GaN after annealing; (d) EDS of the Au/Ti/*p*-GaN after annealing.

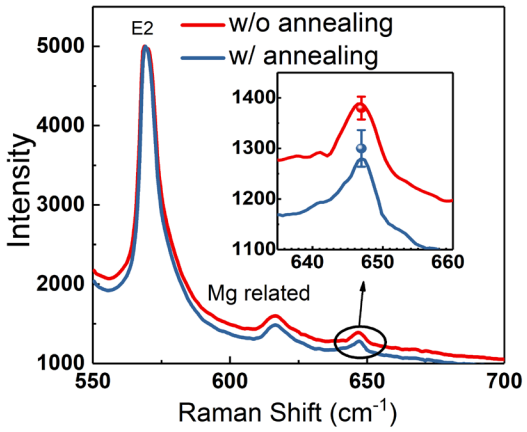


Figure 5.6 Raman spectra of the *p*-GaN with/without Au/Ti annealing; Inset: zoom-in of the Mg-related peak.

Hall measurements were performed on the Au/Ti/*p*-GaN samples with 700 ºC 1 min annealing and without annealing using the van der Pauw method. It was shown that the hole concentration has reduced from 8×10^{17} cm^{-3} to below 5×10^{15} cm^{-3} in the *p*-GaN sample after annealing. Due to the high resistance measured on this sample, it is difficult to make an accurate evaluation of the hole concentration by this method, which requires more dedicated research. Thus, it's reasonable to attribute the current reduction to the hole concentration reduction in the *p*-GaN due to the annealing in contact with the Au/Ti layers. Raman microscopic spectra were observed at room temperature using a 532 nm laser for excitation. Figure 5.6 presents the Raman spectra of the *p*-GaN sample with and without Au/Ti annealing. For the *p*-GaN sample with Au/Ti annealing, the metals have been completely removed by acid before the Raman characterization to avoid the reflection of the laser. The sharp peak at 569.2 cm^{-1} is ascribed to GaN E2 peak; and the peak at 646 cm^{-1} is ascribed to the local vibration mode of Mg-N bonding [144], [145]. The spectra are normalized by the peak intensity of the E2 (569.2 cm^{-1}) mode and shifted vertically for comparison. It's shown that the Mg-N mode peak has decreased in the sample with Au/Ti annealing. Raman characterization were performed at five different positions to acquire statistical data. As illustrated

in the inset of Figure 5.6, the peak intensity of the Mg-N mode in the sample with Au/Ti annealing is 5.7% lower than the sample without annealing on average. Considering the Raman measurement noises and errors, the intensity differences of the Mg-N vibration related peaks are not significant. Future work on the mechanism needs to be conducted.

5.5 The Applications in AlGaN/GaN HEMTs

The technology of achieving high-resistance metal/*p*-GaN junctions conveniently by thermal annealing and with high repeatability is very promising for applications in GaN-based devices consisting of metal/*p*-GaN Schottky contacts (e.g., *p*-GaN gate HEMTs, ultraviolet Schottky barrier photodetectors). To demonstrate the application of this technology, we fabricated HEMTs with Au/Ti/*p*-GaN as the gate structure.

The *p*-GaN gate HEMTs were fabricated on 100 nm *p*-GaN/15 nm $Al_{0.2}Ga_{0.8}N$/0.7 nm AlN/4.5 μm GaN/Si epi-structures. Figure 5.7(a) shows the schematic cross-section of the devices. The fabrication flow started with *p*-GaN gate definition by a Cl-based plasma etching, followed by a Cl_2/BCl_3 plasma etching to form mesas and isolate the devices. After the deposition of Al_2O_3 as the passivation layer by ALD, the source/drain (S/D) ohmic contacts were formed by Ti/Al/Ti/Au (20/110/40/50 nm) deposition and annealing. After the gate window opening and the deposition of gate metal (150 nm Au/40 nm Ti), the sample was divided into two groups. One group of HEMTs were annealed at 700 °C in N2 for 1 min, and the other group didn't have any gate metal annealing.

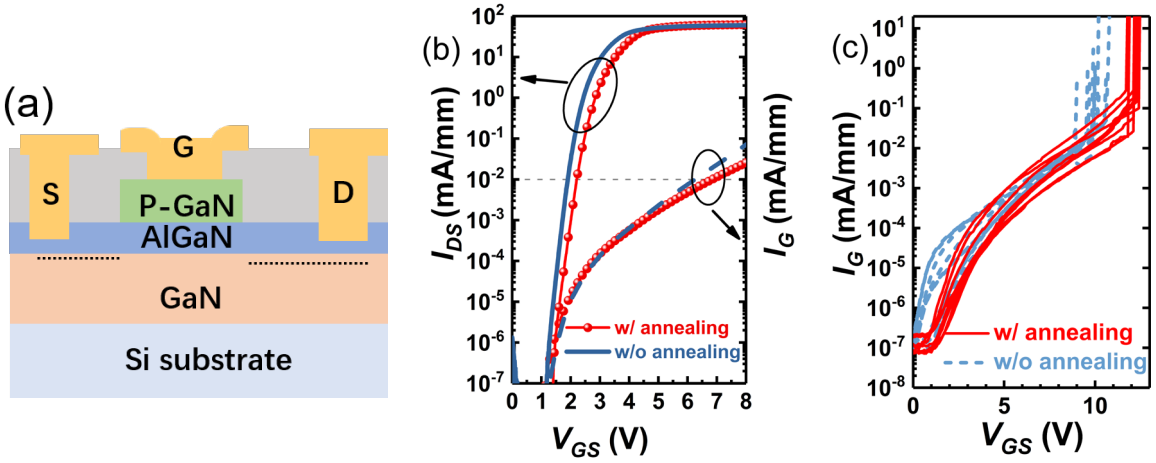


Figure 5.7 (a) Cross-sectional schematics of the *p*-GaN gate HEMTs structure; (b) transfer characteristic of the HEMTs with or without gate metal annealing, and; (c) gate leakage characteristic and gate breakdown voltage, ten devices for each.

The transfer characteristics of the HEMTs with or without Au/Ti gate contacts annealing are shown in Figure 5.7(b). The annealing process step has little impact on the transfer characteristics and gate leakage characteristics of the HEMTs. Since the active *p*-doping concentration is only reduced in the region close to the Schottky interface with the metal, it has a limiting impact on threshold voltage and gate leakage, which are dominated by *p*-GaN/AlGaN/GaN junction [107], [146]. On the other hand, a clear impact of the annealing process can be observed on the gate breakdown voltages as illustrated in Figure 5.7(c). When a positive bias is applied on the gate, and the Schottky metal/*p*-GaN junction is reverse biased. The reduction of the active doping concentration close to the Schottky junction promotes a wider depletion region. Thus, the maximum electric field is lower after the annealing process, resulting in an increase of the average of gate breakdown voltage from 9.9 to 12.1 V. A similar effect has been observed in Ref. [107], where a Mg compensation process has been adopted to reduce the hole concentration close to the Schottky interface. It was shown that the reduction of hole in this region can influence the gate breakdown voltage without altering the threshold voltage, trans-conductance and sub-

threshold slope. This further confirms our assumption that the high-resistance junction results from the formation of Au/Ti-Mg complexes during the annealing process, which reduces the hole concentration in *p*-GaN layer close to the metal.

5.6 Chapter Summary

In summary, we observed a significant leakage current reduction in Au/Ti/*p*-GaN Schottky diodes within a specific annealing window (600-700 ºC, 1-4 min), which has not been reported for metal/*p*-GaN junctions. By comparing the Au/*p*-GaN, Al/Ti/*p*-GaN and Au/Ti/graphene/*p*-GaN Schottky diodes, we inferred that all the three layers (Au, Ti and *p*-GaN) are essential for the formation of this high-resistance junction. Also, the high-resistance regions were formed in the *p*-GaN layer instead of the metal layers. The mechanisms of the Au/Ti/*p*-GaN high-resistance junction formation were further investigated by STEM, Hall and Raman measurements. It was concluded that the increased resistance might result from the decrease of activated Mg in *p*-GaN due to the Au/Ti annealing. This high-resistance junction structure has been employed in *p*-GaN gate HEMTs. The gate breakdown voltage was boosted from 9.9 to 12.1 V with negligible influence on the sub-threshold slope and threshold voltage. The finding of this high-resistance metal/*p*-GaN is promising for the GaN-based applications consisting of metal/*p*-GaN contacts.

Chapter 6: Enhanced Gate Reliability of *p*-GaN Gate HEMTs by Doping Engineering

In this chapter, we present a novel *p*-GaN gate HEMT structure with reduced hole concentration near the Schottky interface by doping engineering in MOCVD, which aims at lowering the electric field across the gate. By employing an additional unintentionally doped GaN (*u*-GaN) layer, the gate leakage current is suppressed and the gate breakdown voltage is boosted. Time-dependent gate breakdown measurements reveal that the maximum gate drive voltage increases. This method effectively expands the operating voltage margin of the *p*-GaN gate HEMTs without any other additional process steps.

Due to the relatively low gate breakdown voltage (BV) (usually 10-12 V), the maximum gate operation voltages ($V_{G\text{-}max}$) for *p*-GaN gate HEMTs are usually between 6-8 V [98], [99]. The reported $V_{G\text{-}max}$ of *p*-GaN gate HEMTs are generally estimated from the time-dependent gate breakdown (TDGB). While the V_{TH} is usually between 1 to 2 V and the gate turn-on voltage is suggested to be at 5 to 6 V for optimum dynamic R_{ON}, the small gate voltage swing has imposed significant constraints on the gate driver design and resulted in a lifetime reduction. Thus, it is highly desired to increase the gate BV and the $V_{G\text{-}max}$ for a wider gate drive window.

Several reliability studies focused on the *p*-GaN gate HEMTs have been carried out over the last few years [102]-[108], [147]-[151]. Different failure mechanisms have been proposed, including: i) metal/*p*-GaN Schottky junction breakdown, which is widely accepted and most likely to happen prior to others [105-107], [147], [148]; ii) the passivation/*p*-GaN sidewall related

breakdown, which is a bigger problem in self-aligned gate metal/*p*-GaN structure [115], [149]; and iii) *p*-GaN/AlGaN/GaN junction breakdown [102], [103]. Many researchers have been tackling the challenge with various methods [116], [110], [150], [151]. Zhou et al. [142] and Zhang et al. [150] adopted special treatments in the gate-stacks to enhance the *p*-GaN/metal Schottky junctions, where suppressed gate leakage currents and enhanced gate BV were achieved. An *n*-GaN/*p*-GaN/AlGaN/GaN epitaxial structure was proposed for gate reliability enhancement [151], where the Schottky junction was replaced by a metal-n-p junction. However, an activation of *p*-GaN after the gate etching is required. The high thermal budget can be detrimental to the AlGaN surface. Thus, a technique based on the commonly used *p*-GaN gate HEMT process would be favored owing to the process simplicity.

In this work, we demonstrated that a doping engineering method of using an additional *u*-GaN layer on top of *p*-GaN could effectively enhance the reliability of HEMTs without additional annealing step. TDGB measurements revealed that $V_{G\text{-}max}$ in the HEMTs with *u*-GaN increased to 10.6 V for a 10-year lifetime with a 1 % gate failure rate, which is much larger than the HEMTs without doping engineering (6.2 V). This *u*-GaN/*p*-GaN gate method neither impairs other electrical characteristics nor requires any extra process steps.

6.1 Device Structure and Fabrication

The *p*-GaN gate HEMTs were fabricated on 85-nm *p*-GaN/15-nm $Al_{0.2}Ga_{0.8}N$/0.7-nm AlN/4.5-μm GaN epi-structure grown by metal-organic chemical vapor deposition (MOCVD) on 2-inch Si (111) substrates from Enkris Semiconductor Inc, as shown in Figure 6.1(a). The *p*-GaN layer was doped with Mg to a concentration of 4×10^{19} cm^{-3}. Three device structure types, named

structure A, B and C, have been adopted, as illustrated in Figure 6.1(b). They have identical epi-structure and growth conditions except that structure B and structure C have additional epitaxial *u*-GaN layers on top of the *p*-GaN grown by MOCVD, which was used to reduce the hole concentration in the region close to the Schottky interface with the metal, thus widening the depletion region and reducing the maximum electric field in the GaN gate. The thickness of *u*-GaN were 20 and 30 nm for structure B and structure C, respectively. Due to the memory effect and diffusion of Mg, the *u*-GaN layers should be slightly p-type doping [152].

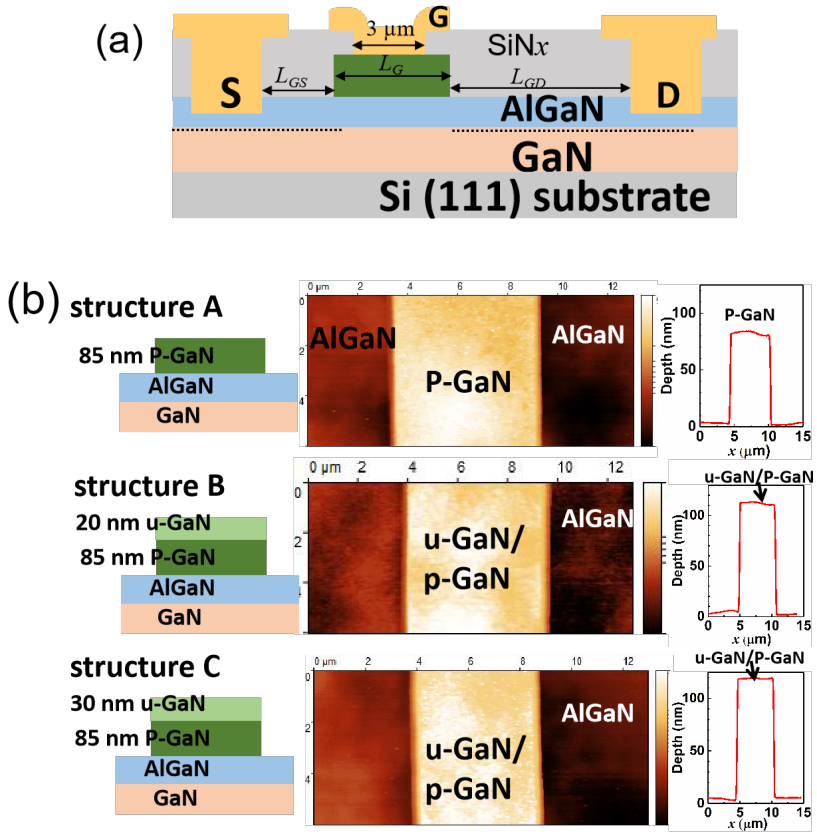


Figure 6.1 (a) Cross-sectional schematics of the *p*-GaN gate HEMTs; (b) Schematics of the gate structure A, B, C after the gate definition by *u*-GaN/*p*-GaN etching (left column) and their corresponding AFM characterization results (middle column), and their extracted profiles (right column).

The fabrication process was described in detail in Chapter 2. Devices with structure A, B and C have an identical fabrication process except that B and C have longer GaN etching times. Thanks to the high-selectivity and low etching rate of the etching recipe, a smooth AlGaN surface with low etching damages has been obtained for all three structures (Figure 6.2(b)). The devices tested feature a W_G of 100 μm, a L_G of 5 μm, a L_{GS} of 5 μm, and a L_{GD} of 15 μm. The relatively longer L_{GS} compared to literature is to suppress the gate breakdown induced by the passivation/*p*-GaN sidewall [107], [115].

6.2 Static Performance and Temperature Dependence

Figure 6.2(a) depicts the transfer characteristics of the devices with structure A, B, and C. All devices exhibit a V_{TH} of ~ 2.1 V (defined at I_D = 0.01 mA/mm), and an I_{ON}/I_{OFF} ratio larger than 10^8. Figure 6.2(b) and (c) show the output characteristic of devices with structure A and C, in both of which a R_{ON} of 22 Ω·mm is obtained. These results show that the doping engineering has a negligible effect on the conducting characteristic (e.g., R_{ON} and V_{TH}), which is consistent with [107], [150]. Meanwhile, a clear impact can be observed on the gate leakage characteristics as shown in Figure 6.2(a) and Figure 6.3(a). Under a forward bias, the gate leakage current is dominant by the metal/GaN Schottky junction [107]. Owing to the reduced acceptor doping concentration in *u*-GaN, B and C show a lower gate leakage under forward bias.

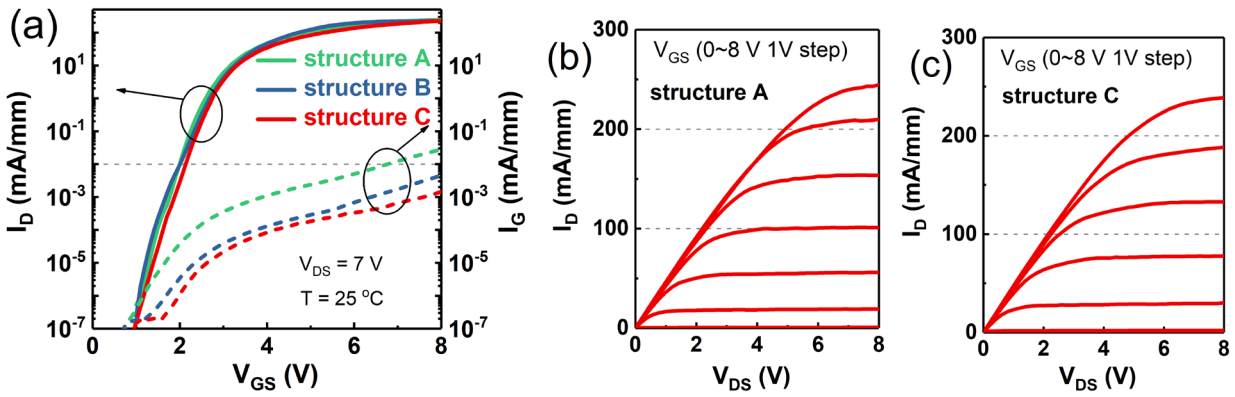


Figure 6.2 (a) Transfer characteristic of the devices with structure A, B, and C; (b) output characteristic of A; (c) output characteristic of C.

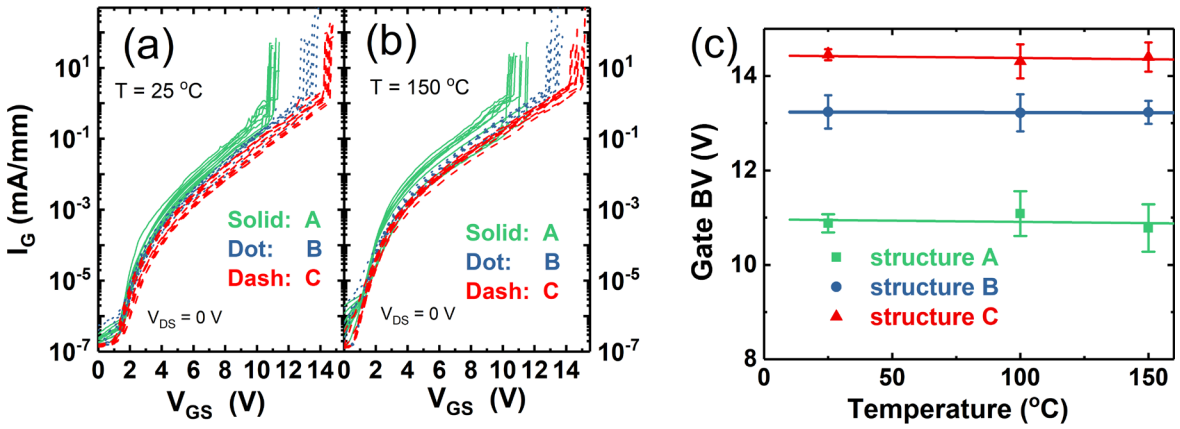


Figure 6.3 (a) Gate leakage and breakdown characteristics of the devices with structure A, B and C at 25 °C, and; (b) at 150 °C; (c) the BV of different structures and their temperature dependences.

Figure 6.3(a) and (b) compares the forward gate breakdown characteristics of A, B and C measured at 25 °C and 150 °C, respectively. The breakdown mechanism was determined to be Schottky junction failure [148]. Compared to A, the additional *u*-GaN layer in B has effectively boosted the BV from 10.9 V to 13.2 V at 25 °C. For C with a thicker *u*-GaN layer, the gate BV further reached 14.6 V. By introducing the *u*-GaN layer between the *p*-GaN and metal, the hole concentration close to the Schottky junction can be effectively decreased, which promotes a wider depletion region when a positive bias is applied. Thus, the peak electric field is lowered and the

gate BV is significantly enlarged. Tallarico et al. have adopted a similar strategy by Mg doping compensation in [107]. However, no significant gate BV increase has been observed in their work. This difference can be attributed to their short L_{GS} and self-aligned metal/*p*-GaN architecture, which makes the *p*-GaN sidewall vulnerable [115], [148], [149].

Figure 6.3(c) shows the statistical summary of the gate BV of structure A, B and C at 25 ^{o}C, 100 ^{o}C and 150 ^{o}C. For each temperature, at least fifteen devices were measured for each structure. All the gate BVs of the three structures show weak dependences on the temperature. These results demonstrate that the doping engineering can effectively suppress the gate leakage current and boost the gate BV without impacting the V_{TH} or any additional fabrication process.

6.3 TDGB Analysis

In recent years, constant gate voltage stress measurements have been commonly used in *p*-GaN gate HEMTs to evaluate the gate reliability similar to the gate oxide reliability investigations in Si MOSFETs [102], [105], [108]. It was shown that the *p*-GaN gate exhibits a time-dependent gate breakdown (TDGB), which has a Weibull distribution. Although the lifetime prediction under dynamic gate stress may be more practical for power switching applications, the constant gate voltage stress measurements are still very meaningful in investigating the reliability and predicting the lifetime [108], [149], [150].

TDGB tests with constant voltage stresses were performed to evaluate the gate reliability of the samples with structure A (Figure 6.4) and C (Figure 6.5). A constant voltage is applied on the gate with V_{DS} = 0 V at room temperature. The time-to-breakdown (t_{BD}) is defined as when the gate leakage shows a sudden increase. For each structure, three different V_{GS} were adopted (10 V,

10.2 V, 10.4 V for structure A, and 12.8 V, 13 V, 13.2 V for structure C). t_{BD} distribution can be described by the Weibull statistics. In this distribution, the cumulative failure probability, F(t_{BD}), is related to t_{BD} as F(t_{BD}) = 1 - $exp(-t_{BD}/\eta)^{\beta}$, where η is the scale factor or 63.2% value of the distribution and β is the shape factor or Weibull slope, proportional to the spread in t_{BD}. By plotting ln[-ln(1-F(t_{BD}))] as a function of ln(t_{BD}), both η and β can be extracted from the linear fit. The shape factor β extracted from structure A is 0.74-0.82, whereas it is 0.76-0.87 from structure C. The comparable β values indicate a similar degradation mechanism.

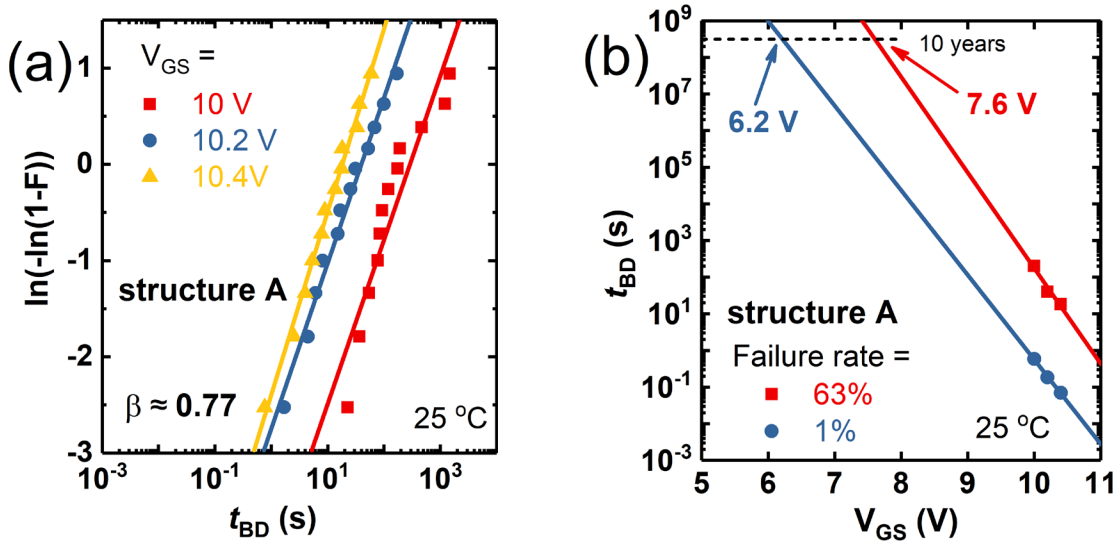


Figure 6.4 (a) Weibull plot of t_{BD} distribution of structure A and; (b) Lifetime prediction. By choosing a 63% and 1% failure rate for a 10-year lifetime, the maximum applicable V_{GS} are 6.2 V and 7.6 V, respectively.

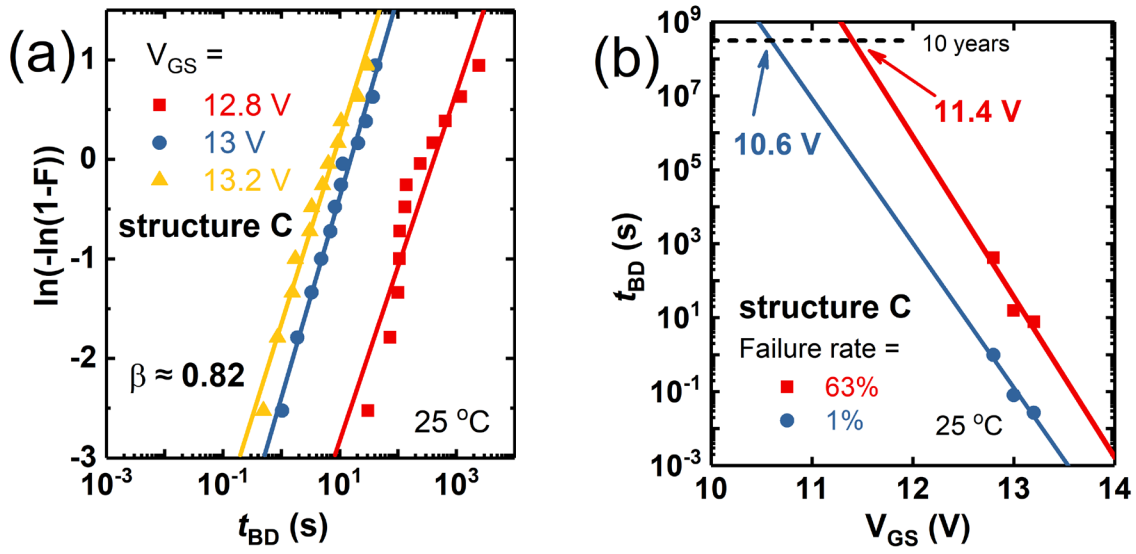


Figure 6.5 (a) Weibull plot of t_{BD} distribution of structure C and; (b) Lifetime prediction. By choosing a 63% and 1% failure rate for a 10-year lifetime, the maximum applicable V_{GS} are 11.4 V and 10.6 V, respectively.

The lifetime prediction was performed using the most conservative exponential law (i.e., linear fitting of the ln(t_{BD})-V_{GS} relationship), as shown in Figure 6.4(b) and Figure 6.5(b). Considering a 10-year lifetime at a failure level of 1%, the $V_{G\text{-}max}$ is determined to be 6.2 V for substrate A. Meanwhile, a much higher $V_{G\text{-}max}$ of 10.6 V has been achieved in structure C. The increased applicable gate voltage range offers more gate driver design flexibility and robust gate reliability.

Figure 6.6 plots $V_{G\text{-}max}$ and the corresponding V_{TH} observed in the *p*-GaN gate HEMTs in this work and other *p*-GaN gate HEMTs in literature. A high V_{TH} and large $V_{G\text{-}max}$ are particularly desired in *p*-GaN gate HEMTs. The $V_{G\text{-}max}$ values are extracted by the exponential law for a 10-year lifetime at a failure rate of either 1% or 63%. Structure C demonstrates the largest $V_{G\text{-}max}$.

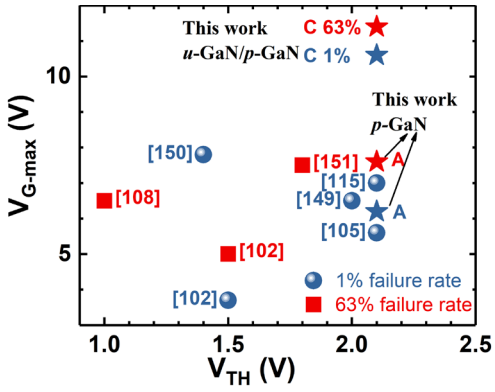


Figure 6.6 Comparison of $V_{G\text{-}max}$ and V_{TH} of structure A and C and other *p*-GaN gate HEMTs. The blue ones are estimated at a failure rate of 1%, and the red ones are estimated at 63%.

6.4 Chapter Summary

In this part of work, a novel *p*-GaN gate HEMT structure with doping engineering was proposed and investigated. By growing an additional *u*-GaN layer on top of the *p*-GaN, the electric field close to the metal/GaN can be successfully lowered. More robust and reliable devices with lower gate leakage currents, higher gate BV (14.6 V), enlarged applicable gate voltage range (10.6 V) were obtained, with negligible impacts on the other characteristics such as the V_{TH}, R_{ON} and sub-threshold slope. Moreover, this *u*-GaN/*p*-GaN technique is fully compatible with the original fabrication process since it requires no additional process step after the MOCVD growth. The proposed *u*-GaN/*p*-GaN structure is highly effective in improving the *p*-GaN gate HEMT reliability for high-efficiency power conversion systems.

Chapter 7: Conclusion and Future work

7.1 Conclusion

This work presents a comprehensive study of *p*-GaN gate HEMTs, including the theoretical background, device fabrication, failure mechanisms, and three different methods to enhance the device's performance. By the design of novel device structures and the optimization of the fabrication process, we realized reliable *p*-GaN gate HEMTs with low R_{ON}, high BV_{DSS}, high V_{TH}, high gate BV, low gate leakage current, and high $V_{G\text{-}max}$.

Chapter 1 includes a background review for power devices, GaN material properties, and basic AlGaN/GaN HEMTs structure. Chapter 2 discusses the fabrication process and characterization methods for *p*-GaN gate HEMTs in detail. A state-of-the-art *p*-GaN gate HEMT fabrication baseline was developed for the subsequent investigation. Some of the most important technological issues, including the *p*-GaN gate etching, the source/drain metal contact formation, the passivation deposition, and the gate metallization have been thoroughly studied. Chapter 3 demonstrates a novel multiple-gate-sweep-based method to identify different gate failure mechanisms, including the Schottky junction breakdown, the PiN junction breakdown, and the passivation-related breakdown. The analysis method was employed for the devices with different passivation materials and showed its applicability. This multiple-gate-sweep-based method is generally applicable for *p*-GaN gate HEMTs. For the first time, it's demonstrated that the PiN junction failure has no effect on gate leakage current at positive V_G.

Based on the baseline process in Chapter 2 and the analysis method in Chapter 3, three different structures aimed at enhancing the *p*-GaN gate HEMTs' electrical performance and reliability are demonstrated from Chapters 3 to 6, including metal/graphene gates, ultra-high-resistance Au/Ti/*p*-GaN junctions, and doping engineering. The three different methods have their own unique strengths. The comparison of the three gate architectures is summarized in Table 7.1. The improvement includes higher V_{TH}, lower gate leakage current, better metal/*p*-GaN interface, and higher gate breakdown voltage.

Especially, the doping technique is fully compatible with the current fabrication process. Among the three methods, it might be the most promising one since the highest gate BV is achieved with the least cost. TDGB measurements also reveal that $V_{G\text{-}max}$ increases significantly, effectively expanding the gate operating voltage margin. Finally, conclusions and plans for future work are summarized in this chapter.

	Strength	**Weakness/Extra processing step**
Chapter 4 Graphene gate	• 0.30 V higher V_{TH} • 0.24 eV higher Φ_B • Better metal/*p*-GaN interface • Lower gate leakage • Higher gate BV	• The commercial use of graphene in industry is not ready.
Chapter 5 Au/Ti/*p*-GaN junctions	• Easily accessible • Higher gate BV	• Au is not compatible with CMOS • One extra high-temperature annealing step is needed
Chapter 6 Doping engineering	• Higher gate BV (14.6 V) • lower gate leakage current • Enlarged $V_{G\text{-}max}$ (10.6 V) • Easy to industrialization • Simple process	• One extra epitaxial growth step needed

Table 7.1 Comparison of *p*-GaN gate HEMTs with different gate structures in Chapter 4-6.

7.2 Future Work

We have achieved good results in the V_{TH} and gate reliability improvement of *p*-GaN gate HEMTs. Other electrical characteristics, especially R_{ON} and BV_{DSS}, deserve further investigation and optimization. To efficiently deplete the 2DEG channel and achieve a positive V_{TH}, a lower Al molar fraction and a thinner AlGaN layer are conventionally adopted in a *p*-GaN gate HEMT compared to that in a normally-on AlGaN/GaN HEMT (e.g., 15 nm $Al_{0.2}Ga_{0.8}N$ versus 25 nm $Al_{0.25}Ga_{0.75}N$). This subsequently results in higher R_{ON} and lower I_{ON} in *p*-GaN gate HEMTs with the same source-drain length compared with normally-on HEMTs. Further reducing R_{ON} without sacrificing BV_{DSS} and V_{TH} remains a critical challenge in this field. A possible approach is selectively epitaxial growth of the AlGaN layer in localized regions. In this structure, a thicker AlGaN layer will be epitaxially grown on the wafer except the gate regions after the *p*-GaN etching step. Hence, the AlGaN layer is thinner in the gate regions while it's thicker in the access regions. A large positive V_{TH} and a low R_{ON} can be achieved simultaneously.

Other possible future works include an investigation on the dynamic switching behavior of *p*-GaN gate HEMTs with different gate architectures. A comprehensive study on gate failure mechanisms has been conducted in this work. Three different approaches to improve the static electrical performances (V_{TH} and gate BV) have been demonstrated. Despite these results, the effect of different gate architectures of *p*-GaN gate HEMTs on the dynamic switching behavior has not yet been investigated, which is indispensable for real applications. Apart from the gate stress under static conditions, studies on the gate degradation under dynamic gate stress are necessary for the lifetime prediction in practical power switching applications. For operation in the inductive-load dominated power systems, the transient switching capability and dynamic R_{ON},

as well as the over-voltage ruggedness under dynamic breakdown events, all pose inevitable challenges to the HEMTs, which deserve future studies.

Bibliography

[1] Roccaforte, F., Greco, G., Fiorenza, P., & Iucolano, F. (2019). An overview of normally-off GaN-based high electron mobility transistors. *Materials*, 12(10), 1599.

[2] Fewson, D. (1998). *Introduction to power electronics*. Butterworth-Heinemann.

[3] Ren, F., & Zolper, J. C. (2003). *Wide energy bandgap electronic devices*. World Scientific.

[4] Kim, M., Seo, J. H., Singisetti, U., & Ma, Z. (2017). Recent advances in free-standing single crystalline wide band-gap semiconductors and their applications: GaN, SiC, ZnO, β-Ga 2 O 3, and diamond. *Journal of Materials Chemistry C*, 5(33), 8338-8354.

[5] Baliga, B. J. (1989). Power semiconductor device figure of merit for high-frequency applications. *IEEE Electron Device Letters*, 10(10), 455-457.

[6] Saito, W., Omura, I., Ogura, T., & Ohashi, H. (2004). Theoretical limit estimation of lateral wide band-gap semiconductor power-switching device. *Solid-State Electronics*, 48(9), 1555-1562.

[7] *Compound Semiconductor Quarterly Market Monitor: Q3-2020.* (2020). Yole Développement (Yole), https://www.i-micronews.com/improved-reliability-in-power-gan-will-further-drive-its-market-growth-an-interview-with-transphorm/

[8] IEA (2016), *World Energy Outlook 2016*, IEA, Paris, https://doi.org/10.1787/weo-2016-en.

[9] Roccaforte, F., Fiorenza, P., Greco, G., Nigro, R. L., Giannazzo, F., Patti, A., & Saggio, M. (2014). Challenges for energy efficient wide band gap semiconductor power devices. *physica status solidi* (a), 211(9), 2063-2071.

[10] Ambacher, O., Smart, J., Shealy, J. R., Weimann, N. G., Chu, K., Murphy, M., ... & Hilsenbeck, J. (1999). Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N-and Ga-face AlGaN/GaN heterostructures. *Journal of applied physics*, 85(6), 3222-3233.

[11] Roccaforte, F.; Giannazzo, F.; Iucolano, F.; Eriksson, J.; Weng, M.H.; Raineri, V. (2010). Surface and interface issues in wide band gap semiconductor electronics. *Appl. Surf. Sci*., 256, 5727–5735.

[12] Rumyantsev, S., Shur, M. S., & Levinshtein, M. E. (Eds.). (2006). *Sic Materials And Devices-Volume 1* (Vol. 40). World Scientific.

[13] Yu, H., & Duan, T. (Eds.). (2017). *Gallium nitride power devices*. CRC Press.

[14] Kente, T., & Mhlanga, S. D. (2016). Gallium nitride nanostructures: Synthesis, characterization and applications. *Journal of Crystal Growth*, 444, 55-72.

[15] Kuzmik, J. (2002). InAlN/(In) GaN high electron mobility transistors: some aspects of the quantum well heterostructure proposal. *Semiconductor Science and Technology*, 17(6), 540.

[16] Dora, Y. (2006). *Understanding material and process limits for high breakdown voltage aluminum gallium nitride/gallium nitride HEMTs*. University of California, Santa Barbara.

[17] Brunner, D., Angerer, H., Bustarret, E., Freudenberg, F., Höpler, R., Dimitrov, R., ... & Stutzmann, M. (1997). Optical constants of epitaxial AlGaN films and their temperature dependence. *Journal of applied physics*, 82(10), 5090-5096.

[18] Vurgaftman, I., & Meyer, J. R. (2007). Electron band structure parameters. N*itride semiconductor devices: Principles and simulation*, 13-48.

[19] Ambacher, O. (1998). Growth and applications of group III-nitrides. *Journal of physics D: Applied physics*, 31(20), 2653.

[20] Smorchkova, I. P., Chen, L., Mates, T., Shen, L., Heikman, S., Moran, B., ... & Mishra, U. K. (2001). AlN/GaN and (Al, Ga) N/AlN/GaN two-dimensional electron gas structures grown by plasma-assisted molecular-beam epitaxy. *Journal of Applied Physics*, 90(10), 5196-5201.

[21] Li, X. Y., Xu, J. T., Tang, Y. W., LI, X., ZHANG, Y., GONG, H. M., ... & YANG, H. (2006). GaN based ultraviolet detectors and its recent development. *Infrared and Laser Engineering,* 35(3), 276.

[22] Ambacher, O., Smart, J., Shealy, J. R., Weimann, N. G., Chu, K., Murphy, M., ... & Hilsenbeck, J. (1999). Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N-and Ga-face AlGaN/GaN heterostructures. Journal of applied physics, 85(6), 3222-3233.

[23] Bernardini, F., Fiorentini, V., & Vanderbilt, D. (1997). Spontaneous polarization and piezoelectric constants of III-V nitrides. *Physical Review B*, 56(16), R10024.

[24] Marcon, D. (2011) *Reliability Study of Power Gallium Nitride Transistors*. PhD thesis, Faculty Eng., Katholieke Univ., Leuven, Belgium.

[25] Jena, D. (2003). *Polarization induced electron populations in III-V nitride semiconductors: Transport, growth, and device applications*. PhD thesis, University of California, Santa Barbara.

[26] Cheng, K. (2008). *Metal Organic Vapour Phase Epitaxy of III-Nitrides on Silicon (111)*. PhD thesis, Faculty Eng., Katholieke Univ., Leuven, Belgium.

[27] Asif Khan, M., Bhattarai, A., Kuznia, J. N., & Olson, D. T. (1993). High electron mobility transistor based on a GaN-Al x Ga1− x N heterojunction. *Applied Physics Letters*, 63(9), 1214-1215.

[28] Mishra, U. K., Parikh, P., & Wu, Y. F. (2002). AlGaN/GaN HEMTs-an overview of device operation and applications. *Proceedings of the IEEE*, 90(6), 1022-1031.

[29] Asif Khan, M., Kuznia, J. N., Olson, D. T., Schaff, W. J., Burm, J. W., & Shur, M. S. (1994). Microwave performance of a 0.25 μm gate AlGaN/GaN heterostructure field effect transistor. *Applied Physics Letters*, 65(9), 1121-1123.

[30] Ueda, H., Sugimoto, M., Uesugi, T., Fujishima, O., & Kachi, T. (2005, May). High current operation of GaN power HEMT. In *Proceedings. ISPSD'05. The 17th International Symposium on Power Semiconductor Devices and ICs, 2005*. (pp. 311-314). IEEE.

[31] Amano, H., Baines, Y., Beam, E., Borga, M., Bouchet, T., Chalker, P. R., ... & Zhang, Y. (2018). The 2018 GaN power electronics roadmap. *Journal of Physics D: Applied Physics*, 51(16), 163001.

[32] Jones, E. A., Wang, F. F., & Costinett, D. (2016). Review of commercial GaN power devices and GaN-based converter design challenges. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 4(3), 707-719.

[33] Lu, B., Piner, E.L., and Palacios, T. (2010). Breakdown mechanism in AlGaN/GaN HEMTs on Si substrate, *Proceedings of the Device Research Conference* (DRC), pp. 193–194.

[34] Sze, S.M. (1981). *Physics of Semiconductor Devices*, 2nd edn, John Wiley and Sons, Hoboken, NJ, pp. 31.

[35] Lidow, A., De Rooij, M., Strydom, J., Reusch, D., & Glaser, J. (2019). *GaN transistors for efficient power conversion*. John Wiley & Sons.

[36] Kranti, A., Haldar, S., & Gupta, R. S. (2002). An accurate charge control model for spontaneous and piezoelectric polarization dependent two-dimensional electron gas sheet charge density of lattice-mismatched AlGaN/GaN HEMTs. *Solid-State Electronics*, 46(5), 621-630.

[37] Liu, Q. Z., & Lau, S. S. (1998). A review of the metal–GaN contact technology. *Solid-State Electronics*, 42(5), 677-691.

[38] Kumar, V., Kuliev, A., Tanaka, T., Otoki, Y., & Adesida, I. (2003). High transconductance enhancement-mode AlGaN/GaN HEMTs on SiC substrate. *Electronics Letters*, 39(24), 1758-1760.

[39] Pu., T.F.(2019). *Study on Normally-off AlGaN/GaN Heterostructure Field-Effect Transistors with p-GaN Cap Layer*. PhD thesis.

[40] Oka, T., & Nozawa, T. (2008). AlGaN/GaN recessed MIS-gate HFET with high-threshold-voltage normally-off operation for power electronics applications. *IEEE Electron Device Letters*, 29(7), 668-670.

[41] Kambayashi, H., Satoh, Y., Kokawa, T., Ikeda, N., Nomura, T., & Kato, S. (2011). High field-effect mobility normally-off AlGaN/GaN hybrid MOS-HFET on Si substrate by selective area growth technique. *Solid-State Electronics*, 56(1), 163-167.

[42] Im, K. S., Ha, J. B., Kim, K. W., Lee, J. S., Kim, D. S., Hahm, S. H., & Lee, J. H. (2010). Normally off GaN MOSFET based on AlGaN/GaN heterostructure with extremely high 2DEG density grown on silicon substrate. *IEEE Electron Device Letters*, 31(3), 192-194.

[43] Fiorenza, P., Greco, G., Iucolano, F., Patti, A., & Roccaforte, F. (2017). Channel mobility in GaN hybrid MOS-HEMT using SiO 2 as gate insulator. *IEEE Transactions on Electron Devices*, 64(7), 2893-2899.

[44] Greco, G., Fiorenza, P., Iucolano, F., Severino, A., Giannazzo, F., & Roccaforte, F. (2017). Conduction mechanisms at interface of AlN/SiN dielectric stacks with AlGaN/GaN heterostructures for normally-off high electron mobility transistors: Correlating device

behavior with nanoscale interfaces properties. *ACS applied materials & interfaces*, 9(40), 35383-35390.

[45] Fiorenza, P., Greco, G., Giannazzo, F., Iucolano, F., & Roccaforte, F. (2017). Effects of interface states and near interface traps on the threshold voltage stability of GaN and SiC transistors employing SiO2 as gate dielectric. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, 35(1), 01A101.

[46] Cai, Y., Zhou, Y., Chen, K. J., & Lau, K. M. (2005). High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment. *IEEE Electron Device Letters*, 26(7), 435-437.

[47] Cai, Y., Zhou, Y., Lau, K. M., & Chen, K. J. (2006). Control of threshold voltage of AlGaN/GaN HEMTs by fluoride-based plasma treatment: From depletion mode to enhancement mode. *IEEE transactions on electron devices*, 53(9), 2207-2215.

[48] Tang, Z., Jiang, Q., Lu, Y., Huang, S., Yang, S., Tang, X., & Chen, K. J. (2013). 600-V Normally Off SiNx/AlGaN/GaN MIS-HEMT With Large Gate Swing and Low Current Collapse. *IEEE Electron Device Letters*, 34(11), 1373-1375.

[49] Zhang, Z., Fu, K., Deng, X., Zhang, X., Fan, Y., Sun, S., ... & Zhang, B. (2015). Normally Off AlGaN/GaN MIS-high-electron mobility transistors fabricated by using low pressure chemical vapor deposition Si 3 N 4 gate dielectric and standard fluorine ion implantation. *IEEE Electron Device Letters*, 36(11), 1128-1131.

[50] Chen, C., Liu, X., Tian, B., Shu, P., Chen, Y., Zhang, W., ... & Li, Y. (2011). Fabrication of Enhancement-Mode AlGaN/GaN MISHEMTs by Using Fluorinated Al_2O_3 as Gate Dielectrics. *IEEE electron device letters*, 32(10), 1373-1375.

[51] Lorenz, A., Derluyn, J., Das, J., Cheng, K., Degroote, S., Medjdoub, F., ... & Borghs, G. (2009). Influence of thermal anneal steps on the current collapse of fluorine treated enhancement mode SiN/AlGaN/GaN HEMTs. *physica status solidi c*, 6(S2 2), S996-S998.

[52] Baliga, B. J. (2006). *Silicon carbide power devices*. World scientific.

[53] *Transform tp65h035g4ws datasheet.* [Online]. Available : https://www.transphormusa.com/en/document/datasheet-tp65h035g4ws-650v-gan-fet/

[54] Hwang, I., Kim, J., Choi, H. S., Choi, H., Lee, J., Kim, K. Y., ... & Chung, U. I. (2013). p-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current. *IEEE Electron Device Letters*, 34(2), 202-204.

[55] Uemoto, Y., Hikita, M., Ueno, H., Matsuo, H., Ishida, H., Yanagihara, M., ... & Ueda, D. (2007). Gate injection transistor (GIT)—A normally-off AlGaN/GaN power transistor using conductivity modulation. *IEEE Transactions on Electron Devices*, 54(12), 3393-3399..

[56] Greco, G., Iucolano, F., & Roccaforte, F. (2018). Review of technology for normally-off HEMTs with p-GaN gate. Materials Science in Semiconductor Processing, 78, 96-106.

[57] Fujii, T., Tsuyukuchi, N., Hirose, Y., Iwaya, M., Kamiyama, S., Amano, H., & Akasaki, I. (2007). Fabrication of enhancement-mode AlxGa1–xN/GaN junction heterostructure field-effect transistors with p-type GaN gate contact. *physica status solidi c*, 4(7), 2708-2711.

[58] Hilt, O., Knauer, A., Brunner, F., Bahat-Treidel, E., & Würfl, J. (2010, June). Normally-off AlGaN/GaN HFET with p-type Ga Gate and AlGaN buffer. In *2010 22nd International Symposium on Power Semiconductor Devices & IC's (ISPSD)* (pp. 347-350). IEEE.

[59] Hilt, O., Brunner, F., Cho, E., Knauer, A., Bahat-Treidel, E., & Würfl, J. (2011, May). Normally-off high-voltage p-GaN gate GaN HFET with carbon-doped buffer. In *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs* (pp. 239-242). IEEE.

[60] Efthymiou, L., Longobardi, G., Camuso, G., Chien, T., Chen, M., & Udrea, F. (2017). On the physical operation and optimization of the p-GaN gate in normally-off GaN HEMT devices. *Applied Physics Letters*, 110(12), 123502.

[61] Posthuma, N. E., You, S., Liang, H., Ronchi, N., Kang, X., Wellekens, D., ... & Decoutere, S. (2016, June). Impact of Mg out-diffusion and activation on the p-GaN gate HEMT device performance. In *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)* (pp. 95-98). IEEE.

[62] Kozodoy, P., Xing, H., DenBaars, S. P., Mishra, U. K., Saxler, A., Perrin, R., ... & Mitchel, W. C. (2000). Heavy doping effects in Mg-doped GaN. *Journal of Applied Physics*, 87(4), 1832-1835.

[63] Roccaforte, F., Frazzetto, A., Greco, G., Giannazzo, F., Fiorenza, P., Nigro, R. L., ... & Raineri, V. (2012). Critical issues for interfaces to p-type SiC and GaN in power devices. *Applied Surface Science*, 258(21), 8324-8333.

[64] Kaufmann, U., Schlotter, P., Obloh, H., Köhler, K., & Maier, M. (2000). Hole conductivity and compensation in epitaxial GaN: Mg layers. *Physical Review B,* 62(16), 10867.

[65] Lee, F., Su, L. Y., Wang, C. H., Wu, Y. R., & Huang, J. (2015). Impact of gate metal on the performance of p-GaN/AlGaN/GaN high electron mobility transistors. *IEEE Electron Device Letters*, 36(3), 232-234.

[66] Greco, G., Iucolano, F., Di Franco, S., Bongiorno, C., Patti, A., & Roccaforte, F. (2016). Effects of annealing treatments on the properties of Al/Ti/p-GaN interfaces for normally OFF p-GaN HEMTs. *IEEE Transactions on Electron Devices*, 63(7), 2735-2741.

[67] Meneghini, M., Hilt, O., Wuerfl, J., & Meneghesso, G. (2017). Technology and reliability of normally-off GaN HEMTs with p-type gate. *Energies*, 10(2), 153.

[68] GaNSystems 650V GaN transistors [Online]:https://gansystems.com/gan-transistors/

[69] Meneghini, M., Rossetto, I., Rizzato, V., Stoffels, S., Van Hove, M., Posthuma, N., ... & Zanoni, E. (2016). Gate stability of GaN-based HEMTs with p-type gate. *Electronics*, 5(2), 14.

[70] Su, L. Y., Lee, F., & Huang, J. J. (2014). Enhancement-mode GaN-based high-electron mobility transistors on the Si substrate with a P-type GaN cap layer. *IEEE Transactions on Electron Devices*, 61(2), 460-465.

[71] Kim, H. S., Lee, D. H., Lee, J. W., Kim, T. I., & Yeom, G. Y. (2000). Effects of plasma conditions on the etch properties of AlGaN. *Vacuum*, 56(1), 45-49.

[72] Smith, S. A., Wolden, C. A., Bremser, M. D., Hanser, A. D., Davis, R. F., & Lampert, W. V. (1997). High rate and selective etching of GaN, AlGaN, and AlN using an inductively coupled plasma. *Applied physics letters,* 71(25), 3631-3633.

[73] Buttari, D., Chini, A., Meneghesso, G., Zanoni, E., Chavarkar, P., Coffie, R., ... & Mishra, U. K. (2002). Systematic characterization of Cl_2 reactive ion etching for gate recessing in AlGaN/GaN HEMTs. *IEEE Electron Device Letters*, 23(3), 118-120.

[74] Wu, T., Hao, Z. B., Tang, G., & Luo, Y. (2003). Dry etching characteristics of AlGaN/GaN heterostructures using inductively coupled H_2/Cl_2, Ar/Cl_2 and BCl_3/Cl_2 plasmas. *Japanese journal of applied physics*, 42(3A), L257.

[75] Zhou, Y., Zhong, Y., Gao, H., Dai, S., He, J., Feng, M., ... & Yang, H. (2017). p-GaN gate enhancement-mode HEMT through a high tolerance self-terminated etching process. *IEEE Journal of the Electron Devices Society*, 5(5), 340-346.

[76] Wong, J. C., Micovic, M., Brown, D. F., Khalaf, I., Williams, A., & Corrion, A. (2018). Selective anisotropic etching of GaN over AlGaN for very thin films. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, 36(3), 030603.

[77] Greco, G., Iucolano, F., & Roccaforte, F. (2016). Ohmic contacts to Gallium Nitride materials. *Applied Surface Science*, 383, 324-345.

[78] Iucolano, F., Greco, G., & Roccaforte, F. (2013). Correlation between microstructure and temperature dependent electrical behavior of annealed Ti/Al/Ni/Au Ohmic contacts to AlGaN/GaN heterostructures. *Applied Physics Letters*, 103(20), 201604.

[79] Lide, D. R. (Ed.). (2004). *CRC handbook of chemistry and physics* (Vol. 85). CRC press.

[80] Lu, C. J., Davydov, A. V., Josell, D., & Bendersky, L. A. (2003). Interfacial reactions of Ti/n-GaN contacts at elevated temperature. *Journal of applied physics*, 94(1), 245-253.

[81] Lin, M. E., Ma, Z., Huang, F., Fan, Z. F., Allen, L. H., & Morkoc, H. (1994). Low resistance ohmic contacts on wide band-gap GaN. *Applied Physics Letters,* 64(8), 1003-1005.

[82] Liu, Q. Z., & Lau, S. S. (1998). A review of the metal–GaN contact technology. *Solid-State Electronics*, 42(5), 677-691.

[83] Reeves, G. K., & Harrison, H. B. (1982). Obtaining the specific contact resistance from transmission line model measurements. *IEEE Electron device letters*, 3(5), 111-113.

[84] Green, B. M., Chu, K. K., Chumbes, E. M., Smart, J. A., Shealy, J. R., & Eastman, L. F. (2000). The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs. *IEEE Electron Device Letters*, 21(6), 268-270.

[85] Hashizume, T., & Nakasaki, R. (2002). Discrete surface state related to nitrogen-vacancy defect on plasma-treated GaN surfaces. *Applied physics letters*, 80(24), 4564-4566.

[86] Hashizume, T., Nishiguchi, K., Kaneki, S., Kuzmik, J., & Yatabe, Z. (2018). State of the art on gate insulation and surface passivation for GaN-based power HEMTs. *Materials science in semiconductor processing*, 78, 85-95.

[87] Ofuonye, B., Lee, J., Yan, M., Sun, C., Zuo, J. M., & Adesida, I. (2014). Electrical and microstructural properties of thermally annealed Ni/Au and Ni/Pt/Au Schottky contacts on AlGaN/GaN heterostructures. *Semiconductor Science and Technology,* 29(9), 095005.

[88] Karmalkar, S., & Mishra, U. K. (2001). Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate. *IEEE transactions on electron devices*, 48(8), 1515-1521.

[89] Ando, Y., Okamoto, Y., Miyamoto, H., Nakayama, T., Inoue, T., & Kuzuhara, M. (2003). 10-W/mm AlGaN-GaN HFET with a field modulating plate. *IEEE Electron Device Letters*, 24(5), 289-291.

[90] Okamoto, Y., Ando, Y., Nakayama, T., Hataya, K., Miyamoto, H., Inoue, T., ... & Kuzuhara, M. (2004). High-power recessed-gate AlGaN-GaN HFET with a field-modulating plate. *IEEE Transactions on Electron Devices*, 51(12), 2217-2222.

[91] Tallarico, A. N., Stoffels, S., Posthuma, N., Magnone, P., Marcon, D., Decoutere, S., ... & Fiegna, C. (2017). PBTI in GaN-HEMTs With p-Type Gate: Role of the Aluminum Content on ΔV_{TH} and Underlying Degradation Mechanisms. *IEEE Transactions on Electron Devices, 65(1)*, 38-44.

[92] Zhong, Y., Su, S., Chen, X., Zhou, Y., He, J., Gao, H., ... & Yang, H. (2019). Normally-off HEMTs with regrown p-GaN gate and low-pressure chemical vapor deposition SiN_x passivation by using an AlN pre-layer. *IEEE Electron Device Letters*, 40(9), 1495-1498.

[93] Hao, R., Fu, K., Yu, G., Li, W., Yuan, J., Song, L., ... & Zhang, B. (2016). Normally-off p-GaN/AlGaN/GaN high electron mobility transistors using hydrogen plasma treatment. *Applied Physics Letters*, 109(15), 152106.

[94] Choi, W., Seok, O., Ryu, H., Cha, H. Y., & Seo, K. S. (2013). High-Voltage and Low-Leakage-Current Gate Recessed Normally-Off GaN MIS-HEMTs With Dual Gate Insulator Employing PEALD-SiN_x/RF-Sputtered-HfO_2. *IEEE Electron Device Letters*, 35(2), 175-177.

[95] Hwang, I., Kim, J., Choi, H. S., Choi, H., Lee, J., Kim, K. Y., ... & Chung, U. I. (2013). p-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current. *IEEE Electron Device Letters*, 34(2), 202-204.

[96] Chen, W., Wong, K. Y., & Chen, K. J. (2008, December). Monolithic integration of lateral field-effect rectifier with normally-off HEMT for GaN-on-Si switch-mode power supply converters. In *2008 IEEE International Electron Devices Meeting* (pp. 1-4). IEEE..

[97] Lee, B., Kirkpatrick, C., Yang, X., Jayanti, S., Suri, R., Roberts, J., & Misra, V. (2010, December). Normally-off AlGaN/GaN-on-Si MOSHFETs with TaN floating gates and ALD SiO_2 tunnel dielectrics. In *2010 International Electron Devices Meeting* (pp. 20-6). IEEE..

[98] GaN Systems (2019) GS66502B 650V [Online]: https://gansystems.com/gan-transistors/gs66502b/

[99] EPC (2019) EPC2019 200V [Online]: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2019_datasheet.pdf

[100] Wu, T. L., Marcon, D., You, S., Posthuma, N., Bakeroot, B., Stoffels, S., ... & Decoutere, S. (2015). Forward bias gate breakdown mechanism in enhancement-mode p-GaN gate AlGaN/GaN high-electron mobility transistors. *IEEE Electron device letters*, 36(10), 1001-1003.

[101] Meneghini, M., Rossetto, I., Borga, M., Canato, E., De Santi, C., Rampazzo, F., ... & Decoutere, S. (2017, April). Degradation of GaN-HEMTs with p-GaN Gate: Dependence on temperature and on geometry. In 2017 *IEEE International Reliability Physics Symposium (IRPS)* (pp. 4B-5). IEEE.

[102] Ťapajna, M., Hilt, O., Bahat-Treidel, E., Würfl, J., & Kuzmik, J. (2016). Gate reliability investigation in normally-off p-type-GaN cap/AlGaN/GaN HEMTs under forward bias stress. *IEEE Electron Device Letters*, 37(4), 385-388.

[103] Ruzzarin, M., Meneghini, M., Barbato, A., Padovan, V., Haeberlen, O., Silvestri, M., ... & Zanoni, E. (2018). Degradation mechanisms of GaN HEMTs with p-type gate under forward gate bias overstress. *IEEE Transactions on Electron Devices*, 65(7), 2778-2783.

[104] Rossetto, I., Meneghini, M., Canato, E., Barbato, M., Stoffels, S., Posthuma, N., ... & Zanoni, E. (2017). Field-and current-driven degradation of GaN-based power HEMTs with p-GaN gate: Dependence on Mg-doping level. *Microelectronics Reliability*, 76, 298-303.

[105] Tallarico, A. N., Stoffels, S., Magnone, P., Posthuma, N., Sangiorgi, E., Decoutere, S., & Fiegna, C. (2016). Investigation of the p-GaN gate breakdown in forward-biased GaN-based power HEMTs. *IEEE Electron Device Letters*, 38(1), 99-102.

[106] Tallarico, A. N., Stoffels, S., Posthuma, N., Magnone, P., Marcon, D., Decoutere, S., ... & Fiegna, C. (2017). PBTI in GaN-HEMTs With p-Type Gate: Role of the Aluminum Content on ΔV_{TH} and Underlying Degradation Mechanisms. *IEEE Transactions on Electron Devices, 65(1)*, 38-44.

[107] Tallarico, A. N., Stoffels, S., Posthuma, N., Decoutere, S., Sangiorgi, E., & Fiegna, C. (2019). Threshold voltage instability in GaN HEMTs with p-type gate: Mg doping compensation. *IEEE Electron Device Letters*, 40(4), 518-521.

[108] Rossetto, I., Meneghini, M., Hilt, O., Bahat-Treidel, E., De Santi, C., Dalcanale, S., ... & Meneghesso, G. (2016). Time-dependent failure of GaN-on-Si power HEMTs with p-GaN gate. *IEEE Transactions on Electron Devices*, 63(6), 2334-2339.

[109] He, J., Wei, J., Yang, S., Hua, M., Zhong, K., & Chen, K. J. (2019, May). Temperature-Dependent Gate Degradation of p-GaN Gate HEMTs under Static and Dynamic Positive Gate Stress. *In 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)* (pp. 295-298). IEEE.

[110] Jiang, H., Zhu, R., Lyu, Q., & Lau, K. M. (2019). High-voltage p-GaN HEMTs with off-state blocking capability after gate breakdown. *IEEE Electron Device Letters*, 40(4), 530-533.

[111] Kini, R. L., Dhakal, S., Mahmud, S., Sellers, A. J., Hontz, M. R., Tine, C. A., & Khanna, R. (2020). An investigation of frequency dependent reliability and failure mechanism of pGaN gated GaN HEMTs. *IEEE Access*, 8, 137312-137321.

[112] Ge, M., Ruzzarin, M., Chen, D., Lu, H., Yu, X., Zhou, J., ... & Zanoni, E. (2019). Gate reliability of p-GaN gate AlGaN/GaN high electron mobility transistors. *IEEE Electron Device Letters*, 40(3), 379-382.

[113] Kozodoy, P., Ibbetson, J. P., Marchand, H., Fini, P. T., Keller, S., Speck, J. S., ... & Mishra, U. K. (1998). Electrical characterization of GaN pn junctions with and without threading dislocations. *Applied physics letters*, 73(7), 975-977.

[114] Efthymiou, L., Murukesan, K., Longobardi, G., Udrea, F., Shibib, A., & Terrill, K. (2019). Understanding the threshold voltage instability during OFF-state stress in p-GaN HEMTs. *IEEE Electron Device Letters*, 40(8), 1253-1256.

[115] Stoffels, S., Posthuma, N., Decoutere, S., Bakeroot, B., Tallarico, A. N., Sangiorgi, E., ... & Šatka, A. (2019, March). Perimeter driven transport in the p-GaN gate as a limiting factor for gate reliability. In *2019 IEEE International Reliability Physics Symposium (IRPS)* (pp. 1-10). IEEE.

[116] Stockman, A., Canato, E., Tajalli, A., Meneghini, M., Meneghesso, G., Zanoni, E., ... & Bakeroot, B. (2018, March). On the origin of the leakage current in p-gate AlGaN/GaN HEMTs. In *2018 IEEE International Reliability Physics Symposium (IRPS)* (pp. 4B-5). IEEE.

[117] Xu, N., Hao, R., Chen, F., Zhang, X., Zhang, H., Zhang, P., ... & Zhang, B. (2018). Gate leakage mechanisms in normally off p-GaN/AlGaN/GaN high electron mobility transistors. *Applied Physics Letters*, 113(15), 152104.

[118] Hua, M., Zhang, Z., Wei, J., Lei, J., Tang, G., Fu, K., ... & Chen, K. J. (2016, December). Integration of LPCVD-SiN x gate dielectric with recessed-gate E-mode GaN MIS-FETs: Toward high performance, high stability and long TDDB lifetime. In *2016 IEEE International Electron Devices Meeting (IEDM)* (pp. 10-4). IEEE.

[119] Shen, L., Zhang, D., Cheng, X., Zheng, L., Xu, D., Wang, Q., ... & Yu, Y. (2017). Performance improvement and current collapse suppression of Al 2 O 3/AlGaN/GaN HEMTs achieved by fluorinated graphene passivation. *IEEE Electron Device Letters,* 38(5), 596-599.

[120] Robinson, J. T., Burgess, J. S., Junkermeier, C. E., Badescu, S. C., Reinecke, T. L., Perkins, F. K., ... & Snow, E. S. (2010). Properties of fluorinated graphene films. *Nano letters*, 10(8), 3001-3005.

[121] O'Hern, S. C., Stewart, C. A., Boutilier, M. S., Idrobo, J. C., Bhaviripudi, S., Das, S. K., ... & Karnik, R. (2012). Selective molecular transport through intrinsic defects in a single layer of CVD graphene. *ACS nano*, 6(11), 10130-10138.

[122] Hu, S., Lozada-Hidalgo, M., Wang, F. C., Mishchenko, A., Schedin, F., Nair, R. R., ... & Geim, A. K. (2014). Proton transport through one-atom-thick crystals. *Nature*, 516(7530), 227-230.

[123] Liang, X., Sperling, B. A., Calizo, I., Cheng, G., Hacker, C. A., Zhang, Q., ... & Richter, C. A. (2011). Toward clean and crackless transfer of graphene. *ACS nano*, 5(11), 9144-9153.

[124] Giubileo, F., & Di Bartolomeo, A. (2017). The role of contact resistance in graphene field-effect devices. *Progress in Surface Science*, 92(3), 143-175.

[125] Ferrari, A. C., & Basko, D. M. (2013). Raman spectroscopy as a versatile tool for studying the properties of graphene. *Nature nanotechnology*, 8(4), 235-246.

[126] Lükens, G., Hahn, H., Kalisch, H., & Vescan, A. (2018). Self-aligned process for selectively etched p-GaN-gated AlGaN/GaN-on-Si HFETs. *IEEE Transactions on Electron Devices*, 65(9), 3732-3738.

[127] Neamen, D. A. (2001). *Electronic circuit analysis and design* (Vol. 2). New York, NY.: McGraw-Hill.

[128] Lin, Y. J., Lee, C. T., Chang, S. S., & Chang, H. C. (2008). Electronic transport and Schottky barrier height of Ni contact on p-type GaN. *Journal of Physics D: Applied Physics*, 41(9), 095107.

[129] Stockman, A., Masin, F., Meneghini, M., Zanoni, E., Meneghesso, G., Bakeroot, B., & Moens, P. (2018). Gate conduction mechanisms and lifetime modeling of p-gate AlGaN/GaN high-electron-mobility transistors. *IEEE Transactions on Electron Devices*, 65(12), 5365-5372.

[130] Bae, S., Kim, H., Lee, Y., Xu, X., Park, J. S., Zheng, Y., ... & Iijima, S. (2010). Roll-to-roll production of 30-inch graphene films for transparent electrodes. *Nature nanotechnology*, 5(8), 574-578.

[131] Morkoç, H., Di Carlo, A., & Cingolani, R. (2002). GaN-based modulation doped FETs and UV detectors. *Solid-State Electronics*, 46(2), 157-202.

[132] Katz, O., Garber, V., Meyler, B., Bahir, G., & Salzman, J. (2001). Gain mechanism in GaN Schottky ultraviolet detectors. *Applied physics letters*, 79(10), 1417-1419.

[133] Mishra, U. K., Shen, L., Kazior, T. E., & Wu, Y. F. (2008). GaN-based RF power devices and amplifiers. *Proceedings of the IEEE*, 96(2), 287-305.

[134] Kang, B. S., Ren, F., Gila, B. P., Abernathy, C. R., & Pearton, S. J. (2004). AlGaN/GaN-based metal–oxide–semiconductor diode-based hydrogen gas sensor. *Applied physics letters*, 84(7), 1123-1125.

[135] Schalwig, J., Müller, G., Eickhoff, M., Ambacher, O., & Stutzmann, M. (2002). Gas sensitive GaN/AlGaN-heterostructures. *Sensors and Actuators B: Chemica*l, 87(3), 425-430.

[136] Li, G., Wang, W., Yang, W., Lin, Y., Wang, H., Lin, Z., & Zhou, S. (2016). GaN-based light-emitting diodes on various substrates: a critical review. *Reports on Progress in Physics*, 79(5), 056501.

[137] Bader, S. J., Chaudhuri, R., Hickman, A., Nomoto, K., Bharadwaj, S., Then, H. W., ... & Jena, D. (2019, December). GaN/AlN Schottky-gate p-channel HFETs with InGaN contacts and 100 mA/mm on-current. In *2019 IEEE International Electron Devices Meeting (IEDM)* (pp. 4-5). IEEE.

[138] Won Jang, H., Min Jeon, C., & Lee, J. L. (2003). Low-resistance, high-transparency, and thermally stable ohmic contacts on p-type GaN using Ru and Ir. *physica status solidi* (c), (1), 227-230.

[139] Jang, S. H., & Jang, J. S. (2013). Electrical characteristics and carrier transport mechanism for Ti/p-GaN Schottky diodes. *Electronic Materials Letters*, 9(2), 245-249..

[140] Roy, S. S., & Arnold, M. S. (2013). Improving graphene diffusion barriers via stacking multiple layers and grain size engineering. *Advanced Functional Materials*, 23(29), 3638-3644.

[141] Hong, J., Lee, S., Lee, S., Han, H., Mahata, C., Yeon, H. W., ... & Min, B. W. (2014). Graphene as an atomically thin barrier to Cu diffusion into Si. *Nanoscale*, 6(13), 7503-7511.

[142] Zhou, G., Wan, Z., Yang, G., Jiang, Y., Sokolovskij, R., Yu, H., & Xia, G. (2020). Gate leakage suppression and breakdown voltage enhancement in p-GaN HEMTs using metal/graphene gates. *IEEE Transactions on Electron Devices*, 67(3), 875-880.

[143] Morrow, W. K., Lee, C., DenBaars, S. P., Ren, F., & Pearton, S. J. (2016). Role of graphene interlayers in mitigating degradation of Ni/Au ohmic contact morphology on p-type GaN. *Vacuum*, 128, 34-38.

[144] Harima, H., Inoue, T., Sone, Y., Nakashima, S., Ishida, M., & Taneya, M. (1999). Local vibrational modes in p-type GaN observed by Raman scattering. *physica status solidi* (b), 216(1), 789-792.

[145] Götz, W., Johnson, N. M., Bour, D. P., McCluskey, M. D., & Haller, E. E. (1996). Local vibrational modes of the Mg–H acceptor complex in GaN. *Applied Physics Letters*, 69(24), 3725-3727.

[146] Bakeroot, B., Stockman, A., Posthuma, N., Stoffels, S., & Decoutere, S. (2017). Analytical Model for the Threshold Voltage of *p*-(Al)GaN High-Electron-Mobility Transistors. *IEEE Transactions on Electron Devices*, 65(1), 79-86.

[147] He, J., Tang, G., & Chen, K. J. (2018). V_{TH} Instability of *p*-GaN Gate HEMTs Under Static and Dynamic Gate Stress. *IEEE Electron Device Letters*, 39(10), 1576-1579.

[148] Zhou, G., Zeng, F., Jiang, Y., Wang, Q., Jiang, L., Xia, G., & Yu, H. (2021). Determination of the Gate Breakdown Mechanisms in p-GaN Gate HEMTs by Multiple-Gate-Sweep Measurements. *IEEE Transactions on Electron Devices*, 68(4), 1518-1523.

[149] Tallarico, A. N., Stoffels, S., Posthuma, N., Bakeroot, B., Decoutere, S., Sangiorgi, E., & Fiegna, C. (2019). Gate reliability of p-GaN HEMT with gate metal retraction. *IEEE Transactions on Electron Devices*, 66(11), 4829-4835.

[150] Zhang, L., Zheng, Z., Yang, S., Song, W., He, J., & Chen, K. J. (2020). *p*-GaN gate HEMT with surface reinforcement for enhanced gate reliability. *IEEE Electron Device Letters*, 42(1), 22-25.

[151] Wang, C., Hua, M., Yang, S., Zhang, L., & Chen, K. J. (2020, September). E-mode pn junction/AlGaN/GaN HEMTs with enhanced gate reliability. In *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)* (pp. 14-17). IEEE.

[152] Xing, H., Green, D. S., Yu, H., Mates, T., Kozodoy, P., Keller, S., ... & Mishra, U. K. (2003). Memory effect and redistribution of Mg into sequentially regrown GaN layer by metalorganic chemical vapor deposition. *Japanese journal of applied physics*, 42(1R), 50.