ELIMINATION OF SLACK BUS ITERATION / DROOP BUS ITERATION IN SEQUENTIAL AC-DC POWER FLOW ALGORITHM

by

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Abstract

High Voltage Direct Current (HVDC) transmission is a power transmission technology used for integrating large-scale renewable energy over long distances into AC grid. It uses power electronics technology to convert the electric power from AC systems into DC and then transmits this power over long distances and finally converts back DC into AC systems to inject power into AC grid. Current-Sourced Converters (CSC) and voltage-Sourced Converters (VSC) are two major converters deployed in HVDC. The Multi Terminal DC (MTDC) system is a DC grid having multiple terminals containing several converters connected to a common DC system. One converter end is connected to the DC grid and its other end is connected to the AC grid thus forming an integrated AC-DC grid. One converter regulates the constant DC voltage at the DC bus and is called as DC slack bus converter while the other converters regulate their power output to the AC grid. This DC slack bus also performs the voltage droop control function in combination with other converters to regulate DC grid voltage. These converters share power flows between DC and AC sides under two types of power flow algorithms, i.e., unified power flow and sequential power flow methods. This thesis focuses on sequential power flow algorithm to solve AC-DC power flow equations separately and in a sequence.

The iterative solution of sequential AC-DC power flow algorithms requires solving extra iteration loop to find the unknown power losses in DC slack or droop bus converters. This extra iteration loop causes additional computational burden on the top of iterative solution. This thesis aims to eliminate Slack Bus Iteration (SBI) or Droop Bus Iteration (DBI) while preserving the accuracy of the AC-DC power flow results. The proposed algorithm brings modification in converter loss formula by applying the AC-DC power balance principle. Simulation results are

based on IEEE New England 39-bus system with 6-bus DC grid and demonstrate the accuracy of proposed algorithm by comparing results with conventional algorithm and further can reduce the total computational burden by 11 % and 23 % with SBI and DBI elimination respectively.

Lay Summary

Voltage source converters play an important role in integrating AC and DC grids and this integration entails estimating power flows between the AC and DC grids by an algorithm termed as sequential power flow. This sequential power flow algorithm results in solving power flow equations with multiple iterations and consumes a lot of computational power and therefore it's a disadvantage. The idea presented in this thesis is to reduce the multiple iterations and this can be achieved by formulating the converter power loss formula using the DC current instead of the AC current. In this thesis, the operational performance of sequential power flow algorithm is analyzed, and the derivation of the converter power loss formula is investigated to reduce the multiple iterations while preserving the accuracy of the sequential power flow algorithm. The results are simulated and verified in Matlab using IEEE 39-bus AC system integrated with 6-bus DC grid.

Preface

This thesis is based on the research work conducted in the School of Engineering at the University of British Columbia, Okanagan Campus, under the supervision of Dr. Liwei Wang. This thesis contains research work that will be submitted to an IEEE journal. I am the principle contributor to this thesis and related research work. For the research progress, Dr. Liwei Wang provided me with the new concept of eliminating the multiple iterations in power flow algorithm by modifying power loss formula in integrated AC and DC grids. Mr. Yuanshi Zhang helped me with programming AC-DC power flow in Matlab and providing converter parameters based on his previous research work.

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Acknowledgement

First, I would like to thank my supervisor, Dr. Liwei Wang for his endless support, technical guidance and understanding. I will be always inspired by his hard work and professional dedication.

I would like to thank my research committee member, Dr. Wilson Eberle and Dr. Morad Abdelaziz for their help and technical support. This research would not be possible without the valuable suggestions and helps from my co-research fellow, Mr. Yuanshi Zhang.

I will be forever thankful to my parents, Mohammad Saleem and Iqbal Fatima for providing me courage and affection from thousands of miles away.

Dedication

To my Wife Munazza, son Rohaan, and daughter Parihaan for their patience, love, and emotional support.

Chapter 1 Introduction

1.1 Background

High Voltage Direct Current (HVDC) technology based on Voltage Source Converters (VSC) is an emerging power transmission technology for efficient and reliable integration of large-scale renewables, e.g., offshore wind and photovoltaic generations, into AC grids. This widely adoption of the VSC HVDC technology results in Multi-Terminal Direct Current (MTDC) system configuration (also known as DC grid) where multiple (three or more terminal) AC/DC converters can be interconnected to AC systems to form AC-DC super-grid. The MTDC systems provides exceptional controllability and excellent transmission efficiency [1],[4], compared to the point-to-point HVDC connections.

The concept of MTDC system was proposed using Line Commutated Converter (LCC) based on thyristors. The Quebec-New England HVDC phase II was constructed in 1990 as the first MTDC system in the world which was an extension of the existing two-terminal Québec-New England link into a five-terminal HVDC system, with a power rating of 2000 MW and a DC voltage rating of ±450 kV [5]. The LCC-HVDC technology has the limitation that the power flow direction change requires to reverse direct voltage polarity. This is because the LCC is a current source converter which has constant DC current direction. This limit makes LCC-HVDC system undesirable to respond quickly to changing power flow directions and demands [5]. The VSC-HVDC can keep DC voltage polarity constant due to the use of voltage source converters. Therefore, the change in power flow direction is easily achieved by changing the direct current polarity, which is very desirable for constructing MTDC systems.

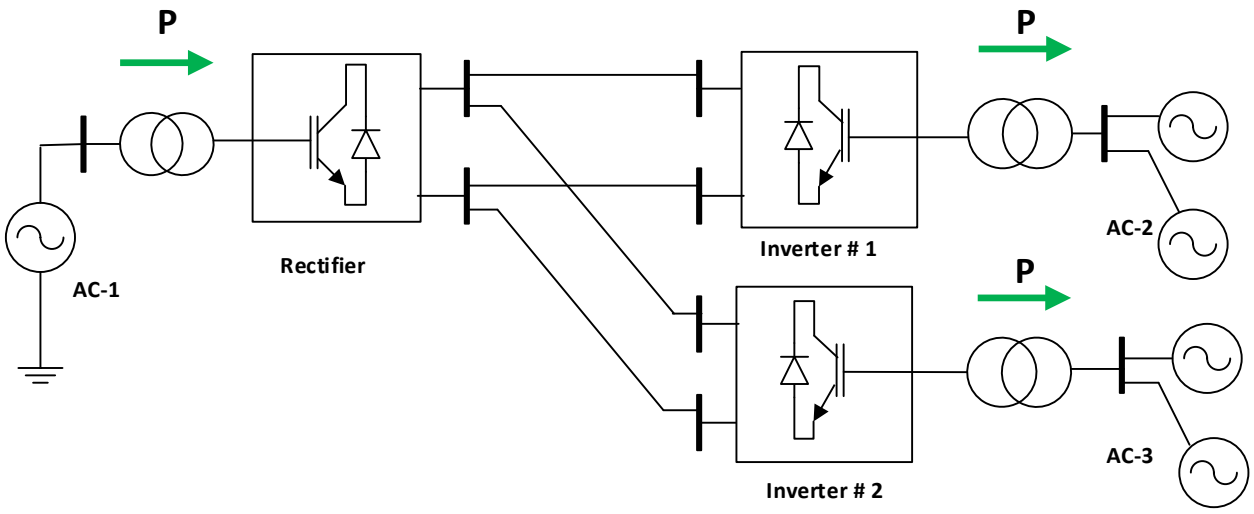


Figure 1.1 An example of three-terminal VSC-HVDC system

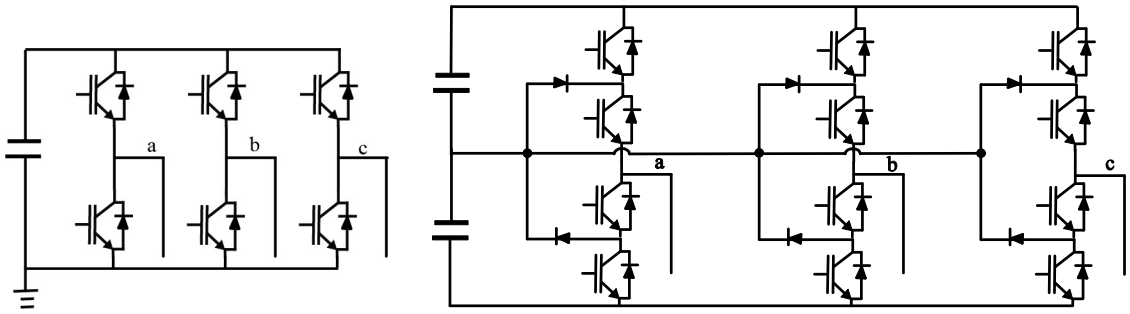
The conceptual arrangement of a three-terminal VSC-HVDC system is shown in Figure 1.1 in which the three VSCs are interconnected by DC transmission lines or DC cables. A VSC can work either as rectifier or inverter mode depending on real power flow directions. When the real power P flows from AC to DC side of a VSC, the VSC functions as a rectifier as shown in Fig. 1.1. On the other hand, the VSC operates in inverter mode when the real power flows from DC to AC side. Therefore, the power flow direction (i.e., direct current flow direction) determines the VSC operating mode.

1.2 VSC as AC-DC Grid Interface

Power electronic converters interface AC grid and remotely located renewables, such as offshore wind farms, through DC transmission network using AC-DC power conversion. There are two types of power electronic converters in use for HVDC transmission: 1-Current Source Converter (CSC) and 2-Voltage Source Converter (VSC). In a CSC, the DC side current is kept constant using large inductor thus forming a current source at the DC side. The direction of power

flow depends on polarity of the DC voltage while the direction of DC current flow remains the same. In this context, thyristors are deployed as switching devices [4]. A thyristor can be turned on by the thyristor gate while its turn-off is not controlled by the gate but through other circuit operating conditions, e.g., by applying a negative anode-to-cathode voltage to the thyristor. A VSC is quite different than that of a CSC where the DC side voltage remains the same polarity and is kept constant by using a large capacitor to form a voltage source at the DC side. Fully controllable semiconductor switches such as Insulated Gate Bipolar Transistor (IGBT) is usually employed in VSC HVDC. The switching devices are controlled by Pulse Width Modulation (PWM) technique to generate pulses for turn-on or turn-off. Due to the advancement of high-power semiconductors (i.e. controllable switches), HVDC technology [3] has considerably evolved from LCC to VSC technology. The advantages of the VSC over LCC technology include independent control of the active and reactive powers, reduced passive filter size, and improved power quality.

The VSC technology has been advanced in the last two decades, from two- and three-level converters to Modular Multilevel Converter (MMC). The configurations of two- and three-level converters are illustrated in Figure. 1.2. Each IGBT position of the two- or three-level converters requires hundreds of IGBTs in series for typical HVDC converter with a DC side voltage of several hundreds of kV (typically $\pm$320 kV) since single IGBT module has the blocking voltage of only 4.5 kV typically. Therefore, it is challenging to ensure that the hundreds of series connected IGBTs at each IGBT position are switched simultaneously. The typical switching frequency of the IGBTs are in 1~2 kHz range leading to large switching loss and high electromagnetic emission due to high switching voltage.



(a) two-level converter (b) three-level converter

Figure 1.2 VSC configuration

The MMC has recently emerged for high power and high voltage applications, e.g., VSC HVDC. The MMC concept was proposed in Germany by Prof. Marquardt [15] and was first implemented by Siemens in the Trans Bay cable project in the United States. The two- and three-level converters suffer from high switching loss while the MMC has the output voltage built up by stepping through many voltage levels leading to reduced converter switching loss and electromagnetic emission. The MMC is based on different submodule/cell types: half bridge or full bridge or their combination. These half bridge submodules are also called power electronic building block. The half-bridge based MMC has been the most efficient converter for VSC-HVDC system with typical efficiency of 1% of the converter transmitted power while the efficiency of the conventional two- and three-level converters can only reach to the efficiency of 1.3%.

The structure of MMC is based on cascaded connection of half-bridge submodules, shown in Figure. 1.3. There are six arms in the MMC, three upper arms and three lower arms. Each converter phase comprises one upper arm and one lower arm as shown in Figure 1.3. By switching each submodule on or off every period of the sinusoidal signal at given instances, many small voltage steps are formed, which then build the stepwise AC waveform as shown in Figure 1.4. It

is assumed that "N" submodules are connected in series in each arm of the MMC. Each submodule has one DC capacitor as shown in the Figure 1.3 and the reference voltage of each submodule capacitor is v_{DC}/N. At any moment, the total number of inserted submodules [9] in both upper and lower arm of one converter phase equals "N" to maintain the DC-side voltage v_{DC}. The voltage level at mid point of each phase leg equals N+1 where N is the submodule number of each arm of the MMC. Arm inductors L_{arm} are inserted in series with submodules in each arm circuit to control the circulating current and to limit the DC-side fault current.

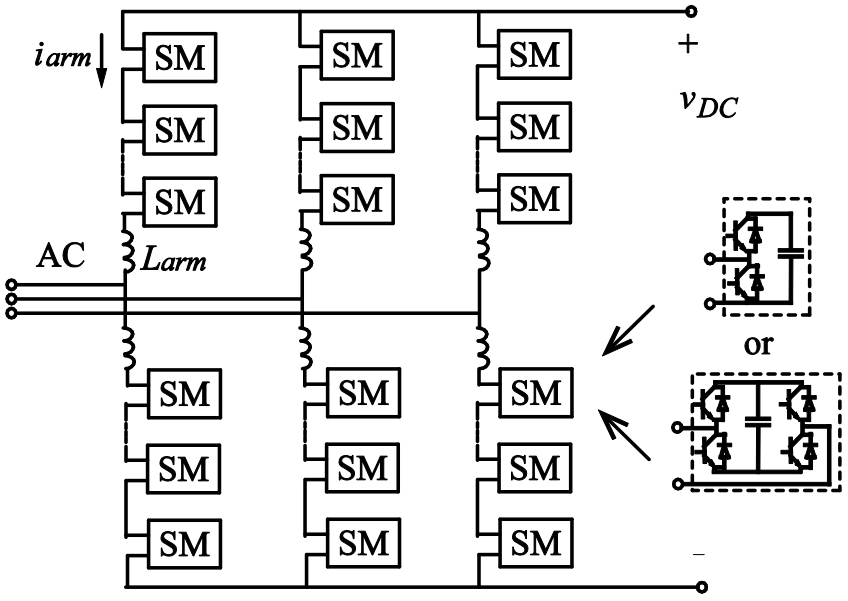


Figure 1.3 MMC circuit diagram

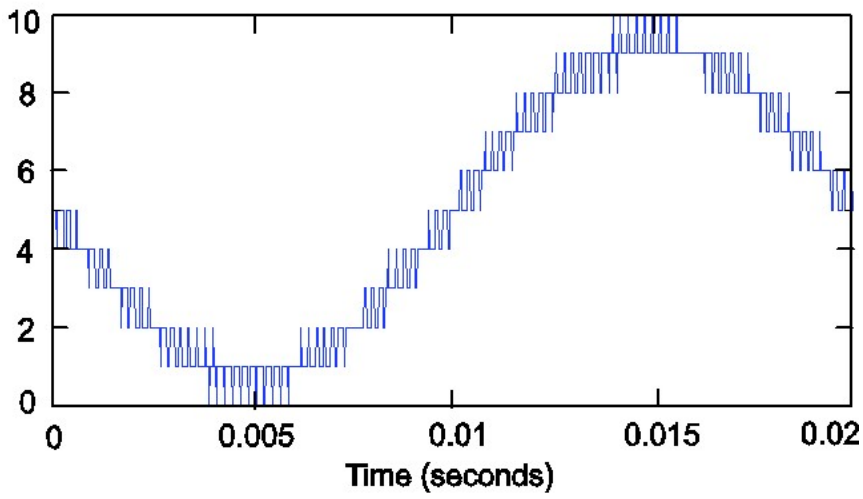


Figure 1.4 Synthetized stepwise AC waveform for MMC

The MMC is structurally scalable and theoretically can meet any voltage level requirements. Multi-carrier pulse width modulation technique is often used in the MMC. Each arm of the MMC is equivalent to a controlled voltage source with a magnitude of $N_{inserted} \times v_{DC}/N$ where $N_{inserted}$ is the inserted submodule in each arm. A typical converter arm voltage with 10 submodules per arm is shown in Figure. 1.4. During normal operations of the MMC, the arm current flows through the capacitors to charge or discharge the capacitors. The current flows through each converter arm has two components, i.e., the DC current and AC current as given in (1.1) and (1.2). One third of the DC current flows through each of the phases while the AC current divides equally between the upper and lower converter arm for each phase. The DC current is essential for the operations of the MMC.

$$i_u = \frac{i_{ac}}{2} + \frac{i_{dc}}{3} \tag{1.1}$$

$$i_l = \frac{i_{ac}}{2} - \frac{i_{dc}}{3} \tag{1.2}$$

where i_u and i_l are upper and lower arm currents, respectively.

1.3 VSC Station Configuration

A typical VSC station is represented in Fig. 1.5 where the converter components including converter valve, DC-side capacitor, AC transformer, phase reactor, and AC passive filter, are illustrated. The IGBT symbol inside the box represents the VSC valve, i.e., the series connected semiconductor switches and/or power electronic submodules. The DC-side capacitor is used to represent the DC voltage dynamic of the converter. It is noted that actual DC-side capacitors exist for two- or three-level converters while the MMC does not have the actual DC-side capacitors. Instead, the MMC has distributed DC capacitors in the half-bridge submodules of each converter arm which form an equivalent DC-side capacitor, like the 2- or 3-level converter.

In the 2- or 3-level VSCs, Pulse Width Modulation (PWM) with switching frequency of 1~2 kHz is used in order to create the high-quality sinusoidal voltage to transmit power between the AC and DC networks coupled to the converter stations. The pulsed voltage waveforms from the converter needs to be filtered to eliminate the switching harmonic content [4], [7], using AC filters. It is noted that the AC filters used in the VSC HVDC has much less footprint compared to those passive filters used in LCC HVDC absorbing low frequency harmonics. In the latest generation of VSC technology, i.e., MMC, the AC filter is removed due to very fine stair-case AC voltage waveforms produced by the MMC.

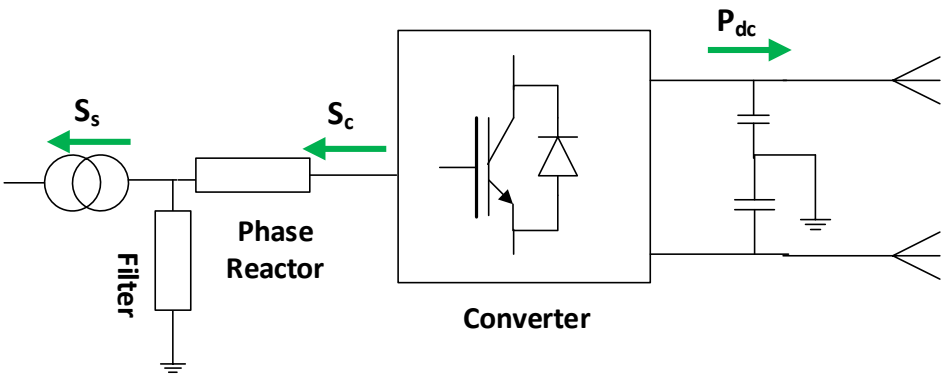


Figure 1.5 VSC station representation in DC grid

The functionality of the VSC components are summarized as follows:

1-Converter Valve Unit:

The main component of VSC system is the value unit that contains the switching device, i.e., IGBTs, gate drivers, and converter control and protection circuits. For the converter to work effectively, auxiliary circuit may be required for the IGBTs. Snubbers are often used for the series connected IGBTs to minimise over voltages during switch turn-on and turn-off. In addition, overcurrent protection circuit and voltage sharing resistors are usually connected in parallel with the IGBTs to ensure safe operations of the IGBTs. Furthermore, the gate of each IGBT switch needs isolated gate driver control circuitry [2].

2-DC Capacitors:

The primary function of the capacitors on the DC side of the converter is to stabilise the DC voltage and limit the DC voltage ripple. Sizing the capacitors should be in accordance with the switching frequency for optimum performance and economy. The faster switching frequency uses smaller capacitors and passive filters [2], [8], however, leading to increased switching losses. The primary purpose of DC capacitors is to limit the DC voltage ripple within a predefined

permissible limit, particularly when PWM switching is applied. These capacitors are necessary in 2- or 3-level converters. However, in MMC, they are not necessary, since the submodule capacitors in the six converter arms also serve as energy storage elements on the DC side. The DC capacitor can also function as an energy storage element that helps to maintain the power balance during transient events [2].

3-AC Transformers:

The AC transformers provide isolation and voltage matching [34]. They can also contribute to the reactance between VSC and the grid. The transformer works as interface between the VSC and the AC system. It adapts the grid voltage to a suitable level for the VSC. The transformer can also provide a second stage of ripple current attenuation [4].

4-Phase Reactors:

The phase reactors serve several proposes. They assist in controlling the flow of reactive and active power, reduce harmonic currents and limit any fault currents. Phase reactors are required at the VSC's AC terminals to allow for active and reactive power control. In 2- or 3-level VSC, phase reactors are also sized to help limit the ripple current at the AC side caused by PWM switching below an acceptable level [1]. In MMC, the six arm reactors functions similarly as the AC phase reactor which limit the circulating current of the converter arms and the DC fault current rise-up.

5-AC Filters:

AC filters are used in VSC to eliminate high order harmonics produced by the switching of the VSC. Different from the case of LCC HVDC, where the passive filters are required to

provide reactive power, the AC filters in VSC HVDC are not required to provide reactive power. Therefore, the size of the AC filters is significantly reduced. Depending on applications, a DC filter may be needed to reduce the harmonic currents on the DC side [3], [6].

1.4 VSC Control Modes

As the interface of AC-DC grid, the VSC plays an important role for controlling power flow and AC-DC system voltages. Understanding the VSC control modes is the key for the steady-state and transient analysis of AC-DC grid. In [10], [37], different control modes of the VSCs are categorized based on the independent controls of the real and reactive powers injected into the AC system. The four control modes are as follows:

A. Constant real-power P control mode:

In this scheme, the VSC maintains constant real power P injection into AC grid. The constant real-power control mode is often used to interface off-shore power generation.

B. Constant DC voltage control mode:

In this scheme, the VSC maintains the constant DC voltage by controlling its real power injection into AC grid. The DC node with constant DC voltage control is also called DC slack bus.

C: Constant reactive power Q control mode:

In this mode, the reactive power injection into the AC grid, from the converter is kept constant. The reactive power can be inductive or capacitive, depending on the power system operation requirement.

D: Constant AC terminal voltage control mode:

In this mode, the converter maintains the constant AC bus voltage at the Point of Common Coupling (PCC) by adjusting the VSC's reactive power injection into the AC grid.

1.5 Distributed Power-Voltage Droop Control in DC Grid

In an MTDC system, the proper control of DC bus voltage is critical for the stable and secure operations of the system. In general, two main schemes are used for DC voltage control in MTDC system, namely master-slave control and power-voltage droop control [7], [8], [39]. The master-slave control is based on single DC slack bus that adapts its active power injection to compensate for the power losses in the DC grid by maintaining constant DC voltage. Therefore, the DC slack bus is the single concentrated point of connection in DC grid that maintains the system stability. However, in case power outage occurs at the DC slack bus converter, the entire DC grid becomes dysfunctional which undermines the safety and reliability of the system. Therefore, the distributed DC voltage droop control is used where the control function of the single DC slack bus is duplicated to other converters that would be functioning as back-up DC slack buses to take over DC voltage control in case of primary DC slack bus converter fails. In other words, multiple converters can jointly control the DC voltage for an improved reliability of the DC grid. The DC voltage is distributed among the converters by introducing the droop control as shown in Fig. 1.6. It indicates that multiple converters can assist in the DC voltage control by adapting their real power injections according to their droop characteristics. It is observed in Fig. 1.6 that lowering the droop coefficient k will lead to more converter active power for the given DC voltage change.

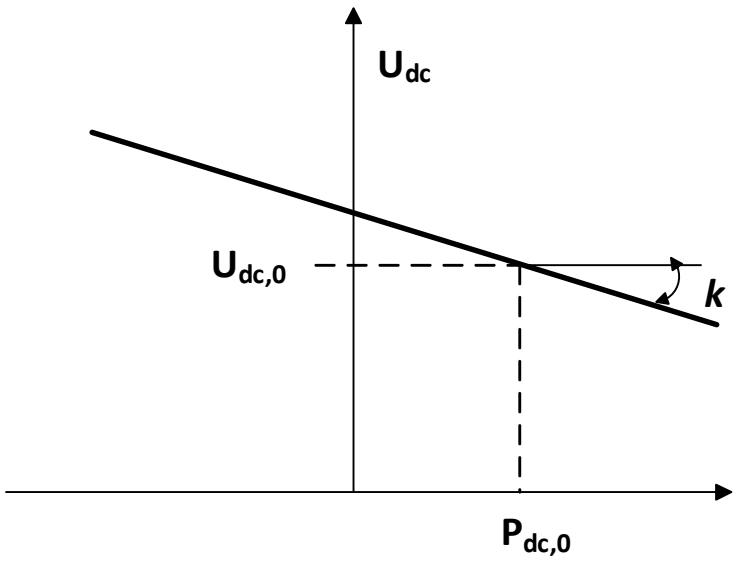


Figure 1.6 Power-voltage droop characteristics of a VSC

The DC voltage droop control is similar to frequency droop control in AC systems with one major difference that frequency remains constant in all AC system; but the DC voltages are different from one bus to another bus in DC grid. So in the light of [9], the reference value is suggested for every converter called load reference set point. These reference values are set to system's working conditions in steady state without voltage droop control being active.

1.6 Thesis Outline

This thesis includes four chapters. The first chapter explained the motivation for the research and the technical background of the topic. It gives an insight on VSC's working principle as an interface between AC grid and DC grid. The VSC station configurations and the control modes of VSC operations were described in the first chapter. Additionally, it introduced the latest VSC technology, i.e., MMC, its operating principle, and advantages over the conventional 2- or

3-level VSCs. The voltage droop control is briefly explained to expand the concept of parallel operation of multiple converters as slack bus converters.

Chapter 2 provides a literature review on the operations of the AC busses and explains the sequential power flow algorithm in greater details including the modelling of AC grid and DC grid and their power flow equations. The concept of DC slack bus iterations is analyzed for the calculation of the DC slack bus converter loss in each AC-DC power flow iteration.

Chapter 3 explains the core idea of this research and prime contribution of the thesis. This chapter addresses the elimination of slack bus iterations/droop bus iterations in sequential power flow algorithm. This elimination entails balancing the power between AC side and DC side of the converter and bring modifications in analytical power loss formula. The modification in the loss coefficients of the power formula is thoroughly investigate and explained. The grid model under study is IEEE New England 39-node AC grid with 6-node DC grid. The original and modified power loss formula is implemented and simulated in Matlab. It is demonstrated that the proposed algorithm can reduce the total computational burden by 11 % and 23 % with SBI and DBI elimination respectively. The simulation results also show the proposed sequential AC-DC power flow algorithm produces accurate simulation results compared to the conventional AC-DC power flow algorithm.

Chapter 4 provides the summary of this thesis and propose possible future work which facilitates further improvement in the power flow algorithm of AC-DC grid.

Chapter 2 Literature Review

2.1 Introduction

Power flow analysis is concerned with describing the operating state of the entire power system which includes the network of generators, transmission lines and loads. It works with the set of given known and unknown quantities, known as phasors with magnitude and phase angle. Typically power flow analysis finds the relationship between the known and unknown values and concludes by finding the amount of current/power in branches or nodes in electrical network [8], [38].

Power flow analysis starts first by defining the type of network, i.e., AC network or DC network, and network representation in terms of nodes, reactances or resistances as components of the network and their interconnection presented in single line diagram. The next step is to select the set of known and unknown quantities in terms of electrical parameters such as voltage magnitude, voltage angle, active power and reactive power, and subsequently expressed them in terms of multiple nonlinear algebraic equations called power flow equations. Then, these power flow equations are manipulated by given sufficient information (known values) by applying various numerical techniques to yield numerical results of the unknowns.

Firstly, the AC-grid power flow analysis is reviewed below which classify the grid nodes/buses into the following three types.

1**- Generator Bus:**

It is also called PV bus since the known values are “real power” and “voltage magnitude” while the unknown values are “voltage angle” and “reactive power”. The power flow will compute

the voltage angle and reactive power at this bus. This is so called generator bus as it relates to the generator.

2-Load Bus:

It is also called PQ bus as the known values are “active power” and “reactive power” while the unknown values are “voltage angle” and “voltage magnitude”. This is so called because of its connection to the load.

3-Slack Bus:

The purpose of this bus is to keep the power system stable by maintaining the active power and reactive power within the limits. This bus is used to offset the small adjustments to balance real and reactive power flows, so the known variables are “voltage magnitude” and “voltage angle” and unknown variables are “real power” and “reactive power”.

4- Does AC slack bus maintain the balance of system P and Q and has infinite capacity?

The slack bus is a fundamental concept in load flow studies and arises because the I^2R losses of the system are not known accurately in advance for the load flow calculation. The characteristic of the slack bus is based on the fact that active power and reactive power of the network is not known prior as the power losses in the network is not known before solving power flow equations so in order to compensate for the losses in the network , one of the largest generator is assigned to provide the active power and reactive power to maintain the power system in balance. This bus works on constant voltage magnitude and phase angle and only absorb or emit the active or reactive power from the power system. This bus is called Slack Bus. The slack bus does not carry any load.

At this bus, the magnitude and phase angle of the voltage are specified. The phase angle of the voltage is usually set equal to zero.

After solving the load flow problem, the difference (slack) between the total specified power (P) going into the system at all other buses and the total output (P) plus the losses (I^2R) are assigned to the slack bus. For this reason a generator bus must be selected as a slack bus.

Generally, the bus of the largest generator is selected as slack bus and numbered as bus 1.

This slack bus is taken to be an infinite bus as it doesn't have constraints on active and reactive powers as described above.

5- Power Flow Solutions:

There are well defined non-iterative and iterative solutions and procedures to compute the power flow in AC network. Gauss elimination, Jacobi, or Gauss Sidel method are generally required to solve linear algebraic equations whereas Newton Raphson method is required to solve non-linear algebraic expressions. Since power flow equations are non-linear algebraic equations so Newton-Raphson method is popular candidate to solve power flow equations.

The DC power flow analysis is similar to AC power flow with the exception that there are no reactance and no reactive power in the DC network. Additionally, there is no voltage angle required in DC power flow so only voltage magnitude is used in power flow analysis. The load buses, generator buses or slack buses function similar to AC network but with only DC electrical parameters. The rest of the details will be explained in the following subsections. The power flow solution methods of AC-DC grid are categorized into two types:

1- Unified power flow approach

2- Sequential power flow approach.

The unified power flow approach is proposed by Arrillaga and P. Bodger [11] based on organizing and constantly solving power flow equations together as an integral part [12], [13]. The unified method formulates the power flow equations of AC and DC systems simultaneously with an augmented nodal matrix incorporating AC and DC nodes together. It possesses quadratic convergence and high precision, because it solves AC-DC grid power flows simultaneously.

The sequential approach is proposed by J. Reeve solving AC and DC power flow in alternate manner [5], [6], [14]. The advantage of sequential method is that it can be coded into existing AC power flow program which can reduce the programming complexity. The unified method works out power flow equations for AC and DC grids simultaneously and entire AC/DC system in one iterative run whereas the sequential method iterates between AC and DC systems. So, for the sequential algorithm, AC and DC power flow equations will be solved separately and in a sequence that starts by first solving AC power flow to compute the parameters in AC grid. Then, it runs the DC power flow to check the convergence of the AC-DC power flow. If the AC-DC power flow doesn't converge, the sequential method will perform AC and DC power flow iteratively until convergent solution is achieved.

2.2 VSC Station Model

The VSC station can be modelled by controlled voltage source. The converter transformer, filter, and reactors can be modelled in terms of impedances. The modelling of VSC station is presented in the schematic view in Fig. 2.1 which is used to formulate the AC-DC power flow equations [1], [3].

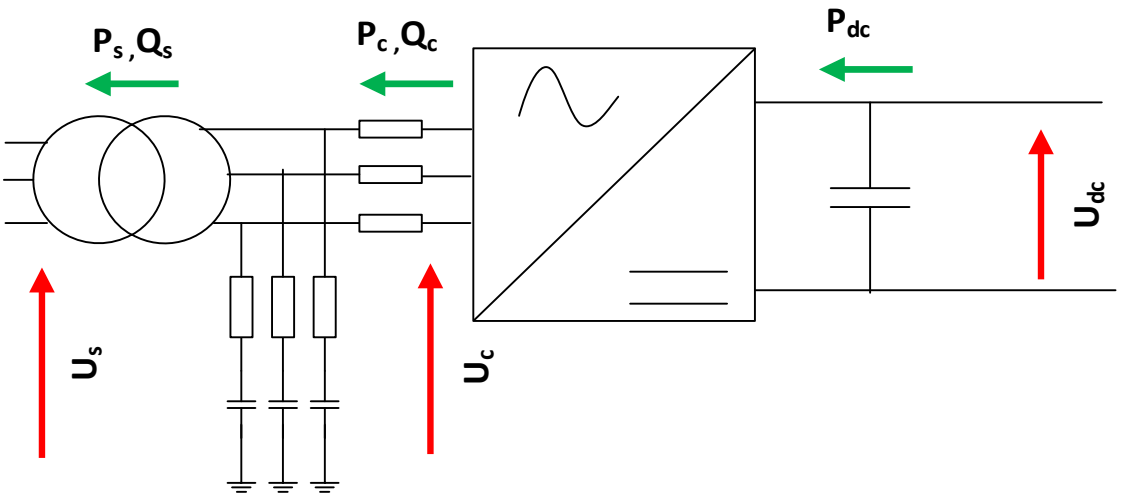


Figure 2.1 Generic VSC-HVDC station model

In Fig. 2.1, P_{dc} is the real power in the DC side , P_c and Q_c are the real and reactive powers injected by the VSC into AC side , U_c is the converter terminal voltage, P_s and Q_s are the active and reactive powers at the AC grid terminals; and U_s is the AC terminal voltage. The single-phase representation of the VSC converter station is drawn below in Fig. 2.2

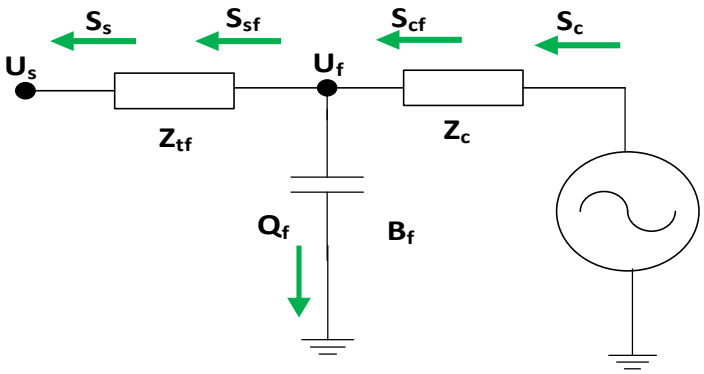


Figure 2.2 Single-phase VSC power flow model

In Fig. 2.2, the VSC station is modeled as controllable voltage source behind the complex impedances which includes the reactor and transformer impedances and filter susceptance. The phase reactor is connected to the susceptance which forms a part of the low pass filter [4], [5]. The

filter bus is connected to the AC grid through a transformer impedance; $U_c\angle\delta_c$, $U_f\angle\delta_f$, $U_s\angle\delta_s$ are the voltages at converter terminal bus, filter bus, and AC bus; $Z_c = R_c + jX_c$ is reactor impedance; $Z_{tf} = R_{tf} + jX_{tf}$ is the transformer impedance; and B_f is low pass filter susceptance. The apparent powers S_{cf} S_{sf} , S_c , S_s are the powers passing from converter bus to AC system bus through filter bus.

Figure 2.2 shows that there are three busses in this VSC model: converter bus, filter bus, and AC system bus. Regarding the output filtering requirements, it depends on the converter technology used. In case of MMC technology, the output voltage waveform is very close to the sinusoidal waveform. Therefore, the low pass filter is not required which simplifies the VSC model in power flow equation. Thus, the filter bus can be removed after the impedances of the reactor and transformer in Fig. 2.2 and are lumped together, resulting in a simplified converter station model in Fig. 2.3 below.

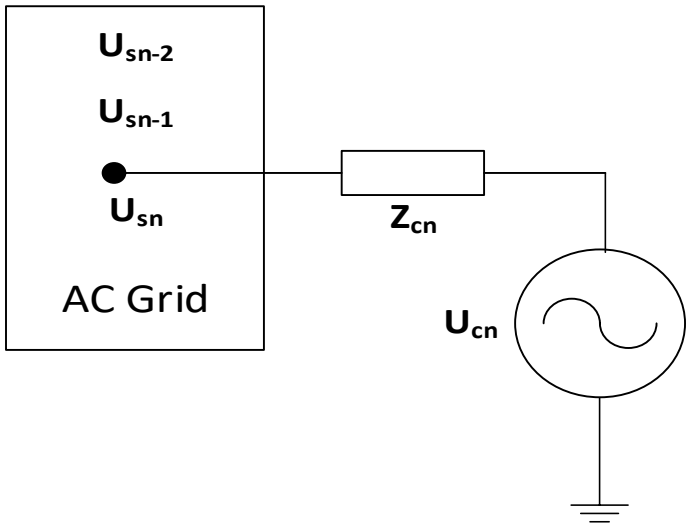


Figure 2.3 Simplified VSC station model with filter branch removed

Recalling the four control modes of the VSC stations introduced in Chapter 1, these converter control modes provide essential information for the AC-DC power flow calculation. In the case of converter PQ control mode, since the active and reactive power injections to the AC grid are controlled by the converter, the two unknown values on the converter bus are therefore voltage magnitude and voltage angle to be determined by running AC power flow. When the converter bus operates in PV control mode, the active power injection is controlled by the converter and the AC voltage magnitude is also controlled by adapting the reactive power control. The unknown values on this converter bus are reactive power Q and the voltage angle to be determined by the AC power flow.

There is only one converter control mode left, i.e., constant DC voltage control mode in which converter active power injection is controlled to maintain the constant DC voltage. This converter acts like a "slack bus" and is therefore simply called "DC slack bus" whose active power injection is not known and only the DC voltage is known.

The VSC station model with active and reactive powers and AC/DC voltages is illustrated in Fig. 2.4. The converter stations are mostly in PQ or PV control mode except for only one converter called DC slack bus converter whose primary function is to control the DC voltage at constant value. This DC slack bus converter plays a very important role in sequential power flow scheme as the main purpose of the slack bus converter is to offset the power losses that flows in DC power system since the losses are not known prior to running the DC power flow. Therefore, it is observed that the active power injections of all the converters are known except that of the DC slack bus converter. Also, the reactive power injection of all the converters are also known including DC slack bus converter. In a simplest MTDC configuration, the two terminal HVDC system is presented, one terminal operates as DC slack bus converter whereas the second converter

terminal operates as PQ control mode. Similar configuration can be further extended to MTDC containing multiple terminals that also operates in the same way as that of the two terminal MTDC system.

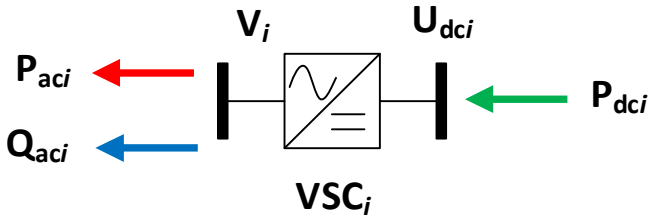


Figure 2.4 VSC station model connecting AC and DC grids

2.3 AC-DC Power Flow by Sequential Algorithm

Although AC grid power flow algorithms have been widely discussed in the contemporary literature, less attention has been paid to AC-DC power flow. The DC power flow can be obtained in a way similar to AC power flow except that there are no reactive component and no voltage angle in the DC power flow since the DC power flow is characterized by active power and DC voltage. In this section, the AC power flow and DC power flow are discussed first which is followed by the sequential power flow containing iterative solutions of AC and DC power flows. Finally, DC slack bus iteration is introduced to calculate the unknown values of the converter current to update the slack bus active power injection to complete the sequential AC-DC power flow solutions.

2.4 AC Grid Power Flow Calculation

The power flow equations for bus "i" in an AC grid with "m" nodes can be written as

$$P_i(U,\delta) = U_i \sum_{j=1}^{m} U_j \left[G_{ij} \cos(\delta_i - \delta_j) + B_{ij} \sin(\delta_i - \delta_j) \right] \quad (2.1)$$

$$Q_i(U,\delta) = U_i \sum_{j=1}^{m} U_j \left[G_{ij} \cos(\delta_i - \delta_j) - B_{ij} \sin(\delta_i - \delta_j) \right] \quad (2.2)$$

The power flow solution is obtained by computing the values of voltage magnitude and voltage angle at the busses under steady state conditions by iteratively solving the power flow equations as shown above. Since power flow equations are non-linear, the appropriate method, e.g., Newton-Raphson iterative process, can be applied to obtain the AC power flow. For the sake of brevity, the Jacobian matrix of Newton Raphson method is presented here

$$\begin{bmatrix} \left(\frac{\partial P}{\partial \delta}\right)^{(k)} & \left(U\frac{\partial P}{\partial U}\right)^{(k)} \\ \left(\frac{\partial Q}{\partial \delta}\right)^{(k)} & \left(U\frac{\partial P}{\partial U}\right)^{(k)} \end{bmatrix} \begin{bmatrix} \Delta\delta^{(k)} \\ \Delta U/U^{(k)} \end{bmatrix} = \begin{bmatrix} \Delta P^{(k)} \\ \Delta Q^{(k)} \end{bmatrix} \quad (2.3)$$

2.5 DC Grid Power Flow Calculation

The authors in [1], [4] and [5] formulated the DC grid power flow model in comparison with AC grid model. An example of four-bus DC grid is shown in Fig. 2.5. The solution of DC power flow is achieved by applying conventional AC power flow solution method to the DC grid. The DC grid is represented by the line resistances and DC voltage magnitude differences between different DC grid nodes. The impedances in AC grid are replaced by pure resistances in DC grid model.

Consider a DC grid with "n" number of nodes, the current injected into node *i* can thus be written as

$$I_{dc,i} = \sum_{\substack{j=1 \\ j \neq i}}^{n} Y_{dc,ij} \times (U_{dc,i} - U_{dc,j}) \quad (2.4)$$

where $U_{dc,i}$ is the DC voltage of node i; $Y_{dc,ij}$ is an element of the admittance matric at entries i and j.

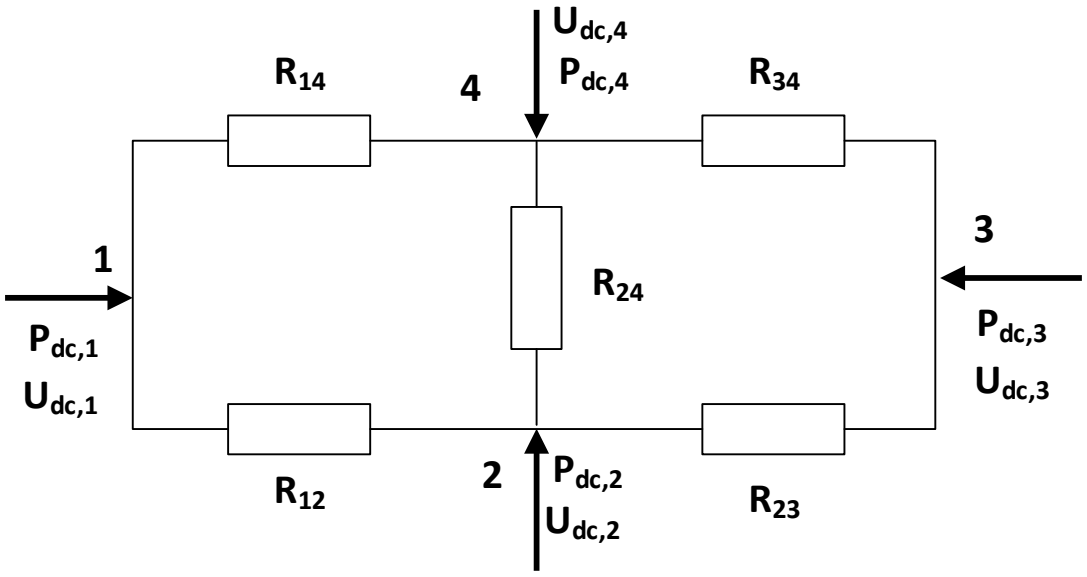


Figure 2.5 An example of four bus DC grid [4]

We can combine all the node currents injected into DC grid in the vector form as

$$I_{dc} = \left[I_{dc,1}\,, I_{dc,2}\,, I_{dc,3}\,, \ldots\ldots I_{dc,n}\right]^{\mathbf{T}} \tag{2.5}$$

Assuming a bipolar DC grid, the active power injected at node i can be written as

$$P_{dc,i} = 2U_{dc,i} \times I_{dc,i} \quad \forall \leq n \tag{2.6}$$

By combining the above-mentioned equations, we can get

$$0 = Y_{dc}\, U_{dc} - \left[P_{dc,i}\,/2U_{dc,i}\right] \tag{2.7}$$

2.6 Sequential AC-DC Power Flow Algorithm

The sequential AC-DC power flow method is adopted in this thesis due to its straightforward implementation in commercial power flow software packages. The authors in [4]–[7], [40] describe sequential power flow method for integrating AC and DC power flows for iterative solutions.

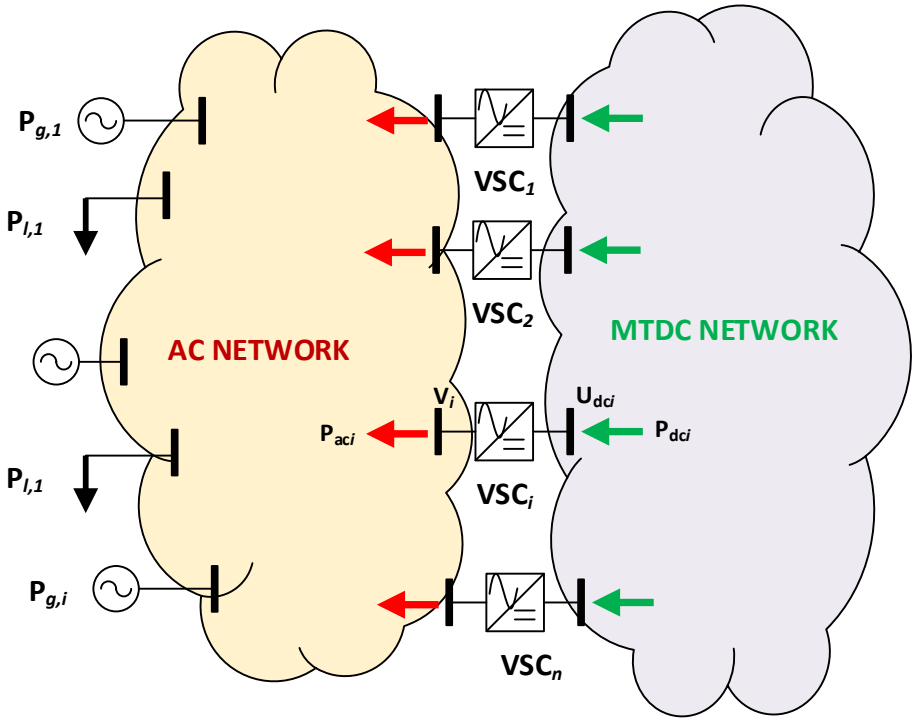


Figure 2.6 Power flow in AC-DC grid

In this section, the step by step solution procedure is explained to elaborate the sequential AC-DC power flow algorithm. An example of the power flow in AC-DC grid is illustrated in Fig. 2.6.

Step 1: Data Input and Per Unit Conversion

The sequential algorithm starts with having all converter and AC-DC grid data converted into per unit on the same base value.

Step 2: Determine the converter's AC power injection into AC grid.

In this step, to initiate the iteration, the initial value of active power injection from the converters into AC network is estimated, assuming the DC network and converters are lossless. The active power injections into AC grid are represented as

$$P_{ac} = \left[P_{ac,1}\,, P_{ac,2}\,, P_{ac,3}\,, \ldots\ldots P_{ac,n-1}, P_{ac,n}\ldots\ldots 0\ldots 0\right]^{\mathrm{T}} \tag{2.8}$$

where n represents total number of converters connected in MTDC network; the n^{th} converter is assumed to be connected with the DC slack bus converter. The first $n-1$ converters are assumed to be under constant active power control. Since the power injection from the DC slack bus converter is unknown, it can be estimated by putting its value equal to the negative of the sum of the total powers of the constant power controlled converters as

$$P_{ac,n} = -\sum_{j=1}^{n-1} P_{ac,j} \tag{2.9}$$

Step 3: AC Grid Load Flow

The active and reactive power flow equations for load flow of AC network can be written as [16], [17]

$$P_i(U,\delta) = U_i \sum_{j=1}^{m} U_j \left[\ G_{ij}\cos(\ \delta_i - \delta_j) + B_{ij}\sin(\delta_i - \delta_j)\ \right] \tag{2.10}$$

$$Q_i(U,\delta) = U_i \sum_{j=1}^{m} U_j \left[\ G_{ij}\cos(\ \delta_i - \delta_j) - B_{ij}\sin(\delta_i - \delta_j)\right. \tag{2.11}$$

where m is the total number of AC buses

The power mismatch vectors can be represented as

$$\Delta P_i = P_i^{Gen} - P_i^{Load} - P_i(U,\delta) + P_{ac,i} \tag{2.12}$$

$$\Delta Q_i = Q_i^{Gen} - Q_i^{Load} - Q_i(U,\delta) + Q_{ac,i} \tag{2.13}$$

where P_i^{Gen} and Q_i^{Gen} represent the active and reactive power generators connected to AC network buses; P_i^{Load} and Q_i^{Load} represent the load connected at AC network buses; $P_{ac,i}$ and $Q_{ac,i}$ represent the active and reactive power injections by VSC converters; $P_i(U,\delta)$ and $Q_i(U,\delta)$ represent the active and reactive powers of AC network buses calculated by the AC load flow. These nonlinear load flow equations can be solved by Newton–Raphson (N-R) load flow algorithm to determine the voltages and phase angles for all the AC buses.

Step 4: Calculation of converter's power and losses

The converter AC-side active power $P_{ac,i}$, and reactive power $Q_{ac,i}$ are solved from the AC load flow calculation results as

$$P_{ac} = -U_{ac}^2\, G_c + U_{ac}\, U_c[G_c \cos(\,\delta_{ac} - \delta_c) + B_c \sin(\,\delta_{ac} - \delta_c) \tag{2.14}$$

$$Q_{ac} = U_{ac}^2\, B_c + U_{ac}\, U_c[G_c \sin(\,\delta_{ac} - \delta_c) - B_c \sin(\,\delta_{ac} - \delta_c)\,] \tag{2.15}$$

The converter AC current is then calculated by converter complex power and AC voltage as

$$I_{c,i} = (P_{ac,i} - jQ_{ac,i})/U_{ac,i}^*\,,\ \forall\, i < n \tag{2.16}$$

The converter voltage $U_{c,i}$ can be solved by

$$U_{c,i} = U_{ac,i} - Z_{c,i} I_{c,i} \tag{2.17}$$

The converter real and reactive powers can be calculated from the converter voltage $U_{c,i}$ a

$$P_{c,i} = U_{c,i}^2 \, G_{c,i} - U_{ac,i} \, U_{c,i} [G_{c,i} \cos(\, \delta_{ac,i} - \delta_{c,i}) - B_{c,i} \sin(\, \delta_{ac,i} - \delta_{c,i}) \,] \tag{2.18}$$

$$Q_{c,i} = -U_{c,i}^2 \, B_{c,i} + U_{ac,i} \, U_{c,i} [G_{c,i} \sin(\, \delta_{ac,i} - \delta_{c,i}) + B_{c,i} \sin(\, \delta_{ac,i} - \delta_{c,i}) \,] \tag{2.19}$$

The converter loss can be calculated as

$$P_{\text{loss}} = a + \, b \times I_c + \, c \, \times {I_c}^2 \tag{2.20}$$

where a represents constant loss term independent of the converter RMS current, b and c are constant coefficients of the linear and quadratic loss terms of the converter RMS current. The converter RMS current is calculated as $I_c = \frac{\sqrt{P_c^2 + Q_c^2}}{\sqrt{3} U_c}$.

Step 5: DC Grid Power Flow

We can find the converter DC-side powers for the $n-1$ constant P controlled converters as [18]

$$P_{DC,i} = \, P_{c,i} + P_{loss,i} \;\; \forall \;\; i \leq n-1 \tag{2.21}$$

The DC voltages $\left[U_{dc,1} \, , U_{dc,2} \, , U_{dc,3} \, , \ldots . U_{dc,n-1}\right]^{\mathrm{T}}$ of the constant P controlled converter nodes are still unknown which will be solved from DC power flow.

For the DC slack bus located at the n^{th} DC bus, the DC voltage is known as u_{dcref} while the DC power $P_{DC,n}$ is unknown. The DC power flow equation (2.7) is rearranged to facilitate the solutions of the DC voltages at the constant P controlled converter nodes and DC power at the DC slack bus as [4]

$$X = \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} = \begin{bmatrix} U_{dc,1} \\ \vdots \\ U_{dc,n-1} \\ P_{dc,n} \end{bmatrix} \tag{2.22}$$

The DC bus admittance matrix is partitioned as

$$Y_{dc} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & y_{22} \end{bmatrix} \tag{2.23}$$

The DC power flow equation (2.7) can be solved using the equations below

$$0 = Y_{11}\, X_1 + Y_{12}.u_{dcref} - \frac{P_{dc,i}}{2X_{1i}} \tag{2.24}$$

$$0 = Y_{21}\, X_1 + y_{22}.u_{dcref} - \frac{X_2}{2u_{dcref}} \tag{2.25}$$

Step 6: DC Slack Bus Iteration

After DC power flow solution, we have found the value of DC power $P_{dc,n}$ at the DC slack bus but the active power at the converter bus is $P_{c,n}$ is still unknown. Since $P_{loss,n}$ depends on converter current and we do not know the value of converter current $I_{c,n}$, another iteration loop is needed to find the active power injection from DC slack bus converter to AC grid [4]. This is called DC Slack Bus Iteration (SBI). When the droop control is used in DC grid, the droop controlled nodes also need Droop Bus Iteration (DBI) to calculate the active power injection from DC droop bus converters to AC grid. The SBI/DBI will be explained in detail in the next section. The flow chart of the sequential AC-DC power flow algorithm is given in Fig. 2.7.

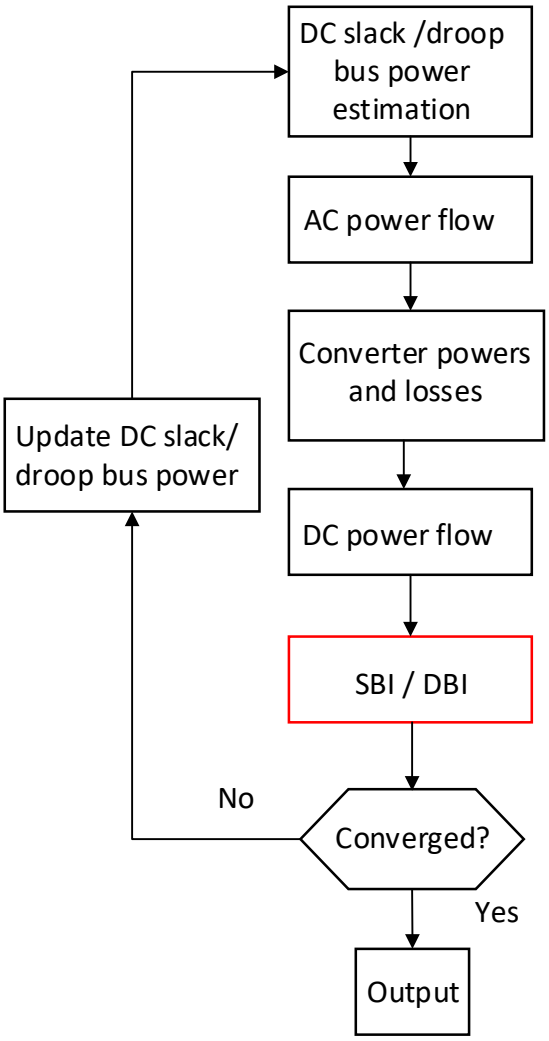


Figure 2.7 Flow chart of the sequential AC-DC power flow algorithm

2.7 DC Slack Bus Iteration

The DC power $P_{dc,n}$ at the DC slack bus is solved from the DC power flow as well as the DC voltages in the DC grid. The active power of the converter $P_{c,n}$ and the active power injection to the AC grid of DC slack bus, $P_{ac,n}$, are still unknown. They depend on the converter loss $P_{loss,n}$ which is calculated using the converter current $I_{c,n}$. Therefore, another iteration loop is required to

calculate the converter active power $P_{c,n}$ and converter active power injection $P_{ac,n}$ to AC grid of the DC slack bus [4].

Step 1:

Now to start the DC slack bus iteration process, an initial estimate is needed, and this estimate comes from the results of AC power flow and DC power flow. Previously, the DC power flow gives the value of $P_{dc,n}$ as DC power at slack bus. The converter loss is estimated using the values of $P_{ac,n}$, $Q_{ac,n}$, U_s, and δ_s from the AC power flow results. Thus, the converter power is calculated as

$$P_{c,n}^{(k)} = P_{DC,n} - P_{loss,n}^{(k)} \tag{2.26}$$

where k is the iteration index. When k is zero, $P_{c,n}^{(0)}$ represents initial guess. Below is the step by step procedure for solving DC slack bus converter active power injection.

Step 2:

This step involves finding U_c and δ_c at the converter bus using the two nonlinear equations (2.27) and (2.28) by applying Newton Raphson method.

$$Q_s = -U_s^2\, B_c + U_s\, U_c[G_c \sin(\, \delta_s - \delta_c) + B_c \sin(\, \delta_s - \delta_c)\,] \tag{2.27}$$

$$P_c = U_c^2\, G_c - U_{ac}\, U_c[G_c \cos(\, \delta_{ac} - \delta_c) - B_c \sin(\, \delta_{ac} - \delta_c)\,] \tag{2.28}$$

The Jacobian matrix is written as

$$\begin{bmatrix} \left(\frac{\partial P_c}{\partial \delta_c}\right)^{(k)} & \left(U_c \frac{\partial P_c}{\partial U_c}\right)^{(k)} \\ \left(\frac{\partial Q_s}{\partial \delta_c}\right)^{(k)} & \left(U_c \frac{\partial Q_s}{\partial U_c}\right)^{(k)} \end{bmatrix} \begin{bmatrix} \Delta {\delta_c}^{(k)} \\ \Delta U_c / {U_c}^{(k)} \end{bmatrix} = \begin{bmatrix} \Delta {P_c}^{(k)} \\ \Delta {Q_s}^{(k)} \end{bmatrix} \tag{2.29}$$

where the elements of Jacobian matrices are below

$$\left(\frac{\partial P_c}{\partial \delta_c}\right)^{(j)} = -Q_c^{(j)} - U_c^{(j)\mathbf{2}} B_c \tag{2.30}$$

$$\left(U_c \frac{\partial P_c}{\partial \delta_c}\right)^{(j)} = -P_c^{(j)} + U_c^{(j)\mathbf{2}} G_c \tag{2.31}$$

$$\left(\frac{\partial Q_s}{\partial \delta_s}\right)^{(j)} = -P_s^{(j)} - U_s^{(j)\mathbf{2}} G_c \tag{2.32}$$

$$\left(U_c \frac{\partial Q_s}{\partial U_c}\right)^{(j)} = -Q_s^{(j)} + U_s^{(j)\mathbf{2}} B_c \tag{2.33}$$

The power mismatch $\Delta P_c^{(j)}$ and $\Delta Q_s^{(j)}$ can be written as

$$\Delta P_c^{(j)} = P_c^{(k)} - P_c(U_s, U_c^{(j)}) \tag{2.34}$$

$$\Delta Q_s^{(j)} = Q_s - Q_s(U_s, U_c^{(j)}) \tag{2.35}$$

Now after solving the above six equations, we found values of U_c and δ_c at the converter bus side.

Step 3:

The equation for reactive power injection Q_c at converter side is now ready to be solved as

$$Q_c = -U_c^2 B_c + U_s U_c[G_c \sin(\delta_s - \delta_c) + B_c \cos(\delta_s - \delta_c)] \tag{2.36}$$

We will also find the converter loss P_{loss} by applying the equation (2.18)

Step 4:

The converter power $P_c^{(k)}$ is updated by (2.26) and compared to the previous iteration value $P_c^{(k-1)}$ to check if the iterative solution reaches convergence.

Step 5:

After the convergence of $P_{c,n}$ in equation (2.26), the active power injection of DC slack bus to the AC system is calculated from the equation (2.14).

The DC slack iteration procedure is summarized in Fig. 2.7 with the above mentioned steps. It is observed from Fig. 2.7 that two iteration loops are embedded in the DC slack iteration procedure, namely outer iteration regarding to the convergence of $P_{c,n}$, and inner iteration with respect to the convergence of Newton Raphson method solving U_c and δ_c in Step 2. The DC slack bus iteration increases the complexity and the computation burden of the AC-DC power flow. It will be desirable to eliminate the DC slack bus iteration in the AC-DC power flow solution while maintain the accuracy of the AC-DC power flow solution which will be discussed in the next chapter, i.e., Chapter 3.

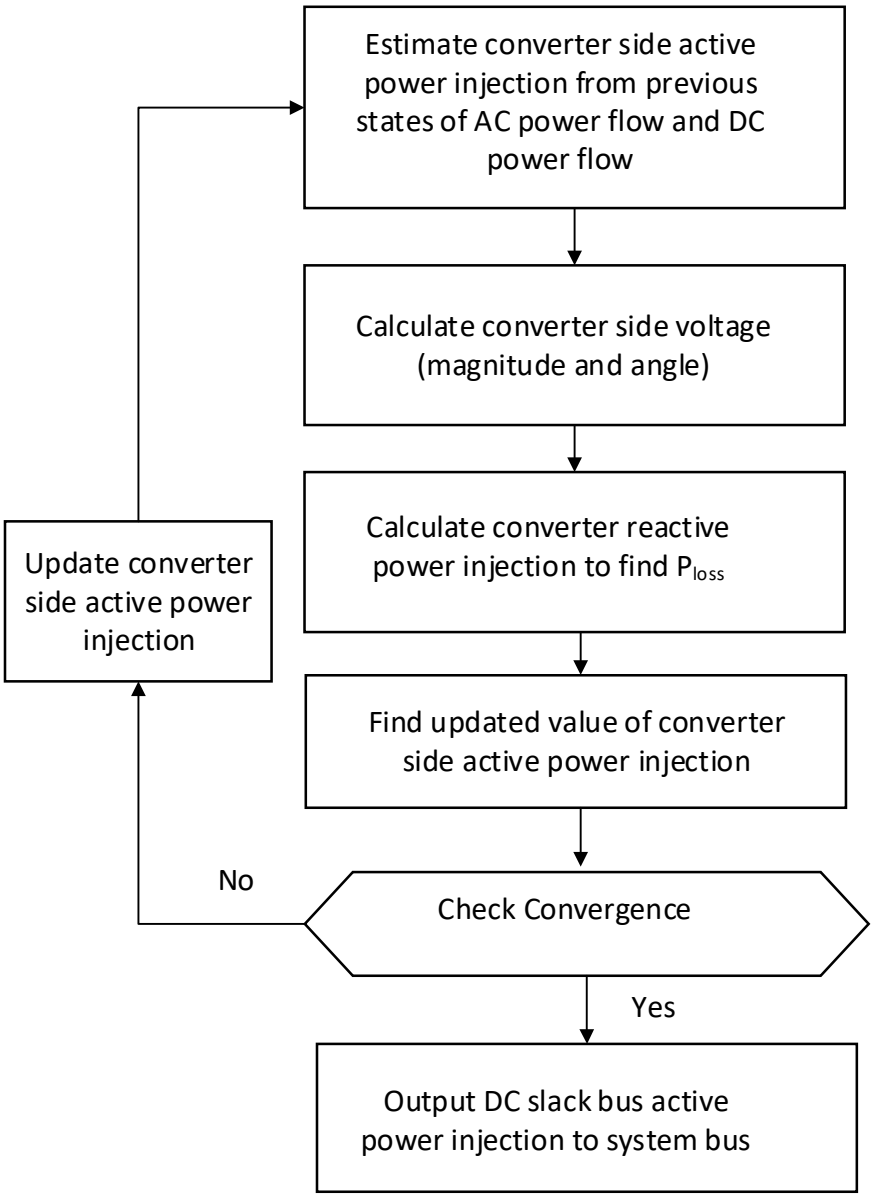


Figure 2.8 DC slack bus iteration [4]

2.8 AC/DC Microgrids

Solar and wind-based renewable energy is the fastest-growing renewable energy source worldwide and advances in DC distributed energy resources (DERs) such as photovoltaic systems

(PVs), fuel cells (FCs), and energy storage systems (ESSs) in addition to the rapid increase in the adoption of modern dc loads, such as electric charging vehicles (EVs) and electric drives, provide a comprehensive approach to architect the DC grid within a distribution network [43]. This led to the introduction of innovative power structures known as microgrids.

Microgrid is defined as a cluster of DERs and loads that works as a self-controlled entity to integrate, control and manage its DERs and loads. The distribution network may have multi coupled microgrids, with each microgrid able to operate in two modes: grid connected and autonomous (islanded).

In grid-connected mode, the microgrid can trade energy with its main grid and other neighbouring microgrids whereas in autonomous mode, the microgrid strives to meet its demand or at least the critical portion of the demand, through local generation with minimal load shedding.

Regarding the topologies of the microgrid, the microgrid can be divided into three types: AC, DC and hybrid AC/DC [43]

AC microgrid is the most used configuration of microgrid as it provides a direct way to integrate distributed generations units in the utility grid with minimum modifications such as voltage modifications however it presents some drawbacks like synchronization of DERs and circulation of reactive power that increases the power losses.

DC microgrid is based on DC based distribution generation units, energy storage systems and loads thereby forming a dc operated distribution network. The main advantage is that the less numbers of interface converters is required and there is no circulation of reactive power so the overall efficiency is increased. Moreover, there is no need for synchronization of distribution

generation units however the disadvantage is the substantial modification of power distribution network that entails high cost.

Hybrid AC/DC microgrid [44] is the combination of AC and DC architectures in the same distribution network so it facilitates the direct integration of AC-based and DC-based distribution generation units, energy storage systems and loads. The DC grid is interfaced with main grid and its adjacent AC grid through converter. In grid connected mode, the converter manages the power transfer between the AC and DC grids and also control the DC voltage. Any mismatch of the power is compensated for by the main AC grid so in that case, this AC main grid acts as a slack bus.

In case of autonomous mode (islanded) [45], the power sharing is done by two ways: centralized communication based, and decentralized non-communication based. In centralized communication based, the two-way communication is required between centralized supervisory controller and distribution generation unit controller as they work in master /slave fashion. This scheme becomes complex, costly and unreliable as AC/DC microgrid contains large number of small distribution generation units with the biggest drawback is the single point of failure.

On the other hand, the communication-less decentralized scheme [45] adopts droop characteristics that utilize local measurements, and therefore require no communication link. The principle behind decentralized droop controllers is that droop controlled DERs mimic the behaviour of synchronous generators whereby the frequency droops as the DER injects more active power and the voltage droops as the DER delivers more reactive power.

2.8.1 Power Flow Analysis of AC-DC Microgrids

As a basic steady state analysis tool for any electrical network, power flow analysis is essential to get the overall view of the system for the design and operation of microgrids. There are different applications in distribution networks like volt-var optimization, distribution automation, network configuration etc. that require the power flow analysis. In this context, the conventional AC/DC power flow programs [9] have been developed only for high voltage levels of AC/DC like HVDC and MTDC systems where there are set of PQ busses, PV busses and slack bus with highest rating.

For AC/DC microgrids in autonomous (Islanded) system [42,44], the power flow analysis requires special attention due to the following reasons

1- Islanded AC/DC microgrid is isolated so the connection to the utility grid or any other dominating source that functions as an infinite/slack bus by supplying theoretically infinite amount of power is absent.
2- AC and DC microgrids both have comparable sizes and limited capacity so no one can take the role of slack bus for its neighboring microgrid.
3- The communication less decentralized droop-controlled distribution generation units are sharing controlling both the frequency and voltage so both the generated active power and the local voltage at each unit are determined locally.
4- The active and reactive loads are quite sensitive to any changes in the voltage and frequency.
5- It is difficult to specify which distribution generation is specified for slack bus from the unit's owner perspective.

For islanded AC/DC microgrid , the three-phase power flow algorithm using Newton Trust region is proposed [42] based on elimination of slack bus , absence of pre-specified steady state frequency , calculating system frequency and use it as the communication medium between different generation units and finally the droop characteristics of the generation units that govern the generation of active and reactive power.

The power flow algorithm [42] is efficient tool to perform steady state analysis for islanded microgrids of considerably larger sizes and this analysis is required for planning and operational performance of microgrids.

2.9 Conclusion

In this chapter, the AC-DC power flow solution algorithms are reviewed and discussed. The unified and sequential AC-DC power flow are introduced and compared. The sequential power flow algorithm is adopted due to its straightforward implementation into commercial power flow software packages. The converter station model for AC-DC power flow algorithm is given which facilitates the AC-DC power flow formulation. The detailed solution procedure of sequential AC-DC power flow is then explained in where the DC slack bus iteration is discussed in detail. The DC slack bus iteration increase the complexity and computational burden for running the sequential power flow algorithm. In order to enhance the computational performance of sequential AC-DC algorithm, research effort is needed to eliminate the DC slack bus iteration and hence to improve the computational efficiency.

Chapter 3 Elimination of DC Slack/Droop Bus Iterations

3.1 Introduction

The core idea of this thesis will be presented in this chapter with the focus of eliminating the DC Slack Bus Iteration (SBI) / Droop Bus Iteration (DBI) in each sequential AC-DC power flow iteration. As explained in the previous chapter that the implementation of sequential AC-DC power flow algorithm results in the DC SBI/DBI. This is due to the unknown converter AC current at the DC slack/droop buses after the DC power flow solution which poses difficulty to find the converter power loss P_{loss}. Consequently, the converter active power injection of DC slack/droop bus is solved iteratively in each AC/DC power flow iteration. In this context, the estimation of the converter AC current and the resulting DC SBI/DBI add complexity and computational burden to the AC-DC power flow algorithm. The new approach presented in this chapter is to eliminate the DC SBI/DBI to reduce computational burden of the sequential AC-DC power flow algorithm. The new approach is implemented based on the calculation of the AC converter current using the power balance principle at AC- and DC-side of the DC slack/droop bus converter after the DC power flow calculation is completed. The proposed approach completely eliminate the DC SBI/DBI while maintaining accurate AC-DC power flow results.

3.2 Proposed Methods of Eliminating SBI/DBI

In this section, the sequential AC-DC power flow algorithm is briefly reviewed in Fig. 3.1. The sequential power flow requires the AC and DC power flows to be solved iteratively. Firstly, the AC active power injection of DC slack bus or droop-controlled busses is estimated using the

negative summation of the active power injections from other buses for DC slack bus or the negative of power reference for DC droop buses. Thereafter, AC power flow, converter powers, and DC power flow are calculated sequentially as shown in Fig. 3.1. After the DC power flow is solved, the active power injection of the DC slack or droop buses is updated using the calculated DC powers as well as the converter losses. The converter loss formula was introduced in (2.20) and is reproduced here with slightly different expressions of the loss coefficients to facilitate the further discussion of eliminating SBI/DBI.

$$P_{loss} = a + b_{ac} \times I_c + c_{ac} \times {I_c}^2 \tag{3.1}$$

where I_c is the RMS value of converter current; a, b_{ac} and c_{ac} are constant, linear, quadratic coefficients of the converter current RMS value. The coefficient a represents the constant losses, including filter, transformer load, and no load losses. Although the DC powers are calculated, the converter currents are yet unknown. Therefore, an iteration loop, i.e., SBI/DBI, is required to calculate the active power injection of DC slack or droop busses as shown in Fig. 3.1.

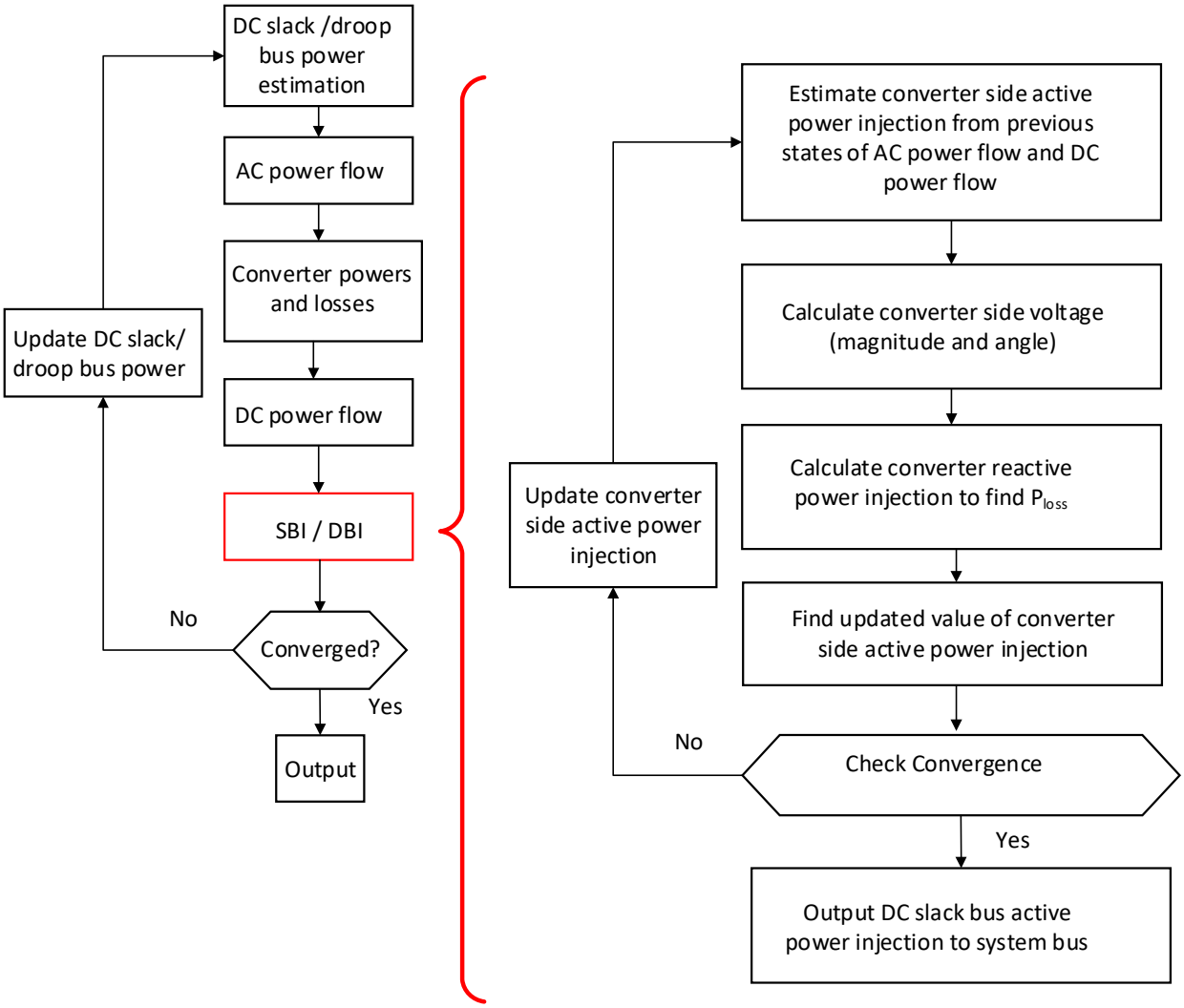


Figure 3.1 Flow Chart of AC/DC Sequential Algorithm with SBI/DBI

The power balance principle of AC/DC converter indicates that the active power flowing from the AC side of the converter equal to the active power delivered to the DC side of the converter, i.e., $P_{ac} = P_{dc}$, given the converter loss is small and ignored. The power balance principle provides a measure to estimate of AC variables from DC variables or vice versa. For example, the converter AC current I_{ac} can be estimated from the converter DC current I_{dc}. It is noted that the DC grid doesn't involve any reactance and reactive power while the AC grid contains reactive components and reactive power. Thus, the power balance principle of AC/DC converter

is the balance of active powers. Therefore, the relationship of I_{ac} and I_{dc} entails a more complex form of current equation containing the power factor and AC-to-DC voltage modulation index which will be further explained analytically in the next section. Recalling that, in sequential AC-DC power flow, the power loss calculation P_{loss} is performed based on the AC current RMS value using power loss coefficients b_{ac} and c_{ac} as explained in the P_{loss} formula, (3.1). After DC power flow, the DC current at the DC slack bus or droop busses can be solved by the DC power and DC voltage. Based on the real power balance at an AC-DC converter, the AC current can be derived from the DC current and is used in (3.1) to calculate the converter losses. Thus, the converter power P_c which can be calculated using (2.26) is now being calculated with DC values that completely eliminates the SBI/DBI iteration process.

The converter AC current calculation using real power balance principle is described below. The AC and DC real powers at the DC slack bus converter is shown in Fig. 3.2 where i represents the bus number. To write the power balance equation for DC- and AC-side, the converter is assumed lossless. On the DC side, the DC power can be presented as the product of U_{dc} and I_{dc}, i.e.,

$$P_{dc} = I_{dc} \times V_{dc} \tag{3.2}$$

where U_{dc} and I_{dc} are the DC voltage and DC current of the converter.

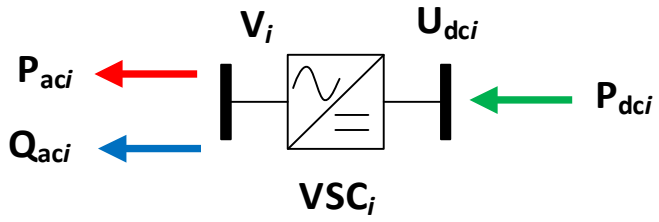


Figure 3.2 AC and DC power flows

On the AC side of the converter, the active power P_{ac} can be written as the product of DC voltage, AC current RMS value, modulation index, and power factor as

$$P_{ac} = 3 \times m \times \frac{V_{dc}}{2} \times I_c \times cos(\varphi) \tag{3.3}$$

where as m is the AC voltage modulation index and $\cos(\varphi)$ is the power factor at the converter AC side.

By applying the power balancing method and equating both the equations (3.2) and (3.3), we can obtain the following equations:

$$P_{ac} = P_{dc} \tag{3.4}$$

$$3 \times m \times \frac{V_{dc}}{2} \times I_c \, cos(\varphi) = i_{dc} \times v_{dc} \tag{3.5}$$

Now the converter current I_c can be represented in terms of the DC current i_{dc} as

$$I_c = i_{dc} \times \frac{2}{3m \, |\cos(\varphi)|} \tag{3.6}$$

Or equivalently, the DC current i_{dc} can be represented by the converter current I_c as

$$i_{dc} = I_c \times \frac{3m \, |\cos(\varphi)|}{2} \tag{3.7}$$

It is noted that the loss coefficients b_{ac} and c_{ac} in the P_{loss} formula largely depend on the manufacture's data sheets, particularly to semiconductors characteristics and converter operating conditions. The derivation of the loss coefficients b_{ac} and c_{ac} for MMC HVDC applications is missing in the literature. However, it is important for power system engineers to be able to estimate the converter loss coefficients without relying on specific manufacturer's data in AC-DC grid planning and designing stage. Thus, another focus of the thesis is to derive the converter loss

coefficients b_{ac} and c_{ac} analytically based on appropriate assumptions and approximations which will be detailed in the next section. It is observed in the loss formula (3.1) that the converter loss is represented by converter AC current RMS value. An interesting question can be raised if the converter loss can be represented by DC current as well which leads to the following loss formula as

$$P_{\text{loss}} = a + b_{dc} * I_{dc} + c_{dc} * {I_{dc}}^2 \tag{3.8}$$

Apparently, once the DC current related loss coefficients are known, the converter losses can be calculated directly from the DC current without SBI/DBI. In next section, the loss coefficients b_{ac}, c_{ac}, b_{dc}, and c_{dc} are derived analytically based on converter semiconductor conduction and switching losses under various MMC operating conditions.

3.3 Analytical Loss Formula for MMC

In steady-state operation, the six arms of the MMC has very similar operation conditions, leading to approximately equal semiconductor losses. Therefore, an arbitrary converter arm is used for the calculation of semiconductor conduction and switching losses. Without loss of generality, the upper arm of Phase A, i.e., I_u, is used for the semiconductor loss calculation. I_u is formulated here as

$$I_u = \frac{i_{ac}}{2} + \frac{i_{dc}}{3} \tag{3.9}$$

where i_{ac} and i_{dc} are converter AC current and DC current respectively.

It is observed from (3.9) that for a balanced three-phase MMC, one third of the DC current will flow through each of the arms while the respective AC current divides equally between the

upper and lower converter arm in each phase. It is assumed that the converter phase current i_{ac} can be represented by sinusoidal wave as

$$i_{ac} = \sqrt{2} \times I_c \times \cos(\theta) \tag{3.10}$$

where I_c is the RMS value of the phase current.

Substituting (3.7) and (3.10) into (3.9) , the arm current, i_u, can be formulated as

$$i_u = \left(\frac{\sqrt{2}\cos\theta}{2} + \frac{m|\cos(\varphi)|}{2}\right) \times I_c \tag{3.11}$$

It is observed from (3.11) that the converter arm depends on voltage modulation index m, power factor $\cos(\varphi)$, and the AC current RMS value I_c.

According to power loss formula P_{loss} in (3.1) and (3.8), the loss coefficients associated with linear and quadratic current components of the RMS AC or DC currents will be derived in this section.

3.3.1 Derivation of Loss Coefficient c_{ac}

The loss coefficient of c_{ac} is associated with conduction loss in the MMC due to semiconductor internal resistance in the turned-on state, known as "on-state resistance", R_{on}. It is recognized that the on-state resistances of the IGBT and diode in an IGBT module are different since the IGBT and diode chips have different on-state characteristics. However, the difference of the two on-state resistances are small. To simplify the converter loss calculation for power system applications, the equivalent on-state resistance R_{on} of the semiconductor is taken as the average of the on-state resistances of the IGBT and the diode. Thus, both diode and IGBT have the same

on-state resistance. Therefore, the total resistance R_{arm} in one arm of half-bridge SM based MMC can be represented as

$$R_{arm} = N\rho R_{on} + N(1-\rho)2R_{on} = NR_{on}(2-\rho) \tag{3.12}$$

where ρ is the percentage of the half bridge SMs out of total SMs in one converter arm and $1-\rho$ is the percentage of full bridge SMs out of total SMs; N is the total number of SMs in one arm; R_{on} is the on-state resistance of each half-bridge SM.

The conduction loss in each arm of MMC due to the on-state resistance is represented as

$$P_{loss,R_{on}} = \frac{6}{2\pi}\int_0^{2\pi} i_u^2 R_{arm} d\theta \tag{3.13}$$

By substituting equation (3.11) and (3.12) into (3.13), we can get

$$P_{loss,R_{on}} = \frac{3}{2}NR_{on}(2-\rho)I_c^2(m^2\cos(\varphi)^2+1) \tag{3.14}$$

Now according to P_{loss} formula given in (3.1), the value of c_{ac} can be expressed as

$$c_{ac} = \frac{3}{2}NR_{on}(2-\rho)(m^2\cos(\varphi)^2+1) \tag{3.15}$$

3.3.2 Derivation of Loss Coefficient b_{ac}

This loss coefficient b_{ac} is associated with the semiconductor loss which is linear to the AC current, i.e., the switching losses and the conduction losses due to saturation voltage in diode and IGBT on-state characteristics.

First, the saturation voltages of the IGBT and diode of the IGBT module are assumed to be the same as V_0, the average of the saturation voltages of the two semiconductor switches. The total saturation voltage in a converter arm can be represented as

$$V_{0,arm} = N\rho V_0 + N(1-\rho)2V_0 = NV_0(2-\rho) \tag{3.16}$$

where V_o is the saturation voltage of each half-bridge while $V_{o,arm}$ is the total saturation voltage in one arm of the converter.

To facilitate the calculation of the conduction loss due to the saturation voltage V_0, the zero-crossing phase angle of i_u can be calculated from (3.11) as

$$\theta_1 = \operatorname{acos}\left(\frac{2}{3}\frac{I_{dc}}{\sqrt{2}I_c}\right) \tag{3.17}$$

The conduction loss due to the saturation voltage V_0 can be formulated as

$$P_{loss,V_0} = 6 * \frac{V_{o,arm}}{2\pi} \int_{\theta_1}^{2\pi+\theta_1} |i_u| \, d\theta \tag{3.18}$$

The average absolute value of the arm current can be formulated as

$$|\bar{I}_u| = \frac{1}{2\pi}\left(\int_{\theta_1}^{2\pi+\theta_1} |i_u| \, d\theta\right) \tag{3.19}$$

Substituting (3.6), (3.11) and (3.17) into (3.19), the average absolute value of the arm current can be calculated as

$$|\bar{I}_u| = \frac{k}{3\pi} i_{dc} \tag{3.20}$$

where k is defined as

$$k = 2\sqrt{\frac{2}{m^2 cos^2\varphi} - 1} + \pi - 2\operatorname{acos}\left(\frac{\sqrt{2}}{2} m|\cos(\varphi)|\right) \tag{3.21}$$

Based on (3.18) and (3.19), the conduction loss due to the saturation voltage V_0 can be reformulated as

$$P_{loss,V_0} = 6 * V_{o,arm} * \ |\bar{I}_u| \tag{3.22}$$

Substituting (3.19) into (3.22), the conduction loss due to the saturation voltage V_0 can be calculated as

$$P_{loss,V_0} = \frac{2kNV_0(2-\rho)}{\pi} \frac{3m|\cos(\varphi)|}{2} I_c \tag{3.23}$$

The switching losses are calculated based on the instantaneous semiconductor currents and voltages before and after switching transients. As can be found in [41], the IGBT turn-on and turn-off energies per pulse (E_{on} and E_{off}) and the diode reverse recovery energy (E_{rec}) at the reference voltages ($V_{T,ref}$ and $V_{D,ref}$) and reference currents ($I_{C,ref}$ and $I_{F,ref}$) are used for the switching loss calculation as

$$P_{on,T} = \frac{1}{T}\sum_{i=1}^{N_i}\left\{\frac{v_{T,on}(t_i)}{v_{T,ref}}\frac{i_C(t_i)}{i_{C,ref}}E_{on}\left(i_{C,ref}\right)\right\} \tag{3.24}$$

$$P_{off,T} = \frac{1}{T}\sum_{j=1}^{N_j}\left\{\frac{v_{T,off}(t_j)}{v_{T,ref}}\frac{i_C(t_j)}{i_{C,ref}}E_{off}\left(i_{C,ref}\right)\right\} \tag{3.25}$$

$$P_{rec,D} = \frac{1}{T}\sum_{k=1}^{N_k}\left\{\frac{v_{D,rec}(t_k)}{v_{D,ref}}\frac{i_F(t_k)}{i_{F,ref}}E_{rec}\left(i_{F,ref}\right)\right\} \tag{3.26}$$

where N_i, N_j, and N_k denote the numbers of IGBT switching events for turn-on, turn-off, and diode reverse recovery in one fundamental cycle T. At every switching instant (t_i, t_j, and t_k), the switching energies are scaled by the ratios of the occurring blocking voltage to the reference blocking voltage and the switching current to the reference current.

The above-mentioned instantaneous semiconductor current and voltage based switching loss calculation cannot be applied directly to power flow calculation. An analytical switching loss calculation method should be derived for MMC. The analytical switching loss calculation has the

following assumptions: (1) the SM capacitor voltages are all equal with the voltage ripples ignored; (2) the converter arm 2nd order harmonic current is suppressed so that only DC and fundamental frequency AC components are present in the arm currents; (3) the switching events are uniformly distributed over the fundamental frequency cycle; (4) the average switching frequency of all SMs is used and all SMs incur the same amount of average switching loss.

The switching loss can be analytically estimated as

$$P_{loss,sw} = 6N \frac{f_P(E_{\text{on}}+E_{\text{off}}+E_{\text{rec}})V_{SM}}{V_{ref}I_{ref}} |\bar{I}_u| \tag{3.27}$$

where E_{on}, E_{off}, and E_{rec} are the IGBT turn-on, turn-off, and the diode reverse recovery energies from datasheet; V_{ref} and I_{ref} are the reference voltage and current for the switching energies; f_P is the switching frequency per SM, V_{SM} is the rated SM voltage; N is the SM number in each arm and can be represented by

$$N = \frac{V_{dc}}{V_{SM}} \tag{3.28}$$

where V_{dc} is the DC side voltage of the MMC.

Substituting (3.20) and (3.28) into (3.27), the switching loss is expressed as

$$P_{loss,sw} = \frac{2kf_P(E_{\text{on}}+E_{\text{off}}+E_{\text{rec}})}{\pi V_{ref}I_{ref}} V_{dc}i_{dc} \tag{3.28}$$

Substituting (3.7) into (3.28), the switching loss is expressed as

$$P_{loss,sw} = \frac{2kf_P(E_{\text{on}}+E_{\text{off}}+E_{\text{rec}})}{\pi V_{ref}I_{ref}} V_{dc} \frac{3m|\cos(\varphi)|}{2} I_{\text{c}} \tag{3.29}$$

Based on (3.23) and (3.39), the conduction loss due to saturation voltage and the switching loss can be combined for the linearly current-dependent loss $P_{loss,linear}$ as

$$P_{loss,linear} = \frac{3mk|\cos(\varphi)|}{\pi}\left(NV_0(2-\rho) + \frac{f_P V_{dc}(E_{\text{on}}+E_{\text{off}}+E_{\text{rec}})}{V_{ref}I_{ref}}\right)I_{\text{c}} \quad (3.30)$$

From power loss formula P_{loss} in (3.1), the loss coefficient b_{ac} can be expressed as

$$b_{ac} = \frac{3mk|\cos(\varphi)|}{\pi}\left(NV_0(2-\rho) + \frac{f_P V_{dc}(E_{\text{on}}+E_{\text{off}}+E_{\text{rec}})}{V_{ref}I_{ref}}\right) \quad (3.31)$$

3.3.3 Power Loss Coefficients b_{dc} and c_{dc}

The power loss formula in (3.8) is formulated based on the DC current, I_{dc} with the loss coefficients b_{dc} and c_{dc}. The value of c_{dc} can be derived by substituting (3.6) into (3.1) as

$$c_{dc} = \frac{2NR_{on}(2-\rho)\left(m^2\cos(\varphi)^2+1\right)}{3m^2|\cos(\varphi)|^2} \quad (3.32)$$

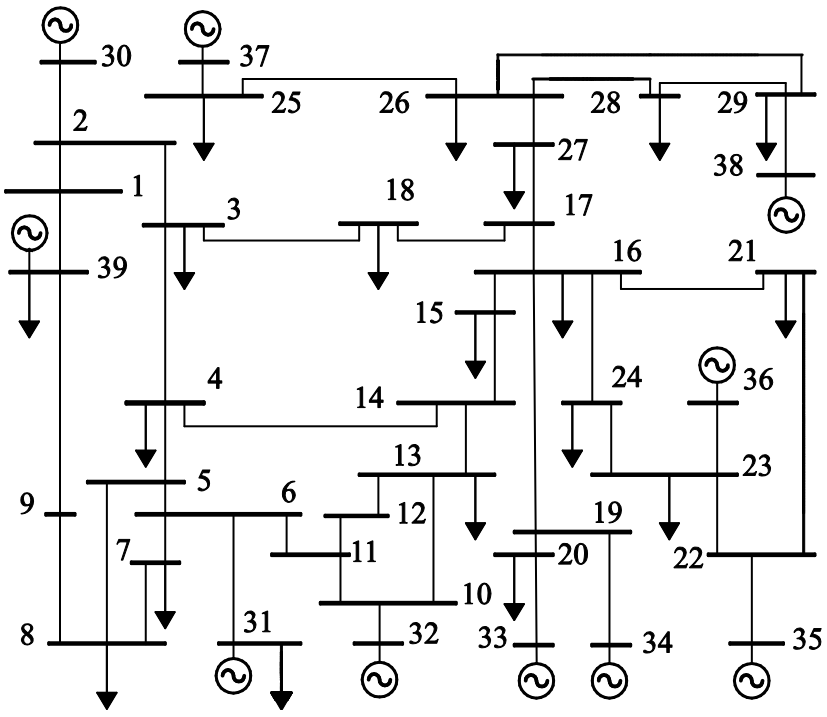
The value of b_{dc} is derived similarly by substituting (3.6) into (3.1) as

$$b_{dc} = \frac{2K}{\pi}\left(NV_0(2-\rho) + \frac{f_P V_{dc}(E_{\text{on}}+E_{\text{off}}+E_{\text{rec}})}{V_{ref}I_{ref}}\right) \quad (3.33)$$

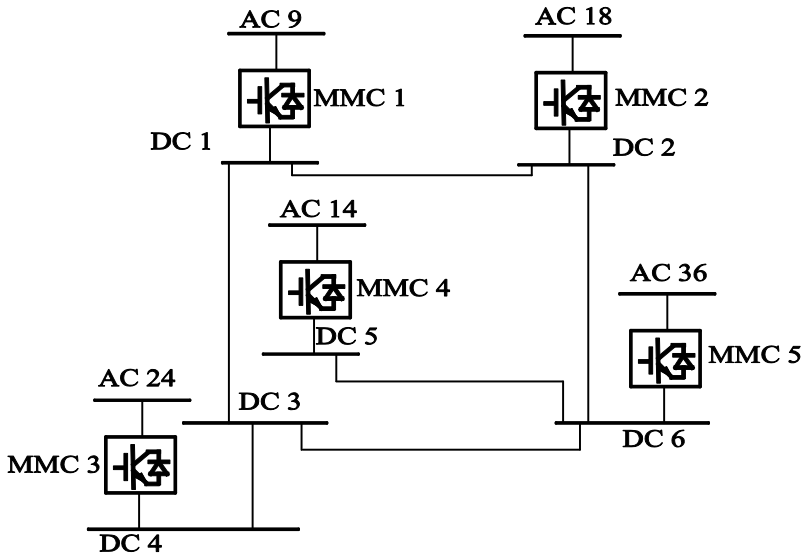
Thus, the converter loss can be calculated directly from the known value of DC current I_{dc} after the DC power flow which eliminates the SBI/DBI in sequential power flow algorithm.

3.4 Simulation Results

The research work leading to modifying generalized converter loss formula as proposed in Section 3.3 with SBI/DBI elimination algorithm is further implemented in MATLAB to test, analyze, and validate the concept in this section. The AC-DC grid in the case studies consists of IEEE New England 39-bus AC grid integrated with a 6-terminal DC system [7]. The schematic diagram of the AC-DC grid is shown in Fig. 3.3. The DC nodes 1, 2, 4, 5, and 6 are connected to the AC grid through five MMC stations. The MMCs that connected to DC nodes 5 and 6 are based on FBSMs, while other MMCs are based on HBSMs. The DC node 3 does not have a converter station tied to the AC grid.



(a) IEEE New England 39-node AC system



(b) MTDC network with MMC stations

Figure 3.3 Schematic diagram of the AC-DC grid

The simulation starts by first implementing conventional sequential AC-DC power flow algorithm [1], [4] and [7] with SBI or DBI and are used as the reference solution. The other part of the simulation comes with eliminating the SBI/DBI in the reference solution.

3.4.1 Accuracy of Loss Coefficients

The loss coefficients in the loss formula (3.1) is verified using IGBT-switching-based detailed model (DM) to obtain the instantaneous and averaged converter losses from which the coefficients b_{ac} and c_{ac} are calculated and are used as the benchmark. The semiconductor data for the MMC loss calculation is listed in Table 3.1.

Table 3.1 MMC HVDC configuration and semiconductor data

Semiconductor Parameter	Detailed Method	Analytical Method
$R_{on,IGBT}$ $R_{on,diode}$	1.21 mΩ 1.07 mΩ	1.14 mΩ
$V_{o,IGBT}$ $V_{o,diode}$	1.82 V 2.27 V	2.05 V
$E_{on,IGBT}$ $E_{off,IGBT}$	11 J 10.5 J	11 J 10.5J
$E_{rec,diode}$	2.8 J	2.8 J
V_{ref}	2.8kV	2.8kV
I_{ref}	1.8kA	1.8kA

For the loss calculation, the DC current i_{dc} is 1560 A; the RMS value of phase current magnitude I_c is 1762A; and the power factor $\cos(\varphi)$ is unity. These calculations are presented in the table and compared. The values obtained show that the loss coefficients are very close in both the cases. Table 3.2 validates that proposed analytical loss formula is quite accurate.

Table 3.2 Comparison of loss coefficients

SM Type	Loss Calculation Method	b_{ac}(p.u.)	c_{ac}(p.u.)
Half Bridge	Detailed Switching Model	$5.4 * 10^{-3}$	$2.3 * 10^{-4}$
	Proposed Analytical Method	$5.7 * 10^{-3}$	$2.3 * 10^{-4}$
Full Bridge	Detailed Switching Model	$8.0 * 10^{-3}$	$4.6 * 10^{-4}$
	Proposed Analytical Method	$8.4 * 10^{-3}$	$4.4 * 10^{-4}$

3.4.2 Comparison of Power Flow Accuracy with and without SBI

The coefficient a in P_{loss} formula is assumed to be $3 * 10^{-3}$, while the values of b_{ac} and c_{ac} from Table 3.2 are used. In this case study, DC node 1 is assumed to be the DC slack bus while the rest of the converters are operating in active power control modes. The results obtained from the conventional AC-DC power flow algorithm with SBI are compared with the results obtained from the proposed algorithm by eliminating SBI at the DC slack bus converter. The power flow calculation results by the two power flow methods are presented in Table 3.3. These results validate that both the two power flow algorithms are producing almost identical values for DC power and converter losses. The DC slack, i.e., DC node 1, presents only 1% difference in the values in DC powers. It is also shown in Table 3.4 that the DC voltages V_{dc} and converter AC side power P_c are almost identical comparing the power flow algorithms with and without SBI.

Table 3.3 Comparison of DC power and converter loss with and without SBI

DC Node	With SBI		Without SBI		Error between P_{dc} and P_{loss} with SBI and Without SBI	
	P_{dc}(MW)	P_{loss}(MW)	P_{dc}(MW)	P_{loss}(MW)	% P_{dc}(MW)	% P_{loss}(MW)
1	-315.72	3.01	-314.67	2.97	-0.33 %	-1.32 %
2	201.84	1.84	201.78	1.84	0 %	0 %
4	80.71	0.71	80.63	0.71	-0.03 %	0%
5	356.56	4.88	356.21	4.88	-0.09%	0%

6	−345.50	4.50	−345.85	4.50	0.1%	0%

Table 3.4 Comparison of DC voltage and converter active powder with and without SBI

DC Node	With SBI		Without SBI		Error between V_{dc} and P_c with SBI and Without SBI	
	V_{dc}(kV)	P_c(MW)	V_{dc}(kV)	P_c(MW)	$\%V_{dc}$(kV)	$\%P_c$(MW)
1	400.00	−318.73	400.00	−317.64	0%	-0.34%
2	384.84	200.00	384.84	199.94	0%	-0.03%
3	392.60	–	392.60	–	0%	–
4	384.20	−341.00	384.20	−341.35	0%	0.1%
5	382.88	351.68	382.88	351.33	0%	-0.1%
6	394.16	−349.00	394.16	−350.35	0%	0.4%

Table 3.5 Comparison of AC nodal voltage with and without SBI

AC Node	With SBI		Without SBI		Error between V_{ac} and δ_{ac} with SBI and Without SBI	
	V_{ac}(kV)	δ_{ac}(degree)	V_{ac}(kV)	δ_{ac}(degree)	$\%V_{ac}$(kV)	$\%\delta_{ac}$(degree)
1	356.76	−16.26	356.77	−16.24	0.002%	-0.12%
2	351.90	−11.10	351.92	−11.13	0.005%	0.3%
3	343.34	−13.34	343.32	−13.34	-0.005%	0%
4	330.41	−14.30	330.43	−14.31	0.003%	0.07%
5	329.23	−13.04	329.23	−13.02	0%	-0.15%
6	329.58	−12.09	329.58	−12.11	0%	0.16%
7	326.30	−15.18	326.31	−15.19	0.003%	0.07%
8	326.34	−16.07	326.34	−16.06	0%	-0.063%

A part of AC power flow results (the voltage phasors of the AC nodes 1-8) using the two power flow algorithms with and without SBI are listed in Table 3.5. It is observed from Table 3.5 that the two AC-DC power flow algorithms give very similar AC power flow results. The other AC node voltages present similar comparison results and are not included due to space limitation.

3.4.3 Comparison of Power Flow Accuracy with and without DBI

The coefficient a in P_{loss} formula is assumed to be $3 * 10^{-3}$, while the values of b_{ac} and c_{ac} are used as mentioned in Table 3.2. In this case, all the converters are in droop control modes except that only the converter at DC node-4 is operated in active power control mode. It is also assumed that the converter at DC node-2 is in outage so the remaining three converters (DC nodes 2, 5, 6) share the power mismatch by droop control. The results of the two algorithms are compared in Tables 3.6−3.8, which validates that the two algorithms produce very close power flow results.

Table 3.6 Comparison of DC power and converter loss with and without DBI

DC Node	With DBI		Without DBI		Error between P_{dc} and P_{loss} with DBI and Without DBI	
	P_{dc}(MW)	P_{loss}(MW)	P_{dc}(MW)	P_{loss}(MW)	$\%P_{dc}$(MW)	$\%P_{loss}$(MW)
1	-174.27	1.60	-174.27	1.55	0%	-3.125%
4	80.71	0.71	80.71	0.71	0%	0%
5	324.57	4.43	324.57	4.39	0%	-0.9%
6	-257.46	3.33	-257.46	3.27	0%	-1.8%

Table 3.7 Comparison of DC voltage and converter active power with and without DBI

DC Node	With DBI		Without DBI		Error between V_{dc} and P_c with DBI and Without DBI	
	V_{dc}(kV)	P_c(MW)	V_{dc}(kV)	P_c(MW)	$\%V_{dc}$(kV)	$\%P_c$(MW)
1	411.12	−175.87	411.12	−175.82	0%	-0.03%
2	407.40	−	407.40	−	0%	_
3	396.96	−	396.96	−	0%	_
4	379.96	−80.00	379.96	−80.00	0%	0%
5	380.60	320.14	380.60	320.18	0%	0.12%
6	401.48	−260.79	401.48	−260.73	0%	-0.02%

The results show that the values as obtained with DBI and without DBI are almost equal with negligible error which elaborates that the elimination of droop bus iteration in sequential power flow algorithm is validated and the algorithm is preserved. The elimination of droop bus iterations are of significant importance in case of large number of droop controlled nodes.

Table 3.8 Comparison of AC nodal voltage with and without DBI

AC Node	With DBI		Without DBI		Error between V_{ac} and δ_{ac} with DBI and Without DBI	
	V_{ac}(kV)	δ_{ac}(degree)	V_{ac}(kV)	δ_{ac}(degree)	$\%V_{ac}$(kV)	$\%\delta_{ac}$(degree)
1	357.28	−16.23	357.28	−16.31	0%	0.5%
2	351.45	−12.28	351.45	−12.25	0%	-0.25%
3	341.96	−14.80	341.97	−14.81	0.003%	0%
4	329.65	−15.06	329.65	−15.08	0%	0.13%
5	329.44	−13.32	329.45	−13.28	0.003%	-0.3%
6	329.85	−12.34	329.85	−12.34	0%	0%
7	326.78	−15.22	326.78	−15.24	0%	0.13%
8	326.85	−16.01	326.85	−16.05	0%	0.25%

3.4.4 Estimation of Computational Burden

The key factor behind the elimination of SBI/DBI is to improve computational efficiency of the power flow algorithm. This can be verified by using 1000 subsequent power flow calculations for IEEE New England 39-bus AC grid integrated with a 6-terminal DC grid. It can be verified that 11% and 23% of total computational burden can be reduced compared to the

conventional AC-DC power flow with SBI/DBI, respectively by applying the proposed method to eliminate SBI/DBI in the sequential AC-DC power flow algorithm. The proposed method with DBI elimination will likely to achieve more significant improvement in computational efficiency when larger numbers of DC droop buses are used in DC grid.

3.5 Approximation in Converter Loss Formulae

The converter loss formula (3.8) using the DC current depends on the power factor cos(φ) as shown in (3.32) and (3.33). This is equally true for the converter loss formula (3.1) using AC current as shown in (3.15) and (3.31). When the converter loss formula (3.1) is used in [4], it is assumed that the coefficients b_{ac} and c_{ac} are constant, which involves approximation/assumption that the power factor is constant. However, the approximation is acceptable because the converter loss accounts for a small proportion of DC/AC transferred power (around 1% per converter station for a half-bridge MMC). Thus, the power factor can be estimated accurately from the AC and DC power flow before the SBI or DBI block. It is possible to implement a new iteration loop inside SBI or DBI (the third iteration loop in addition to the P_c iteration loop and the Newton-Raphson iteration loop in the right-hand portion of Fig. 3.1) to update the power factor, which will make the calculation of P_{ac} more accurate but will increase the computational burden. Similarly, a new iteration loop of the power factor can be added to the loss calculation (3.8) using the DC current, but is not used in the proposed method for calculation efficiency consideration.

The SBI/DBI loop is required when the power flow is formulated as in [4]. Thus, the proposed method can be applied in [4] to eliminate the SBI/DBI. It is noted that the SBI/DBI is not required in the two-building-block algorithm [11]. However, the AC iteration number is increased using the two-building-block algorithm [11] compared to that in [4], since the two-

building-block model uses the AC power flow results to calculate the converter loss of the DC slack bus.

3.6 Conclusion

In this chapter, the performance of the proposed sequential AC-DC power flow algorithm is evaluated by case studies. The conventional AC-DC power flow algorithm is improved by eliminating SBI/DBI with the modifications in the loss formula by replacing the converter current with the DC current after DC power flow. The proposed sequential AC-DC power flow algorithm preserves the accuracy of the power flow and decreases the computational burden thereby to improve computational efficiency of the power flow algorithm.

Simulation results of IEEE New England 39-bus system with 6-bus DC grid validate the performance of proposed algorithm. The simulation results also show that the proposed algorithm can reduce the total computational burden by 11 % and 23 % with SBI and DBI elimination respectively. The proposed method can further improve the calculation efficiency of the sequential AC-DC power flow when larger numbers of DC slack buses are used.

Chapter 4 Conclusion and Future Work

4.1 Introduction

This chapter provide a summary of the topics covered in this research. It also recommends possible future research directions that can be persuaded on the basis of the results presented in this thesis.

4.2 Thesis Conclusion

The MMC HVDC is emerging technology for large scale renewable energy integration into conventional AC grid and enabling MTDC networks. MMC has lower losses and reduced converter footprint compared to the conventional two- or three-level converter technologies. MMC can independently control the active and reactive power injections which is advantageous compared to the conventional LCC HVDC. When implementing sequential AC-DC power flow algorithm, during each AC and DC power flow iteration, the DC slack bus iteration or droop bus iteration is required to update the convertor loss of the DC slack bus or droop buses. This causes additional iterations and therefore leads to extra computational burden to the AC-DC power flow algorithm. This thesis aims to eliminate DC slack bus iteration or droop bus iteration by using the power balance principle between AC side and DC side of the converter while maintaining the accuracy of the AC-DC power flow.

The essential idea of this thesis is to eliminate DC slack bus iteration or droop bus iteration which is made possible when the analytical power loss formula is modified to with the help of the power balance principle of an AC/DC converter.

This thesis contains four chapters. The first chapter elaborates the technical background of the topic with brief explanation of the motivation of the research work. It also details the operation of VSC converter station with emphasis on various converter control modes. The MMC converter is briefly explained and the voltage droop in parallel operation of VSC converter is discussed.

Chapter 2 explains the power flow models for AC and DC grids. It introduces converter station model, converter losses, and AC-DC power flow equations. The chapter provides the logical explanation of including the DC slack bus iterations/droop bus iterations in each iteration of sequential power flow algorithm.

Chapter 3 provides the reason for eliminating the slack bus iterations/droop bus iterations in sequential power flow algorithm. It discusses the power loss formula and apply power balance principle of the AC and DC system that provides the foundation for modifying the loss coefficients in power loss formula and as a result, the slack bus/droop bus iterations can be removed in each iteration. The loss coefficients in the loss formulae are derived analytically based on MMC operation characteristics. Simulation studies are performed to evaluate the overall performance of the proposed sequential AC-DC power flow algorithm with the elimination of slack bus iteration or droop bus iteration. Simulation results show that the elimination of slack bus iteration or droop bus iteration has significantly improved the computational efficiency of sequential AC-DC power flow. The results demonstrate that the proposed AC-DC power flow algorithm is accurate and can reduce the total computational burden by 11% and 23% with the elimination of slack bus iteration or droop bus iteration, respectively. The proposed method can further improve the calculation efficiency of the sequential AC-DC power flow when larger numbers of DC slack buses are used.

4.3 Future Work

In this research, the conventional AC-DC sequential algorithm is improved by eliminating slack bus iteration or droop bus iteration, which reduces the computational burden by 11% and 23%, respectively for IEEE New England 39-bus system with 6-bus DC grid. In order to further improve simulation efficiency of the sequential AC-DC power flow algorithm, other modifications will be sought after in terms of the overall sequential power flow solution framework. For example, it will be very desirable if the AC power flow can be excluded from the overall iteration loop while only the DC power flow is iterated for the AC-DC power flow solution. Thus, the computational efficiency is greatly enhanced with straightforward implementation in commercial power system simulation packages since the AC grid has normally much larger scale in terms of bus number than that of the DC grid. Therefore, future research can be focused on new sequential AC-DC power flow algorithm with only iterative DC grid power flow solution.

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