INVESTIGATION OF SOLUTIONS FOR UNIVERSAL INPUT 208 V-480 V THREE-PHASE AC/DC POWER FACTOR CORRECTED CONVERTERS WITH 400 V DC OUTPUT

by

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Abstract

A high-performance, three-phase power factor corrected (PFC) front-end converter with universal input (i.e. 208 V-480 V AC) and 400 V DC output voltage is desirable for applications including Electric Vehicle (EV) battery chargers and data centers. Products that operate with a universal input reduce development and manufacturing costs, in lieu of multiple products for different values of AC input voltages. Three-phase AC inputs reduce the cost of electric circuit cabling and a 400 V DC output is favorable as it reduces the stress on the back-end isolated DC/DC converter stage between the PFC converter and DC output.

This dissertation focuses on the best practices and solutions for a universal three-phase AC input PFC converter with 400 V DC output. A detailed review of existing solutions is presented with their advantages and drawbacks noted. The conventional solution of three phase boost follows buck was prototyped and used as a benchmark against the proposed solutions. An adaptive intermediate bus voltage control method is proposed to maximize the efficiency in a three-phase six-switch boost-follows-buck converter. A prototype was developed and experimentally tested to confirm the expected efficiency improvement. In addition, a novel truly universal input (i.e. single-phase or three-phase) PFC with 400 V DC output is also proposed and implemented which can serve the dual purpose of single-phase and three-phase operation. It is shown by analysis and experiments that this solution is not only highly efficient for both single-phase and three-phase operation, but also the components sized for single-phase mode of operation are not oversized for three-phase. Finally, a novel universal input single-stage SEPIC based third harmonic injection three-phase AC/DC PFC is proposed. Control simplicity and single-stage operation are among the main features for this topology.

Lay Summary

Battery chargers and Data centers need direct current electricity for operation, thus converters are used to change the alternating input mains into Direct Current (DC) electricity.

Electricity is available in single-phase (two wires) and three-phase (three-wire) form. Three-phase is more economical for high power applications. Moreover, alternating current (AC) mains voltages vary in different geographical regions, typically from 200 to 480 volts. 400 volts direct current (DC) output is the typical voltage that is favorable for designers, as with this output voltage for converter, conventional electronic parts can be used. Finally, electrical codes require that the converter current be a sinusoidal shape and in phase with the voltage.

The focus in this study was to develop novel and highly efficient solutions that can integrate the four important features: universal AC input, three-phase, 400 volts DC output and sinusoidal input current which is in phase with input voltage to comply with electrical code requirements.

Preface

This thesis has six chapters that present the discussion and the results of the proposed solutions to universal AC input PFC with 400 V DC output. All the research, data analysis, prototyping and discussion of results were performed by myself. I prepared and wrote the published manuscripts and my co-authors provided supplemental input in the areas of design, analysis and experimentation in addition to editorial guidance for written work.

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List of symbols

V_{l-l}	Line-to-line voltage
V_o	Output voltage
V_d	Direct axis voltage
V_q	Quadrature axis voltage
V_m	Peak line to neutral voltage
$\mathrm{I}_{\mathrm{ripple\_max}}$	Maximum ripple current
L	Inductance
Δi_L	Inductor peak-to-peak ripple
f_{sw}	Switching frequency
ΔQ	Change in electric charge
C	Capacitance
ΔV	Voltage ripple
M	Modulation index
ω	Angular frequency
f_{line}	Line frequency
V_{ac_min}	Minimum input ac line-to-neutral voltage
D	Duty cycle
V_{DC}	DC voltage
E	Switching energy
B_{pk}	Maximum flux density
r	Percentage of ripple current

Acronyms

AC	Alternating current
PFC	Power factor correction
DC	Direct Current
PF	Power factor
THD	Total harmonic distortion
SEPIC	Single ended primary –inductor converter
SVM	Space vector modulation
SVPWM	Space vector pulse width modulation
DSP	Digital signal processor
IC	Integrated circuit
EMI	Electromagnetic interference
MOSFET	Metal oxide semiconductor field effect transistor
SiC	Silicon carbide

Prefixes for SI units

p	Pico (10^{-12})
n	Nano (10^{-9})
µ	Micro (10^{-6})
m	Millie (10^{-3})
k	Kilo (10^{3})
M	Mega (10^{6})
G	Giga (10^{9})

Acknowledgements

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I also would like to thank my wife for all the support and sacrifice she made for this work to happen. My twins Parsa and Pardis for all the week-ends and evenings they spent without me.

Dedication

To my family

Chapter 1: **Introduction**

1.1 **Foreword**

The front-end AC/DC converter in applications such as battery chargers or data centers should be power factor corrected (PFC) to avoid utility bill surcharges [1] and comply with standards that limit the input current harmonics [2]. For high power applications, three-phase front-end PFC's are favorable as they can reduce the cost of cables [3], [4]. Moreover, a universal AC input mains PFC can significantly reduce the cost of developing multiple products for the companies. 400 V DC output is common for PFC stages in power supplies and battery chargers, typically followed by an isolated DC/DC converter using 600 V rated Silicon devices [5],[6]. Studies have shown that a 400 V DC distribution system is favorable in data center applications and has been adopted for other industrial applications [7], [8]. Therefore, based on the above discussion, a PFC front-end converter with universal AC input capability, three-phase AC mains input and 400 V DC output is highly attractive for kW level power applications.

This thesis focuses on new solutions that can achieve the goals mentioned above – specifically, high efficiency low cost three-phase universal AC input PFC with 400 V DC output.

1.2 **General background**

The AC/DC converter used as front-end should be power factor corrected to comply with permissible input harmonics outlined in [2] and avoid surcharge on utility bill [1]. Power factor in an AC input converter is defined as:

$$PF = \frac{Real\ power}{Apparent\ power} \qquad \textbf{1-1}$$

Where PF is the power factor, real power is the power consumed by the converter and the *apparent power* is the input current times the input voltage. For an ohmic load, where voltage and current are in phase sinusoids, real power and apparent power are equal. Therefore, PF is one. However, for inductive or capacitive loads, there is a phase shift between current and voltage and the PF is given by:

$$PF = \frac{VI\cos\theta}{VI} = \cos\theta \qquad \textbf{1-2}$$

For non-linear loads, such as an uncontrolled AC/DC rectifier, the input current is not a pure sinusoid and contains harmonics along with the fundamental component. The PF in this case is influenced by the distortion in the waveform and is given by:

$$PF = \frac{1}{\sqrt{1 + THD^2}}\cos\theta \qquad \textbf{1-3}$$

Where THD is Total Harmonic Distortion and is defined as:

$$THD = \sqrt{\frac{\mathrm{I_{rms}}^2 - \mathrm{I_{1rms}}^2}{\mathrm{I_{rms}}^2}} \qquad \textbf{1-4}$$

With I_{rms} as the input rms current and I_{1rms} being the fundamental component.

Although, uncontrolled AC/DC rectifiers are easier to implement, they do not have a high PF and cannot regulate the output voltage. Therefore, PFC AC/DC converters have been developed to comply with power quality standards as in [2] avoid surcharge on utility bill [1] and have output voltage regulation. Utility voltages around the world have different values and are available in single-phase and three-phase. For single-phase, two conductors are used to supply power (i.e. phase and neutral wires). Three-phase AC mains uses three wires and as the phases are 120 degrees phase shifted, the sum of the currents is zero at any instant and therefore a neutral wire is not theoretically needed, which helps reduce cabling costs. Table 1-1 summarizes the global AC voltages.

Table 1-1 Typical global AC voltages

Geographical Region	Line-to-Neutral Voltage [V_{LN}]	Line-to-Line Voltage [V_{LL}]
Japan	100	200
North America (low-line)	120	208
Asia and Europe	230	400
North America (high-line)	277	480

A universal input PFC converter that operates across the global three-phase AC input voltage range significantly reduces product development and manufacturing costs and is one of the goals for this study.

1.3 **Literature review**

Three-phase universal AC input front-end PFC with 400 V DC output, inherently requires a converter which needs to have step-down (i.e. buck) and step-up (i.e. boost) capability. Various controlled and uncontrolled classifications of three-phase AC/DC PFC converters can be found in the literature [11], [14]. However, as the focus of this study is 400 V DC output and universal AC input therefore, only controlled rectifiers that can achieve PFC and output regulation are considered. In the following sub-sections, different three-phase boost and buck topologies are reviewed first and then the existing universal AC input solutions are investigated. The results of the discussions will be used to modify the existing solutions, derive and develop new topologies as proposed later in this thesis.

1.3.1 **Three-phase boost converters**

The output voltage of Boost AC/DC PFC Converters should be greater than the peak of input line-to-line voltage to keep PFC status and output voltage regulation [7]. In the following subsections, the most common step-up (i.e. boost) topologies are reviewed.

1.3.1.1 **Three-phase six-switch AC/DC PFC**

The six-switch converter, illustrated in Figure 1-1, is a boost two-level converter with bidirectional capability. The operation and control of this converter is presented in [7].

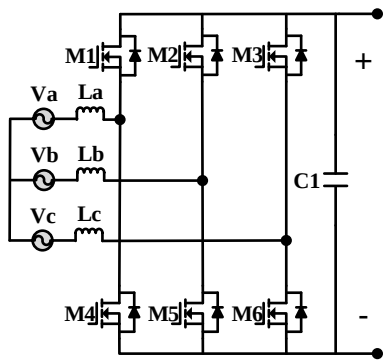

Figure 1-1 Three-phase six-switch AC/DC PFC converter

The voltage stress on the switches is clamped to the output voltage. This converter can also handle failure of one of input phases and operate with two phases. Six-switch power modules are commercially available making implementation somewhat simplified. In order to maintain output voltage regulation and PFC:

$$V_O \geq \sqrt{2}\, V_{l-l} \qquad \textbf{1-4}$$

Where V_O is the converter output voltage and V_{l-l} is the input three-phase line-to-line input voltage. From equation (1-4), for a universal input voltage of 208 V-480 V, assuming a 10 % permissible overvoltage margin, the output voltage should be approximately 800 V to maintain PFC status. This will make losses very high at 208 V (low-line) with the next stage operating at 800 V DC.

1.3.1.2 **Three-level boost AC/DC PFC rectifier**

Figure 1-2 shows a three-level boost topology known as the Vienna rectifier. Different pros and cons for this converter are discussed in [8]. The voltage stress on switches is clamped to half of output voltage as compared to two-level topologies i.e. six-switch boost where the voltage stress equals the bus voltage .Simple structure power and control circuit with only one switch per phase are among the major advantages. On the other hand, the topology is unidirectional and cannot be used where bidirectional capability is desired. Figure 1-3 depicts the alternative bridge leg

configurations. The variant (a) only has three transistors but since two diodes conduct in series with switch in every instant, the conduction losses are higher compared to the other version of Vienna rectifier in (b) and (c). (b) has the advantage of pre-charge for the output capacitors. After the pre-charge cycle is finished, the thyristor is gated and by-passes the charging resistor and series diode. (c) Further reduces the conduction losses compared to (b) [10].

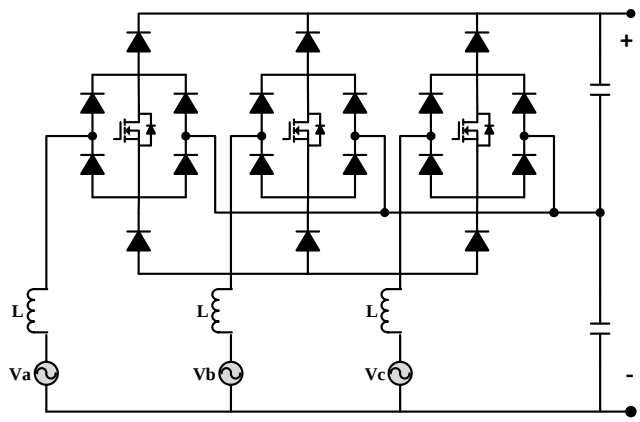

Figure 1-2 Vienna rectifier

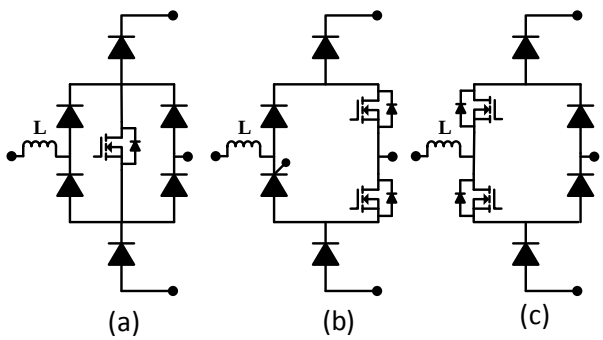

Figure 1-3 Vienna rectifier variants: a) Original Vienna Leg, b) Addition of pre-charge thyristor, and c) the version with the highest efficiency

Another variant of Vienna rectifier is shown in Figure 1-4 [12]. This three-level structure has the advantage of reducing the voltage stress on the switches to half the bus voltage. The increased number of levels helps to reduce the switching voltage across the inductor reducing the inductor current ripple, or enabling the use of smaller inductors in comparison to two level topologies. Moreover, as a result of lower switched voltage, a lower conducted EMI noise level is generated.

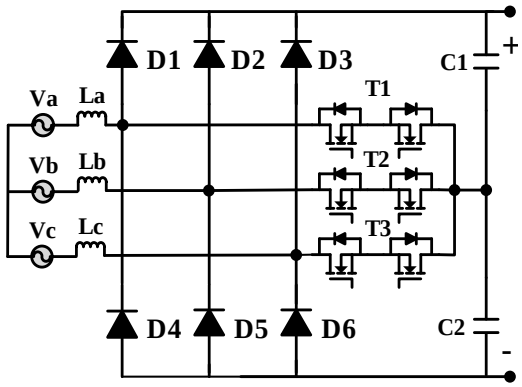

Figure 1-4 Three-phase three-level boost converter

1.3.1.3 Three-phase third harmonic injection boost rectifier

Figure 1-5 shows a third harmonic injection boost AC/DC converter [16]. The current in the inductors *L1* and *L2* can be controlled independently and proportional to the phase voltages. The bidirectional switch connected to the phase with a voltage value between the other two phases is always on and the sum of the current in the other two phases is injected into this phase. Since the sum of currents in a three-wire system is zero and the fact that the currents in the other phases are proportional to the other phase voltages, the current of the third phase will be power factor corrected as well.

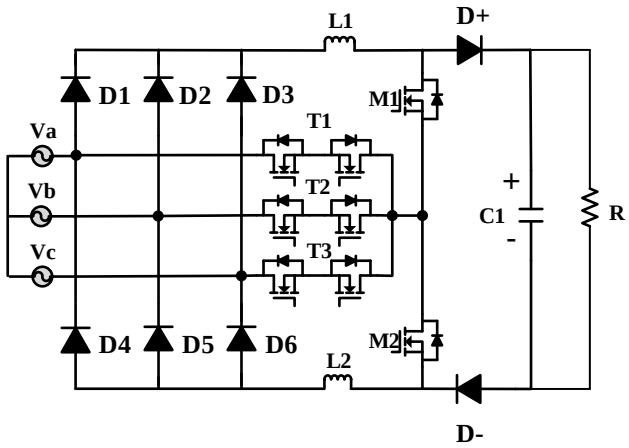

Figure 1-5 Three-phase third harmonic injection boost

1.3.2 Three-phase buck converters

For three-phase buck converters, the output voltage is less than the peak of input line-to-line voltage. Therefore, these converters are suitable where a DC bus voltage less than the input peak line–to line voltage is desired.

1.3.2.1 **Three-phase six-switch buck converter**

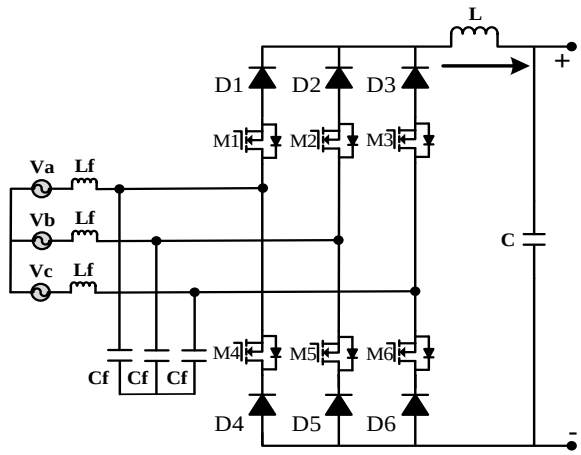

Figure 1-6 Three-phase six-switch buck PFC

The three-phase six-switch buck PFC [11], illustrated in Figure 1.6, is formed by inserting switches in series with the diodes of a full-bridge three-phase diode rectifier, and the addition of input and output LC filters to extract the fundamental component of the input current and output DC voltage. By modulating switches M1-M6, the input current is sinusoidal after being filtered by the input LC filter. By changing the duration of the freewheeling state, the output voltage can be controlled in the range:

$$0 < V_o < \sqrt{\frac{3}{2}}\, V_{l-l} \qquad \textbf{1-5}$$

Where V_o is the output voltage and V_{l-l} is the input line to line voltage. The upper limit comes from the fact that for the highest output voltage, the two largest input voltages are selected at any instant. As these voltages are 60º phase shifted, therefore at cross section of these two waveforms the voltage is $\sqrt{\frac{3}{2}}\, V_{l-l}$. Therefore, to maintain output voltage controllability and achieve PFC, the output voltage is limited to this value.

1.3.2.2 **Three-phase third harmonic injection buck rectifier [17]**

This converter uses the same concept as in the third harmonic injection boost previously described, except that the boost switches and diodes are placed in the buck type configuration as provided in Figure 1-7. The rectifier diodes are not commutated with switching frequency;

therefore, diodes with small voltage drops (i.e. higher reverse recovery time) may be used to reduce conduction losses.

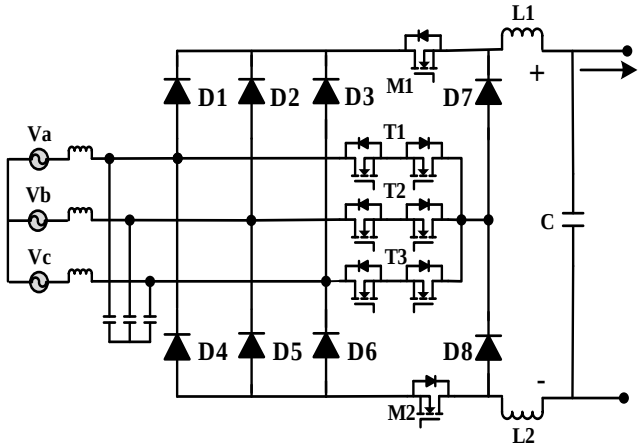

Figure 1-7 Active third harmonic injection buck converter (aka the Swiss rectifier)

1.3.2.3 **Active three switch/phase buck converter [48]**

By inserting four-quadrant switches, as in Figure 1-3(a) into a full-bridge diode rectifier and merging the diodes of the four quadrant switches into the bridge, the topology illustrated in Figure 1-8 is derived. As compared to conventional three-phase buck topology of Figure 1-6 with six switches, this topology has only three switches but has two diodes in current path of each leg making it less efficient.

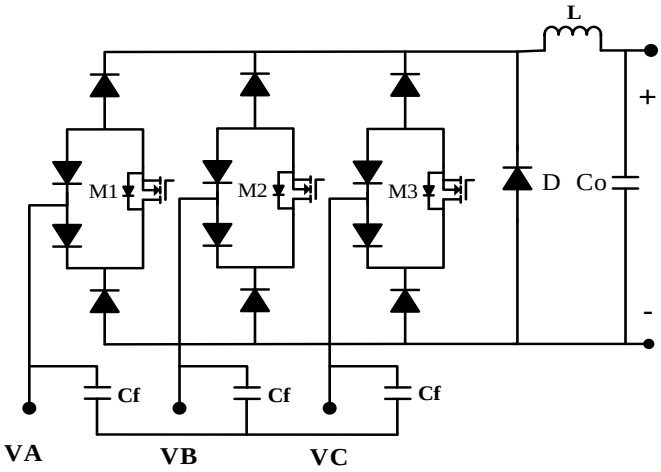

Figure 1-8 Active three switch/phase buck converter

1.3.3 **Universal AC input three-phase PFC converters**

A universal input three-phase PFC converter must be capable of both boost (i.e. step-up) and buck (i.e. step-down) operation. Only boost and only buck converters cannot operate with

universal input and provide 400 V DC output. The three-phase only boost, or only buck AC/DC PFC topologies reviewed in previous sections may be modified, or combined together to provide a single-stage or two-stage universal input solution. In the following sub-sections, universal AC input solutions are reviewed.

1.3.3.1 **Single-stage converters**

Single-stage topologies are derived from DC/DC buck-boost, SEPIC and Ćuk converters. They have a lower component count compared to two-stage solutions, but they also have higher voltage and current stresses on many of the powertrain components. The topology in Figure 1-9 is derived from a DC/DC SEPIC architecture. It has one additional diode and capacitor in each phase leg. This converter features a simple three-level structure, full-controllability of the power flow (independent of the level of the output voltage), sinusoidal input and a simple structure. However, due to its SEPIC-derived structure, the stress on the components are higher compared to boost and buck type solutions.

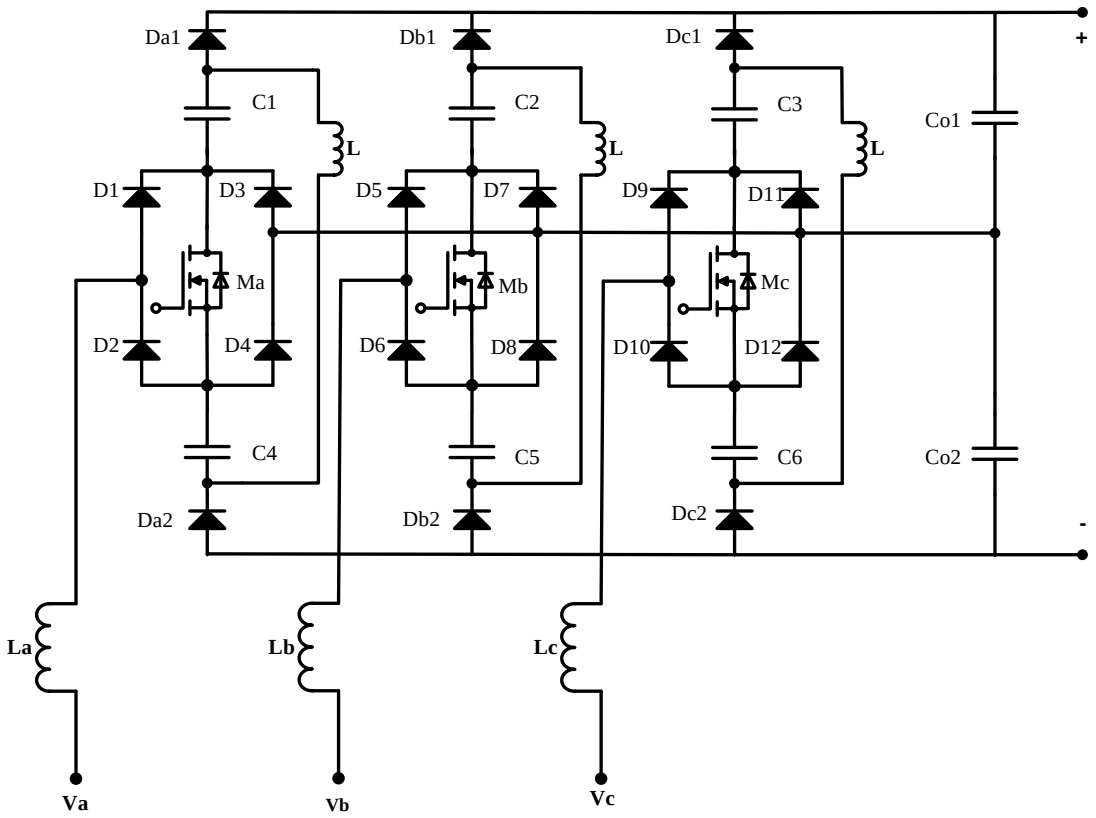

Figure 1-9 Three-phase/Level/Switch AC/DC PFC

A control method for a single-stage, three-phase AC/DC Ćuk-derived converter, Figure 1-10, and its isolated version, were presented in [16]. In this approach, compared to a two-stage topology, the switches need to handle a higher current stress, since at the zero vector instants the output inductor and input inductor phase currents sum, thus increasing the peak and rms currents in the switches.

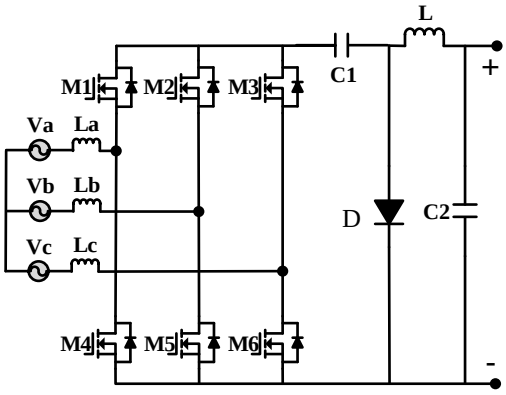

Figure 1-10 Three-phase single-stage boost-buck PFC

A three-phase single-stage buck-boost PFC converter [38] is shown in Figure 1-11. For a universal AC input design, the current stress in the inductor, when operating in step-down mode, can be several times the load current [39]. The implication for high power design is that the inductor must be physically large and therefore lossy, and the switches must also handle higher currents as compared to a two-stage buck-follows-boost or boost-follows-buck solution.

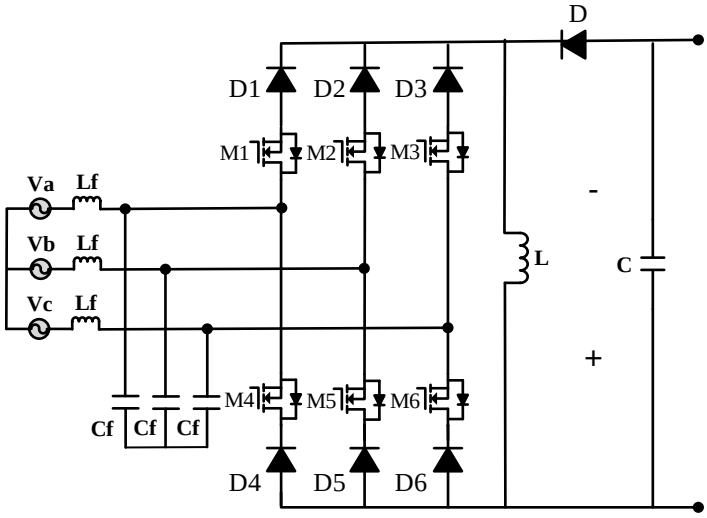

Figure 1-11 Three-phase single-stage buck-boost PFC

1.3.3.2 **Two-stage converters**

The boost-follows-buck two-stage topology, illustrated in Figure 1-12, can also be used for three-phase universal input and 400 V DC output PFC applications, where the first stage buck performs rectification and PFC, and the second stage boost performs DC/DC regulation. The conventional three-phase buck PFC is presented in [11]. This converter followed by a DC/DC boost stage forms a universal input three-phase PFC [40]. An advantage is that a single inductor serves both the buck and boost stages. However, at a low AC input line voltage, the inductor carries a current at least two times the load, therefore requiring a bulky inductor. Finally, unless the diodes are replaced with switches, boost-follows-buck converters are unidirectional and cannot be used for applications such as vehicle-to-grid (V2G), where a battery charger with bidirectional capability is required. A bidirectional three-phase buck PFC combining two buck PFCs in opposite directions is presented in [41]. With this approach, only one converter is working at a given time, so power density is low, and cost is twice that of a unidirectional buck.

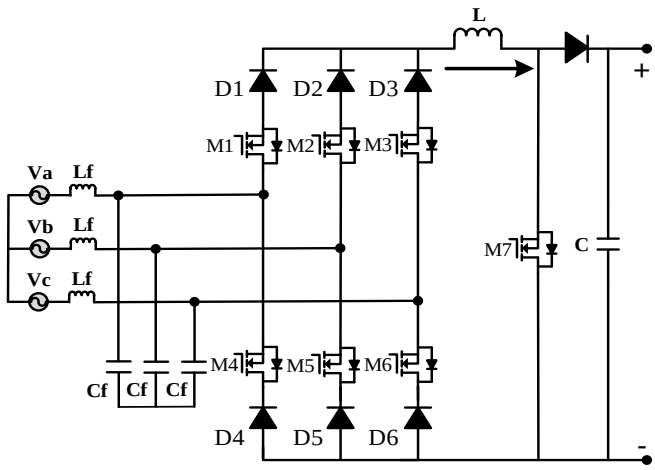

Figure 1-12 Three-phase cascaded buck-boost PFC

Based on the above sections, single-stage topologies with either buck or boost capability could not provide 400 V DC for a universal AC input three-phase of 208-480 V. Single-stage topologies with buck-boost capability had higher voltage and current stresses as compared to two stage topologies. Two-stage solutions can be either buck followed by boost or boost followed by buck, three-phase buck followed by boost is unidirectional and not suitable for applications where inversion mode is required. A three-phase six-switch boost converter followed by a synchronous

buck (i.e. buck-follows-boost) is illustrated in Figure 1-13. This is a bidirectional two-stage approach featuring reduced component stress compared to single-stage three-phase PFC and is well suited for three-phase universal input and 400 V DC output PFC applications.

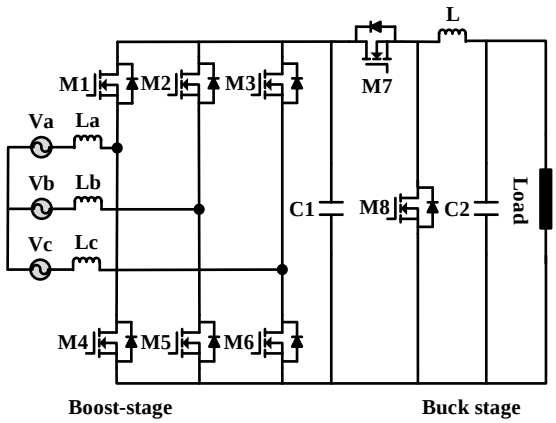

Figure 1-13 Three-phase cascaded boost-buck PFC

1.4 **Summary**

A front-end PFC converter with universal AC input capability, three-phase AC mains input and 400 V DC output is required for kW level power applications. Single-stage and two-stage solutions have been proposed in the literature and presented here. However, given relative advantages and disadvantages, it is generally accepted that the three-phase buck follows boost architecture, illustrated in Figure 1-13, is considered to the most common benchmark architecture. Therefore, this topology is fully analyzed in Chapter 2: and the results are used as benchmark for the work proposed in Chapters 3-5. In Chapter 3: a single stage SEPIC-derived AC/DC power factor correction solution is proposed to increase efficiency and reduce cost as compared to the two-stage benchmark. Chapter 4: proposes an adaptive intermediate bus voltage to increase efficiency as compared to 800 V fixed bus in the benchmark. Lastly, in Chapter 5: a topology is proposed that operates with single-phase, or three-phase AC inputs, therefore providing a truly universal input solution.

Chapter 2: **A benchmark universal input three-phase six-switch boost plus buck AC/DC PFC with 400 V DC output**[1]

The three-phase six-switch boost plus buck converter architecture, discussed in section 1.3.3.2, is a two-stage, bidirectional, industry standard, AC/DC PFC that can operate with a three-phase universal 208-480 V AC input and provide 400 V DC output. The aim of this chapter is to develop a benchmark to compare with the contributions proposed in Chapters 3-5.

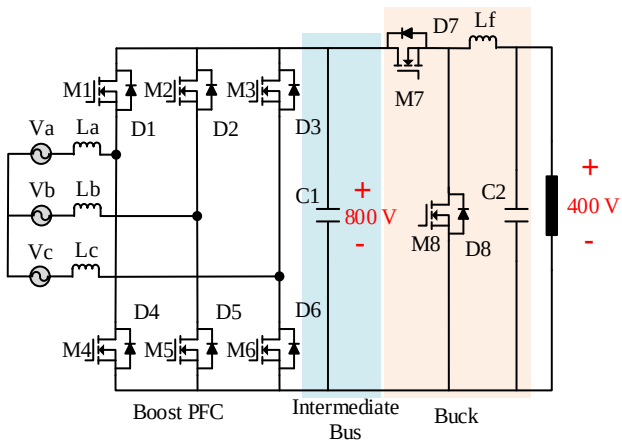

Figure 2-1 Conventional two-stage six-switch boost plus buck universal AC input PFC

2.1 **Converter specifications**

Table 2-1 summarizes the specifications for the two-stage universal input cascaded boost plus buck converter architecture, illustrated in Figure 2-1. The design of the powertrain along with the control are described in the following sub-sections.

[1] The experimental results of the conventional and industry standard three-phase buck follows boost topology developed in this chapter were used as a benchmark against the proposed methods in chapters 4&5. These results were also published in [50],[60]

Table 2-1 Specifications of the benchmark prototype

Specification	Value
Rated power	5 kW
AC Mains (nominal)	200-480 V 3~
AC line frequency	50-60 Hz
Switching frequency (for Boost & Buck stages)	50 kHz
Output Voltage	400 V DC

2.2 **Converter design**

The specifications in Table 2-1 are used to size active and passive components and aid the control design for the boost and buck stages.

2.2.1 **Control and modulation**

A simplified block diagram for the digital implementation of the proposed converter is presented in Figure 2-2. DQ control and space vector modulation (SVM) are used to control the boost PFC stage [22] and voltage mode control was selected for the buck stage.

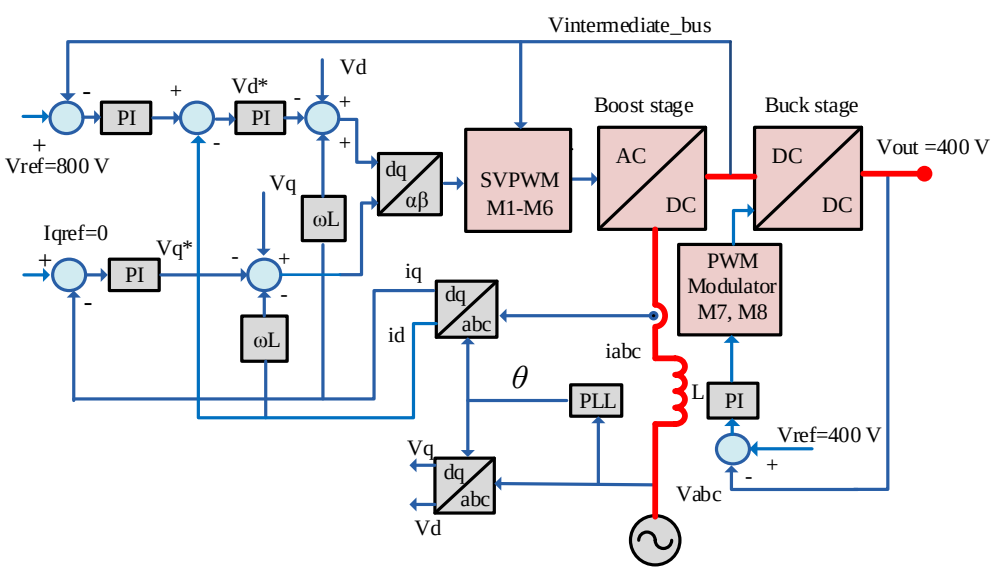

Figure 2-2 Control diagram for the universal AC input two-stage cascaded boost plus buck PFC

2.2.1.1 **DQ control**

The equation describing the voltage and current through the boost inductor, neglecting the ohmic resistance, is:

$$v_{n1} = v_n - L\frac{di_n}{dt} \qquad \textbf{2-1}$$

In equation (2-1), n denotes phases a, b and c and L is the phase inductance. v_n is the phase voltage and v_{n1} is the inductor voltage on the converter side, using the abc/dq rotating frame transformation [22]. DQ control, as shown in Figure 2-2, was used to implement the control for this converter.

2.2.1.2 **Space vector modulation (SVM)**

The boost PFC stage modulation technique has an impact on the efficiency since the number of switching transitions can vary between various modulation techniques. The boost PFC converter can be driven either by carrier-based pulse width modulation (CBPWM), or SVM. SVM is more commonly used due to its simplicity [7] and was selected for this work. Specific SVM strategies include discontinuous space vector modulation (DPSVM), which has four transitions in a switching cycle, and symmetrical vector pulse width modulation (SVPWM), which has six transitions, as illustrated in Figure 2-3 [22]. DPSVM has lower switching losses but higher ripple current, leading to higher THD, and increased core and copper losses in the boost inductors. Due to these drawbacks with DPSVM, SVPWM was used for both the analysis and experimental verification of this work.

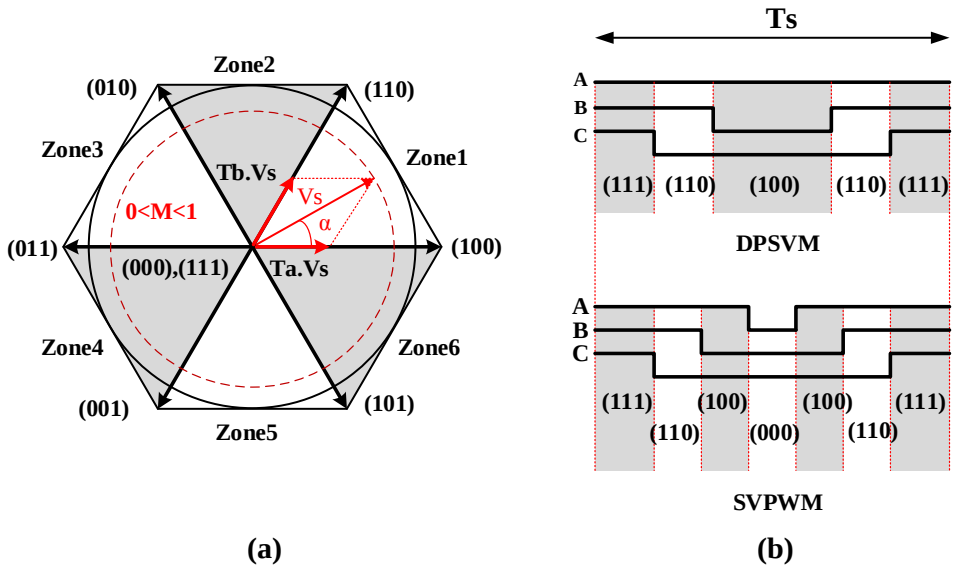

Figure 2-3 (a) Synthesis of rotating vector using adjacent switching states, (b) Switching Pattern for DPSVM and SVPWM [7]

2.2.1.3 **Buck stage voltage mode control**

For the buck stage, voltage mode control with soft-start is used [21].

2.3 **Powertrain design**

The specifications in Table 2-1 are used to size the active and passive components for both boost and buck stages.

2.3.1 **Boost inductors**

The boost inductors are sized based on a maximum target ripple current and the power level they need to handle. These criteria are used to choose the magnet wire gauge, core size and material. The maximum ripple is important as it impacts core loss, and the EMI filter size. The analytical formula to calculate the maximum inductor ripple in a three-phase voltage source inverter is presented in [19] and is applicable to the three-phase boost converter. Given the boost inductor L, DC output voltage V_{DC}, peak line-to-neutral voltage V_m, switching period T_{sw}, and modulation index $0 < M = \frac{\sqrt{3}V_m}{V_{DC}} < 1$, the maximum ripple current is:

$$I_{ripple\_max} = \frac{V_{DC}T_{sw}}{6L}M \qquad \textbf{2-2}$$

In the worst case, assuming 10% overvoltage in the AC mains, $V_m = 277\sqrt{2} + 10\% = 431\,V$. Also by assuming 20% ripple in the inductor at low-line, and, $V_{DC} = 800\,V$, to maintain PFC and output voltage regulation for all AC mains input 208-480 V, a value of L= 500 $\mu\mathrm{H}$ is calculated.

2.3.2 **Buck inductor**

The buck inductor value can be calculated as follows as given in [39]:

$$L = \frac{V_o(1-D)}{\Delta i_L f_{sw}} \qquad \textbf{2-3}$$

Where V_o is the output voltage, D duty cycle, f_{sw} switching frequency, and Δi_L is the peak to peak of ripple current. For a power level of 5 kW and 400 V DC output, the DC inductor current is 12.5 A. Assuming f_{sw}= 50 kHz, Δ_{i_L}= 8 A, and D = 0.5, with an 800 V intermediate bus voltage, a buck inductor value of L = 500 $\mu\mathrm{H}$ is chosen.

2.3.3 **Boost stage capacitor**

In a balanced three-phase PFC system, the instantaneous output power is constant as follows:

$$p(t) = p_a(t) + p_b(t) + p_c(t) = const \qquad \textbf{2-4}$$

Thus, the output capacitor only needs to compensate for the distortion power associated with high frequency ripple in the phase currents. The maximum ripple current is given in (2-4). Assuming ΔV_o is the desired peak-to-peak voltage ripple, and combining (2-4) and the charge equation for the capacitor, i.e. $\Delta Q = C\Delta V$, then the capacitance is given as follows:

$$C_1 = \frac{V_{DC}{T_{sw}}^2}{6\Delta V_o L} M \qquad \textbf{2-5}$$

For $V_{DC} = 800\,V$, M = 1, $\Delta V_o = 30V$, $T_{sw} = \frac{1}{50{,}000}s$, the output capacitor $C_1 = 3.6\ \mu\mathrm{F}$. In practice, the capacitor needs to be oversized to handle unbalanced mains and de-rating, or total loss of one phase. The worst case is the loss of one phase where the converter will operate at $P_{ph\_loss} = \frac{P_o}{\sqrt{3}}$ in this case the output power will contain double line frequency ripple therefore:

$$p(t) = P_o + P_o\cos(2\omega t) \qquad \textbf{2-6}$$

Assuming the output power is constant, the variable term needs to be compensated by the output capacitor. Using power equations, it can be shown that the output capacitor C_1 needed to compensate the variable AC term equals:

$$C_1 \geq \frac{P_o}{2\pi f_{line} V_o \Delta V_o} \quad \textbf{2-7}$$

Where V_o is the boost converter output voltage, P_o is output power, f_{line} is the line frequency and ΔV_o is the output ripple peak voltage. Assuming $P_o = 5kW$, $f_{line} = 60$ Hz, $\Delta V_o = 20\ V$

$C_1 \geq 957$ μF.

The current stress can be calculated as described in [20]:

$$I_{c1\_rms} = \sqrt{\frac{8\sqrt{2}{P_o}^2}{3\pi V_{ac.min} V_o} - \frac{{P_o}^2}{{V_o}^2}} \quad \textbf{2-8}$$

Using the same assumptions as in (2-7) and by plugging $V_{ac.min} = \frac{208}{2} V$ into (2-10), the current stress $I_{c1\_rms} = 13.72\ A$.

2.3.4 **Buck stage output capacitor**

The value of output capacitor for the buck stage may be calculated as in [39] as follows:

$$C2 = \frac{1 - D}{8L(\frac{\Delta Vo}{Vo}){f_{sw}}^2} \quad \textbf{2-9}$$

Assuming D = 0.5, L= 500 μH, f_{sw}= 50 kHz, V_O = 400 V, and ΔVo = 20 V, then $C2 = 1$ μF. The capacitor current stress equals the rms ripple current of the inductor, $\Delta i_L = 8\ A$. The rms value of a triangular waveform equals [39]:

$$I_{C2\_rms} = \frac{\Delta i_L}{2\sqrt{3}} \quad \textbf{2-10}$$

Therefore, $I_{C2\_rms} = 2.31\ A$. A 1 μF capacitor cannot handle this current stress and larger capacitors need to be chosen. As an example a 1 μF (400 V) capacitor with part number ECA-2GM010B can handle only 32 mA at 120 Hz. For this study two 330 μF electrolytic capacitors with part number ALC40A331DF450 were selected to be in series providing 165 μF of capacitance.

2.3.5 **Boost and buck stage switch sizing**

Sizing switches for the boost and buck stages starts by determining the current and voltage stresses for these components. SiC switches and diodes were selected due to their lower switching loss compared to Si switches. The PSIM power circuit simulator was used for stress estimation. As a first estimate, the specifications of a CREE CCS020M12CM2 six-pack module were used to model switches M1-M6 and diodes D1-D6. M7 and M8 were modeled using CREE C2M0025120D and finally C4D20120D from CREE were used for D7 and D8.

Table 2-2 provides a summary of the simulated peak and RMS current stresses in the switches and diodes of the converter. The stress analysis results are within the operating range of components selected, so these components were used for the experimental prototype testing.

Table 2-2 Summary of current and voltage stress in active components

	M1-M6	D1-D6	M7	D7	M8	D8
Current Stress [A]	22	12.7	18	0	18	0
RMS Current [A]	7.6	4.3	9.0	0	9.0	0
Voltage Stress [V]	800	800	800	800	800	800

A summary of the converter powertrain components selected are provided in Table 2-3.

Table 2-3 Components selected for 5 kW universal AC input prototype

Component	Part Name	Value	Quantity
Boost inductors (La, Lb, Lc)	Custom (Appendix D)	500 µH / 20 A	3
Buck inductor (Lf)	Custom (Appendix D)	500 µH / 20 A	1
Boost capacitor (C1)	450KXW150MEFC18X45	1350 µF	2 x150 µF (series) x 18 (parallel)
Buck capacitor (C2)	LGG2W331MELB35	165 µF	2 x 330 µF (series)
M1-M6, D1-D6 (6-pack module)	CCS020M12CM2	MOSFET6CH 29.5 A /1200 V	1
Buck switches (M7, M8)	C2M0025120D	MOSFET 1200 V / 90 A	2
Diodes D7, D8	C4D20120D	1200 V / 16 A	2

2.4 Simulation results

In order to validate the analytical results from previous sections and the converter PFC operation, simulation waveforms of the three phase voltages and currents are shown in Figure 2-4 for 208 V input. These waveforms are sinusoidal and the current waveforms are in phase, indicating PFC operation of the converter. Additional detailed waveforms are shown in Figure 2-5 and Figure 2-6, illustrating the voltage of phase a along with corresponding current for low-line, i.e. 208 V, and high-line, i.e. 480 V, respectively. The power factor was calculated using PSIM for each input voltage at 0.9992 for low-line and 0.9890 for high-line.

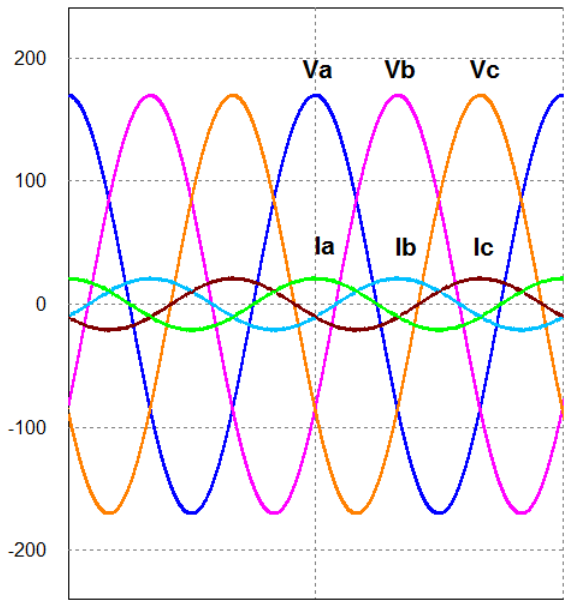

Figure 2-4 Phase voltages and currents at 208 V AC input

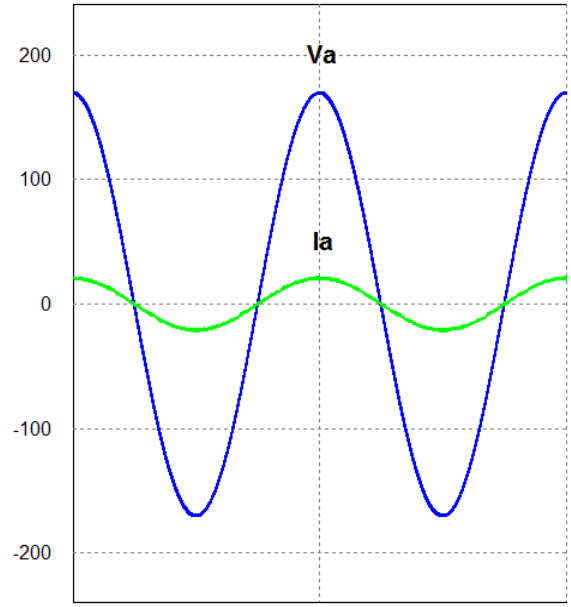

Figure 2-5 Phase a voltage (Va) and current (Ia) at a low-line AC input of 208 V

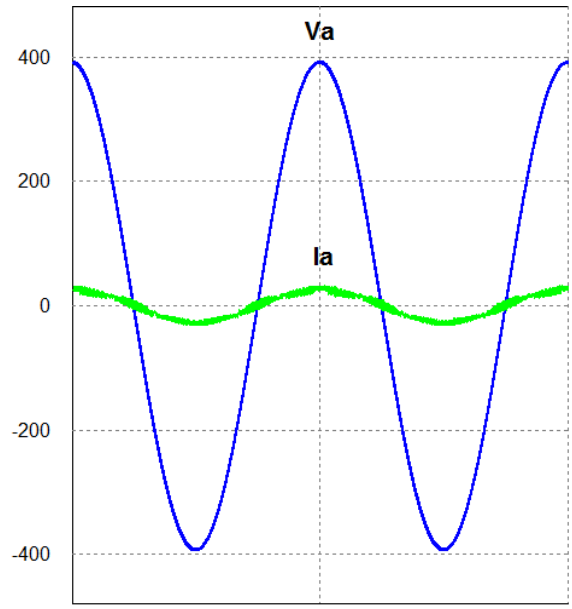

Figure 2-6 Phase a voltage (Va) and current (Ia) at a high-line AC input of 480 V

2.5 Loss estimation

In order to estimate the expected efficiency, total loss and loss distribution among different components, a worst case analysis was performed. Active losses (i.e. MOSFET and diode conduction and switching losses) and passive losses (i.e. losses in the inductors and capacitors) were calculated using component datasheet information. A summary of the component loss parameters is provided in

Table 2-4. PSIM and Mathcad were used to calculate the operating condition values, e.g. rms currents.

Table 2-4 Loss Calculation Parameter Values

Parameter [unit]		Boost Stage	Buck Stage
R_{DS} [mΩ]		200 (CCS020M12CM2)	43 (C2M0025120D)
R_D [mΩ]		120	107
V_f [V]		0.75	0.766
R_{Gext} [Ω]		Turn-on=10 Turn-off=5	Turn on=10 Turn off=5
T_j [°C]		125	125
R_{DC} [Ω]		0.078	0.078
R_{ac} [Ω]		0.148	0.148
ESR [Ω]		0.1	0.29
Core Material KoolMu77617	α $[{}^{mW}/_{Cm^3}]$	193	193
	β	2.01	2.01
	ɣ	1.29	1.29

2.5.1 **Active losses**

For the converter, the conduction loss in each switch, P_{cond_sw}, can be calculated using (2-11), and the conduction loss in each diode, P_{cond_D}, can be calculated using (2-12), where R_{DS} is the drain-source resistance, R_D is the diode dynamic resistance, V_f is the diode forward voltage drop, I_{rms} is the rms switch current, I_{D_rms} is the rms diode current and I_{D_DC} is the average diode current.

$$P_{cond\_sw} = {I_{rms}}^2 R_{DS} \quad \textbf{2-11}$$

$$P_{cond\_D} = {I_{D\_rms}}^2 R_D + V_f I_{D\_DC} \quad \textbf{2-14}$$

The calculations were completed using the datasheet information provided in

Table 2-4, at a junction temperature T_j of 125°C. Switching turn-on/off energy information for SiC MOSFETs can be obtained from data sheets [24]. The switching energy, E is a function of switch current, I_{DS}, drain to source voltage, V_{DS}, gate resistance, R_{Gext} and temperature, T_j. Assuming V_{DS} is known, and T_j is constant for a given operating point and cooling is in a steady-state condition**,** the switching energy curves from the datasheets can be used to provide values of switching energy at various operating currents. The rescaled data points of switching energies from datasheet curves can be described by a second order polynomial using curve-fitting techniques to derive coefficients. k_0 , k_1 and k_2.The switching energy,$E_i(I_{DS})$, in each switching cycle is given by (2-15), where i denotes the switching cycle number in a mains period, and T_{Sw} is the switching period.

$$E_i(I_{DS}) = k_0 + k_1 I_{DS}(iT_{sw}) + k_2 {I^2}_{DS}(iT_{sw}) \quad \textbf{2-12}$$

For an accurate prediction of switching losses, the total switching loss energy in an AC line period can be calculated for each switching cycle using curves of turn-on switching energy, $E_{ion}(I_{DS})$, and turn-off switching energy, $E_{ioff}(I_{DS})$. This data is summed to give the total energy loss, and then averaged over an AC line period, T, to give the switching power loss in each switch as given by (2-13). The switch current waveform is determined using PSIM simulation.

$$P_{sw} = \frac{1}{T} \sum_{i=0}^{\frac{T}{T_{sw}}-1} E_{ion}(I_{DS}(iT_{sw})) + E_{ioff}(I_{DS}(iT_{sw})) \quad \textbf{2-13}$$

The total active losses are then calculated by summing the active device loss components. Reverse recovery current is negligible for SiC devices. Therefore, reverse recovery losses are neglected.

2.5.2 **Passive losses**

The passive losses of the converter consist of losses in the inductors and capacitors. The next two subsections focus on these components.

2.5.2.1 **Inductor losses**

The core loss density, p_L, as a function of flux amplitude and frequency [25] is given by (2-14), where α, β and γ are constants typically provided in magnetic core material datasheets.

$$p_L = \alpha {B_{pk}}^{\beta} {f_{sw}}^{\gamma} \qquad \textbf{2-14}$$

Flux density, B, is a non-linear function of magnetizing field, i.e. $B = B(H)$. Curve fitting equations are often available in the datasheets as well. For the buck stage, B_{pk} is constant and can be used for core loss calculations. However, for the boost inductors, B_{pk} varies with the line cycle. Therefore, to achieve an accurate core loss calculation, B_{pk} can be calculated each switching cycle, then the results of the instantaneous core loss densities should be averaged over an AC line period to give the effective core loss density. The density multiplied by the core volume, V_c, gives the total effective core loss, P_{L_eff}. The upper and lower envelopes of the boost inductor current data, as illustrated in Figure 2-7, should be used to calculate B_{pk} each switching cycle, and then (2-15) is used to calculate the total inductor core loss, P_{L_eff}.

$$P_{L\_eff} = V_c \frac{1}{i} \sum_{i=0}^{\frac{T}{Tsw}-1} \alpha \left| {B_{pk}}^{\beta} i T_{sw} \right| {f_{sw}}^{\gamma} \qquad \textbf{2-15}$$

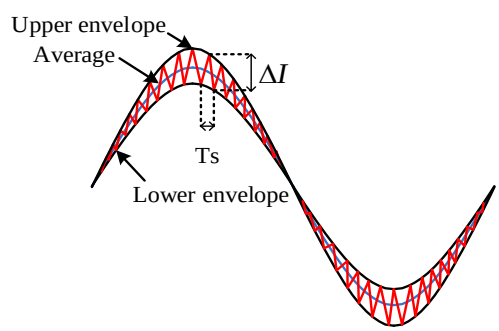

Figure 2-7 Boost inductor current waveform

The current waveform in Figure 2-7 consists of high frequency (i.e. switching and harmonics), I_{high_freq}, and low frequency (i.e. ac line), I_{low_freq}, components. At high frequencies,

the skin effect (i.e. the ac resistance) needs to be included in the loss analysis [31]. Fast Fourier Transform (FFT) data from simulation is used to calculate the high and low frequency current components. The inductor conduction loss, P_{L_cond}, is given by (2-16).

$$P_{L\_cond} = I^2{}_{low\_freq} R_{DC} + I^2{}_{high\_freq} R_{ac} \quad \textbf{2-16}$$

2.5.2.2 **Capacitor loss**

The loss in the DC bus capacitors can be calculated using (2-17) with the equivalent series resistance (ESR), obtained from the capacitance datasheet, and the rms capacitor current obtained via PSIM simulation.

$$P_{cap} = I_{rms}{}^2 ESR \quad \textbf{2-17}$$

Using the specifications of Table 2-1, parameter values of

Table 2-4, PSIM simulations and Mathcad analysis, the losses are calculated.

2.5.3 **Loss estimation discussion**

Combining all loss values, the total estimated losses of the two-stage PFC were calculated at 208 V, 400 V and 480 V AC line input voltages. The results are summarized in Figure 2-8. The details of calculations can be found in Appendix B for 5 kW of output load. The loss may be calculated at other partial load power conditions using a spreadsheet if desired.

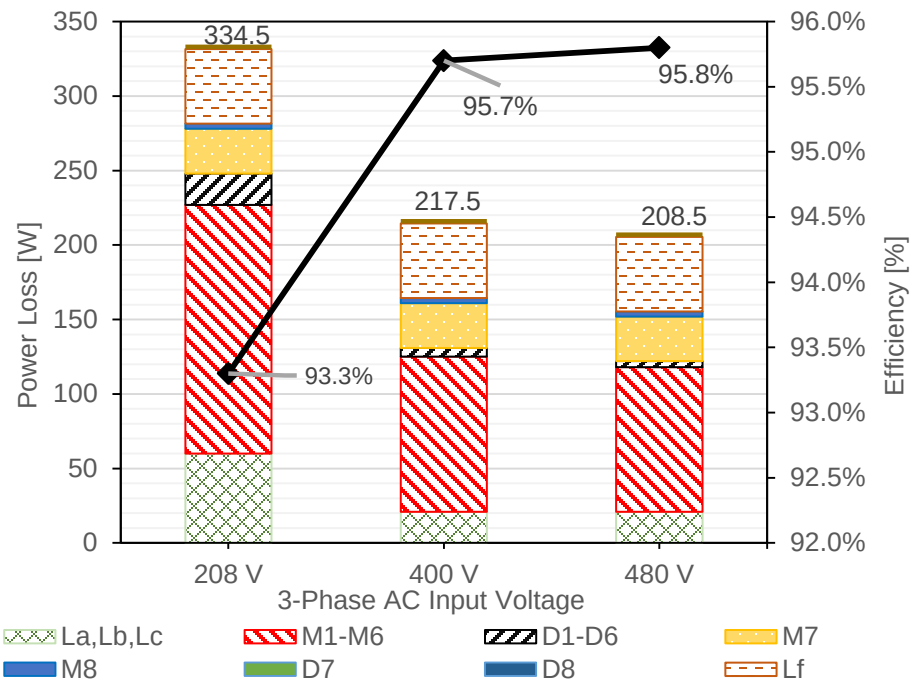

Figure 2-8 Break down of losses for two-stage three-phase AC/DC buck follows boost PFC at AC input voltages of 208 V, 400 V and 480 V at 5 kW full-load

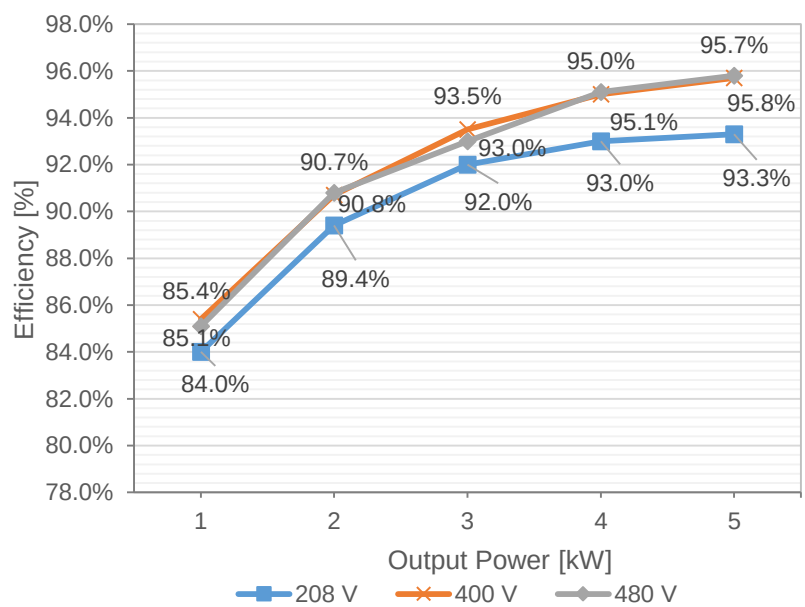

Figure 2-9 Calculated efficiency as a function of load power for the three-phase AC/DC buck follows boost PFC at AC input voltages of 208 V, 400 V and 480 V

2.6 Experimental results

A prototype of the universal three-phase AC input cascaded boost and buck PFC system was built using the 1200 V SiC semiconductors and additional specifications and parameter values listed in Table 2-3. The purpose was to validate PFC operation of the converter at conventional

fixed 800 V intermediate bus, illustrated in Figure 2-1. Balanced operating conditions were tested since unbalanced conditions are typically limited to only 2-3% [23]. For highly unbalanced input mains conditions, there are alternate control techniques that can be used [7]. A signal sampling/conditioning and control board, Figure 2-10, was designed and built using a TMS320f28335 DSP to implement the control strategy, illustrated previously in Figure 2-2. The design documents are included in Appendix A . A six channel Cree CGD15FB45P gate driver board was used for the boost PFC switches and a Cree CRD8FF1217P driver board was used for the buck switches. A photo of the prototype is provided in Figure 2-11.

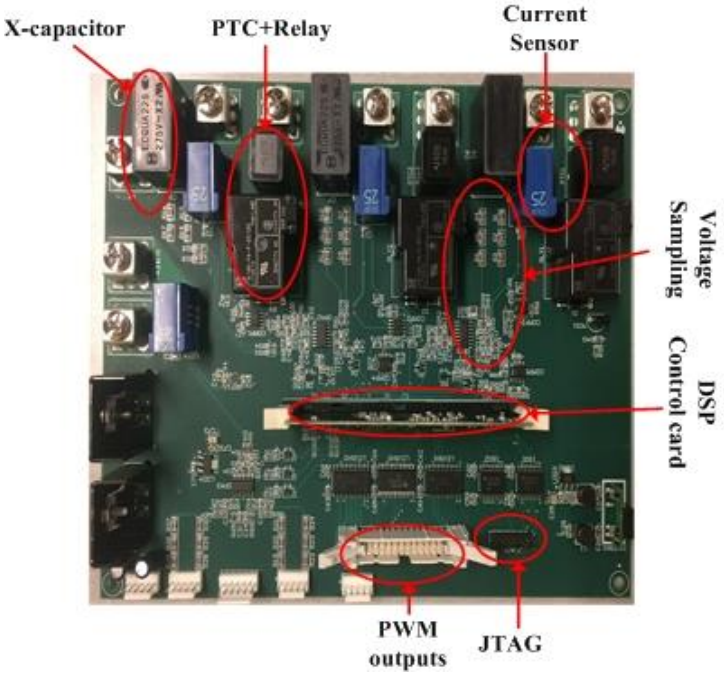

Figure 2-10 Signal sampling/conditioning and DSP board developed

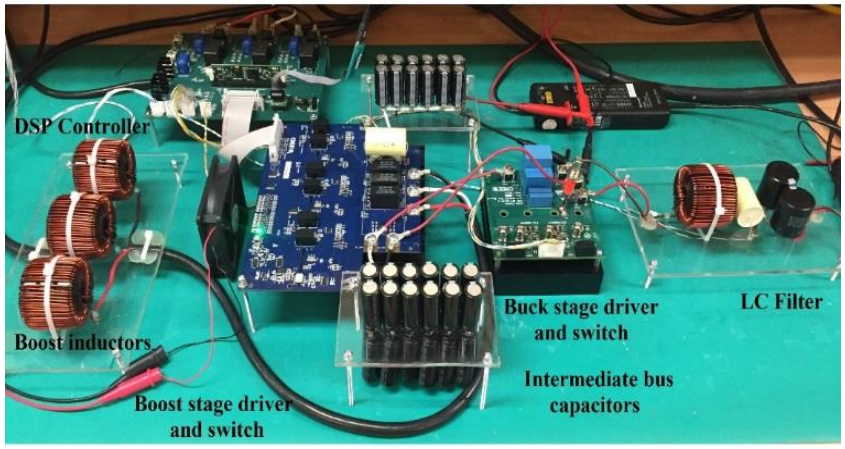

Figure 2-11 Photo of the 5 kW SiC-based digitally controlled three-phase cascaded boost-buck PFC prototype

In Figure 2-12, a scope capture of phase voltages and input currents is also provided to show converter operation for the highest stress condition, which is the low-line input of 208 V AC. Figure 2-13 provides the efficiency as a function of output power for AC mains voltages of 208 V, 400 V and 480 V. The power factor as a function of output power for the above three AC mains voltages is provided in Figure 2-14.

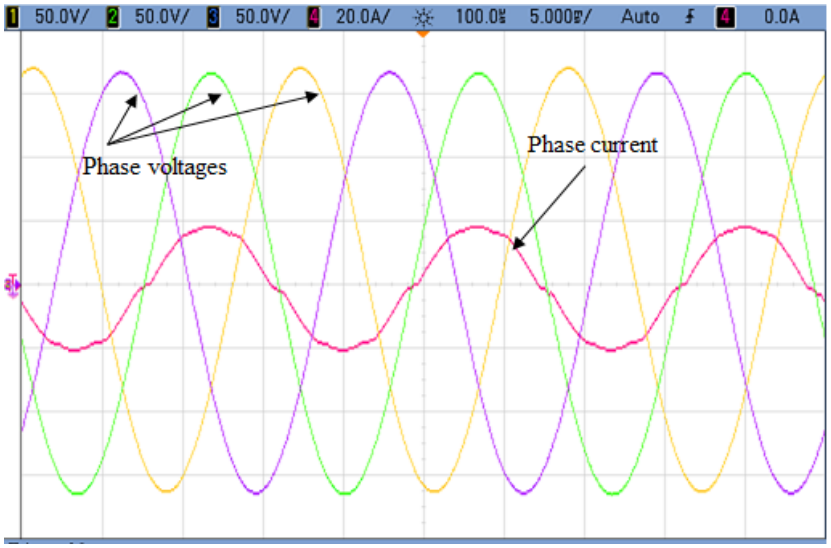

Figure 2-12 Input AC voltages and phase current for low-line 208 V AC input

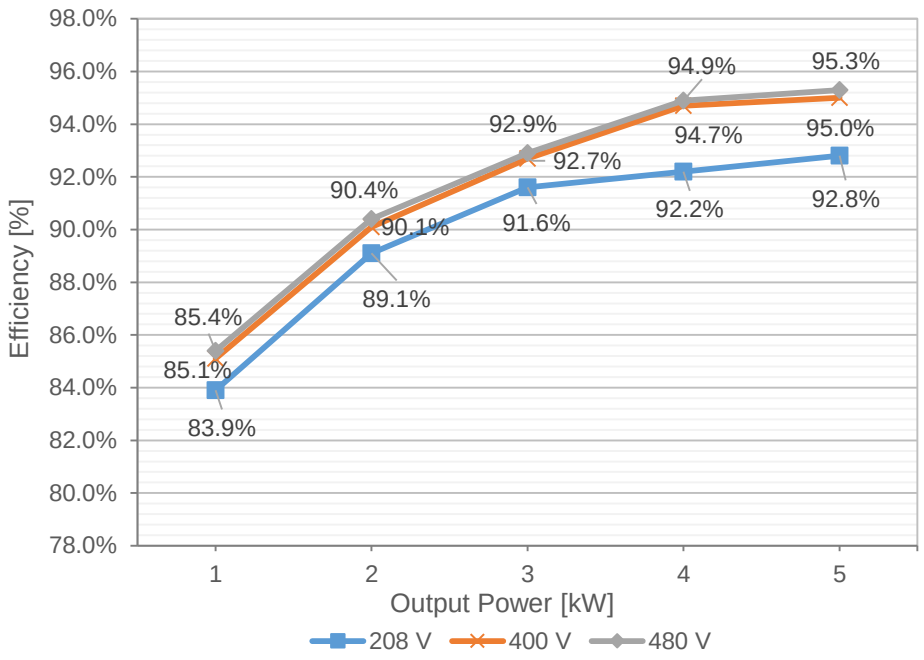

Figure 2-13 Efficiency curves vs. output power at three-phase AC input voltages of 208 V, 400 V and 480 V

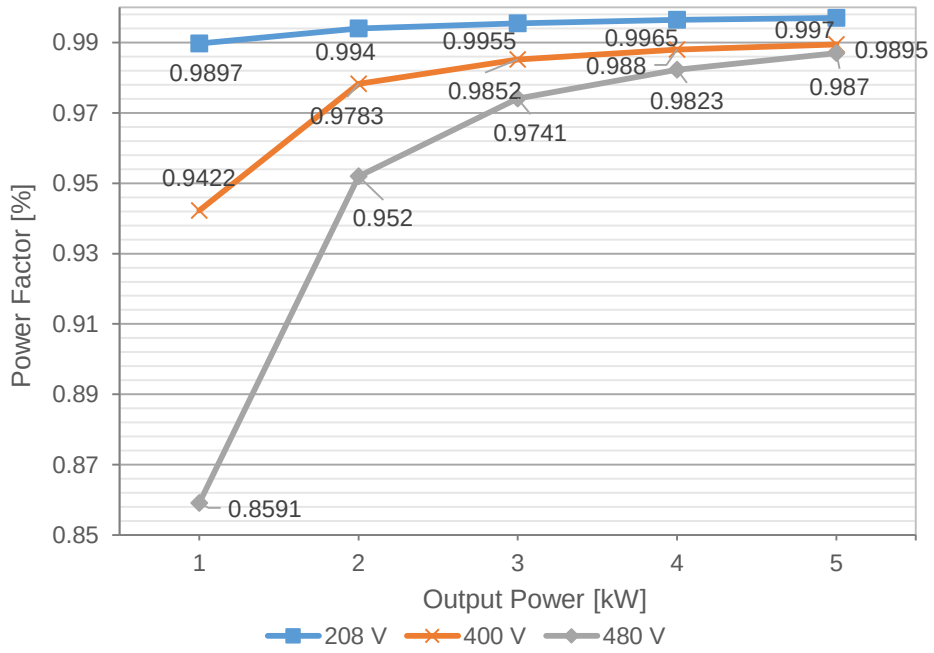

Figure 2-14 Power factor vs. output power at three-phase AC input voltages of 208 V, 400 V and 480 V

2.7 Summary

In this chapter, a universal input three-phase buck-follows-boost 208-480 V AC input PFC converter with 400 V DC output was designed, built and tested. This solution, as discussed in Chapter 1: has advantages over other existing solutions. Therefore, it was chosen as the benchmark. In order to reduce cost and also increase efficiency at low-line for better thermal management as compared to the benchmark, a single-stage SEPIC derived topology is proposed, analyzed and built and presented in Chapter 3: .

Chapter 3: **Three-phase third harmonic injection SEPIC AC/DC front-end PFC**

The boost and buck circuit topologies for three-phase third harmonic injection PFC were discussed in sections 1.3.1.3 and 1.3.2.2 respectively. For universal input operation, a second stage must be added to these converters to step up/down the output of the first stage to 400 V DC output.

In this chapter, a novel three-phase third harmonic injection PFC derived from SEPIC DC/DC converter is proposed. The topology can serve as an alternate single-stage solution for a universal input PFC with 400 V DC output.

3.1 **Single-ended primary inductance converter (SEPIC)**

The DC/DC SEPIC converter, illustrated in Figure 3-1, can step up, or down the input voltage without changing the output polarity [39]. Assuming ideal components and $0 < D < 1$ as duty cycle for a switching period, the relationship between input and output is:

$$V_O = \left(\frac{D}{1-D}\right) V_s \qquad \textbf{3-1}$$

Where V_O is the output voltage and V_s is the input voltage.

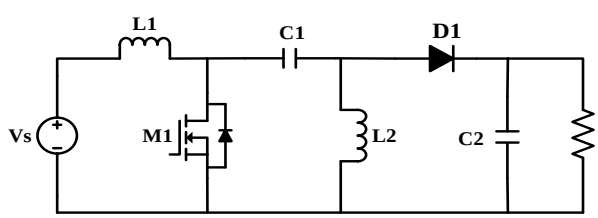

Figure 3-1 Single-ended primary inductance converter (SEPIC)

3.2 **Proposed three-phase third harmonic injection SEPIC AC/DC front-end PFC**

The proposed single stage (i.e. no intermediate DC bus) three-phase third harmonic injection topology is provided in Figure 3-2. Variant third harmonic injection topologies have been proposed in [16]-[18]. However, these topologies are all either only step-down buck or only step-up boost circuits. The proposed topology allows buck-boost operation and can operate over the full universal AC input voltage range, while providing a 400 V DC output voltage, so it is a novel candidate topology replacement for the two-stage universal input cascaded boost plus buck

converter architecture, presented in Chapter 2, Figure 2-1. Moreover, analog control techniques can be used to control this converter, making the control as simple as most DC-DC converters.

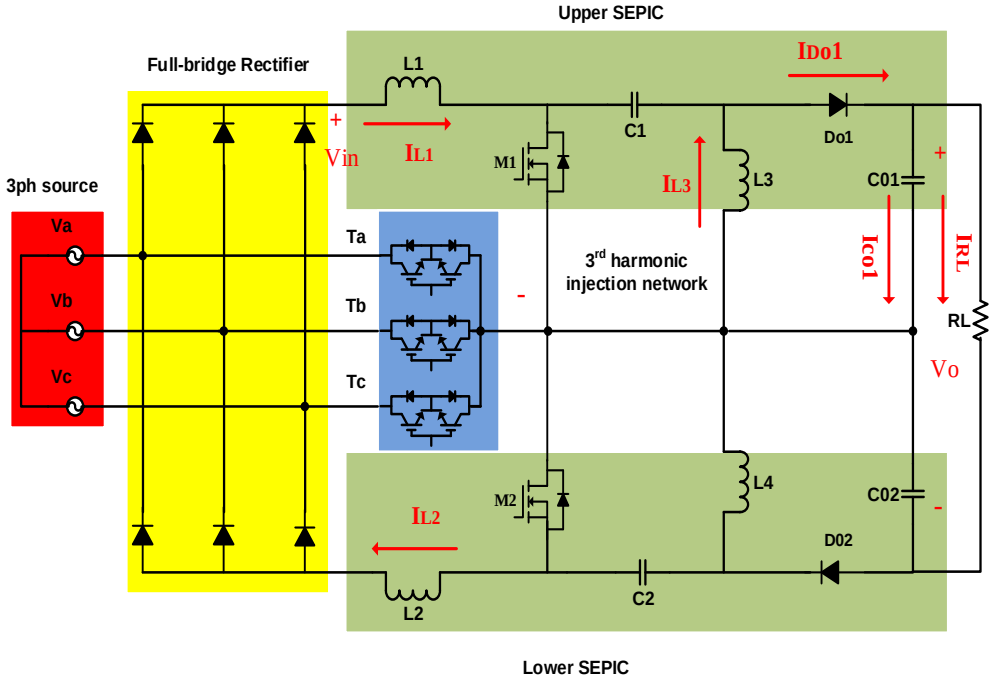

Figure 3-2 Proposed 3rd harmonic injection SEPIC derived AC/DC PFC

3.3 Principles of operation

One there-phase AC line cycle is shown in Figure 3-3, with the cycle divided into six zones of 60 degrees each. Table 3-1 summarizes the 3rd harmonic injection network switch states for the six zones of operation. In zones one through six, the amplitude of one phase lies in between the other two, accordingly it is the middle phase. Therefore, in the three-phase full-bridge diode rectifier in Figure 3-2, the voltage on the upper positive rail will be the phase with the highest magnitude and the voltage on lower negative rail will be the phase with the lowest magnitude. Using this property, and by controlling the currents in inductors L1 and L2 to be proportional to and in phase with the highest and lowest amplitude phase voltages in the respective zone, coupled with selection of the middle phase for the third harmonic injection network, the current in the third phase, which is the sum of the other two currents, will be proportional and in phase with the third phase and PFC is achieved. Therefore, the bi-directional switches in the third harmonic injection network are used to select the appropriate phase in each of the six zones of operation to synthesize the current for the third phase.

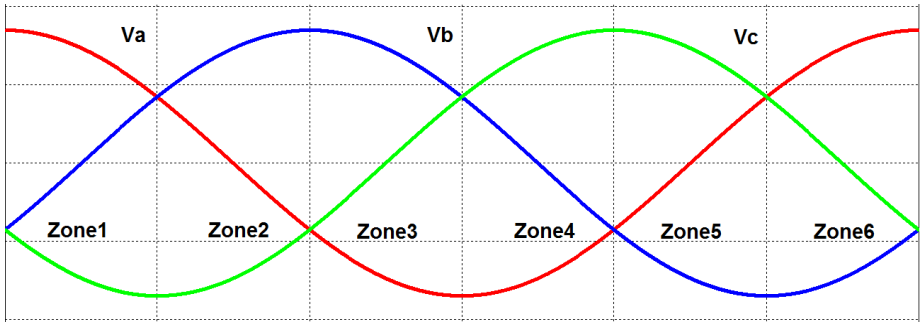

Figure 3-3 Six operation zones of operation in a three-phase AC input cycle

Table 3-1 Switch states of third harmonic injection network

	Zone1 0-60°	Zone2 60°-120°	Zone3 120°-180°	Zone4 180°-240°	Zone5 240°-300°	Zone6 300°-360°
Ta	0	1	0	0	1	0
Tb	1	0	0	1	0	0
Tc	0	0	1	0	0	1

3.4 **Converter design**

To benchmark this converter against the conventional three-phase six-switch boost plus buck approach discussed in chapter 2, the specifications in Table 2-1 are used to size the active and passive components. The derivation of the analytical equations used in the sub-sections that follow can be found in Appendix C.

3.4.1 **Calculation of series inductors L1 and L2**

Assuming the duty cycle of switches M1 and M2 is $0 < D < 1$, f_s the switching frequency, V_m the phase voltage peak value, ΔI_{max} the inductor maximum ripple, it can be shown that the minimum required inductance value for L1 and L2 is L_{min} as follows:

$$L_{min} = 1.5\frac{V_m D_{Vm}}{f_s \Delta I_{max}} \qquad \textbf{3-2}$$

In (3-2), the duty cycle at peak input voltage, D_{Vm}, is as follows, where V_0 is the converter output voltage as in Figure 3-2:

$$D_{Vm} = \frac{V_0}{V_o + 3V_m} \qquad \textbf{3-3}$$

Substituting (3-3) into (3-2), it is evident that L_{min} is higher at high AC line input. Using the data from simulation and assuming $\Delta I_{\max\_highline} = 0.7 I_{\max\_highline} = 0.7(8.5) = 6\ A,\ L_{min} = 500\ \mu\text{H}$. With this value of inductor, the maximum ripple current at low-line $\Delta I_{\max\_lowline} = 4.5\ A$.

3.4.2 Calculation of series capacitors C1 and C2

The series capacitor C1 and C2 are sized based on the value of ripple. Assuming steady-state condition and the fact that the maximum ripple in series capacitor will be at maximum input current. It can be shown that:

$$C_{1,2min} = \frac{I_m(1 - D_{Vm})}{f_s \Delta V_{Cmax}} \qquad \textbf{3-4}$$

Where ΔV_{cmax} is the amount of ripple, and the maximum input current I_m is:

$$I_m = \frac{2}{3}\frac{P_{in}}{V_m} \qquad \textbf{3-5}$$

Assuming $\Delta V_{Cmax} = 0.4 V_m = 68\ \text{V},\ C_1, C_2 = 3.3\ \mu\text{F}$.

3.4.3 Calculation of inductors L3 and L4

The inductors L3 and L4 are energized by capacitors C1 and C2 respectively during the switch on-time D. In the steady-state, the momentarily DC voltage across the series capacitor equals the input voltage therefore, the inductors can be sized using equations (3-2), (3-3). Assuming the same ripple and input voltage condition as section 3.4.1, L3 and L4 are chosen as 500 μH.

3.4.4 Output capacitors Co1 and Co2

The DC current through the capacitors C1 and C2 is zero, therefore the DC value of current in inductor L3, $I_{L3} = I_{Do1}$, where I_{Do1} is the DC current in diode. Ideally, the momentarily DC input power,$P_{in} = V_{in} I_{L1}$, equals DC output power, $P_o = \frac{V_o}{2} I_{L3}$ therefore:

$$I_{L3} = 2\frac{V_{in} I_{L1}}{V_o} \qquad \textbf{3-6}$$

The maximum current in inductor L3, I_{L3m} can be shown to be:

$$I_{L3m} = 3\frac{V_m I_{L1m}}{V_o} \qquad \textbf{3-7}$$

Using a triangular approximation for I_{L3} with the peak value as in (3-7), the output diode current contains switching frequency, a low frequency component at three times the mains frequency and a DC component. The DC component provides output current and the rest of harmonic content needs to be filtered by output capacitor $Co1$. It is shown in Appendix C that the minimum output capacitor for an assumed amount of voltage ripple ΔV equals:

$$C_{o1} = \frac{4}{3\pi^3}\frac{I_{l3m}}{\Delta V f_m} \qquad \textbf{3-8}$$

Where f_m is the mains frequency. Assuming $\Delta V = 0.1V_o = 40\ V$, C_{o1}=2700 μF.

The ripple voltage on upper and lower SEPIC are 180° out of phase, therefore they cancel each other providing a good DC output voltage.

3.5 **Control**

In Figure 3-4, the control block diagram for the proposed topology is shown. The PLL block determines the phase angle. The bidirectional switches Ta, Tb, Tc are selected using this angle and the look-up table shown. For better controllability, DQ control is used to convert the ac voltage and current quantities into DC. For PFC operation, quadrature component of current iq is set to zero. The direct component of current Id is controlled by the outer voltage loop. Using the inverse DQ/ABC transform the current command signals Id^* and Iq^* are converted into Ia^*, Ib^* and Ic^* and applied to PWM block to generate appropriate pulse width modulation. The pulse width generated by the PWM block is proportional to current command to increase, or decrease the current in the upper and lower inductors as needed to keep those currents proportional and in phase to the respective voltages. The output of the PWM block is multiplexed using the look up table as in control diagram to send the respective PWM control to switches M1 and M2.

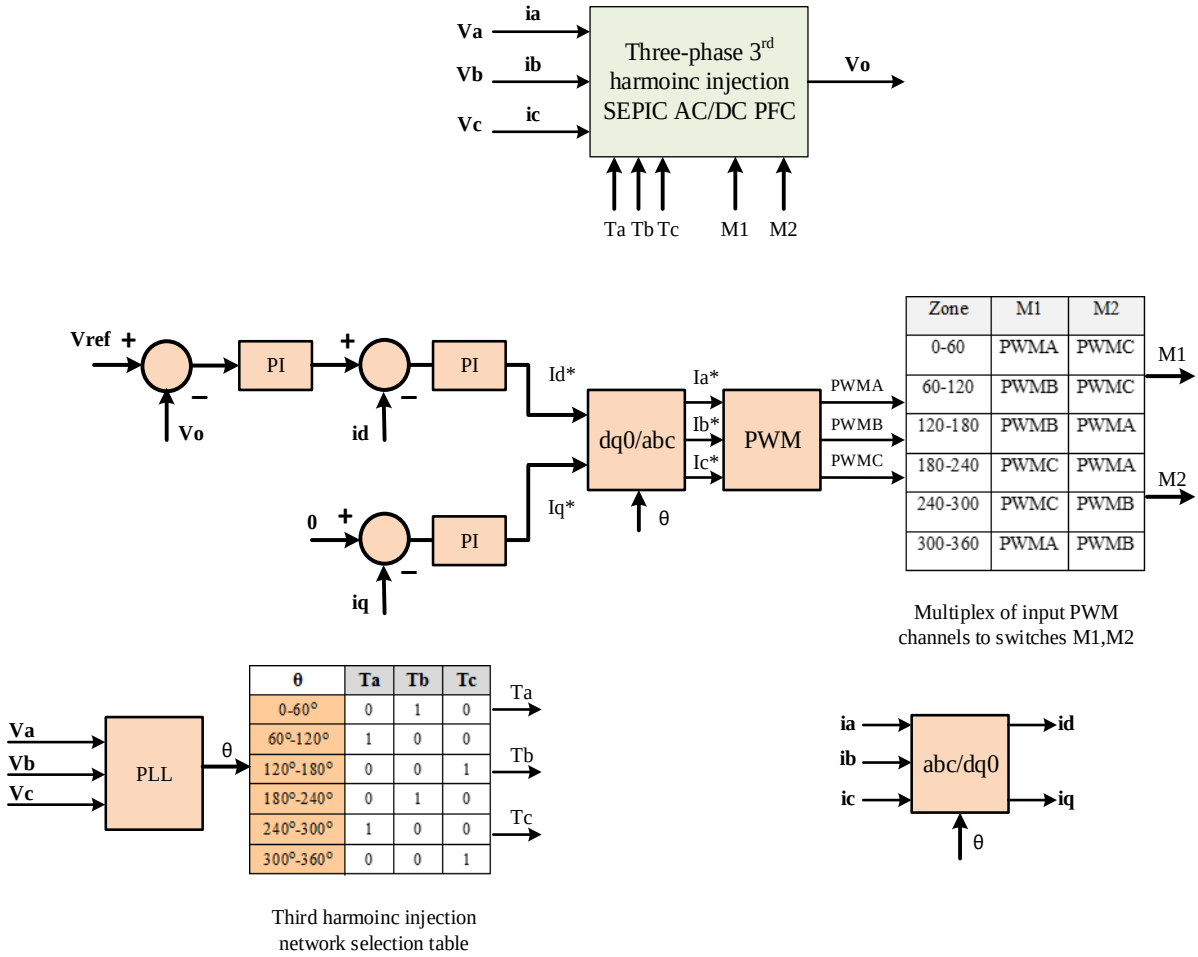

Figure 3-4 Control block diagram employing DQ control and look-up tables for buck-boost PFC operation

3.6 **Simulation results**

The components sized in section 3.4 are used to simulate the circuit of Figure 3-2. The results of simulation are compared to analytical calculations in previous section to further prove the accuracy of derived equations.

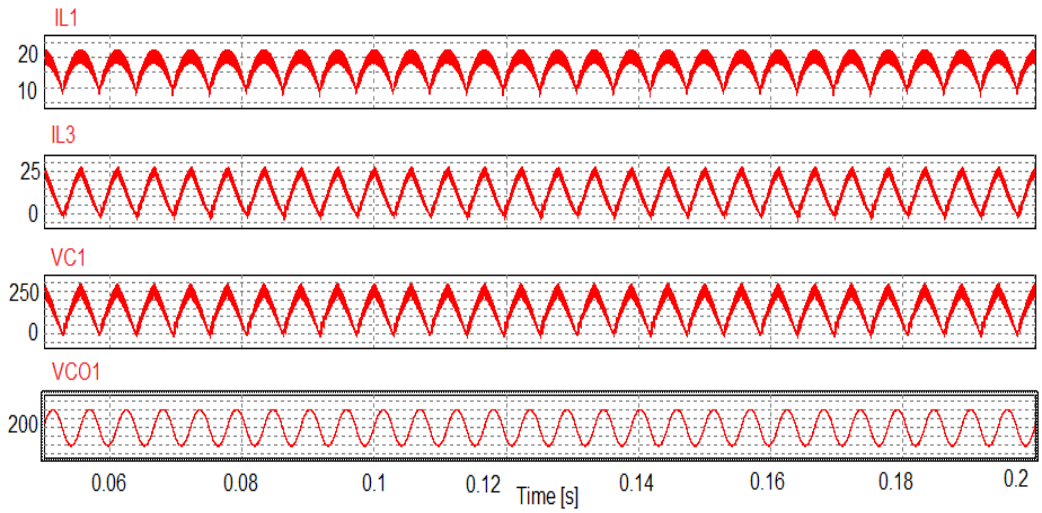

Figure 3-5 Simulation results showing current in inductors L1, L3 and voltages of capacitors C1, CO1

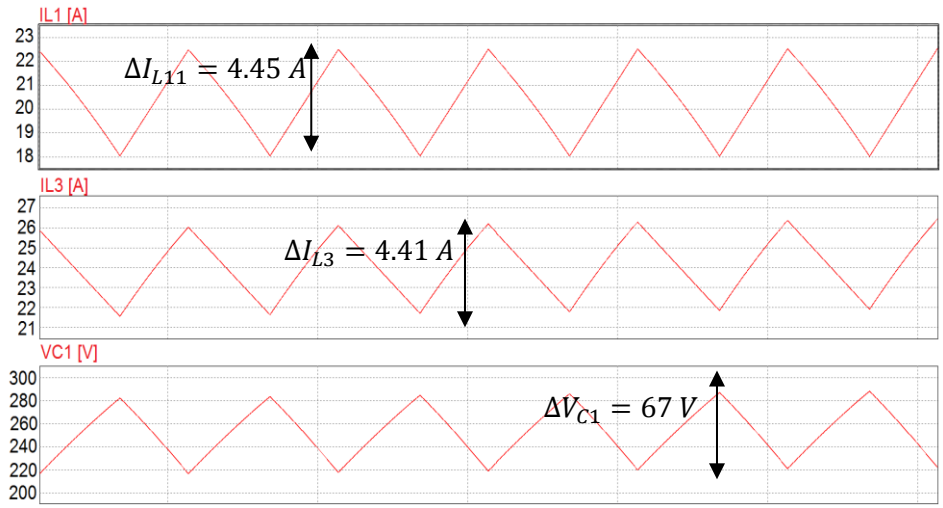

Figure 3-6 Simulation of currents in inductors L1, L3 and voltages of capacitor C1 zoomed at peak value in Figure 3-5

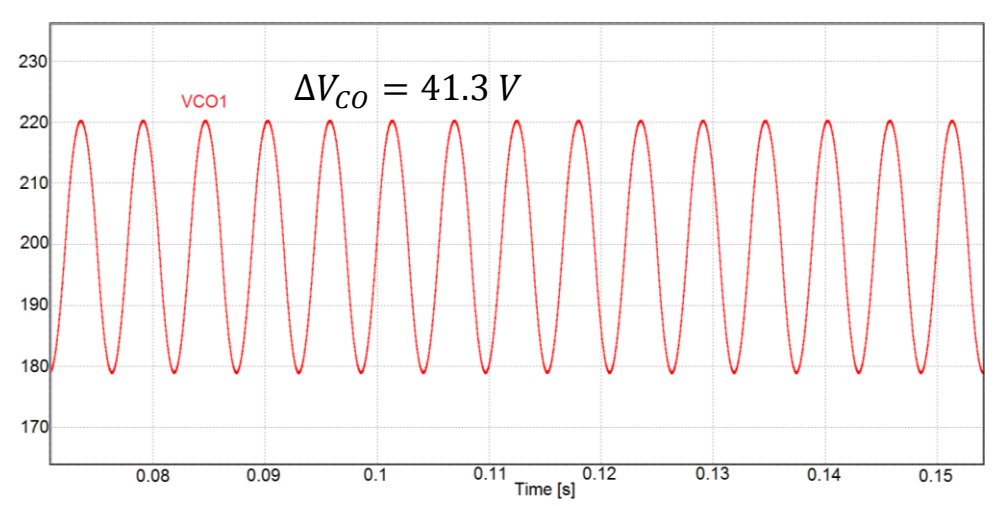

Figure 3-7 Output voltage ripple at three times the mains frequency on upper SEPIC

Figure 3-5 shows the simulation results at low-line 208 V for inductors currents $L1$, $L3$ and capacitor voltages $C1$, $Co1$. These results are zoomed at peak in Figure 3-6 and Figure 3-7. The analytical assumptions and simulation results match well which confirms the validity of derived equations.

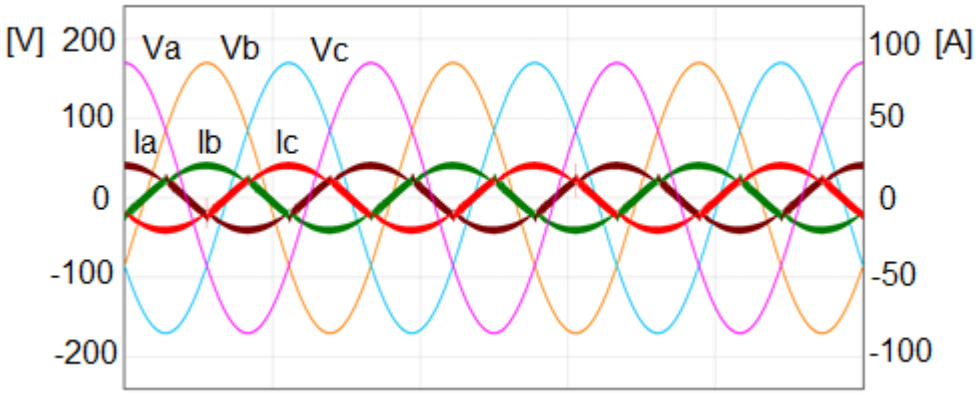

Figure 3-8 Current and voltages of all three-phases at low-line 208 V

Figure 3-8 illustrates the voltages and currents of all three-phases at low-line. The simulation demonstrates a PF of 0.9976 at low-line (208 V) and a PF of 0.9911 at high-line (480 V). In Figure 3-11, the output voltages of the upper and lower SEPIC converters along with load voltage are shown. The phase voltage ripples are 180° out of phase and therefore they cancel each other providing a ripple free DC output to the load.

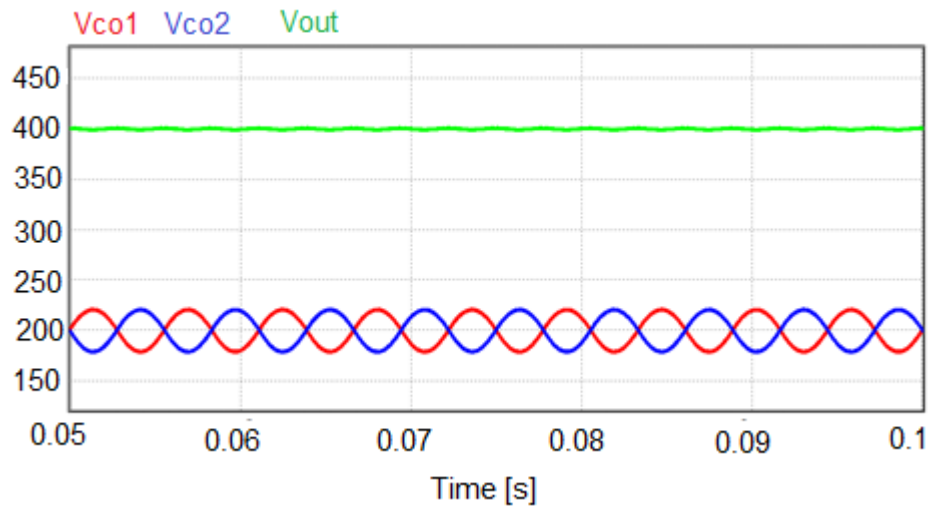

Figure 3-9 Output voltage ripples of upper SEPIC and lower SEPIC cancel providing a ripple-free load voltage

3.7 Selection of components

The results of simulation for current and voltage stress along with rms current through key power components are summarized in Table 3-2 with the stresses highlighted in bold.

Table 3-2 Summary of current and voltage stress along with rms current through the components

	Low-line 208 V			High-line 480 V		
	Irms [A]	Imax [A]	Vmax [V]	Irms [A]	Imax [A]	Vmax [V]
L1, L2	**16.9**	**22.6**	255	7.3	12	**588**
L3, L4	14.8	27.1	292	**15.0**	**30.0**	**614**
C1, C2	**15.3**	**27.0**	292	10.2	12.0	**614**
Co1, Co2	**17.2**	**37.0**	220	13.1	29.5	**220**
M1, M2	**22.8**	**49.6**	494	12.5	42	**814**
Do1, Do2	**21.3**	**49.6**	494	18.1	42	**814**
Ta, Tb, Tc Per switch	**2.8**	**15.6**	255	1.7	2.8	**588**
D1-D6	**9.8**	**22.6**	294	4.2	12.0	**679**

The voltage and current stresses (bold) along with values calculated in sections 3.4.1-3.4.4 are used to choose the appropriate components for the converter as shown in Table 3-3. The minimum required capacitance for C1, C2 was sized to be 3.3 μF. However, to withstand the current stress of 15.3 A, two parallel bank with two TDK B32794D8755 7.5 μF film capacitors in series in each bank, is chosen. The bidirectional switches in third harmonic injection network, Ta,

Tb and Tc are switching at low frequency of 60 Hz, therefore IGBT's are used for their lower cost. Sic MOSFETs from CREE are used for high- frequency switches of M1 and M2. The full-bridge diode and output diodes are also sized according to the respective stresses.

Table 3-3 Summary of selection of components for the 5 kW 3rd harmonic injection SEPIC PFC

Component	Value	Quantity	Part No.
L1, L2	500 μH	2	3stacked kooLMu77191 Cores/66turns/AWG14
L3, L4	500 μH	2	3stacked kooLMu77191 Cores/66turns/AWG14
C1, C2	7.5 μF	2x7.5 μF (series)x 2(parallel)	B32794D8755
Co1, Co2	2700 μF	18x150 μF/450 V (parallel)	450BXW150MEFC18X45
M1, M2	25 mΩ/1200 V	2	C2M0025120D
Do1, Do2	20 A/1200 V	2	C4D20120D
Ta, Tb, Tc	25 A/1200 V	6	IKW25N120T2
D1-D6	3-phase full-bridge diode	1	VS-26MT120

3.8 Loss estimation and cost analysis

A loss and cost analysis is made in the following sections to show the benefits we can get from the proposed topology against the conventional solution of boost follows buck.

3.8.1 Loss estimation

Figure 3-10 provides the calculated losses for proposed 3rd harmonic injection SEPIC and the boost follows buck benchmark. The data from simulation along with Mathcad software are used for loss estimation. The method for loss analysis is already discussed in section 2.5. At low-line, the proposed topology shows lower losses compared to the benchmark, specifically 307 W loss compared to 334.5 W – a 27.5 W, or 8.2 % reduction. Thermal design of the converter is based on the low-line losses where losses are the highest. Therefore, the thermal design cost for this

topology would be lower. Finally, if one parallel switches were added for M1and M2 and parallel diodes for Do1 and Do2 were added, the efficiency could be further improved reducing the low line (208 V) losses to 246 W, therefore improving the high-line (480 V) losses to be close to the benchmark.

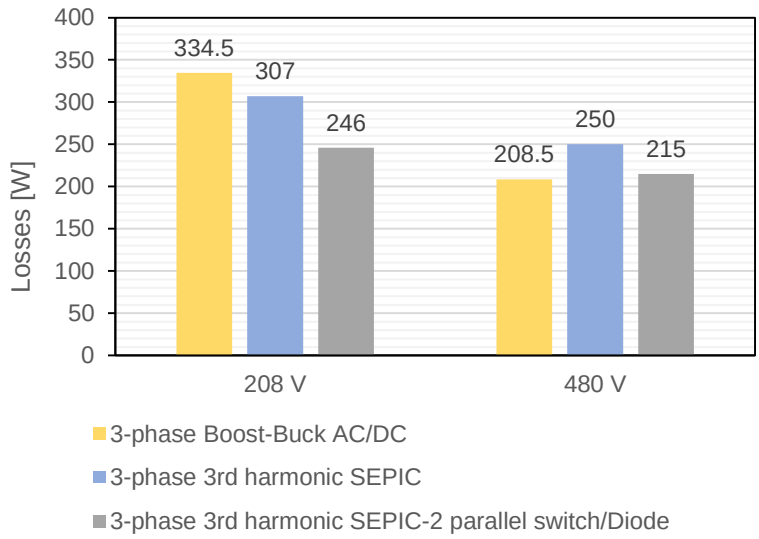

Figure 3-10 Total loss comparison for conventional buck follows boost and proposed topology at different input mains at 5 kW

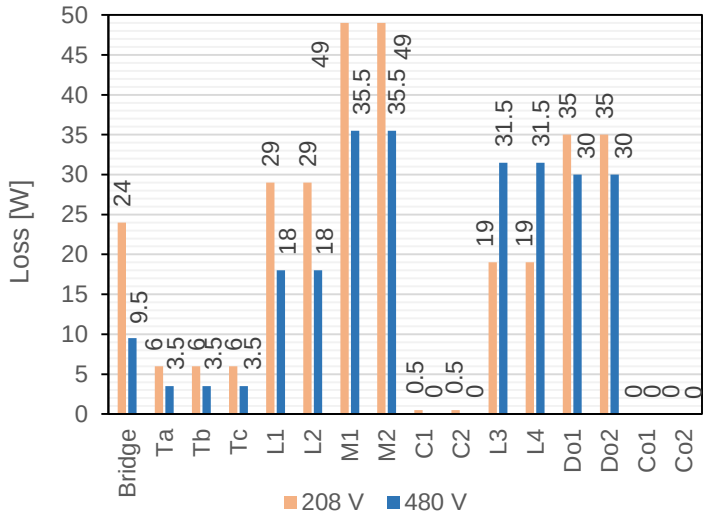

Figure 3-11 Break down of loss estimation for the proposed three-phase 3rd harmonic injection SEPIC AC/DC PFC

The breakdown of losses in Figure 3-11 shows distribution of losses among different components at 5 kW. It contains good information that can help for proper selection of semiconductor packages and overall thermal design.

3.8.2 **Cost analysis**

A cost analysis of the power components for the conventional boost follows buck benchmark and the proposed topology was completed using prices from Digi-Key in 2019 [59] and is summarized in Table 3-4 and

Table 3-5, respectively. The analysis shows that the cost of the power components for the proposed topology are less than the benchmark by $136 or 22%. In addition, based on analysis in section 3.8.1, since the losses at low-line for the proposed topology are lower, the cost of thermal design would be less than the benchmark.

Table 3-4 Bill of material cost for power components in conventional solution of boost follows buck

Component	Value	Part NO.	Quantity	Unit price USD$	Total USD $
La, Lb, Lc	500 μH / 20 A	3stack/kooLMu77191Cores/ 66turns/ AWG14	3	50	150
Lf	500 μH / 20 A	3stacked/kooLMu77191 Cores/66turns/AWG14	1	50	50
C1	1350 μF	450BXW150MEFR18X45	2 x150 μF (series) x 18 (parallel)	1.38	49.68
C2	165 μF	ESMR451VSN331MR30S	2 x 330 μF (series)	3.2	6.4
M1-M6, D1-D6	Six-pack module	CCS020M12CM2	1	198	198
M7, M8	25 mΩ/1200 V	C2M0025120D	2	73.3	146.6
D7, D8	20 A/1200 V	C4D20120D	2	16.07	32.14
				TOTAL USD$	**632**

Table 3-5 Bill of materials cost for power components in third harmonic injection SEPIC powertrain

Component	Value	Quantity	Part No.	Unit Price	Total
L1, L2	500 μH	2	3stacked kooLMu77191 Cores/66turns/AWG14	50	100
L3, L4	500 μH	2	3stacked kooLMu77191 Cores/66turns/AWG14	50	100
C1, C2	7.5 μF	2x7.5 μf (series) 2(parallel)	B32794D8755	3.93	31.44
Co1, Co2	2700 μF	18x150 μf/450 V (parallel)	450BXW150MEF C18X45	1.38	49.68
M1, M2	25 mΩ/1200 V	2	C2M0025120D	73.3	146.6
Do1, Do2	20 A/1200 V	2	C4D20120D	16.07	32.14
Ta ,Tb, Tc	25 A/1200 V	6	IKW25N120T2	3.86	23.16
D1-D6	3-phase full-bridge diode	1	VS-26MT120	12.99	12.99
			TOTAL USD$		**496**

Another advantage of proposed topology in comparison to benchmark is that it needs only five driver circuits compared to eight in conventional solution therefore, cutting the cost for three driver circuits. These benefits are summarized in the Table 3-6.

Table 3-6 Comparison of proposed topology against boost follows buck benchmark

	Proposed 3rd harmonic injection SEPIC AC/DC		Conventional solution of Boost follows buck
Power components cost [USD$]	496	<	633
Number of switch drivers	5	<	8
Losses at low AC line (120 V)	307 W (Less expensive thermal design)	<	334.5 W

3.9 Experimental results

For a proof concept of the proposed topology, a prototype, shown in Figure 3-12, was built and tested up to 2 kW of power level. The DSP signal sampling/conditioning circuit presented in Chapter 2 and illustrated in Figure 2-10 was used for the control. Furthermore, CREE CRD8FF1217P driver boards were used to drive bi-directional switches Ta, Tb, Tc and MOSFET switches M1 and M2.

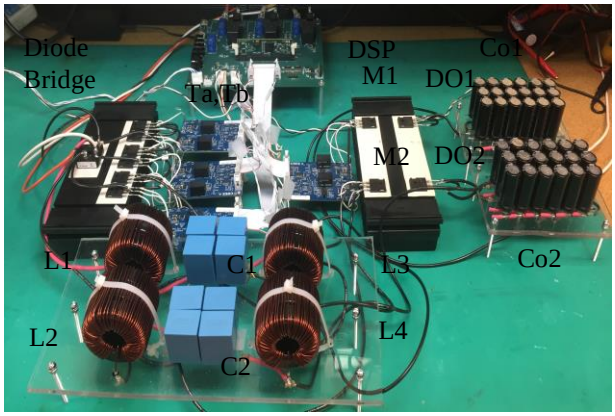

Figure 3-12 Picture of Prototype developed for the three-phase 3rd harmonic injection SEPIC derived AC/DC PFC

The experimental results showing the control signals for bidirectional switches Ta, Tb and Tc are provided in Figure 3-13 and Figure 3-14. The control signals in Figure 3-14 follow the same switching pattern as in Table 3-1 for the six zones of operation. The triangular shape measured voltage on the third harmonic injection network shown in Figure 3-15 and Figure 3-16 confirm that the control signals on this network are working properly.

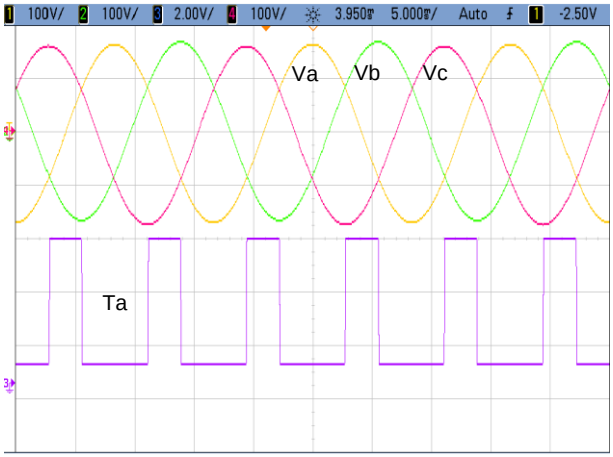

Figure 3-13 Three-phase input mains and control signal for bidirectional switch Ta

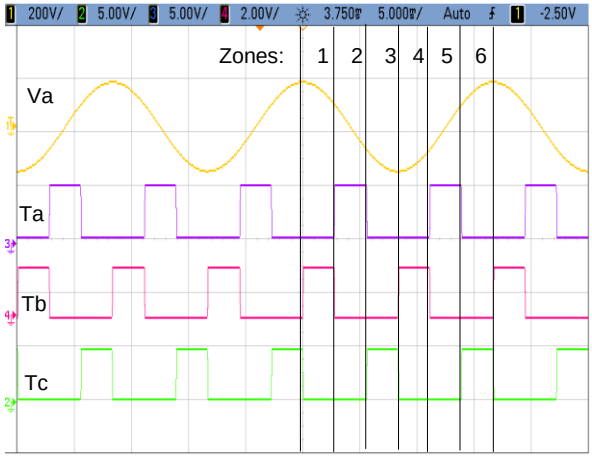

Figure 3-14 Phase a and Control signals Ta, Tb, Tc

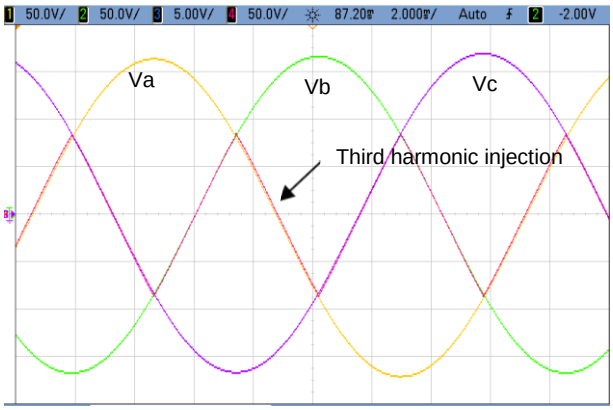

Figure 3-15 Voltages of phases a, b, c and third harmonic injection network voltage (red waveform)

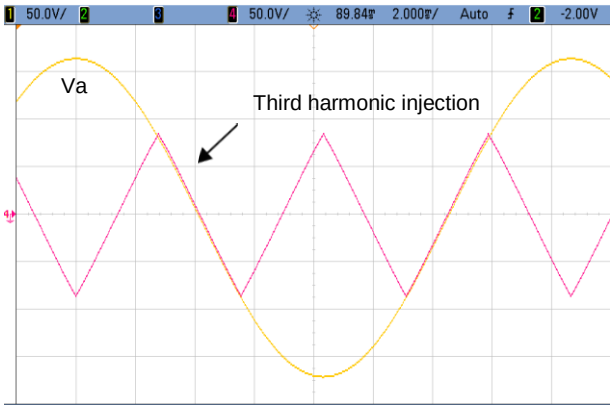

Figure 3-16 Voltage of phase a along with third harmonic injection network voltage

Figure 3-17 provides the voltage and current of the converter at 120 V AC (low-line) input and 2 kW of power level. The current and voltage are in-phase. There are some minor oscillations in the input current, which are due to the stray inductances of the wires used to connect the circuit blocks. These could likely be eliminated with a properly designed PCB based prototype.

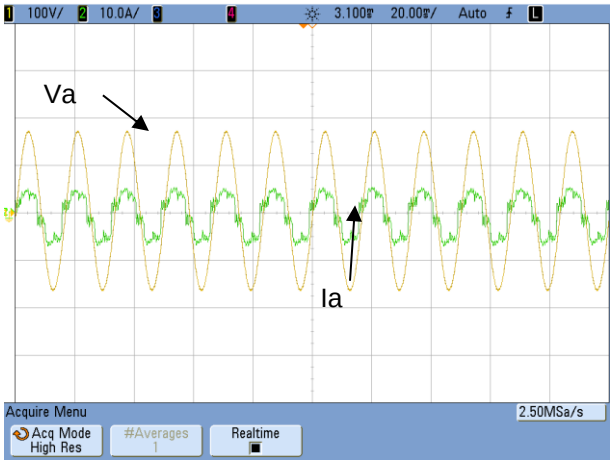

Figure 3-17 Voltage and current of phase A at low-line 120 V and 2 kW of output power

In Figure 3-18, the 400 V DC output voltage along with the voltage across Co1 and Co2 are captured. As expected from simulation, the ripples of capacitors Co1 and Co2 are 180° phase shifted and cancel thus providing a smooth DC output.

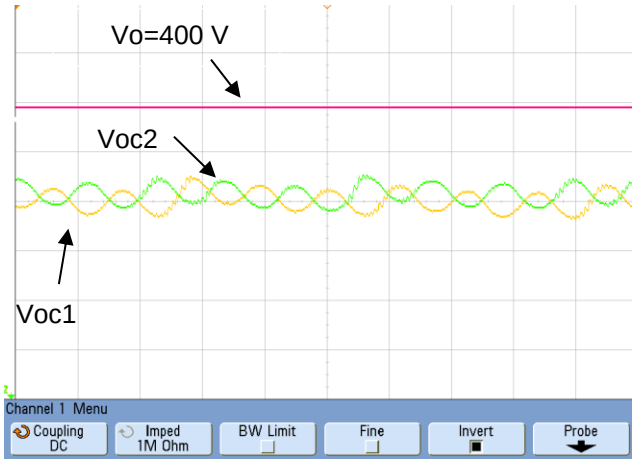

Figure 3-18 Output voltage along with voltages across capacitors Co1 and Co2.

3.10 Summary

A novel single-stage three-phase universal input 208 V – 480 V with 400 V DC output third harmonic injection SEPIC PFC was proposed. The theory of operation was presented along with simulation and analytical equations describing the sizing of powertrain components. A prototype was built and tested at 2 kW as a proof of concept. The total cost for this converter was compared with the benchmark solution of buck follows boost and was shown to be 22 % lower. The modeled efficiency also shows potential improvement at low-line and at 5 kW. These benefits make this topology a favorable solution for a universal input PFC with 400 V DC output voltage. However, this topology is uni-directional and cannot operate in inversion mode as in the two–stage buck follows boost bi-directional benchmark. In the next Chapter, an improved two-stage buck follows boost converter architecture is proposed in order to improve efficiency, while maintaining cost and bi-directional capability.

Chapter 4: **Universal input AC three-phase power factor correction with adaptive intermediate bus voltage to optimize efficiency**[2]

In this chapter an adaptive intermediate bus voltage solution to optimize efficiency in a universal three-phase AC input (200 - 480 V) cascaded buck-follows-boost power factor corrected (PFC) converter with a 400 V DC output voltage is proposed. With this application and architecture, the output voltage of the boost converter needs to be higher than the peak AC input voltage to maintain PFC and regulation. The conventional approach discussed in Chapter 2: would regulate the intermediate bus voltage to near 800 V DC; this allows for 480 V AC high line input, plus allowable overvoltage tolerance and margin for regulation, but it incurs heavy losses at low line input. This work proposes to adaptively change the bus voltage between the boost and buck stages, based on the value of the AC input voltage, and the use of a relay to bypass the buck stage for low AC line input conditions in order to maximize efficiency. A loss analysis is included to show the significant loss savings and efficiency improvement using the proposed method. Experimental results are presented for a 5 kW silicon carbide based prototype. The proposed method demonstrates up to a 4.4 percentage point increase in efficiency (220 W decrease in loss) at low AC line input compared to the conventional PFC approach with an 800 V DC intermediate bus voltage.

4.1 **Introduction**

Universal AC input, three phase power, and 400 V DC output are desirable specifications for kilowatt level power factor corrected (PFC) converters. Universal AC input reduces product development costs by avoiding two or more converter designs for different global AC mains voltages. Three phase input reduces the cost of mains wiring for end users as compared to single-

[2] The work proposed in this chapter has been published in :
[50] H. Hafezinasab, W. Eberle, D. S. Gautam, and C. Botting, "Universal Input AC Three-Phase Power Factor Correction With Adaptive Intermediate Bus Voltage to Optimize Efficiency," IEEE Transactions on Industry Applications, vol. 55, pp. 1698-1707, 2018.H. Hafezinasab, W. Eberle, D. Gautam and C. Botting, "An adaptive selection of intermediate bus voltage to optimize efficiency in a universal input three-phase power factor correction circuit," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, pp. 24-29, 2018.

phase operation [27]. The 400 V DC output is common for front-end PFC stages in power supplies and battery chargers, typically followed by an isolated DC-DC converter using 600 V rated silicon devices[3], [4] as illustrated in Figure 4-1.

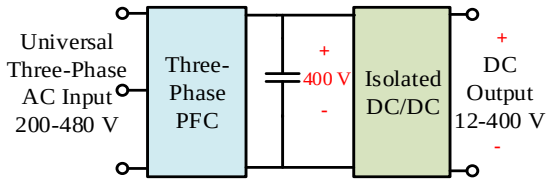

Figure 4-1 Block diagram of a typical three-phase kW level PFC rectifier with 400 V DC bus voltage and application specific DC output voltage typically between 12 V and 400.

Studies have shown that a 400 V DC distribution system is favorable in data center applications, and has been adopted for other industrial applications [5], [6]. Silicon carbide devices are also getting more popular for PFC applications for their high efficiencies. In [29], a high efficiency SiC based three-phase buck PFC converter for application in data centers is presented and a single-phase on-board SiC based charger with high efficiency is proposed in [30]. The focus of this work is on the first block in Figure 4-1, i.e. a universal input, non-isolated, SiC based, three-phase AC input, PFC converter with 400 V DC output. This application requires a converter topology with step up/down capability to maintain output voltage regulation over the global typical nominal three-phase AC input voltage range of 200-480 V [31]. In Table 1-1 , a summary of typical line-to-neutral (V_{LN}) and line-to-line (V_{LL}) voltages by global region is provided. In Japan, the distribution system is open-delta. This system has 200 V line-to-line voltage with the neutral wire connected to the mid-point of the open-delta winding, therefore providing 100 V line-to-neutral. Accordingly, the line-to-line voltage is not $\sqrt{3}$ times the line-to-neutral as in conventional distribution systems [32]. Different solutions for universal input and 400 V DC output were discussed in Chapter 1: . A three-phase six-switch boost converter followed by a synchronous buck (i.e. buck-follows-boost) is a two-stage approach featuring reduced component stress compared to single-stage three-phase PFC with the potential of bi-directionality. This architecture approach is illustrated in Figure 2-1, is well suited for three-phase universal input and 400 V DC output PFC applications. For high line three-phase AC universal input, the intermediate bus voltage (i.e. between the boost and buck stages) must be at least 747 V DC (i.e. 480 V_{LL} rms +

10% overvoltage tolerance = 528 V rms = 747 V_{PK}). The conventional solution would fix the bus voltage at near 800 V DC so that the converter has margin for regulation at high line input. However, a variable bus voltage combined with other modifications proposed can help to improve the overall efficiency at lower mains voltage and is the focus of this chapter.

Optimizing efficiency using a variable DC bus has been proposed for a wide range of power conversion applications. Notable works include the following. An optimum DC bus approach for an inverter motor drive application was proposed in [33]. Use of a variable DC bus voltage to optimize efficiency in a high-power silicon carbide (SiC) based electric vehicle charger was presented in [42]. The influence of the DC link bus voltage on power losses and thermal characteristics in a bidirectional two-level DC-AC inverter was presented in [45]. A method to optimize efficiency by adjusting the DC bus voltage in a hybrid photovoltaic-grid power system was introduced in [44]. Finally, a variable bus voltage optimal operating point tracking technique for an LLC converter coupled with a universal input SEPIC PFC was presented in [30] and [46]. However, an investigation of the impact of the intermediate bus voltage on a three-phase buck-follows-boost coupled with methods to optimize efficiency via the bus voltage is not discussed in the literature.

Taking into consideration the advantages of the two-stage DC-DC buck follows AC-DC boost PFC for a three-phase universal input PFC application, this chapter proposes a system to maximize efficiency and minimize THD by utilizing three key concepts: 1) variable DC intermediate bus, 2) a buck bypass relay system (to minimize losses for low AC input line conditions), and 3) a percent margin concept (to ensure PFC is achieved for practical considerations, including but not limited to component tolerance). The proposed system is compared to a conventional 800 V DC intermediate bus benchmark discussed in chapter 2.

The proposed adaptive intermediate bus control logic is presented in section 4.2. A simulation of total harmonic distortion (THD) and detailed loss analysis is presented in section 4.3, and experimental results are presented in section 4.4. The conclusions are presented in section 4.5.

4.2 Proposed adaptive intermediate bus system

The minimum intermediate bus voltage between the boost and buck stages in a three-phase cascaded buck-follows-boost front-end must be greater than the peak of the line-to-line input voltage to ensure output voltage regulation and PFC [7], as noted by (4-1).

$$\mathrm{V_{Bus}} \geq \sqrt{2}\mathrm{V_{in_{LL}}} \tag{4-1}$$

Below the minimum bus voltage, i.e. $V_{Bus} < \sqrt{2}\mathrm{V_{in_{LL}}}$, the converter input current THD increases steeply and regulation is lost (as is demonstrated later in Section 4.3). Assuming some error in voltage measurement and control, it is necessary to add margin to this minimum operating point for reliable PFC operation. A suitable voltage margin for reliable PFC operation may be adopted by either adding a fixed amount of voltage margin, or scaling up by a fixed percentage, as given by (4-2) and (4-3), respectively, where V_{Bus} is the minimum intermediate bus voltage for reliable PFC operation, V_{Margin} is a fixed voltage and $\%Margin$ is a percentage of input line-to-line peak voltage.

$$\mathrm{V_{Bus}} = \sqrt{2}\mathrm{V_{in_{LL}}} + V_{Margin} \tag{4-2}$$

$$\mathrm{V_{Bus}} = \sqrt{2}\mathrm{V_{in_{LL}}}(1 + \%Margin) \tag{4-3}$$

For a practical design, the % Margin should be chosen to accommodate the maximum component tolerance stack up in the Vin and Vbus voltage measurement circuits, as well as Vbus ripple caused by control overshoot, input line transients, wave shape distortion, and 3-phase voltage unbalance. Experimentally, it was determined that 7% works well.

4.2.1 Powertrain

For the universal AC input voltage, with a conventional non-adaptive system, illustrated in Figure 2-1, the boost PFC output intermediate bus voltage must be at least 747 V, so it is typically set to 800 V to maintain output regulation and PFC. By contrast, the proposed adaptive intermediate bus voltage system is illustrated in Figure 4-2. The system includes a three-phase boost PFC input stage, followed by a second stage buck converter and a relay. The principles of

operation for a three-phase six-switch AC/DC PFC and control strategies can be found in [11], [22].

The output of the system is regulated to 400 V. This system uses control to sense the input voltage and then optimizes the boost PFC output voltage. The algorithm allows voltage boosting to be minimized, reducing losses in both the boost and the buck converters by reducing losses in the active and passive components. Furthermore, the system includes a relay to bypass and disable the second stage buck converter when the AC line is low, such that the optimized boost PFC voltage is directly regulated to 400 V, further improving efficiency. However, since the buck stage is by-passed at low-line, the utilization factor of the converter is not as good as a single-stage boost or buck converter. This is inherent with a universal AC input design as it should work in both boost and buck modes.

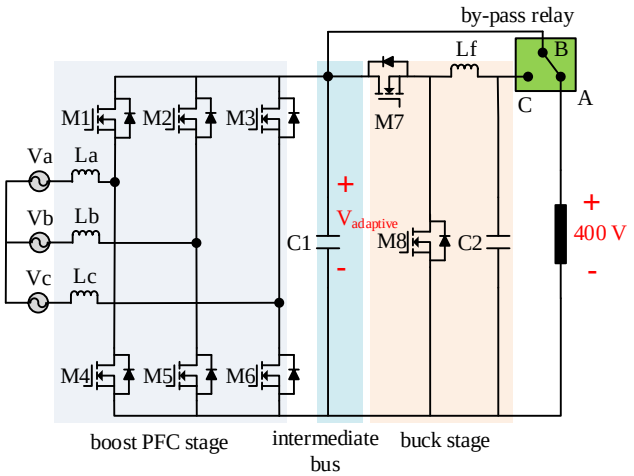

Figure 4-2 Proposed adaptive bus universal input three-phase cascaded boost-buck PFC

An alternate approach for low AC line voltages (i.e. when the peak voltage is less than 400 V) is to leave the buck stage on with 100% duty cycle. This would save the cost of the relay and its coil driver circuitry but would incur higher conduction losses in the buck converter's series MOSFET and inductor. By using a relay with a few milliohms of contact resistance, the conduction loss is negligible, resulting in higher efficiency. In this paper our focus is efficiency, so the bypass relay solution is discussed and presented experimentally.

4.2.2 **Modulation and control**

A plot of the allowable boost PFC output voltage as a function of the AC mains voltage is provided in Figure 4-3. With conventional non-adaptive control, the boost stage minimum output voltage is always 800 V on the upper horizontal blue line. However, with adaptive control for varying AC input voltage, the boost PFC stage output should be regulated along the red line plus some margin for reliable operation. The optimization control strategy is summarized in the flow chart presented in Figure 4-4.

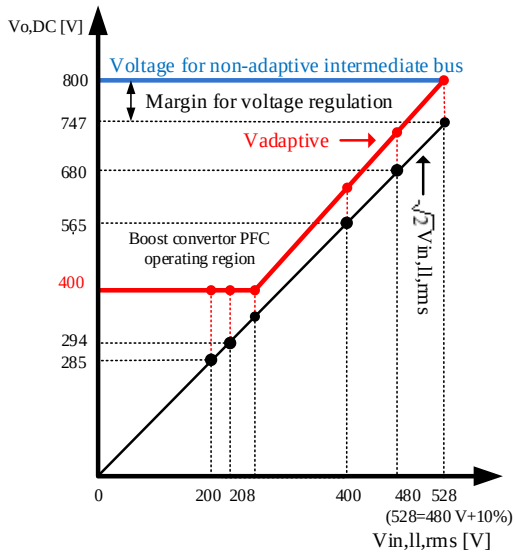

Figure 4-3 Allowable boost PFC output voltage as a function of AC mains input voltage for non-adaptive 800 V PFC bus and adaptive PFC bus. The black dots are minimum allowable voltage while the red dots are the peak voltage at different mains plus a margin.

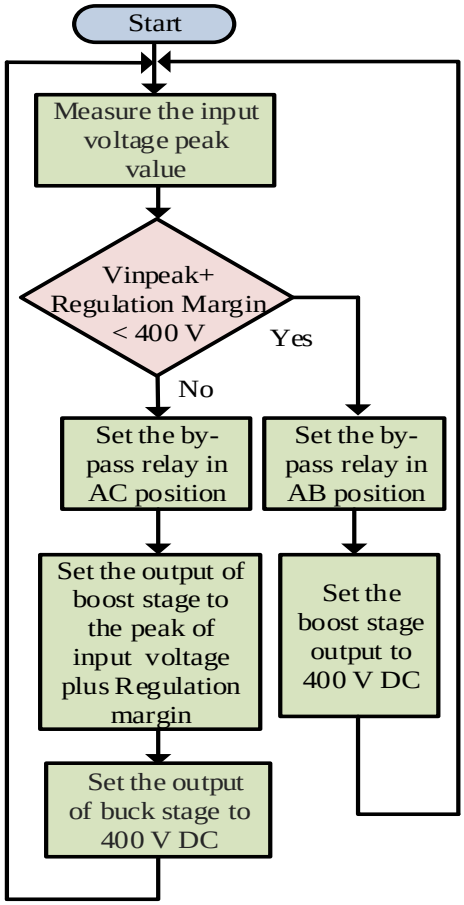

Figure 4-4 Flow chart of proposed adaptive algorithm.

With proper selection of the relay state in Figure 4-2 and adaptive selection of the intermediate bus voltage, the efficiency of the two-stage converter is optimized using two strategies. For AC input mains voltages with a peak value of less than 400 V, the second stage is bypassed (i.e. state A-B) and the output of the boost converter is set to 400 V DC. On the other hand, if the input voltage peak is above 400 V, the relay is switched to state A-C and the intermediate bus voltage is set as given in (4-3).

A simplified block diagram for the digital implementation of the proposed converter is presented in Figure 4-5. DQ control and space vector modulation (SVPWM) can be used to control the boost PFC stage and are described in the following sub-sections.

4.2.2.1 **Boost PFC DQ control**

The equation describing the voltage and current through the boost inductor, neglecting the ohmic resistance, is:

$$v_{n1} = v_n - L\frac{di_n}{dt} \quad \text{4-4}$$

In (**4-4**) n denotes phases a, b and c. L is the phase inductance. v_n is the phase voltage and v_{n1} is the inductor voltage on the converter side. Using the abc/dq rotating frame transformation, (4-4) is decomposed into equations (4-5) and (4-6) [22]. Where v_d and v_q are direct and quadrature components for three-phase AC input voltage. v_{d1} and v_{q1} are direct and quadrature voltage of converter on the inductor side, ω angular frequency of the mains and finally, i_d and i_q are direct and quadrature components of AC input current. For PFC operation, the i_q component is forced to zero while i_d is controlled by outer voltage loop to control the converter bus voltage.

$$v_{d1} = v_d - L\frac{d_{id}}{dt} + \omega L i_q \quad \textbf{4-5}$$

$$v_{q1} = v_q - L\frac{d_{iq}}{dt} - \omega L i_d \quad \textbf{4-6}$$

The closed-loop realization of the targeted adaptive intermediate bus voltage i.e., $V_{adaptive}$ in Figure 4-5, requires multiplying the peak of the line-to-line voltage by the necessary margin (i.e. 1+*%Margin*). The peak of the line-to-line voltage can be calculated using rms measurement software blocks. However, with DQ control for the boost stage, and using the abc/dq transformation, the direct voltage, v_d, and quadrature voltage, v_q, are known. The v_d component in the rotating frame has a DC value equal to the peak of line to neutral voltage [22], thus using scaling factor, K, as in Figure 4-5, the proper value for $\mathrm{V_{Bus}}$ is calculated. This method saves execution time by skipping the calculation of the input rms voltage, Vrms. This value is further applied to the decision block to set the proper intermediate bus voltage.

The relay position and buck stage operation are also set using the $\mathrm{V_{Bus}}$ value. Moreover, the outer loops generating the reference values for $\mathrm{Vd}*$ and $\mathrm{Vq}*$ are slow compared to the inner loops as there is no need for a fast dynamic response for the bus voltage. This is helpful for overall stability of the system against momentary fluctuations in the AC mains.

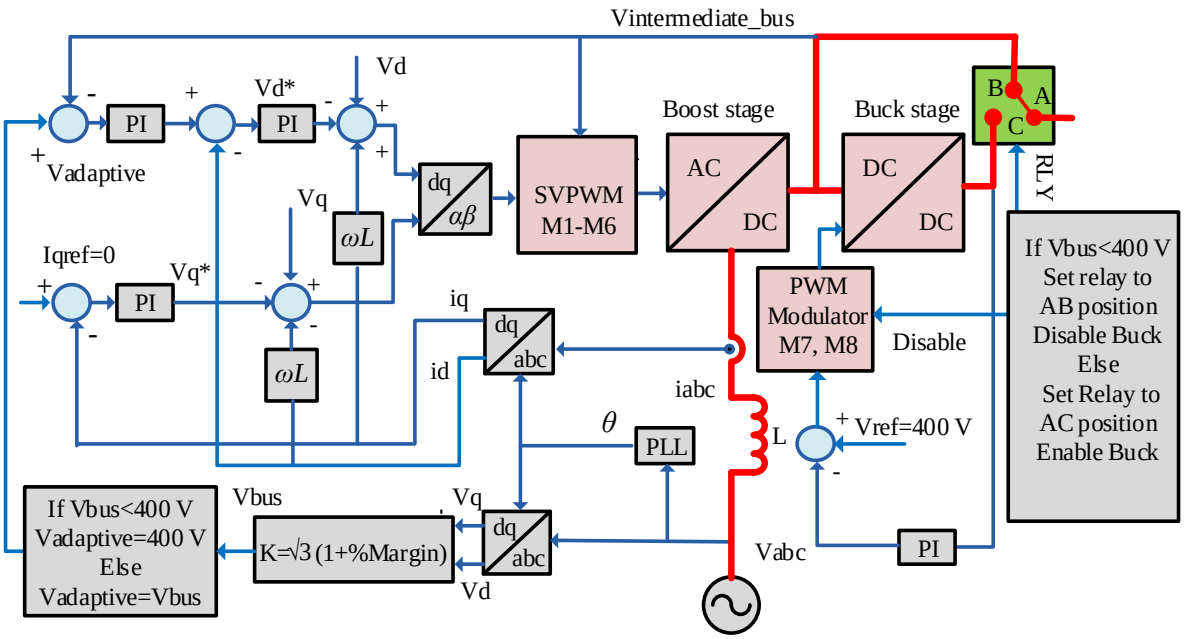

Figure 4-5 Adaptive bus control block diagram

4.2.2.2 **Boost PFC Space vector modulation**

The boost PFC stage modulation technique has an impact on the efficiency since the number of switching transitions can vary between various modulation techniques. The boost PFC converter can be driven either by carrier-based pulse width modulation (CBPWM), or space vector modulation (SVM). SVM is more commonly used due to its simplicity [7], and is selected for this work. Specific SVM strategies include discontinuous space vector modulation (DPSVM), which has four transitions in a switching cycle, and symmetrical pulse width modulation (SVPWM), which has six transitions. DPSVM has lower switching losses but higher ripple current, leading to higher THD, and increased core and copper losses in the boost inductors. Due to these drawbacks with DPSVM, SVPWM was used for both the analysis and experimental verification of this work.

4.2.2.3 **Buck stage control**

For the buck stage, voltage mode control with soft-start can be used [21].

4.3 **Simulation and loss analysis**

To show the advantages and impact of the proposed adaptive intermediate bus voltage technique, the total loss of the two-stage PFC and the input current THD are analyzed as a

function of intermediate bus voltage. The example specifications and components used in the two-stage 5 kW SiC-based PFC prototype design are summarized in Table 4-1.

Table 4-1 Specifications and Components

Specification/ Component	Value	Quantity
Rated power	5 kW	N/A
Mains line-line voltage (nominal)	200-480 V	N/A
AC line frequency	50-60 Hz	
Switching frequency	50 kHz	N/A
Six-switch boost inductors (La, Lb, Lc)	500 µH / 20 A	3
Buck stage output inductor (Lf)	500 µH / 20 A	1
Intermediate bus capacitance (C1)	900 µF	2x150 µF (series sets) x 12 (parallel)
Buck stage output capacitance (C2)	165 µF	2x330 µF in series
Boost switches (M1-M6, D1-D6)	CCS020M12CM2	6-pack module
Buck switches (M7, M8)	C2M0025120D	2
Diodes D7, D8	C4D20120D	2
Panasonic HE-V RELAYS	1000 V, 20 A Two NO contacts Contact resistance: 3 mohm	1

4.3.1 **Simulation results**

A plot of input current THD as a function of intermediate bus voltage is provided in Figure 4-6. Results are summarized at 5 kW load and for AC input mains voltages of 208 V, 400 V, 480 V and 480 V + 10%. It is evident from this figure that the minimum current THD occurs at the minimum boosting voltage (i.e. the peak of line-to-line input voltage) thus at minimum intermediate bus voltage, THD is minimized. However, at points below the minimum bus voltage, THD increases very steeply as the converter starts to lose output voltage regulation at low intermediate bus voltages and the input currents are distorted. This operating point optimizes THD and efficiency, with successful output regulation and sinusoidal input currents. For a practical design, due to tolerances and errors in signal sampling, conditioning and control, it is necessary to add

some margin to this minimum value for reliable regulation and to avoid entering the high THD region.

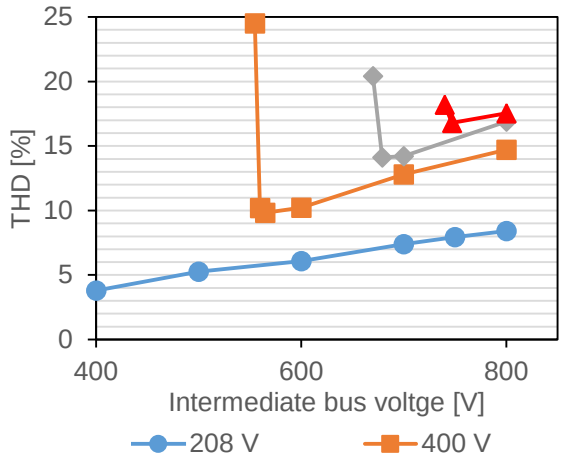

Figure 4-6 Total harmonic distortion as a function of intermediate bus voltage

4.3.2 **Loss calculations**

The methods and equations described in section 2.5 along with parameter values of Table 2-4 are used to calculate losses for different input mains values and at different bus voltages.

4.3.2.1 **Active losses**

Total active losses are determined by summing the active device switching losses as shown in Figure 4-7 and conduction losses for the converter as shown in Figure 4-8, with the results as shown in Figure 4-9. As expected, it can be observed that for any given AC line voltage, the total active losses are minimized by minimizing the intermediate bus voltage. For example, as observed in Figure 4-9, at 208 V AC input, the total active boost stage losses are 189 W if a conventional 800 V DC bus voltage, but only 90 W at 400 V intermediate bus voltage using the adaptive bus technique. Note also that at low AC line voltage conditions, such as 208 V, the buck stage active losses of 7 W can be nearly eliminated by the use of a relay to bypass the buck stage as long as the relay has lower contact resistance.

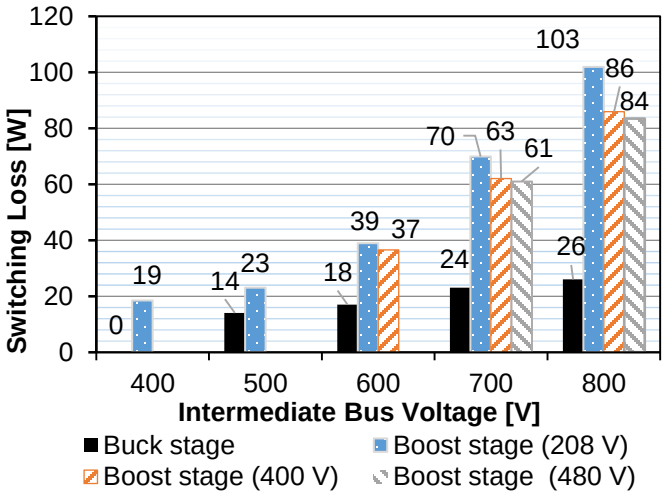

Figure 4-7 Switching loss as a function of intermediate bus voltage at 5 kW

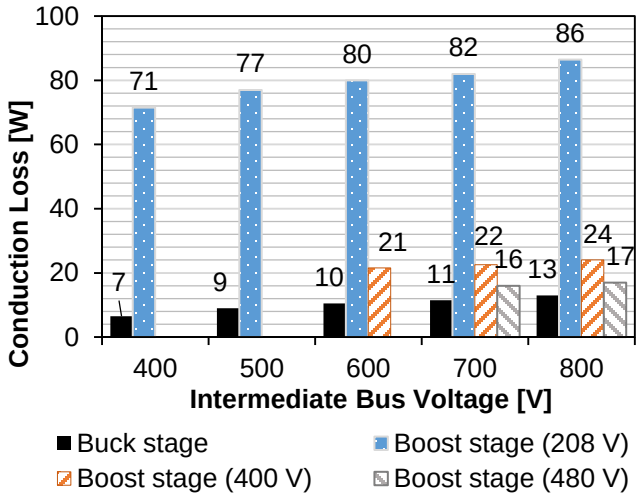

Figure 4-8 Semiconductor conduction loss as a function of intermediate bus voltage at 5 kW

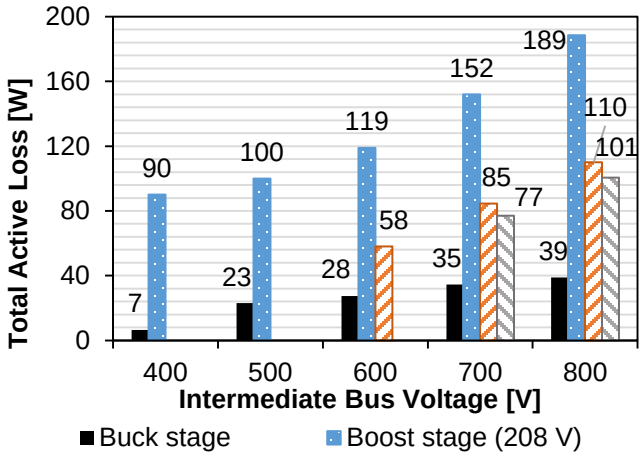

Figure 4-9 Active losses as a function of intermediate bus voltage at 5 kW

4.3.2.2 **Passive losses**

Using the specifications from Table 2-1, parameter values from Table 2-4, PSIM simulations and Mathcad analysis, the total passive losses are provided in Figure 4-10 as a function of intermediate bus voltage for AC line conditions of 208 V, 400 V and 480 V. It is clear that passive losses increase with bus voltage. The increase can be attributed to higher ripple current in the boost and buck inductors, which increases the core loss due to higher B_{pk}, and increased AC resistance copper losses.

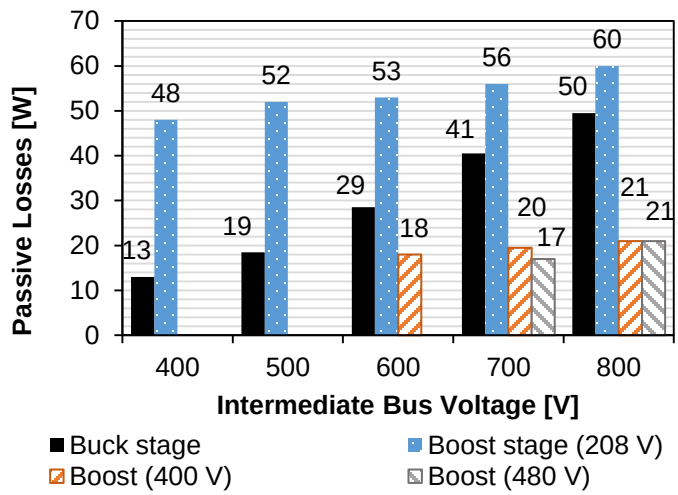

Figure 4-10 Passive losses as a function of intermediate bus voltage at 5 kW

4.3.2.3 **Total loss**

Combining all loss values, the total estimated losses of the two stage PFC as a function of intermediate bus voltage were calculated at 208 V, 400 V and 480 V AC line input. The results are summarized in Figure 4-11. The minimum loss, and hence highest efficiency, occurs at the minimum bus voltage. However, the bus voltage cannot be below the minimum value required to allow power factor correction and regulation as was noted in (4-1). Accordingly, loss results cannot be shown for intermediate bus voltages that are not viable operating points for higher AC input voltages, e.g. 400 V and 480 V. A summary of the estimated total losses for the proposed adaptive and conventional non-adaptive (i.e. 800 V bus) solutions is provided in Table 4-2. Note that for low AC line voltages, e.g. 208 V, since the peak of the voltage is less than 400 V, it is possible to either bypass the buck stage with a relay or leave the buck stage on with 100% duty

cycle. Including a relay potentially increases system cost but reduces total loss by approximately 20 W (i.e. 138 W vs. 158 W). For the relay chosen (Table 4-1) and by paralleling the two contacts, the total contact resistance of 1.5 mΩ will dissipate approximately 0.23 W at full load output current of 12.5 A, which practically may be ignored compared to 20 W loss in the buck always-on solution. Finally, the analysis demonstrates a potential loss reduction of 59 % at low AC input line compared to the non-adaptive, 800 V bus solution.

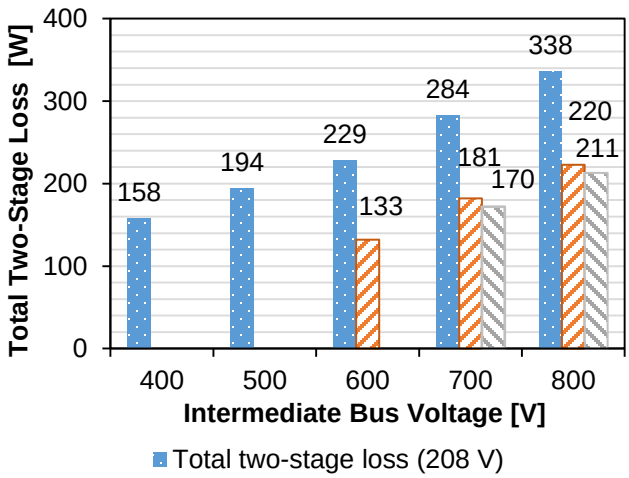

Figure 4-11 Total converter loss as a function of intermediate bus voltage at 5 kW

Table 4-2 Comparison of the adaptive and conventional 800 V bus architectures

Input Voltage [V]	800 V Bus Loss [W]	Adaptive Bus Loss [W]	Loss Reduction [W]	Percentage Loss Reduction [%]
208	338	138 (buck stage bypass relay)	200	59.2
		158 (no buck stage bypass relay)	180	53.3
400	220	133	87	39.5
480	211	170	41	19.5

4.4 **Experimental results**

The prototype built in Chapter 2: for benchmarking purposes was used to validate the proposed adaptive bus method, illustrated in Figure 4-2, in comparison to a conventional fixed

800 V intermediate bus, illustrated in Figure 2-1. Balanced operating conditions were tested since unbalanced conditions are typically limited to only 2-3% [23]. For highly unbalanced input mains conditions, there are alternate control techniques that can be used [7].

Curves of the total loss of cascaded boost-buck PFC as a function of intermediate bus voltage are provided in Figure 4-12 at 208 V, 400 V and 480 V AC (line-to-line) input for full load power of 5 kW. Efficiency curves are provided in Figure 4-13. Losses are lowest in all cases when the lowest intermediate bus voltage is selected. At 208 V low line input, a 400 V intermediate bus can be used, enabling the losses to be minimized to 160 W with the buck stage at 100% duty cycle, or 140 W with the bypass relay on to eliminate the buck stage conduction losses. This represents up to a 61% loss reduction or 4.4 percentage point efficiency improvement (97.2% vs. 92.8%) compared with the conventional fixed 800 V bus solution, which has 360 W of losses. In addition, it is noted that by selecting the minimum loss points, noted by solid circles, the total converter power loss profile becomes significantly flatter, enabling the converter to operate at full power over the universal input range without requiring an overdesigned cooling system.

Results comparing the conventional fixed 800 V bus non-adaptive solution and the proposed adaptive bus solution, assuming $\%Margin = 7\%$, for minimum intermediate bus voltage are provided in Table 4-3. The percentage loss reduction column clearly illustrates the very significant loss savings in using the proposed adaptive bus solution.

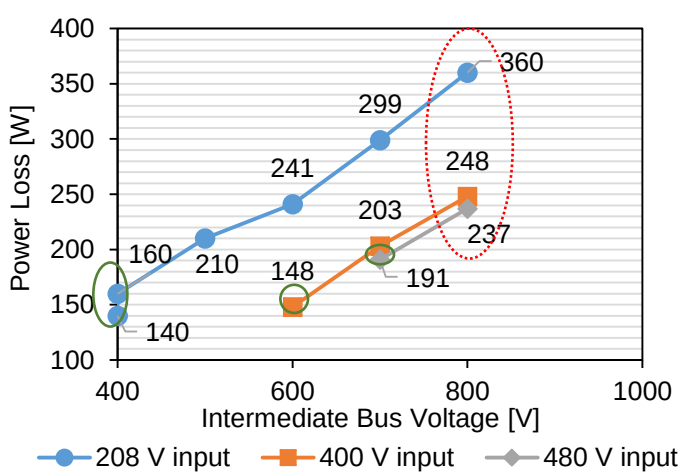

Figure 4-12 Total loss as a function of intermediate bus voltage with fixed 800 V bus operating points circled red and adaptive voltage points circled green at 5 kW.

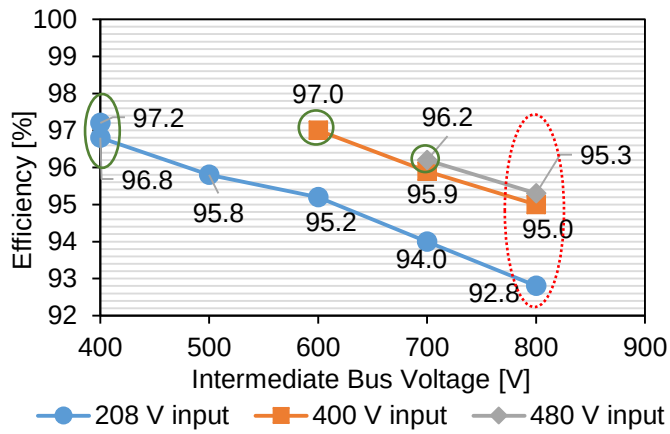

Figure 4-13 Efficiency as a function of intermediate bus voltage with fixed 800 V bus operating points circled red and adaptive voltage points circled green at 5 kW.

Table 4-3 Comparison of Measured Losses for Adaptive and Conventional non-adaptive Control at 5 kW

Input Voltage [V]	800 V Bus Loss [W]	Adaptive Bus Voltage (Margin=7%) [V]	Adaptive Bus Loss [W]	Loss Reduction [W]	Percentage Loss Reduction [%]
208	360	400 (buck stage bypass relay)	140	220	61.1
		400 (no buck stage bypass relay)	160	200	55.5
400	248	605	148	100	40.3
480	237	726	191	46	24.1

4.5 **Summary**

An adaptive intermediate bus voltage control method was presented for a universal input, three-phase AC, 400 V DC output, cascaded buck-follows-boost PFC converter. In the proposed method, the optimal intermediate DC bus voltage before the buck converter is set based on the value of input voltage, improving efficiency compared to the conventional solution using a fixed 800 V DC bus voltage. Simulation and loss analysis were presented to illustrate the THD and efficiency benefits of the proposed method. A 5 kW SiC-based prototype was built and experimental results were presented. It was demonstrated experimentally that the two-stage losses could be reduced by up to 61% (efficiency improvement of 4.4 percentage points at low AC line) with the proposed method. For a practical product design, the proposed approach would enable simplified thermal design, reducing the size of heatsinks and thus the overall cost.

The topology proposed in this chapter operates with only a three-phase AC input. For low kW level power, the capability to have one converter accept a single-phase, or three-phase AC input is attractive because it reduces product development and marketing costs. In addition, it gives users the flexibility to operate from any single, or three-phase AC supply. In the next Chapter a novel topology is proposed that can operate from a single-phase, or three-phase AC supply.

Chapter 5: **A truly universal single and three-phase power factor correction circuit** [3]

In this chapter, a truly universal wide input single-phase and three-phase AC/DC silicon carbide (SiC) based Power Factor Correction (PFC) front end converter with bi-directional capability is proposed. Specifications include single-phase input voltage of 120-240 V AC, three-phase input voltage of 208-480 V AC, and output voltage of 400 V DC at 5 kW, for applications such as battery chargers and data centers. The presented topology is comprised of four half-bridge totem pole legs, passive components, and two relays to reconfigure the converter in each of three modes: single-phase three-channel interleaved totem pole boost, three-phase boost, and three-phase cascaded boost-buck. The firmware switches the relays to the proper state for single-phase or three-phase operation and adjusts the intermediate bus voltage using an adaptive algorithm to maximize efficiency. Calculation of losses, current and voltage stresses in the components shows that, using the proposed topology, a single product can be sized appropriately for both single-phase and three-phase universal input PFC with 400 V DC. A 5 kW SiC-based prototype converter is developed to verify the analysis for the proposed topology.

5.1 **Introduction**

Front-end power factor correction (PFC) converters that can accept both single-phase and three-phase universal AC at their input, i.e. truly universal PFC, are beneficial for kW level DC load applications, such as battery chargers and data centers. Furthermore, these applications typically require a 400 V DC intermediate bus, followed by a second isolated DC/DC conversation stage to meet safety requirements and in order to utilize the high bandwidth of the second stage to eliminate double line frequency ripple at the output. This type of power conversion architecture is already illustrated in the block diagram provided in Figure 4-1. The focus of this work and

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3 This work has been submitted to the IEEE Transactions on Power Electronics and a U.S. Patent Application has been submitted:
[61] H. Hafezinasab, W. Eberle, D. Gautam and C. Botting," A Truly universal single and three-Phase Power Factor Correction Circuit" submitted July 2020 to the *IEEE Journal of Emerging and Selected Topics in Power Electronics*

discussion is on the first stage, i.e. the truly universal PFC with a 400 V DC output. A truly universal AC input design saves the cost of developing multiple products for various single-phase and three-phase AC mains voltages and also reduces other costs such as product marketing. In addition, a 400 V DC output is typical for front-end PFC's followed by an isolated DC/DC stage using 600 V switches [3]. In data center applications, studies have shown that a 400 V DC bus power distribution architecture is more efficient and reliable compared to traditional AC distribution [5], [6].

A truly universal AC input PFC with 400 V DC output should operate globally with both single-phase and three-phase AC mains voltages. These nominal voltages are summarized in Table 1-1, with single-phase voltages in the range of 100 V to 240 V, and three-phase voltages ranging from 200 V to 480 V [31], [32]. In Japan, the electrical distribution system is open-delta, thus the line-to-line voltage is not $\sqrt{3}$ times the line-to-neutral voltage as in conventional distribution systems [32].

Three-phase PFC front-end converter implementations can be either phase-modular, or direct three-phase [11]. A phase-modular design uses three single-phase PFC converters connected in Wye or Delta, while a direct three-phase design is a single integrated topology with three-phase mains input. The direct three-phase approach benefits from overlapping of the phases, thus less filtering is needed compared to using existing single-phase modules, where the double line frequency ripple in each phase needs to be filtered by a large capacitor. Due to a higher component count compared to direct three-phase topologies, the cost of the phase-modular approach is higher. One of the major advantages of the phase-modular approach is the reuse of existing single-phase design knowledge to implement a three-phase PFC. However, a typical universal input single-phase PFC converter is designed for 85-265 V (240 V+10%) which does not allow sufficient head room for a three-phase nominal voltage of 480 $V_{LL,}$ even if a Wye connection reduces this to 277 VLN. For these reasons, phase-modular solutions are not optimal for three-phase input applications and accordingly, direct three-phase solutions are considered exclusively in the discussion that follows.

Direct three-phase buck and boost topologies were reviewed in [8] and [9]. For regulation and PFC operation, the output DC bus voltage of a boost converter must be equal to or greater than the peak value of the input voltage, thus a boost converter cannot provide 400 V DC output voltage for three-phase high-line AC mains input. Conversely, a buck converter cannot provide 400 V DC output voltage for low-line AC mains input [7]. Thus, for universal input applications, a PFC converter must be able to both step up and step down the voltage.

A step up/down topology may be implemented using a single-stage, or a two-stage approach. Three-phase single-stage PFC's are derived from DC/DC buck-boost, SEPIC and Ćuk converters. They have lower component counts as compared to two-stage topologies, but higher current and voltage stresses on the majority of components. A single-stage topology derived from a SEPIC DC/DC converter was proposed in [8]. As compared to a single-phase AC/DC SEPIC, it has one more diode and one more capacitor in each phase leg. Benefits of this topology include a simple three-level structure, sinusoidal input current, and full output voltage controllability. However, stresses on components are higher than most two-stage solutions. A three-phase single-stage buck-boost PFC structure, derived from a DC/DC buck-boost converter, was presented in [38]. The current stress in the inductor in this type of converter, when operating in buck mode, can increase to several times the load current [39], making the inductor large and lossy for a universal AC input high power design. The switches also need to handle the inductor current, thus incurring higher current stress compared to a two-stage boost plus buck, or buck plus boost solution. A control method for a single-stage three-phase AC/DC boost-buck derived from DC/DC Ćuk converter and its isolated version were proposed in [38]. In this method, the switches must handle higher current stress compared to a two-stage topology, since at zero vector instants the output inductor and input inductor phase currents sum, increasing the peak and rms currents in the switches.

Two-stage topologies with a universal AC input and 400 V DC may have a boost plus buck or buck plus boost structure, where the first stage performs rectification and PFC and the second stage performs DC/DC regulation. The conventional three-phase buck PFC is discussed in [11].

This converter followed by a boost stage forms a universal input three-phase PFC [40]. An advantage is that a single inductor serves both buck and boost stages, however at low AC line voltage the inductor carries a current at least two times the load, resulting in a large inductor. Traditional buck plus boost converters are also inherently unidirectional and therefore cannot be used for applications requiring bidirectional power flow, such as vehicle to grid (V2G). The only exception being is if diodes are replaced with switches. A bidirectional three-phase buck PFC which combines two separate buck PFC converters in opposing directions was presented in [41]. This configuration nearly doubles the hardware cost relative to a conventional unidirectional buck, and only one converter is working at a given time, leading to low power density.

A three-phase six-switch boost converter followed by a synchronous buck is a two-stage topology architecture is suitable for a universal three-phase AC input PFC with 400 V DC and has the potential for bi-directionality. It features reduced component stress compared to a single-stage three-phase PFC and is well suited high power I high power applications, including battery chargers requiring V2G and or data centers. Furthermore, by using adaptive control of the intermediate bus voltage between the boost PFC and buck DC/DC converters, the efficiency of this converter can also be significantly improved [50]. In comparison to a conventional 800 V DC intermediate bus (i.e. between the boost PFC and buck stages). Overall, the three-phase boost plus buck PFC converter architecture has clear advantages compared to other solutions for a universal three-phase AC input PFC with 400 V DC output.

Single-phase PFC converters commonly use the conventional diode bridge boost PFC topology. While this design is reliable, it suffers from well-known efficiency and thermal issues due to high conduction losses in the diode bridge rectifier, and is also unidirectional [49]. Bridgeless PFC topologies have been developed to overcome these issues, reducing diode conduction losses, and allowing bidirectional operation [4], [49], [51], [57]. Interleaving also helps to increase the nominal power of the converter, reduce current ripple amplitude, and increase ripple frequency [39], reducing EMI filter requirements. In [55], a two-channel interleaved bridgeless totem pole PFC was proposed. The wide-bandgap silicon carbide (SiC) switches used

have a very low reverse recovery diode current, enabling the converter to operate in continuous conduction mode (CCM). Therefore, the interleaved totem-pole topology has compelling advantages compared to a conventional diode bridge boost PFC, and is particularly suitable for a universal AC input single-phase PFC with 400 V DC output with potential for bidirectional operation

In this chapter, a truly universal AC input PFC topology is proposed that combines the advantages of single-phase and three-phase universal AC input PFC converters supplying a 400 V DC output. The proposed topology architecture is essentially a three-phase cascaded boost PFC followed by buck DC/DC converter and three-channel interleaved totem-pole PFC, utilizing relays to switch between the constituent topologies. In section 5.2 the proposed topology and modes of operation are presented. A procedure for powertrain component design and sizing is presented in Section 5.3. Section 5.4 discusses single-phase and three-phase control methods along with the adaptive intermediate bus voltage. A loss estimation is presented in Section 5.4.4, and the experimental results are presented in Section 5.4.5.

5.2 **Proposed topology**

The proposed truly universal PFC topology architecture is illustrated in Figure 5-1. It utilizes four half-bridge totem pole legs, two relays, and four inductors, two capacitors and two relays. By changing the states of the relays, as shown in Table 5-1, the topology can be easily configured in three different operating modes to achieve PFC and a 400 V DC output: i) single-phase three-channel interleaved totem pole, ii) three-phase boost, and iii) three-phase cascaded boost plus buck.

Table 5-1 Operating modes for the proposed universal AC input topology

Mains voltage	RELAY1	RELAY2	Mode of operation
100 V, 120 V, 240 V 1~	AB	AC	Single-phase three-channel interleaved boost
200 V, 208 V 3~	AB	AB	Three-phase boost (buck stage bypassed)
400 V, 480 V 3~	AC	AB	Three-phase cascaded boost plus buck

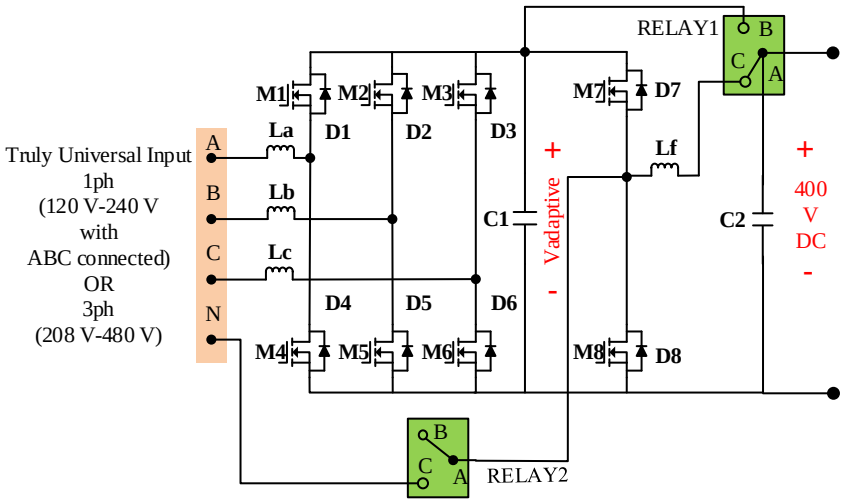


Figure 5-1 Proposed truly universal input single-phase/three-phase PFC with 400 V output

5.2.1 Single-phase input

By setting RELAY1 in the AB position and RELAY2 at AC as in Figure 5-2, the converter is configured as a three-channel interleaved boost totem pole PFC. M1-M6 are high frequency MOSFETs, and M7 and M8 are line frequency MOSFETs that provide the return current path for line current in the negative and positive half cycles, respectively [55]. For a boost converter to maintain PFC, the output DC bus voltage needs to be equal to or greater than the peak value of the input voltage [7] as given by (4-1), where V_{Bus} is the output DC bus voltage, and V_{in} is the rms line-to-neutral voltage in single-phase mode, and line-to-line voltage in three-phase mode.

For single-phase mode of operation with a 400 V output DC bus, PFC is guaranteed over the whole input range as the high-line peak voltage, assuming 10% overvoltage is less than 400 V (i.e. $240\sqrt{2} + 10\% = 374\,V < 400\,V$) and the regulation is achieved without the need for a second stage to step down the voltage to 400 V, as is required for high-line three-phase inputs.

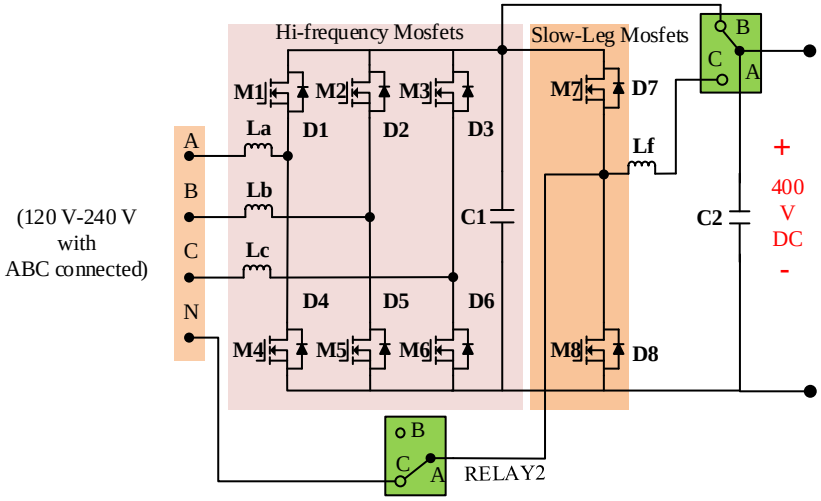


Figure 5-2 Single-Phase three-channel interleaved mode of operation

5.2.2 **Three-phase input**

By setting both RELAY1 and RELAY2 in the AB positions as in Figure 5-3, the converter is configured as a three-phase boost PFC converter. This mode is suitable for three-phase low-line AC mains, where the peak of the line-to-line voltage is less than 400 V.

For PFC operation with AC mains voltages that have a line-to-line peak greater than 400 V, the cascaded boost followed by buck mode of operation is required to provide 400 V DC output. In this case,Figure 5-4, RELAY1 is set to the AC position and RELAY2 to AB. Furthermore, in cascaded two-stage operation, the intermediate bus voltage can be changed adaptively in order to maximize efficiency, as is discussed in Chapter 4: .

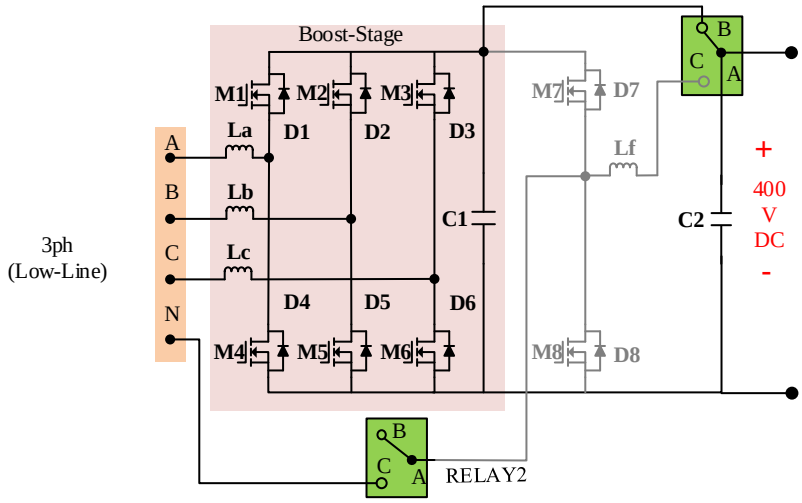


Figure 5-3 Three-Phase Boost mode of operation

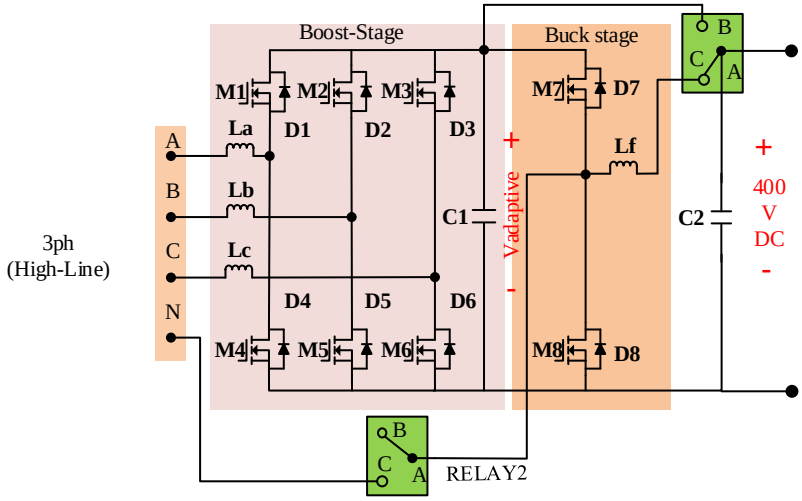


Figure 5-4 Three-phase boost-buck mode of operation

5.3 Converter power train design

To demonstrate the feasibility and advantages of the proposed truly universal PFC topology, a 5 kW prototype with the specifications listed in Table 5-2 was designed. The component selection and design for each mode of operation is discussed in this section.

Table 5-2 Specifications of prototype developed

Specification	Value
Rated power	5 kW
AC Mains (nominal)	200-480 V 3~ 120-240 V 1~
AC line frequency	50-60 Hz
Switching frequency	50 kHz

5.3.1 Boost inductors

Boost inductors are sized based on maximum target ripple current and the maximum power level they need to handle. These criteria are used to choose the magnet wire gauge, core size and material. The maximum ripple in the single-phase and three-phase operating modes are important, as they are used to determine core loss, and they impact the EMI input filter size.

5.3.1.1 Single-phase input

In this mode, the single-phase AC mains voltage range is 100-240 V. Furthermore, with the ANSI C84.1 voltage tolerance standard, the design must work in the AC input range of 85-265 V.

In single-phase AC input mode, the three totem-pole legs operate as three interleaved channels and they should equally share the converter power, so the power processed in each channel is P_o=1.667 kW. The inductors in each leg will operate with the maximum currents at the low-line input voltage, $V_{ac.min}$. At the peak current, for a current ripple percentage, r, switching period T_{sw}, and output voltage, V_o, the minimum required inductance can be calculated using 5-1 and the maximum current through the inductor can be calculated using 5-2 as discussed in [20]. For current ripple of r=0.15, output voltage of V_o=400 V, $V_{ac.min}$= 85 V and f_{sw}=50 kHz, the calculations yield a 404 µH inductor value and a 20.8 A maximum inductor current. Accordingly, the inductor is sized to be 500 µH.

$$L_{min} = \frac{V^2{}_{ac.min}}{P_o r f_{sw}}\left(1 - \frac{\sqrt{2}V_{ac.min}}{V_o}\right) \quad \textbf{5-1}$$

$$I_{Lmax} = \frac{\sqrt{2}P_o}{V_{ac.min}}(1 + \frac{r}{2}) \quad \textbf{5-2}$$

5.3.1.2 **Three-phase input**

The method along with the equations used to size the boost inductor for a voltage source converter are already described in section 2.3.1. Substituting L= 500 µH, calculated in the previous sub-section for single-phase AC input, assuming $V_{DC} = 800\ V$ and $V_m = 277\sqrt{2} + 10\% = 431\ V$, a maximum ripple current of 4.98 A is obtained. The maximum inductor ripple current is similar for both three-phase and single-phase operation, allowing a single inductor size to be suitable for both operating modes.

5.3.2 **Buck inductor**

The equations and criteria to choose the buck inductor are described in section 2.3.2. A 500 µH inductor is chosen for this prototype.

5.3.3 **Boost stage output capacitors**

For the purposes of this study, the boost stage output capacitors are sized using only the ripple voltage and voltage and current stresses. However, for a practical design, larger capacitors may be required to meet as hold-up time and/or lifetime requirements.

5.3.3.1 **Single-phase interleaved operation**

For a single-phase boost PFC, the instantaneous power, $P(t)$ consists of a DC term, P_o, and an AC component with a frequency two times the AC line input as given by 5-3.

$$P(t) = P_o + P_o\cos(2\omega t) \quad \textbf{5-3}$$

Assuming the output power is constant, the instantaneous sinusoidal power needs to be stored and released by the output capacitor. It can be shown that the output capacitor C_1 needed to compensate the variable AC term is given by 2-7, where V_o is the boost converter output voltage, P_o is output power, f_{line} is the AC line frequency and ΔV_o is the output double-line frequency ripple peak-to-peak voltage specification. The output capacitor current stress is given by 2-8 as provided in [20]. For ΔV_o = 25 V, V_o= 400 V, $V_{ac.min}$ = 85 V and P_o = 5 kW, then $C_1 \cong$ 1325 µF and $I_{\mathrm{c1\_rms}}$ = 8.99 A.

5.3.3.2 **Three-phase boost or three-phase cascaded with buck operation**

The same procedure and equations as in 2.3.3 are used to size the output boost stage capacitor. In practice, the capacitor needs to be oversized to handle unbalanced AC mains voltages, de-rating, or total loss of one phase. The worst case is the loss of one phase where the converter will operate at $P_{ph\_loss} = \frac{P_o}{\sqrt{3}}$. Using 2-7 and 2-8, $C_1 \geq 766$ µF with a current stress of $I_{c1\_rms} = 13.72A$.

In order to select the minimum capacitance, C_1, required to enable truly universal single, or three phase operation, the maximum capacitance from the two design cases must be selected. Comparing these calculations, i.e. 1100 µF for single-phase operation vs. 766 µF for three-phase operation, it is clear that more output capacitance is needed for single-phase AC input operation. Selecting suitable capacitors for single-phase operation will result in them being somewhat over-designed for three-phase operation. However, in a practical design the capacitors are often oversized by a significant factor to account for factors such as product lifetime and operating temperature range. In order to meet the single-phase requirement, the NRB-XW 450 V / 150 µF electrolytic capacitors from NIC with a current stress capacity of 1.42 A each were chosen to build

an array of 18 parallel capacitors with two series 450 V/150 µF capacitors in each parallel leg, resulting in a capacitance of 1350 µF.

5.3.4 **Buck stage output capacitor**

Using the method described in 2.3.4, the buck capacitor is sized as 165 µF.

5.3.5 **Active components**

To size the active components, a first estimation of stresses is made for the full load 5 kW output power, so low-loss SiC MOSFETs and diodes were chosen. A summary of the active and passive components from previous sub-sections is provided in Table 5-3 .

Table 5-3 5 kW universal AC input prototype components

Component	Value	Quantity
Boost inductors (La, Lb, Lc)	500 µH / 20 A	3
Buck inductor (Lf)	500 µH / 20 A	1
Boost capacitor (C1)	1350 µF	2 x150 µF (series) x 18 (parallel)
Buck capacitor (C2)	165 µF	2 x 330 µF (series)
M1-M6, D1-D6 (6-pack module)	CCS020M12CM2	1
Buck switches (M7, M8)	C2M0080120D	2
Diodes D7,D8	C4D20120D	2
Panasonic HE-V RELAYS	1000 V, 20A Two NO contacts Contact resistance: 3 mΩ	1

The maximum parameter values for the active and passive components used are the same as those provided in Table 2-4. These values were used for a worst case stress analysis and loss estimation, where R_{DS} is the drain to source resistance of the MOSFETs, R_D is the dynamic resistance for each diode, V_f is the diode forward voltage drop, R_{Gext} is the gate external resistance, R_{DC} and R_{ac} are the DC and AC resistances of the inductor coils, ESR is capacitor equivalent series resistance and finally α, β, γ are inductor core loss coefficients [25]. The worst-case current stress for the active components is summarized in Figure 5-5 for a full load power of 5 kW. The switches M1-M8 along with diodes D7-D8 see the highest current stress at three-stage

low-line single-phase mode of operation. Diodes D1-D6 have the highest current stress in three-phase boost mode of operation. The voltage stress across the active components in both the boost and buck stages is clamped to the intermediate bus voltage and is 800 V.

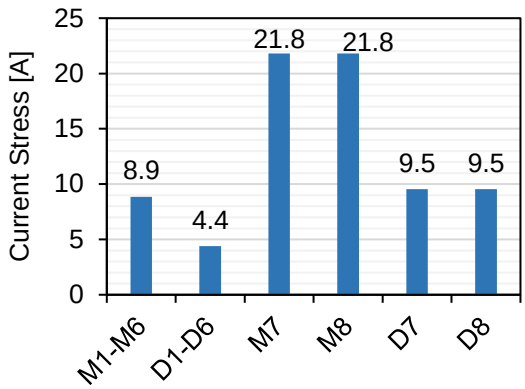


Figure 5-5 Maximum current stress in the active components for the five nominal input voltages analyzed: 120 V and 240 V, 1~, 208 V, 400 V and 480 V 3~

5.4 **Converter control**

The single-phase and three-phase modes of operation and related control are discussed in the following sub-sections.

5.4.1 **Single-phase AC input control**

Average current mode control [58] is used to control the converter illustrated in Figure 5-2. The simplified control block diagram for the three-channel interleaved totem pole PFC is provided in Figure 5-6. An outer voltage loop is used to control the DC bus voltage. The output of the PI controller multiplied by the scaled sampled input voltage provides the sinusoidal current reference for the current loop controllers. The output of the current compensators is applied to the PWM blocks. The PWM registers of the DSP are set in dual slope mode (i.e. triangular carrier) and phases a, b and c are phase shifted by 120° to interleave the three phases. The PWM pulses in each switch leg are complementary and a dead band (DB) of 500 ns was added between the complementary pulses to avoid shoot-through. The slow switches, M7 and M8 provide the return path for the current in the negative and positive half cycles, respectively [55]. A phase lock loop (PLL) block measures the phase angle to control switches M7 and M8.

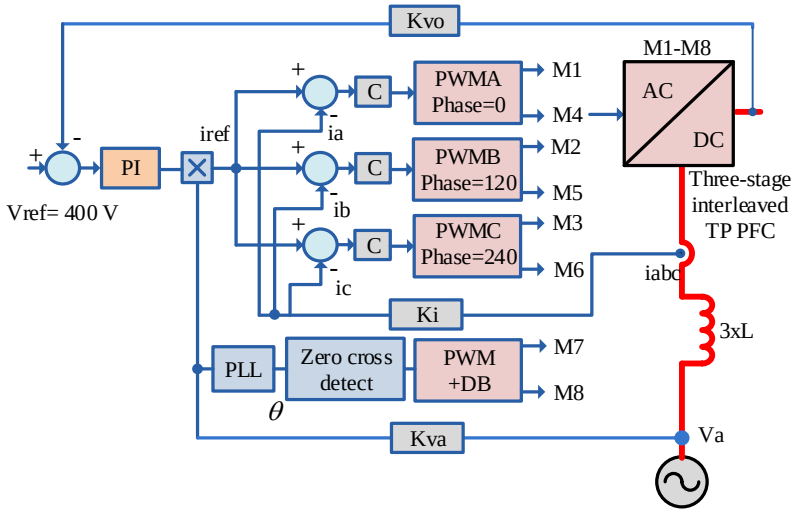


Figure 5-6 Average current mode control block diagram for single-phase AC input three-channel interleaved totem pole PFC

5.4.2 Three-phase AC input Control

The control block diagram for the three-phase AC input mode of operation is the same as Figure 4-5. DQ control and space vector pulse width modulation (SVPWM) are used to run the converter [7], [22]. In order to maximize the efficiency for a universal three-phase AC input cascaded buck follows boost converter with 400 V DC output, the adaptive intermediate bus voltage algorithm proposed in [50] is included in the control block diagram. The second stage buck converter is controlled with voltage mode control for the three-phase boost plus buck mode of operation.

5.4.3 Initialization and adaptive bus control

The simplified operating flow-chart diagram of the truly universal input PFC is shown in Figure 5-7. After general initializations, using the phase voltage information, the firmware determines the input for single-phase or three- phase connection based on the values of line voltages, sets the relays as in Table 5-1 and uses the relevant single-phase or three-phase control as shown in Figure 5-6 and Figure 4-5. The intermediate bus voltage between the boost and buck stages is also adaptively changed to optimize efficiency [50].

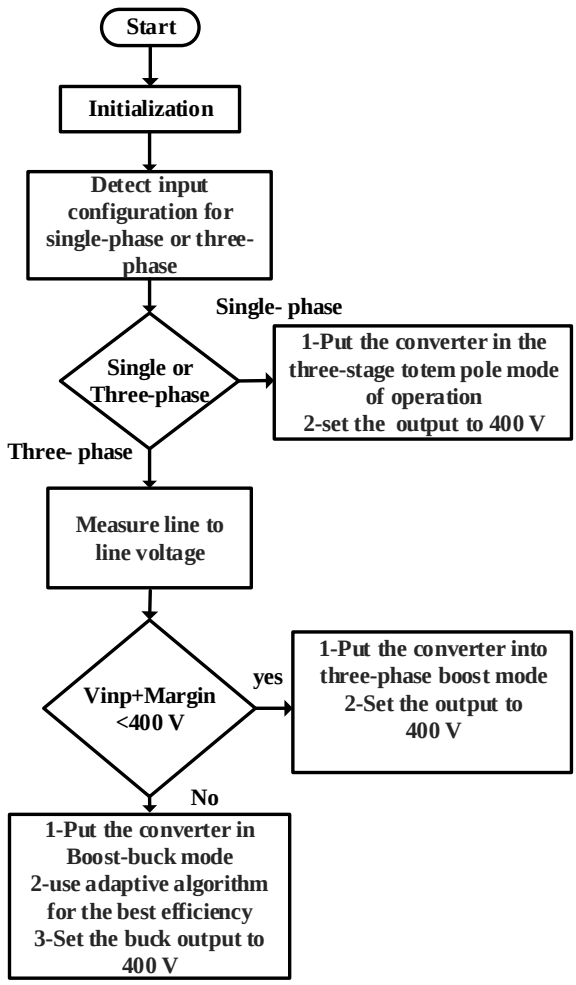


Figure 5-7 Simplified flow chart for truly universal input PFC operation

The conventional solution to maintain PFC regulation for a universal AC input range with the three-phase cascaded buck follows boost converter is to boost the bus voltage to a fixed voltage exceeding the high line peak plus a permissible overvoltage. Thus, at the maximum line input of 480 V, i.e. (480 V) (√2) + 10% = 747 V, is the minimum required bus voltage. Assuming some margin for reliable output regulation, an intermediate bus voltage around 800 V is typically chosen, which is then stepped down to 400 V using the cascaded buck stage. The intermediate bus voltage in the conventional solution and the minimum adaptive operating points to optimize efficiency are illustrated in Figure 4-3. The optimum points (i.e. the adaptive points) are the peak of the line-to-line AC mains voltage plus a margin for reliable regulation as expressed in (4-3), where $\%Margin$ is the regulation margin and may be assumed to be a few percent of input line to line peak voltage for reliable operation.

For input AC mains voltages with a line-to-line peak plus a regulation margin below 400 V, the second stage is bypassed for the best efficiency and the converter operates in three-phase boost mode with RELAY1 and RELAY2 (in Figure 5-3) in the AB position. For AC mains voltages with a line-to-line peak greater than 400 V, the intermediate bus voltage is set equal to (4-3), and the converter operates in three-phase cascaded boost followed by buck operating mode with RELAY1 in the AC position and RELAY2 in AB (in Figure 5-4).

5.4.4 **Loss estimation**

In order to understand the loss distribution among the powertrain components at the extreme operating modes, a worst-case loss estimation was performed to ensure that the design is robust, with sufficient margin in the electrical and thermal sizing of components. PSIM was used to determine the operating condition stresses, e.g. rms currents. Using the component loss parameters provided in Table 5-2 and Mathcad analysis software, a loss estimation was completed for the range of AC mains voltages and operating modes at 5 kW load power. The loss analysis method along with relevant equations is present in [50].

The breakdown of worst-case estimated losses and efficiencies across the range of AC mains voltages is provided in Figure 5-8. It is noted that the efficiencies and the magnitude and distribution of losses are similar in most operating modes, except for single-phase AC input at low-line, i.e. 120 V 1~, where conduction losses in the MOSFETS M1-M6 and inductors La, Lb and Lc are very high. This observation is important as calculations confirm the feasibility of the proposed topology in the sense that sizing components and thermal design for single-phase mode of operation do not need be oversized for three-phase. Accordingly, at single-phase low line, the converter can be limited to operate at partial load if it is desired, or required not to oversize components for three-phase operation. This assumption is reasonable for many typical applications, since in single-phase mode, the on-site AC breaker size and wiring available may be limited to only 20 or 30 A for 120 V, therefore limiting the available input volt-amps and accordingly, the output power to well below 5 kW.

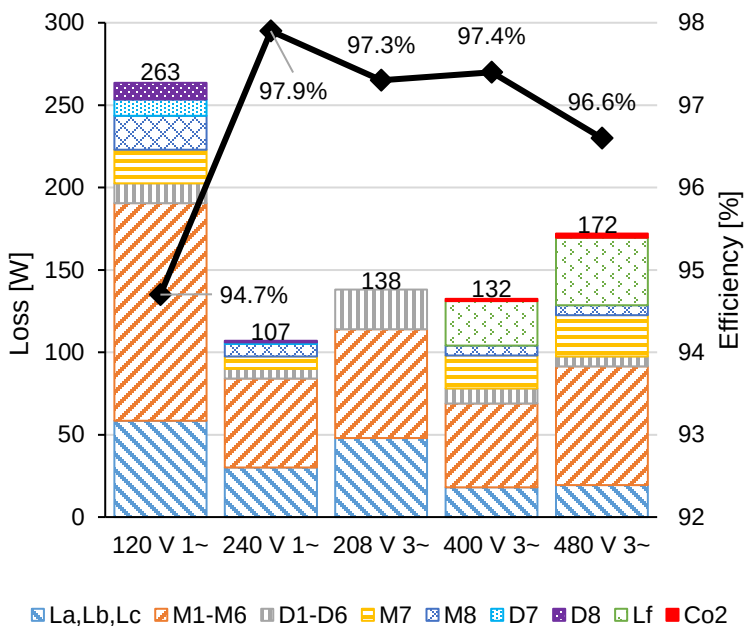


Figure 5-8 Worst-case estimated loss breakdown for the truly universal PFC converter at 5 kW and the following input nominal voltages: single-phase 120 V and 240 V, three-phase 208 V, 400 V, and 480 V

5.4.5 Experimental results

To validate the proposed truly universal input PFC for a 400 V DC output application, a prototype was developed using 1200 V SiC switches with the specifications provided in Table 5-2 and Table 5-3. A sampling/signal conditioning board using a TI Delfino TMS320F28335 DSP was designed and built to implement the control block diagrams provided in Figure 4-5 and Figure 5-6. A photo of the prototype, including powertrain and control, is shown in Figure 5-9. A six channel Cree CGD15FB45P driver was used for driving switches M1-M6. A Cree CRD8FF1217P driver board was used to drive switches M7 and M8.

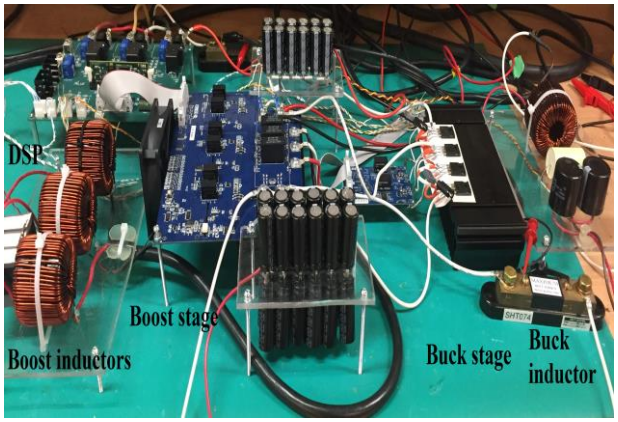


Figure 5-9 truly universal input PFC converter prototype, 5 kW at single-phase 120 V and 240 V, three-phase 208 V, 400 V, and 480 V

Waveforms of one of the input phase currents and the three-phase voltages at the operating mode with highest stress i.e, low-line 208 V are provided for three-phase AC input operation in Figure 5-10. Waveforms of the input current input voltage and output voltage are provided in and Figure 5-11 for the single-phase AC input operating mode with highest current stress i.e, low-line 120 V.

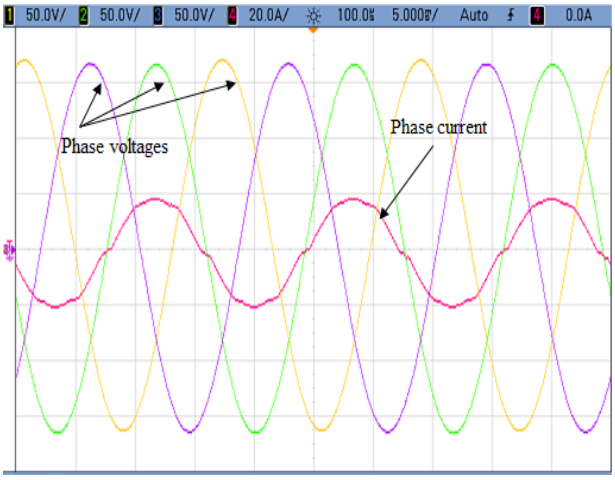


Figure 5-10 Phase voltages and current of phase A waveform for three phase mode of operation at 5 kW and low-line 208 V showing converter operation under the highest stress three-phase condition

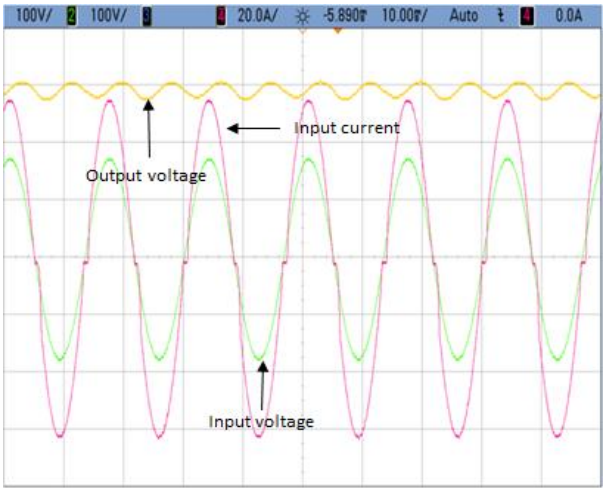


Figure 5-11 Single-phase totem pole PFC mode of operation at 5 kW and 120 V low-line input voltage showing converter operation under the highest single-phase condition.

The measured losses and efficiencies for varying load power are provided in Figure 5-12 and Figure 5-13, respectively. In Figure 5-13, at 5 kW full load, the efficiency results, range from 97.9 to 98.7% for all modes of operation except for low-line 120 V single-phase where it is 96.6%. Therefore, if given a thermal, or loss design constraint, the constraints could be applied without the need for an oversized thermal design, except for low-line where it should operate at partial load, in particular 4 kW or less where the single-phase AC input losses at 120 V input are below those of the other operating modes. In addition, as the current for low-line 120 V and at full-load, exceeds 44 A and the typical available AC breaker and wiring are limited to lower ratings, full-load 5 kW operation at single-phase AC low-line (e.g. in North America) would not likely be used. Moreover, as split-phase 240 V, or two-phase 208 V mains may be available, therefore it would be preferred better to connect the converter to these circuits to minimize input line currents and maximize the converter efficiency.

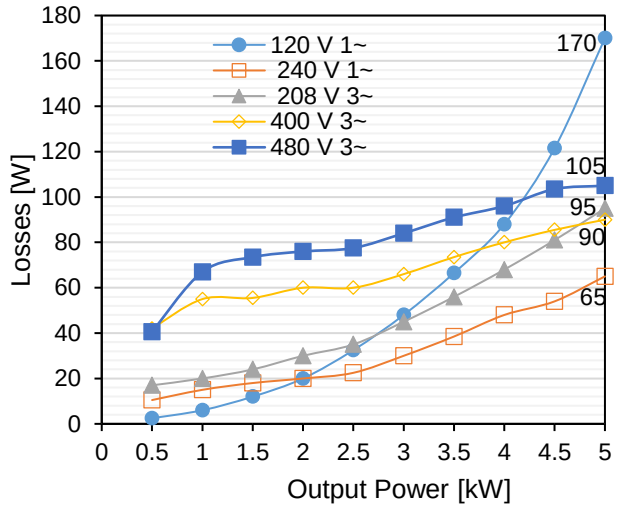


Figure 5-12 Measured power loss vs. output power, at single-phase 120 V and 240 V, three-phase 208 V, 400 V, and 480 V. showing similar losses for most operating modes, except single-phase 120 V

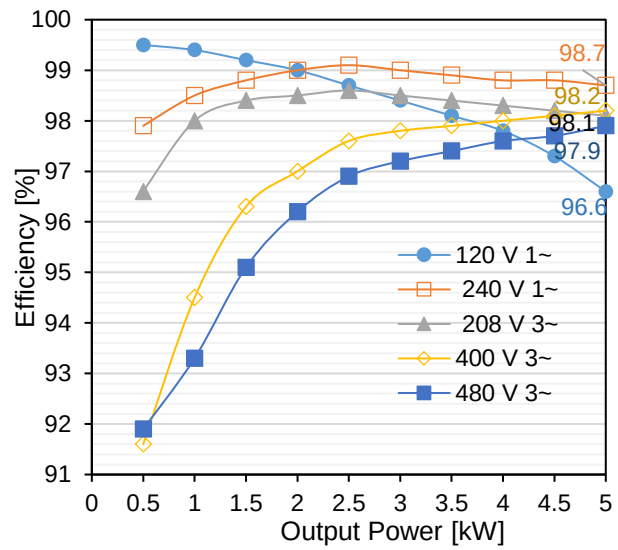


Figure 5-13 Measured efficiency vs. output power, at single-phase 120 V and 240 V, three-phase 208 V, 400 V, and 480 V showing close efficiencies for different modes of operation, except 120 V 1~ low-line

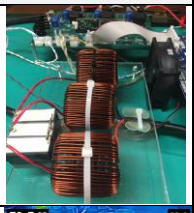
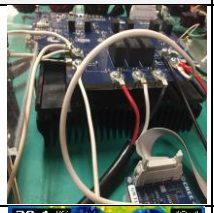
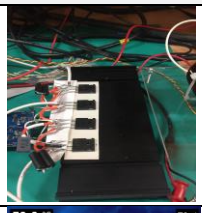
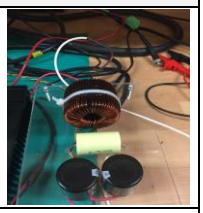
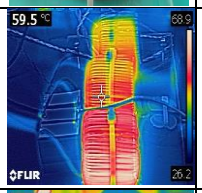
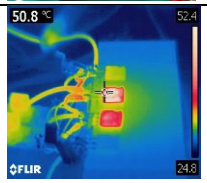
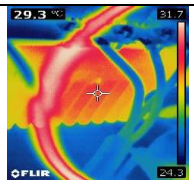
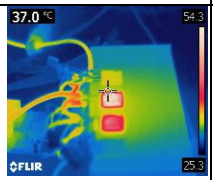
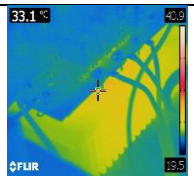
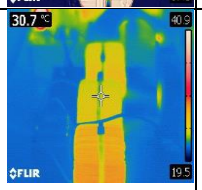
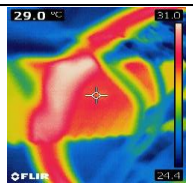
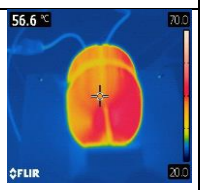
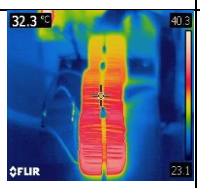
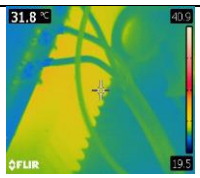
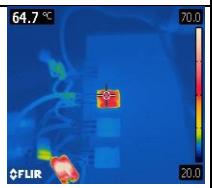
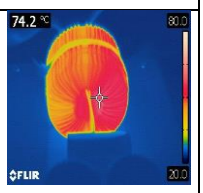
Thermal camera images of the prototype operating at 5 kW for the various AC input modes of operation are provided in Table 5-4. The images provide useful information of the thermal distribution amongst the powertrain components and can also be cross-reference with the loss analysis presented in section 5.4.4 and Figure 5-8.

The boost inductors have the highest temperature at low-line single-phase and three-phase where the current is the highest. This is in agreement with the data in presented Figure 5-8, where at 120 V1~ input, it is noted that the boost PFC inductor losses are high at approximately 58.5 W

total. Aditionally, the temperature of the heat sink, where the six-pack module, i.e. M1-M6, is mounted (third column in Table 5-4), is the highest at 120 V single-phase mode of operation where the losses are the highest, as is supported by the analysis presented in Figure 5-8 ,noting an estimated total loss of 132 W in M1-M6.

The second-stage buck switch M7 and inductor Lf are hottest at 480 V three-phase AC input where the intermediate bus voltage is the highest and so is the voltage stress on buck switch and rms current stress on buck inductor. These results are also supported by the analysis presented in Figure 5-8, which provide estimated losses of 41 W in the buck inductor, Lf and 25 W in the buck switch, M7.

Table 5-4 Thermal images at 400 V output and 5 KW output power

Mode of operation	Boost inductors La, Lb, Lc	Boost switches and diodes M1-M6, D1-D6	Buck/slow leg D7, M7, M8, D8	Buck inductor Lf
				
Three-channel interleaved totem pole PFC, 120 V 1~ input				Bypassed
Three-stage interleaved totem pole PFC, 240 V 1~ input				Bypassed
Three-phase boost, 208 V 3~ input			Bypassed	Bypassed
Three-phase cascaded boost-buck 400 V 3~ input (605 V intermediate boost output)				
Three-phase cascaded boost-buck 480 V 3~ input (726 V intermediate boost output)				

5.5 **Summary**

A novel truly universal AC input power factor correction circuit for application in high-power battery chargers and data centers was proposed that can operate using a 120-240 V single-phase AC input or a 208-480 V three-phase AC input and provide a 400 V DC output at up to 5 kW load power. A worst-case analytical loss estimation was provided indicating the feasibility of design such that the losses for all input operating modes, except low-line 120 V single-phase input, were similar such that the truly universal PFC converter can serve the dual role of operating with a single-phase, or three-phase input. A 5 kW, SiC-based prototype was built and tested to validate the potential of the proposed truly universal architecture. Experimental results were presented with efficiency measurements ranging between 97.9% and 98.7% for all operating modes except for low-line 120 V single-phase input where it was measured to be 96.6%. At 120 V single-phase AC input, the converter can operate at less than 5 kW load if it is assumed that the powertrain components are not overdesigned thermally for higher input voltages. The most significant advantage of the proposed converter architecture is that a single PFC product may be developed that can serve the dual role of a single-phase and three-phase input, i.e. truly universal, PFC circuit with 400 V DC output, thereby significantly reducing development and other costs such as marketing.

Chapter 6: **Conclusions and future work**

6.1 **Conclusions**

Front-end high power AC/DC power factor corrected (PFC) converters are used in applications such as battery chargers and data centers to reduce utility bill surcharges due to poor power factor of uncontrolled rectifiers and also comply with standards limiting the input harmonic content. Efficiency and development cost are two key factors in a high power AC/DC PFC. Higher efficiency lowers the cost of utility bill for consumer while lower development cost makes the product more competitive. This study targeted universal three-phase input 208 V-480 V and 400 V DC output PFC applications with the goal to lower development cost and increase efficiency. Universal input reduces the cost of developing multiple products. 400 V DC output is favorable as it makes the use of 650 V switches possible in the next stage, usually an LLC converter, thus further reducing the development cost and component stress. Based on the above goals, the following three novel contributions were proposed, built and tested.

6.1.1 **Three-phase third harmonic injection SEPIC AC/DC front-end PFC**

A novel single-stage universal input 208 V- 480 V, three-phase third harmonic injection SEPIC AC/DC front-end PFC with 400 V DC output was proposed, analyzed, built and tested and presented in Chapter 3. The loss analysis, benchmarked against six-switch boost plus buck, showed 26 % lower expected losses at low-line input, i.e. 208 V, which is the key operating point to design for thermal management. In addition compared to the benchmark solution, although the same passive component count is used, the cost of silicon (i.e. switches and diodes) is $136 less in the proposed topology.

6.1.2 **Universal input AC three-phase power factor correction with adaptive intermediate bus voltage to optimize efficiency**

An adaptive intermediate bus voltage control method was presented for a universal input, three-phase AC, 400 V DC output, cascaded buck-follows-boost PFC converter. In the proposed method, the optimal intermediate DC bus voltage before the buck converter is set based on the value of input voltage, improving efficiency compared to the conventional solution using a fixed

800 V DC bus voltage. Simulation and loss analysis were presented to illustrate the THD and efficiency benefits of the proposed method. A 5 kW SiC-based prototype was built and experimental results were presented. It was demonstrated experimentally that the two-stage losses could be reduced by up to 61 % (efficiency improvement of 4.4 percentage points at low AC line) with the proposed method. For a practical product design, the proposed approach would enable simplified thermal design, reducing the size of heatsinks and thus the overall cost

6.1.3 A truly universal single and three-phase power factor correction circuit

A novel truly universal AC input power factor correction circuit for application in high-power battery chargers and data centers was proposed that can operate using a 120 V-240 V single-phase AC input or a 208 V-480 V three-phase AC input and provide a 400 V DC output at up to 5 kW load power. A worst-case analytical loss estimation was provided indicating the feasibility of design such that the losses for all input operating modes, except low-line 120 V single-phase input, were similar such that the truly universal PFC converter can serve the dual role of operating with a single-phase, or three-phase input. A 5 kW, SiC-based prototype was built and tested to validate the potential of the proposed truly universal architecture. Experimental results were presented with efficiency measurements ranging between 97.9 % and 98.7 % for all operating modes except for low-line 120 V single-phase input where it was measured to be 96.6 %. At 120 V single-phase AC input, the converter can operate at less than 5 kW load if it is assumed that the powertrain components are not overdesigned thermally for higher input voltages. The most significant advantage of the proposed converter architecture is that a single PFC product may be developed that can serve the dual role of a single-phase and three-phase input, i.e. truly universal, PFC circuit with 400 V DC output, thereby significantly reducing development and other costs such as marketing.

6.1.4 **Comparison summary**

Table 6-1 summarizes the key features of the contributions proposed in Chapters 3-5 compared to the benchmark work presented in Chapter 2.

Table 6-1 Topology feature comparison summary

Chapter	Conversion Mode	Cost	Efficiency Relative to Benchmark (Worst Case)	# AC Supply Phases
Chapter 2: Three-phase buck-follows boost AC/DC PFC (Benchmark)	bi-directional	medium (632 USD)	Benchmark (92.8%)	three
Chapter 3: Three-phase 3rd harmonic injection SEPIC AC/DC PFC	uni-directional	lowest (496 USD)	Higher (93.8%)	three
Chapter 4: Three-phase buck-follows boost AC/DC PFC with adaptive control & Relay system	bi-directional	medium plus one relay	Higher (97%)	three
Chapter 5: Truly universal AC input single & three-phase PFC	bi-directional	medium plus two relays	Higher (97.9%)	one or three

6.2 **Future work**

Possible future work for this study is outlined in this subsection.

6.2.1 **A ZVS three-phase third harmonic injection SEPIC front-end AC/DC PFC**

A possible improvement to the novel topology discussed in this study would be to make it zero voltage switching (ZVS) to improve efficiency.

6.2.2 **An isolated three-phase third harmonic injection SEPIC front-end AC/DC PFC**

Series capacitor in SEPIC topology makes volt-second balancing for this topology possible. Therefore, an isolated version of the proposed topology may be developed which can serve as an isolated AC/DC PFC for EV battery charging applications.

6.2.3 A novel four-legged truly universal input PFC with 400 V DC output

The truly universal single-phase and three-phase high power PFC developed in Chapter 5: used two relays to reconfigure the converter in different single-phase and three-phase modes of operation. Using four totem pole legs, four boost inductors and without the addition of any relays, a truly four-legged universal PFC may be developed that can operate in single-phase (120 V- 240 V) and three-phase modes of operation (208 V- 480 V) with 400 V output. Modulation and control techniques similar to what is already available in the literature for a four-legged inverter may be applied to the truly PFC in three-phase/ four-wire mode of operation. Single-phase three-stage interleaved mode of operation is also already discussed in literature. However, in three-phase/three-wire mode of operation the modulation and control technique along with proper hardware for neutral return path need to be discussed and developed. The performance of control and any necessary modification in case of unbalance of phases also need be discussed for this converter. The other advantage of this truly universal input converter, other than the deletion of relays, is that the bus voltage will not exceed the line-to-neutral voltage making the use of 650 V wide band-gap devices including GaN possible.

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Appendices

Appendix A: **Controller board**

The designed signal sampling /conditioning board in Figure 2-10 contains 5 voltage sampling and 4 current sampling channels.

A.1 **Schematic capture of controller board**

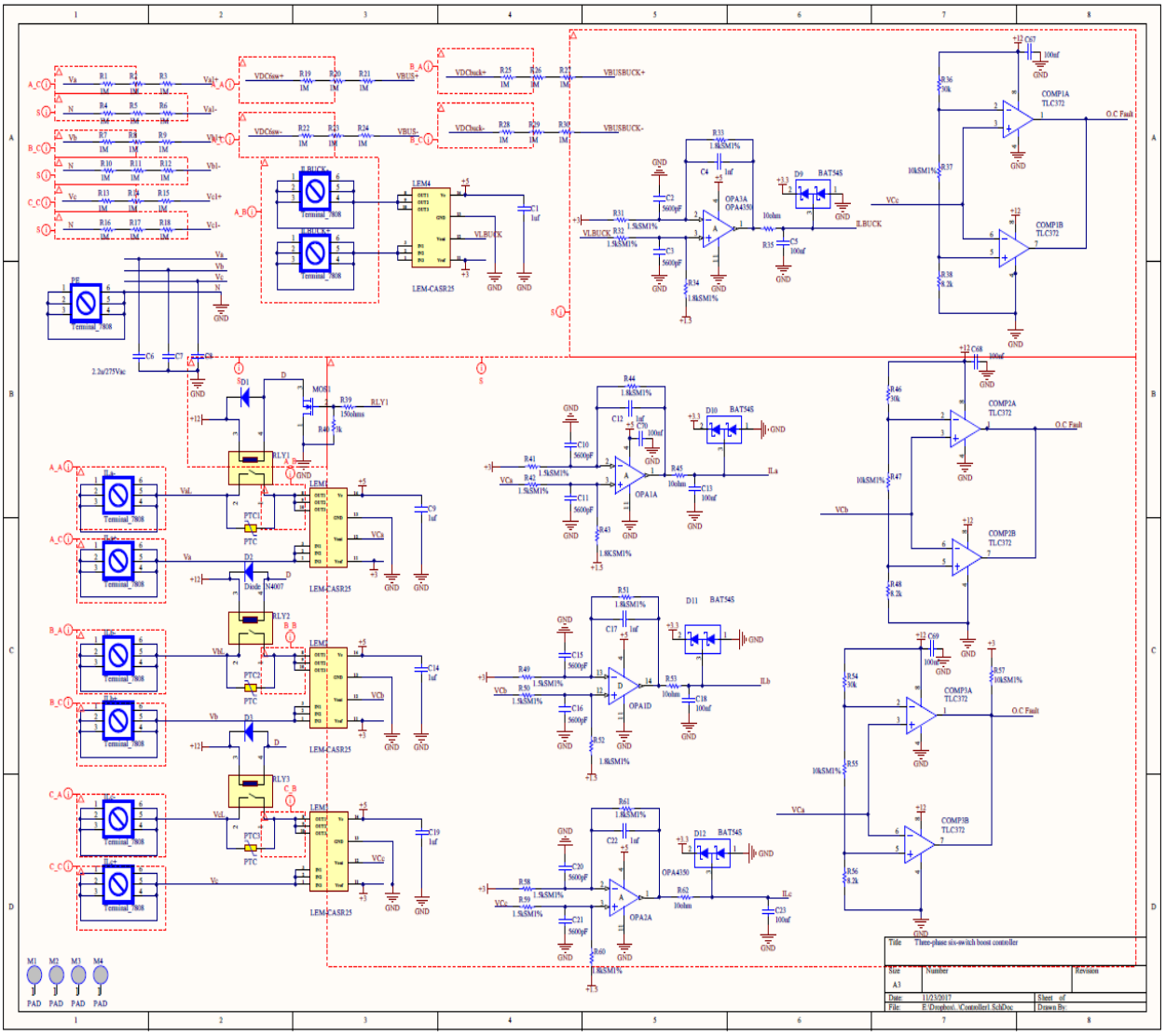

Figure. A-1 Schematic capture of controller board- Page1

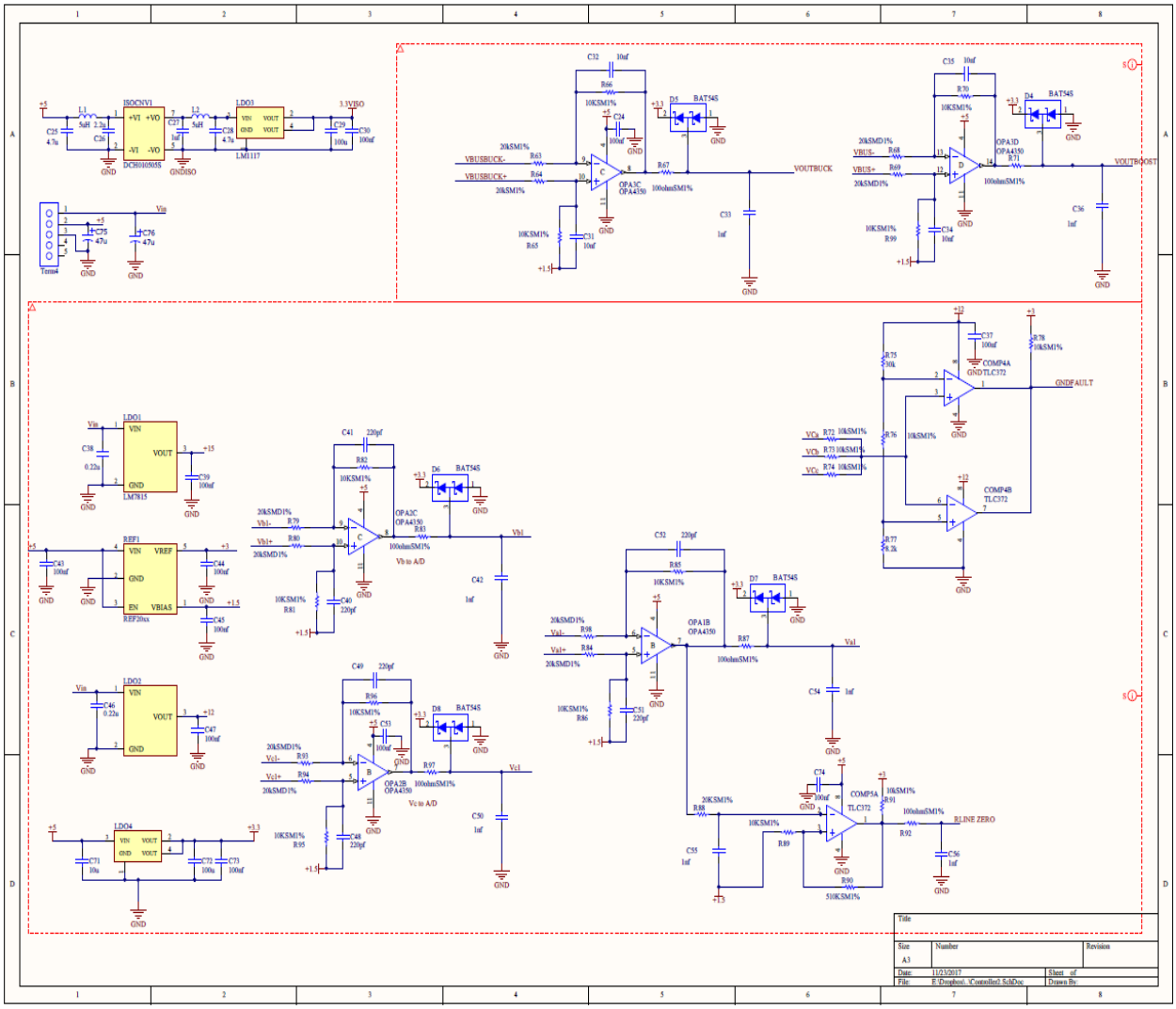

Figure. A-2 Schematic capture of controller board- Page2

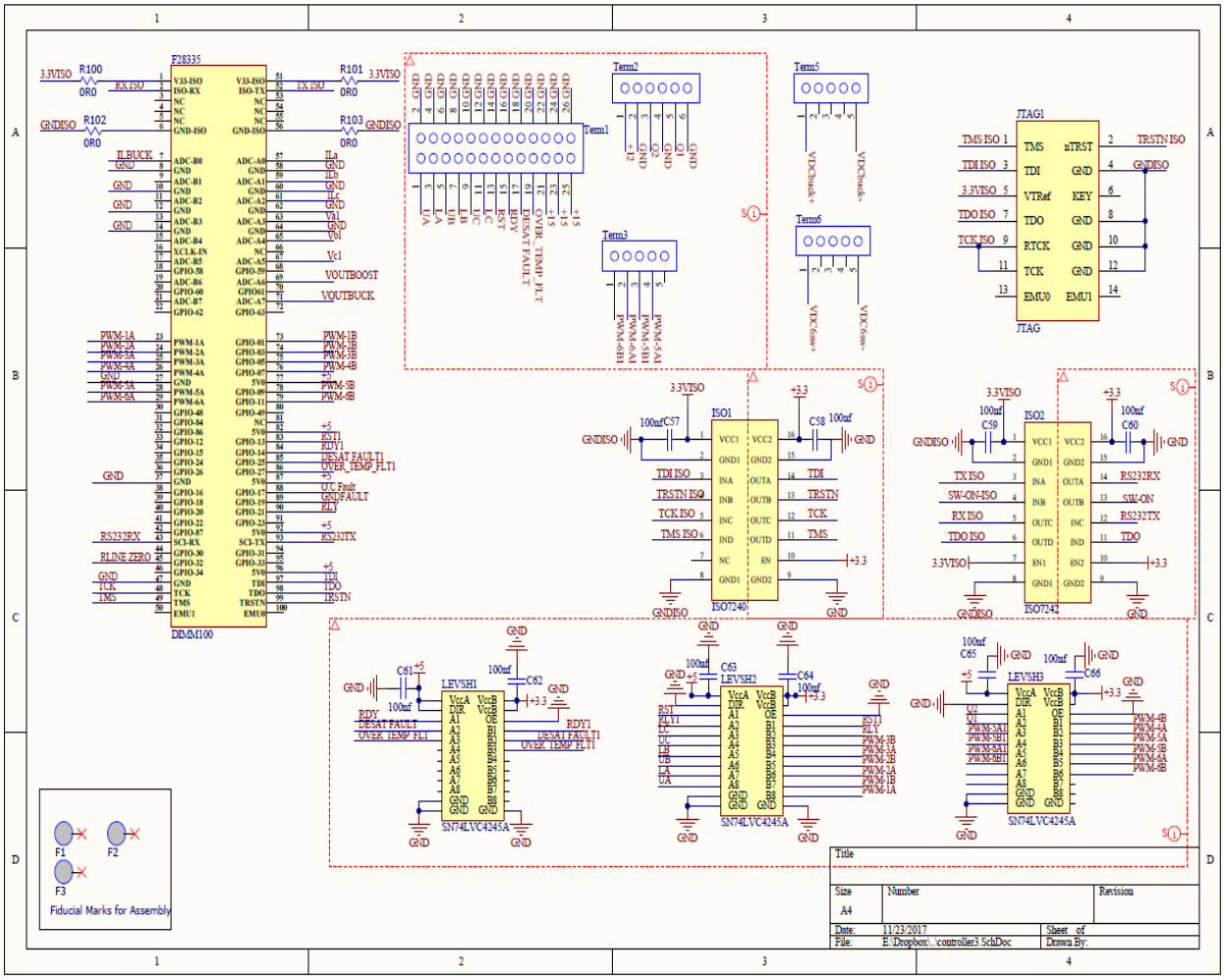

Figure. A-3 Schematic capture of controller board- Page 3

A.2 **Printed circuit capture**

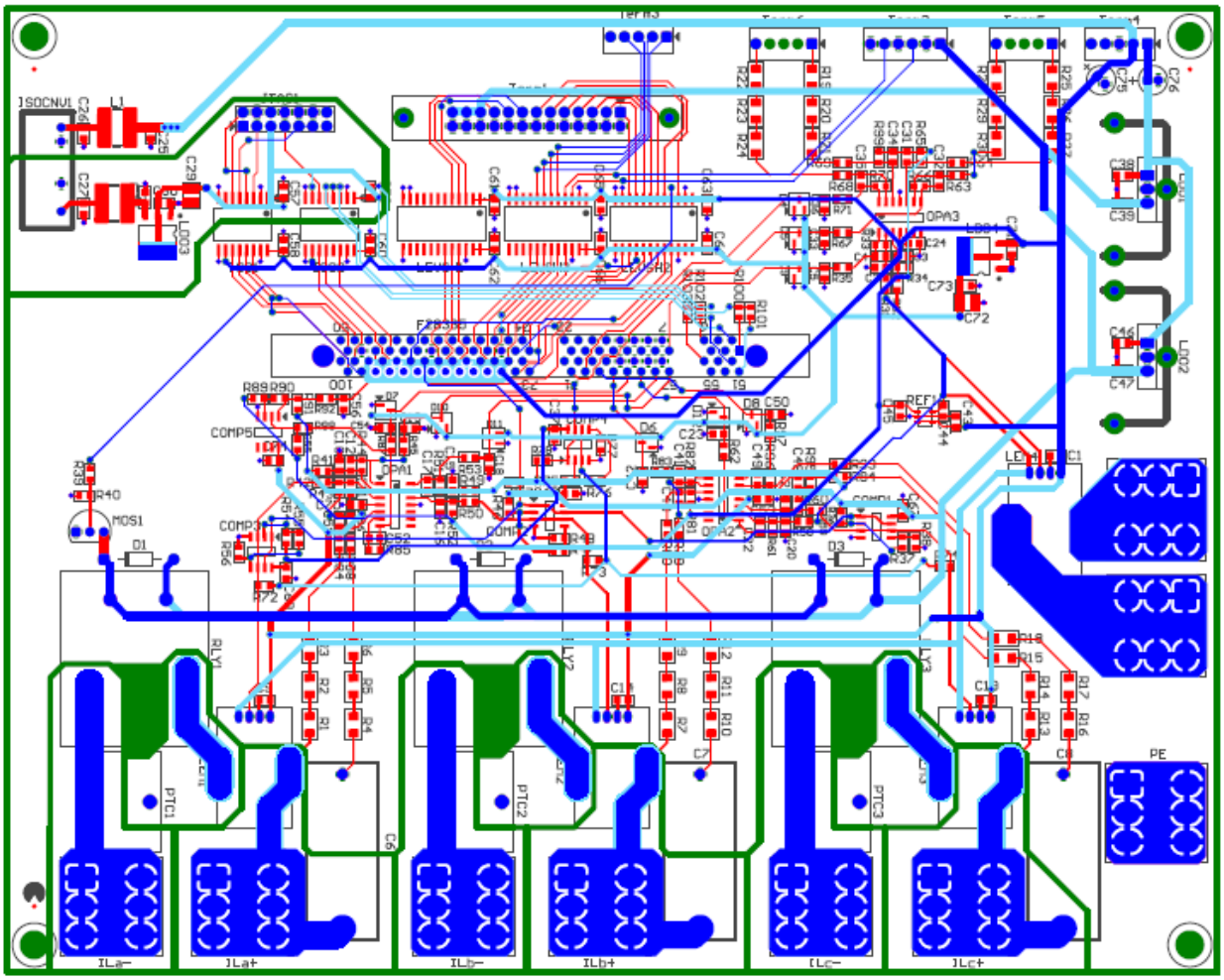

Figure. A-4 Controller four-layer PCB layout

A.3 **Bill of materials**

Table A-1 Controller bill of materials

Comment	Designator	Footprint	Quantity
1 µF	C1,C9,C14,C19,C27	CAPC2012N	5
5600pF	C2,C3,C10,C11,C15,C16,C20,C21	CAPC2012N	8
1nf	C4,C12,C17,C22,C33,C36,C42, C50, C54, C55, C56	CAPC2012N	11
100nf	C5, C13, C18, C23, C24, C30, C37, C39, C43, C44, C45, C47 C53, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C73, C74	CAPC2012N	29
2.2u/275Vac	C6, C7,C8	CAP-32x13mm	3
4.7u	C25,C28	CAPC2012N	2
2.2u	C26	CAPC2012N	1
100u	C29,C72	CAPC3225X125N	2
10nf	C31,C32,C34,C35	CAPC2012N	4
0.22u	C38,C46	CAPC2012N	2
220pf	C40,C41,C48,C49,C51,C52	CAPC2012N	6
10u	C71	CAPC2012N	1
47u	C75,C76	CAPPR2.0-5x11	2
TLC372	COMP1,COMP2,COMP3, COMP4, COMP5	SOIC127P600-8M	5
Diode 1N4007	D1,D2,D3	DO-41	3
BAT54S	D4,D5,D6,D7,D8,D9,D10,D11,D12	SOT23-3N	9
DIMM100	F28335	DIMM1.27-2V100	1
Terminal_7808	ILa-,ILa+,ILb-,ILb+,ILBUCK-, ILBUCK+, ILc-, ILc+, PE	TERM7808	9
ISO7240	ISO1	SOIC127P103016M	1
ISO7242	ISO2	SOIC127P103016M	1
DCH010505S	ISOCNV1	ISOLATED DC/DC	1
JTAG	JTAG1	TERM-JTAG	1
5 µH	L1, L2	INDUCTOR-SMD	2
LM7815	LDO1	TO-220 HEATSINK	1
LM7812	LDO2	TO-220 HEATSINK	1
LM1117	LDO3, LDO4	SOT230P700X175-4M	2
LEM-CASR25	LEM1, LEM2, LEM3, LEM4	LEM	4
SN74LVC4245A	LEVSH1, LEVSH2, LEVSH3	DW024_N	3
Mosfet N	MOS1		1
OPA4350	OPA1, OPA2, OPA3	SOIC127P600-14M	3
PTC	PTC1, PTC2, PTC3	PTC	3

1M	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13,R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30	RESC3216M	30
1.5kSM1%	R31, R32, R41, R42, R49, R50 , R58, R59	RESC2012N	8
1.8kSM1%	R33, R34, R43, R44, R51, R52, R60, R61	RESC2012N	8
10ohm	R35, R45, R53, R62	RESC2012N	4
30k	R36, R46, R54, R75	RESC2012N	4
10kSM1%	R37, R47, R55, R57, R65, R66, R70, R72, R73, R74,R76, R78, R81, R82, R85, R86, R89, R91, R95, R96, R99	RESC2012N	21
8.2k	R38, R48, R56, R77	RESC2012N	4
150ohms	R39	RESC2012N	1
3k	R40	RESC2012N	1
20kSM1%	R63, R64, R88	RESC2012N	3
100ohmSM1%	R67, R71, R83, R87, R92, R97	RESC2012N	6
20kSMD1%	R68, R69, R79, R80, R84, R93, R94, R98	RESC2012N	8
510KSM1%	R90	RESC2012N	1
0R0	R100, R101, R102, R103	RESC2012N	4
REF20xx	REF1		1
RLY-G8P-1A4P	RLY1, RLY2, RLY3	RLY	3
Terminal-26pin	Term1	TERM26PIN	1
Terminal_molex_6PIN	Term2	TERM6PIN	1
Terminal_molex_5 pin	Term3, Term4, Term5, Term6	TERM5PIN	4

Appendix B: **Loss estimation Mathcad file**

Efficiency worksheet for two-stage three-phase boost+buck topology 800vDC/5kw

A) Buck converter
A-1 Conduction losses

$T_j := 125\ \Delta°C$

$R_{DS\_125c} := 0.043\ \Omega$ Diode:C4D20120D

$V_T := 0.98\ V - T_j \cdot 1.71 \cdot 10^{-3}\ \frac{V}{\Delta°C} = 0.766\ V$ MOSFET:C2M0025120D

$R_T := 0.040\ \Omega + T_j \cdot 5.32 \cdot 10^{-4}\ \frac{\Omega}{\Delta°C} = 0.107\ \Omega$

$I_{sw\_rms} := 9.65\ A$

$I_{D\_avg} := 6.19\ A$

$I_{D\_rms} := 8.91\ A$

$P_{D\_cond} := V_T \cdot \frac{I_{D\_avg}}{2} + R_T \cdot \frac{I_{D\_rms}^2}{4} = 4.485\ W$ Every diode package has two legs

$P_{D\_cond\_sync} := R_{DS\_125c} \cdot I_{D\_rms}^2 = 3.414\ W$

$P_{sw\_cond} := R_{DS\_125c} \cdot I_{sw\_rms}^2 = 4.004\ W$

$P_{conduction\_total\_without\_sync} := 2 \cdot P_{D\_cond} + P_{sw\_cond} = 12.975\ W$

$P_{conduction\_total\_after\_sync} := P_{D\_cond\_sync} + P_{sw\_cond} = 7.418\ W$

A-2 switching losses

$f_s := 50\ KHz$

$I_{DSon} := 0\ A$

$I_{DSoff} := 6\ A$ IDS(turn-on)=0A

$E_{ON} := 0.208 \cdot 10^{-3}\ J$

$K1 := \frac{0.75}{0.5}$ IDS(turn-off)=6A

$E_{ON} := K1 \cdot E_{ON}$ Rext(on)=10, Rext(off)=5 use scale factor for Eon

$E_{off} := 0.167 \cdot 10^{-3}\ J$

$P_{sw\_switching} := f_s \cdot \langle E_{ON} + E_{off} \rangle = 23.95\ W$

$Q_c := 52\ nC$

$V_o := 800\ V$

$P_{D\_switching} := Q_c \cdot V_o \cdot f_s = 2.08\ W$

$P_{switching} := P_{sw\_switching} + P_{D\_switching} = 26.03\ W$

A-3 Total Active loss

$P_{loss\_total\_active} := P_{conduction\_total\_without\_sync} + P_{switching} = 39.005\ W$

$P_{loss\_total\_active\_sync} := P_{conduction\_total\_after\_sync} + P_{switching} = 33.448\ W$

A-4 Passive losses

A-5 inductor losses

Core loss calculation

$N := 56$

$l_e := 14.4\ cm$

$I_{DC} := 12.5\ A$

$\Delta I := 8\ A$

$H_{ACmax} := \frac{N}{l_e} \cdot \left(I_{DC} + \frac{\Delta I}{2}\right) = 64.167\ \frac{A}{cm}$

$H_{ACmin} := \frac{N}{l_e} \cdot \left(I_{DC} - \frac{\Delta I}{2}\right) = 33.056\ \frac{A}{cm}$

$a := 1.658\ 10^{-4}$

$b := 2.301\ 10^{-5}\ \frac{cm}{A}$

$c := 7.297\ 10^{-5}\ \frac{cm^2}{A^2}$

$e := 6.053 \cdot 10^{-5}\ \frac{cm^2}{A^2}$

$d := 5.906\ 10^{-3}\ \frac{cm}{A}$

$X := 0.5$

$H := H_{ACmin}$

$B_{min} := \left(\frac{a + b \cdot H + c \cdot H^2}{1 + d \cdot H + e \cdot H^2}\right)^X\ T = 0.253\ T$

$H := H_{ACmax}$

$B_{max} := \left(\frac{a + b \cdot H + c \cdot H^2}{1 + d \cdot H + e \cdot H^2}\right)^X\ T = 0.431\ T$

$B_{pk} := \frac{1}{2} \cdot (B_{max} - B_{min}) = 0.089\ T$

$P_L := 193\ \frac{mW}{cm^3} \cdot \left(B_{pk} \cdot \frac{1}{T}\right)^{2.01} \cdot \left(\frac{f_s}{1000} \cdot s\right)^{1.29} = 231.649\ \frac{mW}{cm^3}$

$V_e := 3 \cdot 51.8\ cm^3 = 155.4\ cm^3$

$P_{core\_loss\_buck} := P_L \cdot V_e = 35.998\ W$ Three KOOLMu 77617 cores stacked

Copper loss

$C := 25.91\ mm$

$A := 62.91\ mm$

$B := 31.69\ mm$ Core dimensions

$N := 54$

$l_W := N \cdot (6 \cdot C + (A - B)) = 10.081\ m$ Three cores stacked

$R_{per\_meter\_14\_AWG} := 0.00828\ \frac{\Omega}{m}$

$R_{DC} := l_W \cdot R_{per\_meter\_14\_AWG} = 0.083\ \Omega$

$E_{ON1}(\theta) := -8.5 \cdot 10^{-5} \cdot (I_{DSon}(\theta))^2 + 0.013457 \cdot I_{DSon}(\theta) + 0.25086$

$E_{ON}(\theta) := K \cdot E_{ON1}(\theta)$

$E_{off}(\theta) := 0.067$

$$P_{sw\_Mosfet} := \left| \begin{array}{l} f_s \leftarrow 50000 \\ \theta \leftarrow 0 \\ \text{for } i \in 0 .. \frac{f_s}{120} - 1 \\ \quad E \leftarrow E + E_{ON}(\theta) + E_{off}(\theta) \\ \quad \theta \leftarrow \theta + \frac{120 \cdot \pi}{f_s} \\ \quad E \cdot \frac{60}{1000} \ W \end{array} \right. = 17.023 \ W$$

$P_{Active\_boost\_total\_208l\_1} := (P_{Cond} + P_{sw\_Mosfet}) \cdot 6 = 188.598 \ W$

$P_{Active\_total\_Buck\_plus\_boost\_208} := P_{Active\_boost\_total\_208l\_1} + P_{loss\_total\_active} = 227.603 \ W$

For Vin=400[v] and Vout=800[v] P=1[kw]

$I_{Davg} := 0.9 \ A$

$I_{Drms} := 1.76 \ A$

$I_{Mos\_avg} := 1.3 \ A$

$R_{DS\_125} := 0.2 \ \Omega$

$I_{Mos\_rms} := 3.8 \ A$

$V_D := 0.75 \ V$

$R_D := 0.12 \ \Omega$

$P_{Cond} := R_{DS\_125} \cdot I_{Mos\_rms}^2 + R_D \cdot I_{Drms}^2 + V_D \cdot I_{Davg} = 3.935 \ W$

$\theta := 0$

$I_{DSon}(\theta) := (9.5) \cdot \sin(\theta)$

$I_{DSoff}(\theta) := (11.5) \cdot \sin(\theta)$

$E_{ON1}(\theta) := -8.5 \cdot 10^{-5} \cdot (I_{DSon}(\theta))^2 + 0.013457 \cdot I_{DSon}(\theta) + 0.25086$

$E_{off}(\theta) := 0.067$

$E_{ON}(\theta) := K \cdot E_{ON1}(\theta)$

$E_{off}(\theta) := 0.067$

$$P_{sw\_Mosfet} := \left| \begin{array}{l} f_s \leftarrow 50000 \\ \theta \leftarrow 0 \\ \text{for } i \in 0 .. \frac{f_s}{120} - 1 \\ \quad E \leftarrow E + E_{ON}(\theta) + E_{off}(\theta) \\ \quad \theta \leftarrow \theta + \frac{120 \cdot \pi}{f_s} \\ \quad E \cdot \frac{60}{1000} \ W \end{array} \right. = 14.383 \ W$$

$P_{Active\_boost\_total\_400l\_l} := \left(P_{Cond} + P_{sw\_Mosfet}\right) \cdot 6 = 109.904\ W$

$P_{Active\_total\_Buck\_plus\_boost\_400} := P_{Active\_boost\_total\_400l\_l} + P_{loss\_total\_active} = 148.909\ W$

For Vin=480[v] and Vout=800[v] P=1[kw]

$I_{Davg} := 0.62\ A$

$I_{Drms} := 1.25\ A$

$R_{DS\_125} := 0.2\ \Omega$

$I_{Mos\_avg} := 1.4\ A$

$I_{Mos\_rms} := 3.3\ A$

$V_D := 0.75\ V$

$R_D := 0.12\ \Omega$

$P_{Cond} := R_{DS\_125} \cdot I_{Mos\_rms}^{\ 2} + R_D \cdot I_{Drms}^{\ 2} + V_D \cdot I_{Davg} = 2.831\ W$

$\theta := 0$

$I_{DSon}(\theta) := (8) \cdot \sin(\theta)$

$I_{DSoff}(\theta) := (9.5) \cdot \sin(\theta)$

$E_{ON1}(\theta) := -8.5 \cdot 10^{-5} \cdot \left(I_{DSon}(\theta)\right)^2 + 0.013457 \cdot I_{DSon}(\theta) + 0.25086$

$E_{off}(\theta) := 0.067$

$E_{ON}(\theta) := K \cdot E_{ON1}(\theta)$

$E_{off}(\theta) := 0.067$

$$P_{sw\_Mosfet} := \left| \begin{array}{l} f_s \leftarrow 50000 \\ \theta \leftarrow 0 \\ \text{for } i \in 0 .. \dfrac{f_s}{120} - 1 \\ \quad E \leftarrow E + E_{ON}(\theta) + E_{off}(\theta) \\ \quad \theta \leftarrow \theta + \dfrac{120 \cdot \pi}{f_s} \\ \quad E \cdot \dfrac{60}{1000}\ W \end{array} \right. = 13.928\ W$$

$P_{Active\_boost\_total\_480l\_l} := \left(P_{Cond} + P_{sw\_Mosfet}\right) \cdot 6 = 100.55\ W$

$P_{Active\_total\_Buck\_plus\_boost\_480} := P_{Active\_boost\_total\_480l\_l} + P_{loss\_total\_active} = 139.555\ W$

B-2) Passive losses Vin=208[v] , Vo=800[v] , P=5[kw]

Inductor losses

1-1) Core losses (core 77191A7)

$N := 66$

$l_e := 12.5\ cm$

$I_{min}(\theta) := 18.75 \cdot \sin(\theta)\ A$

$I_{max}(\theta) := 21.25 \cdot \sin(\theta)\ A$

$$H_{ACmax}(\theta) := \frac{N}{l_e} \cdot |I_{max}(\theta)|$$

$$H_{ACmin}(\theta) := \frac{N}{l_e} \cdot |I_{min}(\theta)|$$

$a := 5.868\ 10^{-5}$

$b := 9.362\ 10^{-5}\ \frac{cm}{A}$

$c := 9.011\ 10^{-6}\ \frac{cm^2}{A^2}$

$d := -3.682\ 10^{-4}\ \frac{cm}{A}$

$e := 8.747 \cdot 10^{-6}\ \frac{cm^2}{A^2}$

$X := 0.5$

$$B_{min}(\theta) := \left| \frac{a + b \cdot H_{ACmin}(\theta) + c \cdot \left(H_{ACmin}(\theta)\right)^2}{1 + d \cdot H_{ACmin}(\theta) + e \cdot \left(H_{ACmin}(\theta)\right)^2} \right|^X T$$

$$B_{max}(\theta) := \left| \frac{a + b \cdot H_{ACmax}(\theta) + c \cdot \left(H_{ACmax}(\theta)\right)^2}{1 + d \cdot H_{ACmax}(\theta) + e \cdot \left(H_{ACmax}(\theta)\right)^2} \right|^X T$$

$$B_{pk}(\theta) := \frac{1}{2} \cdot \left(B_{max}(\theta) - B_{min}(\theta)\right)$$

$$P_{core\_boost\_208l\_l} := \left\| \begin{array}{l} \theta \leftarrow 0 \\ f_s \leftarrow 50000 \\ f_m \leftarrow 60 \\ P_L \leftarrow 0 \\ \text{for } k \in 0 .. \frac{f_s}{f_m} - 1 \\ \quad \theta \leftarrow \theta + 2 \cdot \frac{\pi}{f_s} \cdot f_m \\ \quad P_L \leftarrow P_L + 120\ \frac{mW}{cm^3} \cdot \left(\left|B_{pk}(\theta)\right| \cdot \frac{1}{T}\right)^{2.09} \cdot \left(\frac{f_s}{1000}\right)^{1.46} \\ f_m \cdot \frac{P_L}{f_s} \end{array} \right. = 4.189\ \frac{mW}{cm^3}$$

$V_e := 28.6\ cm^3$

$n_{stacked\_cores} := 3$

$P_{core\_loss\_total\_208l\_l} := n_{stacked\_cores} \cdot V_e \cdot P_{core\_boost\_208l\_l} = 0.359\ W$

1-2) Vin=400v ,Vo=800v, P=5kw

$I_{min}(\theta) := 9.5 \cdot \sin(\theta)\ A$

$I_{max}(\theta) := 11.5 \cdot \sin(\theta)\ A$

$H_{ACmax}(\theta) := \frac{N}{l_e} \cdot |I_{max}(\theta)|$

$H_{ACmin}(\theta) := \frac{N}{l_e} \cdot |I_{min}(\theta)|$

$a := 5.868\ 10^{-5}$

$b := 9.362\ 10^{-5}\ \frac{cm}{A}$

$c := 9.011\ 10^{-6}\ \frac{cm^2}{A^2}$

$d := -3.682\ 10^{-4}\ \frac{cm}{A}$

$X := 0.5$

$e := 8.747 \cdot 10^{-6}\ \frac{cm^2}{A^2}$

$$B_{min}(\theta) := \left| \frac{a + b \cdot H_{ACmin}(\theta) + c \cdot H_{ACmin}(\theta)^2}{1 + d \cdot H_{ACmin}(\theta) + e \cdot H_{ACmin}(\theta)^2} \right|^X T$$

$$B_{max}(\theta) := \left| \frac{a + b \cdot H_{ACmax}(\theta) + c \cdot H_{ACmax}(\theta)^2}{1 + d \cdot H_{ACmax}(\theta) + e \cdot H_{ACmax}(\theta)^2} \right|^X T$$

$$B_{pk}(\theta) := \frac{1}{2} \cdot \langle B_{max}(\theta) - B_{min}(\theta) \rangle$$

$$P_{core\_boost\_400l\_l} := \left| \begin{array}{l} \theta \leftarrow 0 \\ f_s \leftarrow 50000 \\ f_m \leftarrow 60 \\ P_L \leftarrow 0 \\ \text{for } k \in 0 .. \frac{f_s}{f_m} - 1 \\ \quad \left| \begin{array}{l} \theta \leftarrow \theta + 2 \cdot \frac{\pi}{f_s} \cdot f_m \\ P_L \leftarrow P_L + 120\ \frac{mW}{cm^3} \cdot \left(|B_{pk}(\theta)| \cdot \frac{1}{T} \right)^{2.09} \cdot \left(\frac{f_s}{1000} \right)^{1.46} \end{array} \right. \\ f_m \cdot \frac{P_L}{f_s} \end{array} \right. = 3.024\ \frac{mW}{cm^3}$$

$V_e := 28.6\ cm^3$

$n_{stacked\_cores} := 3$

$P_{core\_loss\_total\_400l\_l} := n_{stacked\_cores} \cdot V_e \cdot P_{core\_boost\_400l\_l} = 0.259\ W$

1-3) Vin=480 , V0=800, P=1kw

$I_{min}(\theta) := 8 \cdot \sin(\theta)\ A$

$I_{max}(\theta) := 9.5 \cdot \sin(\theta)\ A$

$H_{ACmax}(\theta) := \frac{N}{l_e} \cdot |I_{max}(\theta)|$

$H_{ACmin}(\theta) := \frac{N}{l_e} \cdot |I_{min}(\theta)|$

$a := 5.868\ 10^{-5}$

$b := 9.362\ 10^{-5}\ \frac{cm}{A}$

$c := 9.011\ 10^{-6}\ \frac{cm^2}{A^2}$

$d := -3.682\ 10^{-4}\ \frac{cm}{A}$

$e := 8.747 \cdot 10^{-6}\ \frac{cm^2}{A^2}$

$X := 0.5$

$$B_{min}(\theta) := \left(\frac{a + b \cdot H_{ACmin}(\theta) + c \cdot H_{ACmin}(\theta)^2}{1 + d \cdot H_{ACmin}(\theta) + e \cdot H_{ACmin}(\theta)^2}\right)^X T \qquad B_{max}(\theta) := \left(\frac{a + b \cdot H_{ACmax}(\theta) + c \cdot H_{ACmax}(\theta)^2}{1 + d \cdot H_{ACmax}(\theta) + e \cdot H_{ACmax}(\theta)^2}\right)^X T$$

$$B_{pk}(\theta) := \frac{1}{2} \cdot \langle B_{max}(\theta) - B_{min}(\theta) \rangle$$

$$P_{core\_boost\_480l\_l} := \left| \begin{array}{l} \theta \leftarrow 0 \\ f_s \leftarrow 50000 \\ f_m \leftarrow 60 \\ P_L \leftarrow 0 \\ \text{for } k \in 0 .. \frac{f_s}{f_m} - 1 \\ \quad \theta \leftarrow \theta + 2 \cdot \frac{\pi}{f_s} \cdot f_m \\ \quad P_L \leftarrow P_L + 120\ \frac{mW}{cm^3} \cdot \left(|B_{pk}(\theta)| \cdot \frac{1}{T}\right)^{2.09} \cdot \left(\frac{f_s}{1000}\right)^{1.46} \\ f_m \cdot \frac{P_L}{f_s} \end{array} \right. = 1.687\ \frac{mW}{cm^3}$$

$V_e := 28.6\ cm^3$

$n_{stacked\_cores} := 3$

$P_{core\_loss\_total\_480l\_l} := n_{stacked\_cores} \cdot V_e \cdot P_{core\_boost\_480l\_l} = 0.145\ W$

2)copper losses

2-1) For Vin=208 and Vo=800

$R_{DC} := 0.078\ \Omega$

$R_{ac} := 5.4\ \Omega$

$I_{rms} := 14.53\ A$

$I_{60Hz\_rms} := 14.51\ A$

$I_{50KHz} := 0.76\ A$

$P_{copper\_loss\_boost\_inductor\_208l\_l} := R_{DC} \cdot I_{60Hz\_rms}^2 + R_{ac} \cdot I_{50KHz}^2 = 19.541\ W$

2-2) For Vin=400 and Vo=800

$I_{rms} := 7.49\ A$

$I_{60Hz\_rms} := 7.46\ A$

$I_{50KHz} := 0.67\ A$

$P_{copper\_loss\_boost\_inductor\_400l\_l} := R_{DC} \cdot I_{60Hz\_rms}^2 + R_{ac} \cdot I_{50KHz}^2 = 6.765\ W$

2-3) For Vin=480v and Vo=800v

$I_{rms} := 6.24\ A$

$I_{60Hz\_rms} := 6.182\ A$

$I_{50KHz} := 0.85\ A$

$P_{copper\_loss\_boost\_inductor\_480l\_l} := R_{DC} \cdot I_{60Hz\_rms}^2 + R_{ac} \cdot I_{50KHz}^2 = 6.882\ W$

Total inductor loss 208L-L

$P_{total\_boost\_inductor\_208l\_l} := P_{core\_loss\_total\_208l\_l} + P_{copper\_loss\_boost\_inductor\_208l\_l} = 19.901\ W$

Total inductor loss 400L-L

$P_{total\_boost\_inductor\_400l\_l} := P_{core\_loss\_total\_400l\_l} + P_{copper\_loss\_boost\_inductor\_400l\_l} = 7.024\ W$

Total inductor loss 480L-L

$P_{total\_boost\_inductor\_480l\_l} := P_{core\_loss\_total\_480l\_l} + P_{copper\_loss\_boost\_inductor\_480l\_l} = 7.027\ W$

C) Output capacitor loss (Co=1350uf)

Two banks of capacitors each 18 *470uf in parallel ESR=2.76mohm each

$ESR := 3.07 \cdot 10^{-4}\ \Omega$

$I_{crms\_480l\_l} := 7.44\ A$

$I_{crms\_208l\_l} := 11.57\ A$

$I_{crms\_400l\_l} := 8.13\ A$

$P_{outcap\_boost\_208l\_l} := ESR \cdot I_{crms\_208l\_l}^2 = 0.041\ W$

$P_{outcap\_boost\_400l\_1} := ESR \cdot I_{crms\_400l\_1}^{2} = 0.02\ W$

$P_{outcap\_boost\_480l\_1} := ESR \cdot I_{crms\_480l\_1}^{2} = 0.017\ W$

Total passive loss boost 208v

$P_{total\_passive\_boost\_208l\_1} := P_{outcap\_boost\_208l\_1} + 3 \cdot P_{total\_boost\_inductor\_208l\_1} = 59.743\ W$

Total passive loss boost 400v

$P_{total\_passive\_boost\_400l\_1} := P_{outcap\_boost\_400l\_1} + 3 \cdot P_{total\_boost\_inductor\_400l\_1} = 21.093\ W$

Total passive loss boost 480v

$P_{total\_passive\_boost\_480l\_1} := P_{outcap\_boost\_480l\_1} + 3 \cdot P_{total\_boost\_inductor\_480l\_1} = 21.099\ W$

Total passive loss boost+buck 208v

$P_{total\_passive\_208l\_1} := P_{total\_passive\_boost\_208l\_1} + P_{loss\_passive\_buck} = 112.665\ W$

Total passive loss boost+buck 400v

$P_{total\_passive\_400l\_1} := P_{total\_passive\_boost\_400l\_1} + P_{loss\_passive\_buck} = 74.015\ W$

Total passive loss boost+buck 480v

$P_{total\_passive\_480l\_1} := P_{total\_passive\_boost\_480l\_1} + P_{loss\_passive\_buck} = 74.02\ W$

Total loss boost+buck 208 V

$P_{total\_208} := P_{total\_passive\_208l\_1} + P_{Active\_total\_Buck\_plus\_boost\_208} = 340.268\ W$

Total loss boost+buck 400 V

$P_{total\_400} := P_{total\_passive\_400l\_1} + P_{Active\_total\_Buck\_plus\_boost\_400} = 222.924\ W$

Total loss boost+buck 480 V

$P_{total\_480} := P_{total\_passive\_480l\_1} + P_{Active\_total\_Buck\_plus\_boost\_480} = 213.576\ W$

Total efficiency boost+buck 208 V

$$Eff_{208V} := \frac{\left(5000\ W - P_{total\_208}\right)}{5000\ W} \cdot 100 = 93.2$$

Total efficiency boos+buck 400 V

$$Eff_{208V} := \frac{\left(5000\ W - P_{total\_400}\right)}{5000\ W} \cdot 100 = 96$$

Total efficiency boos+buck 480 V

$$Eff_{208V} := \frac{\left(5000\ W - P_{total\_480}\right)}{5000\ W} \cdot 100 = 95.7$$

$\rho := 1.68 \cdot 10^{-8}\ \Omega \cdot m$

$\mu := 4 \cdot \pi \cdot 10^{-7}\ \frac{N}{A^2}$

$D_{pen} := \sqrt{\frac{\rho}{\pi \cdot \mu \cdot f_s}} = 0.292\ mm$

$r := 0.8575\ mm$

$R_{ac} := \frac{\pi \cdot r^2}{\pi \cdot r^2 - \pi \cdot \langle r - D_{pen} \rangle^2} \cdot R_{DC} = 0.148\ \Omega$

$I_{ac\_rms} := \frac{\Delta I}{\sqrt{12}} = 2.309\ A$ RMS value of triangular wave

$P_{copper\_inductor\_buck} := R_{DC} \cdot I_{DC}^2 + R_{ac} \cdot I_{ac\_rms}^2 = 13.83\ W$

$P_{loss\_inductor\_buck\_total} := P_{copper\_inductor\_buck} + P_{core\_loss\_buck} = 49.829\ W$

A6) capacitor loss

$ESR := 0.29\ \Omega$ EPCOS datasheet for B43504 470u/450v cap

$P_{loss\_buckcap} := 2 \cdot ESR \cdot I_{ac\_rms}^2 = 3.093\ W$ Two capacitors in series

A7) Total loss

$P_{loss\_passive\_buck} := P_{loss\_inductor\_buck\_total} + P_{loss\_buckcap} = 52.922\ W$

$P_{loss\_buck\_total\_without\_sync} := P_{loss\_total\_active} + P_{loss\_passive\_buck} = 91.927\ W$

$P_{loss\_buck\_total\_sync} := P_{loss\_total\_active\_sync} + P_{loss\_passive\_buck} = 86.37\ W$

B) Boost converter

Vin=208[v] Vo=800[v] Po=2[kw] CCS020M12CM2

B1) Mosfet+ Diode conduction losses

$I_{Davg} := 2\ A$

$I_{Drms} := 4.1\ A$

$R_{DS\_125} := 0.2\ \Omega$

$I_{Mos\_avg} := -0.138\ A$

$I_{Mos\_rms} := 7.38\ A$

$V_D := 0.75\ V$

$R_D := 0.12\ \Omega$

$P_{Cond} := R_{DS\_125} \cdot I_{Mos\_rms}^2 + R_D \cdot I_{Drms}^2 + V_D \cdot I_{Davg} = 14.41\ W$

B2) Mosfet switching losses SVPWM

CCS020M12CM2 datasheet and curve fitting

Rext(ON)=10ohm Rext(off)=5ohm for switch driver from CREE

$I_{DSoff}(\theta) := 21.25 \cdot \sin(\theta)$

$I_{DSon}(\theta) := 18.75 \cdot \sin(\theta)$

$K := \frac{0.775}{0.5}$ factor to scale the curve fitting equation for R=10 turn on gate resistance

Appendix C: **Derivation of analytical design equations for AC/DC three-phase third Harmonic injection SEPIC PFC**

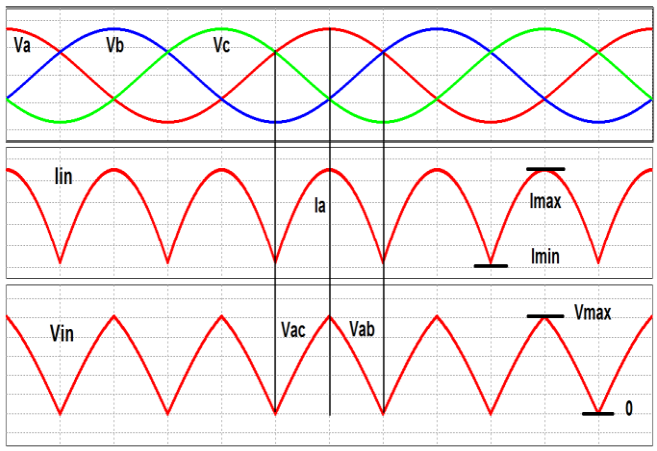

Figure. C-1 Upper SEPIC Input current and voltage

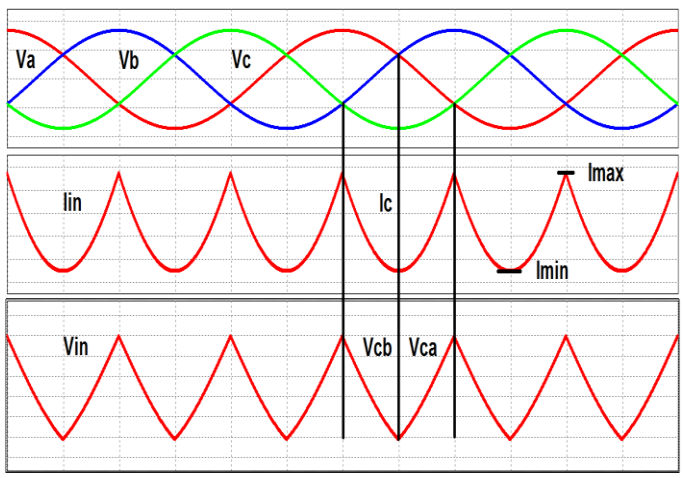

Figure. C-2 Lower SEPIC input current and voltage

C.1 **Sizing of L1, L2, L3, L4**

The above figures show the input current and voltage waveforms of Figure 3-2 with the input current depicted ideally without any ripple. The maximum input voltage is at crossing point of two phase voltages and equals $V_{max} = \sqrt{3}V_m \sin\frac{\pi}{3} = \frac{3}{2}V_m$ where V_{max} is the input peak voltage and V_m is the peak of the phase voltage. The duty cycle at peak voltage D_{Vm} equals:

$$D_{Vm} = \frac{\frac{V_0}{2}}{\frac{V_0}{2} + \frac{3}{2}V_m} = \frac{V_o}{V_o + 3V_m}$$

Using the inductor equation $\Delta V = L\frac{dI}{dt}$, and by plugging D_{Vm} , the minimum inductor for the targeted maximum ripple of ΔI_{max} equals:

$$L_{min} = \frac{\Delta V.dt}{dI} = \frac{\frac{3}{2}V_m D_{Vm} T_s}{\Delta I_{max}} = 1.5\frac{V_m D_{Vm}}{\Delta I_{max} f_{sw}}$$

Where T_s and f_{sw} are the switching period and frequency respectively. This equation can be used to size the inductors L1, L2 in Figure 3-2. The inductors L3 and L4 are energized by capacitors C1 and C2 respectively during the switch on-time D. In the steady-state, the momentarily DC voltage across the series capacitor equals the input voltage therefore, the inductors can be sized using the same equation.

C.2 **Sizing of C1 and C2**

The voltage ripple across the series capacitors C1, C2 is used as criteria for sizing. The maximum ripple across the capacitors is at maximum input average current I_m where the change in the electric charge on capacitors is maximum. Using the power equation

$$I_m = \sqrt{2}\frac{P_{in}}{\sqrt{3}V_L} = \frac{\sqrt{2}P_{in}}{\frac{\sqrt{3}.\sqrt{3}V_m}{\sqrt{2}}} = \frac{2}{3}\frac{P_{in}}{V_m}$$

Where P_{in} is the input power and V_L is the line-to line voltage. Using the capacitor charge equation and assuming ΔV_{Cmax} as maximum voltage ripple across the series capacitor:

$$C_{1,2min} = \frac{\Delta Q}{\Delta V_{Cmax}} = \frac{I_m(1 - D_{Vm})T_s}{\Delta V_{c1}} = \frac{I_m(1 - D_{Vm})}{f_{sw}\Delta V_{Cmax}}$$

C.3 **Sizing of Co1 and Co2**

The DC current through the capacitors C1 and C2 is zero, therefore the DC value of current in inductor L3, $I_{L3} = I_{Do1}$, where I_{Do1} is the DC current in diode. Ideally, the momentarily DC input power,$P_{in} = V_{in}I_{L1}$ equals DC output power, $P_o = \frac{V_o}{2}I_{L3}$ therefore:

$$\mathrm{I_{L3}} = 2\frac{\mathrm{V_{in}I_{L1}}}{\mathrm{V_o}}$$

The maximum current in inductor L3, $\mathrm{I_{L3m}}$ equals:

$$\mathrm{I_{L3m}} = 2\frac{V_{max}\mathrm{I_{L1}}}{\mathrm{V_o}} = 2.\frac{3}{2}\frac{\mathrm{V_m I_{L1m}}}{\mathrm{V_o}} = 3\frac{\mathrm{V_m I_{L1m}}}{\mathrm{V_o}} = 3\frac{\mathrm{V_m I_m}}{\mathrm{V_o}}$$

Assuming a triangular approximation forI_{L3}, the waveform can be described by the Fourier series:

$$I_{l3}(t) = \frac{8I_{l3m}}{\pi^2}\sum_{n=1,3,5,\ldots}^{+\infty}\frac{(-1)^{\frac{(n-1)}{2}}}{n^2}\sin(\omega nt)$$

Where n is the harmonic number. The output diode current contains DC component, switching frequency, and low frequencies (multiples of mains frequency). The DC component provides output current and the rest of harmonic content needs to be filtered by output capacitor Co1.The capacitor sized to filter out low frequency will filter out switching frequency as well. The first harmonic from above equation equals: $I_{l3_1} = \frac{8I_{l3m}}{\pi^2}$ and has the dominant amplitude as compared to other harmonic numbers and therefore to a very good approximation can be used to size the output capacitor. the output capacitor need to filter out this component for the desired output ripple. Thus, the minimum output capacitor for an assumed amount of voltage ripple ΔV_{co} equals:

$$C_{o1} = \frac{I_{co1}}{\Delta V_{co}\omega} = \frac{I_{l3_1}}{\Delta V_{co}\omega} = \frac{4}{3\pi^3}\frac{I_{l3m}}{\Delta V_{co}f_m}$$

Where $\omega = 2\pi f_m$ is the mains angular frequency and f_m is the mains frequency.

Appendix D**: Boost and Buck inductor design**

Based on the amount of ripple assumed in sections 2.3.1 and 2.3.2, a value of 500 μH was calculated for inductors La, Lb, Lc and Lf of Figure 2-1. According to converter specifications as in Table 2-1 and assuming a worst-case efficiency $= 0.9$, the highest rms current I_{lrms} , and the maximum I_{lmax} for the nominal output power $P_{out} = 5000\ \mathrm{W}$ in boost inductors will be at low-line 208 V and equal:

$$I_{lrms} = \frac{P_{out}}{\eta\sqrt{3}V_{l\_lrms}} = \frac{5000\ \mathrm{W}}{0.9.\sqrt{3}.208} = 15.42\ \mathrm{A}$$

$$I_{lmax} = 21.8\ \mathrm{A}$$

The powder core catalog from magnetics is used for inductor core selection procedure [47]. For the above current level and assuming a current density of 800 $\left[\frac{\mathrm{A}}{\mathrm{Cm}^2}\right]$, AWG14 magnet wire size is chosen. KooLMu cores were selected for good performance and cost. Using LI^2 charts of core catalog KooLMu 77191 from magnetics were chosen.

For a typical design with a winding factor, $\mathrm{WF} = 30\%$, the number of turns N, Assuming $\mathrm{A_W}$ as wire cross-section and $\mathrm{W_A}$ as toroid core internal cross-section equals:

$$N = \frac{\mathrm{WF.W_A}}{\mathrm{A_W}} = \frac{0.3 * 514}{2.31} = 66$$

To determine the number of cores to be stacked. We first calculate the total amount of inductance factor, A_{Ltotal} at full-load:

$$A_{Ltotal} = \frac{L}{N^2} = \frac{500\ \mu\mathrm{H}}{66^2} = 115\ [\frac{\mathrm{nH}}{\mathrm{T}^2}]$$

Referring to core chart, the ampere-turns at full load, $A.T = 22 * 66 = 1452[\mathrm{A.T}]$. At this point $A_L = 42\ [\frac{\mathrm{nH}}{\mathrm{T}^2}]$, therefore, n, the number of cores to be stacked, equals:

$$n = \frac{A_{Ltotal}}{A_L} = 2.7$$

Therefore, three cores are stacked and the value of inductance factor at full-load and no-load are:

$$A_{full-load} = 3 * 42 = 126[\frac{\mathrm{nH}}{\mathrm{T}^2}]$$
$$A_{No-load} = 3 * 60 = 180[\frac{\mathrm{nH}}{\mathrm{T}^2}]$$

Therefore, the values of inductor at full-load and no-load will be:

$$L_{full-load} = A_{full-load}.N^2 = 549\ \mu\mathrm{H}$$
$$L_{No-load} = A_{No-load}.N^2 = 784\ \mu\mathrm{H}$$

Using the above design, boost inductors cores depicted in Figure 2-1 were built. The no load inductance was measured to be $778\ \mu\mathrm{H}$. The frequency response of the inductor is also depicted in figure below showing good characteristics for the range of frequency of operation.

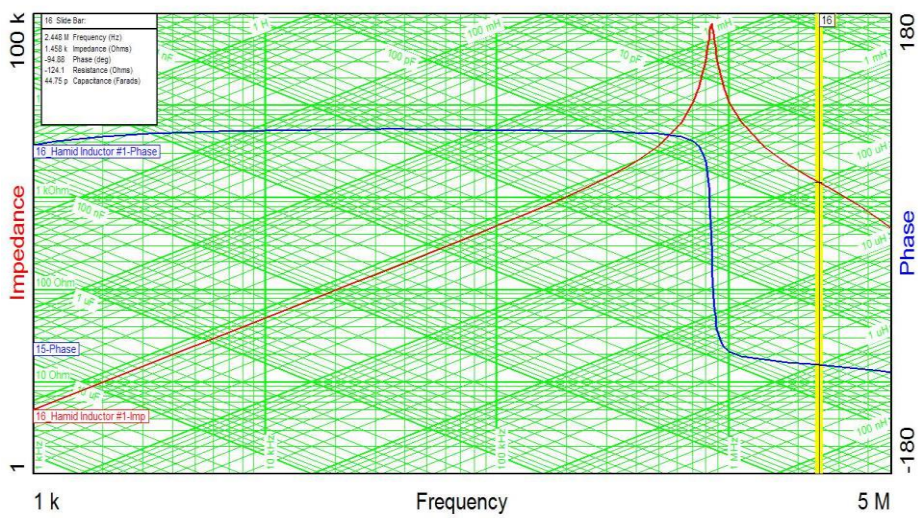

Figure. D-1 Frequency response of designed 500 µH inductor

A similar procedure may be used for the design of buck inductor and is skipped here for the sake of brevity.