High-Efficiency and Low Noise Planar Transformers for Power Converters: Paired Layers Interleaving

by

Mohammad Ali Saket Tokaldani

BSc., Amirkabir University of Technology, Iran, 2009
MSc., Sharif University of Technology, Iran, 2011

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The following individuals certify that they have read, and recommend to the Faculty of Graduate and Post-doctoral Studies for acceptance, the dissertation entitled:

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submitted by Mohammad Ali Saket Tokaldani in partial fulfillment of the requirements for
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Examining Committee:

Dr. Martin Ordonez, Professor, Electrical and Computer Engineering, UBC
Supervisor

Dr. Wilson Eberle, Associate Professor, Electrical Engineering, UBC Okanagan
Supervisory Committee Member

Dr. Shahriar Mirabbasi, Professor, Electrical and Computer Engineering, UBC
University Examiner

Dr. Bhushan Gopaluni, Professor, Chemical and Biological Engineering, UBC
University Examiner
Abstract

Nowadays, many applications, such as consumer electronics, the automotive industry, and telecoms require high power density and low height power electronics converters. To implement slim power converters, Planar Transformers (PT) have emerged, featuring low height, low leakage inductance, and low thermal resistance. Despite these benefits, PTs have large parasitic capacitance, which degrades the performance of power converters. Capacitive effects in transformers are divided into two groups: inter-winding and intra-winding capacitance. Inter-winding capacitance generates large amounts of Common-Mode (CM) noise, creating serious Electromagnetic Interference (EMI) problems. Intra-winding capacitance affects the performance of the converter and can cause loss of voltage regulation in the LLC resonant converter.

The inter-winding capacitance can be reduced by separating primary and secondary windings, at the cost of increased leakage inductance and AC resistance. On the other hand, interleaved structures minimize AC resistance and leakage inductance but significantly increase the inter-winding capacitance. Therefore, there is an unfortunate trade-off in the transformer design. In order to resolve this trade-off as well as problems resulting from PTs large parasitic capacitance, this dissertation develops new design methods that target the root cause of the problem. A detailed parasitic capacitance model is developed for PTs that relate the distributed capacitance of layers to the equivalent circuit of the transformer. Based on this model, the concept of paired layers is introduced that provides criteria to achieve zero CM noise generation in PTs. Paired layers can be used to design interleaved structures that not only have low AC resistance and leakage inductance but also have almost zero CM noise generation. Multiple examples are provided for different types of windings, different turn ratios, and different topologies to show the generality of the method. The proposed method is validated using analysis, Finite Element Method (FEM), and experiments.

Besides the paired layers method, this dissertation studies the detrimental effects of PTs large intra-winding capacitance on light-load voltage regulation of LLC resonant converter. It is shown that large intra-winding capacitance results in loss of voltage regulation. To resolve this, six improved winding layouts with low intra-winding capacitance are presented to maintain voltage regulation even under no-load condition.
This dissertation proposes a new design method for planar transformers-paired layers interleaving-that eliminates a fundamental trade-off in planar transformer design. Using the proposed method, it is possible to design highly efficient transformers that have not only low conduction loss but also minimal noise emission. These two advantages cannot be attained using traditional design methods, so planar transformers were traditionally either efficient or low noise. The proposed method resolves this trade-off and introduces a new family of planar transformers that have it all. Planar transformers are the state-of-the-art high-frequency transformers used at the heart of power electronics converters, which in turn are fundamental to the continued profitable growth of the telecommunications, automotive, aerospace, medical, military, and data processing industries. The design of the planar transformers significantly affects the converters overall performance. Now, with the proposed method, the efficiency and performance of such converters can be considerably improved.
Preface

This work is based on research performed at the Department of Electrical and Computer Engineering of the University of British Columbia by Mohammad Ali Saket Tokaldani, under the supervision of Prof. Martin Ordonez. Chapter 1 contains modified portions of text from all the below-listed publications. Portions of Chapters 2, 3, and 4 have been published in IEEE Transactions on Power Electronics, IEEE Applied Power Electronics Conference & Exposition (APEC), and IEEE Energy Conversion Congress and Exposition (ECCE) [1–4]. It worth mentioning that the paired layers interleaving method won a Second Place Prize Paper Award for 2018 in IEEE Transactions on Power Electronics. The paper was nominated for this award out of 935 papers published and some 13,000 papers that were submitted to the journal in 2018.


I was the lead investigator of the above papers, developed the proposed concepts, built simulation models,
performed experimental verifications, and wrote the manuscripts. Prof. Martin Ordonez was the supervisory author on the above papers and was involved throughout the project and provided technical advice and edited manuscripts. Dr. Navid Shafiei helped me in building the experimental test setup. Mr. Marian Craciun and Mr. Chris Botting were industry partners (Delta-Q Technologies, Vancouver, BC) in this project and provided feedback on the outcomes of the research.

Portions of Chapter 5 have been published in IEEE Transactions on Power Electronics, IEEE Applied Power Electronics Conference & Exposition (APEC), and IEEE Energy Conversion Congress and Exposition (ECCE) [5-7].


As the first author and lead investigator of the above-mentioned publications, the author of this thesis developed the proposed concepts, built simulation models, performed experimental tests and wrote the manuscripts. Prof. Martin Ordonez was the supervisory author on the above papers and was involved throughout the project by providing technical advice and editing manuscripts. Dr. Navid Shafiei helped me in building the experimental test setup. Mr. Marian Craciun and Mr. Chris Botting were industry partners (Delta-Q Technologies, Vancouver, BC) in this project and provided feedback on the outcomes of the research.
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# Glossary

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<tr>
<td>3D</td>
<td>three dimensional</td>
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<tr>
<td>CM</td>
<td>Common-Mode</td>
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<td>DM</td>
<td>Differential-Mode</td>
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<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
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<td>FEA</td>
<td>Finite Element Analysis</td>
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<td>FHA</td>
<td>First Harmonic Approximation</td>
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<tr>
<td>FI</td>
<td>Fully Interleaved</td>
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<tr>
<td>FEM</td>
<td>Finite Element Method</td>
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<td>LED</td>
<td>Light-Emitting Diode</td>
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<td>LISN</td>
<td>Line Impedance Stabilization Networks</td>
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<td>MMF</td>
<td>Magneto-Motive Force</td>
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To my parents, Zeinab and Aliakbar
Chapter 1

Introduction

1.1 Motivation

Today, high-efficiency power converters are fundamental to the continued profitable growth of the telecommunications, automotive, aerospace, and data processing industries. Power converters are high-frequency power conversion circuits used to convert a DC or AC input voltage to a DC or AC output voltage having a larger or smaller magnitude, possibly with opposite polarity or with the isolation of the input and output ground references. At the heart of an isolated power converter is a high-frequency transformer that aids the voltage gain of the converter and also provides isolation between primary and secondary windings. In order to reduce the size of the transformer and increase the power density of the converter, a high switching frequency is employed.

Nowadays, many modern applications require low profile power converters, such as consumer electronics, the automotive industry, and telecoms. Due to the height of traditional magnetic cores, the form factor of power converters is often plump and bulky. In order to implement slim converters for the above-mentioned applications, the Planar Transformer (PT), which has an intrinsically lower height, can be used. Unlike traditional wire-wound transformers, windings in PTs can be made using Printed Circuit Boards (PCB), copper foils, or a combination of both. Figure 1.1 shows two types of PTs made using copper foils and PCBs.

Despite the promising low profile and other advantages, PTs have extremely high parasitic capacitance, resulting in severe problems for power converters. In comparison to wire-wound transformers, PTs exhibit much larger parasitic capacitance due to the proximity of the planar layers and their significant overlap. In

\footnote{Portions of this chapter have been modified from [1-7]}
Figure 1.1: Different winding types in PTs: a) single-turn copper foils and b) multi-turn spiral PCBs.

In particular, parasitic capacitances in the transformers are divided into two groups: inter-winding and intra-winding capacitance. Intra-winding capacitance originates from the capacitive coupling between layers of the same winding, while inter-winding capacitance is the result of capacitive coupling between layers of different windings (i.e., one from primary and another from secondary). These capacitive effects are distributed, as indicated in Fig. 1.2 (a). The total effect of distributed parasitic capacitance can be modeled by six different capacitors in the transformer equivalent circuit, as shown in Fig. 1.2 (b). The distributed intra-winding capacitance of each winding can be modeled as a lumped capacitor between terminals of that winding. These capacitors are shown in purple in Fig. 1.2. On the other hand, the effect of distributed inter-winding capacitance can be modeled by four capacitors between primary and secondary windings of the transformer, which are shown in red in Fig. 1.2.

Both intra- and inter-winding parasitic capacitance have detrimental effects on the performance of DC-DC converters. Transformers’ inter-winding capacitance is one of the main sources of Common-Mode (CM)
noise in the converter. CM noise in the transformer originates from an undesired electrostatic coupling between primary and secondary windings. In PTs, whenever a layer of primary winding overlaps a layer of the secondary winding, due to the proximity and large overlapping area of planar layers, a large parasitic capacitance is formed between overlapping layers. This parasitic capacitance is exposed to a large $\frac{dv}{dt}$ when the voltage of overlapping layers changes rapidly. This leads to the generation of pulsating currents (known as CM noise) that circulate between primary and secondary windings through the earth and create EMI problems [8]. Since the current in the parasitic capacitor is equal to $C \frac{dv}{dt}$, the value of $\frac{dv}{dt}$ between overlapping layers is a major factor in the value of CM noise. While traditional interleaving methods reduce AC resistance by interleaving primary and secondary layers [9, 10], these methods do not consider $\frac{dv}{dt}$ of overlapping layers and may lead to large $\frac{dv}{dt}$ coupling. Unfortunately, CM noise of traditional interleaved structures imposes the use of large CM chokes to comply with EMI standards, reducing the converter’s power density. To date, no design method for PTs has been proposed that can achieve both low AC resistance and very low CM noise generation.

On the other hand, the high intra-winding capacitance gives rise to a high charging current at the transformer input, resulting in lower efficiency and increased peak voltage stress across secondary rectifying devices [11]. In addition to these problems, intra-winding capacitances bring unwanted regulation issues in some DC-DC converters, such as LLC resonant converter with wide output voltage regulation. Voltage regulation is a critical specification in power converters in order to accommodate input voltage fluctuations (e.g., line regulation) or output voltage changes (e.g., battery chargers) [12, 13]. The high intra-winding capacitance of the transformer severely distorts the light-load current and voltage waveforms of the converter, leading to unpredictable behavior of output voltage at the light-load [14].

This work investigates new design methods for PTs that overcome the inherently large parasitic capacitances, allowing PTs to be used more widely in modern power converters. To do so, this work proposes a detailed model for capacitive effects in PTs that links the distributed capacitance of Fig. 1.2 (a) to the lumped capacitors of Fig. 1.2 (b). This model gives a good insight into the nature of parasitic capacitance and shows how winding arrangement affects the equivalent capacitance circuit of the transformer. Using this model, the concept of “Paired Layers” is introduced, which can be used to design high-efficiency PTs with almost zero CM noise generation. This method finally eliminates the trade-off between parasitic elements in the transformer and results in interleaved PTs that have a low AC resistance, low leakage inductance and almost zero generation of CM noise at the same time. Since the design method depends on the transformer’s voltage distribution, different DC-DC topologies are considered and the proposed concept is used to develop
design methods for PTs used in these converters. Besides the paired layers interleaving method, this work also proposes six different winding layouts with very low intra-winding capacitance. These winding layouts can be used to resolve the light-load voltage regulation of LLC resonant converters with PTs. These layouts also can be used to design planar inductors with high self-resonant frequency, which is very desirable in high-frequency power converters.

1.2 Literature Review

Design, optimization and modeling of planar magnetic components started in the early 1990s [15–17]. In recent years, with the rapid development of PCB technology, research into slim power converters with low-profile cores and PCB winding technologies has attracted widespread international attention [18–29]. Planar magnetics have a number of advantages, which can be summarized as follows:

1. **Low Profile:** Generally, the height of a planar magnetic component is 1/4 to 1/2 the height of its wire-wound counterpart [10]. This makes them an excellent choice for slim power converters.

2. **Repeatability and Parasitic Element Predictability:** Windings in planar magnetics are usually made using PCB and/or copper foils. The simple automatic assembly process increases the repeatability and results in consistent, predictable, and controllable parasitic parameters of the manufactured devices [30].

3. **Ease of Manufacture and Lower Cost:** Advances in the PCB industry have not only reduced the cost of PCB manufacturing but also significantly increased the speed of PCB production. Nowadays, large quantities of PCB windings can be manufactured in a short amount of time and for competitive prices. Besides, PCB windings can be assembled using automated machines, increasing the speed of manufacturing and reducing labor costs.

4. **Excellent Thermal Characteristics:** Due to a higher ratio of surface area to volume, they exhibit a low thermal resistance and efficiently conduct heat, which leads to a lower temperature rise of the component. The ease of heat removal greatly increases the power density of the converter [31,32].

5. **Modularity:** Circuit components can be mounted on the same PCB winding, eliminating the need for extra connections.

6. **Flexibility in Winding Arrangement:** Using PCBs for windings allows for sophisticated interleaving schemes, minimizing AC resistance and leakage inductance of windings.
Despite the above-mentioned benefits, PTs suffer from large parasitic capacitance due to the large overlapping area of planar layers and their proximity. The work in [1] compares a 100W PT that has 700\(pF\) inter-winding capacitance with its wire-wound equivalent transformer which only has 10\(pF\) inter-winding capacitance. The large parasitic capacitance of PTs significantly deteriorates the performance of the circuit and cannot be ignored. For instance, it creates serious EMI problems, reduces efficiency, and can result in loss of voltage regulation in some topologies. However, most of the publications for planar transformer design address the reduction in leakage inductances and high-frequency winding losses, while winding capacitances have rarely been considered effectively [10]. This dissertation targets problems that arise from the parasitic capacitance of PTs and proposes design methods for PTs that resolve these problems. Parasitic capacitance in the transformers is divided into two groups: intra-winding capacitance and inter-winding capacitance. Inter-winding capacitance is the major source of CM noise in the converter, which creates EMI issues. On the other hand, intra-winding capacitance affects the performance and efficiency of the converter and can result in loss of voltage regulation in certain topologies. These problems and their related literature are discussed here.

1.2.1 Transformer CM Noise Minimization

Every commercial power supply has to pass EMI tests before going to the market. This means that the converter’s level of conducted noise (which consists of Differential-Mode (DM) and Common-Mode (CM) noise) should be below standard limits. It is always a challenge to ensure that the EMI of a converter meets EMI standards [33–36]. Both CM and DM filters are used at the EMI filter stage to suppress noise. Reducing CM noise emission can greatly reduce the size of required CM chokes and enhance the converter’s power density. In most cases, CM noise current is mainly caused by the displacement current within the inter-winding parasitic capacitance of transformers and the parasitic capacitance between semiconductor switches and the ground. The CM noise paths in a Flyback converter are shown in Fig. 1.3. The CM noise current flows into the ground through the parasitic capacitance between the high \(\frac{dV}{dt}\) nodes, such as the drain of the MOSFET. In Fig. 1.3 the MOSFET’s drain-to-heatsink parasitic capacitance is between the ground and a high \(\frac{dV}{dt}\) point. Therefore, this parasitic capacitance generates \(i_{CM-S}\) flowing back to the converter via Line Impedance Stabilization Networks (LISN). This figure shows that the transformer’s parasitic capacitance is another major source of CM noise. As shown in this figure, the transformer’s CM noise \(i_{CM-T}\) flows back to the converter via LISNs at the primary side, increasing the total noise of the converter. Figure 1.3 also shows that secondary side diode’s anode-to-heatsink parasitic capacitance generates CM noise current of
$i_{CM-D}$. However, since this current does not return through LISNs, it does not affect the converter’s CM noise. In order to comply with the standards, both $i_{CM-S}$ and $i_{CM-T}$ must be minimized. Different methods for attenuating $i_{CM-S}$ can be found in [37–40]. The focus of this work, however, is on attenuating $i_{CM-T}$.

Since the structure of the transformer determines CM noise levels, this topic has been considered in numerous works, and interesting methods have been proposed to mitigate CM noise. Regarding the transformer structure, mitigation methods can be classified into two groups. In the first group, additional layers are added to the transformer structure to either shunt away or inject anti-phase displacement currents to reduce noise. These methods are applicable on both wire-wound transformers and PTs and include using Faraday shields [8, 41, 42], introducing out of phase displacement currents [43–45] and integrating a Y-cap in the structure of the transformer [46]. However, since extra layers (in addition to the primary and secondary) are required, the transformer fill factor is reduced, which increases the resistance of the windings. In addition, conduction loss may increase due to eddy currents in these additional, auxiliary windings. As well, the additional layers (Faraday shields or anti-phase windings) prevent the implementation of interleaved structures that are required to minimize AC resistance (there are multiple overlaps of primary and secondary layers in interleaved structures). The second group of methods targets the source of CM noise and mitigates the CM noise without adding extra layers. Reducing the inter-winding capacitance [11] is the most straightforward method of reducing the CM noise and can be done in both wire-wound transformers and PTs. This can be done using a non-interleaved structure (in which primary and secondary are separated and only have one overlapping area) or avoiding the overlap between the primary and secondary windings. However, doing this
dramatically increases the AC resistance and therefore conduction losses. Recently, the winding cancellation method for wire-wound transformers has been presented in a number of papers [47–52]. This method minimizes the amount of CM noise generated not by reducing the inter-winding capacitances but by reducing the $\frac{dv}{dt}$ to which these capacitances are exposed. Therefore, it does not produce the side effects of other methods, such as higher winding resistance or extra eddy current loss. As the problem of parasitic capacitance is more significant with PTs, having a similar method that can attenuate the CM noise without requiring extra components or leading to additional loss and increased complexity is highly beneficial. Therefore, there is a significant opportunity to develop a winding cancellation technique for PTs to achieve minimal CM noise generation.

This dissertation resolves the large CM noise problem of PTs by proposing the concept of paired layers. According to this concept, layer layout and winding arrangement can be designed in a way that results in PTs with almost zero CM noise generation. In comparison with methods reported in the literature, the proposed concept does not separate primary and secondary windings and can achieve zero CM noise generation even in the highly interleaved structures.

1.2.2 Winding Optimization for Reducing AC Resistance and Leakage Inductance

Similar to the conventional magnetic structures, the demand for high-frequency switching increases winding losses due to the skin and the proximity effects, particularly at frequencies above 100 kHz [9]. AC resistance effects due to sinusoidal currents were treated by Bennett and Larson [53] and this work was tailored specifically for transformers by Dowell [54]. Dowell’s equations were later analyzed, rearranged, and improved for different situations [54–59]. The work in [60] presents the optimum layer thickness of conductors to minimize winding loss. The effect of winding arrangement on AC resistance and leakage inductance is discussed in numerous works [9, 60–64]. In most papers about optimizing PTs, the main purpose is to reduce leakage inductances, and they do this by proposing highly interleaved structures that minimize leakage fluxes. However, stray capacitances of these arrangements have not seriously been considered. As discussed before, interleaved structures have multiple overlaps of primary and secondary layers and so exhibit a very large inter-winding capacitance, generating a large amount of CM noise and consequently contributing to EMI problems [65].

From the above discussion, it is can be concluded that the reported methods in the literature minimize AC resistance and leakage inductance at the expense of large CM noise. This trade-off is presented in Fig. 1.4 (a). On the left side, an interleaved structure is shown that has a low AC resistance and leakage inductance.
Figure 1.4: a) The tradeoff between low AC resistance and low inter-winding capacitance. b) The proposed method resolves this tradeoff and achieves low AC resistance, low leakage inductance and minimal CM noise at the same time.

However, since it has multiple overlapping of the primary and secondary windings, it has a large parasitic capacitance which generates high amounts of CM noise. On the right side, a non-interleaved structure that separates primary and secondary windings is shown. Since there is only one overlapping between primary and secondary windings, the value of inter-winding capacitance (and so generated CM noise) is reduced. However, this structure has the side effect of having large AC resistance and leakage inductance. No design method has been reported in the literature that resolves this trade-off and achieves both low AC resistance and very low CM noise generation.

This has been considered in this dissertation, and interleaving methods have been combined with the proposed concept of “paired layers” to achieve PTs that not only have minimal AC resistance and leakage inductance but also generate almost zero CM noise. According to the concept of paired layers, there are layers in the primary and secondary that have a similar $\frac{dv}{dt}$ and it will be shown that overlapping of such
layers does not generate CM noise. These layers can be used to design highly interleaved structures that not only have a very low AC resistance and leakage inductance, but also generate almost zero CM noise, although they have a very large inter-winding capacitance. The key is to use these paired layers at the intersections of primary and secondary in the transformer structure. As shown in Fig. 1.4 (b), paired layers interleaving finally eliminates the trade-off between low AC resistance and low CM noise and gives the designer a tool to achieve both.

1.2.3 LLC Resonant Converter Light-Load Voltage Regulation With PTs

In order to reduce switching loss and to improve EMI, soft switching techniques have emerged. Soft switching also enables working at higher frequencies which reduces the size of magnetic components [66-72]. Among different soft-switched converters, the LLC resonant converter offers many advantages, including high part-load efficiency, no-load voltage regulation, wide gain range over narrow frequency variation, inherent short circuit capability, and good cross regulation [73]. In a high-frequency LLC converter, magnetic components are often the bulkiest parts, and they determine the overall height of the converter [74]. In order to implement slim profile LLC converters, PTs can be used since they feature low height, reproducibility, lower leakage inductance, and low thermal resistance [9, 75]. Despite the promising low profile and manufacturing advantages of PTs, their inherent high parasitic capacitances result in severe problems for LLC converters. The paired layers method introduced in the previous parts minimizes CM noise by making dv/dt of inter-winding parasitic capacitors equal to zero. As mentioned before, intra-winding capacitance is another type of parasitic capacitance that can interrupt the dynamic behavior of the LLC resonant converter. Unfortunately, the paired layers method only targets inter-winding capacitance and does not resolve issues due to intra-winding capacitance. To solve this issue, a different approach from the paired layers method was employed which tries to minimize the value of parasitic capacitances. To do so, this part of the work proposes new winding layouts and structures to reduce both intra-winding and inter-winding capacitance.

Figure 1.5 (a) shows a LLC resonant converter schematic and includes the parasitic elements of the transformer (leakage inductances, winding resistances, and parasitic capacitances). Figures 1.5 (b), (c), (d) and (e) present the problems that arise from the transformer’s parasitic capacitances. As discussed, the high inter-winding capacitance between primary and secondary generates CM noise and contributes to EMI issues. A large intra-winding capacitance gives rise to a high charging current at the transformer input, resulting in lower efficiency and increased peak voltage stress across secondary rectifying devices. In addition to these problems, parasitic capacitances bring unwanted regulation issues for LLC resonant
Figure 1.5: (a) The LLC resonant converter considering parasitic elements of the transformer and one capacitor model of the transformer. (b) Transformer distorted no-load voltage due to the stray capacitance. (c) The no-load voltage gain characteristics of the converter with different transformers: Unfortunate increase of voltage and deviation of experimental characteristics from FHA prediction with high stray capacitance. (d) CM noise problem due to the inter-winding capacitance. (e) A portion of the transformer consisting of one primary PCB and two secondary PCBs (each PCB is a double-layer PCB).

converters with wide output regulation. Voltage regulation is a critical specification in power converters to accommodate input voltage fluctuations (e.g., line regulation) or output voltage changes (e.g., battery chargers). The large parasitic capacitance of a transformer severely distorts the light-load current and voltage waveforms of the converter. This leads to the erratic behavior of output voltage which cannot be seen by
First Harmonic Approximation (FHA), which is the conventional approach to model this type of converter.

During the last few years, interesting research has been done to design high efficiency PT, for LLC resonant converters [9, 11, 76–86]. Most of these papers have focused on the AC resistance and leakage inductance, so the impact of transformer parasitic capacitance on the LLC performance is not covered. In particular, it is interesting to note that the root cause of the LLC regulation problem using PTs has not been addressed in detail in the past. Since the voltage regulation problem of the LLC resonant converter also can be caused by rectifier diode junction capacitance, [14, 87, 88] have developed methods to address this problem. The work in [87] developed a higher-order topology that can mitigate the effect of diode junction capacitances for different modes of operation. Research in [14] suggests that adding a dummy load can solve the problem for small values of diode junction capacitance. The work in [88] presents another mitigation strategy by adding a capacitor to the primary side. Although prior methods are successful in resolving the regulation issue due to the diode junction capacitance, their efficacy is limited to the values in the range of diode junction capacitance. Since the parasitic capacitance of PTs is much larger, preceding methods cannot be used to resolve the regulation problem. For instance, the work in [9] reports stray capacitances in the order of a few Nano Farads for conventional PTs, which results in serious regulation problems in the LLC resonant converters. Although many papers have discussed different aspects of using PTs in LLC resonant converter, a paper that resolves the light-loading voltage regulation problem along with high full-load efficiency still is missing in the literature.

As will be discussed in chapter 5, in order to have a high efficiency LLC converter with wide output regulation, both parasitic capacitance and AC resistance should be minimized. The strategies proposed in chapter 5 provide solutions for light-loading regulation while ensuring high efficiency under full-load condition. These strategies include proposing winding layouts that achieve extremely low intra-winding capacitance (to solve light-loading voltage regulation problem) and winding arrangements that minimize AC resistance and winding loss.

1.3 Contributions of the Work

In order to eliminate the trade-off in PT design and also to address other problems associated with PTs’ large parasitic capacitance, this dissertation targets the root cause of the problem and proposes new design methods for PTs. The main contributions of this work are the following:

1. **Detailed parasitic capacitance model of PTs:** The first step of this work involves developing a detailed parasitic capacitance model for PTs, which is presented in chapter 2. This parasitic capacitance
model starts from modeling the overlapping of two planar layers, which is then extended to the whole winding. As mentioned before, parasitic capacitance has a distributed nature and the six-capacitor model of the transformer is an equivalent model. The developed parasitic capacitance model relates the distributed capacitance of each overlapping to the six-capacitor model, giving a deep insight into how the value of each capacitor in the model depends on the arrangement of the winding. The model is extracted analytically and is verified using Finite Element Analysis (FEA)\(^2\) and experimental measurements. This model provides a theoretical basis for the proposed concepts in chapters 3 and 4.

2. **Paired-layers interleaving.** In order to resolve the trade-off in PT design and minimize AC resistance, leakage inductance, and CM noise at the same time, the concept of “paired layers” is proposed in this work. This concept resolves the trade-off between EMI problems (inter-winding capacitance) and high-efficiency performance (low AC resistance and leakage inductance). The concept of paired layers matches layers with similar \(\frac{dv}{dt}\) and shows which layers can overlap without generating CM noise. This concept enables the designer to use interleaved structures and not to worry about CM noise, as the layers and winding arrangement are designed in such a way that the overlapping of primary and secondary layers does not generate CM noise. The method is verified using analysis, and experimental results prove the strength of the method in achieving low CM noise and high-efficiency PTs. Since the mechanism of CM noise generation in the transformer depends on the topology, different types of power converters are divided into three groups and the method is developed for each group. Many examples are provided for different topologies, turns ratios, and different types of planar windings throughout chapters 3 and 4 to make the method easy to understand.

3. **PCB winding layout with low intra-winding capacitance:** The high intra-winding capacitance of regular multi-turn PCB winding layouts causes a number of problems in DC-DC converters. If used for planar inductors, large intra-winding capacitance reduces the self-resonant frequency of the inductor, limiting its operating frequency range. If used as the planar transformer, the high intra-winding capacitance gives rise to a high charging current at the transformer input, resulting in lower efficiency and increased peak voltage stress across secondary rectifying devices [11]. In addition, PTs’ intra-winding capacitance brings unwanted regulation issues for LLC resonant converters with wide output regulation. To solve these problems, this work proposes novel winding layouts that have a significantly lower intra-winding capacitance. Six new winding layouts are proposed and it is shown that the use of

\(^2\)MAXWELL software from ANSYS was used for the simulations.
these layouts resolves the above-mentioned problems.

1.4 Dissertation Outline

In Chapter 2 a detailed parasitic capacitance model of PTs is developed to gain insight into the factors that influence the parasitic capacitance of PTs. The model starts with the analysis of overlapping between two planar layers and is then extended to the full transformer. This model shows how lumped parasitic capacitors of the transformer’s equivalent circuit are related to the distributed capacitance of overlapping layers and how the value of each lumped capacitance can be tuned by changing the winding arrangement. Besides, numerical analyses required to extract the equivalent parasitic capacitance are proposed in this chapter. The proposed model is verified using FEA and experimental measurements. This model provides a theoretical basis for the methods proposed throughout the dissertation.

In chapter 3, the concept of paired layers is proposed as a means to develop design methods that result in PTs with almost zero CM noise generation. First, the mechanism of CM noise generation when a layer of primary overlaps a layer of secondary is modeled and criteria to make the net CM noise of this overlapping equal to zero is found. The criteria set some rules on the layout of planar layers and also on which layers of primary and secondary are allowed to overlap (these layers are called paired layers). This concept matches layers with similar $\frac{dv}{dt}$ and shows which layers can overlap without generating CM noise. Besides, methods are proposed to avoid CM noise generation through the core. Since the topology of the converter is an important factor contributing to the transformer’s CM noise, different DC-DC topologies are divided into three groups and paired layers are found for each topology. Besides, the layout requirement of overlapping layers is discussed in this section. The proposed concept is also verified using the proposed capacitance model of chapter 2. It is shown that incorporating the paired layers concept in the winding arrangement results in an equivalent circuit for PT that has net CM noise equal to zero.

In Chapter 4, the concept of paired layers is combined with interleaving methods to resolve the trade-off in PT design. The resulting method is called paired layers interleaving which allows us to design PTs that not only have a very low AC resistance and leakage inductance, but also have a near-zero CM noise generation. Different types of planar windings are considered and it is shown how the method can be used with almost any type of planar winding. The three groups of topologies are considered in this chapter and examples are provided for each group to make the method easy to understand and implement.

In Chapter 5 the problem of LLC resonant converters with conventional PTs is discussed, and it is shown that the large intra-winding capacitance of conventional PTs results in loss of voltage regulation in
LLC resonant converters under light-loading condition. The proposed paired layers method only targets the inter-winding capacitance and has no effect on intra-winding capacitance. To resolve the issue of intra-winding capacitance, novel PCB winding layouts are proposed that significantly reduce the intra-winding capacitance of the transformer and resolve the issue of voltage regulation in LLC resonant converters. The proposed winding layouts can also be used for planar inductors and result in inductors with a wide operating frequency range, as the self-resonant frequency of the resulting PTs is much higher than that of the regular planar inductors. It should be mentioned that the approach in this chapter is different from the paired layers method and the proposed methods reduce the adverse effects of parasitic capacitance by directly reducing the value of parasitic capacitance.

Chapter 6 contains the relevant conclusions, contributions, and planned areas of future work. The work contributes significantly to the field of planar magnetics by proposing the paired layers interleaving method and also low intra-winding spiral PCB winding layouts. The contributions are highlighted in seven relevant publications in IEEE Transactions journals and international conference papers.
Chapter 2

Parasitic Capacitance Model for PTs

Parasitic capacitance in transformers can be divided into two groups: inter-winding and intra-winding capacitance. Intra-winding capacitance originates from the capacitive coupling between layers of the same winding, while inter-winding capacitance is the result of capacitive coupling between layers of different windings (i.e., one from primary and another from secondary). These parasitic capacitances are distributed, as indicated in Fig. 2.1 (a). The total effect of distributed parasitic capacitance in the lower frequency range can be modeled by six lumped capacitors in the transformer equivalent circuit, as shown in Fig. 2.1 (b). Such a model proved to be reliable up till one and, even, two decades beyond \( f_o \), that is the lower parallel resonance frequency of the transformer which appears on the Bode plots [89]. The distributed intra-winding capacitance of each winding can be modeled as a lumped capacitor between terminals of that winding. These capacitors are shown in purple in Fig. 2.1 (b). On the other hand, the effect of distributed inter-winding capacitance can be modeled by four capacitors between the primary and secondary ports of the transformer, shown in red in Fig. 2.1 (b).

The objective of this chapter is to develop a general equivalent parasitic capacitance model that relates the distributed capacitance of individual layers in Fig. 2.1 (a) to the six lumped capacitors of Fig. 2.1 (b). This model will be used in the next chapter to analytically validate the concept of paired layers which achieves virtually zero CM noise generation in PTs.

2.1 General Method for Modeling Equivalent Parasitic Capacitance

Figure 2.2 (a) shows a typical cross section of a PT. As shown in this figure, there are multiple overlaps between layers which contribute to the equivalent parasitic capacitance model of Fig. 2.1 (b). Fig. 2.2

\footnote{Portions of this chapter have been published in [1–4]}
Figure 2.1: a) Distributed parasitic capacitance in PTs. b) Transformer’s equivalent circuit.

(b) shows one of these intersections. This figure shows a typical condition that occurs when two layers of different windings overlap (i.e. one from the primary and the other from the secondary). As shown in Fig. 2.2 (b), depending on the turns ratio, overlapping layers can have a different number of turns. These layers are part of primary or secondary windings. Figure 2.2 (c) shows how these layers (turns) are related to the primary and secondary windings. In this example, four turns of the primary are exposed to two turns of the secondary. The electrostatic behavior of this overlapping can be modeled by six capacitors, as shown in Fig. 2.2 (c).

A similar condition happens for every overlapping, and six capacitors are needed to model the behavior of each overlapping. If the overlapping layers belong to the same winding, this model can be simplified into one capacitor, as will be shown in the next section. While the transformer is a two-port system from the magneto-static perspective, the inter-winding capacitance between primary and secondary winding provides a path from primary to secondary, making the transformer a three-port system from the electrostatic standpoint.

Figure 2.2: a) A typical cross-section of winding arrangement in PTs. b) Physical Representation of one overlapping of primary and secondary layers and c), parasitic capacitance model of this overlapping relative to the whole winding arrangement. Three voltages are defined to find the parasitic capacitance model.
For a three-port system, three independent voltages are needed to model the electrostatic behavior of the system. Without losing the generality, these three independent voltages are selected as in Fig. 2.2(c) and are defined as $V_1$, $V_2$, and $V_o$. $V_o$ is the DC offset voltage between windings. Using this voltage definition, the voltage across each capacitor of Fig. 2.2(c) can be found. In order to find individual values of $C_{ab}$, $C_{ac}$, $C_{ad}$, $C_{bc}$, $C_{bd}$, and $C_{cd}$, the energy method can be used. According to this method, the total energy of the overlapping is equal to the energy that is stored in the lumped capacitors of Fig. 2.2(c). This relationship is presented in (2.1).

$$W_t = \frac{1}{2} \int V \cdot D \, dV = \frac{1}{2} C_{ab} (aV_1 - bV_1)^2 + \frac{1}{2} C_{cd} (cV_2 - dV_2)^2 + \frac{1}{2} C_{bd} (bV_1 - dV_2 - V_o)^2 + \frac{1}{2} C_{ad} (aV_1 - dV_2 - V_o)^2 + \frac{1}{2} C_{bc} (bV_1 - cV_2 - V_o)^2 + \frac{1}{2} C_{ac} (aV_1 - cV_2 - V_o)^2$$  (2.1)

Where $E$ and $D$ are electric field and electric displacement field, respectively. Both of these quantities depend on $V_1$, $V_2$, and $V_o$. Unfortunately, finding a general analytical solution that describes the individual capacitor values for arbitrary winding layouts is not possible. Different number of overlapping turns lead to different equations, and the resulting relationships are complex and not insightful. Later in this chapter, two special cases that lead to insightful results are considered and solved analytically.

The next step in developing the parasitic capacitance model of the transformer is transferring $C_{ab}$, $C_{ac}$, $C_{ad}$, $C_{bc}$, $C_{bd}$, and $C_{cd}$ to the terminals of the transformer. Figure 2.3 shows this process. The energy method is again used to find the reflected values of these capacitors shown as $C_{12}$, $C_{13}$, $C_{14}$, $C_{23}$, $C_{24}$, and $C_{34}$ in Fig.

**Figure 2.3:** Transferring parasitic capacitance model of a single overlapping to the terminals of the winding. a) Parasitic capacitance model of an arbitrary overlapping, and b) the reflected parasitic capacitance model to the terminals of windings.
Equation (2.2) presents the energy relationship between Fig. 2.3 (a) and (b).

\[ W_t = \frac{1}{2} C_{ab} (aV_1 - bV_1)^2 + \frac{1}{2} C_{ad} (cV_2 - dV_2)^2 + \frac{1}{2} C_{bd} (bV_1 - dV_2 - V_o)^2 + \frac{1}{2} C_{ad} (aV_1 - dV_2 - V_o)^2 \]
\[ + \frac{1}{2} C_{bc} (bV_1 - cV_2 - V_o)^2 + \frac{1}{2} C_{ac} (aV_1 - cV_2 - V_o)^2 = \frac{1}{2} C_{12} (V_i)^2 + \frac{1}{2} C_{34} (V_2)^2 \]
\[ + \frac{1}{2} C_{24} (V_o)^2 + \frac{1}{2} C_{14} (V_1 - V_o)^2 + \frac{1}{2} C_{23} (-V_2 - V_o)^2 + \frac{1}{2} C_{13} (V_1 - V_2 - V_o)^2 \]  

Equating terms with similar coefficients results in transfer functions from the capacitor values of Fig. 2.3 (a) to capacitor values of Fig. 2.3 (b). This procedure should be done for every overlapping, and once it is done for all of the intersections, there will be six different groups of capacitors that are connected between terminals of the transformer. Each group consists of several capacitors that are connected in parallel. Under this condition, the equivalent capacitance of each group can be found by adding capacitors of that group, as all of the capacitors of each group are connected in parallel. The result is the six-capacitor model of the transformer which was depicted in Fig. 2.1 (b).

In the next section, the above-mentioned steps are done for the case of transformers with single-turn overlapping layers. For transformers with multiple-turn overlapping layers (such as Fig. 2.2), finding a general analytical solution is not possible and results in complicating and non-insightful equations. Numerical methods such as FEA should be used for these cases which are discussed later in this chapter.

### 2.2 Case 1: Parasitic Capacitance Modeling for PTs With Single-Turn Layers

As it was shown in Fig. 2.1 the capacitive behavior of a transformer in the lower frequency range can be modeled with six different capacitors. The proposed parasitic capacitance model of this section relates the distributed capacitance of layers to the lumped parasitic capacitors of Fig. 2.1 (b), and shows how winding arrangements affect the value of each lumped capacitor. In other words, the model discussed here fills the gap between the microscopic distributed capacitance and the transformer lumped capacitor model. The analysis starts with the capacitance model of two overlapping layers, and will then be extended to create a model for a complete winding structure.

Fig. 2.4 (a) shows two overlapping layers in PTs. Since the terminations of different windings are usually on different sides of the PTs, Fig. 2.4 (a) represents a typical interface of two layers that belong to different windings (i.e., one for the primary and the other for secondary). Four terminals are corresponding to these layers, which are shown as 1, 2, 3, and 4. Like the behavior of the transformer, the capacitive behavior
Figure 2.4: Electrostatic behavior model of two overlapping layers that belong to different windings:
a) 3D model of the system along with terminals and voltage directions. b) the overlapping layers are straightened while the voltage gradient between overlapping layers is preserved and c) the electrostatic model of the system of this system can be modeled with six lumped capacitances that are connected between the terminals of these layers. Three different voltages are needed to describe the electrostatic behavior of this system. These voltages are shown in Fig. 2.4. \( V_1 \) and \( V_2 \) are defined as the voltage between the terminals of the top and bottom layers, respectively. \( V_o \) is the offset voltage between the two layers. Using this voltage definition, the voltage across each capacitor can be found. The energy method will be used here to find the parasitic capacitance model of this system. According to this method, the total electrostatic energy of the system is equal to the energy that is stored in the lumped capacitances. In order to calculate the energy of Fig. 2.4(a), the layers should be straightened, while the voltage gradient between them should be preserved. Since the directions of the layers are different, there is a discontinuity in the voltage gradient of the two layers (which is indicated by the split line in Fig. 2.4(a)). Therefore, two straightened surfaces are required to model each layer. Figure 2.4(b) shows these surfaces. Since in these surfaces the voltage is changing in just one direction, the voltage distribution of these surfaces can be represented by a linear function that varies in one dimension. The voltage distribution for the yellow and blue layers are presented in (2.3).

\[
V_y(x) = \frac{V_1}{L} x \\
V_b(x) = \begin{cases} 
V_o + \frac{V_2}{2} - \frac{V_o}{L} x & 0 < x < \frac{L}{2} \\
V_o + \frac{3V_2}{2} - \frac{V_o}{L} x & \frac{L}{2} < x < L 
\end{cases}
\]  

(2.3)

Where \( L \) and \( W \) are the length and width of the layers in Fig. 2.4(a). When the voltage distribution is known,
the total energy of the system can be found by (2.4).

\[ W_t = \int_{0}^{L} \frac{1}{2} \varepsilon_0 \varepsilon_r \frac{W}{d} (V_y - V_b)^2 \, dx = \frac{C_0}{24} (4V_1^2 - 7V_1V_2 - 12V_1V_3 + 4V_2^2 + 12V_2V_3 + 12V_3^2) \] (2.4)

In the above equation, \( C_0 \) is the static capacitance between the layers, and can be found by using the parallel plate capacitor formula which is presented in (2.5).

\[ C_0 = \varepsilon_0 \varepsilon_r \frac{W \times L}{d} \] (2.5)

The energy of the system also can be found by using lumped capacitors. The total energy of the system based on the lumped capacitance model is presented in (2.6).

\[ W_t = \frac{1}{2} C_{12} V_1^2 + \frac{1}{2} C_{34} V_2^2 + \frac{1}{2} C_{24} V_3^2 + \frac{1}{2} C_{14} (V_1 - V_o)^2 + \frac{1}{2} C_{23} (V_2 + V_o)^2 + \frac{1}{2} C_{13} (V_1 - V_o - V_2)^2 \] (2.6)

Equations (2.4) and (2.6) both represent the total electrostatic energy of the system and therefore they are equal. Equating similar terms in these two equations, the value of the six lumped capacitors can be found based on the static capacitance. These capacitors are shown in Fig. 2.4(c), and the describing terms based on the static capacitance are presented in (2.7).

\[
C_{12} = C_{34} = \frac{-C_0}{6} \\
C_{13} = C_{24} = \frac{7C_0}{24} \\
C_{14} = C_{23} = \frac{5C_0}{24}
\] (2.7)

A similar analysis can be done for a case where the direction of the layers is the same. Figure 2.5(a) shows two overlapping layers that have the same direction. This condition usually occurs when the overlapping layers belong to the same winding (i.e., both belong to either primary or secondary). To extract the capacitance model of this condition, the overlapping layers should be straightened and the voltage gradient between the layers should be preserved. Figure 2.5(b) shows these layers when they are straightened. The voltage distributions of these surfaces are presented in (2.8).

\[ V_y(x) = \frac{V_1}{L} x \quad \quad \quad V_b(x) = V_3 + \frac{V_2}{L} x \] (2.8)

When the voltage distribution is known, the electrostatic energy of the system can be found. Following the
Figure 2.5: Electrostatic behavior model of two overlapping layers that belong to the same windings: a) 3D model of the system along terminals and voltage directions, b) the overlapping layers are straightened while the voltage gradient between overlapping layers is preserved, c) the electrostatic model of the system and d) the electrostatic model of the system if the overlapping layers are the successive turns of the same winding.

same procedure that was used in the previous case, the capacitive model of this condition is shown in Fig. 2.5 (c), and the describing terms based on the static capacitance are presented in (2.9).

\[
\begin{align*}
C_{12} &= C_{34} = -\frac{C_0}{6} \\
C_{13} &= C_{24} = \frac{C_0}{3} \\
C_{14} &= C_{23} = \frac{C_0}{6}
\end{align*}
\]  

(2.9)

If the layers of Fig. 2.5 (a) are successive layers of the same winding, points 2 and 3 are connected and the capacitance model can be simplified. Under this condition, the equivalent capacitance between point 1 (start of the first layer) and point 4 (end of the second layer) is equal to \( \frac{C_0}{4} \), as shown in Fig. 2.5 (d).

After developing the parasitic capacitance model for two overlapping layers, the parasitic capacitance model of two layers should be extended to a complete transformer. Figure 2.6 (a) shows a PT with an interleaved structure. \( V_1 \) and \( V_2 \) are the voltage between the beginning of the first turn and the end of the last turn of the primary and secondary windings, respectively. The parasitic capacitance model of one intersection of primary and secondary is shown in Fig. 2.6 (b), which is similar to the parasitic capacitance model of Fig. 2.4 (c). In this figure, every layer is shown with a grey rectangle, and a series connection of these rectangles constitutes the winding. As shown in Figs. 2.6 (a) and (b), there are two terminals for each layer (one at the beginning of the layer and one at the end), and each of these terminals experiences a different pulsating voltage. The voltage waveforms at the terminals of each layer depend on the position of that layer.

In order to transfer the capacitance model of Fig. 2.6 (b) to the terminals of transformer (Fig. 2.6 (c)), one of the transformer terminals in each side is selected as a reference point. For the case that is presented in Fig. 2.6 (b), the voltages at the terminals of primary layer are equal to \( bV_1 \) and \( aV_1 \), where \( b \) and \( a \)
are defined as a ratio of the voltages at these terminals to the total voltage of primary. For instance, if the
winding has eight turns, the values of $a$ and $b$ for the third turn (layer) of the winding are equal to $3/8$ and $2/8$,
respectively. These values for the last turn are equal to $8/8=1$ and $7/8$. A similar explanation is considered
ture for the parameters $c$ and $d$ on the secondary side. These parameters represent the ratio of the voltages at
the terminals of each secondary layer to the total voltage of secondary. Given this definition, it is possible to
use the energy method to transfer the parasitic capacitance network of each overlapping to the terminals of
the transformer, as shown in Fig. 2.6 (c). This can be done by considering that the total electrostatic energies
of Fig. 2.6 (b) and (c) are equal. The total energy of Fig. 2.6 (b) is presented in (2.10).

$$W_t = -\frac{1}{2} C_0 (aV_1 - bV_1)^2 - \frac{1}{2} C_0 (cV_2 - dV_2)^2 + \frac{1}{2} C_0 (bV_1 - dV_2 - V_o)^2
+ \frac{1}{2} C_0 (aV_1 - dV_2 - V_o)^2 + \frac{1}{2} C_0 (bV_1 - cV_2 - V_o)^2$$

This equation is equal to (2.6), which represents the total energy in Fig. 2.6 (c). Equating similar terms
in these equations provides the required equations for transferring the parasitic capacitance model of the
overlapping to the winding terminals. These equations are presented in Table 2.1 and show that the values
of transferred capacitors depend on the parameters $a$, $b$, $c$, and $d$, which are determined by layers that
are overlapping. The transfer equations presented in Table 2.1 should be used to transfer the parasitic
capacitance network of each overlapping to the terminals of the transformer. Once this is done for all the intersections, there will be six different groups of capacitors that are connected between the terminals of the transformer. Each group consists of several capacitors that are connected in parallel. Under this condition, the equivalent capacitance of each group can be found by adding the capacitors of that group, as all capacitors in each group are connected in parallel. For example, the equivalent parasitic capacitance between terminal 1 and terminal 3 of the transformer in Fig. 2.6 (b) is equal to the sum of all transferred parasitic capacitances that are connected between these terminals. Therefore, in the end, there would be only six capacitors between the terminals of the transformer, which is equal to the six-capacitor model of the transformer. In the next chapter, equations in Table 2.1 will be used to validate the concept of “paired layers”.

**Table 2.1:** Equations for transferring the distributed capacitances to the transformer terminals

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Transfer Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{13}$</td>
<td>$\frac{C_0}{24} [5ad + 7bd + 7ac + 5bc]$</td>
</tr>
<tr>
<td>$C_{14}$</td>
<td>$\frac{C_0}{24} [12a + 12b - 5ad - 7bd - 7ac - 5bc]$</td>
</tr>
<tr>
<td>$C_{23}$</td>
<td>$\frac{C_0}{24} [12c + 12d - 5ad - 7bd - 7ac - 5bc]$</td>
</tr>
<tr>
<td>$C_{24}$</td>
<td>$\frac{C_0}{24} [24 + 5ad + 7bd + 7ac + 5bc - 12a - 12b - 12c - 12d]$</td>
</tr>
<tr>
<td>$C_{12}$</td>
<td>$\frac{C_0}{24} [8a^2 + 8b^2 + 8ab - 12a - 12b]$</td>
</tr>
<tr>
<td>$C_{34}$</td>
<td>$\frac{C_0}{24} [8c^2 + 8d^2 + 8cdb - 12c - 12d]$</td>
</tr>
</tbody>
</table>

### 2.3 Case 2: Parasitic Capacitance Modeling of Symmetrical Overlapping

One special case that will be used in the next chapter to develop the concept of “paired layers” is when the intersection is symmetrical. Figure 2.7 shows this condition. When the intersection is symmetrical, the overlapping layers have the same number of turns, the same PCB layout and are only rotated by 180 degrees around the core center leg. Due to symmetry, one can say that the following equations are valid.

$$C_{ad} = C_{bc} \quad , \quad C_{ab} = C_{cd} \quad (2.11)$$

This relationship is also true for the case of single-turn layers that were presented in section 2.2, as overlapping of single-turn layers also is symmetrical. Although (2.11) does not give the exact equation for individual capacitor values, this relationship can be used to find a solution to cancel the adverse effect of parasitic capacitances. This is discussed in detail in the next chapter.
Figure 2.7: a) A symmetrical overlapping of primary and secondary layers. b) Equivalent parasitic capacitance model for a symmetrical overlapping.

2.4 Equivalent Capacitance Model Extraction Using FEA

As discussed earlier, for transformers with multiple-turn overlapping layers such as Fig. 2.2, finding a general analytical solution is not possible and results in complicate and non-insightful equations. Numerical methods such as FEA can be used to extract the equivalent parasitic capacitance for these cases. This is discussed in this section.

While the transformer is a two-port system from the magnetostatic perspective, the inter-winding capacitance between primary and secondary winding provides a path between primary and secondary, making the transformer a three-port system from the electrostatic standpoint [90]. For a three-port system, three independent voltages and six capacitors are needed to model the electrostatic behavior of the system. Figure 2.8 (a) shows one way of selecting the independent voltages and the six-capacitor model of the transformer.

The total energy of the system can be found by summing energies of lumped capacitors. Under this

Figure 2.8: Electrostatic behavior model of the transformer: (a) Six-capacitor model with three independent voltages, (b), (c), and (d) the required numerical analysis to find six-capacitor model.
condition, the total energy of the system is equal to (2.12).

\[ W_t = \frac{1}{2} C_{12} V_1^2 + \frac{1}{2} C_{34} V_2^2 + \frac{1}{2} C_{14} (V_1 - V_o)^2 + \frac{1}{2} C_{23} (V_2 + V_o)^2 + \frac{1}{2} C_{13} (V_1 - V_o - V_2)^2 \] (2.12)

By rearranging (2.12) based on voltages, (2.13) can be obtained.

\[ W_t = \frac{1}{2} (C_{12} + C_{14} + C_{13}) V_1^2 + \frac{1}{2} (C_{34} + C_{23} + C_{13}) V_2^2 + \frac{1}{2} (C_{24} + C_{14} + C_{23} + C_{13}) V_o^2 \]

\[ + (-C_{14} - C_{13}) V_1 V_o + (C_{23} + C_{13}) V_2 V_o + (-C_{13}) V_1 V_2 \] (2.13)

The total energy of the system also can be computed using electric fields. Since Maxwell’s equations are linear, they satisfy the superposition principle. In a system with three independent voltages, like the one in Fig. 2.8 (a), the total electric field is equal to the sum of \( \vec{E}_1, \vec{E}_2, \) and \( \vec{E}_o, \) corresponding to the voltages \( V_1, V_2, \) and \( V_o. \) Therefore, the total electric field and electric displacement field in the system can be written as follows:

\[ \vec{E}_t = \vec{E}_1 + \vec{E}_2 + \vec{E}_o \]
\[ \vec{D}_t = \vec{D}_1 + \vec{D}_2 + \vec{D}_o \] (2.14)

The total electrostatic potential energy may be expressed in terms of these fields in the form of following equation:

\[ W_t = \frac{1}{2} \oint_V (\vec{E}_1 + \vec{E}_2 + \vec{E}_o) \cdot (\vec{D}_1 + \vec{D}_2 + \vec{D}_o) dV = \frac{1}{2} \oint_V \vec{E}_1 \cdot \vec{D}_1 + \frac{1}{2} \oint_V \vec{E}_2 \cdot \vec{D}_2 dV + \frac{1}{2} \oint_V \vec{E}_o \cdot \vec{D}_o dV \]
\[ + \frac{1}{2} \oint_V (\vec{E}_1 \cdot \vec{D}_2 + \vec{E}_2 \cdot \vec{D}_1) dV + \frac{1}{2} \oint_V (\vec{E}_1 \cdot \vec{D}_o + \vec{E}_o \cdot \vec{D}_1) dV + \frac{1}{2} \oint_V (\vec{E}_2 \cdot \vec{D}_o + \vec{E}_o \cdot \vec{D}_2) dV \] (2.15)

Numerical methods like FEA can be employed to calculate the energy using (2.15). Three different analyses are required to find the six-capacitor model and they are presented in Figs. 2.8 (b), (c) and, (d). The cases presented in Fig. 2.8 (b) and (c) require a linear voltage distribution on the turns of one winding, and zero voltage on all the turns of the other winding. The linear distribution of the voltage on the turns of one side is signified by a triangle next to that winding. The analysis performed in Fig. 2.8 (d) requires a constant voltage on all turns of the secondary side and zero voltage on all turns of the primary side. The constant voltage on all turns of the secondary side also is signified by a rectangle next to that winding, which shows that there is no voltage difference between the terminals of the secondary side. Obtaining the values of the first three terms in (2.15) are straightforward. The total electrostatic energy in Figs. 2.8 (b), (c) and (d) are equal to the first, second, and, third terms, respectively. The remaining three components are found using the superposition theorem.
Similar to (2.13), equation (2.15) indicates that the total energy is composed of six components. Equating corresponding terms in (2.15) and (2.13), expressions for finding six capacitors are presented in Table 2.2. Among six capacitors, \(C_{13}, C_{14}, C_{23}, \) and \(C_{24}\) are inter-winding capacitances and \(C_{12}\) and \(C_{24}\) model the intra-winding capacitances of windings. As mentioned before, reducing the inter-winding capacitances can significantly attenuate CM noise and enhance the performance of the converter.

Table 2.2: Equations describing parasitic capacitances based on field analysis

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>(C_{13})</td>
<td>(\frac{1}{2\pi V_1} \int \vec{E}_1 \cdot \vec{D}_2 dV + \vec{E}_2 \cdot \vec{D}_1 dV)</td>
</tr>
<tr>
<td>(C_{14})</td>
<td>(\frac{1}{2\pi V_1} \int \vec{E}_1 \cdot \vec{D}_o + \vec{E}_o \cdot \vec{D}<em>1 dV - C</em>{13})</td>
</tr>
<tr>
<td>(C_{23})</td>
<td>(\frac{1}{2\pi V_o} \int \vec{E}_2 \cdot \vec{D}_o + \vec{E}_o \cdot \vec{D}<em>2 dV - C</em>{13})</td>
</tr>
<tr>
<td>(C_{12})</td>
<td>(\frac{1}{V_2} \int \vec{E}<em>1 \cdot \vec{D}<em>1 dV - C</em>{14} - C</em>{13})</td>
</tr>
<tr>
<td>(C_{34})</td>
<td>(\frac{1}{V_2} \int \vec{E}<em>2 \cdot \vec{D}<em>2 dV - C</em>{13} - C</em>{23})</td>
</tr>
<tr>
<td>(C_{24})</td>
<td>(\frac{1}{V_2} \int \vec{E}<em>o \cdot \vec{D}<em>o dV - C</em>{13} - C</em>{23} - C_{14})</td>
</tr>
</tbody>
</table>

2.5 **Equivalent Capacitance Model Extraction Using Measurement**

The value of lumped capacitors of equivalent circuit can be measured using six different impedance measurements. There are four ports and different measurement configurations are possible to extract the six-capacitor model. The measurement can be done between any two ports, and also ports can be connected together. An important criterion in selecting measurement configuration is that the resulting circuit should not have any two capacitors in series. In other words, in a right configuration, all capacitors are in parallel. Otherwise, it produces wrong results. Six different measurements of Fig. 2.9 satisfy this requirement and can give six equations to find the value of six capacitors. For example, the equivalent capacitance measured in Fig. 2.9 (a) is equal to \(C_{13} + C_{14} + C_{23} + C_{24}\) and there is no series connection of capacitors. Equivalent capacitance of each measurement is presented in (2.16).

\[
\begin{align*}
C_{M1} &= (C_{13} + C_{14} + C_{23} + C_{24}) \\
C_{M2} &= (C_{34} + C_{13} + C_{23}) \\
C_{M3} &= (C_{12} + C_{13} + C_{14}) \\
C_{M4} &= (C_{12} + C_{24} + C_{23}) \\
C_{M5} &= (C_{34} + C_{14} + C_{24}) \\
C_{M6} &= (C_{12} + C_{23} + C_{14} + C_{34})
\end{align*}
\]  

Having the equivalent capacitance of each measurement, the value of each capacitor is found based on
Figure 2.9: Six different measurements to establish transformer’s six capacitance model (a) $M_1$, (b) $M_2$, (c) $M_3$, (d) $M_4$, (e) $M_5$, and (f) $M_6$

d the measurements and is presented in (2.17).

\[
\begin{align*}
C_{12} &= \frac{1}{2} (C_{M3} - C_{M1} + C_{M4}) \\
C_{13} &= \frac{1}{2} (C_{M2} + C_{M3} - C_{M6}) \\
C_{14} &= \frac{1}{2} (C_{M1} - C_{M2} - C_{M4} + C_{M6}) \\
C_{23} &= \frac{1}{2} (C_{M1} - C_{M3} - C_{M5} + C_{M6}) \\
C_{34} &= \frac{1}{2} (C_{M2} - C_{M1} + C_{M5})
\end{align*}
\]

(2.17)

2.6 Validation of the Proposed Parasitic Capacitance Model

In this section, FEA simulations and experimental measurements are used to validate the proposed parasitic capacitance model. The verification starts with a model of double layer PCB and then extends to the case of a simple PT with four double-layer PCBs.

Fig. 2.10 (a) shows a double-layer PCB with one turn on each side. As shown in Fig. 2.10 (b), the capacitance between the top and bottom layers are called static capacitance, $C_1$. The value of this capacitor can be found by using the formula of the parallel plate capacitor, as shown in (2.18).

\[
C_0 = \varepsilon_0 \varepsilon_r \frac{A}{d} = (8.85 \times 10^{-12}) \times (4) \times \frac{(11.5 \times 10^{-4})}{0.66 \times 10^{-3}} = 62pF
\]

(2.18)

The area is found using the PCB design software and $d$ is the thickness of PCB used. Due to the fringing of E-field, the actual value of this capacitance is slightly higher than the calculated value. To consider the fringing effect, the static capacitance between the top and bottom layers is also found using FEA. Figure 2.10 (c) shows E-field between the top and bottom layers and the simulation result for the static capacitance is
Figure 2.10: a) A double-layer PCB with one turn on each side. b) Definition of static capacitance between top and bottom layers, $C_1$. c) E-field distribution showing fringing of E-field.

equal to 66pF. This capacitance is called $C_1$ in this section. This was expected as the fringing of the electric field slightly increases the overlapping area.

As analytically proven in section 2.2 and shown in Fig. 2.5 if the overlapping turns are successive turns of the same winding, their equivalent parasitic capacitance from the start of the top turn to the end of the bottom turn is equal to one-fourth of the static capacitance. To verify this, the equivalent capacitance from point a in Fig. 2.11 to point b in Fig. 2.11 was found using FEA. One volt was applied between the start of the top turn and the end of the bottom turn. The total energy was equated to the energy stored in the self-capacitance and so the value of equivalent capacitance was found. Using this method, the value of equivalent capacitance between points a and b is equal to 16pF, which is almost one-fourth of static capacitance between the top and bottom layers (66pF/4=16.5pF) found using FEA. This PCB layout also has been measured experimentally to validate the model. Figure 2.11 (b) shows the prototype of this PCB and the impedance of this layout is presented in Fig. 2.11 (c). The measured capacitance value is equal to 15.8pF which is in a good agreement with the simulated value (16pF) and calculated value (15.5pF).

Figure 2.11: Finding equivalent capacitance from point a to point b. a) Voltage distribution on turns, b) prototype of the PCB and c) frequency response of the prototype.
Figure 2.12: a) FEA model of PT under study and b) the prototype of PT. The turns ratio is 4:2. Each PCB has two turns and secondary PCBs are connected in parallel.

After verifying the model for the single PCB, now a simple PT structure is used to validate the proposed parasitic capacitance model. Figures 2.12(a) and (b) show the FEA model and physical prototype of this PT, respectively. The turns ratio is 4 : 2 and each PCB has two turns (one on the top layer and another one on the bottom layer). Secondary PCBs are in parallel and are placed between primary layers. The distance between PCBs is 0.83mm and the material between them is air.

Fig. 2.13 (a) shows the structure of the transformer. As shown in Fig. 2.13 (a), there are seven overlappings between layers in this structure (indicated by OV1 to OV7). OV1, OV3, OV5, and OV7 are the overlapping between the top and bottom layers of the same PCB. Therefore, the parasitic model from the start of the top turn to the end of the bottom turn is equal to one-fourth of static capacitance (as discussed in 2.10). For OV2, OV4, and OV6, the material between overlapping layers is air and the distance is 0.83mm. This results in a static capacitance value of 17.86pF. This capacitance is called $C_0$ in the following parts. OV4 is the overlapping between successive turns of the same winding, so its parasitic capacitance model is equal to one-fourth of static capacitance. However, for this case, the static capacitance is $C_0$. OV2 and OV6 are the overlappings between layers of different windings. Therefore, they need six capacitors to model their capacitive behavior. Fig. 2.13 (b) shows the parasitic capacitance model of this PT. Color coding is used in this figure and the parasitic capacitance model of each overlapping is shown with the same color as it was indicated in Fig. 2.13 (a). The capacitance model of OV2 is shown with a purple color. This capacitance model is similar to the capacitance model developed in section 2.2 and shown in Fig. 2.4 (c). Similarly, modeling OV6 requires six capacitors, and it is shown with brown capacitors in this figure. To
Figure 2.13: Analytical derivation of parasitic capacitance. a) PT arrangement which has 7 different overlappings, b) distributed capacitance model of PT, c) distributed parasitic capacitance of PT transferred to the terminals and d) six-capacitor model of PT.

To validate the parasitic capacitance model of Fig. 2.13 (d), FEA was used to extract the value of each lumped capacitor. As explained in section 2.4, three different analyses are needed to do so. The results
Figure 2.14: Extracting parasitic capacitance model using FEA: a), b) and c) Simulations required to find the model. d) Extracted six-capacitor model.

of these three analyses should be used according to the formulas provided in Table. 2.2 to extract the six-capacitor model. Figures 2.14 (a), (b) and (c) show these three analysis. Figure 2.14 (d) shows the extracted parasitic capacitance model of PT using FEA, which is in great agreement with the analytical model.

Finally, measurements were done to characterize the PT under study, and extract the six-capacitor model of PT. Configurations presented in Fig. 2.9 was used to find the capacitance model. Figure 2.15 (a) shows the frequency response of the first configuration. Figure 2.15 (b) shows the value of measured capacitance in all configurations. These measurements are used in equations provided in (2.17) to find the six-capacitor model of the transformer, which is presented in Fig. 2.15 (c).

Comparing the proposed equivalent parasitic capacitance model of Fig. 2.13 (d) with models found using FEA and experimental tests (Fig. 2.14 (d) and Fig. 2.15 (c)) shows that the proposed parasitic capacitance model accurately predicts the lumped capacitance model of the transformer. This was expected, as the proposed equivalent capacitance circuit is developed using mathematical analysis and no assumptions or simplifications were made.
Figure 2.15: Experimental tests to extract the parasitic capacitance model: a) Frequency response of one of the tests, b) measurements configurations and measured capacitance values and c) parasitic capacitance of PT

2.7 Summary

Parasitic capacitance in PTs has a distributed nature and exists whenever two layers overlap. The net effect of parasitic capacitance can be expressed using the equivalent six-capacitor model. In this chapter, a methodology for extracting the six-capacitor model of PTs was presented based on the energy method. Using this methodology, general equations relating the distributed capacitance of layers to the six-capacitor model of the transformer were derived. These equations show how the winding arrangement affects the six-capacitor model and provide a deep insight into how changing the winding arrangement can manipulate the value of each lumped capacitor. Two special cases of PTs were considered, and analytical equations were derived for each case. In addition to the proposed analytical model, methodologies for extracting the six-capacitor model using FEA and experimental measurements were proposed. Finally, the proposed capacitance model has been verified using FEA and experimental characterization. This model is used in the next chapters to address the root cause of CM noise problems in power converters.
Chapter 3

The Concept of Paired Layers

With the overgrowing demand in applications that require slim-profile power supplies, such as LED drivers, consumer electronics (laptops, flat-panel TVs) [91], and servers [92], the use of PTs has attracted attention [6, 31, 77–79, 81, 83, 86]. Despite many desirable features of PTs, their large inter-winding capacitance generates large amounts of CM noise which creates serious EMI problems. Attenuating large amounts of noise requires large CM chokes which increases the cost and reduces the power density of the converter. The large CM noise of PTs is a severe technical challenge that remains unresolved. The objective of this section is to find a solution that allows us to design PTs that have almost zero CM noise generation.

In the previous chapter, a detailed parasitic capacitance model of PTs was proposed which describes how the winding arrangement affects the six-capacitor model of the transformer. This model is used in this section to find a solution for the large CM noise of PTs. CM noise in the transformer originates from an undesired electrostatic coupling between primary and secondary windings and also between windings and the core. In PTs, whenever a layer of the primary winding overlaps with a layer of the secondary winding, due to the proximity and large overlapping area of planar layers, a large parasitic capacitance is formed between overlapping layers. A parasitic capacitance also is formed between the core and layers of windings that are exposed to the core. When the voltage of overlapping layers changes rapidly due to high-frequency switching, parasitic capacitance is exposed to a large $\frac{dv}{dt}$. This leads to the generation of pulsating currents (known as CM noise) that circulate in the circuit through the earth and create EMI problems [8]. Figure 3.1 (a) shows different sources of CM noise in a transformer. $I_{P-S}$ is the CM noise current that is generated when primary and secondary layers overlap and is the largest part of the transformer’s CM noise. As shown in Fig. 3.1 (a), this current circulates between primary and secondary sides through the earth and shows up in the

\[1\] Portions of this chapter have been published in [1–4]
Common-Mode Noise Generation in Planar Transformers

The Proposed Solution to Eliminate All Common-Mode Noise Sources

**Figure 3.1:** a) Transformer’s CM noise sources and their circulation path in the converter. $I_{P-S}$, $I_{P-C}$, $I_{P-C-S}$, and $I_{S-C}$ are shown with 1, 2, 3, and 4, respectively. Traditional interleaving methods only aim to reduce AC resistance and do not consider $\frac{dv}{dt}$ of overlapping layers which leads to very large levels of CM noise that imposes the use of large CM chokes. b) In the paired layers interleaving method, primary and secondary layers are designed in a way that their overlapping does not generate CM noise. The structure of the transformer also eliminates other CM noise sources and minimizes AC resistance.

standard EMI tests that are done at the input of the converter. The amount of $I_{P-S}$ depends on the structure of the transformer which determines the number of overlapping between primary and secondary layers. The structure of the transformer is also a determining factor in windings’ AC resistance. AC resistance is a factor of skin effect and proximity effect. More interleaved structures that are used to reduce the proximity effect and so minimize winding’s AC resistance significantly increase $I_{P-S}$, as they have multiple overlapping of
primary and secondary which results in a large inter-winding capacitance. The second noise source is $I_{p-C}$, which generates when a primary layer overlaps with the core. Figure 3.1 (a) shows that this current returns to the primary through the parasitic capacitance between the core and earth and appears in the standard EMI tests done at the input of the converter. The third noise source is $I_{p-C-S}$, which is the result of the indirect coupling of primary and secondary layers through the core. As shown in Fig. 3.1 (a), this current goes from primary to secondary (or vice-versa) through the core and returns to its source through the earth. This noise also shows up in the input EMI tests. Finally, the fourth source of noise in a transformer is $I_{s-C}$, which generates when a secondary layer overlaps with the core. This noise then returns to the secondary through the earth and does not appear in the input of the converter. Therefore, it does not affect the results of standard EMI tests of the converter. In order to effectively minimize the CM noise of the converter, $I_{p-S}$, $I_{p-C}$, and $I_{p-C-S}$ should be minimized. While traditional methods reduce AC resistance by interleaving primary and secondary layers, these methods do not consider CM noise sources in the transformer structure, resulting in large amounts of CM noise. To date, no method of interleaving has been proposed for PTs that can achieve both low AC resistance and very low CM noise generation.

This section aims to eliminate the CM noise by introducing the concept of paired layers. Figure 3.1 (b) shows the concept of the proposed method to eliminate different sources of CM noise in PTs. According to this figure, four-layer PCBs are used to make windings (it is also possible to use single-turn copper foil layers, and this is discussed later in the next chapter). $I_{p-S}$, which is the most significant part of the CM noise, is eliminated by a novel PCB winding layout which avoids CM noise generation when primary and secondary layers overlap. $I_{p-C}$ and $I_{p-C-S}$ can be eliminated by using simple criteria in the transformer structure that blocks the CM noise path from the primary to the core. These concepts are discussed in this section.

### 3.1 Eliminating CM Noise Due to the Direct Overlapping of Primary and Secondary Layers ($I_{p-S}$)

$I_{p-S}$ is the most significant part of the transformer’s CM noise and is generated when the primary and secondary layers overlap. Figure 3.2 (a) shows a typical condition that occurs when two layers of different windings overlap (i.e. one from the primary and the other from the secondary). As shown in Fig. 3.2 (a), depending on the turns ratio, overlapping layers can have a different number of turns. The electrostatic behavior of this overlapping can be modeled by six capacitors, as shown in Fig. 3.2 (b) (there are four terminals and one capacitor is needed between each pair of terminals). The total generated CM noise between
these layers can be found by adding the currents in capacitors $C_{ac}$, $C_{ad}$, $C_{bc}$, and $C_{bd}$ (capacitors $C_{ab}$ and $C_{cd}$ do not contribute to CM noise, as they are between layers of the same winding). CM noise currents in these capacitors are presented in (3.1).

$$i_{ac} = C_{ac} \left( \frac{dv_a}{dt} - \frac{dv_c}{dt} \right)$$

$$i_{ad} = C_{ad} \left( \frac{dv_a}{dt} - \frac{dv_d}{dt} \right)$$

$$i_{bc} = C_{bc} \left( \frac{dv_b}{dt} - \frac{dv_c}{dt} \right)$$

$$i_{bd} = C_{bd} \left( \frac{dv_b}{dt} - \frac{dv_d}{dt} \right)$$

(3.1)

Considering these equations, the total generated CM noise can be calculated using (3.2).

$$i_{CM} = i_{ac} + i_{ad} + i_{bc} + i_{bd} = C_{ac} \left( \frac{dv_a}{dt} - \frac{dv_c}{dt} \right) + C_{ad} \left( \frac{dv_a}{dt} - \frac{dv_d}{dt} \right) + C_{bc} \left( \frac{dv_b}{dt} - \frac{dv_c}{dt} \right) + C_{bd} \left( \frac{dv_b}{dt} - \frac{dv_d}{dt} \right)$$

(3.2)

In order to achieve zero CM noise generation between overlapping layers, a condition must be found that makes (3.2) equal to zero. Equation (3.2) shows that the amount of CM noise depends on both the values of $\frac{dv}{dt}$ and capacitors. Both of these factors should be considered to find a condition for making total CM noise equal to zero. The first required condition affects $\frac{dv}{dt}$ of overlapping layers and is presented in (3.3).

$$\frac{dv_a}{dt} = \frac{dv_c}{dt}, \quad \frac{dv_b}{dt} = \frac{dv_d}{dt}$$

(3.3)

**Figure 3.2:** CM noise generation when primary and secondary layers overlap. a) Physical presentation of the overlapping and, b) equivalent parasitic capacitance model which shows how CM noise is generated.
In order to achieve these equalities, two conditions should be met. First, the overlapping layers should have
the same number of turns and, second, the \( \frac{dv}{dt} \) at the ports of overlapping layers should be similar, which can
only happen if specific turns of primary and secondary overlap. By considering (3.3), two terms in (3.2) are
eliminated and (3.2) is reduced to (3.4).

\[
\frac{dv_a}{dt} \quad \text{and} \quad \frac{dv_b}{dt} \quad \text{both belong to the same winding and so cannot be equal, as it is not possible that two}
\text{points of the same winding have similar } \frac{dv}{dt}. \quad \text{Therefore, the only option for making (3.4) equal to zero is to}
\text{have } C_{ad} \text{ and } C_{bc} \text{ equal. As discussed in the previous chapter, parasitic capacitance is distributed in its nature,}
\text{and the six lumped capacitors equivalent circuit of Fig. 3.2 (b) only models the total effect of distributed}
\text{capacitance. The value of lumped capacitors can be found by equating the total energy of the overlapping}
\text{with the energy of the six-capacitor model. This method was used in section 2.2 for overlapping of single-}
\text{turn layers, and the results provided simple and insightful equations for each lumped capacitor. However, in}
\text{the case of overlapping layers with multiple turns, it is not possible to find a simple and insightful equation}
\text{for lumped capacitors. Since the value of } C_{ad} \text{ and } C_{bc} \text{ is not important and it is only required that they to be}
\text{equal, symmetry can be used to make this happen. When the overlapping layers are symmetrical, they have}
\text{the same number of turns, the same PCB layout and are only rotated by 180 degree around the core center}
\text{leg. Figure 3.3 (a) shows a symmetrical overlapping of primary and secondary layers. Due to symmetry, one}
can say that the following equation is valid.}

\[
C_{ad} = C_{bc} \quad \text{(3.5)}
\]

The general equivalent parasitic capacitance of this overlapping is shown in Fig. 3.3 (b).

It should be remembered that the overlapping layers could be multi-turn or single-turn and as long as they
have symmetrical layouts, (3.5) would be valid. This relationship was proven mathematically for the case
of single turn overlapping in the previous section. Based on the analysis provided in the previous chapter,
the overlapping of single-turn layers and its equivalent parasitic capacitance model are shown in Fig. 3.4.
According to this figure, the relationship between inter-winding capacitors are presented in (3.6).

\[
C_{ad} = C_{bc} = \frac{5C_0}{24}, \quad C_{ac} = C_{bd} = \frac{7C_0}{24} \quad \text{(3.6)}
\]
Figure 3.3: a) Symmetrical overlapping and b) equivalent parasitic capacitance model of the overlapping.

Where $C_0$ is presented in (3.7).

$$C_0 = \varepsilon_0 \varepsilon_r \frac{W \times L}{d} \quad (3.7)$$

Satisfying (3.3) and (3.5) is the required condition to make CM noise equal to zero in (3.4). Figure 3.5 shows an overlapping of two layers of similar design that have similar $\frac{dv}{dt}$ on their ports and so generate zero CM noise.

From the above discussion, the overlapping layers must have the same number of turns and the same PCB layout. They can be single-turn or multiple-turn and be made using PCB or copper foil. Besides, the overlapping layers should have a similar $\frac{dv}{dt}$ on their ports to satisfy (3.3). It means that only certain turns

Figure 3.4: a) Overlapping of single-turn layers as an example of symmetrical overlapping and b) equivalent capacitance circuit of the overlapping.
of primary and secondary are allowed to overlap and other turns should never meet any part of the other winding. Turns that are allowed to overlap are called paired turns in this document. The first step in building such a winding structure is finding paired turns in primary and secondary. Finding paired turns depends on the transformer’s voltage distribution and paired turns of one topology are not necessarily paired in another topology. It is important to note that paired layers interleaving is only applicable if there is a quiet point in the primary side. On this basis, three different groups of topologies are considered as follows:

1. Topologies with a quiet point at one terminal of each winding. Examples of this are Flyback and Forward converters.

2. Topologies with a quiet point at one terminal of primary and a quiet point on the middle turn of the secondary. Converters with half-bridge inverter fall in this category.

3. Topologies with a quiet point in the middle of both primary and secondary winding. The push-pull converter is an example of this type of converters.

In the next section, these three groups of topologies along their various configurations are considered and paired turns are found for them. These paired turns (layers) are used in the next chapter to implement the paired-layers interleaving method.
3.2 Paired Turns in Topologies With a Quiet Point at One Terminal of Each Winding

The first category of converters encompasses topologies that have a quiet point on one terminal of each winding. Flyback and Forward converters are two well-known examples of these topologies. In both of these topologies, one terminal of the primary winding is directly connected to the DC bus and has a quiet voltage. One terminal of the secondary also is connected to secondary ground and has a quiet potential. These topologies can be realized using two different configurations on the secondary side and it will be shown that only one of these configurations allows us to find paired turns. These topologies, their different configurations, and a methodology to find paired turns in them are topics of this subsection.

3.2.1 Paired Turns in Flyback Converters

Flyback is a commonly used low-cost topology for low power isolated applications [98–100]. The efficiency, performance, power-density, and form factor of this topology highly depends on the characteristics of the transformer, which is a key part of this converter. Fig. 3.6 (a) shows the topology of a Flyback converter and provides a list of important challenges in designing high-efficiency, high power-density Flyback converters. The transformer leakage inductance significantly affects the performance of the Flyback converter. Large leakage inductances that are present in the traditional wire-wound transformers cause large voltage spikes on the switch, leading to the selection of switches with higher rated voltage. Besides, a large voltage spike creates large $\frac{dv}{dt}$ which creates CM noise in the switch parasitic capacitance [101] and transformer’s interwinding capacitance. The transformer form factor also significantly affects the overall height and size of the converter as usually, it is the tallest and bulkiest part of the circuit along with the output capacitor. Due to their high height, traditional cores cannot be used in certain low profile applications like Flat TVs or portable devices. Higher height also is a disadvantage from the heat transfer point of view, as it leads to high thermal resistance. Figure 3.6 (b) summarizes the aforementioned drawbacks of wire-wound transformers. Some of these problems can be resolved using planar transformers (PT), which are well suited to slim-profile power converters. They provide extremely low leakage inductances that cannot be attained using traditional wire-wound transformers and elaborated interleaved structures can be implemented easily in PTs in such a way as to minimize leakage inductance[9, 85].

Despite these advantages, PTs have extremely high inter-winding parasitic capacitance, due to the proximity of the layers and their significant overlap, and this generates large levels of Common-Mode noise leading to serious EMI problems [6–8, 46–48, 94–96]. As discussed in previous chapters, CM noise is created
**Challenges:**

1. EMI
2. Efficiency
3. Form Factor
4. Heat Extraction

---

**Transformer Effects:**

Inter-winding Capacitance

- EMI (CM noise)

Leakage Inductance

- EMI (Large dv/dt over switch)
- Efficiency (Snubber Loss)

---

**Wire-Wound Transformer**

- Large (dv/dt) as a result of High profile
- Large area for heat extraction
- Large Levels CM noise

**Proposed PT**

- Small (dv/dt) as a result of Low profile
- Extremely low levels of CM noise
- Excellent Heat extraction capability

---

**Figure 3.6:** a) Topology of Flyback converter along with important challenges in designing power Converters. Leakage inductance and transformer parasitic capacitance are major causes of CM noise. b) The main drawbacks of wire-wound transformer including high levels of noise, high leakage inductance, high height, and high thermal resistance. c) The problems of traditional transformers can be resolved using the proposed PTs which not only have very low leakage inductance but also generate almost zero levels of CM noise.

by displacement currents that flow from the voltage pulsating nodes in the circuit to the protective earth (PE) though parasitic capacitors [8]. Figure 3.6 (a) shows how CM noise currents are generated in the parasitic capacitors and circulate in the circuit. According to this figure, transformer inter-winding capacitors play a major role in CM noise generation. These parasitic capacitors not only generate CM noise but also provide a path for secondary side parasitic capacitors and lead to the generation of CM noise currents in these parasitic capacitors. While interleaved structures that have many intersections between primary and secondary windings can significantly reduce leakage inductance and enhance the efficiency of the transformer, they also lead to very large parasitic capacitance, which increases the level of CM noise generated. Higher levels
of CM noise require more attenuation to comply with standards and regulations, and this requires the use of larger CM choke filters at the input of the converter. The goal of paired layers interleaving is to eliminate this trade-off and attain interleaved PTs that not only have a low leakage inductance but also have no generation of CM noise.

To find paired turns in the transformer of a Flyback converter and achieve no generation of CM noise, the converter should be realized using the right configuration. The transformer of a Flyback converter has a static terminal in each winding, which is not affected by the switching of the converter. The remaining two terminals have pulsating voltages that change relative to each other. In order to find turns that have similar $\frac{dv}{dt}$ (which are called paired turns in this document), the $\frac{dv}{dt}$ of pulsating terminals must have the same polarity. The polarity of $\frac{dv}{dt}$ of pulsating terminals depends on the configuration of the converter. In order to show how the configuration of the converter affects the polarity of $\frac{dv}{dt}$, Figs. 3.7 (a) and (b) show two possible configurations of a Flyback converter. As shown in this figure, the configuration of Fig. 3.7 (a) results in a condition in which the voltage of pulsating terminals move in the same direction. In other words, the polarity of $\frac{dv}{dt}$ in pulsating terminals of the primary and secondary is similar. Under this condition, it is possible to find turns in primary and secondary that have similar $\frac{dv}{dt}$ (paired turns). Another configuration of the Flyback converter can be realized by placing the diode in the return path, as shown in Fig. 3.7 (b). In this configuration, the voltages of pulsating terminals move in opposite directions (the polarity of $\frac{dv}{dt}$ in pulsating terminals of the primary and secondary is different). Therefore, it is impossible to find turns with a similar $\frac{dv}{dt}$. Therefore, it is essential to use the configuration of Fig. 3.7 (a) to implement paired-layers interleaving.

Fig. 3.8 shows the voltage distribution of windings in a Flyback converter with the configuration of Fig.

![Figure 3.7](image)

**Figure 3.7:** a) Flyback converter configuration with pulsating voltages that change in the same directions (right configuration) and b) Flyback converter configuration with pulsating voltages that change in opposite directions (wrong configuration)
Both primary and secondary have a static terminal and a pulsating terminal. The static terminal of the primary is connected to the DC bus and the pulsating terminal is connected to the switch. The terminal of the secondary that is directly connected to the output has static potential and the terminal that is connected to the diode has the pulsating voltage. Starting from the terminal with static voltage, the amplitude of voltage fluctuation increases after each turn and reaches its maximum at the other terminal. Based on this figure, one can say that the first turn after the static terminal of the primary has a similar $\frac{dv}{dt}$ as the first turn after the static terminal of the secondary. The same is true for the second turns of both windings and so on. The number of paired turns is similar to the number of turns of the winding with fewer turns. In order to avoid CM noise generation, the structure of the transformer should be designed in a way that only paired turns overlap. According to Fig. 3.8 (which shows the case for a step-down transformer), there are turns on the primary side that have no pair on the secondary and should not overlap with any of secondary turns.

By knowing the voltage distribution along windings, it is possible to identify turns with a similar $\frac{dv}{dt}$. Figure 3.9 shows paired turns for both step-up and step-down cases. The following guideline can be used to find paired turns:

1. The dot convention should be used to name primary and secondary turns. For the primary winding, the dot point is connected to the first turn $P(1)$ and the non-dot point is connected to the last turn of the primary, which is called $P(n1)$. Similarly, the secondary’s first turn $S(1)$ is connected to the dot point and the last turn $S(n2)$ is connected to the non-dot point.

2. Using the above convention, $P(1)$ is paired with $S(1)$, $P(2)$ is paired with $S(2)$, $P(3)$ is paired with $S(3)$

---

**Figure 3.8:** Windings’ voltage distribution in a Flyback converter with the configuration of Fig. 3.7 (b).
and so on. The number of paired layers is equal to $n_1$ or $n_2$, whichever is less.

3. By using the above convention, the dot point of both windings should be connected to the static point.

Fig. 3.10 shows paired turns in an 8 : 4 PT using single-turn copper foils. Under this condition, the first four turns of the primary are paired with the four turns of the secondary and so can overlap with them. The other four turns of the primary do not have a pair and so should be hidden from the secondary winding. Any structure that satisfies this requirement does not generate CM noise. A simple structure that only has overlapping between paired layers is shown in Fig. 3.10 (c). More complicated structures that utilize this concept are presented in the next chapter.
3.2.2 Paired Turns in Forward Converters

The forward converter is another popular Switch Mode Power Supply (SMPS) that is used for producing isolated and controlled DC voltage from the unregulated DC input supply. As in the case of Flyback converter the input DC supply is often derived after rectifying (and little filtering) of the utility AC voltage. The forward converter, when compared with the Flyback circuit, is generally more energy-efficient and is used for applications requiring little higher power output (in the range of 100 watts to 200 watts) [102–104]. However, the circuit topology, especially the output filtering circuit is not as simple as in the Flyback converter. The transformer used in the forward converter is desired to be an ideal transformer with no leakage fluxes, zero magnetizing current, and no losses. Interleaved PTs are a perfect solution to achieve low leakage inductance and AC resistance and at the same time enhance the form factor of the converter. However, as discussed earlier, interleaved PTs result in a large inter-winding capacitance that generates CM noise. To resolve this trade-off, the concept of paired turns (layers) has been proposed in this chapter that can be used to design interleaved structures that generate no CM noise. In other words, paired layers interleaving results in PTs that have the best of both worlds: low leakage inductance and AC resistance and also no CM noise generation.

In order to find paired turns in a Forward converter, the voltage distribution on the transformer’s windings should be investigated. Similar to the transformer of a Flyback converter, the transformer of a Forward converter has a static terminal in each winding which is not affected by the switching of the converter. The remaining two terminals have pulsating voltages that change relative to each other. In order to find turns that have similar $\frac{dv}{dt}$ (which are called paired-turns), it is required that the $\frac{dv}{dt}$ of pulsating terminals of primary and secondary windings have the same polarity. The polarity of $\frac{dv}{dt}$ of pulsating terminals depends on the configuration of the converter. Two possible configurations of the Forward converter are shown in Figs. 3.11 (a) and (b). For the Forward converter, the traditional configuration that is shown in Fig. 3.11 (a) cannot provide the required condition, as the pulsating voltages change in opposite directions. To resolve this issue, the diode $D_1$ and output filter inductance $L_f$ are moved to the return path, which is shown in Fig. 3.11 (b). In this configuration, the pulsating voltages change in the same direction and, therefore, the condition required for no CM noise generation is obtained.

Fig. 3.12 shows the voltage distribution of windings in a Forward converter with the configuration of Fig. 3.11 (b). The situation is very similar to Flyback Converter. Both primary and secondary have a static terminal and a pulsating terminal. The static terminal of the primary is connected to the DC bus and the pulsating terminal is connected to the switch. The ground of the secondary side is often connected to protective earth for safety and so has the static potential. The terminal of the secondary that is directly
**Figure 3.11:** a) Forward converter configuration with pulsating voltages that change in opposite directions (wrong configuration) and b) Forward converter configuration with pulsating voltages that change in the same direction (right configuration).

Connected to the output has static potential and the terminal that is connected to the diode has the pulsating voltage. Starting from the terminal with static voltage, the amplitude of voltage fluctuation increases after each turn and reaches its maximum at the other terminal. By knowing the voltage distribution along the windings, it is possible to identify turns with a similar \( \frac{dv}{dt} \). Figure 3.12 shows paired regions of windings for both step-up and step-down cases. Based on Fig. 3.12 the following guideline can be used to find paired turns:

1. The dot convention should be used to name primary and secondary turns. For the primary winding, the dot point is connected to the first turn \( P(1) \) and the non-dot point is connected to the last turn of the primary, which is called \( P(n1) \). Similarly, the secondary’s first turn \( S(1) \) is connected to the dot

**Figure 3.12:** Windings’ voltage distribution in a Forward converter with configuration of Fig. 3.11 (b).
point and the last turn $S(n2)$ is connected to the non-dot point.

2. Using the above convention, $P(1)$ is paired with $S(1)$, $P(2)$ is paired with $S(2)$, $P(3)$ is paired $S(3)$ and so on. The number of paired layers is equal to $n1$ or $n2$, whichever is less.

3. By using the above convention, the dot point of both windings should be connected to the static point.

Fig. 3.13 shows paired turns in an 8 : 4 PT using single-turn copper foils. Under this condition, the first four turns of the primary are paired with the first four turns of the secondary and so can overlap with them. The other four turns of the primary do not have a pair and so should be hidden from the secondary winding. Any structure that satisfies this requirement does not generate CM noise. A simple structure that only has overlapping between paired layers is shown in Fig. 3.13 (c). More complicated structures that utilize this concept are presented in the next chapter.

### 3.3 Paired Turns in Topologies With a Quiet Point at One Terminal of Primary

In the second category of converters, one terminal of the primary winding has a quiet point but none of the terminals of the secondary winding are quiet. Converters with half-bridge inverter and full-bridge/center-tapped rectifier fall under this category. For this type of converters, the configuration of the converter is not important and paired turns always can be found in primary and secondary. One famous example of this type of converters is half-bridge LLC resonant converter which will be considered in the next subsection and paired turns would be found for that.
3.3.1 Paired Turns in Half-Bridge LLC Resonant Converters

The LLC resonant converter is an excellent option for achieving high efficiency and power density [105-108]. This topology has several advantages including soft switching operation, high part-load efficiency, no-load voltage regulation, high gain range over narrow frequency variation, and its soft-switching operation [109-111]. Soft switching operation minimizes switching loss and reduces Electromagnetic Interference (EMI). Due to these benefits, this topology has been widely adopted in applications that have strict requirements regarding efficiency and power density [91, 92, 112]. With the overgrowing demand in applications that require slim-profile power supplies, such as Light-Emitting Diodes (LEDS) drivers, consumer electronics (laptops, flat panel TVs) [91] and, servers [92], the use of Planar Transformers (PT) in LLC resonant converters has attracted attention [6, 77-79, 81, 83, 86], as they are the solution for designing low-profile power converters. PTs also have several other advantages including low leakage inductance, repeatability and, low thermal resistance [5, 9, 10, 93]. However, in spite of all these benefits, traditional PTs present high levels of Common-Mode (CM) noise, a severe technical challenge that remains unresolved. In comparison to wire-wound transformers, PTs generate significantly larger Common-Mode (CM) noise which creates serious EMI problems [7, 8, 46-48, 94-96].

Fig. 3.14 shows the topology of a half-bridge LLC resonant converter along with the detailed model of the transformer. As discussed earlier, the requirement of minimizing AC resistance and leakage inductance is in contradiction with the requirement of minimizing inter-winding capacitance (shown with red color in the figure). Interleaved structures that reduce AC resistance and leakage inductance lead to large capacitive coupling between primary and secondary windings and result in large inter-winding capacitance. To resolve this trade-off, the idea of paired-layers interleaving is proposed in this document. In order to find paired turns in the half-bridge LLC resonant converter, it is essential to have a detailed look at the voltage waveforms.

Figure 3.14: Half-bridge LLC resonant converter considering transformer’s parasitic elements.
Fig. 3.15 shows voltage waveforms at different parts of the transformer in the LLC resonant converter. In the half-bridge LLC resonant converter, one terminal of the primary winding is connected to the negative terminal of the DC bus, so it has static potential that is not affected by the switching of the converter. The other terminal of the primary fluctuates between $V_1/2$ and $-V_1/2$ in each switching period, where $V_1$ is the primary voltage. By going from the static terminal to the other end of the primary winding, the amplitude of fluctuation increases after each turn, reaching its maximum at the other terminal of the winding (which is equal to $V_1$). Considering that the increment of voltage fluctuation after each turn is equal to $V_1/n_1$, the voltage waveform on different parts of the primary winding is shown in Fig. 3.15. This figure also shows that all parts of the winding have a similar polarity of $\frac{dv}{dt}$, which means that they all go up and down together. On the other hand, none of the secondary terminals have static potential, as both terminals have a square-shaped voltage waveform with a peak-to-peak amplitude of $V_2$, where $V_2$ is the voltage at secondary. However, the polarities of $\frac{dv}{dt}$ at the secondary terminals are the opposite. This means that when the upper terminal is $V_2/2$, the lower terminal is $-V_2/2$ and they both change polarity at the switching moment. Under this condition, the middle point of the secondary winding has a static potential, which is not affected by the switching of the converter. These conditions are presented in Fig. 3.15 which shows the voltage waveform along the secondary winding.

By knowing voltage distribution along windings, it is possible to identify turns with a similar $\frac{dv}{dt}$. According to Fig. 3.15, the secondary winding can be divided into two equal sections. The polarity of $\frac{dv}{dt}$ in half of

![Figure 3.15](image)

**Figure 3.15:** Finding primary and secondary turns with similar $\frac{dv}{dt}$ in LLC PTs. a) When $2 \times n_1$ is larger than $n_2$, and b) when $2 \times n_1$ is less than $n_2$. 

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the turns of the secondary is opposite to the polarity of $\frac{dv}{dt}$ in the primary turns. Therefore, it is impossible to find corresponding turns for these turns on the primary side. On the other hand, the polarity of $\frac{dv}{dt}$ on the turns of the other section is similar to the polarity of $\frac{dv}{dt}$ on the turns of the primary. So, it is possible to find paired layers for them in the primary. According to this figure, turns with a similar $\frac{dv}{dt}$ have equal distance from the static point of their windings. The above explanation can be formulated in the following steps to find turns with a similar $\frac{dv}{dt}$ on the primary and secondary windings.

1. The dot convention should be used to name primary and secondary turns. For the primary winding, the non-dot point is connected to the first turn $P(1)$ and the dot point is connected to the last turn of the primary, which is called $P(n1)$. For the secondary winding, the sequence is the opposite. This means that the secondary’s first turn $S(1)$ is connected to the dot point and the last turn $S(n2)$ is connected to the non-dot point.

2. Using the above convention, $P(1)$ is paired with $S(n2/2)$, $P(2)$ is paired with $S(n2/2 - 1)$, $P(3)$ is paired $S(n2/2 - 2)$ and so on. The number of paired layers is equal to $n2/2$ or $n1$, whichever is less.

3. The above convention is only valid if the non-dot terminal of the primary is connected to the quiet point (i.e. $-V_{DC}$).

The above explanations are also shown in Fig. 3.15. Figure 3.15 (a) shows the condition when $2n1$ is larger than $n2$. Under this condition, some of the primary turns cannot be matched with any of the secondary turns. Therefore, these turns also should not overlap with any part of the secondary winding. Figure 3.15 (b) shows the condition when $2n1$ is less than $n2$. Under this condition, all of the primary turns have a corresponding turn on the secondary that has a similar $\frac{dv}{dt}$. In order to achieve zero CM noise generation, the overlapping layers of primary and secondary should have the same number of turns and only consist of turns that have similar $\frac{dv}{dt}$. This should be considered when PCB layouts are designed and will be discussed in the next chapter.

Fig. 3.16 shows an 8 : 4 PT using single-turn copper foils. Under this condition, the first two turns of the primary are paired with two turns of the secondary and so can overlap with them. The other six turns of the primary and the other two turns of the secondary do not have a pair and so should be hidden from the other winding. A simple structure that only has overlapping between paired layers is shown in Fig. 3.16 (c). More complicated structures that utilize this concept are presented in the next chapter.
3.4 Paired Turns in Topologies With a Quiet Point at the Middle of Both Primary and Secondary Winding

The third category of converters consists of topologies that have a quiet point in the middle of primary and secondary windings. In these converters, both terminals of primary and secondary windings have pulsating voltages that move in opposite directions. One example of these topologies is the Push-Pull converter which will be studied in the next subsection and paired turns will be found for that.

3.4.1 Paired Turns in Push-Pull Converters

The Push-Pull isolated converter is illustrated in Fig. 3.17. This converter is used always with the low input voltage, high input current. It tends to exhibit low primary side conduction losses since at any given instant only one transistor is connected in series with the dc source $V_g$ [115]. The ability to operate with transistor duty cycles approaching unity also allows the turns ratio to be minimized, reducing the transistor currents. The push-pull converter is one of the few available galvanic isolated topologies in which both transistors are referred to primary ground, which makes it easier to drive them. Both primary and secondary windings are center-tapped and their center-tap is connected to the quiet points of primary and secondary. Both terminals in primary and secondary have pulsating voltages that move in opposite directions.

To find paired turns in the Push-Pull converter, it is essential to have a detailed look at the voltage waveforms present at different parts of the transformer. Figure 3.18 shows voltage waveforms at different parts of the transformer in the push-pull converter. Based on this figure, the following guideline can be used to find paired turns of primary and secondary.

1. The dot convention should be used to name primary and secondary turns. For the primary winding,
Figure 3.17: Push-Pull converter along voltage waveforms at terminals of the transformer.

The dot point is connected to the first turn $P(01)$ and the non-dot point is connected to the last turn of the primary, which is called $P(n1)$. For the secondary winding, the sequence is the same. This means that secondary’s first turn $S(01)$ is connected to the dot point and last turn $S(n2)$ is connected to the non-dot point.

2. Using the above convention, $P(n1/2)$ is paired with $S(n2/2 + 1)$, $P(n1/2 - 1)$ is paired with $S(n2/2 + 1)$.

Figure 3.18: Finding primary and secondary turns with similar $\frac{dv}{dt}$ in Push-Pull PTs. a) When $n1$ is larger than $n2$, and b) when $n1$ is less than $n2$. 

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Figure 3.19: Implementation of the method for an 8 : 4 Push-Pull PT using single-turn copper foils. 
(a) Primary and secondary layouts, b) paired layers of primary and secondary, and c) a simple 
structure for PT that satisfies the requirements of no CM noise generation.

2), \(P(n1/2 - 2)\) is paired \(S(n2/2 + 2)\) and so on. In addition, \(P(n1/2 + 1)\) is paired with \(S(n2/2)\), 
\(P(n1/2 + 2)\) is paired \(S(n2/2 - 1)\) and so on. The number of paired layers is equal to \(n2\) or \(n1\), 
whichever is less.

Fig. 3.19 shows an 8 : 4 Push-Pull PT using single-turn copper foils. Figure 3.19 (b) shows paired turns 
of primary and secondary which are found using the above guidelines. A simple structure that only has 
overlapping between paired layers is shown in Fig. 3.19 (c).

3.5 Mathematical Proof for Paired Layers Interleaving

In this section, the parasitic capacitance model of PTs with single-turn layers (developed in section 2.2) is 
used to analytically validate the concept of paired layers. It will be shown that designing the structure based 
on the concept of paired layers results in an equivalent lumped capacitance circuit for the transformer that 
has a net amount of CM noise equal to zero. The first group of converters is considered for this analytical 
validation. The same method can be used to analytically validate the concept for second and third groups of 
converters.

In order to achieve no generation of CM noise in the transformer of Flyback and Forward converters, 
these topologies should be realized using the right configuration. In addition, transformer lumped parasitic 
capacitances should also satisfy a certain condition. The level of CM noise that is generated due to the 
transformer inter-winding capacitance depends on the voltages at the transformer terminals. Both Flyback 
and Forward converters have a static terminal on each side, which is not affected by the switching of the 
converter. The remaining two terminals have pulsating voltages that change relative to each other. To show
what condition is required to achieve CM noise cancellation for the transformer, Figs. 3.20 (a) and (b) show two different conditions that can occur in the aforementioned power converters. The whole effect of transformer inter-winding capacitance on CM noise can be modeled using four lumped capacitors between terminals of the primary and secondary. These two figures are only different in the way that voltages in the swinging terminals change relative to each other. From the continuity of the current in the green cut-set of Fig. 3.20 (a), (3.8) can be derived.

\[ 2i_{CM} = i_{13} + i_{14} + i_{23} + i_{24} \]  

(3.8)

The expressions for the displacement currents are presented in (3.9).

\[
\begin{align*}
    i_{13} &= C_{13} \left( \frac{dv_1}{dt} - \frac{dv_3}{dt} \right) \\
    i_{14} &= C_{14} \left( \frac{dv_1}{dt} - \frac{dv_4}{dt} \right) = C_{14} \frac{dv_1}{dt} \\
    i_{23} &= C_{23} \left( \frac{dv_2}{dt} - \frac{dv_3}{dt} \right) = -C_{23} \frac{dv_3}{dt} \\
    i_{24} &= C_{ac} \left( \frac{dv_2}{dt} - \frac{dv_4}{dt} \right) = 0
\end{align*}
\]

(3.9)

No CM noise generation means that the \( i_{CM} \) should be equal to zero. In order to achieve this, \( i_{13}, i_{14}, i_{23}, \) and \( i_{24} \) should cancel one another out and make the total CM noise equal to zero. Equating \( i_{CM} \) to zero in (3.8) and using (3.9), the required conditions for achieving full CM noise cancellation for Flyback and Forward converters can be obtained, and are presented in (3.10).

\[
\frac{dv_1}{dt} (C_{13} + C_{14}) = \frac{dv_3}{dt} (C_{13} + C_{23})
\]

(3.10)

Equation (3.10) can be achieved only if \( dv_1/dt \) and \( dv_3/dt \) have the same sign. When this condition is met, it means that the voltages in the swinging terminals change in the same direction. Otherwise, all of
the displacement currents will have the same direction and will be unable to cancel each other out. This explanation is conceptually depicted in Figs. 3.20(a) and (b). Figure 3.20(a) shows the condition in which the voltages are changing in opposite directions. In this case, the displacement currents all have the same direction and, therefore, they cannot cancel each other out. In contrast, the pulsating voltages in Fig. 3.20(b) change in the same direction. Under this condition, one of the displacement currents flows in the opposite direction of the other two currents and, therefore, it cancels them out. Therefore, no CM noise generation for the Flyback and Forward converters requires that the pulsating voltages change in the same direction. Full CM noise cancellation also requires that the transformer’s lumped capacitors satisfy a certain condition. If the coupling between the primary and secondary windings is strong, \( \frac{dv_1}{dt} \) and \( \frac{dv_3}{dt} \) can be related to each other according to \( 3.11 \).

\[
\frac{dv_3}{dt} = k \frac{dv_1}{dt}
\]

(3.11)

Where k is the transformer turn ratio \( n_2/n_1 \). Using this relationship, \( 3.10 \) can be simplified and the following condition for achieving no CM noise generation can be found.

\[
(1 - k)C_{13} + C_{14} = kC_{23}
\]

(3.12)

Therefore, if the transformer’s parasitic capacitances follow \( 3.12 \), displacement currents cancel each other out, and the net CM current is equal to zero. Equation \( 3.12 \) states the conditions necessary in a PT to achieve no CM noise generation in the transformer of Flyback and Forward converters.

Now it is shown that employing paired layers concept achieves the condition of \( 3.12 \). As explained in chapter 2, distributed capacitance of every overlapping can be transferred to the terminals of the transformer. Figure 3.21(a) shows a PT with an interleaved structure. The parasitic capacitance model of one intersection of primary and secondary is shown in Fig. 3.21(b). In this figure, every layer is shown with a grey rectangle, and a series connection of these rectangles constitutes the winding. As shown in Figs. 3.21(a) and (b), there are two terminals for each layer (one at the beginning of the layer and one at the end), and each of these terminals experiences a different pulsating voltage. The voltage waveforms at the terminals of each layer depend on the position of that layer. In order to relate the distributed parasitic capacitances of Fig. 3.21(b) to the six capacitance model of the transformer, one of the transformer terminals on each side is selected as a reference point. For the case that is presented in Fig. 3.21(b), the voltages at the terminals
Figure 3.21: The relationship between distributed parasitic capacitance of layers and the six-capacitor model of the transformer: a) an arbitrary interleaved structure of a PT, b) the parasitic capacitance model of two overlapping layers belong to different windings relative to the terminals of the transformer and c) transferring the same parasitic network to the terminals of the transformer.

of the primary layer are equal to $b \times V_1$ and $a \times V_1$, where $b$ and $a$ are defined as a ratio of the voltages at these terminals to the total voltage of primary. For instance, if the winding has eight turns, the values of $a$ and $b$ for the third turn (layer) of the winding are equal to $3/8$ and $2/8$, respectively. These values for the last turn are equal to $8/8=1$ and $7/8$. A similar explanation is considered true for the parameters $c$ and $d$ on the secondary side. These parameters represent the ratio of the voltages at the terminals of each secondary layer to the total voltage of secondary. Given this definition, it is possible to use energy method to transfer

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Transfer Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{13}$</td>
<td>$\frac{C_0}{24} [5ad + 7bd + 7ac + 5bc]$</td>
</tr>
<tr>
<td>$C_{14}$</td>
<td>$\frac{C_0}{24} [12a + 12b - 5ad - 7bd - 7ac - 5bc]$</td>
</tr>
<tr>
<td>$C_{23}$</td>
<td>$\frac{C_0}{24} [12c + 12d - 5ad - 7bd - 7ac - 5bc]$</td>
</tr>
<tr>
<td>$C_{24}$</td>
<td>$\frac{C_0}{24} [24 + 5ad + 7bd + 7ac + 5bc - 12a - 12b - 12c - 12d]$</td>
</tr>
<tr>
<td>$C_{12}$</td>
<td>$\frac{C_0}{24} [8a^2 + 8b^2 + 8ab - 12a - 12b]$</td>
</tr>
<tr>
<td>$C_{34}$</td>
<td>$\frac{C_0}{24} [8c^2 + 8d^2 + 8cdb - 12c - 12d]$</td>
</tr>
</tbody>
</table>
the parasitic capacitance network of each overlapping to the terminals of the transformer, as shown in Fig. 3.21(c). Equations presented in Table. 3.1 provide transfer equations from distributed capacitance of 3.21(b) to lumped capacitance of 3.21(c). These equations show that the value of transferred capacitors depends on the parameters a, b, c, and d, which depend on the layers that are overlapping.

The concept of paired layers requires that \( \frac{dv}{dt} \) at terminals of overlapping layers to be equal, which was presented in (3.3). This requirement is equivalent to (3.13)

\[
a = kc \quad , \quad b = kd
\]

(3.13)

Where k is the transformer turns ratio \((n_2/n_1)\).

The requirements for achieving zero CM noise in the transformers have been proposed in (3.12). Substituting \(C_{13}, C_{14}, C_{23}\) in (3.12) with their equivalent expressions in table 3.1, the condition for achieving zero CM noise can be found which is shown in (3.14).

\[
(1 - k)C_{13} + C_{14} = kC_{23} \rightarrow
\]

\[
(1 - k) \frac{C_0}{24} [5ad + 7bd + 7ac + 5bc]
\]

\[
+ \frac{C_0}{24} [12a + 12b - 5ad - 7bd - 7ac - 5bc]
\]

\[
= k \frac{C_0}{24} [12c + 12d - 5ad - 7bd - 7ac - 5bc]
\]

(3.14)

The solution for (3.14) is presented in (3.15).

\[
a + b = k[c + d]
\]

(3.15)

This is the general condition that results in zero CM noise and paired layers concept is a special case of this requirement, as (3.13) satisfies this requirement. Any other method that satisfies this requirement also achieves zero CM noise generation.

Considering the above explanations, the concept of paired layers to achieve zero CM noise can be explained in two different ways:

1. **Through lumped Capacitance Circuit:** By using the concept of paired layers, the equivalent lumped capacitance circuit of the transformer is in a way that displacement currents in the four inter-winding parasitic capacitances cancel each other out which leads to net CM noise equal to zero.
2. **Through Distributed Capacitance Model:** When paired layers overlap, the overlapping layers have the same $\frac{dv}{dt}$. Therefore, no displacement current will be induced in the distributed parasitic capacitances. As a result, there would be no CM current in the transformer.

The analytical proof presented in this condition showed that the paired layers concept is a special case of a general condition that results in zero CM noise. Other schemes that satisfy $3.15$ also can be designed to achieve zero CM noise generation.

### 3.6 Eliminating CM Noise Generation Through the Core ($I_{P-C}$ and $I_{P-C-S}$)

As mentioned at the beginning of this chapter, CM noise also can propagate through the core. While the amount of CM noise that is generated through the core is much smaller than the amount of CM noise that generates when layers of primary and secondary overlap, efforts should be made to avoid the generation of CM noise through the core to achieve very low CM noise generation. As shown in Fig. 3.22(a), $I_{P-C}$ is the CM noise that is generated when a layer of primary overlaps with the core and injects CM noise current into it. Part of this CM noise goes to the earth through parasitic capacitance between core and ground ($C_{C-G}$) and returns through the Line Impedance Stabilization Networks (LISN). Since most of the time EMC tests are done at the input of the power converter, this CM noise will be part of the measured noise, and thus it should be eliminated. On the other hand, $I_{P-C-S}$ is the part of CM noise that is generated from capacitive

![Figure 3.22: Eliminating CM noise generation through the core. a) $I_{P-C}$ and $I_{P-C-S}$ are generated when primary layers overlap with the core. b) $I_{P-C}$ and $I_{P-C-S}$ are eliminated when secondary layers are used at the top and bottom of the structure to avoids exposing primary winding to the core. $I_{S-C}$ returns to its source without going to the primary and does not show up on the input noise.](image-url)
coupling between primary and secondary through the core. Both $I_{P-C}$ and $I_{P-C-S}$ can be eliminated by not overlapping the primary layers and the core. This means that the primary layers should be placed between secondary layers and the top layer and bottom layer of the PT structure should belong to the secondary. This condition is shown in Fig. 3.22(b). Since no layer of the primary overlaps with the core, no CM noise will be injected from primary to the core and both $I_{P-C}$ and $I_{P-C-S}$ will be eliminated.

It should be noted that this technique is only possible if the structure of the transformer starts and ends with the secondary winding. For instance, in applications that have a strict isolation requirement, a non-interleaved structure should be used to satisfy the isolation requirement. Under this condition, the primary winding is exposed to the core and causes some CM noise through the core. In this case, the distance between the primary winding and the core should be increased to minimize the effect of this overlapping. As a result, the core window is not utilized efficiently.

It is also worthwhile to mention that the above-mentioned rules only target CM noise and depending on the situation, the designer might decide to expose the primary winding to the core. Usually, this happens in step-up transformers, where $\frac{dv}{dt}$ of secondary layers is much higher than primary turns. Since a conductor with high $\frac{dv}{dt}$ acts like an E-field antenna, exposing secondary turns to the core and circuit creates a radiation problem. Similar to conducted noise tests, power converters should pass radiated tests too and passing this test would be hard with exposed secondary turns. As a result, the designer might compromise common-mode noise for getting lower radiated noise.

### 3.7 Summary

In this section, the concept of paired layers was introduced as a method of avoiding CM noise generation in PTs. According to this concept, if the overlapping layers have the same layout and similar $\frac{dv}{dt}$, such an overlapping does not generate CM noise. These layers are called paired layers and any winding arrangement that only has overlapping of paired layers at primary and secondary intersections theoretically has zero CM noise generation. In order to implement this idea, turns with similar $\frac{dv}{dt}$ (called paired turns) should be found in primary and secondary windings. Finding paired turns depends on the voltage distribution of windings which depends on the topology. From transformer’s voltage distribution point of view, power converters were divided into three groups and paired turns were found for each group. Besides, different configurations of topologies were studied and right configuration that allows for finding paired turns in primary and secondary were presented. A simple example of an 8 : 4 PT that incorporate the concept of paired layers was presented for each group to make the procedure easy to understand. Also, a mathematical proof for the concept of
paired layers were presented. It was shown that employing the concept of paired layers in the transformer structure leads to a lumped capacitance network for PT that has net amount of CM noise equal to zero. Beside, methods for eliminating CM noise generation through the core was presented. In the next chapter, paired turns will be combined with interleaving methods to achieve PTs with low AC resistance, low leakage inductance, and no CM noise generation.
Chapter 4

Paired Layers Interleaving

The main purpose of introducing the concept of “paired layers” is to develop a design method that results in PTs with no CM noise generation. In this section, this concept is combined with interleaving methods to achieve PTs that not only have low AC resistance and leakage inductance but also benefit the converter by not generating CM noise. The combination is a design method called “paired layers interleaving” which eliminates the long-standing trade-off in transformer design and allows the designer to use interleaved structures to minimize AC resistance and leakage inductance, and not to worry about CM noise.

In the first part of this chapter, different methods of designing planar layers are discussed. Then, the effect of winding arrangement on AC resistance and leakage inductance is briefly discussed, and conventional interleaving methods for PTs are presented. These winding arrangements are then combined with the concept of “paired layers” to develop paired layers interleaving method. Three different groups of converters are considered and several designs using the paired layers interleaving method are provided for each group to make the method easy to understand. These examples are further experimentally tested to verify the proposed methods and concepts.

4.1 Methods of Implementation

As explained in the previous section, eliminating $I_{P-S}$ (which is the result of direct overlapping of primary and secondary) requires the overlapping layers of primary and secondary to have the same number of turns, the same layout, and the same $\frac{dv}{dt}$ at their ports. Depending on the number of turns in primary and secondary windings, different methods can be used to make this happen. In this section, different winding methods to implement the concept of “paired layers is discussed.

\[1\] Portions of this chapter have been published in [1-4]
4.1.1 Implementation Using PCB

If both windings consist of a large number of turns, four-layer PCBs that are commonly used in circuit design can be used to construct both windings. Figure 4.1 shows a diagram of primary and secondary windings made using four-layer PCBs; The design should be done in such a way that top layer of the primary and the bottom layer of the secondary have turns with similar $\frac{dv}{dt}$; therefore, their overlapping does not create CM noise. The same criterion should be applied in the design of the bottom layer of the primary and the top layer of the secondary. Turns that do not share the $\frac{dv}{dt}$ with any turn of the other winding should be placed on the middle layers, so they are shielded by the top and bottom layers and do not create CM noise.

Considering the above-mentioned rules for designing PCBs, Fig. 4.2 shows PCB layouts for different turns ratios in LLC PTs. The criteria for finding paired-turns in LLC PTs was discussed in section 3.3.1. Figure 4.2 (a) shows how primary and secondary PCBs should be designed for a 16 : 16 turns ratio specification. As shown in Fig. 4.2 (a), the top layer of the primary PCB has the first four turns of the primary (P(01) to P(04)). On the other hand, the bottom layer of the secondary, which faces the top layer of the primary, contains the turns S(05) to S(08) of the secondary (these turns have similar $\frac{dv}{dt}$ as turns P(01) to P(04)). Therefore, the overlapping of the top layer of the primary and bottom layer of the secondary does not create CM noise. The same condition is true for the bottom layer of the primary (which contains turns P(05) to P(08)) and the top layer of the secondary (which contains turns S(01) to S(04)). Since these turns have similar $\frac{dv}{dt}$, their overlapping does not generate CM noise. Figure 4.2 (a) also shows the turns that have no pair on the other winding (P(09) to P(16) on the primary winding and S(09) to S(16) on the secondary winding) are placed within the middle layers of PCBs. Therefore, they are not exposed to the other winding and so do not contribute to CM noise generation. Figs. 4.2 (b) shows the PCB layout design specified for

![Figure 4.1: Disposition of how different layers of the PCB should be used to avoid CM noise generation.](image-url)
The disadvantage of using the proposed layouts of Fig. 4.2 is the extra DC resistance of the layout. In the traditional PCB layouts for planar windings, the turns are distributed equally between the PCB layers. Since all turns have the same width, the current distribution is even and so the DC resistance of the winding is minimized. In the proposed layouts of Fig. 4.2, the turns of primary PCB do not necessarily have the same width. According to Fig. 4.2, when the turns ratio is unity, the number of turns on each layer of the primary PCB is the same. However, as the turns ratio deviates from unity, more turns should be placed on mid-layers and fewer turns are allowed to be on top and bottom layers. This increases the DC resistance of the primary winding as a side effect of using the method to minimize CM noise. To find out by how much primary winding resistance is increased as the result of using the proposed method, FEA has been used to find the DC resistance of the layouts; and the results are shown in Fig. 4.3. These layouts are designed for an ER/41/10/28 core and the copper thickness is 3oz. Figure 4.3 (a) shows the primary and secondary

![Layouts for 16:16 LLC PT](a)

![Layouts for 16:8 LLC PT](b)

Figure 4.2: PCB layouts for eliminating $I_{P-S}$ in LLC PTs. Layout for a) 16 : 16 turns ratio, and b) 16 : 8 turns ratio.
Figure 4.3: Analysis of DC resistance increase of windings caused by use of proposed method. The proposed layout and its DC resistance for a) 16:16 turns ratio, b) 16:8 turns ratio, c) 16:4 turns ratio and, d) 16:2 turns ratio.

layouts for the 16:16 turns ratio. In this layout, turns are distributed equally between layers of the primary PCB and there is no increment of the primary winding’s resistance. In other words, there is no extra DC resistance penalty when the proposed layout is used for 16:16 turns ratio. Figure 4.3 (b) shows the primary and secondary layouts for the 16:8 turns ratio. In this case, the primary turns are not equally shared between PCB layers (top and bottom layers each have two turns and middle layers have 6 turns each). This causes the primary winding resistance to increase by 21% and the total windings’ resistance reflected to the primary \((R_1 + R_2 \times (\frac{n_1}{n_2})^2)\) to increase by 11.5% (in comparison to a traditional layout for 16:8 turns ratio). Note that the secondary PCB always has an equal number of turns in each layer and so there is no increase in the secondary winding resistance. Figure 4.3 (c) and (d) show the primary and secondary layouts for the 16:4 and 16:2 turns ratios. Compared to traditional layouts, these layouts have 32% and 45% more DC resistance than traditional layouts for these turns ratios. However, it does not mean that the conduction losses for these layouts are 32% and 45% more: for transformers with large step-down ratios, most of the high-frequency
Conduction losses are on the secondary winding, which does not have extra resistance due to the use of the proposed method. Therefore, the secondary losses are similar in the proposed and the traditional methods, and the extra conduction loss is much less than 32% and 45%. This aspect will be explained in the next section when a proposed 16 : 1 : 1 PT is compared to a traditional 16 : 1 : 1 PT.

4.1.2 Implementation Using a Combination of PCB and Copper Foil

If one winding has a large number of turns and the other has fewer turns (as the case for high step-up or step-down PTs), the winding with a large number of turns can be constructed using four-layer PCB and the other winding can be realized using single-turn copper foils. Figure 4.4 shows this condition for a 14 : 2 Flyback PT. In this case, the first two turns of the primary are paired with secondary turns. Secondary turns are realized using copper foils (as they are high-current). The first two turns of the primary (that are paired with the secondary turns) are placed on the top and bottom layers of PCB and the rest of primary turns are placed within the middle layers of the PCB. As a result of this layout, secondary turns only overlap with paired turns and their overlapping does not generate CM noise.

If the use of four-layer PCBs is prohibitive due to the cost issue, a combination of two-layer PCBs and copper foils can be used for PTs with large or small turns ratio. Figure 4.5 shows this type of implementation for a 36 : 2 Flyback PT. Using this layout, only the first two turns of the primary have a pair on the secondary side. The remaining 34 turns do not have a pair on the secondary and, therefore, should not overlap with the secondary winding. To implement the proposed idea, the first two turns of the primary are realized using single-turn layers. These two layers can overlap with their pair on the secondary side. The remaining 34 turns are realized using a double layer PCB. This PCB is placed between the first two turns of the primary to hide them from the secondary winding.

Figure 4.4: Implementing the method using PCB for one winding and copper foil for another winding. Winding layouts for eliminating \( i_{P-S} \) in a 14 : 2 Flyback PT.
4.1.3 Implementation Using Copper Foil

If the number of turns is small in both windings, it is possible to use single-turn copper foils for both windings. Figure 4.6 shows an 8:4 Flyback PT using single-turn copper foils. Under this condition, the first four turns of the primary are paired with four turns of the secondary and so can overlap with them. The other four turns of the primary do not have a pair and so should be hidden from the other winding. A simple structure that only has overlapping between paired layers is shown in Fig. 4.6 (c). Unlike the PCB-based windings, this method does not have the penalty of having more conduction loss in the primary winding.

In this section, the implementation of the paired-layers method has been explained through several examples. The proposed PCB layouts can overlap with each other without generating CM noise. The method was implemented for different turns ratios to show the method’s flexibility and also to make it easy to understand. Implementing the method using single-turn copper foils also has been discussed through an example.

Figure 4.6: Implementation of the method for an 8:4 Flyback PT using single-turn copper foils. a) Primary and secondary layouts, b) paired layers of primary and secondary, and c) a simple structure with no CM noise generation.
Later in this chapter, these layouts are used to design interleaved structures that not only have very low AC resistance but also have very low CM noise generation.

### 4.2 The Effect of Winding Arrangement on AC Resistance and Leakage Inductance

The effect of winding arrangements on AC resistance can be explained by Dowel’s formula to calculate the AC resistance that is presented in (4.1).

\[
R_{ac} = R_{dc} \times \frac{\xi}{2} \left[ \frac{\sinh(\xi) + \sin(\xi)}{\cosh(\xi) - \cos(\xi)} + (2m - 1)^2 \times \left( \frac{\sinh(\xi) - \sin(\xi)}{\cosh(\xi) + \cos(\xi)} \right) \right]
\]  

(4.1)

Where \( \xi \) and \( m \) are defined as follows:

\[
\xi = \frac{h}{\delta} \quad \quad m = \frac{F(h)}{F(h) - F(0)}
\]

(4.2)

In (4.2), \( h \) is the thickness of traces, \( \delta \) is the skin depth at the operating frequency, and \( F(h) \) and \( F(0) \) are the Magneto-Motive Force (MMF) at the limits of the conductor, which depend on the arrangement of the transformer. The first term in (4.1) describes the skin effect and only depends on the ratio of copper thickness to skin depth (\( \xi \)). The second term in (4.1) represents the proximity effect and relates the AC resistance to the winding arrangement of the transformer. The proximity effect depends on two factors; \( \xi \) and \( m \). The value of \( m \) for each layer is determined by the leakage fluxes that surround the layer and is calculated based on (4.2).

In the interleaved structures (where primary and secondary layers are interleaved and have several overlaps), the leakage fluxes of primary and secondary windings cancel each other out and, therefore, a low value for \( m \) is obtained. However, for the non-interleaved structure (where primary and secondary are separated), the values of \( m \) are very large and the proximity effect dominates (4.1) and significantly increases the AC resistance. In order to show how the structure of PT affects the value of \( m \), Fig. 4.7 shows three different structures for an 8 : 4 PT. According to Fig. 4.7(a), the non-interleaved structure leads to large values of \( m \), which considerably increases the AC resistance. On the other hand, using the interleaved structures of Fig. 4.7(b) and (c), the values of \( m \) are reduced significantly, which minimizes proximity effect and leads to low AC resistance and leakage inductance.
4.3 Paired Layers Interleaving for Flyback and Forward Converters

In this section, the concept of paired layers is combined with interleaving methods to develop paired layers interleaving method for Flyback converter, which belongs to the first category of power converters discussed in section 3.2. The same winding structures are also applicable on Forward converter, as paired turns are similar in Flyback and Forward converters. This method results in Flyback/Forward PTs that not only generate almost zero CM noise, but also have very low AC resistance and leakage inductance.

The implementation of the proposed principle depends on the number of turns in the primary and secondary. For low voltage applications, the number of required turns is not too high. Therefore, single-turn copper foils can be connected in series to make a complete winding. Under this condition, the proposed method can be implemented easily, as all layers consist of one turn. However, if the input (or output) voltage is high, such as for adapters with universal input voltages (85-265 VAC), then a large number of turns is required. Under this condition, it is not possible to use a single-turn copper foil for every layer, as the space in the core is very limited and cannot accommodate many copper layers. In this case, a combination of PCB and single-turn copper foils is used to implement the proposed idea. In this section, both conditions are considered and a procedure for implementing the proposed idea for both scenarios is proposed. By following the procedure that is presented for these transformers, high-efficiency PTs with no CM noise generation property can be designed.

Figure 4.7: Effect of winding arrangement on the value of m. a) Non-interleaved structure, b) partially interleaved structure, and c) fully interleaved structure.
4.3.1 Implementation of the Proposed Method for PTs With Small Numbers of Turns

The number of turns is directly proportional to the applied voltage. For low voltage applications, few turns are needed and windings can be made using single-turn copper foils that are connected in series. In this situation, the number of layers for each winding is at least equal to the number of turns, as each layer consists of only one turn. If some layers are connected in parallel (to reduce resistance), the number of layers will be more than the number of turns. The focus of this subsection is on showing the applicability of the paired layers interleaving method to PTs with a small number of turns. In order to explain how the proposed idea can be applied to these PTs, the method is implemented for different turn ratios.

Fig. 4.8 explains how paired layers interleaving can be applied on a 7 : 4 PT. Figure 4.8(a) shows the paired layers on the primary and secondary sides and shows that four turns on the primary side have a pair on the secondary side. The remaining three turns of the primary side do not have a pair on the secondary side and, therefore, should be avoided in the intersections. Any structure that satisfies this condition will lead to CM noise elimination. Figure 4.8(b) shows one simple structure that satisfies this condition. As shown in this figure, only paired layers overlap with each other in this structure. In this structure, seven layers of the primary are connected in series to make a seven-turn winding. The four layers of the secondary are also connected in series to make a four-turn secondary winding. Therefore, there are no parallel layers in this

![Diagram showing paired layers and layers with no pair on the secondary](image)

**Figure 4.8:** Interleaved winding arrangement with low AC resistance/leakage inductance and no CM noise generation for a 7 : 4 PT: a) Paired layers in the primary and secondary windings. b) and c) Examples of paired layers interleaved structures.
structure. However, if the core window can accommodate more layers, it is desirable to add more layers in parallel and reduce the resistance. Adding more layers also makes it possible to allow more interleaving and, consequently, to achieve lower leakage inductance. Figure 4.8 (c) shows the same transformer with more layers. In this arrangement, the secondary has eight layers (two layers per turn, connected in parallel). Since each layer of the secondary winding requires a pair in the primary side (to achieve noise cancellation), there should be eight paired layers in the primary. In other words, each of the first four turns of the primary (which have a pair in the secondary) are made using two layers in parallel, while the unpaired turns are realized using only one layer. The above explanation can be seen in Fig. 4.8 (c), as the layers with the same name are connected in parallel. In this figure, parallel layers are also identified using small rectangles of the same color. Both structures in Fig. 4.8 also start and end with a secondary layer, which blocks CM noise generation injection from primary to the core and so avoids CM noise propagation through the core. As a result, both of these arrangements meet the requirements to achieve zero CM noise generation.

The key requirements in implementing paired layers interleaving are as follows:

1. Only paired layers of primary and secondary should overlap each other. The layers that do not have a pair in the other winding should not be placed in the intersections. This ensures that no CM noise will be generated.

2. Legal intersections (overlapping between paired layers) should be used to design an interleaved structure that minimizes leakage flux. This results in low leakage inductance and AC resistance.

3. If parallel layers are used in the winding, they should have similar positions in terms of proximity effect. Otherwise, one of the conductors will carry most of the current.

4. It is desirable to start and end the winding arrangement with secondary layers to avoid CM noise generation through the core.

Following the above criteria for PTs will lead to the creation of high-efficiency PTs that do not produce CM noise, in spite of their very large inter-winding capacitance. The above rules can be applied to transformers with different turn ratios, and without restrictions in turns ratio values. Figure 4.9 (a) shows an optimized winding arrangement that satisfies the no-noise generation requirement and low leakage inductance for a 6:3 Flyback PT. In this figure, parallel layers are also identified using small rectangles of the same color. To illustrate the structure better, a three dimensional model of this structure is shown in Fig. 4.9 (b). Figures 4.9 (a) and (b) show that the above rules are applied to this structure. Therefore, it is expected that this transformer generates no CM noise and at the same time achieves low AC resistance and leakage inductance.
Figure 4.9: An example of paired layers interleaved structure for a 6 : 3 PT. a) The proposed structure and b) a 3D model of the structure from both sides.

confirm this claim, this transformer has been simulated using FEA. According to the FEA results, the total leakage inductance from the primary side is equal to 130 nH which is much lower than leakage inductance of an equivalent wire-wound Flyback transformer (typically in the range of few uH).

In this subsection, the paired layers interleaving method has been implemented for PTs with a few turns on each side. The typical application of these PTs is in low voltage Flyback and Forward converters. Windings in such PTs can be realized using single-turn copper foils that are connected in series. It has been shown that the proposed idea can be implemented easily for different turn ratios. In addition to the proposed CM noise cancellation method, the criteria for achieving low leakage inductance have been provided. Therefore, the resulting PTs not only generate no CM noise but also have very low leakage inductance which improves the performance and efficiency of Flyback converters.

4.3.2 Implementation of the Proposed Method for PTs With a Large Number of Turns

For higher voltage levels, the number of turns should increase to limit the flux density within the core. For instance, given the relatively small size of the cores that are used in low power transformers, the transformers that are used in Flyback adapters with universal voltage range (85-260 Vac) should have a large number of turns in the primary side. If the number of turns in a winding is high, it is not practically possible to make that winding using single-turn copper foils. This is mainly due to the limited space in the core, which cannot accommodate many layers. Besides, a large number of turns require many terminations, which makes it
difficult in small width core design. In this situation, spiral PCB designs can facilitate the creation of many turns in one layer. As explained in section 4.1, this means that four-layer PCBs or a combination of PCB and copper foil can be used to make the PCB with a large number of turns.

Fig. 4.10 (a) shows an interleaved paired layers structure for a 24 : 4 Flyback PT. Under this condition, only the first four turns of the primary have a pair on the secondary side. The remaining 20 turns do not have a pair on the secondary and, therefore, should not overlap with the secondary winding. In this case, the first four turns of the primary are realized using single-turn layers. These four layers can overlap with their pair on the secondary side. The remaining 20 turns are realized using two double-layer PCBs. Each PCB has 10 turns (five on each side), and PCBs are placed between single-turn layers of the primary side to hide them from the secondary winding. On the other hand, the secondary winding consists of four single-turn copper foils that are connected in series. As shown in Fig. 4.10 (a), only paired layers overlap in the structure which avoids CM noise coupling from primary to secondary. For example, P3 only overlaps with its pair which is S3. Beside satisfying paired layers requirement, the top and bottom layer of the structure belongs to the secondary winding which blocks CM noise injection from primary to the core. Therefore, this structure virtually does not generate any CM noise.

Fig. 4.10 (b) shows the implementation of the proposed method for a PT with 36 : 3 turn ratio. The first three turns of the primary side have a pair on the secondary. These turns are realized using single-turn copper foils, and the remaining 33 turns are made using PCBs. Each PCB has 11 turns and the PCBs have been placed between the layers of the primary to avoid overlapping with the secondary winding. Examining the structure that is proposed in Fig. 4.10 (b) confirms that only paired layers meet each other in this structure. Besides, the parallel layers in the secondary side are placed symmetrically from both ends, which ensures even current sharing and low AC resistance. Therefore, this structure also does not create CM noise and provides very low AC resistance and leakage inductance.

In this section, the concept of paired layers has been employed along with interleaving methods to achieve winding structures with very low leakage inductance and close to zero CM noise generation for Flyback PTs. It has been shown that the proposed solution does not have any limitation regarding the turns ratio values, and can be applied to transformers with both large and small numbers of turns. If the number of turns is small, the solution can be implemented using single-turn copper foil layers. If the number of turns is large, a combination of single-turn copper foils and PCBs can be used to implement the idea. Therefore, the proposed method can be implemented for any turns ratio. While implementing the proposed method adds a bit of complexity to the design of the PT structure, the benefits of employing the method are significant and
Figure 4.10: Implementation of the proposed method for PTs with large turn ratios: Implementation of the method for a) a 24 : 4 PT and b) a 36 : 3 PT. Both of these structures satisfy the requirement of no CM noise generation (as only paired layers overlap) and low AC resistance criteria (placing parallel layers in symmetrical positions from both ends).
make using the method worthwhile.

### 4.3.3 Experimental Verification

In order to confirm the validity of the proposed techniques, extensive experimental tests have been done. Fig. 4.11(a) shows the prototype of a PT that is realized using the proposed method. The structure of this transformer is similar to Fig. 4.9. The specifications of this transformer are also presented in Table 4.1. Since this transformer has a highly interleaved structure, the value of leakage inductance is extremely low. On the other hand, since primary and secondary overlap each other several times (as a result of interleaving) and the overlapping layers are tightly placed next to each other, the value of parasitic capacitance is a very large value of 700 pF which is large enough to make serious EMI problems. However, since this transformer has been manufactured using paired layers interleaving method, it will be shown that this transformer generates extremely low levels of CM noise. In order to validate the method, the result of the proposed planar transformer with 700 pF inter-winding capacitance is compared with a wire-wound transformer which only has a

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<th>Flyback Converter</th>
<th>Planar Transformer</th>
<th>Wire-Wound</th>
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<td>72V</td>
<td>$N_p/N_s$ 6/3</td>
<td>$N_p/N_s$ 6/3</td>
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<td>Core RM 12</td>
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<td>$C_{inter}$ 10 pF</td>
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<tr>
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<td>$L_{lk-p}$ 130 nH</td>
<td>$L_{leak}$ 1$\mu$H</td>
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<tr>
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<td>23 m$\Omega$</td>
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**Figure 4.11:** a) The prototype of the proposed PT along with an equivalent wire-wound transformer. b) The circuit that is used to signify the CM currents caused by the inter-winding capacitance.
parasitic capacitance of 10 pF (70 times less). This transformer is shown in Fig. 4.11 (a) and its specifications are presented in table 4.1. In this part, we will show that the proposed PT generates significantly less CM noise than this transformer, although its parasitic capacitance is 70 times more.

The first test intends to separate and visualize the common mode current caused by the transformer’s inter-winding capacitance and proves that the proposed PT generates very little CM noise. Since the standard method of measuring conducted noise at the input side cannot separate the noise of different elements, the circuit that is shown in Fig. 4.11 (b) is used as a test circuit for observing only the CM noise that is generated due to the inter-winding capacitance of the transformer [47]. As there is one terminal with static voltage and another terminal with swinging voltage, the transformer’s voltage is similar for Flyback and Forward converters. Therefore, the transformer’s behavior in terms of CM noise generation is similar to the behavior when used in Flyback and Forward converters. There are two sources of CM noise in Fig. 4.12 (b): The first one is the parasitic capacitance between the drain and heatsink of the switch. Another source of CM noise is the parasitic capacitance of the transformer. Since the secondary side is open, no current is induced in the secondary winding through magnetic coupling and the current at the secondary side consists of only CM noise currents of the transformer. As is shown in Fig. 4.11 (b), the CM noise currents of the switch and transformer propagate in the circuit and return to their source through the earth. In order to separate the transformer CM noise, a resistor has been added between the quiet point of the secondary and the earth. Since the impedance of this resistor is much less than the impedance of parasitic capacitances between the secondary nodes and the earth, most of the transformer CM noise currents complete the path through this resistor. Under this condition, the resistor voltage is a representation of the transformer’s CM noise.
Figs. 4.12 (a) and (b) show the voltage across the resistor with the wire-wound transformer and the PT employed in the circuit, respectively. Since the wire-wound transformer has significantly less inter-winding capacitance (70 times less), the general expectation is that it will generate considerably lower CM noise current. However, the experimental results are presented in Fig. 4.12 (a) and (b) show that the proposed PT with a very large inter-winding capacitance of 700 pF generates extremely low levels of CM noise (close to zero). In other words, the proposed method enables the use of highly interleaved structures for PTs that minimize AC resistance and leakage inductance, while simultaneously generating almost zero CM noise, despite having large inter-winding capacitances.

For the second test, the proposed PT has been employed in a Flyback power converter to confirm the superiority of the proposed method in terms of noise reduction. The specification of the converter is presented in table 4.1. Line Impedance Stabilization Networks (LISN) have been placed at the input of the converter and the total conducted noise has been observed with a spectrum analyzer. The conditions of both tests are the same and the same Flyback converter with RCD snubber is used. Figures 4.13 (a) and (b) show

![Waveforms of the Flyback converter with different transformers. Switch voltage (Ch1) and primary current (Ch2). Waveforms with a) the wire-wound transformer and b) with the proposed PT.](image)

**Figure 4.13:** Waveforms of the Flyback converter with different transformers. Switch voltage (Ch1) and primary current (Ch2). Waveforms with a) the wire-wound transformer and b) with the proposed PT.

![The spectrum of conducted mode noise of the Flyback with a) wire-wound transformer, and b) the proposed PT.](image)

**Figure 4.14:** The spectrum of conducted mode noise of the Flyback with a) wire-wound transformer, and b) the proposed PT.
Figure 4.15: a) Ch1 to Ch6 show the voltage distribution over the primary winding. b) Ch1 to Ch3 and Ch4 to Ch6 are the voltage distribution over the first three turns of the primary and their corresponding pair on the secondary, respectively.

the waveforms of the converter with PT and the wire-wound transformer, respectively. Due to the large leakage inductance of the wire-wound transformer, the switch voltage has a considerably larger spike at turn-off. On the other hand, the proposed PT has a very small leakage inductance which is the result of a highly interleaved structure and leads to less voltage spike on the switch. Figures 4.14 (a) and (b) show the spectrum of conducted noise with wire-wound transformer and the proposed PT, respectively. These figures show that while the proposed PT has a very high parasitic capacitance of 700pF, it produces less noise than does a traditional transformer whose parasitic capacitance is 70 times less. These results show that the proposed method has resolved the trade-off between low leakage inductance and the noise due to interwinding capacitance, leading to a new generation of PTs that have low leakage inductance and extremely low noise generation at the same time.

Finally, as it was explained in chapter 3, the winding method relies on the proposed concept of paired
layers which tries to overlap layers that have similar voltage waveforms (and so similar \( \frac{dv}{dt} \)) to avoid the generation of CM noise. Therefore, it is also interesting to compare the voltage of paired layers to confirm the concept of paired layers and show why the proposed method leads to no generation of CM noise. Figure 4.15(a) shows the voltage distribution along the primary winding. As shown in this figure, the first pin of the primary has a static voltage waveform which is not affected by the switching of the converter. The amplitude of voltage swinging increases after each turn and reaches its maximum after the last turn. Since this is a 6:3 transformer, the first three turns of the primary can be paired with the secondary layers. The remaining three layers of the primary do not have a pair on the secondary side and, therefore, should not overlap with secondary layers (the structure was shown in Fig. 4.9). To confirm this hypothesis, another measurement is done which is shown in Fig. 4.15(b). Figure 4.15(b) shows the voltage of paired layers on the primary and secondary sides. As it was expected, these layers have a similar voltage waveform (the same \( \frac{dv}{dt} \)). As it was explained and analytically proved in chapter 3, the overlapping of such layers does not produce CM noise.

The experimental results verify that the proposed method successfully eliminates the trade-off between inter-winding capacitance and leakage inductance for Flyback PTs. Using this method, designers can use a highly interleaved structure for Flyback PTs to achieve very low leakage inductance without the concern of CM noise generation due to a large inter-winding capacitance of these structures.

4.4 Paired Layers Interleaving for LLC Resonant Converters

In traditional PTs, the amount of the transformer’s CM noise depends on the number of overlapping between primary and secondary layers. Interleaved structures that are used to reduce AC resistance generate significant amounts of CM noise, as they have many overlapping between primary and secondary layers. This means that traditional interleaved PTs reduce AC resistance at the expense of generating large amounts of CM noise and so suffer from a trade-off between AC resistance and CM noise. In this section, the concept of paired layers is employed along with interleaving methods to develop paired layers interleaving method for half-bridge LLC resonant converter, which belongs to the second category of DC-DC converters discussed in section 3.3. It will be shown that the trade-off between low AC resistance and low leakage inductance will be eliminated for LLC PTs by using paired layers interleaving method. This means that no matter how many times these PCBs overlap, no CM noise will be generated, and so the designer is free to use any structure without the concern of CM noise generation.
4.4.1 Implementation of the Paired-Layers in Two-Winding LLC PTs

As discussed before, if the number of turns is large in a winding, four-layer or two-layer PCBs are used to make the winding. Each of the proposed PCBs in section 4.1 makes a complete winding, and so only two PCBs—one for the primary and one for the secondary winding—are required to make the transformer structure. So, in its simplest form, the structure of the transformer only has one primary PCB and one secondary PCB. However, depending on the requirements and specifications, the designer may choose to use several PCBs in parallel or series for each winding to reduce the resistance of the winding. Selecting the transformer’s structure depends on a number of factors. For instance, if the design is cost-driven, the designer might be limited to use only one primary PCB and one secondary PCB (to reduce the cost), thus choose a non-interleaved structure. Depending on the isolation requirements, the designer might not be able to use an interleaved structure. For low voltage and high current applications, the designer might use several layers in parallel for each winding (to reduce DC resistance of the windings) and also use a very interleaved structure to minimize AC resistance. In all different scenarios, the use of the proposed methods guarantees that almost no CM noise will be generated in the PT.

In order to show how the structure of PT affects the AC resistance and loss, Fig. 4.16 shows four different structures for a 16 : 8 PT. The layout of primary and secondary PCBs is similar to the layouts of Fig. 4.2 (b) and so the CM noise generation of all these structures is minimal (because no matter how many times primary and secondary overlap, their overlapping does not generate CM noise). Figure 4.16 (a) shows the simplest structure that only has one PCB for primary and one PCB for secondary. This is a non-interleaved structure with a minimum cost that can be used in applications that have strict requirements regarding cost or isolation. However, the winding resistance is high and so it cannot be used in high current applications. It also does not block the CM noise generation path through the core, as the primary winding is exposed to the core. For higher current levels, it is possible to have multiple PCBs in parallel for each winding to reduce the resistance and conduction loss. Adding PCBs in parallel is only effective if the current is shared evenly between the PCBs. This requires that parallel PCBs have symmetrical positions in the transformer’s structure, such as the structure of Fig. 4.16 (b). Otherwise, due to the skin and proximity effects, the current is not equally shared between the PCBs and only one PCB effectively conducts the current, which means that the added PCB is not helping to reduce resistance and conduction loss. Fig. 4.16 (b) shows an interleaved structure with two PCBs for each winding that are connected in parallel. Using two PCBs for each winding halves the DC resistance and placing the primary PCBs between secondary PCBs helps to reduce leakage flux and AC resistance. This structure also blocks the CM noise path through the core, as primary turns
Figure 4.16: Different structures for 16 : 8 turns ratio. The layouts of primary and secondary PCBs were shown in Fig. 4.2(b). a) A non-interleaved structure with the minimum number of PCBs, b) a structure with two parallel PCBs for each winding, c) a structure with four parallel PCBs for each winding and, d) a structure with three parallel PCBs for each winding. The thickness of PCB traces is $3\Omega$ and the AC resistance results are reported at 200kHz.

are not exposed to the core. Figure 4.16(c) shows another structure with four PCBs in parallel for each winding. Comparing to Fig. 4.16(a), the DC resistance is reduced four times. It also achieves a good current sharing between PCBs, as parallel PCBs are positioned such that they experience similar leakage flux and proximity effect. This structure also blocks the CM noise generation through the core, as the primary PCBs are not exposed to the core. Figure 4.16(d) shows a very interleaved structure that intends to minimize proximity effect and so AC resistance. In this structure, the top and bottom PCBs should only have half of the secondary turns. According to this figure, this structure achieves a low AC/DC resistance ratio and equal
current sharing between parallel layers. It also blocks the path from primary to the core and so minimizes CM noise generation through the core. This structure has been used in the experimental section to confirm the validity of the proposed methods and techniques.

As mentioned in the first section of this chapter (section 4.1.3), if the number of turns is small, single-turn copper foil layers can be used to make both windings. Figure 4.17 shows three different paired-layers interleaved structures with a different number of layers for 8:4 turns ratio. Layers layout and paired layers have been shown in Fig. 4.6(a). These layers are designed for ER/51/10/38 core and the copper thickness is 0.25 mm. As shown in Fig. 4.17, all of these structures satisfy the requirement of no CM noise generation, as only paired layers overlap in these structures. Besides, all of these structures start and end with secondary layers, and so they block the CM noise path from the primary winding to the core. Figure 4.17(a) shows a structure with 12 layers for an 8:4 PT (8 layers for the primary and 4 layers for the secondary). Since there are only two sets of paired layers, only two intersections are possible for this condition. Figure 4.17(b) shows

Figure 4.17: Different paired-layers structures with no CM noise generation for an 8:4 transformer. The layout of primary and secondary PCBs were shown in Fig. 4.6(a). Implementation of the method with a) 12 layers, b) 20 layers and, c) 24 layers. Parallel layers have the same name and are identified using small rectangles of the same color. The thickness of layers are 0.25 mm and the AC resistance results are reported at 200 kHz.
another structure for the same turn ratio. This structure has 20 layers (10 layers for primary and 10 layers for secondary). In this figure, parallel layers are identified using small rectangles that have the same color. Investigating this structure also reveals that only paired layers overlap, and therefore, this structure does not generate CM noise. Based on FEA results, the total AC resistance of winding reflected to the primary side is reduced from 58.66mΩ to 28mΩ, which is the result of using more layers and a more interleaved structure. Finally, Fig. 4.17 (c) shows another structure for the same turns ratio, but with 24 layers (12 layers for both primary and secondary). This figure shows that only paired layers of primary and secondary overlap in this structure; therefore, it generates no CM noise. FEA results also confirm that this structure is more successful in minimizing AC resistance and leakage inductance than the previous structures, as it has a highly interleaved structure. These examples confirm that paired-layers interleaving method is general and can be applied for different turns ratios, different numbers of layers, and different types of layers.

4.4.2 Implementation of the Paired-Layers Method in Center-Tapped LLC PTs

The transformer’s voltage distribution is similar in two-winding and center-tapped transformers. Therefore, the presented PT structures of previous sections also can be used for center-tapped PTs to avoid CM noise generation. For instance, the same structures of Fig. 4.16 that were used for 16 : 8 turns ratio can also be used for 16 : 4 : 4 turns ratio and no CM noise would be generated. However, unlike two-winding transformers, the secondary winding in center-tapped transformers is divided into two windings and only one of these windings conducts at a time. Therefore, for the same turns ratio, the distribution of leakage flux in a center-tapped transformer is different from a two-winding transformer. Center-tapped transformers are used when low voltage and high current are needed at the output. Secondary windings have few turns (one or two turns are common) and they conduct large amounts of current. As the current is high, secondary turns can be realized using copper foil layers (instead of PCB) to increase current handling capability. The objective of this part is to show different approaches in implementing the paired-layers method in center-tapped PTs and to study the performance of these transformers.

Similar to two-winding transformers, depending on the design specifications, different structures can be used to make a center-tapped transformer. The only requirement is that the overlapping layers of the primary and secondary have the same number of turns and the same \( \frac{dv}{dt} \). Figure 4.18 (a) shows primary PCB layout and secondary copper-foil layers that satisfy this condition for 16 : 2 : 2 turns ratio. For this turns ratio, P(01) and P(02) are paired with S(02) and S(01), respectively, and only these turns are allowed to overlap. As shown in Fig. 4.18 (a), the top layer of the primary (P(01)) overlaps with S(02) and the bottom layer of the
Figure 4.18: a) The proposed primary and secondary layouts for a 16:2:2 center-tapped PT to eliminate CM noise. b) The implementation of the transformer with minimum number of layers. c) An interleaved structure by using three parallel windings for both primary and secondary windings. The thickness of PCB traces and secondary layers are 3oz and 0.25mm, respectively, and the AC resistance results are reported at 200kHz.
primary (P(02)) overlaps with S(01). Therefore, these layouts satisfy the requirement of the method. In the most basic form, a non-interleaved structure with the minimum number of layers (one PCB for primary and one copper foil layer for each secondary turn) can be used to make a 16:2:2 PT. If using more layers and interleaved structures is possible, parallel layers can be used to reduce DC and AC resistance. Fig. 4.18(b) and (c) show two different structures for 16:2:2 turns ratio. In this figure, layers of one secondary winding (S(01) and S(02)) are shown with purple color and layers of the other secondary winding (S(03) and S(04)) are shown with blue color. As mentioned earlier, each of the secondary windings conducts for half of the switching period. So each structure has been simulated twice and each time only one of the secondary windings is conducting. Fig. 4.18(b) shows an interleaved structure with the minimum number of layers for this turns ratio. In this structure, only paired layers are overlapping and the core is only exposed to secondary layers. Therefore, this structure does not generate CM noise. If the use of more layers is possible, a number of Fig. 4.18(b) structure can be connected in parallel to reduce windings’ resistance. Figure 4.18(c) shows another structure that is made by connecting three structures of Fig. 4.18(b) in parallel. In this case, the DC resistance is reduced by a factor of three and the use of a more interleaved structure has helped to reduce AC resistance.

Fig. 4.19 shows one implementation of the method for 16:1:1 turns ratio. In this case, the only paired turns are P(1) and S(1) and no other turns of primary and secondary can overlap. Figure 4.19(a) shows the primary PCB layout and secondary copper foils to satisfy this condition. According to Fig. 4.19(a), the primary PCB is designed in such a way that both top and bottom layers only have P(01) (which means that the top and bottom layers have the same turn and are connected in parallel) and P(02) – P(16) are placed on the middle layers of PCB. Figure 4.19(b) shows an interleaved structure using these layouts. The structure is such that the primary PCB always overlaps with S(01) and so it does not generate CM noise. One downside of this structure is the non-symmetrical placement of secondary windings. This causes the leakage inductance of secondary windings to be different, which is not desirable from the circuit operation point of view. In addition, the layers of the non-conducting secondary in each half-cycle are exposed to large values of leakage flux, which induces extra eddy current loss in those layers.

These issues can be solved by using the winding layout and structure of Fig. 4.20. As shown in this figure, it is possible to make a pair for S(2) on the primary side by adding an extra turn to the primary winding. According to Fig. 4.20, the primary winding has 17 turns. However, the first turn is open and the winding starts after the first turn. This turn is only connected to the primary winding from one end and is open at the other end. By doing this, the $\frac{dv}{dt}$ of this extra turn will be similar to S(2). Figure 4.20(a) shows
Figure 4.19: a) First proposed primary and secondary layouts for 16:1:1 center-tapped PT. Only S(01) and P(01) are allowed to overlap in this scheme. b) An interleaved structure that has a low AC resistance and no CM noise generation. The thickness of PCB traces and secondary layers are 3oz and 0.25mm, respectively, and the AC resistance results are reported at 200kHz.

the PCB layout that implements this idea. By using this PCB layout, both S(1) and S(2) can overlap with the primary, and so it is possible to use the symmetrical structure of Fig. 4.20(b). This structure achieves similar leakage inductance for secondary windings and also is designed in such a way that the non-conducting layers are always next to locations that have minimum leakage flux. As a result, this structure significantly reduces the loss associated with eddy current in the layers of non-conducting secondary.

As explained before, in traditional PCB layouts, turns are equally shared between layers of PCB. However, using the paired-layers method causes the primary turns not to be shared equally between PCB layers.
Figure 4.20: a) Second proposed primary and secondary layouts for 16:1:1 center-tapped PT. An additional open-ended turn (called P(-1)) is added to the primary that creates a pair for S(02). In this scheme, S(01) can overlap with P(01) and S(02) can overlap with P(-1). b) An interleaved structure using these layouts that has symmetrical secondary windings, low winding loss, and no CM noise generation. The thickness of PCB traces and secondary layers are 3oz and 0.25mm, respectively, and the AC resistance results are at 200kHz.

As shown in Figs. 4.19 and 4.20, for large turns ratios, most of the primary turns are placed on mid-layers and the top and bottom layer is not used effectively which increases the primary winding resistance. However, since the dominant source of loss for this turns ratio is the secondary windings, which is not affected by the use of the proposed method, this increment in primary resistance does not have a significant effect on the total loss of the PT. In order to quantify the extra loss that is caused by using the proposed PCB layouts, the loss of an equivalent traditional PT has been analyzed using FEA. Fig. 4.21 shows a PT with a traditional PCB layout for primary and the same structure as Fig. 4.20(b). According to this figure, using the proposed winding layout increases the transformer’s loss from 4.4W to 5W. Although the conduction loss is increased...
a bit in the proposed PT, this extra loss is justified by considering the benefits of minimizing the transformer’s CM noise. These benefits include the use of smaller and cheaper CM chokes in the converter’s EMI filter. Smaller CM chokes also have a lower loss which compensates for the extra loss in the transformer.

In this section, the proposed winding layouts of section 4.1 have been used to design several LLC PTs for different turns ratios. It was shown that the proposed winding layouts can be used to design interleaved structures with low AC resistance and no CM noise generation: two features that do not come together using the traditional transformer designs. The proposed method is general and can be applied to different turns.
4.4.3 Experimental Verification

In order to confirm the validity of the proposed methods, extensive experimental tests were done. An 800W LLC resonant converter was used to evaluate the performance of paired layers interleaving in terms of CM noise reduction. The experimental platform is shown in Fig. 4.22 (a). Tests were performed using the suggested setup for measuring conducted noise, and Line Impedance Stabilization Networks (LISN) and spectrum analyzer have been used at the input of the converter to measure the noise. As the proposed method only targets CM noise, Differential-Mode (DM) noise was eliminated from the measured noise and the comparison has been made on CM noise only. The parameters of this experimental platform are shown in Table 4.2.

Three transformers have been manufactured and tested to show the advantages of the proposed method. Figure 4.22 (b) shows these three transformers. The first transformer is a regular 16 : 8 PT. The layout

<table>
<thead>
<tr>
<th>LLC Converter</th>
<th>Test Equipments</th>
<th>Transformers’ Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>400v</td>
<td>LISN II-125A</td>
</tr>
<tr>
<td>$V_o$</td>
<td>100V</td>
<td>Spectrum Analyzer RSA360B</td>
</tr>
<tr>
<td>$P$</td>
<td>800 W</td>
<td>$N_p/N_s$ 16:8 and 16:1:1</td>
</tr>
<tr>
<td>$f_r$</td>
<td>200 kHz</td>
<td>PCB Trace Thickness 3 Oz</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>200 kHz</td>
<td>Copper Foil Thickness 0.25 mm</td>
</tr>
<tr>
<td>MOSFET</td>
<td>IXFH60N65X2</td>
<td>PCB Thickness 1mm</td>
</tr>
<tr>
<td>Diode</td>
<td>B40250TG</td>
<td>Core E43/10/28 3F3</td>
</tr>
</tbody>
</table>

Table 4.2: Experimental Platform Specifications

Figure 4.22: a) Test setup for measuring conducted mode noise. b) Prototypes of transformers under study.
and structure of this transformer are shown in Fig. 4.23(a). The second transformer is a 16 : 8 PT that is made using the paired layers interleaving method. The layout and structure of this transformer are shown in Fig. 4.23(b). According to Fig. 4.23(b), the top layer of the primary PCB and the bottom layer of the secondary PCB in the proposed PT have similar $\frac{dv}{dt}$ and so their overlapping is expected not to generate noise. The same is true for the bottom layer of the primary PCB and top layer of the secondary PCB in the proposed PT. As shown in Fig. 4.23 both transformers have the same structure and so the same number of overlapping between primary and secondary layers. This means that the static inter-winding capacitance (measured between primary and secondary windings) is approximately equal. It will be shown that while both transformers have a similar inter-winding capacitance, the proposed PT generates significantly less CM noise, which is the result of overlapping layers with similar $\frac{dv}{dt}$. To confirm this claim, these PTs were

![Figure 4.23: The comparison of the proposed PT with a traditional PT for 16 : 8 turns ratio. PCB layouts, structure, current distribution in layers, and loss results for a) the traditional PT and b) the proposed PT. The thickness of PCB traces and secondary layers are 3oz and 0.25mm, respectively, and frequency is 200kHz.](image-url)
Figure 4.24: Comparison of conducted noise of the LLC converter with a) the regular PT and b) the proposed PT. Using the proposed method significantly reduces the CM noise which results in smaller filter size and enhanced power density of the converter.

Employed in the LLC resonant converter and the CM noise of the converter in each case was measured. Figures 4.24(a) and (b) show the measured CM noise of the converter with the regular PT and the proposed PT, respectively. As shown in this figure, the proposed PT generates significantly less CM noise in most frequencies and the difference reaches 20.29 dBuV. This means that much smaller CM chokes are required to filter CM noise, considerably increasing the power density of the converter.

The proposed concept and method have also been verified by another experiment. For this experiment, a 16 : 1 : 1 PT was manufactured and tested under different conditions. This transformer, along with its primary PCB and secondary copper foil, is presented in Fig. 4.22(b). The PCB layout of the primary, the layout of secondary copper foils, and the transformer’s structure are similar to those in Fig. 4.20. If the quiet point of the primary (the terminal that goes to the DC bus) is connected to the first turn of primary (the one that overlaps with secondary), the $\frac{dv}{dt}$ of overlapping primary and secondary layers would be similar, and so it is expected no CM noise will be generated as a result of this overlapping. However, if the quiet terminal of the primary is connected to the sixteenth turn of primary, it causes very large $\frac{dv}{dt}$ on the turns that overlap with secondary layers. In this case, $\frac{dv}{dt}$ of overlapping primary and secondary layers are very different which

Figure 4.25: CM noise of the converter with different connections. a) incorrect connection and b) correct connection. It is necessary that quiet point is connected to the first turn of the primary winding, so overlapping layers of primary and secondary have a similar $\frac{dv}{dt}$.
causes a significant amount of CM noise. Figure 4.25 shows the CM noise of the converter with the same transformer under different conditions. As shown in this figure, the same transformer generates significantly lower CM noise if the quiet point of the converter is connected to the correct terminal of the primary winding. This result shows the significant effect of $\frac{dv}{dt}$ of overlapping layers which makes for another proof of concept of the method.

In this section, experimental tests have been presented to validate the paired layers interleaving method. Using the proposed method, the converter’s CM noise has been reduced significantly in most frequencies and the attenuation reaches 20.29 $dB\mu V$. This CM noise reduction results in smaller CM choke filters and improves the power density of the converter.

4.5 Summary

In this chapter, the concept of paired layers have been combined with interleaving methods to design PTs that have it all: low leakage inductance, low AC resistance, and almost zero CM noise generation. Depending on the number of turns, different winding layouts for implementing paired layers concept using multi-layer PCBs, copper foils or a combination of both have been investigated and proposed. The effect of winding arrangement on AC resistance has been briefly discussed and interleaving methods to reduce AC resistance have been presented. Once the concept of paired layers is combined with interleaving methods, the resulting method is called paired layers interleaving.

Paired layers interleaving was used to design a number of Forward/Flyback PTs for different turns ratios. These designs have been validated using FEA and it was shown that they all have low leakage inductance and AC resistance which is the result of their highly interleaved structures. Experimental tests were used to confirm the superiority of the proposed PTs regarding CM noise reduction. In one case, it was shown that a Flyback PT designed with paired layers interleaving generates even less CM noise than a wire-wound transformer that only has 7$pF$ parasitic capacitance. This example shows that paired layers interleaving does not address the CM noise problem by reducing the parasitic capacitance. Instead, it avoids CM noise generation by making the $\frac{dv}{dt}$ of overlapping layers similar. In other words, PTs designed with paired layers interleaving have large parasitic capacitance, but they do not generate CM noise.

Paired layers interleaving was also used to design a number of LLC PTs for different turns ratios, and different types of windings (two-winding, center-tapped). Since only half of the secondary turns have a pair on the primary, an extension of the paired layers concept was also introduced which creates pairs for these turns by adding auxiliary open-ended turns to the primary. The proposed LLC PTs were analyzed using FEA.
and it was shown that they all have low AC resistance and leakage inductance. Experimental tests have been done for two cases and it was shown that a LLC PT designed with paired layers interleaving generates up to 20.29 less CM noise than does an equivalent regular PT.
As explained in chapter 1, capacitive effects in the transformers are divided into inter-winding and intra-winding capacitors. While intra-winding capacitance originates from the capacitive coupling between layers of the same winding, inter-winding capacitance is the result of capacitive coupling between layers of different windings (i.e. one from primary and another form secondary). These parasitic capacitors are distributed and are visualized in Fig. 5.1 (a). The total effect of distributed parasitic capacitance can be modeled by six different capacitors in the transformer equivalent circuit, which is shown in Fig. 5.1 (b). The distributed intra-winding capacitance of each winding can be modeled as a lumped capacitor between terminals of that winding. These capacitors are shown with the purple color in Fig. 5.1. On the other hand, the effect of distributed inter-winding capacitance can be modeled by four capacitors between primary and secondary ports of the transformer which are shown in red color in Fig. 5.1.

Both intra- and inter-winding parasitic capacitors have detrimental effects on the performance of DC–DC converters. The high intra-winding capacitance gives rise to a high charging current at the transformer input, resulting in lower efficiency and increased peak voltage stress across secondary rectifying devices. In addition to those problems, parasitic capacitances also bring unwanted regulation issues for LLC resonant converters with wide output regulation. The effect of inter-winding capacitance is even worse, as it is one of the main sources of CM noise in the power converter. In previous chapters, paired-layers interleaving was introduced as a method that avoids CM noise generation when primary and secondary layers overlap. The basis of this method is to avoid CM noise generation by only overlapping layers that have a similar

\[1\] Portions of this chapter have been published in [5–7].
Figure 5.1: a) Distributed parasitic capacitance in PTs. b) Transformer’s equivalent circuit.

\( \frac{dv}{dt} \). Without going to details of the transformer’s parasitic capacitance model (which was presented in the previous chapters), this can be explained by (5.1) which presents the general relationship between voltage and current of a capacitor.

\[
i = C \left( \frac{dv}{dt} \right)
\]  

(5.1)

Paired-layers interleaving makes CM noise equal to zero by making \( \frac{dv}{dt} \) term equal to zero. Another method of reducing CM noise is to reduce the value of parasitic capacitance. In this chapter, methods of reducing both intra-winding and inter-winding capacitors are presented for PTs that are made using multiple-turn PCB windings. In particular, the detrimental effect of intra-winding capacitance on voltage regulation of LLC resonant converter under light-loading condition is considered, and layouts that have a significantly lower intra-winding and inter-winding capacitors are proposed to resolve this problem.

5.1 Effect of Parasitic Capacitors on Light-Load Voltage Regulation of LLC Resonant Converter

In a high-frequency LLC converter, magnetic components often are the bulkiest parts, and they determine the overall height of the converter [74]. Due to the height of traditional magnetic cores, the form factor of LLC chargers is often plump and bulky. In order to implement slim profile converters, PTs can be used featuring low height, reproducibility, lower leakage inductance, and low thermal resistance.

Despite the promising low profile and manufacturing advantages of PTs, their inherent high parasitic capacitances result in severe problems for LLC converters. Figure 5.2 (a) presents a LLC resonant converter schematic and includes parasitic elements of the transformer (leakage inductances, winding resistances, and parasitic capacitors). Figures 5.2 (b), (c), (d) and (e) present the problems that arise from transformer’s parasitic capacitances. As discussed, the high inter-winding capacitance between primary and secondary
generates CM noise and contributes to EMI issues. Complying with EMI standards requires significant effort to reduce CM noise, especially if the noise level is high. Usually, high EMI noise requires a bulkier filter that consequently increases the volume and cost of the system. In isolated power supplies, reducing inter-winding capacitance decreases CM noise amplitude significantly, simplifies the filter design and shrinks the

**Figure 5.2:** (a) The LLC resonant converter considering parasitic elements of the transformer and one capacitor model of the transformer (1) (b) Transformer distorted no-load voltage due to the stray capacitance (2), (c) The no-load voltage gain characteristics of the converter with different transformers: Unfortunate increase of voltage (3) and deviation of experimental characteristics from FHA prediction with high stray capacitance (4) (d) CM noise problem due to the inter-winding capacitance (5), (e) A portion of the transformer consisting of one primary PCB and two secondary PCBs (each PCB is a double layer PCB).
total filter size. On the other hand, the high intra-winding capacitance brings unwanted regulation issues for LLC resonant converters with wide output regulation. Voltage regulation is a critical specification in power converters to accommodate input voltage fluctuations (e.g., line regulation) or output voltage changes (e.g., battery chargers). The large parasitic capacitance of the transformer severely distorts the light-load current and voltage waveforms of the converter, leading to unpredictable behavior of output voltage which cannot be seen by First Harmonic Approximation (FHA). A typical waveform of the transformer voltage in this condition is presented in Fig. 5.2 (b). Since the requirement of applying FHA in resonant converters is having square shape voltage and sinusoidal current of the same frequency, applying FHA under this condition leads to inaccurate results. Solid and dashed curves in Fig. 5.2 (c) present the light-loading voltage gain characteristics of the LLC resonant converter with experimental measurements and FHA for different values of stray capacitance, respectively. The solid curves show that large parasitic capacitance leads to unpredictable behavior of output voltage and therefore, loss of the regulation. This figure also shows that although FHA can predict an unfortunate increase in the voltage gain due to the parasitic capacitances which limit the ability of the converter to handle low conversion ratios (e.g., low output voltages or high input voltage), it fails to accurately predict the output voltage. As it was mentioned before, this discrepancy in the results is due to the parasitic capacitance that distorts the voltage and current waveforms and leads to regulation problems for LLC resonant converters. It is worth mentioning that the FHA curves are found by combining the effect of all parasitic capacitors into one parallel stray capacitance that is shown in Fig. 5.2 (a). The required equations for getting the value of this stray capacitance based on the six-capacitor model of the transformer will be presented in the next sections. Reducing the value of this capacitor can significantly improve the situation and resolve the regulation problem.

This chapter characterizes the PT capacitance issue in detail and proposes mitigation strategies to improve the performance of LLC converters with PTs. A systematic analysis is performed, and six improved PT winding layouts are introduced and benchmarked with a traditional design. As a result of the investigation, an optimized transformer is obtained to minimize PT parasitic capacitance while maintaining low AC resistance. For each proposed winding layout, the analytical equations describing the parasitic capacitance are found, and the advantages and disadvantages of each layout are presented. In addition to the proposed winding layouts and arrangement, a comprehensive procedure to extract all parasitic elements of PTs are provided, which can be used to run FEA simulations of the electro- and magneto-static behavior of PTs. Experimental results show that the proposed transformers have up to 21.2 and 16.6 times less intra- and inter-winding capacitance, without compromising the resistance. This significant parasitic capacitance
reduction considerably improves the performance of the converter. Experimental results of employing the proposed transformers in a 1.2 kW LLC resonant converter show that the proposed transformers can successfully resolve both CM noise and voltage regulation problems in the LLC resonant converter and can regulate the output voltage even under no-load condition. In addition to these benefits, the converter efficiency increases due to the elimination of the parasitic capacitance.

5.2 Transformer Parasitic Element Extraction Using FEA

As mentioned before, high parasitic capacitances of the transformer have severe detrimental effect on the voltage regulation and CM noise of the LLC resonant converter. In order to attain high conversion efficiency and wider output regulation in LLC resonant converters, PT stray capacitance should be minimized as much as possible while keeping AC resistance low. In this section, a comprehensive study of transformer parasitic elements is presented and a full procedure of getting the equivalent circuit using FEA is proposed with the objective of designing low parasitic PTs to address regulation problems in LLC converters.

5.2.1 Parasitic Capacitance

The procedure for extracting the six-capacitor equivalent circuit of the transformer was presented in 2.4. As discussed, three different analyses are required to find six-capacitor model which are presented in Figs. 5.3 (b), (c) and, (d). Based on these analyses, Table. 5.1 presents relationships that can be used to find the value of each lumped capacitor.

In order to evaluate the overall impact of parasitic capacitance on the voltage regulation, the six-capacitor should be converted to the one capacitor model of Fig. 5.2. The expression for calculating this capacitance depends on the connection between primary and secondary windings. Fig. 5.4 (a) shows the six-capacitor model of the transformer with three independent voltages. If there is no connection between the primary and

![Diagram](image_url)

**Figure 5.3:** Electrostatic behavior model of the transformer: (a) Six-capacitor model with three independent voltages, (b), (c), and (d) the required numerical analysis to extract the six-capacitor model.
Table 5.1: Equations describing parasitic capacitances based on the field analysis

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{13}$</td>
<td>$-\frac{1}{2V_1V_2} \int_V (\vec{E}_1 \cdot \vec{D}_2 + \vec{E}_2 \cdot \vec{D}_1) dV$</td>
</tr>
<tr>
<td>$C_{14}$</td>
<td>$-\frac{1}{2V_1V_o} \int_V (\vec{E}_1 \cdot \vec{D}_o + \vec{E}_o \cdot \vec{D}<em>1) dV - C</em>{13}$</td>
</tr>
<tr>
<td>$C_{23}$</td>
<td>$\frac{1}{2V_1V_o} \int_V (\vec{E}_2 \cdot \vec{D}_o + \vec{E}_o \cdot \vec{D}<em>2) dV - C</em>{13}$</td>
</tr>
<tr>
<td>$C_{12}$</td>
<td>$\frac{1}{V_1V_2} \int_V (\vec{E}<em>2 \cdot \vec{D}<em>1) dV - C</em>{14} - C</em>{13}$</td>
</tr>
<tr>
<td>$C_{34}$</td>
<td>$\frac{1}{V_1V_2} \int_V (\vec{E}<em>o \cdot \vec{D}<em>2) dV - C</em>{13} - C</em>{23}$</td>
</tr>
<tr>
<td>$C_{24}$</td>
<td>$\frac{1}{V_1V_2} \int_V (\vec{E}<em>o \cdot \vec{D}<em>o) dV - C</em>{13} - C</em>{23} - C_{14}$</td>
</tr>
</tbody>
</table>

secondary windings, the offset voltage between two windings can be found using the following relationship [5].

$$V_{ofs} = \frac{(C_{13} + C_{14})V_1 - (C_{13} + C_{23})V_2}{C_{13} + C_{14} + C_{23} + C_{24}} \tag{5.2}$$

Having the offset voltage as a function of primary and secondary voltages, the six-capacitor model can be reduced to the three capacitors of Fig. 5.4 (b). The expressions for these capacitors can be found by equating

\[ \text{Figure 5.4:} \ a) \text{ Six-Capacitor model of the transformer, b) the three capacitance model of the transformer, c) the equivalent model of the transformer referred to the primary, and d) the one capacitor model of the transformer} \]
the electrostatic energy of this circuit to the energy of the six-capacitor model and replacing $V_{os}$ with $5.2$. These three capacitors then can be referred to the primary side which is shown in the Fig. 5.4 (c). Using the equations that are provided in [90], expressions for these capacitors are presented in (5.3).

$$
C'_p = (C_{12} + C_{14} + C_{13}) - \frac{(C_{14} + C_{13})^2}{C_{13} + C_{14} + C_{23} + C_{24}} + k(-C_{13} + \frac{(C_{14} + C_{13})(C_{23} + C_{13})}{C_{13} + C_{14} + C_{23} + C_{24}})
$$

$$
C'_s = k^2(C_{34} + C_{23} + C_{13} - \frac{(C_{23} + C_{13})^2}{C_{13} + C_{14} + C_{23} + C_{24}}) + k(-C_{13} + \frac{(C_{14} + C_{13})(C_{23} + C_{13})}{C_{13} + C_{14} + C_{23} + C_{24}})
$$

$$
C'_{ps} = -k(-C_{13} + \frac{(C_{14} + C_{13})(C_{23} + C_{13})}{C_{13} + C_{14} + C_{23} + C_{24}})
$$

(5.3)

The circuit shown in Fig. 5.4 (c) can be simplified further if the leakage inductances are negligible in comparison to the magnetizing inductance (which is the case for planar transformers). Under this condition, the capacitance $C_{ps}$ is short circuited and $C'_p$ and $C'_s$ are in parallel. Figure 5.4 (d) shows the one capacitor model of the transformer. The expression for the stray capacitance in this circuit is presented in (5.4).

$$
C_{stray} = C'_p + C'_s
$$

$$
= C_{12} + k^2C_{34} + \left(\frac{(C_{14} + C_{13})(C_{23} + C_{24}) + k^2(C_{13} + C_{23})(C_{14} + C_{24})}{C_{13} + C_{14} + C_{23} + C_{24}}\right) + 2k\left(\frac{C_{14}C_{23} - C_{13}C_{24}}{C_{13} + C_{14} + C_{23} + C_{24}}\right)
$$

(5.4)

Where $k$ is the transformer turns ratio. Equation (5.4) shows that both intra- and inter-winding capacitors contribute to the parallel stray capacitance which leads to regulation problems. Therefore, both types of capacitors should be minimized to reduce the value of this capacitance and solve the voltage regulation problem in the LLC resonant converter.

Equation (5.4) and table 5.1 are useful tools in designing low parasitic capacitance PTs for LLC resonant converter. These equations can be used along FEA to investigate the parasitic capacitance of any design. Regarding CM noise, these equations split the inter-winding capacitance to the four capacitors of $C_{13}$, $C_{14}$, $C_{23}$ and, $C_{24}$ which is a great advantage in CM noise modeling. Regarding the voltage regulation problem, (5.4) can be used to evaluate the value of parallel stray capacitance and avoid the problem of voltage regulation in LLC resonant converters.

5.2.2 AC Resistance and Leakage Inductance Modeling

In order to design an optimized PT for the LLC resonant converter, not only parasitic capacitances should be minimized, but also AC resistance and leakage inductance of the transformer should be kept low. Therefore, it is also important to define a procedure for finding AC resistance and leakage inductance of the transformer.
Neglecting capacitive effects, the transformer is a two-port system whose equivalent circuit is shown in Fig. 5.5 (a). For a two-port system, the relationship between primary and secondary voltages and currents can be represented by a $2 \times 2$ matrix. However, finding the matrix impedance of Fig. 5.5 (a) is not straightforward. Thus, a minor circuit transform is required to get the impedance matrix. The parallel core resistance and magnetizing inductance can be converted to the series from using (5.5). Fig 5.5 (b) shows the modified equivalent circuit.

$$L_{ms} = \frac{Q^2}{Q^2 + 1} \times L_m , \quad R_{cs} = \frac{1}{Q^2 + 1} \times R_c , \quad Q = \frac{\omega L_m}{R_c}$$

(5.5)

The matrix representation of this circuit is expressed in 5.6.

$$Z = \begin{bmatrix}
(R_{ac1} + R_{cs}) + S(L_{lk1} + L_{ms}) & \frac{1}{n}(R_{cs} + SL_{ms}) \\
\frac{1}{n}(R_{cs} + SL_{ms}) & (R_{ac2} + \frac{1}{n^2}R_{cs}) + S(L_{lk2} + \frac{1}{n^2}L_{ms})
\end{bmatrix}$$

(5.6)

Arrays of matrix impedance can be found using field analysis which can be done with the aid of FEA. (5.7) and (5.8) present elements of each array based on the fields.

$$R_{ij} = \frac{1}{2 \times I_{i(pk)} \times I_{j(pk)}} \oint_V (\vec{J}_i \cdot \vec{J}_j + \vec{J}_j \cdot \vec{J}_i) \, dV$$

(5.7)

$$L_{ij} = \frac{1}{2 \times I_{i(pk)} \times I_{j(pk)}} \oint_V (\vec{H}_i \cdot \vec{H}_j + \vec{H}_j \cdot \vec{H}_i) \, dV$$

(5.8)

In the above equations, $J_i$ and $H_i$ are the current density and magnetic field due to the input current at the port $i$. Besides, $R_{ij}$ and $L_{ij}$ are resistance and inductance associated with the array $ij$ in the impedance matrix. In the case of two windings transformer, there are two ports and two different analysis are required to get corresponding current densities and magnetic fields. In finding field solution, eddy currents should be considered to investigate the impact of arrangement on the AC resistance and leakage inductance. After finding field solution for each case, superposition theorem will be used to calculate (5.7) and (5.8). Equating
the matrix produced with these equations with the transformer impedance matrix, the values of equivalent circuit can be found by (5.9).

\[
R_{ac1} = R_{11} - \frac{1}{k} R_{12} \quad L_{lk1} = L_{11} - \frac{1}{k} L_{12} \\
R_{ac2} = R_{22} - k R_{21} \quad L_{lk2} = L_{22} - k L_{21} \\
L_{ms} = \frac{1}{k} L_{12} \quad R_{cs} = \frac{1}{k} R_{12} \quad (5.9)
\]

Where \( k \) is equal to \( 1/n \). Having the required analysis to extract PTs’ parasitic elements, it is possible to design optimized PTs with low parasitic elements for the LLC resonant converter. These analysis tools are used through this paper to investigate different PT structures and designing low parasitic capacitance PTs for the LLC resonant converter with wide output voltage regulation.

### 5.3 Reduction of the Parasitic Capacitances

As discussed in section 5.1, the inter-winding capacitance makes the CM noise problem and the primary stray capacitance leads to a voltage regulation problem under light-loading condition. Therefore, efforts should be made to minimize parasitic capacitances of PT in the design stage. However, reducing the parasitic capacitance often leads to increment in resistance. Therefore, both of these parasitic elements should be considered at the same time to achieve high-efficiency and low-parasitic PT. In this section, a systematic analysis is performed, and six improved PT winding layouts are introduced and benchmarked with a traditional design. The analysis starts with the static capacitance between two layers of the traditional spiral winding layout and then the low parasitic capacitance layouts are introduced.

The value of the static capacitance between two conductive layers with an overlapping area of \( A_r \) and a separation distance of \( d \) is presented in (5.10).

\[
C_{static} = \varepsilon_0 \varepsilon_r \frac{A_r}{d} \quad (5.10)
\]

Where \( \varepsilon_r \) is the permittivity of the material between layers. For a transformer with \( m \) intersections of primary and secondary, the total value of static inter-winding capacitance is presented in (5.11).

\[
C_{static} = m \times \varepsilon_0 \varepsilon_r \frac{A_r}{d} \quad (5.11)
\]

The total value of inter-winding capacitance is equal to the sum of \( C_{13}, C_{14}, C_{23} \) and, \( C_{24} \) capacitors. There-
Therefore, reducing the total value of inter-winding capacitance means that the overall impact of inter-winding capacitance is reduced. Equation (5.11) shows that the total value of static inter-winding capacitance can be reduced by increasing the separation distance, reducing the overlapping area, reducing the number of intersections, and using low permittivity materials between layers. Increasing the separation distance reduces the value of capacitance. However, more distance means more space for insulation and less space for copper which leads to higher conduction losses. As a result, this method often sacrifices resistance to reduce parasitic capacitance. Reducing the overlapping area also reduces PCB utilization and increases the DC resistance. Also, this method suffers from high proximity effect that results in very high AC resistance. Therefore, among different factors, only the number of intersections and the permittivity of the material can be manipulated to reduce the static inter-winding capacitance. Reducing the number of intersections should be done by considering the proximity effect. While the Non-Interleaved (NI) structure has only one intersection, it cannot be used due to the high ratio of AC to DC resistance. The proposed methods and procedures in section 5.2 can be used to find an optimized transformer arrangement that minimizes both AC resistance and inter-winding capacitance. Using low permittivity material is a very effective method of reducing the static capacitance with no penalty on the other parasitic elements.

It should be mentioned that FR4 is the most widely used material for PCBs due to its electrical and mechanical properties. This material is flame resistant and provides up to 20 kV/mm electrical insulation. Despite these advantages, FR4 has a relatively high permittivity of 4.7. This high permittivity leads to a considerable parasitic capacitance between the top and bottom traces. Since commercial PCBs are usually manufactured using FR4, the parasitic capacitance between the top and bottom traces cannot be reduced by using another material. However, we are still able to use low permittivity materials between separate PCBs to reduce the parasitic capacitance between them. This option is only available in the windings realized by modularly stacked double-layers PCBs, as the material between PCBs are not necessarily FR4. As a result, windings made with double-layer PCBs are more customizable and capable of reducing parasitic capacitance than windings that are manufactured by multi-layer PCBs.

In order to explain how the material between PCBs affects the distributed parasitic capacitances, a cross-section of an 8 : 4 transformer is shown in Figs. 5.6 (a) and (b). The primary has four PCBs in parallel and each PCB has eight turns (four on the top and four on the bottom). The secondary also has four PCBs in parallel and each PCB has four turns. Figure 5.6 (b) shows a 2D cross-section of the transformer and explains how the PCBs are arranged. There are four intersections of primary and secondary PCBs. The material that is used in these intersections significantly affects the inter-winding capacitance. In multi-layer PCBs, this
**Figure 5.6:** a) The 3D model of a traditional 8:4 planar transformer with spiral winding and b) 2D cross section of the transformer, showing the arrangement of the transformer. Each primary PCB has eight turns (four on each side), and each secondary PCB has four turns (two on each side). The primary PCBs are connected in parallel and the secondary PCBs also are connected in parallel.

Material is FR4. However, in windings that are made with double-layer PCBs, low permittivity materials like air can be used. Figures 5.7 (a) and (b) show one of these intersections with FR4 and air used, respectively. These figures show that replacing FR4 with air reduces the static capacitance between successive PCBs roughly 4.7 times for the same structure. The separation distance can be realized using hollow frames. Figure 5.8 shows an example of a frame that can be used to provide air separation between layers. Since frames only are required in the soldering process (the transformer will maintain its physical structure after soldering), they may be designed in a way that allows them to be removed after the soldering. Although air effectively reduces the static capacitance between successive layers, it cannot provide the required insulation clearance between overlapping traces. Therefore, the required insulation clearance between layers can be

---

**Figure 5.7:** Inter-winding energy associated with one intersection of primary and secondary. All of the primary turns have voltage equal to 1V, and all of the secondary turns have voltage equal to 0V. The energy distribution: a) with FR4 between PCBs 101\(\mu\)J and b) with air between PCBs 25\(p\)J.
Figure 5.8: Example of the frame that is used for air separation. a) 3D model and b) physical frame realized by using one or two layers of Kapton tape.

Unlike inter-winding capacitance, finding the self-capacitance of two overlapping layers of the same winding requires calculating the total electrostatic energy in that layer. Figure 5.9 shows a double-sided PCB used as a winding in PTs. The analytical expressions for calculating the intra-winding energy between overlapping traces and adjacent turns are presented in (5.12) and (5.13).

\[
E_{\text{overlap}} = \int_{0}^{L} \frac{1}{2} \varepsilon_{0} \varepsilon_{r} \frac{W \times dx}{d} \left( \frac{V_{w}}{L} x \right)^{2} = \frac{1}{6} \varepsilon_{0} \varepsilon_{r} \frac{W \times L}{d} (V_{w})^{2} \quad (5.12)
\]

\[
E_{\text{adjacent}} = 2 * \int_{0}^{L} \frac{1}{2} \varepsilon_{0} \frac{t \times dx}{c} \left( \frac{V_{w}}{n} \right)^{2} = \varepsilon_{0} \frac{(n - 2) t \times L}{n^{3}} (V_{w})^{2} \quad (5.13)
\]

The parameters of (5.12) and (5.13) are presented in the table 5.2. The sum of these energies is equal to the energy stored in the lumped intra-winding capacitance. Equating the energy expressions, the value of

Figure 5.9: a) Traditional spiral winding layout: The distributed capacitance due to overlapping traces (1), the distributed capacitance between adjacent turns at the same side (2) and b) simplified view of the overlapping traces
Table 5.2: Parameters definition

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>Total length of turns in one side</td>
</tr>
<tr>
<td>W</td>
<td>Width of traces</td>
</tr>
<tr>
<td>d</td>
<td>Distance between two layers</td>
</tr>
<tr>
<td>c</td>
<td>Clearance between adjacent traces</td>
</tr>
<tr>
<td>t</td>
<td>Thickness of Copper</td>
</tr>
<tr>
<td>n</td>
<td>Total number of turns in PCB</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>FR4 permittivity</td>
</tr>
<tr>
<td>$A_t$</td>
<td>Total area of turns</td>
</tr>
</tbody>
</table>

lumped capacitor can be found using (5.14).

$$
C_{\text{intra}} = \frac{1}{3} \varepsilon_0 \varepsilon_r \frac{A_t}{d} + \frac{2(n - 2)}{n^3} \varepsilon_0 \frac{t \ A_t}{W \ c} \tag{5.14}
$$

In the equation above, the first term is associated with the overlapping turns and the second term shows the intra-winding capacitance due to the adjacent turns of the same side of PCB. In developing the second part, the fringing of electric field is ignored. In reality, due to the fringing of electric field, part of electric field reaches to the adjacent trace through the PCB. Therefore, the value of the second term is higher than what (5.14) predicts. However, since the thickness of the traces is much smaller than their width and the value of the second term is roughly proportional to $\frac{1}{n^2}$, the value of the second term is negligible in comparison to the first term. For the studied prototypes, the second term is less than three percent of the first term. Ignoring the second term, the intra-winding capacitance of Fig. 5.9 is presented in (5.15).

$$
C_{\text{intra}} \approx \frac{1}{3} \varepsilon_0 \varepsilon_r \frac{A_t}{d} = \frac{1}{3} C_{\text{static}} \tag{5.15}
$$

Equation (5.15) indicates that for the same area, the value of intra-winding capacitance of two overlapping layers of Fig. 5.9 is equal to one-third of the static capacitance between two layers. Since replacing FR4 with air only is applicable between different PCBs, this method cannot be used to reduce the capacitance between traces of the same PCB. However, if PCBs of the same windings are placed next to each other, air can reduce the value of static capacitance between layers of different PCBs. Figures 5.10 (a) and (b) show the intra-winding energy of two successive PCBs of the same winding with FR4 and air between PCBs, respectively. These figures confirm that air only can mitigate the intra-winding capacitance between layers of different PCBs. In other words, the overall impact of this method on the intra-winding capacitance is
much lower. Therefore, other methods should be used to reduce the intra-winding capacitance between traces of the same PCB. In the following subsections, six improved winding layouts with very low parasitic capacitances are proposed and compared regarding the parasitic capacitance and resistance. These winding layouts are shown in the figures 5.11 (b), (c), (d), (e), (f), and (g). For each winding layout, the analytical expressions describing DC resistance and intra-winding capacitance are proposed and verified with the aid of FEA. In comparison to the traditional spiral winding layout, the proposed layouts have up to 21.2 and 16.6 less intra- and inter-winding capacitances which significantly reduce the CM noise and solve the regulation problem in the LLC resonant converter, which is the objective of this section.

5.3.1 No Overlapping Winding Layouts

Minimizing the overlapping area is the first approach to reducing the intra-winding capacitance. Figure 5.11 (b) and (c) show minimized overlapping winding layouts. These winding layouts are called no overlapping winding layouts through this chapter. The energy stored in these winding layouts is proportional to the distributed capacitance between adjacent turns on the same side of PCB. The analytical expression for calculating the parasitic capacitance between adjacent turns is equal to the second term in (5.14). Figure 5.12 (b) shows the intra-winding energy associated with the layout of Fig. 5.11 (b). This figure shows that these layouts strongly reduce the intra-winding energy as the value of intra-winding energy is reduced from 33 pJ in the traditional design to 1.7 pJ. Regarding the inter-winding capacitance, these layouts offer double space between windings and reduce the value of static inter-winding capacitance. Although these layouts effectively mitigate the problem of intra-winding capacitances, they have higher DC resistance comparing to the traditional winding layout. In these layouts, only 50% of PCBs are used and consequently, the values
Figure 5.11: The proposed improved winding layouts to reduce the parasitic capacitances in LLC converters: a) Traditional spiral, b) and c) No overlapping, d) Optimized overlapping, e) Alternating, f) Alternating & no overlapping and, g) Zero voltage gradient winding layouts.
of DC resistances are roughly twice the traditional winding layout. Due to higher conduction loss, these designs are not suitable for high-efficiency LLC applications.

5.3.2 Optimized Overlapping Winding Layout

The second winding layout which attempts to reduce the parasitic capacitance with less resistance increment is shown in Fig 5.11 (d). The stored energy between overlapping traces depends on the voltage gradient of those traces. Therefore, the energy is not evenly distributed in the area between two layers, and more energy is stored between outer turns that have larger capacitance and voltage gradient. This feature is used in this layout to remove the overlapping area between the outer turns and effectively reduce the intra-winding capacitance. Removing the overlapping between these turns means that putting \((\frac{n}{2} + 1)\) turns on one side and \((\frac{n}{2} - 1)\) on the other side. For PCBs with the odd number of turns, it means having \((\frac{n+1}{2})\) turns on one side and \((\frac{n-1}{2})\) turns on the other side. This winding layout is called Optimized overlapping winding layout in this chapter. For even values of \(n\) the intra-winding energy and corresponding capacitance can be found using (5.16).

\[
E_{\text{intra}} = \int_0^{\frac{n}{2}+1} \frac{1}{2} \varepsilon_0 \varepsilon_r \frac{W}{d} \times \left( \frac{V_w (\frac{n-2}{n})}{\left(\frac{n}{2}+1\right)} \right)^2 = \left[ \frac{1}{2} \varepsilon_0 \varepsilon_r \frac{W}{d} V_w^2 \left(\frac{n}{2}+1\right) \right] \times \left[ \frac{n-1}{2} \left(\frac{n}{n} - 2\right)^2 \right] \\
C_{\text{intra}} = \left[ \frac{1}{3} \varepsilon_0 \varepsilon_r \frac{W \times L}{d} \right] \times \left[ \frac{n-1}{2} \left(\frac{n}{n} - 2\right)^2 \right] 
\] (5.16)
Following the same procedure for odd values of $n$, the intra-winding capacitance associated with this condition is presented in (5.17).

\[
E_{\text{intra}} = \int_0^L \frac{1}{2} \varepsilon_0 \varepsilon_r \frac{W \times dx}{d} \left[ V_w \frac{n-1}{n+1} L \right] \frac{dV_w}{L} \times \left[ \frac{n-1}{n+1} \right]^2 \] 

\[
C_{\text{intra}} = \left[ \frac{1}{3} \varepsilon_0 \varepsilon_r \frac{W \times L}{d} \right] \times \left[ \frac{(n-1)^3}{n^2(n+1)} \right] 
\] 

Assuming the total length of winding is equal to the traditional winding layout, DC resistance for each case is presented in (5.18).

\[
n = \text{Even} \quad R_{\text{DC-Opt}} = \left( \frac{n+2}{n} \right) R_{\text{DC-trad}} 
\]

\[
n = \text{Odd} \quad R_{\text{DC-Opt}} = \left( \frac{n(n+1)}{n^2+1} \right) R_{\text{DC-trad}} 
\] 

In the above equations, $R_{\text{DC-trad}}$ is the DC resistance of traditional spiral design. Figures 5.13 (a) and (b) show the normalized DC resistance and intra-winding capacitance of Optimized overlapping winding layout for different values of $n$. The base values for normalization are the DC resistance and intra-winding capacitance of traditional winding layout. These figures show that the value of intra-winding capacitance can be reduced effectively, without doubling the DC resistance. An eight-turn winding layout with this strategy is shown in Fig. 5.11 (d). The intra-winding energy distribution of this layout is shown in Fig. 5.12 (c). This figure shows that in the case of eight turns PCBs, removing the overlapping area between first and last turns reduces the intra-winding capacitance by 69%. This result is in a very good agreement with (5.16). The percentage of increase in the DC resistance can be calculated using (5.18) which is equal to 25%. In comparison to the no overlapping winding layouts that have 100% more DC resistance, the DC resistance increment in this layout is just 25%. Although this layout proposes a significant capacitance reduction by a small increment of resistance, the parasitic capacitance still is considerable and can lead to voltage regulation.

**Figure 5.13:** Variations of DC resistance and intra-winding capacitance of Optimized overlapping winding layout for a) even values of $n$ and b) odd values of $n
problems. Therefore, more optimized winding layouts should be investigated to strongly reduce the parasitic capacitance while not letting the resistance increase.

5.3.3 Alternating Winding Layout

No overlapping and optimized overlapping winding layouts are based on the overlapping minimization principle. Although effective in mitigating the intra-winding capacitance, these winding layouts sacrifice DC resistance to achieve this goal. The intra-winding capacitance also can be minimized by reducing the voltage gradient between overlapping traces. Minimizing voltage gradients between large overlapping traces reduces the intra-winding energy and consequently the intra-winding capacitor. One way to reduce the voltage gradient between overlapping traces is illustrated in Fig. 5.14 (a). This winding layout is called Alternating winding layout in this chapter. In this layout, the overlapping traces are two successive turns. In other words, after each turn, the next turn is on the other side. These turns are connected through VIA. For this layout, the intra-winding energy can be calculated by (5.19).

\[
E_{\text{intra}} = \int_0^L \frac{1}{2} \epsilon_0 \epsilon_r \frac{W \times dx}{d} \times \left( \frac{V_w}{n} \right)^2 = \left[ \frac{1}{2} \epsilon_0 \epsilon_r \frac{W \times L}{d} V_w^2 \times \left( \frac{4}{n^2} \right) \right]
\]

\[
C_{\text{intra}} = \left[ \frac{1}{3} \epsilon_0 \epsilon_r \frac{W \times L}{d} \right] \times \left[ \frac{6}{n^2} \right]
\]  

(5.19)

The above equation shows that this winding layout reduces the value of intra-winding capacitance by a factor of \( \frac{6}{n^2} \). Figure 5.14 (b) presents the intra-winding capacitance of this layout for different values of \( n \) and shows that the value of intra-winding capacitance rapidly decreases by increasing the number of turns. Regarding the DC resistance, this winding layout has no increment as all of the available PCB is used for copper traces. Figure 5.11(e) shows an eight turns Alternating winding layout. For the ease of connecting to other PCBs, the winding is started from the middle, and the terminals are at the edges of the PCB. The intra-winding energy distribution of this layout also is shown in Fig. 5.12(d). This figure shows that an eight turns Alternating winding layout has 10 times less intra-winding energy than the traditional winding layout which is in a good agreement with (5.19). In comparison to the previous designs, this layout reduces the intra-winding capacitance without sacrificing the DC resistance. Although this layout is a suitable candidate for wide-range and efficient LLC converters, it does not have any superiority in terms of the inter-winding capacitance. Besides, a large number of VIAs can increase the eddy current loss. Therefore, other winding layouts should be investigated to find an optimum layout that minimizes both types of parasitic capacitances.
Figure 5.14: a) Alternating winding layout with terminals at the outer edges of PCB and b) Variations of intra-winding capacitance of Alternating winding layout for even values of $n$

5.3.4 Alternating & No Overlapping Winding Layout

The minimized overlapping strategy also can be used to reduce the value of inter-winding capacitance. On this basis, Alternating & no overlapping winding layout with minimized overlapping of primary and secondary is shown in Fig. 5.11(f). This layout uses the alternating layout to reduce the intra-winding capacitance and avoids any overlapping between primary and secondary to minimize the inter-winding capacitance. Therefore, this transformer minimizes both intra and inter-winding capacitances. Due to the alternating layout and lower overlapping area between the traces of the same winding, the intra-winding capacitance of this layout is very low. Figure 5.12(e) shows the intra-winding energy of this layout which is roughly 15 times less than the traditional layout. Since the overlapping of primary and secondary is avoided in this structure, this layout also has lower inter-winding capacitance. On the downside, this layout only uses 50% of PCB and therefore has twice DC resistance. More importantly, this layout has a very high AC resistance due to the proximity effect. Therefore, it makes a lot of conduction loss and is not suitable for high efficiency LLC converters. This layout will be discussed more in the next section.

5.3.5 Zero Voltage Gradient Winding Layout

The final proposed winding layout for solving the parasitic capacitance problem is called Zero voltage gradient layout. In order to explain this winding method, an 8 : 4 transformer that is realized using double-layer PCBs is shown in Fig. 5.11(g). There are four different PCBs (two double-sided PCBs for the primary side, and two double-sided PCBs for the secondary side). This figure shows that the eight turns of the primary are split into two parts. The first four turns of the primary are duplicated on both sides of the first PCB of the
primary. The top and bottom layers of this PCB are connected in parallel, which means that this PCB has four turns out of the eight turns of the primary. Since the top and bottom layers of this PCB are identical and connected in parallel, they have the same voltage and there is no voltage gradient between the overlapping turns. This condition also can be seen from the direction of the turns in this PCB. The four remaining turns of the primary are duplicated on both sides of the second PCB of the primary. Similar to the first PCB, the top and bottom layers of this PCB are connected in parallel. The first four turns that are on the first PCB are then connected in series to the four turns of the second PCB via a middle connection, making an eight-turn primary winding. The same is true for the secondary winding. The key idea here is that the top and bottom layers of each PCB should be identical and connected in parallel to achieve zero voltage gradient and minimize the parasitic capacitance.

The proposal is implemented in Fig. 5.11 (g) by dividing each winding into two portions, duplicating each portion on the top and bottom sides of a separate PCB, and then connecting the two PCBs with a middle connection. In general, the proposal can be extended to dividing winding into any even number of groups. Different steps that are required to implement this proposal are provided as follows:

1. Each winding should be split into two (or any even number of) groups, and each group should be duplicated on both sides of a separate PCB. The minimum number of required PCBs for each winding is equal to the number of groups.

2. The top and bottom layers of each PCB should be connected in parallel.

3. Different PCBs should be placed separately to avoid the voltage gradient between them. All different PCBs should then be connected in series to make a complete winding. Middle connections are required to connect two successive PCBs. The number of required middle connections is equal to half the number of PCBs.

It can be seen that the above rules are applied to the transformer shown in Fig. 5.11 (g). In this case, each winding is divided into two groups, and two PCBs are required for each winding (one PCB for each group). Besides, one middle connection is required to connect these PCBs in series.

The intra-winding energy distribution of a PCB, the top and bottom layers of which are connected in parallel, and which has four turns on each side, is shown in Fig. 5.12 (f). Compared to the traditional winding method, the proposed method reduces the value of intra-winding energy from 33$pJ$ to just 1.1$pJ$, while maintaining the same overlapping area and without compromising DC resistance. This reduction in
parasitic capacitance is even greater than that provided by the minimized overlapping winding layouts that have double conduction loss.

As mentioned before, the minimum number of PCBs that are required for each winding in this method is equal to the number of portions into which the winding is divided. If the core windows can accommodate more layers, it is desirable to add extra layers in parallel to reduce the resistance. For example, in Fig. 5.15, the windings of the same transformer are realized by using four PCBs (two PCBs in parallel for each portion of windings). The PCBs that are connected in parallel are identical and both have the same portion of winding. Therefore, they also have the same voltage distribution. This characteristic can be used to reduce the inter-winding capacitance. Due to the zero voltage gradient between these PCBs, they can be placed very close together without raising concerns about increasing the intra-winding capacitance or violating the electrical clearance, which saves space in the limited height of the core windows. This space can be used to increase the number of layers or to increase the separation distance in the primary and secondary intersections to reduce the inter-winding capacitance. This advantage is shown in Fig. 5.15. This figure shows that identical PCBs are separated just by one Kapton layer, providing more separation distance for intersections of the primary and secondary. Therefore, this winding layout not only results in minimum intra-winding capacitance but also provides the opportunity to reduce the inter-winding capacitance. The benefits of this winding layout can be summarized as follows:

1. Extremely low intra-winding capacitance due to the zero voltage gradient between overlapping traces.
2. No increment in the value of DC resistance. The same DC resistance as in the traditional winding layout.

**Figure 5.15:** Zero voltage gradient transformer with the $P1S1P2P2S2P1$ structure. This figure shows that all overlapping traces of the same winding have zero voltage gradient.
3. Identical PCBs can be placed very close together without increasing the intra-winding capacitance. Therefore, there is more space to be used in the intersections of the primary and secondary, resulting in less inter-winding capacitance.

Since it results in very low parasitic capacitance, this layout can resolve both CM noise and light-load voltage regulation problems in the LLC converter; at the same time, it produces a low level of resistance, which ensures high full-load efficiency. Therefore, this layout is suitable for use with LLC resonant converters.

5.3.6 Comparison of the Proposed Winding Layouts

In the previous section, six improved winding layouts were proposed to minimize the parasitic capacitance of PT and consequently, solve problems due to the parasitic capacitance in the LLC resonant converter. Among the proposed winding layouts, those that reduce the parasitic capacitance by decreasing the overlapping have higher DC resistance. On the other hand, designs that minimize the parasitic capacitance by reducing the voltage gradient have the benefit of using all the available space and therefore do not compromise DC resistance. The DC resistance and intra-winding capacitance of different winding layouts are compared in Figs. 5.16 (a) and (b). Figure 5.16 (a) shows that all of the proposed winding layouts have considerably lower intra-winding capacitance than the traditional spiral layout.

No overlapping layouts can strongly mitigate the parasitic capacitance and solve the regulation problem. However, they also double the DC resistance which leads to higher conduction loss. Optimized overlapping layout is the optimized version of No overlapping layouts that reduces a big portion of parasitic capacitance by a small increase in the resistance. However, it is not as effective as No overlapping layout and since

![Figure 5.16](image)

**Figure 5.16:** Parasitic elements comparison of different winding layouts: a) Intra-winding capacitance and b) DC resistance
wide output regulation requires very low parasitic capacitance, it may not solve the regulation problem. *Alternating* layout also strongly reduces the intra-winding capacitance without increasing the DC resistance. Therefore, this layout can be used to resolve the regulation problem without compromising efficiency. However, it does not have an advantage over the traditional layout in terms of CM noise. In order to reduce both intra- and inter-winding capacitances, *Alternating & no overlapping* layout is proposed. Although this layout effectively reduces both parasitic capacitances, it has significantly higher AC resistance in comparison to other layouts which will be discussed more in the next section. Among different layouts, *Zero voltage gradient* layout offers the minimum intra-winding capacitance without any increment in the DC resistance. Reducing the intra-winding capacitance significantly enhances the converter performance and mitigates the regulation problem. In terms of inter-winding capacitance, this layout also provides the lowest inter-winding capacitance. Minimizing the inter-winding capacitance not only reduces the CM noise but also enhances the regulation.

### 5.4 Arrangement Tradeoff Analysis

In the previous section, improved winding layouts have been proposed to significantly reduce the parasitic capacitance and attenuate the CM noise and solve the voltage regulation problem in the LLC resonant converter. In addition to the winding layout, the structure of the transformer strongly affects the parasitic elements. It is interesting to note that there is a trade-off between intra-winding capacitance, AC resistance and leakage.
inductance against the inter-winding capacitance. The values of intra-winding capacitances, AC resistances, and leakage inductances decrease by using interleaved structures. On the other hand, the inter-winding capacitance is proportional to the number of intersections between primary and secondary which increases in the interleaved structure. Most of the proposed winding layouts in the previous section can effectively solve the intra-winding problem. Besides, the leakage inductances are inherently small in PTs comparing to the wire wound transformers and also the primary leakage inductance is capable of being absorbed by the series inductor. For these reasons, the trade-off analysis in finding the optimum arrangement is only made based on AC resistance and inter-winding capacitance. On this basis, the optimum structure is the one that minimizes the AC resistance with the minimum number of intersections between primary and secondary. Figure 5.17 shows the current density in the transformer with four layers of primary and secondary in different structures. This figure shows that the best current distribution between layers happens in the PSSPPSSP structure. In comparison to the Fully Interleaved (FI) structure, the number of intersections has reduced from seven to four, meaning the value of inter-winding capacitance is reduced roughly by 43%. This reduction in the parasitic capacitance can significantly attenuate the CM noise in LLC converters. The comparison of different structures regarding parasitic elements is presented in Figs. 5.18 (a) and (b). The stray capacitance in Fig. 5.18 (b) is calculated by using (5.4).

The proposed winding layouts also are investigated with different structures and in all cases, the proposed arrangement gives the best results. The only exception is the Alternating & No overlapping winding layout which has significantly larger AC resistance in all arrangements. Table 5.3 shows the ratio of AC to DC resistance of this layout in different structures.
Table 5.3: The ratio of AC resistance to DC resistance of Alternating & No overlapping winding layout in different structures

<table>
<thead>
<tr>
<th>Parameter</th>
<th>PPPSSSS</th>
<th>PPSSPSS</th>
<th>PSPSPSP</th>
<th>PSSPPSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{R_{ac}}{R_{dc}}$</td>
<td>168.6</td>
<td>184.28</td>
<td>212</td>
<td>201.5</td>
</tr>
<tr>
<td></td>
<td>48.1</td>
<td>48.1</td>
<td>48.1</td>
<td>48.1</td>
</tr>
</tbody>
</table>

This table shows that the interleaving does not solve the proximity effect for this winding layout. Since the primary and secondary turns do not meet each other, primary and secondary MMF do not cancel each other and the proximity effect leads to a high ratio of AC to DC resistance. Figure 5.19 compares the inter-winding energy of the traditional winding layout with the Alternating & No overlapping winding layout. This figure shows that even with no overlapping between primary and secondary, still there are some capacitive coupling between windings due to the fringing of the electric field. Indeed, even with no overlapping between primary and secondary, the value of inter-winding capacitance is half of the traditional winding layout. Considering the problem of AC resistance and the fact that inter-winding capacitance still has a large value, the minimization of overlapping between primary and secondary is not a practical way to mitigate the inter-winding capacitance problem. Instead, the inter-winding capacitance should be minimized through optimizing the structure, increasing the separation distance between windings and, using the low permeability materials in the intersections.

Having improved winding layouts and the optimized structure with low AC resistance and inter-winding capacitance, now we can fabricate very low parasitic capacitance PTs for high efficiency LLC resonant converter with wide output voltage regulation. These transformers can be used to resolve both CM noise and voltage regulation problems in the LLC resonant converter.

5.5 Experimental Results

To verify the theoretical hypothesis, the winding layouts under investigation were manufactured (total of 6) and employed in a 1.2kW LLC resonant converter. The experimental results show that the proposed PTs have extremely lower parasitic elements in comparison to the conventional PTs which mitigates the light-loading

![Figure 5.19](image_url)

**Figure 5.19:** Inter-winding energy of one intersection of primary and secondary windings with a) Traditional and b) Alternating & No overlapping layouts.
voltage regulation problem and also ensures high full-load efficiency by minimizing AC resistance and inter-winding capacitance. The specification of the converter and PTs are provided in Table 5.4. Figures 5.20 (a) and (b) show the prototypes of the special PTs under study and the LLC resonant converter platform, respectively.

**Table 5.4:** Parameters definition

<table>
<thead>
<tr>
<th>Converter Parameters</th>
<th>Transformer Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameters</td>
<td>Value</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>200 V</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>96 V</td>
</tr>
<tr>
<td>Output Power</td>
<td>1200 W</td>
</tr>
<tr>
<td>$f$</td>
<td>200 kHz</td>
</tr>
</tbody>
</table>

Figure 5.21 (a) shows the frequency response of different transformers with the secondary open. As long as the leakage inductances are negligible in comparison to the magnetizing inductance, the equivalent capacitor in this condition is equal to $C_{stray}$. Considering the fact that open circuit inductance is the same in all conditions, Fig. 5.21 confirms that the proposed transformers have significantly lower stray capacitance. Figure 5.21 (b) shows the stray capacitance of different layouts. Among different layouts, zero voltage gradient winding layout has the lowest primary parallel stray capacitance. In comparison to the traditional FI transformer, this transformer has 21.2 times less stray capacitance. Figure 5.21 (c) shows the inter-winding capacitance of the proposed transformers and shows that using an optimized structure and replacing FR4 with air significantly reduces the inter-winding capacitance. Among different layouts, zero voltage gradient winding layout again has the best result as its inter-winding capacitance is 16.6 times less than the

![Figure 5.20: Experimental prototypes: a) Transformers prototypes and b) LLC resonant converter platform](image-url)

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Figure 5.21: Parasitic values of the prototypes: a) frequency response, b) stray capacitance, c) inter-winding capacitance and d) AC resistance.

Figure 5.21: Parasitic values of the prototypes: a) frequency response, b) stray capacitance, c) inter-winding capacitance and d) AC resistance.

traditional FI structure. Figure 5.21 (d) shows the AC resistance of the proposed transformers. This figure shows that while some of the proposed layouts increase the resistance to reduce the parasitic capacitance, zero voltage gradient winding layout reduces the parasitic capacitance without increasing the resistance. Therefore, this transformer is the best one among the proposed transformers in terms of parasitic capacitance and AC resistance.

Figures 5.22 (a) and (b) show full-load waveforms of the LLC resonant converter with the traditional PT and the proposed zero voltage gradient transformer. Here, the inverter voltage is the output voltage of the full-bridge inverter. Comparing the waveforms shows that reducing the inter-winding capacitance reduces the high-frequency currents and considerably improves the current waveforms. Figure 5.23 (a) shows the transformer voltage under the no-load condition with the traditional PT. This figure shows that high stray capacitance distorts the transformer’s no-load voltage in such a way that it cannot be considered square-shaped. This distorted waveform makes serious problems in controlling output voltage under no-load and
Effect of large parasitic Capacitance

The effect of minimizing the parasitic capacitance is

\[ V_{\text{inv}} \]
\[ i_p \]
\[ V_s \]

light-load conditions which cannot be predicted with FHA. On the other hand, Fig. 5.23 (b) shows the no-load voltage of converter with the proposed zero voltage gradient transformer. This figure shows that even under no-load condition, the transformer voltage still is square-shaped.

Since large parasitic capacitances distort the transformer’s no-load voltage, FHA fails to consider all issues introduced by these parasitic capacitances and accurately predict the output voltage behavior. Fig. 5.24 (a), (b), and (c) compare the voltage characteristics of the converter with different transformers in three light-load conditions. This figure shows large stray capacitance leads to an unpredictable voltage behavior under no-load condition. Figures 5.24 (b) and (c) show increasing the load can somehow improve

Figure 5.23: Waveforms in the LLC resonant converter under no-load condition with a) traditional FI and b) zero voltage gradient transformers. Inverter voltage (Ch1), primary current (Ch2), and transformer secondary voltage (Ch3). Reducing the stray capacitances has improved no-load voltage waveforms and successfully mitigated the light-load voltage regulation problem.

Figure 5.22: Waveforms in the LLC resonant converter under full-loading condition with a) Traditional FI and b) zero voltage gradient transformers. Inverter voltage (Ch1), primary current (Ch2), transformer secondary voltage (Ch3), and transformer secondary current (Ch4). This figure shows that reducing the inter-winding capacitances has attenuated CM noise.
the situation. However, the voltage behavior still is unpredictable. In addition to the unpredictable behavior, the converter cannot regulate for low output voltages as shown in Fig. 5.24(c). Minimizing the parasitic capacitance can avoid these problems and enables the converter to regulate the output voltage. This figure shows that for the same sweep of frequency, the converter with zero voltage gradient transformer can provide wider ranges of output and regulate the output voltage.

PTs also are compared regarding the converter efficiency. Figure 5.24(d) shows the full-load efficiency of the converter at the resonant frequency with different transformers. This figure shows that zero voltage gradient transformer has the highest efficiency between different transformers. It is mainly due to low resistance and low CM noise. The efficiency of other transformers that have higher resistance is slightly lower. In the case of Alternating & No overlapping winding layout, as explained in the previous sections, the interleaving does not improve the AC resistance, and this transformer has much higher AC resistance.

Figure 5.24: Converter voltage gain characteristic with different transformers at a) no load, b) very light load and, c) light load. The conventional PT has serious regulation issues for all cases and the proposed Zero voltage gradient layout solves this problem by achieving an extremely low capacitance. d) Full-load efficiency of the converter at resonant frequency with different transformers.
Therefore, the efficiency of this transformer is considerably lower than other transformers. As a result, the non-overlapping strategy is not a suitable layout for high-efficiency applications.

5.6 Summary

This chapter presented the problems associated with the parasitic capacitance of PTs in LLC resonant converters and proposed mitigation strategies to reduce the parasitic capacitance and improve the converter’s performance. It was shown that the high inter-winding capacitance makes the CM noise problems while the parallel stray capacitance leads to voltage regulation problems under the light-loading condition. In order to overcome these problems, a systematic analysis was performed, and six improved PT winding layouts were introduced and benchmarked with a traditional design. The proposed winding layouts were compared regarding parasitic capacitance and resistance with the aid of analytical equations. As a result of the investigation, an optimized structure with minimum AC resistance and inter-winding capacitance was found and verified by FEA and experimental tests. The proposed winding layouts and structure were used to manufacture PTs with very low parasitic capacitance. While all of the proposed transformers significantly reduce the parasitic capacitances, the proposed Zero voltage gradient layout has the best results as it has 21.2 times less primary stray capacitance and 16.6 times less inter-winding capacitance. This structure reduces the stray and inter-winding capacitances from 618\(pF\) and 1414\(pF\) to 32\(pF\) and 85\(pF\), respectively. Another advantage of this transformer is that it reduces the parasitic capacitance without increasing the resistance and has the lowest parasitic capacitances and resistance at the same time. The experimental results of employing the proposed transformers in a 1.2\(kW\) LLC resonant converter shows that not only the proposed transformers have enhanced the performance and efficiency of the converter by minimizing AC resistance and inter-winding capacitance, but also have mitigated the voltage regulation problem and enabled the converter to regulate the output voltage even under no-load condition.

Besides the application in LLC resonant converters, the proposed winding layouts also can be used to design inductors that have a wide-range operating frequency. Since they exhibit much smaller self-capacitance, such inductors have a large self-resonant frequency which is very desirable in high-frequency applications.
Chapter 6

Conclusion

6.1 Conclusions and Contributions

Although PTs feature many advantages such as low height, excellent thermal characteristics, modularity, flexibility, repeatability, and ease of manufacturability, they exhibit large parasitic capacitances which results in severe problems for DC-DC converters. Large parasitic capacitance in PTs is due to the proximity of the planar layers and their significant overlap. In particular, parasitic capacitances in the transformers are divided into two groups: inter-winding and intra-winding capacitance. Intra-winding capacitance originates from the capacitive coupling between layers of the same winding, while inter-winding capacitance is the result of capacitive coupling between layers of different windings (i.e., one from primary and another from secondary). Inter-winding capacitance is the major source of CM noise in the converter which creates EMI issues. On the other hand, intra-winding capacitance affects the performance and efficiency of the converter and can result in loss of voltage regulation in LLC resonant converter.

Comparing to wire-wound components, parasitic capacitances of PTs can be two orders of magnitude larger. Such large values significantly deteriorate the performance of the circuit and cannot be ignored. Most of the publications for planar transformer design concern the reduction in leakage inductances and high-frequency winding losses, but winding capacitances have rarely been considered effectively. To fill this void, this dissertation focuses on parasitic capacitances of PTs and sheds light on the complex nature of capacitive effects in PTs. By targeting the root cause of problems, this work proposes new design methods that resolve problems that arise from the large parasitic capacitance of PTs. The following subsections summarize contributions of this work.
6.1.1 Detailed Parasitic Capacitance Model of PTs

Parasitic capacitances in PTs are distributed, as each overlapping in the PT structure contributes to parasitic capacitance. The total effect of distributed parasitic capacitance can be modeled by six lumped capacitors in the transformer equivalent circuit. In chapter 2, the energy method has been used to develop a general parasitic capacitance model for PTs. This model relates the distributed capacitance of individual layers to the six-capacitor model of the transformer and provides a deep insight into how changing the winding arrangement can manipulate the value of each lumped capacitor. Two special cases of PTs were considered, and analytical equations were derived for each case. In addition to the proposed analytical model, methodologies for extracting the six-capacitor model using FEA and experimental measurements were proposed. The proposed capacitance model has been verified using FEA and experimental characterization. This model provides the mathematical basis of the proposed ideas and is used in chapter 3 to analytically validate the concept of paired layers.

6.1.2 Concept of Paired Layers

CM noise in the transformer originates from an undesired electrostatic coupling between primary and secondary windings and also between windings and the core. In PTs, whenever a layer of the primary winding overlaps with a layer of the secondary winding, due to the proximity and large overlapping area of planar layers, a large parasitic capacitance is formed between overlapping layers. A parasitic capacitance also is formed between the core and layers of windings that are exposed to the core. When the voltage of overlapping layers changes rapidly due to high-frequency switching, parasitic capacitance is exposed to a large \( \frac{dv}{dt} \). This leads to the generation of pulsating currents (known as CM noise) that circulate in the circuit through the earth and create EMI problems. To minimize the CM noise of PTs, the concept of “paired layers” has been proposed in chapter 3. According to this concept, if overlapping layers have a similar layout and equal \( \frac{dv}{dt} \) at their ports, such overlapping does not generate CM noise. This means that if the structure of the PT is designed in a way that only paired layers overlap, the PT does not generate CM noise. Finding paired turns depends on the voltage distribution on the transformer’s windings, which is topology-dependent. From the transformer’s voltage point of view, topologies were divided into three groups and a methodology for finding paired turns in each group has been presented. Examples also were provided for each group to make the methodology easy to understand. The concept of paired layers also has been verified using analysis. It was mathematically proven that any winding structure based on the concept of paired layers has an equivalent capacitor network that results in zero CM noise.
6.1.3 Paired Layers Interleaving

Inter-winding capacitance depends on the number of overlapping between primary and secondary layers, and more interleaved structures exhibit larger inter-winding capacitance. This creates a trade-off in the transformer design, as the requirement of low AC resistance and low leakage inductance is in contradiction with the requirement of low inter-winding capacitance. Interleaved structures that minimize AC resistance and leakage inductance have many overlapping between primary and secondary layers, which results in large inter-winding capacitance. On the other hand, separating primary and secondary windings (non-interleaved structure) achieves low inter-winding capacitance at the expense of large AC resistance and leakage inductance. In most papers about optimizing PT, the main purpose is to reduce leakage inductances, and they do this by proposing highly interleaved structures that minimize leakage fluxes. However, since these methods do not consider capacitive effects, they result in PTs with large inter-winding capacitance and large CM noise generation. No design method had been reported in the literature that resolves this trade-off to achieve both low AC resistance and very low CM noise generation. This has been considered in chapter 4 and interleaving methods have been combined with the proposed “paired layers” concept to achieve PTs that not only have minimum AC resistance and leakage inductance but also have almost zero generation of CM noise. In other words, “paired layers interleaving” finally eliminates the trade-off between low AC resistance and low CM noise and gives the designer a tool to achieve both. Different methods of implementing this method using PCBs and copper foils were proposed and the method has been developed for three groups of topologies. Examples for different turns ratios and topologies have been presented to show the generality of the method and also to make it easy to understand.

6.1.4 Low Parasitic Planar Transformers for LLC Resonant Converters

The high intra-winding capacitance of regular multi-turn PCB winding layouts causes a number of problems in DC-DC converters. If used for planar inductors, large intra-winding capacitance reduces the self-resonant frequency of the inductor, limiting its operating frequency range. If used as the planar transformer, the high intra-winding capacitance gives rise to a high charging current at the transformer input, resulting in lower efficiency and increased peak voltage stress across secondary rectifying devices. In addition to those problems, intra-winding capacitance brings unwanted regulation issues for LLC resonant converters with wide output regulation. In order to overcome these problems, a systematic analysis was performed, and six improved PT winding layouts were introduced and benchmarked with a traditional design. The proposed winding layouts were compared regarding parasitic capacitances and resistance with the aid of analytical
equations. As a result of the investigation, an optimized structure with minimum AC resistance and inter-winding capacitance was found and verified by FEA and experimental results. The proposed winding layouts and structure were used to manufacture PTs with very low parasitic capacitance. It was shown the proposed winding layouts can reduce self-capacitance up to 21.2 times, without compromising winding resistance. The experimental results of employing the proposed transformers in a 1.2 kW LLC resonant converter showed that the use of proposed winding layouts mitigated the voltage regulation problem and enabled the converter to regulate the output voltage even under no-load condition. Besides application in LLC resonant converter, the proposed winding layouts can be used to design inductors with a wide range of operating frequencies. Since they exhibit much smaller self-capacitance, such inductors have a large self-resonant frequency, which is very desirable in high-frequency applications.

6.2 Future Work

This work opens up many full areas of research that can build upon its findings. Some of the main areas in which multiple Masters and Ph.D. students could be supervised include:

- Paired layers interleaving for converters with full-bridge inverter: The paired layers concept requires a quiet point on the primary winding. For converters with the full-bridge inverter, it was expected that a quiet point would exist in the middle of the primary winding. If that was the case, paired layers interleaving in its current form could be applied to this type of converters. However, in the tests done by the author, it was observed that the voltage at the middle point of the primary was affected by the switching and voltage spike were present at switching moments. As a result, paired layers interleaving is not applicable to this type of converters. Investigating the root cause of this, finding mitigation strategies to achieve a quiet point on primary and consequently applying paired layers concept on this type of converters remains to be studied.

- PT capacitance tuning to cancel switch’s CM noise: Besides the transformer, MOSFET’s drain to heatsink parasitic capacitance is another major source of CM noise in the circuit. Paired layers interleaving minimizes PT’s CM noise. However, it does not do anything about the CM noise of the switch. The proposed parasitic capacitance model shows how winding arrangement affects the equivalent parasitic capacitance network of the transformer. Instead of using paired layers interleaving to achieve zero CM noise, the parasitic capacitance model can be used to design PT in a way that its CM noise cancels out CM noise of the switch, making net CM noise of the converter equal to zero. This is a
major opportunity to fully eliminate the total CM noise of the converter which remains as the future work.

- Application of paired layers interleaving in matrix transformers: The matrix transformer is defined as an array of elements inter-wired so that the whole functions as a single transformer. The benefits of the matrix transformer are that it can split current between secondary windings connected in parallel, reduce leakage inductance, reduce winding AC resistance, and improve thermal performance by distributing the power loss throughout the elements. All those features make the matrix transformer very attractive for high current and high-frequency applications. Developing paired layers interleaving for matrix transformers gives them the benefit of no CM noise generation which makes this type of transformers even more desirable. This remains a topic of future research.
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