Advanced Monitoring and Control of Distributed DC Systems

An Embedded Impedance Detection Approach

by

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The following individuals certify that they have read, and recommend to the Faculty of Graduate and Postdoctoral Studies for acceptance, the thesis entitled:

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An Embedded Impedance Detection Approach

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Abstract

Direct Current (DC) systems, made possible by power electronics technology, are becoming more prevalent due to their advantages when integrating renewable energy sources, energy storage, and DC loads. Microgrids and local area energy systems are instrumental to DC systems, and much progress has been made around them. However, DC microgrids face numerous challenges due to their decentralized nature, such as resource optimization, control, and protection. This thesis focuses on developing a core technology, an embedded impedance detection (EZD) method for DC systems, and its application to five critical challenges in DC systems. The proposed method uses a reference signal of minimal amplitude and high frequency, injected in the control loop of the power electronic converter, and a digital Lock-In Amplifier to extract the incremental behavior of the voltage and current around the DC operating point. These are used to calculate the incremental impedance, which is representative of the reactive part of the system as well as the nonlinear characteristics of the system. The proposed EZD method is applied to address five critical problems in today’s DC systems: 1) adaptive control in the presence of active loads - to expand stability and improve transient response; 2) islanding detection - to detect the connection and disconnection of the utility grid and change controllers for autonomous operation; 3) fault location - to detect the distance to a fault and simplify the system restoration; 4) high-impedance fault detection - to accurately distinguish a fault condition from a load increase; and 5) maximum power point tracking of photovoltaic panels - to ensure efficient energy harvesting. For all these applications, the proposed EZD-based solution offers critical benefits and advantages,
such as high sensitivity and accuracy at a low system disturbance and fast detection. The work presents a detailed analysis of the proposed EZD technique as well as considerations for its implementation in commercial microcontrollers, followed by simulations to illustrate its capabilities. The thesis also presents a detailed analysis of each DC system application and its particular considerations. The outlined benefits are supported by simulations and validated through experimental results using a real power electronics platform.
Lay Summary

The accelerated adoption of renewable energy sources (such as solar and wind) and equipment that uses Direct Current (DC) natively (such as electric vehicles, information technology, and consumer electronics) presents challenges compared to traditional power systems based on Alternating Current (AC). Smart power electronics converters and local area electric power systems based on DC can enable the efficient integration of these renewable energy sources, but they are not without problems. This work proposes solutions to some of the main challenges faced by DC systems integrating renewable energy sources. A core technique, embedded impedance detection, which allows extraction of information from the system, is presented. This tool is used to optimize the operation of renewable energy sources, to dynamically adjust the control of the system to changing demands, and to allow the system to detect problems and operate on its own. This work contributes to the development of DC technologies which are fundamental to a more renewable power system.
Preface

This work is based on research performed at the Electrical and Computer Engineering department of The University of British Columbia by Francisco Paz, under the supervision of Dr. Martin Ordonez.

Chapter 2 contains modified versions of all the publications below.

Portions of Chapter 3 have been published at the IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG) and IEEE Transactions on Industrial Electronics [1, 2]:


Portions of Chapter 4 have been published at the IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG) [3] and an extended version is in preparation to be submitted for review to a journal:

Portions of Chapter 5 have been published at the *IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)* [4] and an extended version is in preparation to be submitted for review to a journal:


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Portions of Chapter 7 have been published at the *IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)* and *IEEE Transactions on Industrial Electronics* [6, 7]:


As the first author of these publications, the author of this thesis developed the theoretical contribution, the simulation models, and performed the experimental work. The author received advice and technical support from Dr. Ordonez and members of his research team.
# Table of Contents

Abstract ................................................................. iii

Lay Summary ............................................................. v

Preface ................................................................. vi

Table of Contents ....................................................... viii

List of Tables .......................................................... xii

List of Figures .......................................................... xiii

List of Acronyms ......................................................... xvii

List of Symbols and Notation ........................................ xxii

Acknowledgments ........................................................ xxiv

Dedication ............................................................... xxvi

1 Introduction ........................................................... 1

1.1 Motivation .......................................................... 1

1.2 Literature Review .................................................. 5

1.2.1 Impedance Detection .......................................... 6

1.2.2 Control of Power Converters in DC Systems with Active Loads . 8
1.2.3 Islanding Detection and Autonomous Operation of DC Microgrids  10
1.2.4 Fault Location in DC Systems ................................. 12
1.2.5 High-Impedance Fault Detection in DC Systems ............ 14
1.2.6 Maximum Power Point Tracking for Photovoltaic Panels .... 15

1.3 Contributions of the Work ..................................... 17
1.4 Dissertation Outline ........................................... 20

2 Incremental Impedance Measurement in Power Electronics Converters 22
2.1 Reference Generation and Injection .............................. 25
2.2 Signal Extraction ............................................... 29
   2.2.1 Moving Average Filter .................................. 31
   2.2.2 Digital Lock-In Amplifier ............................... 35
2.3 Impedance Calculation ......................................... 45
2.4 Embedded Impedance Detection Simulations ..................... 48
2.5 Summary ....................................................... 49

3 Transient Performance and Stability Improvement in DC Systems .... 51
3.1 System Model .................................................. 53
   3.1.1 Load Model .............................................. 54
   3.1.2 Dynamic Model of the System ......................... 58
3.2 Proposed Incremental Load Detection Scheme .................... 61
   3.2.1 Equivalent Incremental Load Detection .................. 62
   3.2.2 Control Adjustment Technique .......................... 64
3.3 Simulation Results ............................................ 66
3.4 Experimental Results .......................................... 70
3.5 Comparison Against Other Equivalent Load Detection Techniques ... 74
3.6 Summary ....................................................... 77
4 Islanding Detection and Autonomous Operation for DC Systems

4.1 System Model

4.1.1 DC System Model

4.1.2 Composite Load Model

4.1.3 Bumpless Controller Mode Change

4.1.4 Traditional Islanding Detection Method

4.2 Proposed Islanding Detection Method

4.3 Simulation Results

4.4 Experimental Results

4.5 Comparison Against Other Islanding Detection Techniques

4.6 Summary

5 Low-Impedance Fault Location

5.1 System Model

5.2 Proposed LIF Location Method

5.2.1 LIF Before Load

5.2.2 Load Before LIF

5.3 Simulation Results

5.4 Experimental Results

5.5 Summary

6 High-Impedance Fault Detection

6.1 System Model

6.2 Proposed HIF Detection Method

6.3 Simulation Results

6.4 Experimental Results

6.5 Summary
7 Maximum Power Point Tracking for PV Systems

7.1 System Model

7.1.1 Photovoltaic Panel Background

7.1.2 Standard InCond MPPT Algorithm

7.2 Proposed LIA-Based MPPT

7.2.1 DC Conductance Measurement

7.2.2 Incremental Conductance Measurement

7.2.3 MPP Regulator

7.2.4 Stability of the Proposed MPPT

7.3 Simulation Results

7.4 Experimental Results

7.5 Comparison Against Other MPPT Methods

7.6 Summary

8 Conclusion

8.1 Conclusions and Contributions

8.1.1 Improve Transient and Stability

8.1.2 Islanding Detection

8.1.3 Low-Impedance Fault Location

8.1.4 High-Impedance Fault Detection

8.1.5 Photovoltaic Maximum Power Point Tracking

8.1.6 Specific Academic Contributions

8.2 Future Work

Bibliography
## List of Tables

2.1 Sample LIA Parameters ................................................................. 43

3.1 Normalized Simulation Parameters for Equivalent Incremental Load Detection 67

3.2 Equivalent Load Detection Simulation ........................................... 67

3.3 Experimental Set-Up Parameters ..................................................... 73

3.4 Experimental Measurements .......................................................... 74

3.5 Comparison of the Proposed Technique with Existing Methods ............ 76

4.1 Normalized Simulation Parameters for Islanding Detection .................. 94

4.2 Simulation Load Cases Considering $R_{1,n} = R_{2,n} = 0.01$ ................. 94

4.3 Experimental Set-Up Parameters ..................................................... 100

4.4 Comparison of the Proposed Technique with Existing Methods ............. 102

5.1 Simulation Circuit Parameters .......................................................... 118

5.2 Simulation Results ........................................................................... 121

5.3 Experimental Set-Up Configuration .................................................... 124

5.4 Experimental Results ...................................................................... 124

6.1 Experimental Set-up Parameters ......................................................... 139

7.1 Simulation Profile Definition ............................................................... 161

7.2 MPPT Experimental Set-up Parameters ............................................. 167

7.3 MPPT Comparison Results ................................................................. 172
List of Figures

1.1 Diagram of a DC Microgrid with the proposed EZD tool built-In . . . . . . . 3
2.1 Incremental Behavior of DC Loads and Sources Around the Operating Point 23
2.2 Block Diagram of the DSP Implementation . . . . . . . . . . . . . . . . . . 24
2.3 Nested Loop Power Electronics Converter Controller with Reference Injection 26
2.4 Reference Generation from a Circular Buffer . . . . . . . . . . . . . . . . . . 29
2.5 Lock-In Amplifier Signal-Processing Chain . . . . . . . . . . . . . . . . . . 30
2.6 Moving Average Filter Block Diagram . . . . . . . . . . . . . . . . . . . . 32
2.7 Moving Average Filter Frequency and Step Response . . . . . . . . . . . . . 34
2.8 Digital Lock-In Amplifier Block Diagram and Operation . . . . . . . . . . . 36
2.9 Generation of the Sine, Cosine, and Reference . . . . . . . . . . . . . . . . . 40
2.10 Example Circuit and Bode Plot for LIA . . . . . . . . . . . . . . . . . . . . 42
2.11 Example Simulation Output for the LIA . . . . . . . . . . . . . . . . . . . . 44
2.12 Expanded Diagram of the Impedance Calculation . . . . . . . . . . . . . . . 45
2.13 Impedance Detection Simulation Circuit . . . . . . . . . . . . . . . . . . . . 49
2.14 Embedded Impedance Detection Simulation Outputs . . . . . . . . . . . . . 50
3.1 Block Diagram and Key Benefits of the Impedance Based Controller . . . . . 52
3.2 Power Electronics Converter and Load Schematic . . . . . . . . . . . . . . . . 54
3.3 VI Curves of a Resistive and Constant Power Load . . . . . . . . . . . . . . . 56
3.4 VI Curves of a Combined Load . . . . . . . . . . . . . . . . . . . . . . . . . 58
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.5 Power Electronics Converter and Load Control Model</td>
<td>59</td>
</tr>
<tr>
<td>3.6 VI and Time Domain Curves of a Combined Load with Net-Resistive Nature</td>
<td>63</td>
</tr>
<tr>
<td>3.7 VI and Time Domain Curves of a Combined Load with Net-CPL Nature</td>
<td>64</td>
</tr>
<tr>
<td>3.8 VI and Time Domain Curves of a Combined Load with Net-Zero</td>
<td>65</td>
</tr>
<tr>
<td>3.9 Simulations of the Proposed Incremental Load Detection</td>
<td>69</td>
</tr>
<tr>
<td>3.10 Load Profile for the Simulations</td>
<td>69</td>
</tr>
<tr>
<td>3.11 Simulations of the Adaptive Technique</td>
<td>70</td>
</tr>
<tr>
<td>3.12 Simulations of the Standard Controller for 25% CPL</td>
<td>71</td>
</tr>
<tr>
<td>3.13 Simulations of the Standard Controller for 100% CPL</td>
<td>71</td>
</tr>
<tr>
<td>3.14 Picture of the Experimental Set-Up for the Equivalent Load Test</td>
<td>72</td>
</tr>
<tr>
<td>3.15 Experimental Capture of the Impedance Detection Injected Reference</td>
<td>73</td>
</tr>
<tr>
<td>3.16 Experimental Captures of the Equivalent Load Detection</td>
<td>75</td>
</tr>
<tr>
<td>4.1 Block Diagram of the DC Microgrid and Outline of the Proposed ID Algorithm</td>
<td>80</td>
</tr>
<tr>
<td>4.2 Incremental Model of the Power Electronics Converter in GTM and IM</td>
<td>82</td>
</tr>
<tr>
<td>4.3 V-I Curves of Different Loads</td>
<td>84</td>
</tr>
<tr>
<td>4.4 Incremental Resistance for CPL+CRL and CCL+CRL</td>
<td>87</td>
</tr>
<tr>
<td>4.5 Proposed Islanded Mode Controller</td>
<td>88</td>
</tr>
<tr>
<td>4.6 Block Diagram and Time Diagram of a Standard Islanding Detection Method</td>
<td>90</td>
</tr>
<tr>
<td>4.7 Block and Time Diagram of the Proposed Islanding Detection Method</td>
<td>91</td>
</tr>
<tr>
<td>4.8 Simulations of the Proposed Islanding Detection in Open Loop</td>
<td>96</td>
</tr>
<tr>
<td>4.9 Detail of the Simulations of the Proposed Islanding Detection in Open Loop</td>
<td>97</td>
</tr>
<tr>
<td>4.10 Impedance Plane Simulation Results for Different Loads</td>
<td>98</td>
</tr>
<tr>
<td>4.11 Simulations of the Closed Loop System with Droop Control</td>
<td>99</td>
</tr>
<tr>
<td>4.12 Diagram Experimental Set-Up</td>
<td>100</td>
</tr>
<tr>
<td>4.13 Experimental Captures of Islanding Detection in Open Loop</td>
<td>101</td>
</tr>
</tbody>
</table>
7.1 Block Diagram and General Comparison of the Proposed MPPT vs. the Classical Approach .................................................. 145
7.2 Structure of a PV Cell and Behavioral Model ........................................ 147
7.3 Voltage-Current-Power Curves of a PV panel ................................... 149
7.4 MPP Condition ........................................................................... 150
7.5 Flowchart and Time Diagram of the InCond MPPT ............................. 151
7.6 Block and Time Diagram of the LIA-Based InCond MPPT ................. 153
7.7 Stability block diagram ............................................................... 158
7.8 Frequency Response .................................................................... 160
7.9 Simulations of the Traditional InCond .............................................. 162
7.10 Simulations of the LIA-Based MPPT ............................................. 163
7.11 Details of the Simulated Transitions .............................................. 164
7.12 V-I View of the Transients ............................................................ 165
7.13 Start-Up Profile as a Function of $K_I$ ............................................. 165
7.14 MPPT Tracking Efficiency ........................................................... 166
7.15 Picture of the Experimental Set-Up for the MPPT Test .................... 168
7.16 Experimental Capture of the LIA-Based InCond ............................... 170
7.17 Experimental Capture of the Standard InCond ................................. 171
# List of Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>BIBO</td>
<td>Bounded Input Bounded Output</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>CB</td>
<td>Current Breaker</td>
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<tr>
<td>CL</td>
<td>Current Loop</td>
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<tr>
<td>CCL</td>
<td>Constant Current Load</td>
</tr>
<tr>
<td>CPL</td>
<td>Constant Power Load</td>
</tr>
<tr>
<td>CRL</td>
<td>Constant Resistance Load</td>
</tr>
<tr>
<td>CV</td>
<td>Constant Voltage (MPPT method)</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>DTFT</td>
<td>Discrete Time Fourier Transform</td>
</tr>
<tr>
<td>DZ</td>
<td>Detection Zone</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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</tr>
<tr>
<td>EMS</td>
<td>Energy Management System</td>
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<tr>
<td>EZD</td>
<td>Embedded Impedance Detection</td>
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<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite Impulse Response</td>
</tr>
<tr>
<td>FOCV</td>
<td>Fractional Open Circuit Voltage (MPPT method)</td>
</tr>
<tr>
<td>FSCI</td>
<td>Fractional Short Circuit Current (MPPT method)</td>
</tr>
<tr>
<td>GTM</td>
<td>Grid-Tie Mode</td>
</tr>
<tr>
<td>HIF</td>
<td>High Impedance Fault</td>
</tr>
<tr>
<td>HVDC</td>
<td>High Voltage DC</td>
</tr>
<tr>
<td>ID</td>
<td>Islanding Detection</td>
</tr>
<tr>
<td>IDM</td>
<td>Islanding Detection Method</td>
</tr>
<tr>
<td>IM</td>
<td>Islanded Mode</td>
</tr>
<tr>
<td>InCond</td>
<td>Incremental Conductance (MPPT method)</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>KF</td>
<td>Kalman Filter</td>
</tr>
<tr>
<td>LIA</td>
<td>Lock-In Amplifier</td>
</tr>
<tr>
<td>LIF</td>
<td>Low Impedance Fault</td>
</tr>
<tr>
<td>LPF</td>
<td>Low Pass Filter</td>
</tr>
<tr>
<td>MAF</td>
<td>Moving Average Filter</td>
</tr>
</tbody>
</table>
MAP  Magnitude and Phase
MPP  Maximum Power Point
MPPT Maximum Power Point Tracking
NDZ  Non-Detection Zone
OCP  Over-Current Protection
OM   Operating Mode
PEC  Power Electronics Converter
PEDG International Symposium on Power Electronics for Distributed Generation Systems
PI   Proportional Integral (Controller)
PID  Proportional Integral Derivative (Controller)
P&O Perturb and Observe (MPPT method)
PPU  Power Probe Unit
PSO  Particle Swarm Optimization (MPPT method)
PV   Photovoltaic
PWM Pulse Width Modulation
RLS  Recursive Least Squares
ROCOF Rate of Change of Frequency
RT   Rate Transition
TAB  Triple Active Bridge
**THD**  Total Harmonic Distortion

**TZ**  Trip-Zone

**UBC**  The University of British Columbia

**UV/OV**  Under Voltage/Over Voltage

**VL**  Voltage Loop
List of Symbols and Notation

Below there is a list of the most commonly used symbols in the document. Some symbols take special meanings as auxiliary variables in a limited scope in the document (such as $x$ being a generic input signal when explaining a digital filter, instead of the imaginary part of the incremental impedance); when this is the case, it is indicated in the text.

- $\theta_n$: phase of the $n$-th harmonic
- $A_n$: Amplitude of the $n$-th harmonic
- $A_r$: Amplitude of the reference signal
- $b$: Incremental susceptance $b = \text{Im}(y)$
- $e_x$: Error of the variable $x$ (such as tracking error, measurement error, estimation error)
- $f_r$: Frequency of the reference signal
- $f_s$: Sampling frequency
- $f_{sw}$: Switching frequency
- $g$: Incremental conductance $g = \text{Re}(y)$
- $i_{in}$: Input current
- $i_o$: Output current
\( M \) Number of samples in the buffer of the MAF

\( N \) Number of samples in a period of the reference signal

\( N_p \) Number of periods of the reference signal averaged by the LIA

\( r \) Incremental resistance \( r = \text{Re}(z) \)

\( T_{MPPT} \) Sampling Period of the MPPT algorithm

\( T_r \) period of the reference signal \((1/f_r)\)

\( T_s \) Sampling Period \((1/f_s)\)

\( T_{sw} \) Switching Period \((1/f_{sw})\)

\( i_{pv} \) Current output of the photovoltaic panel

\( v_{in} \) Input voltage

\( v_o \) Output voltage

\( v_{pv} \) Voltage output of the photovoltaic panel

\( r \) Incremental reactance \( x = \text{Im}(z) \)

\( y \) Incremental admittance: \( y = 1/z = g + j\ b \)

\( z \) Incremental impedance: \( z = r + j\ x \)
Notation

- Some variables have a subscript ending in ..., n (such as $v_{o,n}$); this indicates the "normalized value of $v_o$".

- Some variables have a hat accent (such as $\hat{v}_o$); this indicates the "estimated value of $v_o$", usually the output of a computation through an algorithm.

- Some variables have a tilde accent (such as $\tilde{v}_o$); this indicates the "the incremental value around the DC operating point".

- Some variables have an asterisk super-index (such as $v^*_{o}$); this indicates a set-point to a control loop.

- Capitalized versions of variables ($V_o$ to $v_o$) signify the average value of $v_o$, in general the quiescent point of the variable.

- Variables followed by (t) (such as $v_o(t)$) are assumed to analog (continuous in time).

- Variables followed by [k] (such as $v_o[k]$) are assumed to be discrete (either as a sampled version of an analog signal) or generated discretely. k can be replaced as the index variable by other symbol (such as $i$, $K$, $n$), when this is the case, it is indicated in the text.
Acknowledgments

Firstly, I would like to thank my supervisor, Dr. Martin Ordonez, for the opportunity to join his team. It has been an experience beyond my dreams. His technical support, patience, drive, and leadership are an inspiration to me.

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To Abu Ñata, our grandmother
Chapter 1

Introduction

1.1 Motivation

Intending to reduce greenhouse gas emissions due to human activities, small local power and energy systems based on renewable energy are becoming more attractive. Traditional energy production (coal and gas plants, big hydroelectric dams, and nuclear power plants) are controllable. Therefore, they can rely on the centralized generation and the Alternating Current (AC) transmission and distribution grid to efficiently integrate them. On the other hand, energy harvesting from renewable energy resources (such as wind, ocean, tidal, and solar) is at the whim of the sun, wind, or ocean and produces variable voltages and currents.

Portions of this chapter have been published in

that are not directly compatible with the AC system. Power Electronics Converters (PECs) are developed to interface these variable inputs to grid-compatible AC levels; however, this can be achieved more efficiently by using Direct Current (DC) directly.

DC systems often use different architectures than AC systems. Many are connected to the utility grid but are also able to operate on their own (islanded mode), receiving the name microgrids. This name is given to a wide range of configurations, from megawatt systems integrating large areas and resources, to small scale grids that feed a single house, a single ship, or a telecommunications hub rated at a couple of kilowatts. Figure 1.1 presents one microgrid and the different elements in it.

Power electronics is one of the key enabling technologies of the microgrid, allowing for control of power flow and quality. The PECs in Fig. 1.1 convert variable voltage, current, and frequency, coming from renewable energy sources, into a regulated voltage and current that meet the requirements of the loads, at extreme levels of efficiency and density. Digital control allows the benefits of power electronics to be extended by adding novel features, such as automatic resource optimization, which are fundamental for an efficient power system.

Moving from a centralized generation architecture (such as the traditional power system) to a distributed generation architecture introduces the challenge of distributing the control and operations. While the traditional grid has only a few power plants to control, the distributed architecture can lead to multiple generators without a direct way to be controlled by the utility. Moreover, centralized control would depend on a communications lifeline, which then becomes a critical point of failure in the system.

Examples of areas of intense research in DC systems technology are:

- resource optimization,
- islanding detection,
- fault detection, analysis, isolation, and system restoration,
DC microgrid

Figure 1.1: DC microgrids offer advantages when integrating renewable energy sources (such as PV and wind), energy storage (such as batteries), and loads (such as variable speed drives and IT equipment), but they have some critical problems; this thesis focuses on the development of a core technology, an embedded impedance detection (EZD) algorithm built into each power electronics converter, which allows each converter to inject a reference signal of minimal amplitude and high frequency, and extract the incremental behavior of the system around the current operating point using a Lock-In Amplifier (LIA); this information is used to address five key problems depending on which converter is considered: (A) adaptive control (AC) for extended stability and improved dynamic performance, (B) islanding detection (ID) for autonomous operation, (C) low impedance fault (LIF) location to find the distance to a fault in the system, (D) high-impedance fault (HIF) detection to differentiate a fault from a load change, and (E) maximum power point tracking (MPPT) for PV panels.
• protection coordination,

• and stability.

Moreover, the magnitudes in DC systems (voltage and currents) present a constant value at a given operating point. The operation of the DC system around constant voltage masks many characteristics of the system, and finding ways to extract them without adding cost in the form of hardware or significant disturbances is challenging. This leads to slow adoption of DC distribution technology and its benefits. For example, the output voltage and current of a DC converter do not convey information about the reactive part of the load; the phase difference between voltage and current in an AC system can be used to detect the reactive part of the impedance.

This work introduces a solution to some of the main challenges faced by DC systems through an embedded impedance detection (EZD) algorithm built into each power converter in the microgrid. The EZD uses a reference signal of small amplitude and known frequency to measure the incremental impedance (i.e., the derivative of voltage with respect to current around one operating point) from the PEC. The incremental impedance has the advantage of being sensitive to the characteristics of the system (constant resistance, constant power, constant voltage, constant current), as well as reflecting the reactive part of the set-up (line inductance, capacitive input). The applications of the EZD to different elements of the microgrid tackled in this thesis are presented in Fig. 1.1, they are

(A) detect the type of load and adjust the controller to improve stability and transient behavior in real time,

(B) islanding detection to switch the controller between modes and achieve smooth continuous operation,
(C) measure the distance to a low impedance fault between conductors, to aid in finding the fault in the system,

(D) detect high impedance faults and differentiate them from load increases in point-to-point architectures, and

(E) control the PECs to perform MPPT from a photovoltaic (PV) panel, even under uncertain parameters and changing conditions.

1.2 Literature Review

Research in DC systems, especially those interfacing with renewable energy sources, have seen a surge of interest in the power electronics community in the past years [8–11]. Many critical pieces of technology were adapted from AC systems, but many of these solutions are not suitable for DC systems [12]. Areas of intense work include optimization of resource integration, control systems, increased autonomy, and fault detection problems [10, 13]. In all these problems, work is put towards the integration of the solution into the PEC whenever possible, but the possibilities and needs are dependent on the type of DC system.

Essential applications of DC systems exist in the form of DC microgrids, or, more generally, local area power and energy systems [14]. On the bigger scale, applications can take the form of a regional microgrid integrating photovoltaic plants, wind turbines, battery storage, and loads with or without a connection to the utility AC grid [9]. Stand-alone DC systems exist in the form of the power system of a ship [15]. DC systems are also critical in providing high reliability power to telecommunication sites [16–19]. The electrification of transportation will likely rely on local storage, integrated into a DC system, to provide the peak power to the EV charging station and avoid over-sizing the grid connection [19]. On the smaller end, DC buildings and homes have been proposed to reduce greenhouse gas emissions [20–22].
This thesis contributes to the implementation of distributed DC systems by proposing an EZD method, built into the PEC, and outlining five critical applications of the proposed technology. The following cited work has been performed in the field of power electronics for distributed generation concerning impedance detection and the target applications for the insights developed in this work.

### 1.2.1 Impedance Detection

The incremental impedance of a system is defined as the derivative of voltage with respect to current at one particular operating point (also called the small-signal impedance) \[23\]; it can yield very crucial information about the behavior of the system. The incremental impedance of the load, for example, defines the input impedance seen by the source converter at a given operating point and affects its stability \[23–26\]. This parameter is challenging to measure in real-time, using only the hardware already employed in a PEC, but can provide useful information if continuously monitored. Detecting the incremental impedance is especially challenging for DC systems, which operate around a stationary operating point, as opposed to AC systems.

Incremental impedance detection is, at its core, a system identification problem; as such, many techniques have been introduced that rely on the fundamentals of this field \[27\]. The recursive least square method (RLSM) and Kalman filter were used in \[28\] to determine the incremental impedance of DC systems. Methods based on discrete sequences \[29\] and the discrete Fourier transform \[30\] were also presented. However, most methods either require large amounts of computational power to determine the equivalent impedance or sacrifice precision. A precise method that is computationally efficient, such that can be implemented in the microcontrollers used to control PECs, would add valuable insight in real time to the system.
The Lock-In Amplifier (LIA), sometimes referred to as the phase-sensitive method, is a versatile algorithm or instrument that can accurately detect a signal of a selected frequency in an environment with high noise [31]. This is achieved by using a combination of modulation and demodulation techniques, along with low pass filtering, to extract the magnitude and phase of the signal of interest. Most commercial applications of the LIA are laboratory equipment [32]. They rely on dedicated hardware to provide adjustable frequency and amplitude control, but do so at an extremely high cost ($10,000 USD or more), and are not suitable to be implemented in every PEC in the system.

The LIA has been used in the past to characterize the impedance of transformers [33] and fuel cells [34, 35]. It was used to determine the junction impedance of a diode [36], and the hysteresis loop of magnetic materials [37]. Detection of optical signals was implemented using a LIA and a 20-bit Analog to Digital Converter (ADC), achieving 103 dB dynamic range [38]. An extended analysis of the frequency response was presented in [39] for the analog case, and a broadband version of the algorithm was presented in [40]. A simplified digital version was presented in [41], and an oversampled one was presented in [42]. The convergence of the method was explored in [43] where an entropy-based method was proposed for optical tests. These applications can extract some specific characteristics of the system using a LIA but use laboratory equipment and desktop computers, as opposed to real time processing in microcontrollers for embedded applications. Little work has been presented in real-time implementation of LIAs in field-equipment.

Although there are algorithms that extract the incremental impedance using powerful hardware (laboratory equipment and desktop/laptop processors), there is room to use advanced algorithms such as the LIA to detect the impedance in real time using embedded microcontrollers and sensors present in PECs.
1.2.2 Control of Power Converters in DC Systems with Active Loads

Control of PECs in DC microgrids faces some particular challenges such as maintaining reliable dynamic performance under changing load conditions, ensuring stability of the system [44, 45]. This can be especially challenging in the presence of active loads, which are PECs themselves, regulating their output voltage. This causes a Constant Power Load (CPL) behavior, leading to stability problems. CPLs present a negative incremental resistance: if the input voltage drops, in order to keep the power delivered to the load constant, the input current has to increase [46]. The negative incremental resistance plays a crucial role in determining the stability of the system [47–50], and the stability analysis has seen many contributions in the past years [14, 51]. Although in real-world applications no CPL has infinite bandwidth, this scenario is relevant in order to account for the worst-case scenario.

Developing modern control strategies that allow the DC microgrid to deal with active loads, especially under uncertain load conditions, requires continuous measurement of the system. Passive solutions rely on changing the passive components (resistors, capacitors, and inductors) strategically to improve the stability of the grid. Rather than proposing novel control strategies, these methods add components to the system. Some solutions propose the use of RC and RL filters to mitigate the CPL problems [52]. Alternatively, increasing the bus capacitance can increase the stability margin of the system at the expense of more expensive capacitors [46]. These methods, although very simple, have the obvious drawback of adding cost in the form of additional components.

Modifications to the control strategy can be done to the source-end PEC or the load-end PEC. Examples of modifications to the load-end controller focus on changing the bandwidth of the controller such that the load does not present such an aggressive CPL behavior. This modification can take the form of an emulated impedance in the DC bus (where the control
loop is designed to behave as a particular impedance to provide the desired benefits), which can be implemented for a single PEC [44, 53, 54] or many [55]. Limiting the current rate of change in the load-end PEC also has the effect of limiting the response and therefore, the CPL behavior [56]. More complex stabilization strategies can be added to the controller to make the system stable [57].

Alternatively, controllers for the source-end PEC have been presented in the form of traditional and nonlinear solutions. Linear approaches include [47, 50, 58, 59], where the method is called active damping for its emulation of a damping circuit. Nonlinear approaches include many techniques [60–64] that allow for robust control by doing away with the small-signal analysis. Geometric control allows improvement of the regulation speed by not requiring small-signal tuning [65]. It has been shown that geometric controllers can contribute to the stability of the microgrid, even if only a small fraction of the PECs are controlled using geometric control [66].

When tuning the controller of the system, considerations are made of the different load states of the PEC, and performance is not uniform for all conditions. Adaptive controllers, based on gain scheduling schemes, have been utilized for many years and provide an advanced solution that still relies on simple controller architectures (such as the Proportional Integral Derivative, PID) [67]. These controllers offer the advantage of linear control, its very well-known operation, with the ability to improve the performance for different changes in the system. Instead of tuning the system to a single state, gain scheduling has a set of controller gains that depends on the state of the system (e.g. the type and size of the load). The use of the EZD method leaves room to perform a smart tuning of the controller as a function of the incremental load.
1.2.3 Islanding Detection and Autonomous Operation of DC Microgrids

Microgrid voltage regulation can be structured in two main ways: either the voltage is regulated cooperatively by all the PECs in the system, or only some PECs (known as grid-forming converters) regulate the voltage while the others follow them. Islanding detection (ID), that is the process of detecting when the grid-forming PEC has been disconnected, is a fundamental feature of any PEC built to work in a DC microgrid and remains an open challenge [68]. A functioning ID method (IDM) allows the system to disconnect as soon as the islanding event happens or switch over to a controller designed for this operating mode. By using the appropriate controller for islanded and grid-tie mode, the DC system can be made to operate safely (by ensuring the bus voltage is regulated at all times) and efficiently (ensuring the distributed sources operate following the local optimization rules).

When the microgrid is connected to a grid-forming PEC, connected PECs follow local rules to optimize their performance (such as maximum power point tracking or battery charging) [69–71]. In the event that a grid forming PEC is not available, the PECs in the DC system follow alternative rules designed to maintain service to the loads. In a master-slave approach, if the grid forming PEC is not available, the duty to regulate the voltage is usually delegated to the energy storage device or a diesel generator. This allows the rest of the devices to continue to operate in MPPT mode, increasing the efficiency of the energy harvesting. Alternatively, PECs might implement a collaborative regulation of the voltage through the use of a droop controller [72–77]. For some applications, such as [75], the droop control can be integrated into the Energy Management System (EMS) to regulate the storage in supercapacitors and other fast storage.

Research in IDMs has seen many contributions in the past years, especially for AC systems [78–81]; however, the same techniques cannot be extended to DC systems. In DC
systems, the only variable magnitude that can be affected during the islanding event is the voltage; therefore, methods that rely on the frequency, such as the Rate of Change of Frequency (ROCOF) [82–85], and those based on phase variation [86] cannot be applied to DC systems.

The passive IDMs rely on measuring signals such as the voltage and current, without injecting any disturbance, and inferring the islanding state from there. The parameters of the microgrid are monitored and if a parameter goes outside some prescribed magnitude (such as the grid voltage going outside of the under/over voltage area) the IDM signals the detection of the islanding event. The passive techniques can be swift and accurate when there is a significant power mismatch in the system between what is being generated and the load [87, 88]. However, they have limitations when the mismatch between generation and load is zero or close to zero. The range of operating points where the IDM is not triggered is called its Non-Detection Zone (NDZ). Examples of passive methods include the under/over voltage (UV/OV) [89], and the autocorrelation function of model current envelope [90]. A comprehensive review of these methods was recently presented in [68].

Active islanding methods, on the other hand, rely on injecting some form of disturbance in the system and inferring, from the transient, the state of the grid. An active method that combines a perturbation with the MPPT algorithm is presented in [91]. This method introduces a perturbation that starts on the order of 10% of the load current and increases in size, generating a significant disturbance that pushes a passive OV/UV scheme to trip. The NDZ of this method can be tuned by selecting different perturbation sizes and frequencies. The positive feedback method relies on injecting a disturbance and increasing it proportionally to the size of the voltage deviation; this method has a very small NDZ, but influences the stability of the system [92, 93].
Some methods rely on a communication to be established between the distributed generators and grid forming device [94–96]. These methods offer almost zero NDZ but are costly and sensitive to damage or attacks in the communications system.

Once the islanding is observed, several actions can be taken. In many applications, it is required that the PECs disconnect from the grid once the islanding event is detected, usually within a small time frame (100-300 ms) [97]. Other applications require the system to continue providing service even during the islanding event, in order to ensure service is provided to the load [72, 73, 98]. It is essential that the controllers are designed to smoothly switch over to different controller modes, which can be achieved using advanced techniques or simple PI techniques [67]. Although many techniques can detect the islanding event, not many IDMs are able to also detect when the system has been reconnected to the grid. The proposed ID can be combined with different controllers for island and non-islanded mode to ensure the system continues to provide regulated power to the loads in a decentralized way (without communications).

1.2.4 Fault Location in DC Systems

A Low Impedance Fault (LIF) between two conductors is the unintended circulation of a high amount of current between the conductors, usually a short circuit. Besides detecting the fault, it is essential to locate where in the system the fault happens in order to isolate that part and repair faster [13].

LIFs in AC systems can be cleared relatively easily due to the natural zero-crossing events produced by the alternating voltage/current; this is not the case in DC systems [13]. The lack of zero-crossing in DC systems has led to much interest in DC protective devices and strategies, capable of breaking a non-zero current [99–102]. Topologies that are connected to the AC grid can rely on fast Circuit Breakers (CBs) on the AC side to extinguish the current and slow switches in the DC side to segment the system [103]. An alternative method to seg-
ment a grid relying on a topology that can limit current on its own is proposed in [104] using the power router, a form of the triple active bridge (TAB) [105]. These novel approaches to break the current and change the path of the current have led to the possibility of implementing architectures with multiple paths that offer higher reliability through redundancy [106, 107]. These have controllable switches that allow for a reconfiguration of the system in the event of a fault to maintain power to the loads in the unaffected part of the system. This reconfigurability increases the availability of the system [107, 108]. Radial architectures provide the least redundancy to the system: a fault in any of the lines cuts power to that part of the system. Ring architectures provide an alternative path to the current, allowing for one fault point before power needs to be cut to the load [109, 110]. Interconnected architectures provide an additional level of redundancy [111]. Adding the different paths for the current also adds challenges to identify the faulted line [103] and the location of the fault in that segment in order to repair the fault promptly.

Several methods to locate a fault in a DC system have been proposed in the past. The method proposed in [112] uses an external Power Probe Unit (PPU) to inject a signal in the system and locates the fault by means of the oscillation frequency and damping. Other examples of methods that rely on external hardware include [113] for marine vehicles and [109] for renewable energy systems. Using external hardware such as PPUs is expensive and requires the repair crew to move the external equipment around. Measuring the transient and using its parameters to estimate the distance to the fault has been proposed in [114, 115]; this has the disadvantage of requiring a very high sampling rate and accuracy to detect the location. A handshake method that can be applied to multiterminal DC systems is presented in [103], which makes use of slow DC switches to interrupt segments of the system to perform the detection, but relies on communications between the converters to be established. Once the LIF is located, the system should be reconfigured, when possible, to restore power to
the loads. Building the fault location features into the PEC facilitates a cost reduction and automate repairs in the system.

1.2.5 High-Impedance Fault Detection in DC Systems

High Impedance Faults (HIFs) can be produced for several reasons [116–119]: aging and damage in the isolation of the wires can create current leakage between the conductors; low conductivity materials (such as tree branches) can come in contact with the conductors; arcs can be established and maintained for long periods of time; or even people or animals touching the conductors can create a high impedance path for the current. These faults are dangerous, as they can accelerate the damage on the isolation leading to short circuit faults, can cause the fault path to heat leading to a fire, or can cause the person or animal to suffer electric shock or burn [120]. Due to the dangers posed by HIFs, it is crucial to detect them and activate the protections swiftly.

The Detection of a HIF is challenging, as the fault current is not likely to trip the Over Current Protection (OCP), being more likely to be confused with a load step-up [10, 116]. However, extensive analysis of the transients and spectrum has yielded methods that enable the detection of a fault.

The Detection of HIFs in AC power systems has seen many contributions over the past years. An extensive characterization of different types of HIFs and their effect on the AC grid was carried out in [121]. An algorithm that integrates time and harmonic analysis with probabilities was discussed in [117]. The method in [122] incorporates information from the current magnitude, the third and fifth harmonic, and the phase of the current harmonics with respect to the voltage to detect HIFs. A method based on the wavelet transform is used in [123] to detect a fault. A decision tree method, based on Fast Fourier Transform (FFT) training on the substation feeder current was introduced in [124]. All these methods use information about the frequency and phase, which are not readily available in DC systems.
The detection of HIF in DC systems remains one of the main challenges today [10]. The study in [125] mentioned the implementation of HIF protection for pole-to-ground faults, based on commercial devices, but does not mention pole-to-pole faults; even then, the detection of pole-to-ground HIFs is challenging [126]. Contributions have been made in High Voltage DC (HVDC) systems that rely on the harmonics injected by the AC side and rectification circuit [127]; but these methods are not suitable for systems with DC inputs or significant storage elements. The traveling wave methods are highly effective, but they require dedicated hardware and have high signal processing requirements that can make them prohibitive to some applications, in particular small systems [128]. A Fourier-based analysis is presented in [129] for a point-to-point architecture, typical in many applications; this as well relies heavily on processing power to detect the fault. The use of a DC reactor to detect the fault in HVDC is proposed in [130, 131]; this can be effective in HVDC but also requires dedicated external equipment. Building the HIF detection into each power converter allows safer operation (by allowing the system to detect the fault and disconnect the power) and simpler system implementation (by removing the need for external, dedicated hardware).

1.2.6 Maximum Power Point Tracking for Photovoltaic Panels

Peak energy harvesting for PV panels has become a fundamental requirement to achieve high overall conversion efficiency (converting as much irradiance into electricity injected in the system), given the non-linear voltage/current characteristics of the panel [132, 133]. The MPPT algorithm is entrusted with ensuring the PV panel operates at the Maximum Power Point (MPP). Many contributions have been implemented in the past years to maximize the energy harvested from PV panels [134], but some issues remain open. A wide variety of MPPT algorithms are available [135, 136] ranging from simple and inaccurate algorithms such as the Constant Voltage (CV), Fractional Open Circuit Voltage (FOCV), or Fractional Short Circuit Current (FSCI); the popular hill-climbing algorithms such as Perturb and Observe
(P&O) and Incremental Conductance (InCond) [137]; and the sophisticated algorithms based on heuristics such as Particle Swarm Optimization (PSO) [138–140] and Fuzzy Logic [141–143].

The popularity of the Hill-Climbing techniques (InCond and P&O) derives from their simplicity, needing a few sensors and tuning parameters. They work by injecting a change in the operating point of the converter (perturbation) and checking for a condition to determine a better operating point. However, several issues remain unsolved. Both the InCond and the P&O algorithm suffer from a characteristic oscillation in steady-state that results in a reduction in efficiency [144, 145]. The step-size of the algorithm and the sampling-time are mixed to produce a trade-off between accuracy and speed [146–148] that leaves the fast algorithms with large oscillations and the accurate algorithms with slow tracking speed; this has lead to optimization criteria [149–151] and adaptive versions of the algorithm [152–154]. Among the adaptive versions of the algorithm, new approaches have been presented using Dual Kalman Filters on FPGA devices [155, 156], this technique is used to identify parameters from the system and adapt the MPPT algorithm for optimization. Another common problem of the InCond and P&O is the tracking of changing environmental conditions, namely the Irradiance ($I_{rr}$) and the Temperature ($T$). The nature of the algorithm leads to confusion during changing conditions and inefficient tracking even when going in the correct direction [157, 158]. Moreover, if the environmental conditions (in particular the irradiance) are not uniform, the PV presents local maxima, which leads to confusions in the MPPT process. Solutions have been presented for some of the issues such as environmental changes [159] and local maxima problems [160–169], the advance of distributed inverters (string, micro, and module integrated) have helped mitigate this problem. Classical approaches, such as the InCond and P&O, exhibit a significant limitation in that the algorithm can make the incorrect decision under specific environmental changes. This error arises when the switching ripple and low frequency perturbation interact. Solutions have been proposed to minimize this interaction
while keeping the standard algorithms [170]. Opportunities to introduce further improvements in steady-state operation and transient dynamic tracking remain open. It has been shown in [171, 172] that the switching ripple can be used as a non-intrusive method to perform optimization. The elimination of perturbation and the use of the switching ripple have the potential to increase MPPT performance, but switching ripple is hard to detect due to its amplitude and the noise.

Different control architectures can influence the speed and accuracy of the MPPT algorithm. Multi-loop controllers use the output of the MPPT as a reference voltage/current for the controller, sacrificing speed for tighter control of the voltage [173]. Single-loop architectures achieve faster transients [174–176] but the control objective is directly aimed at the MPP, ignoring other restrictions (such as current limits). Some methods, based on sliding mode control, allow fast MPPT convergence, while keeping controllers in place [146, 177–180]. Although much progress has been made in uniformly irradiated PV panels, opportunities for smooth, fast, and simple algorithms remain open.

1.3 Contributions of the Work

The objective of this work is to investigate novel control and monitoring techniques that allow for a more efficient and more autonomous DC power system, based on distributed resources. This is achieved through the development of an impedance analysis instrument and its modification and tuning for specific applications. The main contributions of this work are:

1. An Embedded Impedance Detection (EZD) method is introduced. The proposed EZD method can detect the incremental behavior of a system around an operating point at a given frequency. It allows the measurement of the resistive and reactive parts of the impedance both in magnitude and phase, using reference signal (of lower magni-
tude than other methods) injected in the system. The proposed EZD method can be implemented in an industry-standard microcontroller (TI C2000), with no additional sensors.

2. A gain scheduling technique to improve the stability and transient behavior of DC microgrids with active loads is proposed. The EZD is used to determine the incremental behavior of the load and update the controller’s gain, which extends the stability of the system. The performance of the proposed system is compared with a controller tuned for a specific case, which fails under extended active load transients, and against a controller tuned for the worst-case active load, which exhibits undesired performance under other loading conditions. The proposed controller extends the stability to a full active load scenario and reduces overshoots from 15% to 2.5%, without sacrificing speed.

3. A new active IDM for DC microgrids based on the EZD, is presented. The method uses the EZD to detect the incremental load, which is a clear indication of the islanding/non-islanding scenario, even in the most challenging conditions. The proposed method has a minimal non-detection zone, uses a minimal reference signal and converges faster (compared with other active methods), and can detect islanding and non-islanding conditions. This allows the PEC to switch to a grid forming controller and then switch back to a grid follower controller, increasing the autonomy of the system.

4. A Low Impedance Fault (LIF) location technique for DC systems is presented. Using the EZD method, it is possible to detect how far away from the PEC the LIF is located. This measurement is affected by the fault resistance, which introduces error. The EZD allows the LIF location method to use not only the resistive part but also the reactive part of the impedance, to increase the accuracy. The proposed method allows the PEC to be used as a detection unit reducing the time needed to perform the repairs.
Moreover, it allows to restore energy to the healthy part of the system after the incident, without the use of dedicated pieces of equipment (such as PPU).

5. A High Impedance Fault (HIF) detection method based on the EZD is introduced, which exhibits the ability to distinguish a fault condition from a load increase in point of load-end PECs. The HIFs are challenging to detect, as they might not trip the over-current protection and be confused with load increases. The proposed method benefits from the negative incremental resistance of constant power loads to distinguish a HIF from a load increase. The nature of the difference is such that the HIF and load increase push the incremental resistance in different directions, making it a clear distinction between the two cases.

6. A novel Maximum Power Point Tracking (MPPT) algorithm that can follow irradiance changes, operate with no oscillations, adapt the step size to track the irradiance changes, and does so with a single control loop is presented. The control loop is based on impedance sensing using the proposed EZD method, aiming to match the DC and incremental behavior. The proposed method achieves 40 times speed improvement over the traditional incremental conductance method, as well as no oscillation and tracking of transients within 98% of the true MPP.

In the area of DC systems, this work makes significant contributions to building new capabilities and autonomy without adding additional hardware or special microcontrollers. The proposed technique allows for increased energy extraction efficiency and its distribution. It replaces external components, such as power probe units used to locate faults, by internal algorithms. It gives the DC system new capabilities, such as the possibility to self-tune and the ability to switch between grid-follower and grid-forming modes with no extra cost. It improves safety by detecting problems and preventing fires. Ultimately, the contributions of this
work push the development of autonomous DC systems forward, allowing more autonomous and dependable systems to be built.

1.4 Dissertation Outline

The rest of the work is organized as follows:

Chapter 2 introduces the core EZD method, outlining its analysis and implementation. The work builds on the LIA algorithm and explores the details, modifications, and trade-offs needed to implement it in a real-time system of constrained resources, such as the microcontroller in a PEC.

Chapter 3 presents the use of the proposed EZD method to improve the transient stability of a DC microgrid through an adaptive controller. The dynamic response of the system as a function of the load is analyzed. The controller uses a PI structure and updates it following the detected incremental load, achieving improved performance and stability.

Chapter 4 introduces an EZD based IDM and islanding operation. The behavior of the system when the grid is connected and when it is not is analyzed. It is shown that the incremental behavior of the load, measured from the source converter, is a clear ID signal. The proposed EZD-based IDM is compared with a standard Under-Voltage/Over-Voltage in the most challenging scenarios.

Chapter 5 outlines the location of Low-Impedance Faults (LIFs) between conductors in a DC system using the proposed EZD method. The location error is analyzed as a function of the control variables and the unknowns. The use of the EZD method allows for fault location and repair cost reduction.

Chapter 6 outlines the use of the EZD method to detect High-Impedance Faults (HIF) and differentiate them from load increases. The HIFs can be caused by arcs and conductors touching low conductivity materials; if they are not interrupted, they can lead to fires and
equipment damage. The behavior of the PEC under the HIF and under a load increase is analyzed for challenging scenarios.

Chapter 7 presents the implementation of a modified EZD algorithm to perform Maximum Power Point Tracking (MPPT) in a uniformly irradiated PV panel. The proposed method builds on the incremental conductance (InCond) algorithm and pushes the EZD method to the extreme: using only the switching ripple as the reference signal.

For all the applications, simulations and experimental results are presented to validate the proposed technique. A comparison with other methods is presented to validate the benefits of the technique.

Chapter 8 contains the relevant conclusions, contributions, and planned areas of future work derived from this thesis. The findings of this work contributed significantly to the implementation of DC systems; the value of this work is demonstrated by the seven relevant publications in international conferences and Transactions journals from the Institute of Electrical and Electronics Engineers (IEEE).
Chapter 2

Incremental Impedance Measurement in Power Electronics Converters

Reactive components connected to the Power Electronics Converter (PEC) and non-linearities in the sources and loads affect the dynamic behavior of the system. Their variation can be an indicator of problems and changes in the condition of the system. The extent of these characteristics cannot be inferred from simple measurements of the quiescent point of the PECs in a DC system, as it depends on changes around it. Figure 2.1(a) shows the V-I curve of a load that includes reactive components ($L$ and $C$) operating in DC. The straight line represents the resistive component of the impedance, while the ellipse shows the reactive behavior [181]: the amplitude is related to the magnitude, the phase shift of the major axis.

Portions of this chapter have been published in

Figure 2.1: Voltage vs. current \((V - I)\) curves of devices around a DC operation point and their incremental behavior: in (a) a resistive load with reactive component is shown, the DC resistance \(R_i = V_i/I_i\) do not reflect the reactive part, but the incremental behavior shows it; in (b) the characteristics of a non-linear load where \(R_i\) is not distinguishable from a resistor, but the incremental resistance \((dv/di)\) is negative.

to the phase shift, and the direction of rotation to capacitive (clockwise rotation) or inductive (counter clockwise) behavior. From the quiescent point (the DC voltage and current), only the resistive part can be calculated. Figure 2.1(b) shows the behavior of a non-linear load: from the DC operating point, it cannot be differentiated from a resistive load, but the incremental behavior shows its negative resistance.

An advanced algorithm to extract the incremental behavior of the voltage and current, named Embedded Impedance Detection (EZD), is introduced in this chapter. This method allows the extraction of reactive and non-linear behavior around the DC operating point. The proposed EZD method uses sensors typically found in a PEC (current and voltage) and the embedded microcontroller, along with digital algorithms, such as the Moving Average Filter (MAF) and the Lock-In Amplifier (LIA), to extract the incremental impedance seen from the terminals of the PECs. The high sensitivity and selectivity of the proposed technique allow for a minimal reference signal \((r[k])\) to be used to extract the incremental impedance. Even with the outlined benefits, the implementation of the EZD can be carried out in an industry-standard microcontroller; this adds all the benefits of the EZD without adding cost.
Figure 2.2: Block diagram of the DSP based control and supervision system for power electronics converter (PEC); the diagram includes the trip-zone (TZ) hardware protections and the sampling process (ADC+averaging) and control and modulation blocks; it includes the proposed Embedded Impedance Detection (EZD) method and the particular application block (APP) for the detected impedance; this chapter focuses on the blue highlighted blocks that generate the reference \( r[k] \) to be injected through the controller, the Lock-In Amplifier (LIA) to extract the effect of \( r[k] \) on \( v[k] \) and \( i[k] \), and the Impedance Calculation (IC) to combine these effects and compute the incremental impedance \( z \), the following chapters focus on the application blocks and modifications.

A general block diagram of the embedded system implemented for this work is presented in Fig. 2.2, outlining the different tasks and execution priorities, as well as signals needed for this analysis. This microcontroller is tasked with generating the gate signals to the PEC \( S_g \) based on the control decision derived from the measurements of the voltage and current \( (v, i) \) from the PEC. The uppermost layer includes the highest priority (most time-critical) tasks of the PECs controller: sampling using the Analog to Digital Converter (ADC) to convert the analog signals \( v(t) \) and \( i(t) \) to the sampled domain \( (v[k] \text{ and } i[k]) \), averaging, control to regulate the converter through the duty cycle \( (d) \), Pulse Width Modulation (PWM) to convert \( d \) to the gate signals \( S_g \), and the protection blocks (trip-zone, TZ); these need to be executed in real-time otherwise risk damaging the PEC. The middle layer includes the bulk of the proposed technique: the LIA, the impedance calculation, and each application. The
individual application informs the supervisor system and communications. The rest of this chapter focuses on the analysis of the blocks highlighted in blue: the LIA and the Impedance Calculation (IC); the ensuing chapters are devoted to the block highlighted in orange, the particular applications and the modifications to the general scheme to fit them. This chapter first focuses on the generation and injection of $r[k]$ through the controller, then on extracting the effect of the reference in the voltage and current ($v[k]$ and $i[k]$), and then on using this information to calculate the measured impedance ($z$). A simulation example including a PEC, a resistive load with inductance, and a Constant Power Load (CPL) is presented to integrate the concepts discussed.

2.1 Reference Generation and Injection

In order to measure the impedance seen by the PEC at one of its ports, a reference signal ($r[k]$) of an arbitrary frequency ($f_r$) is internally generated and injected into the control system as shown in Fig. 2.2. For this work, $r[k]$ is given by

$$r[k] = A_r \sin (2\pi f_r T_s k),$$

where $A_r$ is the amplitude of the reference, $T_s$ is the sampling period, and $k$ is the sample index. Ultimately, the reference is digitally generated by the same microcontroller that computes the control loops and generates a sinusoidal variation of the PWM duty-cycle; however, depending on $f_r$, it must be injected at different stages of the control computation to ensure the reference passes through the regulation stages. The EZD extracts the incremental impedance at the selected $f_r$.

The control system of most PECs is tasked with regulating some voltages and currents of the PEC. It usually has more than one nested control loop to improve the performance,
Figure 2.3: Most power electronics converters (PECs) have nested control loops; in (a) the block diagram of a control system with a current loop (CL) nested inside a voltage loop (VL) with the possibility to add references at each stage; in (b) simple bode diagram showing the relative bandwidths of the control loops and the frequency of the different reference injected.

add protection (current limiting), or add special features (maximum power point tracking, current sharing through droop control, etc.). Figure 2.3(a) shows a typical control system with two nested loops: the voltage loop (VL) takes the voltage set-point ($v^*$) and compares it to the measured voltage ($v$), and the difference ($e_v$) is fed to the voltage controller ($C_v$) that produces the set-point for the current loop (CL); the CL takes this set-point ($i^*$) and calculates the difference with the measured current ($i$) and feeds this error ($e_i$) to the current controller ($C_i$) that produces the duty-cycle ($D$) for the Pulse Width Modulation (PWM) generator. More control loops can be added on top of these to provide additional features (such as maximum power point tracking or current sharing using droop control).

Each nested controller (such as current or voltage) is designed to be compatible with the others in the loops, as it is represented in Fig. 2.3(b). As a general rule, the innermost loop
(CL in this case) is designed to have a bandwidth (BW) ten times smaller than the switching frequency ($f_{sw}$):

$$CL_{BW} \approx \frac{f_{sw}}{10}. \tag{2.2}$$

In this way, the converter follows the description provided by the small signal approximation around the operating point. The BW of the $VL$ ($V_{LBW}$) is selected ten times smaller than $CL_{BW}$:

$$V_{LBW} \approx \frac{CL_{BW}}{10}. \tag{2.3}$$

This ensures the $CL$ follows the reference as if it were an ideal source. Depending on which band $f_r$ resides in, $r[k]$ needs to be generated differently.

Figure 2.3 shows the different types of $r[k]$ ($v^r$, $i^r$, $d^r$). For $r[k]$ that fall inside the bandwidth of the voltage control loop, $r[k]$ is generated as a voltage reference ($v^r$) with a frequency $f_{vr}$ and injected along with $v^*$. For medium speed (those faster than the bandwidth of the voltage loop and slower than the bandwidth of the current loop), $r[k]$ is generated as a current reference ($i^r$) with a frequency $f_{ir}$ and injected along with $i^*$. Finally, a very fast $r[k]$ (faster than the current control loop) is generated as a direct perturbation of the duty-cycle $d^r$ and added to the output of the $CL$ ($D$) with a frequency $f_{dr}$. It is not possible to use $f_r$ higher than $f_{sw}$, as the PWM only generates one control action per cycle.

Computing trigonometric functions, such as $r[k]$ in real time is resource-intensive, especially if the microcontroller does not have a dedicated accelerator (such as the Trigonometric Math Unit, TMU, in some Texas Instruments microcontrollers), but the specific application in this work offers characteristics that can be exploited to make an efficient implementation. Since $r[k]$ is synchronized with the PWM and the control loop, there are a fixed number of samples ($N$) in the sequence $r$, given by

$$N = (f_r T_s)^{-1}. \tag{2.4}$$
Then, the finite sequence

\[ r[i] = \left\{ A_r \sin \left( \frac{2\pi}{N} i \right) \right\}, \quad 0 \leq i < N \]  

(2.5)

is related to the running sequence \( r[k] \) by

\[ r[k] = r[k \mod N]. \]  

(2.6)

where the notation "\( k \mod N \)" means the remainder of the integer division of \( k \) by \( N \) (e.g. \( 7 \mod 6 = 1 \)). For example, with \( T_s = 100 \mu s \) and \( f_r = 2.5 \text{ kHz} \), \( N \) is given by (2.4):

\[ N = ((2.5 \text{ kHz}) (100 \mu s))^{-1} = 4, \]  

(2.7)

and the finite sequence is

\[ r[i] = \left\{ A_r \sin (0), A_r \sin \left( \frac{\pi}{2} \right), A_r \sin (\pi), A_r \sin \left( \frac{3\pi}{2} \right) \right\}. \]  

(2.8)

A representation of this reference generation method for an \( r[k] \) that is injected into \( d \) is shown in Fig. 2.4. The values of \( r[i] \) are precalculated and stored in a register that is scanned using an index (\( i \)) that wraps back to 0 after \( N \) steps. This is known as a “circular buffer”. After picking the correct value from \( r[i] \), it is added to \( D \) which is updated in the next switching period.

This proposed method to obtain \( r[k] \) from a finite list reduces the reference generation to a simple read from a circular buffer of size \( N \). If memory is constrained, the symmetry property of the \( r[k] \) can reduce the memory footprint to \( N/4 \) with some additional operations. Another advantage of this method is its independence of time.
2.2 Signal Extraction

After $r[k]$ is injected in the system and it propagates to the voltage and current, its effect must be extracted using digital signal processing. The input to the signal extraction stage ($x(t)$) can be divided in

$$x(t) = x_s(t) + x_r(t),$$

where $x_s$ is the part of $x$ that comes from the behavior of the system without $r[k]$ (such as closed loop response and switching ripple), and $x_r$ is the effect of the reference in the system, reflected in the signal $x$ (voltage or current response). That is, $x_r$ is the part of the signal that needs to be analyzed with the signal extraction process and $x_r$ represents interference. The interference can be in the form of noise, switching event, or DC behavior of the signal.
Figure 2.5: Signal-processing chain from a sensor (S), through an amplifier/low pass filter (LPF), an over-sampled Analog to Digital Converter (ADC), a Moving Average Filter (MAF) to remove the switching effects, a rate transition (RT) to adjust to the control loop sampling period, and finally feeding the Lock-In Amplifier (LIA) for signal extraction and the control loop for regulation; the different colors indicate the time domain of the signals.

The signal \( x_r \) is then given by

\[
x_r(t) = \sum_{n=1}^{\infty} A_n \sin (2\pi n f_r t + \theta_n). \tag{2.10}
\]

Where \( A_n \) and \( \theta_n \) are the amplitude and phase of the Fourier decomposition of \( x_r \). The harmonics are considered from \( n = 1 \) to infinity for generality.

To calculate the incremental impedance at \( f_r \), only the amplitude of the first component \( (A_1) \) and its phase-shift \( (\theta_1) \) need to be extracted. The proposed digital LIA offers high dynamic range to extract this small oscillation from the large DC value (up to references of 0.1% of the DC value) using the same sensors included for the control loop.

The signal-processing chain for each of the signals in the system is shown in Fig. 2.5 from the magnitude transducer to separating \( A_1 \) and \( \theta_1 \). The blocks up until \( x[k] \) are mandatory in order to implement the control loop, so they do not add computation overhead. The blocks indicated with a dashed trace are rate transitions (RT), either from the continuous domain \((t)\) to a sampled one (using the ADC), or between two different sampling rates \((T_s' \text{ to } T_s)\). The oversampling of signals is implemented when it is necessary to average the switching ripple from the voltage and current and make the control decision based on the average.
The magnitude to be measured \((v, i)\) is transformed by a sensor (S in the diagram) that produces a voltage output proportional to the magnitude. This sensor could be a simple shunt resistor, a hall effect sensor, or voltage divider. The signal \(x\) is then amplified to fit the requirements of the ADC and filtered using a Low Pass Filter (LPF) to remove the high-frequency components of \(x\) that would cause aliasing. After the LPF, the band-limited version of \(x\), \(x_{\text{bl}}\), is

\[
x_{\text{bl}}(t) = x_{s,\text{bl}}(t) + \sum_{n=1}^{N_{\text{max}}} A_n \sin(2\pi n f_r t + \theta_n),
\]

where \(N_{\text{max}}\) is the maximum harmonic of \(f_r\) that is let through by the LPF.

In the following sections, the main building blocks of the signal chain are discussed in detail. The Moving Average Filter (MAF) serves as a building block of the digital Lock-In Amplifier (LIA) and to remove the effects of the switching ripple. The digital LIA allows the extraction of \(A_1\) and \(\theta_1\) from signals with large offset and noise.

2.2.1 Moving Average Filter

The MAF is a simple digital filter that has low pass characteristics, plus the ability to completely remove some specific frequencies. For a given input signal \((x[k])\), the output of the MAF \((\bar{x}[k])\) is given by

\[
\bar{x}[k] = \frac{1}{M} \sum_{i=0}^{M-1} x[k - i],
\]

where \(M\) is the order of the filter (number of samples in the average). Since the output can be expressed as a finite sum of the input delayed, the MAF is a Finite Impulse Response (FIR) filter, which offers advantages such as guaranteed Bounded-Input Bounded-Output (BIBO) stability and linear phase.
Figure 2.6: Block diagram of the Moving Average Filter (MAF) using (a) a non-recursive implementation vs. (b) a recursive implementation.

Computation of the MAF

A block diagram of the MAF is presented in Fig. 2.6(a), where it can be seen that for a MAF of order $M$, this implementation needs a buffer of size $M$, and needs to compute $M$ sums and one product. This is an expansion of the block labeled MAF in Fig. 2.5. This is feasible for small $M$s, but would be too slow to implement in real time for larger $M$s.

A more computationally efficient way to implement the MAF would be looking at the change in $\bar{x}$ between two steps. From (2.12) the previous iteration of the filter ($\bar{x}[k - 1]$) is

$$\bar{x}[k - 1] = \frac{1}{M} \sum_{i=0}^{M-1} x[k - 1 - i].$$  \hspace{1cm} (2.13)

Then the change between the steps is

$$\bar{x}[k] - \bar{x}[k - 1] = \frac{1}{M} \sum_{i=0}^{M-1} x[k - i] - \frac{1}{M} \sum_{i=0}^{M-1} x[k - 1 - i].$$  \hspace{1cm} (2.14)
Removing all the terms that cancel out from the right hand side of (2.14), the increment is
\[ \bar{x}[k] - \bar{x}[k - 1] = \frac{x[k] - x[k - M]}{M}, \quad (2.15) \]
and the running output of the filter is
\[ \bar{x}[k] = \bar{x}[k - 1] + \frac{x[k] - x[k - M]}{M}. \quad (2.16) \]

This is known as \textit{recursive implementation}, and offers the advantage of requiring two sums and one product for any size \( M \). The block diagram of this implementation is shown in Fig. 2.6(b). It is important to note that neither the memory footprint of the filter nor its FIR nature change.

Inspection of (2.16) shows that, although the number of operations to calculate \( \bar{x}[k] \) is independent of \( M \), it is still necessary to shift the data through the entire delay chain, which has \( O(M) \) operations; this might be too much for a real-time implementation. The shifting is solved using the same kind of circular register used to generate \( r[k] \). This implementation computation time is independent of \( M \).

**MAF Output and Frequency Response**

\( M \) needs to be selected such that it removes some specific frequencies. This is reflected in its Discrete Time Fourier Transform (DTFT) given by
\[ H (e^{j2\pi T_s f}) = \frac{1}{M} \frac{1 - e^{-j2\pi T_s fM}}{1 - e^{-j2\pi T_s f}}. \quad (2.17) \]
where \( f \) is the frequency parameter and \( T_s \) is the sampling time. The filter has a magnitude of
\[ |H (e^{j2\pi T_s f})| = \frac{1}{M} \sqrt{\frac{1 - \cos(2\pi T_s f M)}{1 - \cos(2\pi T_s f)}}, \quad 0 \leq f \leq \frac{1}{2T_s} \quad (2.18) \]
Figure 2.7: Characteristics of the Moving Average Filter (MAF); in (a) the magnitude of the frequency response shows the unitary gain at 0, the notches at $f = n/T_s M$, and the generally lower gain of the filter for higher $M$; in (b) the step response of the same MAF shows the added delay of the filter when $M$ increases.

which is shown in Fig. 2.7(a) for different values of $M$. The following features can be observed from the plot:

- $|H(e^{j2\pi T_s f})| = 1$, for $f = 0$,

- $|H(e^{j2\pi T_s f})| = 0$, for $f = n/T_s M$, with $n = 1, 2, \ldots, M/2$,

- a peak in between each notch, that is attenuated for larger $M$.

Therefore, to remove a signal with frequency $f_r$, $M$ should be chosen such that

$$M = \frac{n}{T_s f_r}.$$  \hspace{1cm} (2.19)

There are many values of $M$ that completely remove the signal at $f_r$. Picking a different $n$ places $f_r$ at the $n$-th notch of $H(e^{j2\pi T_s f})$. The minimum $M$ that can notch $f_r$ (for a given $T_s$) is found when $n$ is one:

$$M_{\text{min}} = \frac{1}{T_s f_r}.$$  \hspace{1cm} (2.20)
Placing \( f_r \) in the \( n \)-th notch requires to average \( n \) periods of the signal at \( f_r \). By selecting the number of periods \( (N_p) \), it is possible to increase the frequency resolution and the attenuation of the filter, but the response becomes more delayed and the memory footprint expands (the time window expands). The final size of the filter is given by

\[
M = N_p \times M_{\text{min}}.
\]  

(2.21)

The step response of the MAF with different sizes is shown in Fig. 2.7(b). The output delay is directly proportional to \( M \). Therefore, a trade-off needs to be found between the attenuation required, the number of notches, the delay, and the memory footprint. This balance is application-specific.

### 2.2.2 Digital Lock-In Amplifier

The Lock-In Amplifier (LIA) is an algorithm that uses the injected \( r[k] \) and extracts the response of the system at the selected \( f_r \). Many instruments can extract the response of the system, but they are generally expensive dedicated pieces of equipment (such as a network analyzer or frequency response analyzer). In this work, an embedded digital version of the LIA is proposed, which allows accurate extraction of the effect of \( r[k] \) on \( v \) and \( i \), which can be used for impedance measurement. This implementation uses the sensors commonly present in the PEC.

**LIA Analysis**

A block diagram of the digital LIA is shown in Fig. 2.8(a), this is an expansion of the block labeled LIA in Fig. 2.5. The input signal \( x \), given by (2.11) is multiplied by a sine and cosine
Figure 2.8: In (a) the block diagram of the proposed implementation of the digital Lock-In Amplifier (LIA), the Magnitude and Phase (MAP) block combines the quadrature and direct components to obtain the desired phase and magnitude; in (b) a simplified outline of the operation of the LIA for the $x_d$ signal.

\[
x_d[k] = x[k] \sin (2\pi f_r T_s k) \tag{2.22}
\]

\[
= \left( x_s[k] + \sum_{n=1}^{N_{max}} A_n \sin (2\pi n f_r T_s k + \theta_n) \right) \sin (2\pi f_r T_s k),
\]

and

\[
x_q[k] = x[k] \cos (2\pi f_r T_s k) \tag{2.23}
\]

\[
= \left( x_s[k] + \sum_{n=1}^{N_{max}} A_n \sin (2\pi n f_r T_s k + \theta_n) \right) \cos (2\pi f_r T_s k).
\]
Considering the detailed expansion of (2.22)

\[ x_d[k] = x_s[k] \sin (2\pi f_r T_s k) + \left( \sum_{n=1}^{N_{\text{max}}} A_n \sin (2\pi n f_r T_s k + \theta_n) \right) \sin (2\pi f_r T_s k) , \quad (2.24) \]

which shows that \( x_s \) is modulated up in frequency to \( f_r \). The second term shows the product of all the harmonics with the sine wave. Expanding the second term of (2.24) using the trigonometric identity

\[ \sin \alpha \times \sin \beta = \frac{\cos (\alpha - \beta) - \cos (\alpha + \beta)}{2}, \quad (2.25) \]

yields

\[
x_d[k] = x_s[k] \sin (2\pi f_r T_s k) + \sum_{n=1}^{N_{\text{max}}} \frac{A_n}{2} \left( \cos (2\pi (n - 1) f_r T_s k + \theta_n) - \cos (2\pi (n + 1) f_r T_s k + \theta_n) \right). \quad (2.26)
\]

This operation splits the amplitude of \( A_n \) between one harmonic up \((n+1)\) and one harmonic down \((n-1)\). This operation is illustrated in Fig. 2.8(b) (in a simplified case with no phase shift).

The signal \( x_d \) is then fed through a MAF tuned for \( f_r \) and its harmonics. Given (2.18) and (2.26), the following is observed:

- In steady-state \( x_s[k] \) does not include high-frequency components; its DC value is eliminated by the notch at \( f_r \).

- For \( n = 2, 3, ..., N_{\text{max}}, \) \( n + 1 \) and \( n - 1 \) fall in a notch of the MAF and they are completely eliminated.

- For \( n = 1, \) \( n + 1 \) falls in the second notch, while \( n - 1 = 0 \) falls in the DC gain of the MAF, which is one.
Considering these observations, it can be seen that in steady-state, the output of the MAF assigned to \( x_d[k] \) is
\[
\bar{x}_d[k] \approx \frac{A_1}{2} \cos(\theta_1).
\] (2.27)

An analogous study can be done for (2.23) using the trigonometric identity
\[
\sin \alpha \times \cos \beta = \frac{\sin (\alpha - \beta) + \sin (\alpha + \beta)}{2},
\] (2.28)

which yields
\[
\bar{x}_q[k] \approx \frac{A_1}{2} \sin(\theta_1).
\] (2.29)

Combining (2.27) and (2.29), the magnitude and phase (MAP) block in Fig. 2.8 as
\[
A_1 = \sqrt{\bar{x}_d^2 + \bar{x}_q^2},
\] (2.30)
\[
\theta_1 = \tan^{-1}_{4Q}\left(\frac{\bar{x}_q}{\bar{x}_d}\right),
\] (2.31)

where \( \tan^{-1}_{4Q}(\cdot) \) is the four-quadrant inverse tangent\(^1\).

For some applications, it is neither useful nor efficient to compute (2.30) and (2.31), as it requires the computation of square roots and inverse tangents. The outputs of the algorithm can be
\[
X_d = A_1 \cos \theta_1,
\] (2.32)
\[
X_q = A_1 \sin \theta_1,
\] (2.33)

as shown in Fig. 2.8(a). These outputs allow the computation of the impedance components from products and divisions, which are easier to compute.

\(^1\)In (2.27) and (2.29) the equation use the approximate instea d of the quality to account for the case of spectral leakage due to the time-limited window. This effect is reduced for longer windows due to the increase attenuation of the MAF. Moreover, this effect is much smaller in steady-state, when the DC component of \( x_s \) is dominant.
Equations (2.30) and (2.31) or (2.32) and (2.33) yield the ultimate output of the LIA, yet some implementation details need to be noted before moving on to the impedance calculation, namely the generation of the sine and cosine and the MAF size selection.

**Sine and Cosine Generation**

In order to compute the LIA, it is necessary to have available a sine and cosine pair, and this can be computationally intensive. As it was mentioned in Section 2.1, when the filter and PWM are completely synchronized, it is possible to precalculate the finite sequence (2.5), and the same can be done for the sine signal:

\[ s[i] = \sin \left( \frac{2\pi}{N} i \right), \quad 0 \leq i < N, \quad (2.34) \]

with \( N \) given by (2.4). The sine signal is then computed as

\[ \sin (2\pi f_r T_s k) = s[k \mod N], \quad (2.35) \]

updated every \( T_s \). It is evident from (2.6) and (2.35) that the reference can be generated by simply having

\[ r[k] = A_r s[k \mod N]. \quad (2.36) \]

Given the symmetric properties of the sine and cosine

\[ \sin(\theta) = \cos(\theta + \frac{\pi}{2}), \quad (2.37) \]

or, in terms of \( s[i] \),

\[ \cos (2\pi f_r T_s k) = s \left[ \left( k + \frac{N}{4} \right) \mod N \right], \quad (2.38) \]
if $N$ is an integer multiple of four. This method to generate $r[k]$ along with the sine and cosine pair is illustrated in Fig. 2.9. As it is observed, the method uses a single circular buffer of size $N$ and two indexes to compute the reference and all the sine and cosine pairs.

**LIA’s MAF Size Selection**

Selecting the size of the MAF ($M$) is important to guarantee that the filter eliminates the desired frequency $f_r$ and that it attenuates all the bands around the different frequencies enough. A trade-off between the memory footprint, delay, frequency resolution, and noise rejection need to be developed for each application.

For a given reference signal $r[k]$, of frequency $f_r$ sampled at $T_s$, the number of samples in the signal is given by (2.4),

$$N = (f_r T_s)^{-1},$$

(2.39)
which is the same as (2.19) for \( n = 1 \)

\[
M = \frac{1}{T_s f_r}. \tag{2.40}
\]

This yields that the minimum size of the MAF to eliminate \( f_r \) is the same number of samples as the reference has:

\[
M_{\text{min}} = N. \tag{2.41}
\]

This is reasonable since a moving average of a sine wave that has a window of exactly one period is zero. To increase the noise immunity, \( n \) in (2.19) can be increased. Under this consideration, \( n = N_p \) becomes the \textit{number of periods of} \( r[k] \) \textit{to average}.

By selecting \( N_p \), the size of the MAF is then

\[
M = N_p \times N. \tag{2.42}
\]

Increasing \( N_p \) increases the noise rejection, the attenuation of the side bands, the convergence time, and the memory footprint. It also reduces the frequency interference during the analysis.

**LIA Simulations**

A simulation example of the LIA is presented in Fig. 2.10(a). A simple \( RC \) circuit is shown, there is an input voltage source \( (v_{in}) \) that has a constant value of 1 V. The signal detected \( (x) \) is the capacitor voltage. During the simulation, the value of \( R \) suddenly changes from 0.5 \( \Omega \) to 2.0 \( \Omega \).

The frequency response of the system is given by

\[
X(j\omega) = \frac{1}{j\omega RC + 1}. \tag{2.43}
\]
Figure 2.10: In (a) a sample circuit to illustrate the behavior of the proposed Lock-In Amplifier (LIA) where the reference is injected as a voltage and the resistance \((R)\) changes; in (b) the Bode plot of the circuit before and after the change of resistance indicating the gain and phase at the reference frequency \((f_r)\).

Since \(R\) changes during the simulation, \(X(j\omega)\) changes as well. Bode plot of the two scenarios is shown in Fig. 2.10(b) indicating the magnitude and phase at \(f_r\) \(|X(j2\pi f_r)|_R\) and \(\angle X(j2\pi f_r)_R\).

The \(r[k]\) is injected at the voltage control stage \((v^r[k])\) with the parameters outlined in Table 2.1, given by

\[
v^r[k] = r[k] = A_r \sin (2\pi f_r T_s k).
\] (2.44)

The simulations are shown for a deterministic case (no noise injected) for different \(N_p\), and a fixed \(N_p\) adding noise. The objective of the LIA is to extract the effect of the reference on the system \((A_1\) and \(\theta_1)\). Based on this and \(X\), the expected values for the outputs of the
Table 2.1: Sample LIA Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Frequency</td>
<td>$f_r$</td>
<td>1 Hz</td>
</tr>
<tr>
<td>Reference Amplitude</td>
<td>$A_r$</td>
<td>0.01</td>
</tr>
<tr>
<td>Number of Reference Samples</td>
<td>$N$</td>
<td>16</td>
</tr>
<tr>
<td>Number of Averaged Periods</td>
<td>$N_p$</td>
<td>1, 2, 4</td>
</tr>
<tr>
<td>Sampling Period</td>
<td>$T_s = 1/Nf_r$</td>
<td>1/16 s</td>
</tr>
</tbody>
</table>

LIA are

$$A_1 = A_r \times |X(j2\pi f_r)|,$$

$$\theta_1 = \angle X(j2\pi f_r).$$

This shows how the LIA is able to extract the response of the system to the selected $r[k]$ around the DC operating point. The main limitation in the extraction depends on the resolution of the ADC, which limits how small a signal can be and still be detected (oversampling can be implemented to extend the resolution [182]).

The simulation results for the deterministic case (without noise) are shown in Fig. 2.11(a) neglecting the start-up of the system. Both before and after the change in $R$, $A_1$ and $\theta_1$ accurately measure the expected values. The outputs are shown for several number of averaged periods ($N_p$); as it can be observed, increasing $N_p$ slows the response of the system. From the knowledge of $A_r$ it is possible to reconstruct the value of $X$ at $f_r$.

The outputs of the simulated system for the case with significant measurement noise ($\eta$) are shown in Fig. 2.11(b) compared with the deterministic case (both with $N_p = 4$). The noise is generated using Simulink’s Band-Limited White Noise block with a Noise Power of $1 \times 10^{-6}$. The resulting amplitude of the injected noise is the same as $A_r$. With this noise,
Figure 2.11: In (a) the signal \( x \) and the outputs of the LIA \( A_1 \) and \( \theta_1 \) for different number of averaged periods \( (M_p) \); in (b) significant noise is added to \( x \) and the \( A_1 \) and \( \theta_1 \) are shown for \( M_p = 4 \) with and without noise (\( \eta \)).

The standard deviation (normalized) in steady state over a period of the MAF, given by

\[
s_{A_1} = 100 \times \frac{\sqrt{\sum_{n=1}^{N_p N} \left( A_1[k-n] - A_{1,R_x} \right)^2}}{A_{1,R_x}}
\]

is below 5%.

These simulations illustrate the principle of operation of the proposed LIA and the effect of the design parameters. Using the LIA, it is possible to build an instrument to extract the effect of selected signals on one of the variables of the system. The selection of the parameters depends on the particular application.
2.3 Impedance Calculation

Once the injected $r[k]$ propagates through the system and the LIA extracts its effect on a variable, these results can be combined to detect the incremental impedance ($z$). The outputs of the EZD can be calculated in terms of magnitude and phase ($|z|$ and $\theta_z$) or as the real and imaginary part ($z = r + jx$), which might be adequate for some specific applications.

A block diagram of this implementation is shown in Fig. 2.12; this diagram expands on the block diagram of Fig. 2.2. Two LIA blocks, one for a voltage ($v$) and one for the current ($i$), are implemented; since the two LIAs are synchronized only one $r[k]$, and one sine and cosine pair are needed. To calculate $|z|$ and $\theta_z$ each LIA produces two outputs: a magnitude ($A_{1,x}$) and a phase ($\theta_{1,x}$), where $x$ stands for $v$ or $i$.

From $A_{1,x}$ and $\theta_{1,x}$, the magnitude of $z$ at $f_r$ is calculated using the block diagram in Fig. 2.12(a):

$$|z| = \frac{A_{1,v}}{A_{1,i}}, \quad (2.48)$$
and the phase measurement is given by

$$\theta_z = \theta_{1,v} - \theta_{1,i}. \quad (2.49)$$

From these, \(r\) and \(x\) can be calculated as

$$r = |z| \cos \theta_z, \quad (2.50)$$
$$x = |z| \sin \theta_z. \quad (2.51)$$

Unfortunately, (2.50) and (2.51) require the computation of the sine and cosine of \(\theta_z\) in real time (and they use the results from (2.30) and (2.31), that require the computation of inverse tangents.

For applications where \(r\) and \(x\) are necessary, a better implementation can be obtained by computing the complex division of the pair

$$v_1 = v_d + j v_q, \quad (2.52)$$
$$i_1 = i_d + j i_q, \quad (2.53)$$

as shown in Fig. 2.12(b). Then, \(z\) is given by

$$z = \frac{v_d + j v_q}{i_d + j i_q} \quad = \frac{v_d i_d + v_q i_q}{i_d^2 + i_q^2} + j \frac{v_q i_d - v_d i_q}{i_d^2 + i_q^2}. \quad (2.54)$$
Using (2.54) $r$ and $x$ are given by

\begin{align}
    r &= \frac{v_d i_d + v_q i_q}{i_d^2 + i_q^2}, \\
    x &= \frac{v_q i_d - v_d i_q}{i_d^2 + i_q^2},
\end{align}

which avoid the calculation of $\tan^{-1}(\cdot)$ (and the multiplication by 2, for that matter) in the LIA, and the sine and cosine calculations in (2.50) and (2.51). Moreover, the denominator of (2.55) and (2.56) is the same, so it only needs to be calculated once.

**Admittance Calculation**

Through this section, the calculations are referred to as “impedance calculation”, but the same information can be used to calculate the admittance. For some applications, the relationships are more directly evident or apparent by using the conductance. In general, the admittance is given by

$$y = g + j b,$$

where $g$ is the conductance and $b$ is the susceptance.

From the outputs of the two LIAs, $y$ is given by

$$|y| = \frac{A_{1,i}}{A_{1,v}},$$

and the phase is given by

$$\theta_y = \theta_{1,i} - \theta_{1,v}.$$
From these, \( g \) and \( b \) can be calculated as

\[
g = |y| \cos \theta_y, 
\]

\[
b = |y| \sin \theta_y. 
\]

Moreover, the complex division version is given by

\[
g = \frac{v_d i_d + v_q i_q}{v_d^2 + v_q^2}, 
\]

\[
b = \frac{i_q v_d - i_d v_q}{v_d^2 + v_q^2}. 
\]

Through this document, the method is referred to as “impedance detection”, even when using \( y \), to maintain clarity. If the application calls for the use of \( y \), it is indicated in the equations, figures, and text.

### 2.4 Embedded Impedance Detection Simulations

This section presents simulation results for the proposed EZD method illustrating the behavior of the system for resistive loads and CPL. Figure 2.13 shows the simulated PEC, including the PWM, with the schematic of the two loads. The outputs of the EZD algorithm extraction of the incremental impedance value for the two sample loads.

The outputs of the simulation for a resistive load \( (R_n) \) with line inductance \( (L_l) \) are shown in Fig. 2.14(a). The load goes from \( R_n = 2.0 \) (half the nominal load) to \( R_n = 1.0 \) (nominal load). Since the load is resistive, the real part of \( z \) (\( r \)) is \( R_n \). The reactive part (\( x \)) reflects the value of the reactance at \( f_r \). Although \( r \) could be calculated in this example from the DC values \( (V_0 \text{ and } I_o) \), they give no information to calculate \( x \). For a passive load, the proposed EZD allows extraction of \( x \).
Figure 2.13: Simulation circuit for the proposed Embedded Impedance Detection (EZD) method; a standard dual loop controller is used \((i_L \text{ and } v_o)\) driving the duty-cycle of the PWM, and the EZD measures \(i_o\) and \(v_o\); the simulations include resistive load with line inductance \((R_n \text{ and } L_l)\) and constant power load \((\text{CPL})\).

The outputs of the simulation for a CPL are shown in Fig. 2.14(b). The CPL goes from 0.5 \((\text{half of the nominal load})\) to 0.75. The real part of the outputs of the EZD \((r)\) for the CPL is negative as expected: the incremental impedance of a CPL is negative. Since the CPL is ideal in the simulation, its bandwidth is infinite, and \(x\) is zero. For the CPL case, \(x\) can represent a) the effect of the line inductance, b) the effect of the input capacitor, or c) the behavior of a band-limited CPL. As opposed to the resistive load before, \(r\) cannot be inferred from the DC operating point directly: the ratio of \(V_o\) and \(I_o\) is always positive.

2.5 Summary

This chapter presented the general idea and analysis of the proposed Embedded Impedance Detection (EZD) method, based on the digital Lock-In Amplifier (LIA). It outlined the ability of the proposed technique to extract the incremental impedance from the DC system, as seen by the Power Electronics Converter (PEC). The main building blocks of the proposed EZD method, the reference \((r[k])\) generation, the Moving Average Filter (MAF), the LIA, and the Impedance Calculation, were studied analytically. Simulations of various individual stages,
as well as a simple integrated system, were presented. Special considerations were mentioned that outline its implementation in real-time with commercial microcontrollers.

The following chapters explore the use of this proposed technique to different applications. Each application looks at the particular requirements and modifications performed to the fundamental EZD algorithm introduced in this chapter. The system looks at the input port, as well as the output port of the PEC to provide useful, actionable information for a DC system.
Chapter 3

Transient Performance and Stability Improvement in DC Systems

Power Electronic Converters (PECs) connected to a grid, as shown in Fig. 3.1(a), interface loads that can have various different behaviors, such as resistive or constant power, or combinations of them. In the outlined grid, the PEC regulates the voltage of the bus, maintaining it within the requirements of the system. Since the output regulation provided by the PEC and its stability are dependent on the behavior of the load, it is important to either design a controller that is robust enough to handle any combination of load (i.e. 0 to 100% of rated load, 0 to 100% constant power), or to dynamically adjust the controller to the different loads. Robust controllers are usually tuned to guarantee stability in the most challenging scenario but sacrifice dynamic performance in many other conditions. The proposed Embedded Impedance Detection (EZD) method can be used to extract the equivalent load and adjust the controller to achieve reliable dynamic performance (in terms of maintaining the performance indicators such as overshoot and rise time) without sacrificing stability.

Portions of this chapter have been published in

In this chapter, the proposed EZD method is deployed to estimate the incremental behavior of the load of a PEC connected to a DC microgrid. This incremental load is used to dynamically tune the PEC’s controller to improve the performance of the system. An outline of the features of the proposed method is presented in Fig. 3.1(b). It uses only sensors already present in the system, output current and voltage, and is computed in real time by the microcontroller. This proposed EZD method is in turn used to implement the adaptive control technique that monitors the load and updates the controller coefficients ➊ to maintain reliable transient performance ➋ and extend the stability beyond normally tuned controllers ➌. Controllers are traditionally tuned using constant gains, and show overshoots that exceed the expected values for some loads and can fail for others. The ability of the proposed EZD
method to extract the incremental load behavior from the different combinations of loads, as well as the benefits of implementing the adaptive control, are validated through computer simulations. An experimental test set-up is deployed using a PEC controlled by a standard microcontroller, as well as resistances and electronic loads, to validate the ability of the EZD method to detect the equivalent impedance in a real setting. Finally, the implementation is compared against other load identification techniques to validate its advantages and outline the limitations.

3.1 System Model

In this section, a general outline of the system under study is presented. The block diagram of the proposed system is presented in Fig. 3.1(a); it consists of a PEC connected to a DC bus that feeds several types of loads, and that may include other Distributed Generators (DGs). The average and incremental behavior of the different composite loads as seen by the PEC are presented. The converter is controlled using a DSP that senses the variables of the PEC and implements an inner current control loop and an outer voltage control loop. The EZD method is used to extract the incremental load and update the PI controller for the outer loop. A model of the system and the controller is presented around the operating point, and the impact of the load in the selection of the controller is studied.

A schematic of the system under study is presented in Fig. 3.2. A buck converter is connected to the DC bus that interfaces some loads that are resistive (passive) and some that behave as Constant Power Loads (CPLs). The source is assumed to be ideal, able to provide the needed power for the system at this operating point. The PEC is controlled using a dual loop controller that can linearize the inner part (inductor current) and provide additional regulation and protections. The outer control loop is assumed to be slower than
Figure 3.2: Schematic diagram of the analyzed source-end Power Electronics Converter connected to a network feeding several loads; the loads are grouped in resistive loads \((R_L)\) and Constant Power Loads (CPLs).

the inner control loop, as it usually is the case, in order to provide the benefits of the dual loop controller.

### 3.1.1 Load Model

In a DC system, many loads with different behaviors are connected to the bus; altogether, they present a resistive behavior partially, and partially a CPL behavior. Although these loads present the same DC behavior (i.e., their average output voltage and current are the same), they influence the dynamic performance of the PEC differently.

In general, the load presents a relationship between its voltage \((v_L)\) and current \((i_L)\):

\[
i_L = f(v_L).
\]

In a DC system, \(v_L\) is mostly constant. The operating point of the DC load is then given by a point \((V_L, I_L)\) in the characteristic curve of the load. The equivalent DC conductance of the load is then defined as

\[
G = \frac{I_L}{V_L}.
\]

This represents the equivalent resistance seen by the source in this particular operating point.
The incremental behavior of the load gives the response of the current around the operating point, as a linearization:

\[ i_L \approx I_L + g \times (v_L - V_L), \quad (3.3) \]

where \( g \) is the incremental conductance presented by the PEC.

Resistive loads (and those active loads designed to behave as resistances) present a very well known characteristic, given by Ohm’s law. The current taken by the passive load \( (i_{RL}) \) is given by

\[ i_{RL} = \frac{v_L(t)}{R_L}, \quad (3.4) \]

where \( R_L \) is the equivalent resistance of all the passive loads in the network.

The DC characteristic of the resistive load is simple enough: for a DC load voltage \( (V_L) \), the current is given by

\[ I_{RL} = \frac{V_L}{R_L}. \quad (3.5) \]

Therefore, the DC conductance of the resistive load is given by

\[ G_{RL} = \frac{1}{R_L}. \quad (3.6) \]

The incremental conductance of the resistive load (i.e. the change in \( i_{RL} \), for a change in \( v_L \)) is clearly given by

\[ g_{RL} = \frac{di_{RL}}{dv_L} = \frac{1}{R_L}. \quad (3.7) \]

This behavior is illustrated in Fig. 3.3(a). The load behaves as a straight line with positive slope, as expected. A higher resistive load (lower \( R_L \)) draws higher \( I_{RL} \) and has a steeper slope.
Figure 3.3: Voltage and Current (V-I) curves of two types of load operating in DC operating points given by $V_L$, in (a) the curves of a resistive load for different resistance ($R_L$) values; in (b) the curves for a Constant Power Load (CPL) of different values.

The current in the CPL part of the load ($i_{CPL}$), on the other hand, is given by

$$i_{CPL} = \begin{cases} \frac{P_{CPL}}{v_L} & \text{if } v_L > V_{min}, \\ 0 & \text{if } v_L \leq V_{min}, \end{cases} \quad (3.8)$$

where $P_{CPL}$ is the combined power of all CPLs. While the CPL does not work for low $v_L$ (in order to prevent over current events, from (3.8)), in this chapter it is considered that $v_L$ is such that it does not go into shutdown mode.

The DC behavior of the CPL for different $P_{CPL}$ is shown in Fig. 3.3(b), showing its DC value and non-linear incremental behavior. The DC operating point is given by

$$I_{CPL} = \frac{P_{CPL}}{V_L}. \quad (3.9)$$
This DC conductance is indistinguishable from a resistive load with a conductance such that

\[ G_{CPL} = \frac{I_{CPL}}{V_L} = \frac{P_{CPL}}{V_L^2}, \quad (3.10) \]

as represented by the dashed lines in Fig. 3.3(b). However, the real incremental behavior of the CPL around \( V_L \) is given by

\[ g_{CPL} = \frac{d i_{CPL}}{dv_L} = -\frac{P_{CPL}}{V_L^2}, \quad (3.11) \]

which is negative (increasing \( v_o \) causes the CPL to draw less \( i_{CPL} \)). This negative \( g_{CPL} \) is highly challenging for controllers, as it pushes the poles of the characteristic equation to the right-half-plane, making the system unstable.

Since both types loads are connected in parallel to the bus, the total current that the load draws is given by

\[ i_L = i_{RL} + i_{CPL} = \frac{v_L}{R_o} + \frac{P_{CPL}}{v_L}. \quad (3.12) \]

When the operating point \( V_L \) and \( I_L \) are considered, the equivalent load \((G_e)\) is given by

\[ G_e = \frac{1}{R_L} + \frac{P_{CPL}}{V_L^2}, \quad (3.13) \]

which is seen as an equivalent resistive load, if the incremental behavior is ignored.

For the same \( V_L \) and \( I_L \), the incremental behavior is a combination of a fraction of CPL and a fraction of resistive load. The equivalent incremental behavior of the mixed load is given by

\[ g_e = \frac{1}{R_L} - \frac{P_{CPL}}{V_L^2}. \quad (3.14) \]

This behavior is shown in Fig. 3.4. Loads that are mostly resistive at the given operating point show a positive \( g_e \). Loads that are mostly CPL present a negative \( g_e \). For a load that is
Figure 3.4: Voltage and Current (V-I) curves of several loads that consume the same amount of power at $V_L$; each load has a combination of CPL and $R_L$ that total 100% at the operating point; since they all consume the same current ($I_L$), the nature of the load cannot be inferred from the DC values, but the incremental behavior is very different.

Precisely 50% CPL, $g_e = 0$: the extra current taken by the CPL is the same as the reduction on the resistive part.

Although the DC operating point of the mixed loads is the same as the resistive and the CPL, the stability of the system depends on $g_e$. The $g_e$ cannot be inferred from the DC operating point alone. Other components of the system can present reactive behavior (inductive and capacitive). The proposed EZD method detects both the magnitude and phase of the dynamic load in order to obtain the complete behavior.

### 3.1.2 Dynamic Model of the System

In this section, the system introduced in Fig. 3.2 is modeled around an operating point in order to determine: a) its stability and b) its dynamic response. The dynamic response and its dependency on the equivalent dynamic load are presented. The loads are connected to
The proposed controller uses two nested loops, a current loop for the inductor current \(i_{L_b}\) and another voltage loop for \(v_o\). In this work, the current loop is modeled as ideal, and the analysis focuses on the voltage loop, as indicated in Fig. 3.5(a).

The differential equation for the outer loop is given by

\[
C_b \frac{dv_o}{dt} = i_{L_b} - i_o = i_{L_b} - \frac{v_o}{R_L} - \frac{P_{CPL}}{v_L},
\]

where \(C_b\) is the output capacitor. The schematic of the system model is presented in Fig. 3.5(b). After linearizing around the operating point \((V_o, I_o)\), the incremental equation
is given by

\[ C_b s \tilde{v}_o(s) = \tilde{i}_L(s) - \left( \frac{1}{R_L} - \frac{P_{CPL}}{V_o^2} \right) \tilde{v}_o(s). \]  

(3.18)

where the tilde indicates the incremental variable. The incremental model of the PEC is presented in Fig. 3.5(b). In open loop ($\tilde{i}_{Lb} = 0$), the system is stable if the pole in (3.18) remains negative. This is obtained if

\[ \frac{1}{R_L} > \frac{P_{CPL}}{V_o^2}. \]  

(3.19)

When the control loop is closed, the control objective is considered to be $\tilde{v}_o = 0$. Using a PI controller, $i_L(s)$ is given by

\[ \tilde{i}_L(s) = \left( K_p + \frac{K_i}{s} \right) (-\tilde{v}_o(s)), \]  

(3.20)

where $K_p$ and $K_i$ are the proportional and integral gains respectively. The loop equation is then given by

\[ C_s \tilde{v}_o(s) = - \left( K_p + \frac{K_i}{s} \right) \tilde{v}_o(s) - \left( \frac{1}{R_L} - \frac{P_{CPL}}{V_o^2} \right) \tilde{v}_o(s) \]

\[ = - \left( g_{eq} + \frac{K_i}{s} \right) \tilde{v}_o(s), \]  

(3.21)

where

\[ g_{eq} = K_p + \frac{1}{R_L} - \frac{P_{CPL}}{V_o^2} = K_p + g_e, \]  

(3.22)

is the total equivalent resistive term and $g_e$ is given by (3.14).

The dynamic response to disturbances to the system is then given by

\[ P(s) = s^2 + \frac{g_{eq}}{C_b} s + \frac{K_i}{C_b} \]  

(3.23)
With the following characteristics

\[
\omega_n = \sqrt{\frac{K_i}{C_b}},
\]

\[
\varsigma = \frac{g_{eq}}{2\sqrt{K_iC_b}}.
\]

Two observations can be derived from (3.23), (3.24) and (3.25): a) the stability of the system is determined by

\[
g_{eq} > 0,
\]

or

\[
K_p > -g_e;
\]

and b) the dynamic response of the system is dramatically impacted by \(g_e\), even more so than by the total load, and this value can change in real-time. The use of the EZD method for determining \(g_e\) and an adaptive control scheme based on this real-time measurement is detailed are introduced in the following section.

### 3.2 Proposed Incremental Load Detection Scheme

The performance and stability of the controller under different load conditions are affected by the selection of \(K_p\) and \(K_i\). This section proposes a method to tune the controller, dynamically changing \(K_p\) and \(K_i\), based on the equivalent load. The proposed adaptive control is based on using the EZD method, built into the PEC, to measure \(g_e\) and adjusting the controller for the desired response; these key objectives are outlined in Fig. 3.1. The two critical steps of this approach are outlined in this section: measuring \(g_e\), and using this information to improve the controller.
3.2.1 Equivalent Incremental Load Detection

To measure $g_e$, the proposed EZD method is used. The reference signal, a small perturbation in the duty cycle ($d$), is added to the control loop of the PEC. The minimum size of the perturbation is limited by the sensitivity of the instrument, ADC, and sensors. The output of the algorithm, implemented using the conductance mode, are

$$
|\hat{y}_e| = \frac{\hat{A}_{1,i}}{A_{1,v}} \quad (3.28)
$$

$$
\hat{\theta}_{ye} = \hat{\theta}_{1,i} - \hat{\theta}_{1,v} \quad (3.29)
$$

where $\hat{A}_{1,i}$ and $\hat{A}_{1,v}$ are given by (2.30), and $\hat{\theta}_{1,i}$ and $\hat{\theta}_{1,v}$ are given by (2.31). Then,

$$
\hat{g}_e = \text{Re}(\hat{y}_e) = |\hat{y}_e| \cos(\hat{\theta}_{ye}) \quad (3.30)
$$

Figure 3.6(a) shows the V-I of the load connect to the PEC; the load combines a resistive part and a CPL part. In this case, the resistive part is larger than the CPL, denoted by the positive slope of the combined VI curve around the operating point. In Fig. 3.6(b), $v_o$ and $i_o$ for the PEC in this condition are shown; as it can be observed, the injected oscillation magnitude is related to the slope of the V-I curve. Since the load is mostly resistive, the oscillations in $v_o$ and $i_o$ is in phase, which leads to $\hat{\theta}_{ye} = 0$.

Figure 3.7(a) shows the V-I of the load connected to the PEC; the load combines a resistive part and a CPL part. In this case, the resistive part is smaller than the CPL, denoted by the negative slope of the combined VI curve around the operating point. The $v_o$ and $i_o$ for the PEC with this load are shown in the right of Fig. 3.7(b); as it can be observed, the injected oscillation magnitude is related to the slope of the V-I curve. The opposite phase of $v_o$ and $i_o$ clearly shows the $\hat{\theta}_{ye} = \pi$, characteristic of the CPL net result.
Figure 3.6: In (a) Voltage and Current (V-I) curves of a resistive load \((R_L)\) with a parallel CPL; the \(R_L\) presents a positive incremental behavior, while the CPL presents a negative incremental behavior; the black curve shows the VI curve of the combined load, since the resistance draws more power at this operating point, the incremental behavior is resistive \((g_e > 0)\); in (b) the time domain curves show the variation in \(v_o\) and the effect on each load separately \((i_{CPL} \text{ and } i_{R_L})\) and the combination, since the load is mostly resistive, the result is \(v_o\) and \(i_o\) are in phase.

An exceptional condition is presented when \(\hat{g}_e\), given by (3.14), approaches zero: any small error triggers the change of \(\hat{\theta}_{ye}\) between 0 and \(\pi\); this, however, is not reflected in a larger than typical error in the estimation. This condition is shown in Fig. 3.8(a), when the CPL exactly matches the resistive part. Since the estimation depends on the decomposition in real and imaginary parts (by multiplying by sine/cosine), the oscillation maps to a sign change in the real part. Since \(|\hat{y}_e|\) in itself is close to zero, the resulting amplitude is only around \(\pm \Delta Re/2\) (the measurement error). When \(|\hat{y}_e|\) is more substantial, this change does not show as a large oscillation, although the magnitude of the actual error is the same.

The selection of the EZD parameters (especially \(M\) and \(A_r\)) is dependent on the ripple tolerance of the system and the computational power available. Since the EZD method can be implemented very efficiently in the microcontroller (using very few computation resources in real time), the buffer size \(M\) can be incremented to increase the sensitivity of the technique.
Figure 3.7: In (a), the Voltage and Current (V-I) curves of a resistive load \( (R_L) \) with a parallel CPL; the \( R_L \) presents a positive incremental behavior, while the CPL presents a negative incremental behavior; the black curve shows the VI curve of the combined load, since the CPL draws more power at this operating point, the incremental behavior is CPL (\( g_e < 0 \)); in (b) the time domain shows the variation in \( v_o \) and the effects on each load and the net result, the net change is a 180° shifted in \( i_o \).

Critical information from the system can be extracted in real-time and used to improve the performance of the system using this technique.

### 3.2.2 Control Adjustment Technique

The equivalent load can be used to tune a controller to exhibit a set of desired response characteristics and be adjusted in real-time to keep the response constant using the information obtained from the EZD method. For this, a gain-scheduling technique is presented.

To ensure the stability of the small-signal model, the resistive contribution of the controller has to be kept at

\[
K_p + g_e > 0.
\]  

(3.31)

This presents a lower boundary for \( K_p \), especially when the load is mostly CPL (\( g_e < 0 \)).
Figure 3.8: In (a) the Voltage and Current (V-I) curves of a resistive load \( (R_L) \) with a parallel CPL; the \( R_L \) presents a positive incremental behavior, while the CPL presents a negative incremental behavior; the black curve shows the VI curve of the combined load, since the CPL and \( R_L \) draw precisely the same power at this operating point, the incremental behavior is null \( (\dot{y}_e = 0) \); in (b) the time domain shows how a displacement in \( v_o \) causes no change in \( i_o \), caused by the exact match between the variation of \( i_{RL} \) and \( i_{CPL} \).

The dynamic performance of the PEC is given by (3.24) and (3.25). Once again, it can be seen from (3.25) that \( \varsigma \) is influenced by \( g_e \) which works by adding gain to the loop (if the resulting load is CPL), or by subtracting it (if the resulting load is resistive). The selection of \( K_p \) has to be tuned to ensure stability and consistent dynamic response when the load changes.

The selection of the possible coefficients depends on \( g_e \): if \( g_e < 0 \), \( K_{pe} \) should be increased enough to meet (3.31) and then the final selection is made as

\[
K_i = C_b \omega_n^2, \tag{3.32}
\]

and

\[
K_p = 2C_b \omega_n s - g_e. \tag{3.33}
\]
This yields the desired response independently of the load. If $g_e > 0$, there is the possibility that (3.33) yields $K_p < 0$; in this case, it was preferred to keep $K_{pw} > 0$ and sacrifice some performance in order to avoid a nonminimal phase zero in the system.

The update of the controller coefficients is performed in steady-state, to avoid errors produced by transients in $\dot{y}_e$. During the transient, the PEC goes through a series of dynamic states; as shown in Fig. 3.4, $g_e$ is only defined at each operating point, not during the transients. Moreover, in a real implementation, the CPLs have limited bandwidth, which leads to a slower response and a transient behavior that is not entirely representative of the expected dynamic load. The proposed application allows the controller to add a margin of stability by adding some extra gain around the current operating point, instead of designing for the absolute worst transient.

### 3.3 Simulation Results

The previous section introduced the use of the proposed EZD method to measure the incremental behavior of the equivalent load and adapt the controller to it. Simulation results are presented in this section to validate the detection method and the proposed adaptive control approach. The simulations are performed over the circuit in Fig. 3.2. All the magnitudes in the simulation system are introduced in the normalized domain, according to the values in Table 3.1. This allows the simulation to be performed independently of the size of the PEC.

In order to validate the ability of the proposed algorithm to extract the incremental behavior of the total load, several transitions are tested that take the system from a pure resistive state to a mostly CPL state. Table 3.2 shows the different scenarios in the simulation, along with the increment in each kind of load, the total load, and the equivalent DC and incremental conductances calculated from (3.14) and (3.13). The loads are presented normalized
Table 3.1: Normalized Simulation Parameters for Equivalent Incremental Load Detection

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Normalized Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{o,n}$</td>
<td>1</td>
</tr>
<tr>
<td>$L_{b,n}$</td>
<td>$1/2\pi$</td>
</tr>
<tr>
<td>$C_{b,n}$</td>
<td>$1/2\pi$</td>
</tr>
<tr>
<td>$Z_{o,n}$</td>
<td>$\sqrt{L_b/C_b} = 1$</td>
</tr>
<tr>
<td>$I_{o,n}$</td>
<td>$V_{o,n}/Z_{o,n} = 1$</td>
</tr>
<tr>
<td>$f_{o,n}$</td>
<td>$1/2\pi\sqrt{L_bC_b}$</td>
</tr>
<tr>
<td>$t_n$</td>
<td>$t \times f_{o,n}$</td>
</tr>
<tr>
<td>$v_{o,n}$</td>
<td>$v_o/V_o^*$</td>
</tr>
<tr>
<td>$i_{o,n}$</td>
<td>$i_o/I_o^*$</td>
</tr>
<tr>
<td>$R_{o,n}$</td>
<td>$R_o/Z_o$</td>
</tr>
</tbody>
</table>

Table 3.2: Simulation Conditions for Testing the Equivalent Load Detection Algorithm

<table>
<thead>
<tr>
<th>Label</th>
<th>Resistive</th>
<th>CPL</th>
<th>Total Load</th>
<th>$G_n$</th>
<th>$g_{e,n}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.25</td>
<td>0</td>
<td>25</td>
<td>0.25</td>
<td>0.25</td>
</tr>
<tr>
<td>B</td>
<td>0.25</td>
<td>0</td>
<td>50</td>
<td>0.50</td>
<td>0.50</td>
</tr>
<tr>
<td>C</td>
<td>0</td>
<td>0.50</td>
<td>100</td>
<td>1.00</td>
<td>0.00</td>
</tr>
<tr>
<td>D</td>
<td>0</td>
<td>0.25</td>
<td>125</td>
<td>1.25</td>
<td>-0.25</td>
</tr>
</tbody>
</table>

with respect to $Z_{o,n}$; they are described as

$$P_n = \frac{V_{o,n}^2}{Z_{o,n}} = 1.$$  \hspace{1cm} (3.34)

Under these conditions, the start-up condition of a 0.25 resistive load means

$$R_{L,1,n} = \frac{V_{o,n}^2}{P_{R_{L,1}}} = \frac{1}{0.25} = 4.$$  \hspace{1cm} (3.35)

The steps in the load in CPL mode are given as a fraction of the unitary load.
The simulation results of the proposed technique are presented in Fig. 3.9. The upper plot shows $v_{o,n}$, while the lower plots show the outputs of the EZD method ($|\hat{y}_{e,n}|$ and $\hat{\theta}_{ye}$). The transients (A) and (B) present a resulting resistive behavior that is correctly captured by the algorithm. Transient (C) adds enough CPL to cause $|\hat{y}_{e,n}| = 0$ (which causes oscillations in $\hat{\theta}_{ye}$), as expected from measuring zero. If the load were to present a dynamic reactive component (considering input capacitance, connection inductance), the oscillation would not be noticeable, since the oscillation would be a minimal variation around $\pi/2$ (0.25 in the normalized domain). Finally, 0.25 CPL is added which causes the resulting $|\hat{y}_{e,n}|$ to be equal to the initial step, but with $\hat{\theta}_{ye} = \pi$. Even though the total load is 1.25, the incremental load is very different. The results in Fig. 3.9 show how the proposed algorithm can accurately measure the incremental behavior of the load from the injected perturbation.

It can be seen from Fig. 3.9 that the transient response of the EZD method goes through several values before settling in the correct value. This transient is mainly influenced by the transient in $v_o$ and $i_o$. During this transition, the information provided by the EZD algorithm (in the form of $|\hat{y}_{e,n}|$ and $\hat{\theta}_{ye}$) does not reflect the true nature of the equivalent dynamic impedance, since this is defined around a given operating point, in steady-state. During this transition, the controller cannot be adjusted using the output of the sensor; this adjustment should be made only in steady-state.

Next, transient simulations comparing the proposed controller against fixed controllers tuned for different nominal loading conditions are presented. Figure 3.10 shows the load profile used for the simulations. The load starts at zero and it periodically increases in steps of 25% of the nominal load until the full load condition is reached.

The simulation results for the sample application of the adaptive controller are shown in Fig. 3.11, and the same transients are presented for two fixed controllers tuned for 25% CPL in Fig. 3.12 and for 100% CPL in Fig. 3.13. During the simulation, more CPL is added in steps of 0.25 periodically; the performance of the PEC is evaluated accordingly. After the second
Figure 3.9: Simulation results of the proposed EZD method under load change conditions in the normalized domain; the load changes from 0.25 (resistive), adding 0.25 resistive, then adding 0.75 units of CPL in two steps; the output of the instrument shows the detection of the magnitude and phase of $\hat{y}_{e,n}$ as expected.

Figure 3.10: Load profile for the simulated transient; the CPL starts at 0% of the nominal load and periodically increases by 25% until nominal load is reached.
step, the controller tuned for 25% CPL becomes unstable. The controller tuned for 100% CPL is stable all the time since it was tuned for the worst condition. However, it presents variable performance, including oscillations, compared with the adaptive controller. The oscillations are observed during the transients for the 100% CPL controller, given by the interaction with the current loop. In order to compensate for the expected CPL, the bandwidth of the voltage loop is pushed too close to that of the current loop. New coefficients can be selected to improve the dynamic performance and stability of the controller in real-time following (3.32) and (3.33).

### 3.4 Experimental Results

The simulations in the previous section showed that the proposed EZD method could capture the incremental behavior of the load for both resistive, CPL, and mixed loads; however, it remains to be tested that the this can be performed in a real PEC with standard sensors and real CPLs. To further validate the use of the proposed algorithm, an experimental set-
Figure 3.12: Simulation capture of the standard controller tuned for 25% CPL condition; the transient coincides with the proposed adaptive technique for the first step, but changes after the second, and becomes unstable at the third.

Figure 3.13: Simulation capture of the standard controller tuned for 100% CPL condition; the transient coincides with the proposed adaptive technique for the last step, but in the intermediate steps shows poor performance and oscillations.

up was built with components that maintain the relationships outlined in the normalization procedure in Table 3.1, and the outputs of the proposed instruments were logged.

The tests are implemented in a power platform, as shown in Fig. 3.14. The power supply (a) feeds the PEC (b), controlled by an industry standard microcontroller (c). The resistive part of the load ($R_L$) is implemented using power resistors (d), while the CPL part
Figure 3.14: Picture and diagram of the experimental set-up implemented to test the proposed EZD method to measure the incremental behavior of the load. The power supply (a) feeds the PEC (b), controlled by an industry standard microcontroller (c). The resistive part of the load ($R_L$) is implemented using power resistors (d), while the CPL part is implemented using an electronic load (e).

is implemented using an electronic load (e). The parameters of the implemented PEC are shown in Table 3.3.

The platform’s $v_o$ and $i_o$ are presented in Fig. 3.15, the upper plots indicate the time domain signal including the reference. The injected perturbation is so small that it cannot be plainly seen in the signals given the switching ripple. The panel to the right shows a zoom of the measured signals. The lower plots show the FFT of $v_o$ until the first components of the switching ripple (removing the DC component). The injected perturbation is shown in
Table 3.3: Experimental Set-Up Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_b$</td>
<td>2.108 mH</td>
</tr>
<tr>
<td>$C_b$</td>
<td>4.75 μF</td>
</tr>
<tr>
<td>$f_o$</td>
<td>1.5 kHz</td>
</tr>
<tr>
<td>$Z_o$</td>
<td>21 Ω</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>10 kHz</td>
</tr>
<tr>
<td>$f_s$</td>
<td>40 kHz</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>24 V</td>
</tr>
<tr>
<td>$V_o$</td>
<td>12 V</td>
</tr>
<tr>
<td>$f_r$</td>
<td>250 Hz</td>
</tr>
<tr>
<td>$M$</td>
<td>40</td>
</tr>
<tr>
<td>$A_r$</td>
<td>0.1%</td>
</tr>
</tbody>
</table>

Figure 3.15: Experimental noise immunity test in steady-state; the upper traces ($v_o$ and $i_o$) show that the advantageous small perturbation signal cannot be seen in the time domain (switching ripple dominates in the zoomed signals); the lower FFT plots depicts how small the perturbation signal is compared to the switching ripple.

The experimental capture of the EZD and the outputs are presented in Fig. 3.16 for three different loading conditions. The results of the proposed EZD method are outputted via a Digital to Analog Converter (DAC) and scaled correspondingly with the Oscilloscope. In
Table 3.4: Experimental Measurements

<table>
<thead>
<tr>
<th>Figure</th>
<th>Load Configuration</th>
<th>Calculated Value</th>
<th>EZD Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$R_L$ [Ω]</td>
<td>CPL [W]</td>
<td>$g_{CPL}$ [Ω⁻¹]</td>
</tr>
<tr>
<td>3.16(a)</td>
<td>24</td>
<td>0</td>
<td>$\infty$</td>
</tr>
<tr>
<td>3.16(b)</td>
<td>24</td>
<td>5</td>
<td>$-0.0347$</td>
</tr>
<tr>
<td>3.16(c)</td>
<td>24</td>
<td>10</td>
<td>$-0.069$</td>
</tr>
</tbody>
</table>

Fig. 3.16(a) the load is purely resistive and therefore, $g_e$ matches the load resistance. In Fig. 3.16(b) a CPL of 5 W is added; $g_{eq,L}$ becomes larger. However, $g_e$ remains positive, since the contribution of the CPL is not enough to change the sign; this is appropriately reflected in the output of the algorithm. Finally, in Fig. 3.16(c) another 5 W of CPL are added, making the influence of the CPL larger than that of $R_L$. The output of the instrument reflects this by changing the phase to $\pi$.

A summary of the experimental cases, as well as the measured result, can be found in Table 3.4. The maximum error found in the measurement is below 5%. Table 3.4 compares the results obtained from measuring $g_e$ from (3.14) with the output of the proposed EZD method. The accuracy of the proposed technique for a given size of the perturbation presents evidence of the excellent characteristic features of the technique, allowing accurate estimation with low distortion injected. Increasing the size of the perturbation can increase the accuracy or relax the requirements on the buffer size.

3.5 Comparison Against Other Equivalent Load Detection Techniques

In the previous sections, the proposed EZD based load detection method was introduced, and simulation and experimental results showing the behavior of the algorithm were presented. In this section, a comparison of the proposed technique with existing load impedance detection
Figure 3.16: Experimental captures of the outputs of the impedance measurement algorithm for different load conditions; in (a) with a 24 Ω resistive load, in (b) a parallel connection of 5W CPL is added, and in (c) the CPL part is increased to 10W.
Table 3.5: Comparison of the Proposed Technique with Existing Methods Reported in the Literature

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Perturbation Type</th>
<th>Amplitude</th>
<th>Frequency ( (f_r) )</th>
<th>Convergence time [step]</th>
<th>Operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>EZD-Based*</td>
<td>( \sin -d(t) )</td>
<td>0.1%</td>
<td>High‡</td>
<td>( N_p/f_r )</td>
<td>+, \times, /, table</td>
</tr>
<tr>
<td>Kalman Filter (KF)†</td>
<td>square-( i(t) )</td>
<td>25%</td>
<td>Low‡</td>
<td>( 1/2f_r )</td>
<td>+, ( AB, A^{-1} )</td>
</tr>
<tr>
<td>Recursive Least Square (RLS)†</td>
<td>square-( i(t) )</td>
<td>25%</td>
<td>Low‡</td>
<td>( 1/2f_r )</td>
<td>+, ( AB, A^{-1} )</td>
</tr>
</tbody>
</table>

* Implementation is performed in a microcontroller, trigonometric functions are implemented with tables.
† Implementation was performed in a Core-i5 computer, with a real time simulator; each iteration of the KF or RLS takes about 50\( \mu \)s.
‡ In this case, the low or high frequency is compared to the bandwidth of the controller, in the LIA, the perturbation is faster than the loop, in the KF and RLS it is much slower.

techniques is presented. These are compared using some of the critical indicators of the algorithm’s performance: the type and amplitude of the perturbation, the computational cost (as indicated by the type of operations required), and the convergence time. Two algorithms are presented for comparison, both of which are based on the Kalman Filter. Other impedance estimation algorithms exist, but they are not implemented for DC systems and have to operate within the utility frequency (60 – 50 Hz), which makes them fundamentally different.

The comparison of the main parameters is presented in Table 3.5 for the RLS and the KF. Several main differences can be outlined: the injected perturbation (reported in the experimental results) indicates that the technique uses a large slow perturbation to estimate the impedance; this perturbation is later removed, which is an advantage. The quick and small perturbation introduced by the LIA provides the benefit of continuous estimation with minimal interference in the system. Moreover, the computations required to use the LIA

76
are simple recursive additions (using a circular buffer) and some trigonometric calculations, which can all be implemented efficiently using tables. Both the Kalman Filter and the RLS implementations require the inversion of a matrix, as well as several more computations; for this reason, the computations take much longer even when implemented in a desktop-grade microprocessor (about 50 µs). The computations for the LIA-based method take less than 12 µs. The KF and RLS methods do offer one advantage compared to the LIA-Based method: they converge faster, relative to the frequency of the perturbation (1/2\(f_r\)). This is compensated by the faster perturbation and reduced computational cost offered by the LIA-Based algorithm.

### 3.6 Summary

In this chapter, the use of the Embedded Impedance Detection (EZD) method, built into a Power Electronics Converter (PEC), operating in a DC network was proposed as a way to improve the transient performance and the stability of the system. The PEC feeds several loads of different types and magnitudes, and its stability and dynamic behavior depend on the incremental load, rather than the total load. Constant Power Loads (CPLs) present an especially challenging problem since their dynamic behavior has an inherent negative incremental resistance that leads to instability. The proposed EZD method was used to produce an adaptive control scheme that keeps the transient behavior of the PEC predictable under load change conditions.

The proposed technique offers several key benefits: a) real-time detection of the equivalent incremental load, seen from the PEC, with minimal signal injection; b) transient performance improvement for different types of load; and c) extension of the stable operation region without compromising performance in other conditions. The information extracted through
the EZD method allows the real-time adjustment of the controller coefficients in order to obtain a reliable response under load change conditions.

Simulations have been carried out to show the ability of the proposed technique to extract the incremental behavior of the load, not only when it is either purely resistive or purely CPL, but also when it is of mixed nature. Moreover, the integration of this instrument to adapt the controller was presented, and compared against a standard PI controller tuned for specific cases.

Experimental results using a power platform as well as a standard microcontroller were presented, showing the accuracy of the proposed technique. The experimental validations show the power of the technique to detect a perturbation much smaller than the switching ripple.

Finally, a comparison of the proposed technique with other impedance estimation methods for stability was introduced, comparing the advantages and disadvantages of the proposed technique. The proposed technique, although narrower in its application, can be implemented in real-time in a standard microcontroller, as opposed to other techniques that are powerful but too demanding to implement in real time using small microcontrollers.
Chapter 4

Islanding Detection and Autonomous Operation for DC Systems

Figure 4.1(a) presents a block diagram of a DC microgrid with an AC interface. In this microgrid, the grid interface Power Electronics Converter (PEC) is in charge of the regulation of the bus voltage; if it disconnects, the other PECs need to detect this islanding event and either disconnect or change controllers to support the grid voltage. Fast and accurate islanding detection (ID) is critical to ensure the system disconnects or transitions to the islanding operation mode. This is especially challenging in DC systems since some of the variables typically used to differentiate the islanding event (such as phase and frequency) are not present in DC. Impedance-based methods exist for AC systems and provide minimal Non-Detection Zones (NDZ), so the proposed Embedded Impedance Detection (EZD) method can be suitable for this application.

In this chapter, a novel active ID Method (IDM) for DC systems, based on the EZD, is presented. Figure 4.1(b) presents a general diagram of the proposed technique, comparing a traditional Over-Voltage/Under-Voltage (OV/UV) IDM to the proposed impedance-based IDM. The proposed IDM provides three key benefits: virtually zero NDZ for all types of

Portions of this chapter have been published in

Figure 4.1: In (a) a block diagram of the DC system feeding a composite load from a grid interface PEC and other source PECs, when the grid interface disconnects, the source-end PEC has to detect this condition and take over regulation of the bus; in (b) behavior of the proposed EZD-based islanding detection method (IDM) against a traditional Over-Voltage/Under-Voltage (OV/UV) detection method for an islanding event with a closely matched source and load, a load change, and a grid re-connection; the OV/UV method is not able to detect the event under very closely matched conditions and does not detect a re-connection; the proposed method is based on incremental impedance, and therefore offers: no NDZ ➊, small perturbation ➋, fast detection ➌, and the ability to detect both islanding and non-islanding conditions; paired with a simple controller, it provides smooth transition between autonomous and following behavior.

loads ➊; the injected signal is 1\% of the duty-cycle, given the sensitivity of the Lock-In Amplifier (LIA), produces a Total Harmonic Distortion (THD) of 1.4% ➋; converges in less than 20 ms ➌; and the ability to detect both islanding events (grid disconnection) and grid re-connection events ➍. This allows the system to transition between Grid Tie Mode (GTM) and Islanded Mode (IM) without powering down, communications links, or leaving the bus unregulated, contributing to increase the reliability and the quality of service.

The proposed method is studied for a challenging scenario, where the DGs are producing the same power that the load is consuming (causing voltage and current not to change during the islanding event), both including and not including line impedances. Moreover, different
types of loads are included in the analysis to validate the accuracy of both active and passive loads. A simple bumpless controller to regulate the operation in GTM and IM is included. Simulations of the proposed algorithm, as well as a standard passive method, are included to illustrate the proposed algorithm. Experimental results further validate the proposed method. A general comparison against other algorithms is included to measure the virtues and limitations of the proposed method.

4.1 System Model

This section presents a general outline of the system when the grid is connected and in islanding mode. Figure 4.1(a) shows the block diagram of the DC microgrid. The grid forming PEC, connected to the utility AC distribution grid regulates the bus voltage, while the distributed generators (DGs) inject power to the system following their guidelines (such as maximum power point tracking, battery charging profile). The total load is a composition of several types of load. The constant resistance loads (CRLs, such as heating) show a passive behavior; active loads, on the other hand, can show different behaviors such as constant power loads (CPLs) or constant current loads (CCL).

During an islanding event, the switch $S_b$ disconnects and the bus is not regulated anymore. The control algorithm in the DGs can be switched over to one that can regulate the bus voltage, instead of other rules.

The following subsections cover the building blocks for the proposed method, along with a traditional IDM. It presents the operation of the PEC in its DC equilibrium state and the DC and incremental behavior of the loads and its composition. The section outlines a simple controller that can operate in both IM and GTM, with the ability to move in between them smoothly, and switch between modes following the ID signal.
Figure 4.2: Incremental model of the microgrid, as seen by the source-end power electronics converter in (a) Grid Tied Mode (GTM) and (b) islanded mode.

### 4.1.1 DC System Model

Figure 4.2(a) shows a model of the system when the grid is connected ($S_b$ is closed). The source-end PEC is modeled as a current source with a parallel capacitor, modeling the inner current loop of the PEC. The $Z_1$ and $Z_2$ model the losses of the wires connecting the load and the grid-forming PEC. The grid forming PEC is considered an ideal voltage source. The $R_e$ represents the fraction of the composite load that is fed by the PEC under analysis.

When the PEC is not islanded, the average output voltage ($V_{o,ni}$) is given by

$$V_{o,ni} = \left( R_1 + \frac{R_e R_2}{R_e + R_2} \right) I_s + \left( \frac{R_e}{R_e + R_2} \right) V_{dc}, \quad (4.1)$$

where $I_s = I_o$ (the ripples are absorbed by the capacitor). In this condition, the resistance ($R_{ni}$) seen from the terminals of the source-end PEC is

$$R_{ni} = \frac{V_{o,ni}}{I_o} = \left( R_1 + \frac{R_e R_2}{R_e + R_2} \right) + \left( \frac{R_e}{R_e + R_2} \right) \frac{V_{dc}}{I_s}, \quad (4.2)$$

a superposition of the load components, the line, and the influence of the grid forming PEC. Since $R_1$ and $R_2$ are relatively small, $V_{o,ni}$ is approximately

$$V_{o,ni} \approx V_{dc}, \quad (4.3)$$

which does not depend on the load condition.
Figure 4.2(b) shows the same system under the islanded condition. In this case,

\[ V_{o,i} = (R_1 + R_e)I_s \approx I_s R_e, \]  

and the resistance seen from the source-end PEC in islanded mode \((R_i)\) is

\[ R_i = \frac{V_{o,i}}{I_{o,i}} = R_1 + R_e \approx R_e. \]  

The \(R_i\) clearly depends on the load condition.

This difference in DC resistance could be enough to differentiate between the islanded and the non-islanded condition in many cases, but lacks the ability to detect when the load closely matches the source. In this case, since the source-end PEC was initially supplying the load, the difference is minimal. The difference is affected by unknowns, such as \(R_1\) and \(R_2\).

### 4.1.2 Composite Load Model

Loads can come in different forms and combinations. The simplest is a Constant Resistance Load (CRL), in which Ohm’s Law gives the \(V - I\) relationship. Active loads come in the form of CCL, where the current is independent of the voltage applied, and Constant Power Loads, where \(i = P/v\). Ideal CCLs have infinite parallel resistance, while ideal CPLs have infinite bandwidth. A diagram of these kinds of loads, along with their \(V - I\) curves, is presented in Fig. 4.3. Although the DC resistance \((R_e = V_{\text{load}}/I_{\text{load}})\) is the same for all the cases, the incremental resistance \((r_e = dv/di)\) is different. The CCLs have an infinite \(r_e\), while CPLs present an inherent negative resistance \((dv/di < 0)\).
The resistive load that draws $P_{CRL}$ is given by

$$R_L = \frac{V_L^2}{P_{CRL}},$$

(4.6)

where $V_L$ is the voltage in the load. The incremental behavior is given by

$$r_{CRL} = \frac{dv_{CRL}}{di_{CRL}} = R_L.$$

(4.7)

For a CCL, that draws $P_{CCL}$, the incremental behavior is given by

$$r_{CCL} = \frac{dv_{CCL}}{di_{CCL}} = \infty.$$

(4.8)

Finally, for a CPL, the incremental behavior for a load of $P_{CPL}$ is given by

$$r_{CPL} = \frac{dv_{CPL}}{di_{CPL}} = -\frac{V_L^2}{P_{CRL}}.$$

(4.9)
For a composite load (i.e. a load that is part CRL, part CPL, part CCL), and that draws $P_L$ given by
\[ P_L = P_{CRL} + P_{CPL} + P_{CCL}, \] (4.10)
the incremental behavior depends on the combination of loads. The state of load ($p_L$) of the PEC is defined by the ratio between $P_L$ and the rated load ($P_N$)
\[ p_L = \frac{P_L}{P_N} = \frac{1}{P_N} (P_{CRL} + P_{CPL} + P_{CCL}). \] (4.11)
Moreover, it is possible to analyze the load combination by analyzing the fraction of the load that is of each kind. The normalized load ($p_L$) represents the total load in relationship to the nominal load of the converter and is given by
\[ p_L = \frac{P_L}{P_N} = \frac{P_L}{P_N} \left( \frac{P_{CRL}}{P_L} + \frac{P_{CPL}}{P_L} + \frac{P_{CCL}}{P_L} \right). \] (4.12)
The $r_e$ is given by the parallel connection of all the types of load, then
\[ r_e = \left( \frac{1}{r_{CRL}} + \frac{1}{r_{CCL}} + \frac{1}{r_{CPL}} \right)^{-1}. \] (4.13)
Plugging in (4.6), (4.7), (4.8), and (4.9), the $r_e$ is given by
\[ r_e = \left( \frac{P_{CRL}}{V_L^2} + \frac{1}{\infty} - \frac{P_{CPL}}{V_L^2} \right)^{-1}, \] (4.14)
\[ = \left( \frac{P_{CRL}}{V_L^2} - \frac{P_{CPL}}{V_L^2} \right)^{-1}, \] (4.15)
\[ = V_L^2 (P_{CRL} - P_{CPL})^{-1}. \] (4.16)
Using (4.10) in (4.16)

\[ r_e = V_L^2 (P_L - P_{CCL} - 2P_{CPL})^{-1}, \]  
\( (4.17) \)

\[ = \frac{V_L^2}{P_L} \left( 1 - \frac{P_{CCL}}{P_L} - 2 \frac{P_{CPL}}{P_L} \right)^{-1} \]  
\( (4.18) \)

By multiplying and dividing by \( P_N \), the \( r_e \) can be expressed as

\[ r_e = R_N \frac{1}{P_L} \left( 1 - \frac{P_{CCL}}{P_L} - 2 \frac{P_{CPL}}{P_L} \right)^{-1} \]  
\( (4.19) \)

where \( R_N \) is the nominal load resistance

\[ R_N = \frac{V_L^2}{P_N}. \]  
\( (4.20) \)

From (4.19) it can be observed that \( r_e \) can be lower than zero, but its absolute value is always greater than \( R_N \).

Figure 4.4(a) shows the normalized \( r_e \) (i.e. \( r_{e,n} = r_e/R_N \)) for a mix of CPL and CRL \((P_{CCL} = 0)\). The plot shows all the combinations of loads, including different \( p_L \) and different \( P_{CPL}/P_L \). For a fraction of CPL lower than 50%, the \( r_e \) is positive, while for higher than 50%, \( r_e \) is negative. However, this transition passes through an asymptote, without crossing 1 or 0.

Figure 4.4(b) shows the same plot for a CCL with CRL. The plot shows all the combinations of loads, including different \( p_L \) and different \( P_{CCL}/P_L \). As the portion of CCL increases, the \( r_e \) increases, and for very light load condition, the \( r_e \) also increases.
Figure 4.4: Normalized incremental resistance \( (r_{e,n}) \) for a composite load that is part resistance and in (a) part CPL and in (b) part CCL, as a function of the load state \( (P_L/P_N) \) and the fraction of active load; \( |r_e| > 1 \) for all conditions.

### 4.1.3 Bumpless Controller Mode Change

The control of the distributed generators can follow two alternative modes: grid-tie or island; switching over between them depends on the IDM. Figure 4.5 shows a block diagram of the proposed controller. In GTM, the current reference \( (I_s^*) \) of the inner loop can come from different strategies, such as the maximum power point tracking (MPPT) algorithm or the battery management system. Since \( v_o \) is being regulated by the grid forming PEC, there the voltage variation is only due to small line resistance.

In IM, the PEC should regulate \( v_o \). This regulation can take several forms: in a master-slave setting, the energy storage could take the lead to regulate \( v_o \) after the grid connection is lost, while other DGs keep working in GTM; in a current share setting, a droop law is implemented to share regulation among the PECs.

The controller in Fig. 4.5 is a simple PI controller, given by

\[
  u_c = K_p \left( e_v + \int \left( K_i e_v + K_w e_n + K_t e_i^* \right) dt \right),
\]

(4.21)
Figure 4.5: Proposed controller for the source Power Electronics Converter (PEC); in GTM, the PEC operates in current source mode, and its reference comes from the local controller; in islanded mode the controller follows a voltage reference \( V^* \) using a PI controller \( (K_p, K_i) \), the controller includes an anti-windup method \( (K_w) \) and an output tracker \( (K_t) \) to allow for a bumpless transition between modes; the IDM allows switching between modes.

where \( K_p \) and \( K_i \) are the PI constants. The controller includes two amendments to account for non-ideal conditions: control signal saturation with anti-windup, and control signal tracking. The saturation is given by

\[
    u_s = \begin{cases} 
        u_c & \text{if } I_{\text{min}} \leq u_c \leq I_{\text{max}}, \\
        I_{\text{max}} & \text{if } u_c > I_{\text{max}}, \\
        I_{\text{min}} & \text{if } u_c < I_{\text{min}}, 
    \end{cases} \quad (4.22)
\]

where \( I_{\text{max}} \) and \( I_{\text{min}} \) are the limits of the PEC output. Then, \( e_u \) is drawn to zero by the integral controller with a gain of \( K_w \), ensuring the integrator does not extend beyond the saturation limit.

To allow for a smooth transition between the GTM and IM, the IM controller needs to have the same output as the GTM controller when in GTM mode. This tracking is achieved by incorporating a feedback of the actual control signal and the decision of the IM controller \( (e_{i_2}) \), adjusted by the tracking gain \( (K_t) \). Using these adjustments, the controller can switch between modes smoothly. A similar tracking mechanism is implemented for the GTM.
In the master-slave case, the voltage set-point of the IM output voltage set-point \((V_o^*)\) is

\[
V_o^* = V_{set},
\]

(4.23)

where \(V_{set}\) is the rated bus voltage. In the current sharing mode, \(V_o^*\) is given by the droop law

\[
V_o^* = V_{set} - R_d i_o,
\]

(4.24)

where \(R_d\) is the droop gain. In this chapter, the controller implemented uses a droop law, but the results are the same for a master-slave setting. Although the controller might be the same, the criteria used to switch between modes can make a difference in the system behavior, and traditional modes do not always do a good job.

4.1.4 Traditional Islanding Detection Method

This section presents a traditional IDM as a reference. The method is based on the under-voltage/over-voltage (UV/OV) method. Figure 4.6(a) shows a block diagram of the proposed method. The algorithm compares \(v_o\) with the reference set-point and creates a detection zone (DZ, usually \(\pm 5\%\)) where \(v_o\) is allowed to vary and still be considered as non-islanded. The main advantage of the UV/OV voltage is its simplicity and passive nature, which allows it not to distort the operation of the system at all.

A time diagram of the traditional method is presented in Fig. 4.6(b). When the grid is connected, as per (4.3) \(V_o\) is close to the grid voltage, independently from the load. During an islanding event, the \(V_o\) is given by (4.4). If the load and source are different (e.g., if the source is supplying 10 A and the load takes 15 A) \(V_{o,ni}\) is very different from \(V_{o,i}\) and the traditional method can detect the change. However, if the load is closely matched with the source (e.g., if the source is supplying 10 A and the load takes 9.9 A) \(V_{o,ni}\) is very similar from \(V_{o,i}\) and the
Figure 4.6: In (a) a block diagram of a simple under-voltage/over-voltage (UV/OV) IDM; in (b) a timing diagram of the outputs of the UV/OV method, the output voltage ($v_o$) changes after the islanding event, as the load takes less power, however, depending on how closely matched the load and source are, this can go unnoticed; if the islanding event is triggered, the method is not good to detect the reconnection.

The UV/OV method is aimed to disconnect the PEC from the grid under the islanding event; therefore, the reconnection criteria is given by $V_o$ returning to the safe zone. If the system is configured to change the mode to a grid forming mode, then the voltage is always in the range; therefore the UV/OV method is not able to detect the grid reconnection in this scenario.
4.2 Proposed Islanding Detection Method

The proposed Incremental-Impedance Based IDM is based on two key elements: using the proposed EZD method to measure $r_e$, and defining a band of values for each operation mode. The simple block diagram of the proposed method is shown in Fig. 4.7.
When the proposed EZD method is used to inject a reference in the current set-point \( (i_s^*) \), it causes a small variation to appear in all the variables

\[
i_s = I_s + \tilde{i}_s, \quad (4.25)
\]
\[
i_o = I_o + \tilde{i}_o, \quad (4.26)
\]
\[
v_o = V_o + \tilde{v}_o, \quad (4.27)
\]
\[
v_{dc} = V_{dc} + \tilde{v}_{dc}. \quad (4.28)
\]

In non-islanded mode, \( \tilde{v}_o \) is then given by

\[
\tilde{v}_{o,ni} = \left( R_1 + \frac{r_e R_2}{r_e + R_2} \right) \tilde{i}_o + \left( \frac{r_e}{r_e + R_2} \right) \tilde{v}_{dc}. \quad (4.29)
\]

Therefore the incremental resistance seen by the PEC in non-islanded mode is given by

\[
r_{ni} = \frac{\tilde{v}_{o,ni}}{\tilde{i}_o} = \left( R_1 + \frac{r_e R_2}{r_e + R_2} \right) + \left( \frac{r_e}{r_e + R_2} \right) \frac{\tilde{v}_{dc}}{\tilde{i}_o}. \quad (4.30)
\]

In islanded mode, \( \tilde{v}_o \) is then given by

\[
\tilde{v}_{o,i} = (R_1 + r_e) \tilde{i}_o. \quad (4.31)
\]

Then, the incremental resistance seen by the PEC in islanded mode is given by

\[
r_i = \frac{\tilde{v}_{o,i}}{\tilde{i}_o} = (R_1 + r_e). \quad (4.32)
\]

It remains to be seen whether the use of these expressions creates a more sensitive ID criteria.

The behavior observed in Fig. 4.4, that illustrates the results in (4.19) shows an incremental behavior that is never lower than \( R_N \) (in absolute value). This can be used in combination
with (4.30) and (4.32), and with the consideration that $\tilde{v}_{dc}$ is very small, to obtain

$$r_{ni} = R_1 + R_2 \approx 0,$$

(4.33)

$$r_i = R_1 + r_e \approx r_e,$$

(4.34)

with $|r_e| > R_N$. This creates a significant gap between the system operation with and without the grid connection, even when considering the losses in the line, making it an effective method to detect the islanding conditions.

These two scenarios are identified using the EZD method presented in Chapter 2. The incremental resistance ($\hat{r}_{inc}$) is calculated using (2.55):

$$\hat{r}_{inc} = \frac{v_d i_d + v_q i_q}{i_d^2 + i_q^2}.$$  

(4.35)

This calculation allows accurate extraction of the $\hat{r}_{inc}$ with minimal reference injection.

Using the difference between $r_i$ and $r_{ni}$, the operating mode (OM) is given by

$$OM = \begin{cases} GTM & \text{if } |\hat{r}_{inc}| < R_N, \\ IM & \text{if } |\hat{r}_{inc}| \geq R_N. \end{cases}$$

(4.36)

This simple criteria allows for accurate detection of the islanding condition for any load (even exactly matched), regardless of the line resistances, and can detect the grid reconnection.

The reactive part of the measured incremental impedance ($\hat{x}_{inc}$) does not play a role in the IDM. However, it could interfere with the detection. The proposed algorithm allows detecting $\hat{x}_{inc}$ by using (2.56), and the results are shown in the simulations, showing that it does not interfere with the detection.
Table 4.1: Normalized Simulation Parameters for Islanding Detection

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Normalized Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{o,n}$</td>
<td>1</td>
</tr>
<tr>
<td>$L_{b,n}$</td>
<td>$1/2\pi$</td>
</tr>
<tr>
<td>$C_{b,n}$</td>
<td>$1/2\pi$</td>
</tr>
<tr>
<td>$Z_n$</td>
<td>$\sqrt{L_b/C_b} = 1$</td>
</tr>
<tr>
<td>$I_{o,n}$</td>
<td>$V_{o,n}/Z_{o,n} = 1$</td>
</tr>
<tr>
<td>$f_{o,n}$</td>
<td>$1/2\pi\sqrt{L_bC_b}$</td>
</tr>
<tr>
<td>$t_n$</td>
<td>$t \times f_{o,n}$</td>
</tr>
<tr>
<td>$v_{o,n}$</td>
<td>$v_o/V_o^*$</td>
</tr>
<tr>
<td>$i_{o,n}$</td>
<td>$i_o/I_o^*$</td>
</tr>
<tr>
<td>$R_{o,n}$</td>
<td>$R_o/Z_o$</td>
</tr>
</tbody>
</table>

Table 4.2: Simulation Load Cases Considering $R_{1,n} = R_{2,n} = 0.01$

<table>
<thead>
<tr>
<th>Type</th>
<th>$L_{\text{line},n}$</th>
<th>$R_{o,n}$</th>
<th>CPL</th>
<th>CPL BW</th>
<th>CCL</th>
<th>Trace</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>[%$Z_{o,n}$]</td>
<td>[]%$P_n$</td>
<td>$\times f_r$</td>
<td>Color</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRL</td>
<td>0</td>
<td>0.99</td>
<td>0</td>
<td>-</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0.99</td>
<td>0</td>
<td>-</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>CPL</td>
<td>0</td>
<td>1.38</td>
<td>25</td>
<td>200</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1.38</td>
<td>25</td>
<td>200</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1.38</td>
<td>25</td>
<td>20</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1.38</td>
<td>25</td>
<td>20</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>CCL</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>1</td>
<td>*</td>
</tr>
</tbody>
</table>

4.3 Simulation Results

This section presents the computer simulations of the proposed IDM for different types of loading conditions. The results are normalized with the parameters given in Table 4.1. Several loads are considered to evaluate the effect of different conditions on the efficacy of the detection. Table 4.2 presents the different scenarios and their trace color. For the simulations, the parameters of the LIA are $A_{r,n} = 0.01$, $f_{r,n} = 8$, $N_p = 1$. 

94
Figure 4.8 shows the simulation results for an islanding event. During the islanding event, given the close match between the source and load, there is a slight change in $v_{o,n}$. The $THD_i$ before the islanding event is lower than 1.4% and after the event is much lower than that. The lower two axes show the outputs of the EZD algorithm. During non-islanded operation, the EZD reports $r_{inc}$ equal to the sum of both line resistances ($R_1$ and $R_2$) while the values of $x_{inc}$ are equal to the line’s inductive part ($x_{line} = 2\pi f_r L_{line}$). After the islanding event, two things can be observed: 1) for all cases, the detected impedance is much larger than the non-islanded case and is distinguishable from the non-islanded mode; 2) limiting the bandwidth of the CPL results in a capacitive-like effect manifesting. In all cases, the gap between non-islanded and islanded is significant, allowing for a clear differentiation between both operating modes.

A magnification during the islanding transient is shown in Fig. 4.9. The type of load implemented affects the length of the transient in the LIA. Adding $L_{line}$ slows down the convergence by a small amount while adding the CPL increases the convergence time significantly. Moreover, if the CPL has a bandwidth that is close to the LIA’s frequency, the transient is significantly larger. In all cases, the proposed EZD method converges to a value that can be flagged as an islanding condition and allows the controller to implement the appropriate decision.

A different comparison of the simulation results can be seen in Fig. 4.10 for the steady-state outputs of the proposed EZD method before and after the islanding event. The results in Fig. 4.10 are presented in the impedance plane, showing how the simulation results never come inside the area defined by $r_{i,n} < 1$. An $r_{i,n} < 1$ would imply the PEC is overloaded, and this would trip the protections. Although some tolerance is allowed in $i_o$, it never brings $r_{i,n}$ close to $r_{ni,n}$. On the other hand, confusion could come from the losses in the line ($Z_1$), but there are not many applications in which losses are comparable to the load itself. This gives the EZD method a wide application range.
Figure 4.8: Simulation results of the proposed incremental impedance-based IDM in open loop (no control action) for different types of loads listed in Table 4.2 with a small line impedance; before the islanding event, the output voltage ($v_o$) is stiff and current ($i_o$) shows a larger oscillation (a low $\hat{r}_{inc}$), while after the islanding event, this is reverted; the proposed algorithm is able to separate the effect of the line inductance ($L_1$) and the bandwidth of the CPL and reliably detect the islanding event in all cases.

A final comment on the simulation scenarios: Table 4.2 lists a case with a CCL ($\ast$), but as expected an ideal CCL can not be implemented, so it was limited by the parallel resistor ($R_p$). Under these conditions, the output of the islanding detector yields $\hat{r}_{inc} = R_p$ (a very large number). This case is easy to detect due to the very large value of $R_p$ (tens of times
Figure 4.9: Detail of the simulation in Fig. 4.8 showing the transient behavior of the proposed detection method for the different loads; the type of load can extend the transient, but the worst-case puts the reliable detection well inside one time constant of the power electronics converter.

A simulation of the proposed system in closed-loop, using either the proposed impedance-based IDM or a traditional OV/UV method is presented in Fig. 4.11. The capture shows $v_o$ and $i_o$, as well as the operating mode the system is in. The controller is the same for both methods, only changing the criteria to switch between them. As can be seen, during the first
Figure 4.10: Simulation results of the proposed IDM for different loads in the impedance plane, normalized to the nominal load; for all loads, the detected impedance in non-islanded mode is 100 times or more smaller than the impedance in islanded mode, even including the line impedance; for the islanded mode, the impedance is higher than 1, even for limited bandwidth CPLs.

interval A, the PEC operates in GTM, reflected by the low oscillation in \( v_o \) (stiff voltage), the load is closely matched to the source. In B, the grid forming PEC is disconnected, while the OV/UV method does not detect the change due to the load falling in the NDZ, the proposed method quickly identifies the event and switches to IM. In C, the load changes causing the OV/UV to detect the condition and change mode; it is also noted that this transient does not cause a false detection with the proposed method. Finally, in D the grid forming PEC reconnects and the proposed method promptly identifies this condition and switches to GTM. The OV/UV method does not detect this. This is all achieved with a reference amplitude of 1% duty cycle.
Figure 4.11: Simulations of the proposed closed-loop system using the traditional OV/UV IDM and the proposed impedance-based method; the traditional method fails to detect the islanding event at first, and only does so after the load transient, while the proposed method smoothly transitions between modes quickly and accurately.

### 4.4 Experimental Results

The simulations in the previous section showed that the proposed EZD method can detect the connection and disconnection of the grid, i.e., the islanding events, clearly for a variety of loads and that this can be used to switch between a GTM regulator and an IM regulator. To further validate the use of the proposed algorithm, an experimental set-up was built with parameters that follow the proportions outlined in the normalization stage stage in Table 4.1, and the outputs of the proposed instruments were logged.

Figure 4.12 shows a diagram of the platform used to test the proposed method. The power supply feeds the PEC controlled by an industry-standard microcontroller. The load is implemented using a power resistor and an electronic load, while the grid forming PEC...
Figure 4.12: Diagram of the experimental set-up used for validating the proposed method. The power supply (a) feeds the PEC controlled by an industry-standard microcontroller (b). The load is implemented using a power resistor and an electronic load (c), while the grid forming PEC is implemented using a PEC (d) and source (e).

Table 4.3: Experimental Set-Up Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_b$</td>
<td>2.108 mH</td>
</tr>
<tr>
<td>$C_b$</td>
<td>4.75 μF</td>
</tr>
<tr>
<td>$f_o$</td>
<td>1.5 kHz</td>
</tr>
<tr>
<td>$Z_o$</td>
<td>21 Ω</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>10 kHz</td>
</tr>
<tr>
<td>$f_s$</td>
<td>40 kHz</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>30 V</td>
</tr>
<tr>
<td>$V_o$</td>
<td>24 V</td>
</tr>
<tr>
<td>$f_r$</td>
<td>5 kHz</td>
</tr>
<tr>
<td>$N_p$</td>
<td>4</td>
</tr>
<tr>
<td>$A_r$</td>
<td>1%</td>
</tr>
</tbody>
</table>

is implemented using a PEC (d) and source (e). The parameters of the implemented PEC are shown in Table 4.3.

The platform’s $v_o$ and $i_o$ are presented in Fig. 4.13, the upper plots indicate the time domain signal, including the reference. The injected perturbation cannot be seen in the
Figure 4.13: Experimental captures of the proposed incremental impedance-based IDM in open loop (no control action) for different types of loads listed: in (a) a resistive load and in (b) a mixed load part CPL and part resistance.

signals given the switching ripple. The lower plots show the outputs of the EZD algorithm through a DAC (and properly re-scaled). It can be seen that for different kinds of loads, the output of the sensor differentiates the GTM from the IM.
### Table 4.4: Comparison of the Proposed Technique with Existing Methods

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Perturbation</th>
<th>Amplitude ((f_r))</th>
<th>Frequency</th>
<th>Convergence time [step]</th>
<th>NDZ</th>
<th>ID/N-ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed method</td>
<td>sin (-i_s)</td>
<td>0.1%</td>
<td>High</td>
<td>(N_p/f_r)</td>
<td>none</td>
<td>yes</td>
</tr>
<tr>
<td>OV/UV</td>
<td>none</td>
<td>–</td>
<td>–</td>
<td>fast</td>
<td>large</td>
<td>no</td>
</tr>
<tr>
<td>Current Injection</td>
<td>(\Delta I_s)</td>
<td>large(^\dagger)</td>
<td>low</td>
<td>slow</td>
<td>(f(\Delta I_s))</td>
<td>no</td>
</tr>
<tr>
<td>Positive Feedback</td>
<td>(i_s) or (v_o)</td>
<td>large(^*)</td>
<td>–</td>
<td>medium</td>
<td>none</td>
<td>no(^\dagger)</td>
</tr>
</tbody>
</table>

\(^\dagger\) Perturbation is 0.1 to 0.9 of \(I_s\), and is periodically increased
\(^\dagger\) Can be used to detect the reconnection if the action when the islanding event is detected is to disconnect
\(^*\) there are several combinations that are grouped under this name

### 4.5 Comparison Against Other Islanding Detection Techniques

The previous sections introduced the proposed incremental impedance-based IDM and presented simulation and experimental results. The results were compared against a traditional IDM: the UV/OV method. However, many algorithms offer specific advantages and disadvantages. This section presents a comparison of the proposed technique against several other IDMs. These are compared using some of the critical indicators of the algorithm’s performance: the type and size of the perturbation, the convergence time, the NDZ, and the ability to detect a reconnection as well as an islanding event. Two other algorithms, the current injection and positive feedback, are presented for comparison.

Table 4.4 shows a comparison of several IDMs in the literature. Most methods are not designed to detect the reconnection of the grid if the system is switched to an islanding controller. The current injection method is a combination of the UV/OV method with a...
forced change in the set-point. If a change of 10% in the current set-point leads to a change in \( v_o \), a new step is injected that can trip the UV/OV scheme. This method can produce large perturbations in the regular operation of the system (±10% of the rated current during normal operation), leading to lower MPPT performance and large THD. The NDZ is proportional to the size of the perturbation.

The positive feedback method is another IDM that can be used in DC systems. The perturbation can be injected in several parts of the loop, and it is proportional to the observed deviation. In the event of islanding, this perturbation leads the system to unstable operation that trips the detection method. Since this method relies on forcing the system to operate in an unstable region, it requires careful design to ensure the instability is controlled.

Most of these methods are designed to disconnect the system in the event of an islanding condition. Therefore, they do not target reconnection in their specifications. If the system is disconnected, the OV/UV can be used to reconnect when \( v_o \) returns to the normal operating range; but it does not work to achieve smooth operation.

### 4.6 Summary

This chapter proposed the use of the Embedded Impedance Detection (EZD) method, built in a Power Electronics Converter (PEC), operating in a DC microgrid as an active islanding detection method (IDM). The PEC feeds a composite load, showing a mix of resistive (CRL), Constant Power (CPL), and Constant Current (CCL) parts. The proposed incremental impedance-based IDM can differentiate the GTM, where the incremental resistance is almost zero, from the IM where the incremental resistance is higher than the nominal load.

The proposed technique offers several key benefits: a) no NDZ due to the significant difference in the impedance, b) small perturbation, compared with other active methods, c) fast convergence, and d) the ability to detect both islanded and non-islanded scenarios.
The proposed technique is combined with a simple droop controller to allow for bumpless transition between modes, maintaining the DC system voltage during the whole process.

The proposed technique is limited to a case with a single, designated, converter to regulate the voltage in the event of an islanding condition. If more than one converter has such role, the interference of the other source converters in the same grid can present a challenge. If more than one converter injects the reference at the same frequency, these can interfere with each other; this can be addressed by selecting different frequencies for each converter, but require coordination in the installation. On the other hand, this problem can also be addressed by implementing complementary IDMs: while a leader converter injects the reference signal, a follower will work to cancel its own injection (presenting a high impedance at the reference’s frequency). This allows the leader to apply the proposed IDM and the follower to detect the islanding by the change in the cancellation signal, more research is needed to address this challenge.

Simulations were carried out to show the ability of the proposed technique to detect the islanding event. Many different mixed loads were analyzed; for all, the proposed method can detect the islanding event.

Experimental results using a power platform as well as a standard microcontroller were presented, showing the accuracy of the proposed technique. The experimental validations show the power of the EZD method to detect the islanding condition for different types of load.

Finally, it presented a comparison of the proposed technique with other IDMs (both active and passive), comparing the advantages and disadvantages of the proposed technique. The proposed technique is able to detect the islanding event with an injected signal of 1% of the nominal current, using an industry standard microcontroller and sensors.
Chapter 5

Low-Impedance Fault Location

Modern DC systems are pushed to increase their autonomy as generation is becoming more distributed. One feature that has the potential to be distributed in the system is a fault location mechanism for Low Impedance Faults (LIFs) after the Over-Current Protection (OCP) is activated. This mechanism would allow the power electronics converters (PECs) in the system to report the faulted connection and the distance to the fault to speed up repairs. Accurate knowledge of the faulted line can significantly reduce repair time and cost, by avoiding the use of dedicated hardware that needs to be move around to scan the grid looking for the fault.

New architectures for DC systems that allow for reconfiguration have been presented. Figure 5.1(a) presents a block diagram of a sample DC system with two sources feeding a resistive load. The system shows a LIF in the line connecting source 1 and 2. A ring-type microgrid can restore power to the healthy parts of the system (i.e., the parts to the left of source 1 and right of source 2) that are using DC switches. Moreover, this reconfiguration feature can be used to implement the LIF location method in the system, even for challenging configurations.

This chapter presents a method to measure the distance from a source-end PEC to a LIF. The proposed method uses the Embedded Impedance Detection (EZD) method introduced in

Portions of this chapter have been published in

this work to turn the source-end PEC into a Power Probe Unit (PPU) which in turn gathers the location of the fault. The system is analyzed showing the different possible locations of the fault relative to the load and the source-end PEC, and its impact on the accuracy of the method. The key benefits of the proposed technique are outlined in Fig. 5.1(b). The proposed
method benefits from the embedded nature of the algorithm, avoiding the need for external hardware ➊, the ability to use the reactive part of the impedance reduces the error due to the load ➋, the fast convergence of the method can quickly locate the LIF, returning the source-end PEC to feed the system ➌, and, in a reconfigurable system, the configurations that yield more error can be avoided by changing the configuration of the system ➍. Increasing the reference frequency allows the influence of the error to be reduced when the reactive part is included. The limitations of the technique are explored, and a solution for reconfigurable systems is proposed. The proposed method does not require high-speed communications.

Simulations of the proposed method in different configurations are included. The simulations show accurate measurements for beneficial configurations, as well as highlight the problematic situations. Further validation of the proposed technique is included with an experimental platform implemented with an industry-standard microcontroller and sensors.

5.1 System Model

This section presents a description of the system and the different possible locations of the LIF in relationship with the line and load. These configurations impact the effectiveness of the proposed technique and its modifications. The objective of the LIF location technique is to determine the distance to the LIF.

The characteristics of the system, the load, and the LIF affect the effectiveness of the LIF location estimation technique. In many applications, the load \( R_L \) is connected at the end of the wire coming from the load source, as shown in Fig. 5.2. The source-end PEC produces the output voltage and current \((v_o, i_o)\) for the load. In the event of a LIF, the \( v_o \) drops significantly; for active loads (such as constant power loads, constant current loads, and those loads with some start-up procedure), this causes the load to disconnect.
During normal operation, the value of $R_L$ can be

$$R_N \leq R_L \leq \infty,$$  \hspace{1cm} (5.1)

where $R_N$ is the nominal load of the PEC (lower $R_L$ trips the OCP). Any load with an $R_L$ lower than $R_N$ forces the source-end PEC to provide more than the maximum current.

The $R_f$ can also take different values. In the ideal LIF,

$$R_f = 0.$$  \hspace{1cm} (5.2)

In order for the fault to be a LIF, it needs to trip the OCP and therefore $R_f$ is

$$0 \leq R_f \leq R_N.$$  \hspace{1cm} (5.3)

In practice, it is not expected that $R_f$ takes a value close to $R_N$.

In the case outlined in Fig. 5.2, the LIF can only happen between the load and source. The line impedance between the source and load ($Z_{sL}$) is

$$Z_{sL} = d_{sL} (\rho + j\omega\lambda),$$  \hspace{1cm} (5.4)
where \( d_{sL} \) is the distance between source and load, \( \rho \) is the resistance per unit of distance, and \( \lambda \) is the inductance per unit of distance in the wire. When the LIF happens, the impedance of the wire between the source and the fault \((Z_{sf})\) is

\[
Z_{sf} = d_{sf} (\rho + j\omega \lambda), \tag{5.5}
\]

where \( d_{sf} \) is the distance from the source to the fault. Also, the impedance of the wire between the fault and load \((Z_{fL})\) is given by

\[
Z_{fL} = d_{fL} (\rho + j\omega \lambda), \tag{5.6}
\]

where \( d_{fL} \) is the distance from the fault to the load. As expected

\[
d_{sL} = d_{sf} + d_{fL}. \tag{5.7}
\]

In many DC systems, such as a ring DC microgrid there are multiple source-end PECs with lines feeding the loads. This allows reconfiguring the microgrid in the event of a LIF to re-energize the part that is not damaged. This is illustrated in Fig. 5.3, where several source-end PECs connected in a ring configuration through switches allow feeding either side of the ring or both. In the event of a LIF, the system identifies which line is faulted and reconfigures the system to stop powering only this segment. This configuration where the line extends between two source-end PECs leads to a situation where the LIF can be located further away from the source-end PEC performing the location algorithm, introducing new challenges.

This configuration presents different characteristics for the LIF location problem, as outlined in Fig. 5.4. This is especially challenging if the load is not smart enough to disconnect
in the event of a LIF. In the event of a LIF, part of the line and the load are in parallel, distorting the measurement of the distance.

Finally, if the system is reconfigurable, as indicated in Fig. 5.3, the location estimation can be made using the other end of the line. This is illustrated in Fig. 5.5; by closing switch 2 and opening switch 1, a LIF condition of the type shown in Fig. 5.4 can be modified to look like
5.2 Proposed LIF Location Method

A schematic of the proposed LIF location method is presented in the Fig. 5.6. The method uses the proposed EZD method to turn each of the PECs in the system into a PPU that can make an estimation estimation of the distance to the LIF. The EZD outputs two measure-
ments: the resistance \((r)\) and the reactive part \((x)\), given by (2.55) and (2.55)

\[
r = \frac{v_d i_d + v_q i_q}{i_d^2 + i_q^2}, \tag{5.8}
\]

\[
x = \frac{v_d i_d - v_d i_q}{i_d^2 + i_q^2}, \tag{5.9}
\]

Two estimations of the distance from the PEC to the LIF \((d_{sf})\) can be made from outputs of the EZD method

\[
\hat{d}_r = \frac{r}{\rho}, \tag{5.10}
\]

\[
\hat{d}_l = \frac{x}{2 \pi f_r \lambda}, \tag{5.11}
\]

where \(f_r\) is the frequency of the injected reference signal from the LIA. The relative error of each of the estimations is given by

\[
e_{d_r} = \left| \frac{\hat{d}_r - d_{sf}}{d_{sf}} \right|, \tag{5.12}
\]

\[
e_{d_l} = \left| \frac{\hat{d}_l - d_{sf}}{d_{sf}} \right|. \tag{5.13}
\]

This error depends on the relative location of the source, load, and LIF, as well as the values of these magnitudes.

### 5.2.1 LIF Before Load

This condition corresponds to that shown in Fig. 5.2, where \(d_{sf}\) is lower than \(d_{sL}\). In this case, the impedance measured by the source-end PEC using (5.8) and (5.8)

\[
z = r + jx = d_{sf} (\rho + j2\pi f_r \lambda) + \frac{1}{\frac{1}{R_f} + \frac{1}{R_L + d_{fL}(\rho + j2\pi f_r \lambda)}}. \tag{5.14}
\]
Considering that \( d_{sL} = d_{sf} + d_{fL} \), (5.14) can be written as

\[
z = r + jx = d_{sf} (\rho + j2\pi f r \lambda) + \frac{1}{\frac{1}{R_f} + \frac{1}{R_L+(d_{sL}-d_{sf})(\rho+j2\pi f r \lambda)}}. \tag{5.15}
\]

The estimation based on resistance is then given by

\[
\hat{d}_r = \frac{\text{re}(z)}{\rho} = d_{sf} + \frac{\text{re}\left(\frac{1}{\frac{1}{R_f} + \frac{1}{R_L+(d_{sL}-d_{sf})(\rho+j2\pi f r \lambda)}}\right)}{\rho}, \tag{5.16}
\]

and the estimation based on the reactive part is given by

\[
\hat{d}_l = \frac{\text{im}(z)}{2\pi f r \lambda} = d_{sf} + \frac{\text{im}\left(\frac{1}{\frac{1}{R_f} + \frac{1}{R_L+(d_{sL}-d_{sf})(\rho+j2\pi f r \lambda)}}\right)}{2\pi f r \lambda}. \tag{5.17}
\]

The second terms of (5.16) and (5.17) define the absolute error in the estimation of the values introduced by each method. Using (5.12) and (5.13), the relative errors for this configuration are are given by

\[
e_{d_r}|_{R_f=0} = \left| \frac{\text{re}\left(\frac{1}{\frac{1}{R_f} + \frac{1}{R_L+(d_{sL}-d_{sf})(\rho+j2\pi f r \lambda)}}\right)}{\rho d_{sf}} \right|, \tag{5.18}
\]

\[
e_{d_l}|_{R_f=0} = \left| \frac{\text{im}\left(\frac{1}{\frac{1}{R_f} + \frac{1}{R_L+(d_{sL}-d_{sf})(\rho+j2\pi f r \lambda)}}\right)}{2\pi f r \lambda d_{sf}} \right|. \tag{5.19}
\]

Some particular cases are of interest for the error evaluation:

- If \( R_f = 0 \) or very close, then both (5.18) and (5.19) yield zero error, as the term \( 1/R_f \) becomes infinity and nullifies the error. This makes intuitive sense, as a perfect short circuit would eliminate the effect of anything after the LIF in Fig. 5.2.
• If the load is smart enough to disconnect after the LIF ($R_L \to \infty$), then errors become

$$
\begin{align*}
  e_{dr}|_{R_L \to \infty} &= \left| \frac{\text{re} \left( R_f \right)}{\rho d_{sf}} \right|, \\
  e_{dl}|_{R_L \to \infty} &= \left| \frac{\text{im} \left( R_f \right)}{2\pi f_r \lambda d_{sf}} \right| = 0.
\end{align*}
$$

(5.20)

(5.21)

In this case, $e_{dr}$ depends only on $R_f$ and $d_{sf}$ (worse for LIFs that are closer to the source-end PEC), but $e_{dl}$ is always zero.

• If the estimation is performed using $f_r = 0$, that is, using the DC values instead of the LIA, there is no opportunity to measure $\hat{d}_l$ and $e_{dr}$ is given by

$$
\begin{align*}
  e_{dr}|_{f_r=0} &= \left| \frac{\text{re} \left( \frac{1}{R_f + R_L + (d_{sl} - d_{sf})\rho} \right)}{\rho d_{sf}} \right|, \\
&= \left| \frac{\text{re} \left( \frac{1}{R_f + R_L + (d_{sl} - d_{sf})\rho} \right)}{\rho d_{sf}} \right|,
\end{align*}
$$

(5.22)

which still depends on $R_f$, $R_L$, and $d_{sf}$.

• If the estimation is performed using a very high $f_r$ ($f_r \to \infty$), the errors are

$$
\begin{align*}
  e_{dr}|_{f_r \to \infty} &= \left| \frac{\text{re} \left( R_f \right)}{\rho d_{sf}} \right|, \\
  e_{dl}|_{f_r \to \infty} &= \left| \frac{\text{im} \left( R_f \right)}{2\pi f_r \lambda d_{sf}} \right| = 0.
\end{align*}
$$

(5.23)

(5.24)

After considering the particular cases, a more general expression of the error can be analyzed.

With no particular condition, $e_{dr}$ is given by

$$
\begin{align*}
  e_{dr} &= \frac{R_f}{\rho d_{sf}} \frac{(R_L + (d_{sl} - d_{sf})\rho)(R_f + R_L + (d_{sl} - d_{sf})\rho) + ((d_{sl} - d_{sf})2\pi f_r \lambda)^2}{(R_f + R_L + (d_{sl} - d_{sf})\rho)^2 + ((d_{sl} - d_{sf})2\pi f_r \lambda)^2}.
\end{align*}
$$

(5.25)

Since (5.25) has the term that depends on $f_r$ in the numerator and denominator in the same power, the expression levels off for higher frequencies. This means the error does not
significantly improve by increasing $f_r$. On the other hand, $e_{d_l}$ is given by

$$e_{d_l} = \frac{R_f^2(d_{sL} - d_{sf})}{d_{sf}((R_f + R_L + (d_{sL} - d_{sf})\rho)^2 + ((d_{sL} - d_{sf})^2 2\pi f_r \lambda)^2)},$$

(5.26)

which shows two main benefits: the error reduces with the square of $R_f$ (which is expected to be small), and it has $f_r^2$ only in the denominator. By increasing $f_r$, it is possible to improve the estimation of the measurement significantly.

### 5.2.2 Load Before LIF

This condition corresponds to that shown in Fig. 5.4, where $d_{sf}$ is greater than $d_{sL}$. In this case, the impedance measured by the source-end PEC using (5.8) and (5.8)

$$z = r + jx = d_{sL} (\rho + j2\pi f_r \lambda) + \frac{1}{\frac{1}{R_L} + \frac{1}{R_f + d_{fL}(\rho + j2\pi f_r \lambda)}}.$$  

(5.27)

The estimation based on the resistance yields

$$\hat{d}_r = \frac{\text{re}(z)}{\rho} = d_{sL} + \frac{\text{re}\left(\frac{1}{\frac{1}{R_L} + \frac{1}{R_f + d_{fL}(\rho + j2\pi f_r \lambda)}}\right)}{\rho},$$

(5.28)

and the estimation based on the reactive part is given by

$$\hat{d}_l = \frac{\text{im}(z)}{2\pi f_r \lambda} = d_{sL} + \frac{\text{im}\left(\frac{1}{\frac{1}{R_L} + \frac{1}{R_f + d_{fL}(\rho + j2\pi f_r \lambda)}}\right)}{2\pi f_r \lambda}.$$  

(5.29)

Equations (5.28) and (5.29) show that, unlike the case where the LIF is located before the load, the first term of each equation is not the correct distance ($d_{sf}$). If the load is smart enough to disconnect, then (5.28) and (5.29) return to (5.16) and (5.17) and the error is only
present in the \( \hat{d}_r \), and is proportional to \( R_f \). In other cases, the error is given by

\[
e_{dr} = \left| d_{sl} - d_{sf} + \frac{\text{re} \left( \frac{1}{R_L + R_f + d_{L}L(p + j2\pi f r \lambda)} \right)}{d_{sf}} \right|, \tag{5.30}
\]

\[
e_{dl} = \left| d_{sl} - d_{sf} + \frac{\text{im} \left( \frac{1}{R_L + R_f + d_{L}L(p + j2\pi f r \lambda)} \right)}{2\pi f r \lambda} \right|. \tag{5.31}
\]

Considering that \( d_{sf} = d_{sl} + d_{Lf} \), then the error is given by

\[
e_{dr} = \left| -d_{Lf} + \frac{\text{re} \left( \frac{1}{R_L + R_f + d_{L}L(p + j2\pi f r \lambda)} \right)}{d_{sf}} \right|, \tag{5.32}
\]

\[
e_{dl} = \left| -d_{Lf} + \frac{\text{im} \left( \frac{1}{R_L + R_f + d_{L}L(p + j2\pi f r \lambda)} \right)}{2\pi f r \lambda} \right|. \tag{5.33}
\]

These equations show that, when the LIF happens after the load, the error is not compensated by \( f_r \), even when \( R_f = 0 \). This is true for both the resistive and reactive estimations and presents a limitation to the method. However if the system has the ability to reconfigure and use the other PECs to probe, both directions can be tested and the LIF can be located by reducing the circuit in Fig. 5.4 to that of Fig. 5.2. The masking of the resistance is a common issue in many applications of LIF location, by making the LIF location algorithm a firmware update to the PECs in the system, moving the location equipment is avoided thereby reducing
the repair times and cost. Even when the error is increased for the condition where the load is located before the fault and the system is not reconfigurable, the proposed method still provides a better solution than looking through the whole line.

5.3 Simulation Results

In this section, computer simulations of the proposed LIF location method are presented to demonstrate the behavior of the proposed LIF location technique. The simulated circuit is presented in Fig. 5.7 in which the source-end PEC is modeled as a buck converter, normalized for generality, and the load is presented as a resistive load. The PEC is controlled using standard PI control methods with a current limit for the injection in LIF-location mode (low voltage). The simulations neglect the switching behavior for clarity. Three different LIF cases are simulated, related to the different scenarios discussed in the previous section, in order to validate the errors introduced and the capability of the system: 1) a short circuit LIF before the load, 2) a short circuit LIF after the load, and 3) a LIF with a larger $R_f$ after the load. In all these cases, it is assumed the load is not smart enough to disconnect from the system during the LIF because this is the worst case scenario.

The parameters of the circuit are presented in Table 5.1, in the normalized domain. The $\rho$ and $\lambda$ of the line are listed normalized and per meter. The reference signal is injected in the current control loop, as the converter is working current injection mode.

Figure 5.8 presents the simulation results for Case 1 (a short circuit at a short distance from the source). After the LIF, the location method injects current with the reference signal. The proposed EZD method outputs the resistive ($r_n$) and reactive ($x_n$) part, that, when combined with the configured parameters ($\rho$ and $\lambda$), allow estimating the distance accurately to the LIF ($d_{LIF}$). The two estimations are shown: the one calculated using the resistance ($d_r$), and the one calculated using the inductance ($d_I$). As can be seen, the results
Figure 5.7: Schematic of the simulated circuit; the load is connected in the middle of the line and is not disconnected after the Low Impedance Fault (LIF); three cases are presented at different distances and with a different LIF resistance ($R_f$).

Table 5.1: Simulation Circuit Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{b,n}$</td>
<td>1/2\pi</td>
</tr>
<tr>
<td>$L_{b,n}$</td>
<td>1/2\pi</td>
</tr>
<tr>
<td>$f_o = 1/\sqrt{LC}$</td>
<td>1</td>
</tr>
<tr>
<td>$Z_o = \sqrt{L/C}$</td>
<td>1</td>
</tr>
<tr>
<td>$V_{o,n}^*$</td>
<td>1</td>
</tr>
<tr>
<td>$D^*$</td>
<td>0.5</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>15</td>
</tr>
<tr>
<td>$R_{L,n}$</td>
<td>1</td>
</tr>
<tr>
<td>$I_{\text{max},n}^*$</td>
<td>2</td>
</tr>
<tr>
<td>$\rho$</td>
<td>$1e-5$</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>$1e-6$</td>
</tr>
<tr>
<td>$f_s$</td>
<td>$4f_{sw}$</td>
</tr>
<tr>
<td>$f_r$</td>
<td>$f_o/5$</td>
</tr>
</tbody>
</table>

show the accuracy of the method for this scenario. The accuracy of the measurement is related to zero $R_f$ and the fact that the LIF happens before the load.
Figure 5.8: Simulation results of the proposed LIF location method for a short circuit close to the source-end power electronics converter; the top plot shows the output voltage and current ($v_o$ and $i_o$), while the bottom two plots show the outputs of the Embedded Impedance Detection (EZD) method; after the Low Impedance Fault (LIF), both the resistive and reactive part provide accurate estimations of the distance.

The simulation results for Case 2 (a short circuit after the load) are presented in Fig. 5.9; in this case, the accuracy of the method is affected by the presence of the load in the path. Since the load is configured to remain connected, it introduces a parallel path (although a relatively high impedance one) for the scanning signal. Even including this, the low $R_f$ allows accurate measurement.

Finally, simulations for the Case 3 (a higher $R_f$ after the load) are presented in Fig. 5.10. The results of the estimation show that the error of the measurement is significant, as expected. This reflects the limitations of the method when the loads do not disconnect in the
Figure 5.9: Simulation results of the proposed LIF location method for a short circuit farther from to the source-end power electronics converter (after the load); the top plot shows the output voltage and current ($v_o$ and $i_o$), while the bottom two plots show the outputs of the Embedded Impedance Detection (EZD) method; after the Low Impedance Fault (LIF), as $R_f$ is very small, the estimation is suitable for both methods.

The measured values coincide with the expected results from the error equations. The most significant error is present when the load is located closer to the source than the LIF, as it was expected. This corresponds to the architecture limitations considered in the error analysis that can be overcome when the system is operated in a reconfigurable architecture.

event of a LIF. In practice, most loads in DC systems are active and disconnect in the event of a LIF, making the location more accurate.

Table 5.2 shows a summary of the results of the simulations. As can be observed, the location of the LIF with respect to the load has a significant impact on the accuracy of $d_{sf}$. The measured values coincide with the expected results from the error equations. The most significant error is present when the load is located closer to the source than the LIF, as it was expected. This corresponds to the architecture limitations considered in the error analysis that can be overcome when the system is operated in a reconfigurable architecture.
Figure 5.10: Simulation results of the proposed LIF location method for a short circuit farther from to the source-end power electronics converter (after the load) and with a higher resistance; the top plot shows the output voltage and current ($v_o$ and $i_o$), while the bottom two plots show the outputs of the Embedded Impedance Detection (EZD) method; after the Low Impedance Fault (LIF), the higher $R_f$ (20% of the nominal load) in combination with the load produce very inaccurate results.

Table 5.2: Simulation Results

<table>
<thead>
<tr>
<th></th>
<th>Case 1</th>
<th>Case 2</th>
<th>Case 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$d_{sf}$ [km]</td>
<td>10.0</td>
<td>30.0</td>
<td>40.0</td>
</tr>
<tr>
<td>$r_n$</td>
<td>0.100</td>
<td>0.302</td>
<td>0.508</td>
</tr>
<tr>
<td>$d_r$ [km]</td>
<td>10.0</td>
<td>30.2</td>
<td>50.8</td>
</tr>
<tr>
<td>$e_d$ [%]</td>
<td>0</td>
<td>0.66</td>
<td>27.00</td>
</tr>
<tr>
<td>$l_n$</td>
<td>0.0100</td>
<td>0.0282</td>
<td>0.0300</td>
</tr>
<tr>
<td>$d_l$ [km]</td>
<td>10</td>
<td>28.2</td>
<td>30.0</td>
</tr>
<tr>
<td>$e_d$ [%]</td>
<td>0</td>
<td>6.00</td>
<td>25.00</td>
</tr>
</tbody>
</table>
5.4 Experimental Results

The simulation results in the previous section showed how the proposed LIF location method could measure the distance to a LIF in different conditions. To further validate the proposed method, an experimental set-up was built with similar characteristics to the simulated system, and it was used to measure different impedances. These experimental results confirm the ability of the proposed EZD method to measure the low values are expected during the LIF, allowing the system to locate the LIF, using only the microcontroller and sensors built into the PEC and no additional hardware.

A picture and diagram of the experimental set-up is shown in Fig. 5.11. The power platform (a) is controlled by a standard C2000 microcontroller (b). The three LIF cases are implemented using the electronic load with three different channels (c), (d), and (e) in fault-test mode. The load of the system is (f). The $R_f$ is implemented using a lumped resistors (g). The inductances of the line are represented using lumped inductors of given values (i). The parameters of the implemented platform are given in Table 5.3.

The transient response of the different LIFs are presented in Figs. 5.12, 5.13, and 5.14 for each of the LIFs presented. Since the lumped elements in the network are not proportional to each other, it is not possible to determine an equivalent distance for the LIF. Instead, the results are analyzed based on the accuracy of the impedance measured, which would translate into the accuracy of the predicted distance. A summary of the experimental results and their error is presented in Table 5.4 when compared with the expected results. As can be seen, the error remains below 5% for all the cases.

As expected, the proposed method can use standard sensors to measure the impedance accurately. In a scenario where the wires were present, the outputs of the proposed system could be used to measure the distance to the LIF. The proposed method is still subject to the errors that come from the location of the LIF in relationship with the load and $R_f$. The
The proposed method helps locate the LIF using a standard controller for the PEC but can be subject to error in certain situations. If the system is can be reconfigured to the simple line topology, the LIF location accuracy is significantly improved compared with the ring architecture.
Table 5.3: Experimental Set-Up Configuration

(a) Converter Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_b$</td>
<td>4.75 $\mu$F</td>
</tr>
<tr>
<td>$L_b$</td>
<td>2.108 mH</td>
</tr>
<tr>
<td>$f_o = 1/\sqrt{LC}$</td>
<td>1.59 kHz</td>
</tr>
<tr>
<td>$Z_o = \sqrt{L/C}$</td>
<td>21.3</td>
</tr>
<tr>
<td>$V_o^*$</td>
<td>25</td>
</tr>
<tr>
<td>$D^*$</td>
<td>0.5</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>20 kHz</td>
</tr>
<tr>
<td>$R_L$</td>
<td>24</td>
</tr>
<tr>
<td>$f_s$</td>
<td>80 kHz</td>
</tr>
<tr>
<td>$f_r$</td>
<td>250 Hz</td>
</tr>
<tr>
<td>$N_p$</td>
<td>4</td>
</tr>
<tr>
<td>$A_r$</td>
<td>0.1$%$</td>
</tr>
</tbody>
</table>

(b) Line Segment Parameters

<table>
<thead>
<tr>
<th>Segment</th>
<th>Resistance [Ω]</th>
<th>Inductance [mH]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.089</td>
<td>4.26</td>
</tr>
<tr>
<td>2</td>
<td>0.260</td>
<td>2.57</td>
</tr>
<tr>
<td>3</td>
<td>0.111</td>
<td>2.0</td>
</tr>
<tr>
<td>4</td>
<td>0.080</td>
<td>1.36</td>
</tr>
</tbody>
</table>

(c) Fault Cases

<table>
<thead>
<tr>
<th>Case</th>
<th>Resistance [Ω]</th>
<th>Switch Resistance [mΩ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>−</td>
<td>17 (c)</td>
</tr>
<tr>
<td>2</td>
<td>−</td>
<td>17 (d)</td>
</tr>
<tr>
<td>3</td>
<td>5 (g)</td>
<td>80 (e)</td>
</tr>
</tbody>
</table>

Table 5.4: Experimental Results

<table>
<thead>
<tr>
<th>Case</th>
<th>Case 1</th>
<th>Case 2</th>
<th>Case 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$r_{calc}$</td>
<td>1.106</td>
<td>1.86</td>
<td>6.30</td>
</tr>
<tr>
<td>$x_{calc}$</td>
<td>6.69</td>
<td>13.79</td>
<td>14.22</td>
</tr>
<tr>
<td>$\hat{r}$</td>
<td>1.12</td>
<td>1.75</td>
<td>6.40</td>
</tr>
<tr>
<td>$\hat{x}$</td>
<td>6.98</td>
<td>14.15</td>
<td>14.5</td>
</tr>
<tr>
<td>$e_r[%]$</td>
<td>1.3</td>
<td>3.31</td>
<td>1.58</td>
</tr>
<tr>
<td>$e_x[%]$</td>
<td>4.3</td>
<td>2.61</td>
<td>1.97</td>
</tr>
</tbody>
</table>
\[ \text{fault} = 25 \text{ V} \]
\[ \text{o} \]
\[ \text{o} \]
\[ \text{o} \]
\[ \text{v} \]
\[ \text{o} \]
\[ \text{r} \]
\[ \text{=} \]
\[ 2 \text{ A} \]
\[ \text{x} \]
\[ 98 \Omega \].
\[ = \]
\[ 6 \]
\[ \times \]
\[ 12 \Omega \].
\[ = \]
\[ 1 \]
\[ r \]
\[ \hat{x} \]
\[ \hat{x} \]
\[ \hat{x} \]
\[ \hat{x} \]
\[ 85 \times 507 \]

Figure 5.12: Experimental capture for the transient during a Low Impedance Fault (LIF) in the location of Case 1. The estimated resistance is 1.1 Ω, and the reactance is 6.98 Ω.

\[ \text{fault} = 25 \text{ V} \]
\[ \text{o} \]
\[ \text{o} \]
\[ \text{o} \]
\[ \text{v} \]
\[ \text{o} \]
\[ \text{r} \]
\[ \text{=} \]
\[ 2 \text{ A} \]
\[ \text{x} \]
\[ 75 \Omega \].
\[ = \]
\[ 1 \]
\[ r \]
\[ 15 \Omega \].
\[ = \]
\[ 14 \]
\[ \times \]
\[ 15 \Omega \].
\[ = \]
\[ 1 \]
\[ r \]
\[ \hat{x} \]
\[ \hat{x} \]
\[ \hat{x} \]
\[ \hat{x} \]
\[ \hat{x} \]
\[ 85 \times 282 \]

Figure 5.13: Experimental capture for the transient during a Low Impedance Fault (LIF) in the location of Case 2. The estimated resistance is 1.75 Ω, and the reactance is 14.15 Ω.

5.5 Summary

In this chapter, a new implementation of the impedance-based Low Impedance Fault (LIF) location technique, using the proposed Embedded Impedance Detection (EZD) method for DC systems, was proposed. The analysis of the systems, as well as the possible locations of the different elements (source, load, and LIF), were presented. The impact of the different configurations in the error, as well as the parameters of the proposed method, were analyzed.
By using the proposed EZD method, it is possible to turn each source-end PECs into a power probe unit (PPU), instead of using external hardware.

The proposed LIF location method benefits from the high accuracy of the proposed EZD method and its ability to measure both the resistive and reactive part of the impedance, to accurately locate the LIF. From the error analysis, it is observed that using the reactive part of the line to estimate the distance is less sensitive to error when the LIF is located between source and load. When the LIF is located after the load, the error in the method can be reduced by using a reconfigurable architecture to allow the system to measure from the other direction.

The proposed method was validated through simulations, where the accuracy of the method in both resistive and reactive parts was presented. The simulation results reflect the predicted biases due to the load’s characteristics. The limitations of the method, namely related to the LIF resistance and the presence of passive loads that do not disconnect from the system were shown. The proposed method was further validated by experimental captures of several scenarios, showing the ability of the proposed algorithm to measure the fault impedance when implemented with a microcontroller and standard sensors.
Chapter 6

High-Impedance Fault Detection

High-Impedance Faults (HIFs) can be caused by many reasons and are hard to detect since they draw a small amount of current that does not trip the Over Current Protection (OCP). However, detecting them in time is crucial to avoid fires, damage to equipment, and possible harm to people. This task is challenging, and cannot always be achieved by a single algorithm, but for some particular cases, special techniques can be developed.

One such case is the Point-to-point architecture, like the one illustrated in Fig. 6.1(a), where a Power Electronics Converter (PEC) feeds a load that also has a PEC. A HIF in between the conductors (indicated by the red cross in the diagram) establishes a resistive connection between the conductors. This increases the output current without tripping the OCP.

This chapter presents an algorithm to detect HIFs between conductors in a point-to-point connection. The algorithm relies on the use of the proposed Embedded Impedance Detection (EZD) to measure the incremental resistance ($r_{inc}$) seen by the PEC. Based on the CPL nature of the load, its $r_{inc}$ decreases after a current increase, while a HIF is reflected in an increase in $r_{inc}$.

A diagram of the two different transients, a load step-up and a HIF, and the proposed technique is presented in Fig. 6.1(b). The proposed method uses the measurement of the

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Figure 6.1: In (a) a block diagram of a DC system feeding an electronic load through a line with a HIF; in (b) a comparison of the transient for a HIF (blue) as opposed to a load increase (orange): although the voltage and current \((v_o \text{ and } i_o)\) show no difference in steady-state (leading to no difference in \(R\)), the incremental resistance \((r_{inc})\) shows a clear difference by moving in the opposite direction.

output voltage and current \((v_o \text{ and } i_o)\) to determine \(r_{inc}\) as seen by the PEC. As opposed to the DC resistance \((V_o/I_o)\), which is the same for both events, detection based on \(r_{inc}\) using the proposed EZD offers three key benefits: high sensitivity, due to the qualitative difference between the fault and load \(r\) ➊, small reference injected ➋, fast detection while keeping the sampling frequency low ➌. Moreover, the proposed method is embedded in the PEC which adds the detection without additional hardware. The benefits and performance of the proposed HIF detection method are validated using simulations showing the comparison for closely matched cases. Experimental results, implemented in an industry-standard microcontroller, are provided to assess the performance of the proposed strategy and its feasibility.
6.1 System Model

Figure 6.1(a) presents the system under study. The system uses a point-to-point connection where the source-end PEC regulates the output voltage \( v_o \) that is sent through a wire to the load-end PEC. The load-end PEC regulates its output voltage to supply the load, causing a Constant Power Load (CPL) behavior. During a HIF, the fault resistance \( R_f \) is significant (higher than the nominal load), which causes the OCP not to trip in most conditions. The line connecting the source-end PEC with the load-end PEC can be considered to have losses, modeled with a resistance distributed through the line \( R_{\text{line}} \). In the event of a HIF in some part of the line, the \( R_{\text{line}} \) can be divided as

\[
R_{\text{line}} = R_{sf} + R_{fL},
\]  

where \( R_{sf} \) is the resistance from source-end PEC to a fault and \( R_{fL} \) is the resistance from fault to load-end PEC.

Fig. 6.2(a) shows a circuit schematic of the system for the DC operating point. For a CPL, the load current \( I_L \) is given by

\[
I_L = \frac{P_L}{V_L},
\]  

where \( P_L \) is the CPL power and \( V_L \) is the voltage at the terminals of the CPL. The incremental behavior of the CPL is given by

\[
r_L = -\frac{V_L^2}{P_L}.
\]  

This is the inherent negative resistance of a CPL. This incremental model is presented in Fig. 6.2(b).
Figure 6.2: In (a) the functional diagram of the system in its DC operating point, the DC resistance \((R_{\text{DC}})\) is the ratio of \(V_o\) and \(I_o\); in (b) the incremental behavior of the system under a small perturbation, the incremental resistance \(r_{\text{ac}}\) is \(\frac{\text{dv}_o}{\text{di}_o}\).

The equivalent load \((R)\), seen from the terminals of the source-end PEC, is

\[
R = \frac{V_o}{I_o},
\]

(6.4)

where \(V_o\) and \(I_o\) are the average \(v_o\) and \(i_o\). Both an increase in \(P_L\) and a HIF cause \(I_o\) to increase; the difference cannot be distinguished from \(R\). In other words: there is an increase in \(P_L\) that yields the same \(\Delta I_o\) as a HIF of a given \(R_f\); therefore, \(R\) cannot be used as an indicator of the HIF.

The incremental model shown in Fig. 6.2(b), the equivalent incremental resistance \((r_{\text{inc}})\) seen from the source-end PEC is given by

\[
r_{\text{inc}} = \frac{\text{dv}_o}{\text{di}_o} = R_{sf} + \frac{1}{R_f} + \frac{1}{R_{fl} + r_L}.
\]

(6.5)
Figure 6.3: Output current \( (I_o) \) as a function of the load power \( (P_L) \) under regular operation and during a fault; the DC resistance \( (R_{DC}) \) seen from the source is the same for both cases but the incremental resistance \( (r_{ac}) \) is different.

The measurement of \( r_{inc} \) shows different behavior for the transitions: for a HIF, \( R_f \) changes from infinity to a finite value (although a large one); for the load step-up, \( R_f \) remains at infinity, but the \( r_L \) becomes less negative.

Figure 6.3 shows \( I_o \) under normal operations as a function of \( P_L \) in orange, and depicts the curve, in a cyan trace, under a HIF of a given \( R_f \). The lower axis shows \( R \) in a solid line and \( r_{inc} \) in a dashed line for both cases. Two possible transitions are shown from \( A \) to \( B \) (load increases by \( \Delta P \)) and from \( A \) to \( C \) (HIF event). It can be seen that from measuring \( I_o, V_o, \) and \( R \) it is not possible to differentiate the two events. However, \( r_{inc} \) presents a completely different behavior: while \( r_{inc,B} > r_{inc,A}, \) \( r_{inc,A} < r_{inc,C} \).

The observed difference is sensitive to the value of the fault resistance \( (R_f) \): as \( R_f \) increases, it becomes harder to distinguish a HIF from the regular operation. This is expected since a HIF with very high impedance is indistinguishable from no change at all. The variation of the curves as a function of \( R_f \) is shown in Fig. 6.4.
Figure 6.4: Effect of a higher fault resistance ($R_f$) in the detected change; as $R_f$ increases, it becomes harder to distinguish the HIF from a load increment; for very high $R_f$ the difference is too small.

### 6.2 Proposed HIF Detection Method

The proposed HIF detection method is based on two key elements: using the proposed EZD method to measure the incremental behavior of the load, and defining a correlation between the increment in $i_o$ with a change in $r_{inc}$. The simple block diagram of the proposed method is shown in Fig. 6.5. As discussed in the previous section, it is possible to differentiate a load increment from a HIF by looking at $r_{inc}$. Given the constant nature of the DC system, this information is not readily available from $v_o$ and $i_o$ and needs to be inferred somehow.

The proposed method injects a reference signal to the duty cycle reference given by

$$d_r = A_r \sin (2\pi f_r T_s k),$$  \hspace{1cm} (6.6)
where \( T_s \) is the sampling rate of the LIA and EZD, and \( f_r \) is the reference frequency, \( A_r \) is the amplitude of the reference. The incremental variables are given by

\[
\begin{align*}
    i_o &= I_o + \tilde{i}_o, \\
    v_o &= V_o + \tilde{v}_o, \\
    i_L &= I_L + \tilde{i}_L, \\
    v_L &= V_L + \tilde{v}_L.
\end{align*}
\]

Using the LIA as discussed in Chapter 2 the incremental behavior of the system can be extracted.
Using EZD and the expression in (2.55), the \( r_{inc} \) measured from the terminals of the source-end PEC is given by

\[
r_{inc} = \frac{v_d i_d + v_q i_q}{i_d^2 + i_q^2},
\]

where \( v_{dq} \) and \( i_{iq} \) are the direct and quadrature components of the LIA implemented to perform EZD. The algorithm then computes the difference between \( r_{inc} \) between two steps of the algorithm given by

\[
\Delta r_{inc}[K] = r_{inc}[K] - r_{inc}[K - 1].
\]

It is important to note that \( K \) denotes the time-steps of the HIF detection algorithm, a sub-rate of \( T_s \). The time-step of the HIF detection algorithm has to be selected, considering that the system has reached a stable output, given that the transient can go through several values.

As some \( i_o \) circulates through \( R_f \), an increase in \( i_o \) is a requirement for a HIF to have happened. The change in \( i_o \) is calculated as

\[
\Delta I_o[K] = I_o[K] - I_o[K - 1],
\]

where \( I_o \) is calculated using a MAF tuned to \( f_r \), which removes the reference signal. The calculated \( \Delta I_o \) is reflected in the second condition in the diagram of Fig. 6.5: \( \Delta I_o > 0 \).

Using the extracted information, the HIF is determined to have occurred as

\[
F = \begin{cases} 
1 & \text{if } (\Delta r_{inc} > 0) \text{ and } (\Delta i_o > 0), \\
0 & \text{otherwise}. 
\end{cases}
\]
This simple criteria allows for accurate detection of the HIF, as long as the changes can be observed by the available sensors.

### 6.3 Simulation Results

The previous section presented the use of the EZD method to detect HIFs. The algorithm benefits from the efficient and accurate calculation of $r_{\text{inc}}$ implemented using the proposed EZD, as well as the nature of the load connected, to differentiate a HIF from a load step-up. This section introduces the validation of the proposed technique through computer simulations. The simulations are presented in the normalized domain, for generality, and correspond to two transients that yield the same DC operating point. In other words, the proposed simulations represent similar transitions to those outlined in Fig. 6.3, where $I_o$ and $V_o$ are the same for both transients. Using the EZD, the difference between the two transients is clear. The simulations neglect the switching ripple for clarity.

Figure 6.6 presents the transient when there is a load increase. The simulations show the output voltage ($v_o$) and load voltage ($v_L$) in the top plot. The second plot shows the output current ($i_o$) and the load current ($i_L$). Finally, the output of the EZD ($r_{\text{inc}}$) is presented along with the DC resistance $R$, calculated as the ratio of the average values of $v_o$ and $i_o$. During the load step-up, $i_o$ and $i_L$ remain the same, as there is no current that goes through a different loop (the parallel $R_f$ is very large). As expected from the calculations, the $\Delta r_{\text{inc}}$ is positive (the $r_{\text{inc}}$ becomes less negative) due to the increase in power from (6.3). This simulates a transition from point $A$ to $B$ in Fig. 6.3, where the system does not have a HIF. For the simulations, the transient in $r_{\text{inc}}$ takes only one period of $f_r$, as there is no need to average for noise.

Figure 6.7 shows the transient when there is a HIF. During the HIF, $i_o$ and $i_L$ are different: some of the current circulates through the HIF. As expected from the calculations, the $\Delta r_{\text{inc}}$
is negative (the $r_{inc}$ becomes more negative) due to the effect of $R_f$. This reflects a transition from point A to C in Fig. 6.3 that the EZD HIF detection method should identify as a HIF.

As can be observed, these transients, although they match precisely the DC behavior (having the same $R$) show a clear difference in $r_{inc}$. The simulation results show clearly the features of the proposed method: the difference in behavior between HIF and $\Delta P_L$ is qualitative ➊; the injected signal is small ➋; the convergence of the method is fast ➋. Moreover, the proposed method is built into the converter, allowing the detection of the fault without any additional hardware.
Figure 6.7: Simulations during a load step up; the current in the output and the load \( i_o \) and \( i_L \) are different, as some current circulates through the HIF; the \( r_{inc} \) reflects a decrease (more negative).

6.4 Experimental Results

The simulation results in the previous section show the ability of the proposed method to differentiate between a load increase and a HIF. This section presents further validation implemented using a real microcontroller. The experiments show the ability of the proposed EZD method to distinguish the qualitative difference between a HIF and the load step-up and to do so with a small reference injection and fast convergence time. The experiment is implemented using an industry-standard microcontroller, and practical sensors for the current and voltage. The results in this section validate the implementation of the HIF detection method in a real system.
Figure 6.8: Picture and Diagram of the experimental set-up implemented to test the proposed HIF detection method; the proposed method can identify the load change (implemented with an electronic load) from a HIF (implemented with a resistance). The PEC (a) is controlled by the standard microcontroller board (b), where the EZD-based HIF detection algorithm is implemented. The CPL is implemented using an electronic load (d) in CPL mode that can be externally controlled to step-up. Another channel of the electronic load is used to generate the HIF (c) using the fault test mode. The line connection is implemented using discrete components (e) and $R_f$ can be changed using a discrete resistor (f).

A picture of the experimental set-up used for the validation is shown in Fig. 6.8. The PEC (a) is controlled by the standard microcontroller board (b), where the EZD-based HIF detection algorithm is implemented. The CPL is implemented using an electronic load (d) in CPL mode that can be externally controlled to step-up. Another channel of the electronic load
Table 6.1: Experimental Set-up Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_b$</td>
<td>470 nF</td>
</tr>
<tr>
<td>$L_b$</td>
<td>2.2 mH</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>10 kHz</td>
</tr>
<tr>
<td>$V_o$</td>
<td>24 V</td>
</tr>
<tr>
<td>$P_{L,1}$</td>
<td>24 W</td>
</tr>
<tr>
<td>$\Delta P$</td>
<td>6 W</td>
</tr>
<tr>
<td>$R_f$</td>
<td>100 Ω</td>
</tr>
<tr>
<td>$f_s$</td>
<td>40 kHz</td>
</tr>
<tr>
<td>$f_r$</td>
<td>1 kHz</td>
</tr>
<tr>
<td>$N_p$</td>
<td>2</td>
</tr>
<tr>
<td>$A_r$</td>
<td>2.5%</td>
</tr>
</tbody>
</table>

is used to generate the HIF $c$ using the fault test mode. The line connection is implemented using discrete components $c$ and $R_f$ can be changed using a discrete resistor $f$. The set-point of the CPL, the increment, and the value of $R_f$ are selected to match the expected transitions such that they are indistinguishable from the DC operating point. The parameters of the implemented PEC are given in Table 6.1, they are selected to match the normalized values in the simulations section. The load increment ($\Delta P$) is 6 W, while the $R_f$ of 100 Ω takes 5.76 W. The similarity between both the $\Delta P$ and the extra power drawn from $R_f$ causes two conditions to look very similar for the detection algorithm, presenting the same challenge as in the simulations.

Figure 6.9 shows an oscilloscope capture of the voltage and current ($v_o$ and $i_o$) from the prototype during a load step-up (corresponding to the simulated transient in Fig. 6.6). The output of the proposed EZD method is captured using a DAC from the microcontroller and then scaled correspondingly in the oscilloscope. The system starts from the normal operating point $A$, where the load is 24 W and transitions to a state $B$ where the load is 30 W. During the transition, $i_o$ increases and the output of the EZD algorithm, calculated
Figure 6.9: Oscilloscope captures of the experimental set-up before and after the load change; the $r_{inc}$, measured by the proposed algorithm and extracted using a DAC, reflects an increase (less negative).

in the microcontroller, reflects an increase in $r_{inc}$ (less negative) from $-24 \Omega$ to $-19 \Omega$, as it was expected from (6.3). The signal injected in the system is relatively small and can be further reduced. The transient in $r_{inc}$ shows two peaks, corresponding to the two periods averaged by the EZD, which stem from the need to average in the presence of noise. Convergence is achieved after $5 \text{ ms}$. The proposed method is able to detect the change in the load accurately using the sensors present in the PEC without adding cost.

The transient during the HIF event is shown in Fig. 6.10 (matching the transient simulated in Fig. 6.7). The system starts from the normal operating point $\mathbb{A}$, where the load is $24 \text{ W}$ and transitions to a HIF state $\mathbb{C}$ where an $R_f$ of $100 \Omega$ is added in parallel. While the transient in $v_o$ and $i_o$ are very similar, and the steady-state values are precisely the same, the output of the EZD algorithm reflects a decrease in $r_{inc}$ (more negative), from $-24 \Omega$ to $-29 \Omega$, as expected from the calculations outlined before $\mathbb{1}$. The signal injected in the system
Figure 6.10: Oscilloscope captures of the experimental set-up before and after the HIF; the $r_{inc}$, measured by the proposed algorithm and extracted using a DAC, reflects a decrease (more negative).

is relatively small ➂ and can be further reduced. The transient in $r_{inc}$ shows the same two peaks, corresponding to the two periods averaged by the EZD, which are the same as for the transient load experiment. Convergence is also achieved after 5 ms ➌.

Further comparisons of the transient can be drawn from using the memory feature of the oscilloscope. The comparison is shown in Fig. 6.11. As can be seen, after the transition, the two transients diverge, even when the system has not reached steady state. This apparent difference between the $r_{inc}$ during a load step-up and a HIF in the output of the proposed EZD based method allows the differentiation of both events. The experimental captures shown in Figs. 6.9, 6.10, and compared in 6.11 clearly show the features of the proposed method: the difference in behavior between HIF and $\Delta P_L$ is qualitative ➊; the injected signal is small (less than 2% of the DC voltage) ➋; the detection converges in less than 3 ms ➌.
Figure 6.11: Comparison of the oscilloscope captures using the memory features of the scope; the voltage and current ($v_o$ and $i_o$) are very similar for both transients, but the $r_{inc}$ shows a clear departure.

6.5 Summary

This chapter presented an active High Impedance Fault (HIF) detection method, based on the proposed Embedded Impedance Detection (EZD) method, for DC systems with Constant Power Loads (CPL). The algorithm uses a small signal injected by the Power Electronics Converter (PEC) (through the control loop) to scan the incremental behavior of the system and monitor the transitions. After an output current increase, which could be due to a load increase or a HIF, the HIF detection algorithm monitors the change in the incremental resistance to determine the nature of the transient. The algorithm benefits from the negative resistance of the CPL to differentiate it from the HIF condition.

The combination of the EZD and the nature of the load produce four key advantages: 1) high sensitivity, due to the difference in sign of the change, 2) small reference injected to the system, due to the EZD features, 3) high convergence speed, and 4) embedded implementation.
using the existing hardware. These features allow the proposed method to help prevent
equipment damage, as well as fires, and human harm at no additional cost.

Simulation results showed the difference in readings from the method for HIFs and load
increments that look equal in terms of DC operating point. The proposed algorithm is
further validated with captures of the output of a microcontroller implementation. The
implementation of the EZD method is computationally efficient without sacrificing accuracy,
allowing it to be implemented in an industry-standard microcontroller without increasing
cost. The experimental captures match the simulation results.
Chapter 7

Maximum Power Point Tracking forPV Systems

One essential function of a Power Electronics Converter (PEC) interfacing a renewable energy source as in Fig. 7.1(a), such as a photovoltaic (PV) panel, is to ensure that it maximizes the power transferred to its load. This Maximum Power Point Tracking (MPPT) task is usually challenging, as it is often the case that the actual operating conditions of the renewable energy source are not known. Since maximum power transfer is achieved when the source and load impedances are matched, it stands that the proposed Embedded Impedance Detection (EZD) method can offer unique advantages in this field.

A first approach would be to use a reference injected in the system and extract the impedance as outlined before. This approach was explored in a preliminary version of this work, and it provided some benefits [6], such as accurate tracking and reduced perturbation size; however, the power of the proposed EZD method allows this technique to be pushed to the extreme: no reference injection at all.

Portions of this chapter have been published in

This chapter presents an MPPT algorithm for uniformly irradiated PV cells to provide switching ripple detection and tracking abilities in the presence of noise to allow high MPPT performance. The core implementation of the EZD method is modified to use the switching ripple as the reference signal, executing the EZD algorithm every switching cycle.
The novel MPPT technique, based on the Lock-In Amplifier, takes advantage of the existing switching ripple and provide adaptive-steps resulting in enhanced performance. Due to its core resemblance to the Incremental Conductance (InCond) algorithm, the proposed technique is dubbed *LIA-Based InCond*. The three key desirable features of this algorithm are outlined in Fig. 7.1(b) in comparison with the standard InCond algorithm: Using the switching ripple to measure the conductance allows for smooth operation in steady-state ➊, fast and accurate start-up ➋, and accurate tracking during the transients with no errors ➌.

The benefits and performance of the LIA-Based InCond are validated using simulations to carefully compare it with the traditional InCond, a benchmark algorithm widespread in the industry and literature. Experimental results, implemented in an industry-standard microcontroller and real PV panels, are provided to assess the performance of the proposed strategy and its feasibility. A comparison is performed with other competing high-performance algorithms to show how this technique fares with resent advancements.

### 7.1 System Model

The behavior of the PV panel with the PEC can be analyzed from the block diagram in Fig. 7.1(a). The DC bus is assumed to be able to take all the energy available from the PV panel, therefore making it useful to have MPPT, and the selected PEC is a boost converter. The $i_{pv}$ and $v_{pv}$ are regulated by the PEC to maximize the power transferred. Two MPPT algorithms are implemented in this chapter: the proposed LIA-Based MPPT and the standard InCond, as a comparison reference. The standard InCond algorithm is selected as a baseline comparison since most modern MPPT algorithms are at some point compared with the InCond; by comparing with this algorithm, it is possible to extend the comparison to other existing algorithms and future improvements. In this work, the algorithms directly drive
the duty-cycle ($d$) of the PEC, producing MPPT-oriented control algorithms that maximize speed while reducing complexity by removing the need for voltage and current loops.

### 7.1.1 Photovoltaic Panel Background

A PV cell is a semiconductor device that transforms photons arriving at its surface into electrical current. Figure 7.2(a) shows a simple diagram of a PV panel; the PV cell is, in essence, a diode exposed to light and, as expected, its behavior responds to the characteristics of a diode. Figure 7.2(b) presents an equivalent behavioral model of a PV cell: the PV cell behaves like a current source ($I_{pv}$), given by the amount of irradiance arriving at the cell ($I_{rr}$); with a parallel diode ($D$), a parallel resistor ($R_{sh}$), and a series resistor ($R_s$).

The voltage and current ($v_{pv}$ and $i_{pv}$) of a PV cell are given by

$$i_{pv} = I_{ph} - \left( e^{\frac{v_{pv} + i_{pv}R_s}{nVT}} - 1 \right) - \frac{v_{pv} + i_{pv}R_s}{R_{sh}}, \quad (7.1)$$
where \( n \) is the diode ideality factor (1 for an ideal diode), and \( V_T \) is the thermal voltage given by

\[
V_T = \frac{\kappa T}{q},
\]

where \( \kappa \) is Boltzmann’s constant, \( T \) is the absolute temperature, and \( q \) is the elementary charge.

A PV cell on its own produces a small amount of power; its voltage is approximately 0.6 V and its current is around 2 A; for this reason, PV cells are built into panels of series/parallel connections. A connection of \( M_s \) cells in series is called a \textit{string} and it increases the voltage by \( M_s \). \( M_p \) strings can be connected in parallel to increase the current. For \( M_p \) equal strings of \( M_s \) series-connected cells, the characteristic V-I curve is given by

\[
i_{pv} = M_pI_{ph} - M_pI_0 \left( e^{\frac{v_{pv} + i_{pv}R_sM_s/M_p}{M_sV_T}} - 1 \right) - \frac{v_{pv} + i_{pv}R_sM_s/M_p}{M_sR_{sh}}.
\]

The power produced by the PV panel \( p_{pv} \) is given by

\[
p_{pv} = i_{pv} \times v_{pv}.
\]

Fig. 7.3 presents the V-I and V-P curves of a PV panel. The output of the PV panels is affected by \( I_{rr} \) (which increases the current and the overall power) and by the temperature. The effects of \( I_{rr} \) are shown in Fig. 7.3(a), while the effects of the temperature are shown in Fig. 7.3(b).

The maxima of (7.4) has to be found to operate the PV panel at the MPP. When the system operates at the MPP, the power characteristic has a zero derivative

\[
\frac{dp_{pv}}{dv_{pv}}_{MPP} = 0,
\]
Expanding (7.5) for the V-I expressions, the condition can be stated as

$$\left. \frac{i_{pv}}{v_{pv}} \right|_{MPP} = -\left. \frac{di_{pv}}{dv_{pv}} \right|_{MPP}. \quad (7.6)$$

The left term of (7.6) is the equivalent load that the PEC presents to the PV panel, that is the DC conductance ($G$). The right term of (7.6) is the negative of the incremental conductance ($-g$) of the PV panel. As expected, $g$ is negative for a PV panel (increasing $v_{pv}$ yields a lower $i_{pv}$). Therefore, the MPP condition can be

$$G = -g. \quad (7.7)$$

This condition is represented in Fig. 7.4. The load line (whose slope is given by $G$) has to be perpendicular to the tangent line (with a slope of $-g$) at that MPP. Keeping the PV panel
Figure 7.4: Characteristic behavior of the PV cell around the MPP: the MPP is characterized by the equivalent load ($G$) being equal to the negative of the incremental conductance ($g$), which gives a flat V-P curve.

working in this condition under changing environmental conditions is the task of the MPPT algorithm.

### 7.1.2 Standard InCond MPPT Algorithm

Figure 7.5(a) shows a flowchart of the standard InCond MPPT algorithm. The algorithm scans the I-V curve looking for the condition of (7.7). The estimated $G$ is

$$\hat{G}[K] = \frac{i_{pv}[K]}{v_{pv}[K]},$$

(7.8)
where $i_{pv}[K]$ and $v_{pv}[K]$ are the current and voltage of the PV panel measured at a given operating point in step $K$. The estimated $\hat{g}$ is given by

$$\hat{g} = \frac{i_{pv}[K] - i_{pv}[K - 1]}{v_{pv}[K] - v_{pv}[K - 1]}.$$  

(7.9)

With (7.8) and (7.9), the new operating point is

$$d[K + 1] = \begin{cases} 
  d[K] - \Delta d & \text{if } \hat{G}[K] < -\hat{g}[K] \\
  d[K] + \Delta d & \text{otherwise}
\end{cases},$$  

(7.10)
where $d[K]$ is the PEC’s duty-cycle and $\Delta d$ is the step-size of the algorithm. The selection of $\Delta d$ and the time between MPP decisions ($T_{MPPT}$) has to be selected based on the application and is one of the disadvantages of the InCond algorithm.

Figure 7.5(b) shows the timing diagram of the InCond algorithm. The algorithm waits for the PEC to stabilize in the new operating point before making a new decision since this time depends on the operating point, it has to be calibrated for the worst case (slowest response).

This algorithm has several disadvantages that are inherent to its core nature: a) the continuous injection of a perturbation causes an oscillation in between three states that reduces the overall efficiency of the PEC, b) the fixed $\Delta d$ and $T_{MPPT}$ create a trade-off between accuracy (given by a smaller $\Delta d$) and speed (given by a larger $\Delta d$) and a balance has to be selected, c) since the PEC has to reach steady-state to obtain a valid measurement, the $T_{MPPT}$ is limited by the PEC’s speed further compromising the tracking, d) since changes in irradiance can happen in between samples, errors can happen in the calculation of $\hat{g}$ causing deviations in the operating conditions, and e) the tracking of gradual changes in the irradiance is not accurate except when $\Delta d$ coincides with the optimal changing rate. The proposed LIA-Based MPPT algorithm tackles those limitations.

### 7.2 Proposed LIA-Based MPPT

The InCond algorithm is based on the estimation of $G$ and $g$ by the difference between adjacent operating points. However, a more accurate estimation can be obtained using the EZD method proposed in this work. The block diagram of the proposed LIA-Based MPPT algorithm is shown in Fig. 7.6(a); it uses a MAF to extract the average values of $v_{pv}$ and $i_{pv}$ to calculate $G$ and uses two LIAs and the switching ripple injected by the PEC as the reference signal to measure $g$. A digital Integral controller ($I(z)$) is used to drive the difference
Figure 7.6: In (a) a block diagram of the proposed LIA-Based InCond algorithms, it is based on using the switching ripple along with a fast LIA and MAF to measure the $G$ and $g$ and match them using an integral controller ($I(\tilde{z})$); in (b) a time diagram of the proposed MPPT algorithm in steady-state showing the PV panel voltage and current ($i_{pv}$ and $v_{pv}$), and the switching signal ($S_g$), the amplitude of the fundamental components ($A_{1,i}$ and $A_{1,v}$) are used to extract $g$, while the averages are used to calculate $G$.

between $G$ and $g$ to zero. A timing diagram of the operation of the proposed LIA-Based MPPT algorithm is shown in Fig. 7.6(b).

The use of a PEC to adapt the voltage/current characteristics of the PV panel to the load and do the MPPT process introduces an inherent ripple to the PV panel controlled by the switching frequency ($f_{sw}$), the duty cycle ($d$), and the reactive components of the converter ($C_b$ and $L_b$). This ripple is usually lower than 1% of the DC voltage. Using this ripple to measure $g$ is particularly convenient since: a) it is already in the system, so no additional perturbation is injected, b) it is small compared with the standard step-size of the InCond algorithm (usual values for the InCond stepsize are around 10% of $V_{oc}$), c) it is very fast, which allows for accurate tracking of changing environmental conditions (the
steps of the InCond are injected at intervals of 500 – 100 ms, while the ripple has a period of 0.01 – 0.1 ms), and d) it calculates the tangent line around the operating point, instead of the secant line between two operating point.

Two characteristics need to be identified from \( v_{pv} \) and \( i_{pv} \): the average value (\( \bar{i}_{pv} \) and \( \bar{v}_{pv} \), to calculate \( G \)), and the amplitude of the fundamental components from ripple (\( A_{1,i} \) and \( A_{1,v} \), to calculate \( g \)). This is achieved by sampling the ripple and applying the MAFs to extract \( \bar{i}_{pv} \) and \( \bar{v}_{pv} \) in the switching cycle, and the LIAs to extract \( A_{1,i} \) and \( A_{1,v} \). It is important to note that, as opposed to the general formulation of the EZD method outlined in Chapter 2, the LIA, and impedance calculation are computed every switching cycle and without injecting the reference signal. This makes the computation efficiency more critical than the case where the reference is injected at a lower frequency and the computations are performed only once per switching cycle (and at a lower priority).

Once \( G \) and \( g \) have been measured, the MPPT’s task is to keeping the difference between them zero. While traditional InCond implementations check the difference and move the operating point one step in that direction, a more straightforward implementation can be made using an integral controller.

### 7.2.1 DC Conductance Measurement

Measuring the DC conductance (\( G \)) presented by the PEC to the PV panels is relatively simple: measuring \( i_{pv} \) and \( v_{pv} \), the mean value in a cycle is related to the DC load as

\[
G[K] = \frac{\bar{i}_{pv}[K]}{\bar{v}_{pv}[K]},
\]

(7.11)

where \( \bar{i}_{pv}[K] \) and \( \bar{v}_{pv}[K] \) are the outputs of the MAF used for oversampling after the rate transfer block, as shown in Fig. 2.5 and discussed in Section 2.2.1. For an oversample of \( M \)
points per switching cycle, the MAF for each signal is given by (2.12)

\[
\bar{i}_{pv}[k] = \frac{1}{M} \sum_{i=0}^{M-1} i_{pv}[k-i],
\]

(7.12)

\[
\bar{v}_{pv}[k] = \frac{1}{M} \sum_{i=0}^{M-1} v_{pv}[k-i].
\]

(7.13)

Note the difference in the sample index between the MPPT step \((K)\) and the oversample step \((k)\). The averages are taken inside a single switching period subdivided in \(M\) samples, only one decision is made per switching cycle, as illustrated in Fig. 7.6(b).

### 7.2.2 Incremental Conductance Measurement

The calculation of the incremental conductance \((g)\) is performed using the proposed EZD method. For this application, the reference signal that the LIA locks-into is the switching ripple introduced by the PECs. For this, two crucial modifications are introduced in the system: 1) the EZD block (in particular the LIAs) is moved to before the rate transition in the signal chain in Fig. 2.5, and 2) no reference signal \((r[k])\) is generated.

The switching ripple has a fundamental frequency of \(f_{sw}\). Therefore the reference frequency is given by

\[
f_r = f_{sw}.
\]

(7.14)

The number of samples in the reference is selected as the same as the oversample rate

\[
N_s = M,
\]

(7.15)

which makes the sampling time

\[
T_s = \frac{1}{M f_{sw}}.
\]

(7.16)
This introduces the challenge to compute the LIA $M$-times per switching cycle, which requires much more computation than the injected reference approach. The efficient computations introduced in Chapter 2 allow it to be performed. Moreover, the fact that the value of $g$ is only used once per switching cycle allows the equivalent impedance calculation to be computed only once per cycle, avoiding additional products and divisions for discarded results. Finally, for most applications that concern such a fast MPPT, the reactive components in the connections are minimal, and the phase shift can be neglected.

Considering this, $g$ is given by

$$g[K] = \frac{A_{1,i}[K]}{A_{1,v}[K]}.$$  \hfill (7.17)

If a significant phase shift is expected (due to long wires or high capacitance in the particular PV panels), (7.17) can be expanded using (2.60).

The use of the embedded LIA allows the fundamental amplitude of the ripples to be extracted and combined to calculate $g$.

### 7.2.3 MPP Regulator

Once $G$ and $g$ have been measured, the objective of the MPPT algorithm is to make them match, such that

$$G - g = 0.$$  \hfill (7.18)

While the traditional InCond would compare the two values and step in one direction based on the sign of the difference, a simpler solution can be implemented. By selecting the step-size to be proportional to the difference between the two resistances, the duty cycle is

$$d[K + 1] = d[K] + K_f(G - g),$$  \hfill (7.19)
where \(d[K]\) is the duty-cycle in step \(K\), and \(K_I\) is the proportionality constant; this corresponds to a digital Integral Controller \((I(z))\) that regulates the difference between the two conductances to be zero. The MPPT happens at switching speed

\[
T_{MPPT} = \frac{1}{f_{sw}} = MT_s.
\]  
(7.20)

In summary, the proposed LIA-Based MPPT algorithm uses a MAF and LIA to measure \(G\) and \(g\) accurately, and a simple \(I(z)\) achieving zero steady-state error and adaptive-step characteristics. The implementation of the filters is computationally efficient, and the tuning of \(K_I\) is simple, given its well-known behavior.

### 7.2.4 Stability of the Proposed MPPT

In order to evaluate the stability of the proposed LIA-Based MPPT strategy a small signal model of the plant and controller around the MPP is developed. A block diagram of the system is presented in Fig. 7.7, where \(G\) is obtained by the MAF and \(g\) is obtained with the EZD method. The digital controller is evaluated once every MPPT sample period \((T_{MPPT})\) indicated by the index \(K\). The new duty cycle \(d[K]\) is determined by the integral controller \(I(z)\) to produce the adaptive-step and passed through the Zero-Order-Hold to the continuous time domain. The DC/DC PEC and PV panel are modeled by \(H_{dV}\). It is important to note that the sample time of the MAF and LIA \(T_s\) is \(M\)-times smaller and indicated by the index \(k\); the output of the filters is evaluated only once per MPPT cycle resulting in a cycle average and avoiding the interaction between the filters and the control loop.

The small signal averaged transfer function of the PEC around the MPP is given by

\[
H_{dV}(s) = \frac{-V_{link}}{L_b C_b s^2 + L_b G_{MPP} s + 1},
\]  
(7.21)
Figure 7.7: Block diagram of the LIA-based MPPT algorithm with the control loop to evaluate stability.

where $G_{MPP}$ is the DC conductance at the MPP and $V_{link}$ is the voltage of the DC bus. The error signal $(e)$ is given by the MPP criteria given in (7.7) and it can be rewritten as

$$e = \frac{i_{pv}}{v_{pv}} + \frac{di_{pv}}{dv_{pv}}. \quad (7.22)$$

A linearization of $e$ around the MPP is given by

$$e(v_{pv}, i_{pv}) \approx e(V_{MPP}, I_{MPP}) +$$
$$+ \left. \frac{\partial e(v_{pv}, i_{pv})}{\partial v_{pv}} \right|_{V_{MPP}, I_{MPP}} (v_{pv} - V_{MPP}) +$$
$$+ \left. \frac{\partial e(v_{pv}, i_{pv})}{\partial i_{pv}} \right|_{V_{MPP}, I_{MPP}} (i_{pv} - I_{MPP}), \quad (7.23)$$

And considering the approximation of $i_{pv}$ around the MPP is

$$i_{pv} \approx 2I_{MPP} - G_{MPP}v_{pv}, \quad (7.24)$$
the e signal can be estimated as

\[ e(v_{pv}, i_{pv}) \approx 2G_{MPP} - 2\frac{G_{MPP}}{V_{MPP}}v_{pv}. \]  
(7.25)

The small-signal, averaged \( e \) is given by

\[ \hat{e}(v_{pv}, i_{pv}) \approx -2\frac{G_{MPP}}{V_{MPP}}\hat{v}_{pv}. \]  
(7.26)

The change in the duty cycle is given by

\[ \hat{d}(z) = -2\left(\frac{G_{MPP}}{V_{MPP}}\hat{v}_{pv}\right)\left(\frac{K_I T_{MPPT}}{z - 1}\right), \]  
(7.27)

and after the ZOH, the continuous time duty-cycle is given by

\[ \frac{\hat{d}(s)}{\hat{v}_{pv}(s)} = -2\left(\frac{G_{MPP}}{V_{MPP}}\right)\left(\frac{K_I T_{MPPT}}{e^{sT_{MPPT}} - 1}\right)\left(1 - \frac{e^{sT_{MPPT}}}{sT_{MPPT}}\right). \]  
(7.28)

The time delay \( e^{sT_{MPPT}} \) can be approximated by Taylor’s expansion as \( (1 - sT_{MPPT}) \). This model yields the following expression for the voltage-to-duty-cycle transfer function

\[ \frac{\hat{d}(s)}{\hat{v}_{pv}(s)} = -2\left(\frac{G_{MPP}}{V_{MPP}}\right)\left(\frac{K_I(1 - sT_{MPPT})}{s}\right). \]  
(7.29)

The characteristic equation is given by

\[ H(s) = 1 + 2\left(\frac{K_I G_{MPP}V_{link}}{V_{MPP}}\right)\left(\frac{1 - sT_{MPPT}}{L_b C_b s^3 + L_b G_{MPP} s^2 + s}\right). \]  
(7.30)

The range of stable values for \( K_I \) depends on the system parameters as well as \( T_{MPPT} \) as expected. Figure 7.8 presents the bode plot for the simulated system parameters; it shows

159
the Gain and Phase Margins available for the system. The range of stable values for $K_I$ in each application can be determined using this model.

### 7.3 Simulation Results

The previous section introduced the proposed LIA-Based InCond algorithm. This algorithm benefits from the fast and efficient computation of the DC and incremental conductances ($G$, and $g$) using the proposed EZD method, and the impedance matching characteristic of the MPPT process to produce a novel MPPT algorithm with desirable characteristics. Computer simulations are performed incorporating the proposed algorithm and comparing against the InCond to validate the outlined claims.

The simulated model of the system consists of a PV panel connected to a constant DC bus through a boost converter and the MPPT controller to determine the duty cycle of
the converter, as shown in Fig. 7.1(a). The MPPT and control block implement either the proposed or the standard method. The analog stages and quantization of ADC are implemented in the model to better reflect the behavior of the platform and its possible shortcomings.

The results of the simulations are presented in the normalized domain, where the normalization factors are the MPP current, voltage, and power in standard test conditions ($I_{MPP}^o$, $V_{MPP}^o$ and $P_{MPP}^o$). The $f_{sw}$ is set to 10 kHz and $f_s$ to 80 kHz which makes the order of the MAF

$$M = \frac{f_s}{f_{sw}} = 8. \quad \text{(7.31)}$$

Different slopes are considered during the simulation to validate the ability of the proposed algorithm to track different transients. The details of the transients implemented are presented in Table 7.1, each transient is assigned a label (A, B, C and D) to track them through the different simulation captures and domains.

Table 7.1: Simulation Transients Implemented to Test MPPT Algorithms

<table>
<thead>
<tr>
<th>Label</th>
<th>Initial $I_{rr}$ [kWm$^{-2}$]</th>
<th>Final $I_{rr}$ [kWm$^{-2}$]</th>
<th>Speed [kWm$^{-2}$s$^{-1}$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.6</td>
<td>1.0</td>
<td>40</td>
</tr>
<tr>
<td>B</td>
<td>1.0</td>
<td>0.3</td>
<td>−70</td>
</tr>
<tr>
<td>C</td>
<td>0.3</td>
<td>1.0</td>
<td>7</td>
</tr>
<tr>
<td>D</td>
<td>1.0</td>
<td>0.3</td>
<td>−7</td>
</tr>
</tbody>
</table>

Figure 7.9 presents the simulation results for the standard InCond algorithm. The standard InCond presents a slower start-up time and oscillations in steady-state; the step-size selection balances the tracking speed and accuracy and constitutes a trade-off between these aspects. During the transients (A, B, C, and D), the algorithm can make the wrong decision (increase $d$ instead of decreasing it) based on the direction of the irradiance change and the previous step-direction. Even when tracking in the correct direction, the InCond algorithm is prone to overshoot if the tracking speed does not precisely match the irradiance.
change speed. These oscillations, delays, errors, and overshoots contribute to reducing the tracking efficiency of the algorithm and are well-known limitations of the InCond algorithm.

Figure 7.10 presents the simulation results for the proposed LIA-Based MPPT. The proposed LIA-Based MPPT algorithm solves all those issues effectively. Using the LIA and the inherent switching ripple of the PEC it is possible to produce smooth operation in steady-state maximizing the extracted power \(^1\), the adaptive-step feature allows the quick and accurate start-up of the system \(^2\), and the combination of both can clearly identify the changes in \(I_{rr}\) and track them \(^3\). From Fig. 7.10, the benefits of the proposed LIA-Based MPPT are evident.

A comparison of the transient tracking capabilities of both algorithms is presented in Fig. 7.11 for the transients \(\text{A}, \text{B}, \text{C}\) and \(\text{D}\) in Figs. 7.9 and 7.10. The proposed LIA-
Based MPPT keeps the tracking within 98% of the MPP during all the transients, while the standard InCond deviates notably during the transient. While the transient in A shows a high tracking accuracy, this is due to the excellent match between the slope of the transient and the step-size. For transients where the slope is descending, such as B and D, the mismatch is exacerbated by the confusion caused by the descent. During transient C, even when the InCond chooses the correct direction, it overshoots by 10%. The proposed LIA-Based algorithm prevents all these shortcomings: tracking during all the transients is smooth and remains with 98% of the simulated MPP.

The same transients can be observed in Fig. 7.12 in the $V - I$ plane. The proposed MPPT has a superior performance operating over the optimal line while the standard InCond algorithm deviates visibly from that optimal trajectory. The labels A, B, C, and D...
indicate the trajectory of the InCond algorithm since the LIA-Based MPPT stays very close to the optimal line. Transient (D) shows a drop of 23% in power output for the InCond caused by the typical confusion (wrong decision during irradiance changes) of the standard InCond algorithm due to the overall power decreasing for a long period of time; the proposed LIA-Based algorithm does not present this problem, producing accurate tracking all the time.

The selection of $K_I$ influences the transient effects in the same way as any control loop. The effects of this parameter for a range of 0.3 to 3 are shown in Fig. 7.13. Even when the whole range of parameters produces stable behavior, the selection can lead to faster tracking or have overshoot when it is not correctly selected. The value of 2 was selected for $K_I$ for these simulations.
Figure 7.12: $V-I$ plane representation of the transients A, B, C and D for the proposed LIA-Based MPPT and the Standard InCond algorithms.

Figure 7.13: Influence of the selection of the integral gain $K_I$ on the tracking capabilities of the LIA-Based MPPT.

Finally, a summary of the tracking efficiency (defined as the distance to the true MPP, in percentage) of both algorithms during the complete simulation can be observed in Fig. 7.14. The curves show how the proposed MPPT keeps the tracking efficiency within 98% all the time and within 99% in steady-state. The variations in the tracking efficiency have one component for the proposed LIA-Based MPPT (the switching ripple) and an additional component for the InCond MPPT (the oscillation in steady-state). The tracking efficiency is lower at lower irradiance since the step-size is constant and $v_{MPP}$ is not linearly dependent on
the irradiance, leading to a proportionally more significant loss due to the variation at lower irradiance. This is expected given the logarithmic dependence of $v_{MPP}$ with the irradiance. The using the standard InCond result in lower tracking efficiency, especially during the transients where it goes below the top 10%.

### 7.4 Experimental Results

The simulation results in the previous section showed how the standard InCond algorithm has a limited start-up speed (given by the fixed step-size and sample time), has oscillations in steady-state, and can make the incorrect decision when tracking transient irradiance profiles if those do not match the tuned speed. To further validate the proposed LIA-Based InCond algorithm, an experimental set-up was built with similar characteristics to the simulated system, and it was tested using fast transitions in $I_{rr}$. These experimental results not only confirm the benefits shown in the simulations but also show evidence that the proposed EZD method is able to measure $g$ from the switching ripple using standard sensors and microcontrollers used in PECs.
Table 7.2: MPPT Experimental Set-up Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_b$</td>
<td>470 nF</td>
</tr>
<tr>
<td>$L_b$</td>
<td>2.2 mH</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>10 kHz</td>
</tr>
<tr>
<td>$f_s$</td>
<td>80 kHz</td>
</tr>
<tr>
<td>$f_c$</td>
<td>40 kHz</td>
</tr>
<tr>
<td>$M$</td>
<td>8</td>
</tr>
<tr>
<td>$T_{MPPT,InC}$</td>
<td>2 ms</td>
</tr>
<tr>
<td>$\Delta d_{fast}$</td>
<td>2%</td>
</tr>
<tr>
<td>$\Delta d_{slow}$</td>
<td>1%</td>
</tr>
<tr>
<td>Voltage Range</td>
<td>0 to 30 V</td>
</tr>
<tr>
<td>Current Range</td>
<td>0 to 6 A</td>
</tr>
</tbody>
</table>

Figure 7.15 shows a picture and a diagram of the experimental platform. Figure 7.15(a) shows the picture of the experimental set-up. Real PV panels are used to test such a high-speed algorithm since PV array emulators have limited bandwidth. As such, the custom-built solar chamber indicated by (a) contains two PV panels and lamps to generate controllable irradiance profiles. The DC source (b) driven in external mode by a signal generator (c) with a custom profile powers the lamps. The power platform (d) is connected in its input port to the PV panels and its output port to the DC Load (e), working in constant-voltage (CV) mode.

Figure 7.15(b) shows a detailed picture of the power platform. The power stage (f) is controlled by a TI C2000 microcontroller (g), typically employed to control PECs, to perform the MPPT process. A summary of the system parameters is presented in Table 7.2.

Figure 7.16(a) shows an oscilloscope capture of the experimental set-up operating in steady-state to show the signals that are used to measure the impedance. The $v_{pv}$ and $i_{pv}$ are measured using voltage and current probes, while $p_{pv}$ is calculated using a math operation. The standard resolution, shown in the left, presents no oscillation in steady-state and
Figure 7.15: Experimental set-up implemented to test the proposed LIA-Based MPPT algorithm against the classic InCond method; in (a) the overall picture of the set-up shows the chamber with the PV panels, illuminated by lamps controlled with a DC source to produce the desired profile, the PEC is connected to a DC load set in constant voltage mode; in (b) a picture of the PEC in the experimental platform, the controller is implemented in a TI microcontroller; in (c), a block diagram of the experimental platform.
a smooth behavior, a desirable operating mode to maximize the energy extracted, without
the oscillation in steady-state that reduces the efficiency. The zoom-in section, shown to the
right, shows the switching oscillation that is isolated by the LIA to extract the incremental
conductance. This small ripple is characteristic of the system, as opposed to the perturba-
tion injected by the InCond algorithm to locate the MPP. The $v_{pv}$ and $i_{pv}$ are 180° separated
(the maximum $v_{pv}$ happens at the $i_{pv}$ minimum), this is expected, given the nature of the
V-I curve of the PV panel. The LIA can extract this small value rejecting the noise, while
the computation time for this configuration was measured to be less than 0.6 µs per sample,
which would allow further increasing $f_{sw}$ to hundreds of kilohertz.

Fig. 7.16(b) shows an experimental capture of the proposed LIA-Based MPPT for irradi-
ance transients. The irradiation of the PV panel changes during the transient; the dynamics
of the lamps limit the transient speed. The proposed LIA-Based MPPT stabilizes at the
MPP showing no oscillations $\ddagger$, and can track the MPP in a smooth way $\ddagger\ddagger$, this coincides
with the simulated results.

Figures 7.17(a) and (b) present experimental captures of the standard InCond with two
different steps-sizes (fast and slow). The InCond with a small tracking step produces smaller
oscillations in steady-state but is not able to track the MPP during changing environmental
conditions, producing a lagging result. The InCond with a large step-size can track faster
but has occasional overshoots and a much larger oscillation in steady-state which leads to
reduced efficiency. Proper tuning leads to a balance for a given slope, panel, and oscillation
but the benefits are lost if the slope of the change in $I_{rr}$ is changed.

7.5 Comparison Against Other MPPT Methods

The comparison of the proposed LIA-Based MPPT algorithm was performed against the
standard InCond. This provides a reference point to compare with advanced MPPT algo-
Figure 7.16: In (a), the steady-state experimental capture of the proposed LIA-based MPPT, the zoom shows the small switching ripple used to identify \( g \); in (b), the transient experimental capture of the proposed LIA-based MPPT, it benefits from the ➊ eliminated oscillation, the small-signal identification, and ❼ adaptive-step.

Table 7.3 shows a comparison of the proposed LIA-Based MPPT with the results reported for other advanced MPPT algorithms. The selected algorithms are presented for their advanced features that allow for fast tracking and account for environmental changes. Since the tracking speed is highly dependent on the size of the PEC [183], the tracking time is normalized to the resonance frequency of the PEC (for those documents that provide said values). The selected algorithms use InCond versions with adaptive-step (such as the \( \beta \) algorithm) or very high-speed controllers such as the sliding mode controller to increase the speed. The proposed algorithm benefits from the single loop MPPT-oriented control.
to increase the speed and the LIA and MAF to reduce the perturbation size allowing fast, accurate, and smooth behavior.

Although the proposed technique presents higher computational demand for the sampling and filters compared with standard MPPT algorithms, the removal of the perturbation that leads to higher steady-state tracking efficiency, the ability to identify the changes and the adaptive step-size obtained are a significant advantage over more simple algorithms. Typical digitally-controlled PECs sample several times per switching cycle to average the behavior of the current/voltage, and the processing power of industry-standard microcontroller (C2000) is capable of handling this load. The benefits of the proposed implementation, with smooth
Table 7.3: Comparison of the proposed LIA-Based MPPT algorithm, the InCond, and the results reported in the literature for four advanced MPPT algorithms

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Loops</th>
<th>Perturbation</th>
<th>$\tau_o$</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>InCond ($\Delta d_{fast}$)</td>
<td>MPPT</td>
<td>Fixed</td>
<td>742</td>
<td>Baseline comparison algorithm</td>
</tr>
<tr>
<td>LIA-Based</td>
<td>MPPT</td>
<td>None</td>
<td>20</td>
<td>Tracking of transient slopes and steps are optimized; higher compu-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>tational cost</td>
</tr>
<tr>
<td>Sliding Mode</td>
<td>V + MPPT</td>
<td>Fixed</td>
<td>405</td>
<td>Control is based on Sliding mode, while MPPT is based on InCond;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Tracking of slope changes shows problems as InCond</td>
</tr>
<tr>
<td>Locus Based Emulated Resistance</td>
<td>I + MPPT</td>
<td>Fixed†</td>
<td>187</td>
<td>Requires off-site characterization</td>
</tr>
<tr>
<td></td>
<td>V + MPPT</td>
<td>$V_{oc}$ measured</td>
<td>74</td>
<td>Requires off-site characterization and temperature characterization;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>requires periodic measurement of $V_{oc}$</td>
</tr>
<tr>
<td>$\beta$</td>
<td>MPPT</td>
<td>Variable‡</td>
<td>52</td>
<td>Requires off-site characterization and temperature characterization and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>irradiance tuning for $\beta$</td>
</tr>
</tbody>
</table>

* Tracking time normalized to the converter resonance frequency $\tau_o = T_o/(2\pi\sqrt{LC})$
† Fixed step is used in steady-state, the large tracking is done with the Locus Based Method
‡ Reduced until a minimum value

operation and adaptive tracking speed become evident when compared with the standard MPPT algorithms.

The additional computation required can present a limitation for very fast switching power converters (above 250 kHz, for the selected microcontroller) given that they will overflow the computation capabilities of the microcontroller. However, for this scenarios, the $g$ measured at such frequency is not representative of the power transfer and will not yield the MPP\(^2\).

\(^2\)This high frequency is interesting however for other applications of the EZD for high frequency devices such as \cite{184}
7.6 Summary

A new Maximum Power Point Tracking (MPPT) algorithm for uniformly irradiated photovoltaic (PV) panels, based on the proposed Embedded Impedance Detection (EZD) method, was presented in this chapter. This algorithm, dubbed Lock-In Amplifier (LIA) based incremental conductance (LIA-InCond), used the inherent ripple in Power Electronics Converters (PEC) combined with the Moving Average Filter and the LIA to produce accurate tracking of the MPP, even in the presence of changes in the environmental conditions, without the need of injecting any kind of disturbance to the system or including any additional sensors. An Integral controller was used to produce an adaptive-step feature for variable tracking speed that allows for fast tracking, and its stability was studied based on the small-signal model.

The combination of these characteristics produced: 1) smooth operation in the steady-state, maximizing the transferred power and removing the characteristic oscillations of standard MPPT algorithms to achieve 99% tracking efficiency in steady-state, 2) fast and accurate tracking during the start-up (40 times faster than the reference InCond method) and 3) irradiance change identification and tracking for variable change rates (with 98% tracking efficiency during transients).

The proposed algorithm was validated using computer simulations comparing against the standard InCond algorithm as a benchmark. Further validation was performed with an experimental platform, showing good agreement with the simulations and the feasibility of implementing the EZD method based on the switching ripple. A comparison of the results of the proposed MPPT algorithm was performed against several modern MPPT algorithms to highlight the benefits and drawbacks. It was shown that the proposed LIA-InCond achieves 40 times speed improvement over the traditional InCond, and between 2 and 20 times im-
provement over other fast methods, without the need of device specific tuning, removing the 
perturbation, and using a single control loop oriented to MPPT.

The performance improvements provided by this simple method, based on the proposed 
EZD method, both in steady-state and during transients show the benefits of using the 
inherent ripple as the reference signal. The power of the proposed detection technique to 
isolate a minimal signal in the voltage and current and compute the impedance in real-time 
allows this to be achieved.
Chapter 8

Conclusion

8.1 Conclusions and Contributions

This dissertation introduced the Embedded Impedance Detection (EZD) method and explored five critical applications for it: Maximum Power Point Tracking (MPPT) for Photovoltaic (PV) systems, Adaptive Control for systems with Constant Power Loads (CPLs), Islanding Detection (ID), Low-Impedance Fault (LIF) Location, and High-Impedance Fault (HIF) Detection. The general analysis and design considerations of the proposed method were discussed in Chapter 2. That chapter introduced the fundamental building blocks: the signal-processing chain, the reference generation, the signal extraction, and the computation of the impedance; and their design considerations.

The core contribution of this work is the possibility of implementing online, real-time, impedance detection on every power converter in the system, using only the sensors already present in the converter. For this reason, Chapter 2 placed particular emphasis on the implementation considerations to make the system as accurate and fast as possible, while maintaining a computationally efficient implementation. In the past, impedance detection was limited to dedicated, expensive, hardware in the laboratory environment, the proposed EZD allows it to be carried out inside all converters.

The ensuing chapters discussed the characteristics of each application. Each chapter showed the analysis of the problem, the use of the EZD as a solution, and its validation. The validation section included time-domain simulation, experimental results implemented
in real Power Electronics Converters (PECs), Hardware-In-The-Loop (HIL) co-simulations, and comparison with competing technologies, as appropriate.

Overall, this work showed that real-time impedance detection can be implemented in distributed PECs with little to no cost and adds new capabilities to the system. It shows that the EZD provides critical insights into the behavior of the DC system, such as real-time detection of the incremental behavior of the load, otherwise masked by the constant voltage and current in the system. These new features increase the autonomy and modularity of the system by providing insights into more than just the DC operating point. This technique can be implemented in new designs, as well as in existing hardware, as it does not require specialized hardware.

As the power and energy industry continues moving towards DC systems in pursuit of higher efficiency, reliability, and autonomy, the proposed EZD method offers an inside look into the state of the system. It provides solutions to some of the main gaps in DC systems research.

8.1.1 Improve Transient and Stability

Chapter 3 introduced the use of the EZD method to characterize the equivalent load seen by a PEC and its incremental behavior to adapt the controller. The presence of non-linear constant power loads (CPLs) introduces a negative incremental resistance that is highly detrimental to the performance of power electronics systems. The traditional approach of tuning the PEC for the worst-case load is not always optimal, as the performance for mixed loads is unpredictable. The proposed algorithm uses the measured impedance to adapt the controller and obtain reliable performance for an extended variation of the load condition.

The adaptive control technique introduced in this chapter allowed the real-time adjustment of the controller coefficients to obtain a reliable response under changing load conditions. The simulations showed a comparison against the fixed controller schemes tuned for different
operating points showing better performance and matching the fixed cases for each condition. The proposed controller reduced overshoot from 15% to 2.5%, while maintaining convergence time and extending the range of CPL that can be tolerated when compared with fixed tuned controllers.

### 8.1.2 Islanding Detection

Chapter 4 introduced the incremental impedance-based IDM in DC systems. Without the phase and frequency information present in AC grids, ID is challenging in DC systems. The proposed method used the small signal injected and detected the change between the grid-connected scenario (very low incremental impedance) and the islanded scenario (large incremental impedance). The method was studied for different types of loads, including passive loads, constant power loads, and constant current loads, showing very high sensitivity to the change. The proposed IDM allowed a smooth transition between islanded and grid-tied mode, allowing flexible operation of the microgrid.

The proposed method offers significant advantages when compared with the current methods: Over-Voltage/Under-Voltage (UV/OV) and perturbation injection. Voltage based methods fail in closely matched source-load conditions (which is a desirable operating mode, as it minimizes energy transactions). Perturbation injection methods inject increasingly larger deviations to the set-point which deviates the system from equilibrium. The proposed IDM uses a reference signal of 1% the amplitude of the DC current and is able to detect the islanding event in less than the time constant of the output filter.

### 8.1.3 Low-Impedance Fault Location

Chapter 5 introduced the use of the EZD method for locating Low Impedance Faults (LIFs) in a DC microgrid using the distributed generators as Power Probe Units (PPUs). Once
a LIF is detected, and the faulted section of the system is isolated, finding the distance to a LIF in the system is essential to speed up repairs. The proposed method builds on the EZD to measure the resistance and inductance seen by the source-end PEC and estimate the distance based on this. The use of the proposed method allows the use of the reactance, which is less sensitive to errors due to fault resistance, and the load resistance.

In the event of a fault further away than the load, the proposed method benefits from being able to be embedded in all the source-end PECs in the system. The system can be taken to a configuration that reduces the error and use any of the distributed PECs.

The adoption of the proposed EZD-based fault location technique removes the need for expensive additional equipment, such as external PPUs or smart relays to locate the fault in the system. The use of external PPUs needs human intervention (and is therefore expensive and time-consuming); smart relays are costly and require a communication lifeline to work. The proposed algorithm uses the same sensors present in the PEC and needs no high-speed communications link, making it more convenient to distribute the control of the microgrid. Simulations show the algorithm at work for different fault scenarios, and the location capabilities are validated through experimental results.

8.1.4 High-Impedance Fault Detection

Chapter 6 introduced the use of the EZD method to detect High Impedance Faults (HIF) in point-to-point DC systems. As opposed to LIFs, HIFs do not trip the OCP and are often confused with load changes. This can lead to HIF being maintained for a long time. By detecting the incremental impedance and comparing its change through time, it is possible to differentiate a load change from a fault condition.

The proposed method benefits from the nature of the active loads (having non-linear V-I characteristics) and the faults being mainly resistive. This difference yields a qualitative difference between a change in the load (positive change) and a fault condition (negative
change). Simulations and experimental results showed the performance of the algorithm and its sensitivity.

8.1.5 Photovoltaic Maximum Power Point Tracking

Chapter 7 presented a solution to the problem of tracking the Maximum Power Point of a Photovoltaic panel, dubbed LIA-InCond, using the proposed EZD method. The proposed algorithm goes beyond the standard implementation of the EZD method and the state of the art MPPT algorithms by avoiding injecting a reference signal at all. Instead, the LIA-InCond uses the inherent ripple introduced by switching PECs as its reference signal and extracts the incremental conductance every switching cycle. This reference signal requires computing a reduced version of the proposed EZD method several times per switching cycle.

This proposed solution solves some of the main issues in MPPT algorithms and eliminates the need for voltage or current controllers in the PEC. The MPPT algorithm makes impedance matching the primary goal through an integral controller, allowing for variable speed tracking and accurate direction detection - a solution to two of the major drawbacks of most MPPT algorithms. The combination of these characteristics produced: 1) no oscillation in steady-state maximizing the transferred power, 2) start-up tracking 40 times faster than the standard InCond, and 3) irradiance change identification and tracking within 98% accuracy for variable change rates.

The proposed algorithm was validated by performing computer simulations to show the benefits and compare it with the standard InCond as a benchmark. Further validation was performed using an experimental platform showing not only the same advantages but also the feasibility of using the ripple as the scanning signal with standard microcontrollers and sensors. Finally, the performance and features of the PEC were compared against several modern algorithms proposed in literature showing the ability of the proposed method to
achieve above 98% tracking efficiency using only a single control loop, no additional sensors, no injected reference, and needing to device-specific tuning.

8.1.6 Specific Academic Contributions

The following publications introduced the Embedded Impedance Detection in a DC microgrid scenario to characterize the equivalent load and improve the stability of the system:


The work on using the embedded impedance detection to identify the islanding condition in a DC microgrid for diverse sets of loads was published in:


The work on low-impedance fault location was published in:


The work to use the embedded impedance detection to differentiate a high-impedance fault from a load step-up in a point-to-point DC system is accepted in:

The work on Maximum Power Point Tracking (MPPT) for Photovoltaic systems culminated with the following publications:


These publications cover a preliminary implementation of the LIA-InCond using the standard Embedded Impedance Detection Method, as well as the perturbationless version.

Some publications resulted from collaborative research around photovoltaic systems, DC microgrid systems, and MPPT for other applications:


• G. Bogado, F. Paz, I. Galiano Zurbriggen, and M. Ordonez, “Optimal Sizing of a PV and Battery Storage System Using a Detailed Model of the Microgrid for Stand-


8.2 Future Work

This body of work opens many new lines of research. Some open problems that could be addressed using the proposed EZD method include:

• **Investigating the use of the EZD for battery energy storage:** Impedance is an indicator of the State of Charge (SoC) and State of Health (SoH) of batteries. Online characterization is challenging, as it is highly sensitive to the chemistry of the battery, temperature, and aging; however, it can yield promising results.

• **Arc Fault detection and characterization:** During an Arc Fault event, impedance increases rapidly and has a wide frequency spectrum. An extension of the EZD that monitors multiple frequencies would be needed to allow this application.

• **Extending Fault Detection and Location to other architectures:** Extending the algorithm to work with different architectures (radial and interconnected) would allow it to work in different systems such as data centers and electric ships. This is challenging as the existence of multiple paths can mask some of the effects.

• **Maximum Power Point Tracking for other renewable energy sources:** the EZD-based MPPT developed for photovoltaic systems can be extended to other systems such as wind and ocean turbines. Research needs to be carried out to implement impedance analogies for electromechanical systems.

• **Implementing the impedance detection in non-energy producing nodes:** with the advances in PECs, microgrid architectures that use PECs at different stages, such as
power routers and smart nodes, are becoming a possibility. These nodes sacrifice efficiency in exchange for controllability and protection of the system; building the EZD can give extra information to these nodes.


