On the Design of High-Performance mm-Wave CMOS VCOs

by

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Abstract

The increasing demand for higher data rates in wireless communication such as IEEE 802.15.3c wireless personal area networks (WPANs), wireless local area networks (WLANs), and next generation wireless systems, have made the development of radio-frequency (RF) and millimeter-wave (mm-wave) frequency integrated circuits (ICs) that operate in few tens of gigahertz more popular. In the context of high data rate wireless systems, the 5th generation (5G) of wireless systems is expanding its operation frequency to millimeter wave (mm-wave) bands where more signal bandwidth are available.

To implement such circuits, the preferred technology is CMOS (complementary metal-oxide semiconductor) since compared to other technologies, it offers lower supply voltage, lower cost, higher levels of integration, and potentially lower power. Many CMOS solutions for RF and mm-wave applications have been proposed over the past few years and thanks to continuous reductions in feature size of CMOS devices into deep-submicron range, many efficient and high performance state-of-the-art RF and mm-wave receivers have been reported. However, efficient system integration at mm-wave frequencies in CMOS is still a challenging task.

Voltage-controlled oscillators (VCOs) are indispensable in the operations of fully integrated transceiver architectures. In many cases, quadrature local oscillator (LO) signals are required for frequency conversion. Major challenges in particular in portable applications include the generation of such quadrature phase outputs with low power consumption. This also applies to emerging mm-wave applications, where one would like to achieve a wide tuning range while maintaining low-power consumption and low phase noise. In this work, we investigate several design techniques for achieving a high performance wireless receiver building block with a specific focus on LC-based VCOs.

Based on the measurement results, one of the VCOs achieves an average PN of −111.9 dBc/Hz at 10 MHz offset over the entire frequency tuning range, and a TR of ~18%, from 50.1 to 59.8 GHz, resulting in a figure of merit incorporating the tuning range (FOM_T) of –184 dBc/Hz. The VCO core consumes 6.2 mW from a 1-V supply and excluding the pads occupies a compact silicon area of 0.06 mm^2.

Lay Summary

This thesis summarizes our efforts to further improve the performance of mm-wave signal sources that are implemented in Complementary Metal-Oxide-Semiconductor (CMOS) technology so they can achieve lower phase noise, wider tuning range, lower power consumption, and more compact chip area. The proof-of-concept prototypes are implemented in a cost-effective CMOS technology to facilitate the mm-wave operation (28 GHz and 60 GHz) for the fifth generation (5G) of communication systems and other high data-rate wireless systems, as well as medical, security and internet-of-things (IoT) applications. We have designed and implemented the proposed integrated oscillators using a 65-nm CMOS process and have experimentally validated the performance of the circuits.

Preface

I, Milad Haghi Kashani, am the principal contributor of all chapters of this dissertation. Professor Shahriar Mirabbasi has supervised the research by providing financial support, technical consultation, and editing assistance on the manuscript. During my Masters studies, we have collaborated with a number of scholars and research groups as reflected in publication list below. I confirm that I have completed all the research in the following papers by myself. I just would like to thank Prof. Ehsan Afshari, Dr. Reza Molavi, Dr. Amirahmad Tarkeshdouz, and Dr. Hormoz Djahanshahi for their technical discussion and help in writing and revising the manuscripts. Please find below the list of the published works which some of them have been used as the main chapters of this thesis:

Conferences:

[1] M. H. Kashani, R. Molavi and S. Mirabbasi, "A Wide-Tunning-Range Low-Phase-Noise Colpitts Oscillator with Variable Capacitive Feedback," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, May 2018, pp. 1-5.

[2] M. H. Kashani, R. Molavi, H. Djahanshahi and S. Mirabbasi, "On the Design of Vertical-Turn Solenoids for Magnetically Isolated Densely Integrated LC Oscillators," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, May 2018, pp. 1-5.

[3] M. H. Kashani, A. Tarkeshdouz, E. Afshari, and S. Mirabbasi, "A 60-GHz CMOS Down-Conversion Mixer with High Conversion Gain and Low Noise Figure," *16th IEEE International NEWCAS Conference*, Montreal, Canada, June 2018, pp. 1-4. **Recipient of Regroupement Stratégique en Microsystème du Québec (ReSMiQ) Best Paper Award.**

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[4] M. H. Kashani, A. Tarkeshdouz, R. Molavi, E. Afshari, and S. Mirabbasi, "A Wide-Tuning-Range Low-Phase-Noise mm-Wave CMOS VCO with Switchable Transformer-based Tank," *IEEE Solid-State Circuits Letters*, vol. 1, no. 3, pp. 66-69, June 2018.

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List of Abbreviations

CMOS	**Complementary Metal-Oxide Semiconductor**
CPW	**Coplanar Wave Guide**
FOM	**Figure of Merit**
FTR	**Frequency Tuning Range**
GCPW	**Grounded Coplanar Wave Guide**
g_m	**Transconductance**
IF	**Intermediate Frequency**
IC	**Integrated Circuit**
LO	**Local Oscillator**
PN	**Phase Noise**
THz	**Terahertz**
TR	**Tuning Range**
VCO	**Voltage Control Oscillator**
V_{GS}	**Gate-to-Source voltage**
V_{OV}	**Overdrive Voltage**
V_{th}	**Threshold Voltage**

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TO MY FAMILY

Fin Garden, Kashan , Iran

Chapter 1. Introduction

1.1. Motivation

The surge in demand for high data-rate communication in wireless standards such as IEEE 802.15.3c wireless personal area networks (WPANs) and next generation wireless systems has attracted considerable attention toward development of integrated circuits and systems that operate in mm-wave frequencies [1]–[4]. In particular, the availability of an increased signal bandwidth has been the major drive for the 5th generation (5G) of wireless systems to extend their operation frequency to mm-wave bands. Although the frequency band for 5th-generation wireless systems has not been completely specified yet, the unlicensed 28-GHz and 60-GHz frequency bands are amongst the most promising candidates for such systems in many countries [5].

The millimeter-wave frequency range is prominent and necessary for basic and fundamental applications as it consists molecular vibration frequencies and absorption bands of the atmosphere and common materials. This frequency range is also useful for technological applications, such as imagers, radars, security, and medical applications. Imaging at these frequencies can be used to detect concealed weapons or explosives and reveal features in skin, teeth, and solid organs. Millimeter-wave imagers are considered as a superior alternative as compared to traditional metal detectors, since the reflection pattern of metals, plastics, ceramics and liquids are detectable quickly for radiation at these frequencies [6-8]. The function of radars is to measure the distance or speed of aircrafts, ships, automotive vehicles, and many other moving objects. Hence, the security domain facilitates one of the major areas for millimeter-waves imaging systems [3]. Another advantage of mm-wave ICs is the possibility of integrating the antenna. Because of the short wave length any interconnection with the antenna will constitute a huge parasitic element. This may cause the circuit to work improperly while it can be addressed by designing on-chip

antenna and transmission lines. Although on-chip antennas have been designed and fabricated before, they have not been introduced commercially.

To implement such circuits, the preferred technology is CMOS (complementary metal-oxide semiconductor) since as compared to other technologies, it offers low supply voltage, low power, low cost, and high levels of integration (with possibility of integrating analog and digital functionality on the same chip) [4]. Research during the past decades provided CMOS solutions to RF and mm-wave applications. For decades, CMOS technology has dominated digital and mixed-signal ICs because of its good switching performance and low cost. CMOS technology also takes the advantages for RF and millimeter-wave circuits and systems. In addition, high-frequency circuits can be digitally controlled and calibrated [9].

Despite great advances, there are still existing bottlenecks in CMOS designs as they need to be addressed. In other words, many challenges and limitations to CMOS technology should still be alleviated to realize millimeter-wave circuits and systems. The cut-off frequencies (f_T , f_{max}) are relatively lower than for other technologies [6]. The low breakdown voltages limits the supply voltage and AC voltage swings for reliability [2-5]. In addition, passive devices suffer from high losses and low quality factors. As the technology is scaled down, the thickness and the elevation of the metals also shrink, which increases the losses in inductors and transmission lines. In this work, we are doing our best to address those challenges and unsolved problems and push the boundaries of cost-effective electronics further toward higher speed data-rates and lower power consumption.

1.2. Organization

With abovementioned motivations, the objective of this research is to study and design the following building blocks in a cost-effective CMOS process that can be used in high-performance mm-wave communication systems such as 5G systems:

1) Low-Phase-Noise Wide-Tuning-Range 60-GHz CMOS VCO (Chapter 2)

2) Low-Power Wide-Tuning-Range 28-GHz CMOS VCO (Chapter 3)

As a proof-of-concept, for each building block, a test chip is designed, fabricated, successfully measured, and its performance is compared with the related state-of-the-art designs. The CMOS process that is used is 65-nm which provides a good cost-performance trade-off for designs that are operation in the abovementioned frequency bands.

1.2.1. mm-Wave Signal Generation in CMOS Technology

The development of the integrated circuits (ICs) operating at millimeter-wave (mm-wave) frequencies has become very popular over the past few years. This popularity is the corollary of the increasing demand for high data-rate communication standards such as IEEE 802.15.3c wireless personal area network (WPAN). In addition, the 5th generation of wireless systems (5G) has extended its operation frequency to mm-wave band, where an increased signal bandwidth is available [1]. Voltage-controlled oscillators (VCOs) are amongst the essential building blocks required for operation of integrated mm-wave transceivers. One of the challenges associated with designing mm-wave VCOs is to generate a wide-band, low-phase-noise signal while maintaining low power consumption.

With recently commercialized 5G cellular network, researches are looking for mm-wave and more specifically 60-GHz frequency bands, aiming for up to 10 Gb/s for wireless communication [8-10]. The signal integrity in general and the phase noise (PN) performance of the receiver or transmitter clock in particular is necessary for any high performance communication system. Most of previous researches and analytical calculations on phase noise have been focused on low RF frequency bands and in some cases they make certain assumptions which are not valid at mm-

wave bands [11]. As an illustration, the effect of non-linear transistor capacitors are neglected. Although these capacitances have just second-order effects on the noise performance at low frequencies, at mm-wave frequencies, any small variation in these capacitances can directly or indirectly impact PN. Signal generation at mm-wave frequencies is a major challenge in solid-state electronics due to the limited transit frequency (which is the frequency at which the current gain is unity), f_T, maximum oscillation frequency (which is the frequency at which the power gain is unity), f_{max}, breakdown voltage of active devices and the lower quality factor of passive components resulted by ohmic and substrate loss [6].

1.3. Thesis Outline

This thesis is organized as follows:

1. Investigation and implementation of low-phase-noise wide-tuning-range mm-wave oscillator design are presented in Chapter 2.
2. Investigation and implementation of low-power wide-tuning-range mm-wave oscillator design are presented in Chapter 3.
3. Measurement results of the fabricated prototypes are presented in Chapter 4.
4. Conclusion remarks are presented in Chapter 5.

Chapter 2. A Low Phase-Noise Wide-Tuning-Range mm-wave CMOS VCO.

2.1. Introduction and Overview of Recently Published Works

The availability of wide bandwidth in the mm-wave portion of the frequency spectrum makes these bands attractive for high-data-rate applications such as wireless high-definition video streaming and medical imaging [2]–[4]. One of the main challenges in most communication systems operating in the 60 GHz and higher frequency bands is to synthesize an on-chip local oscillator (LO) with a high spectral purity and a large tuning range.

Several techniques have been reported to improve the tuning range of different mm-wave VCO topologies [7][8][9]. Capacitive tuning methods are not suitable at mm-wave frequencies due to the degraded quality factor (Q) of capacitors [7]. Alternatively, inductive tuning methods have been introduced to overcome the aforementioned challenges [7][8][9]. An inductor loaded transformer is designed in [7] with switches placed at different locations on the secondary coil to increase the number of sub-bands, and the resulting tuning range. However, the relatively large number of switches required for symmetric implementation increases the contributed parasitic capacitance. Furthermore, the parasitics of off switches on the secondary coil still affects the overall performance. In [8], switchable coupled VCO cores are designed to realize a dual mode operation at the cost of a higher power consumption and larger area; the design also suffers from a low output power. In [9], switched inductors are utilized to change the effective inductance of the tank, thereby extending the tuning range at the cost of a relatively large area and high power consumption.

In [4] the size of the varactor is reduced to improve the tank quality factor and the VCO oscillation frequency is varied by the drain capacitance of the MOS device facilitated by using the body effect.

However, this design suffers from a narrow (below 5%) frequency tuning range due to the small size of varactor. A large FTR (~28%) is achieved in [10] by utilizing dual-mode LC-tank. However, the figure-of-merit (FOM) and phase noise performance is degraded due to the use of a complex inductor structure and in turn sacrificed tank quality factor which deteriorates the moise performance. Another interesting technique is to increase the f_{max} and the transconductance of the cross-coupled pair by using inductive peaking at the gate of MOS devices [3]. This technique enhances the phase noise while still utilizing an explicit MOS varactor. However, achieving a compromise trade-off between the phase noise, power consumption, and FTR is still a challenge.

The inductive tuning method introduced in [7] also extends the tuning range. The inductor loaded transformer designed in [7] uses switches placed at different locations on the secondary coil to increase the number of sub-bands, and the resulting tuning range. However, the relatively large number of switches required for symmetric implementation increases the parasitic capacitance. As the number of switches increases, the total load capacitance (resistance) reflected back to the primary of the transformer increases (decreases). Furthermore, the parasitics of switches that are off still affects the performance. Due to these parasitics the structure has a relatively narrower frequency tuning range. In this work, we not only use less number of switches but also present a design approach which is based on the mutual coupling between the auxiliary coils. The proposed approach lowers the loading effect of the parasitics of switches when reflected back to the primary side, which in turn results in a wider tuning range and lower phase noise than those of [7]. In chapter 2, we will also show that by increasing the coupling factor among the loads the adverse effects of loading are reduced and thus lower loss and better phase noise can be achieved. The improved coupling is facilitated by proposing a transformer structure that uses three layers of metals to achieve a 3D transformer structure.

In this chapter, we propose a design technique for a mm-wave VCO architecture which incorporates a switchable transformer topology to extend the tuning range with minimal adverse effects on the phase noise performance and area. The switches in the secondary and tertiary coils are implemented differentially to reduce the on-state resistance that negatively affects the phase noise. Moreover, employing a three-dimensional (3D) implementation of the transformer, i.e., each coil is laid out in a different metal layer, the mutual coupling factors, especially one between the secondary and tertiary coils, are improved leading to lower the loading effect of the auxiliary sides on the primary coil. Given that NMOS Class-C VCOs typically have a better performance in terms of power consumption and phase noise compared to traditional cross-coupled LC-VCOs [11], we select this structure for the core oscillator. The proposed VCO offers a compact size, wide tuning range, and low phase noise. The rest of this chapter is organized as follows; Sections II and III describe the proposed technique and the VCO implementation, respectively. Measurement results are presented in Section IV and concluding remarks are provided in Section V.

2.2. Proposed Inductive Tuning Method [12]

The proposed inductive tuning technique benefits from a switchable transformer topology that is comprised of three magnetically coupled inductors two of which are terminated by switches. In this method, by turning these switches on and off, the magnetic flux passing through the primary coil is varied, leading to a change in the effective inductance seen at the primary side. Because of the presence of the two switches, four frequency sub-bands are achieved as a result of turning the auxiliary coils on and off. In this setting, the fine tuning is realized by varactors to continuously cover the sub-bands introduced by the proposed inductive tuning method.

To have a design guideline, a simplified model for the proposed inductive tuning method considering all the possible switching states is shown in Fig. 1. In this figure, k_{ij}, R_{si}, C_{off}, and R_p

represent the coupling factor between the corresponding i^{th} and j^{th} coils, the loss (i.e., series resistance) of the i^{th} inductor, the off-state parasitic capacitance of the switch, and the on-state resistance of the switch, respectively. To analyze the circuits shown in Fig. 1, without loss of generality, the following simplifying assumptions are considered; (i) the off-state resistance and on-state parasitic capacitance of the switches are negligible. (ii) The loss of the secondary and tertiary coils are assumed to be the same ($R_{S2} = R_{S3} = R_S$), and (iii) the mutual inductance between the secondary and primary coils is the same as that of the tertiary and primary coils ($M_{12} = M_{13} = M$).

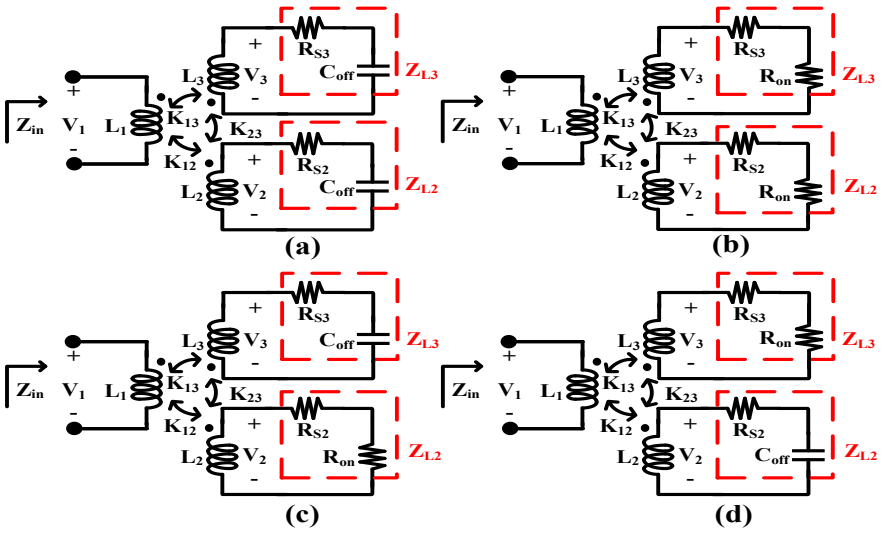

Figure 1. The simplified model for the proposed inductive tuning technique; (a) SW1 and SW2 are off; (b) SW1 and SW2 are on; (c) SW1 is on and SW2 is off; (d) SW1 is off and SW2 is on.

The simple model of the proposed transformer is shown in Fig. 1. Note that this circuit model consider the high frequency loss which is summarized in R_{Si}. As mentioned earlier, the objective of using the simplified model is to provide some insights and intuitions on the advantages of the proposed technique. The high-frequency effects (parasitics) will definitely affect the performance, however, including them when we just want to motivate the idea will complicate the derivations and perhaps will cause more confusion.

To validate the effectiveness of the proposed transformer, consider the simplified model of a non-ideal transformer shown in Fig. 2.

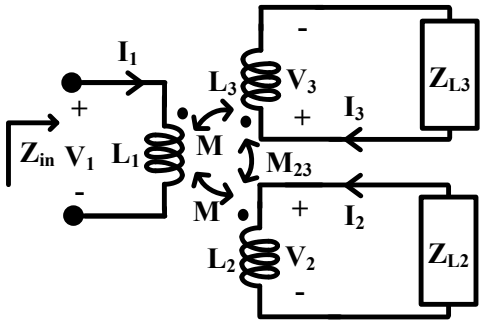

Figure 2. Simplified schematic of the proposed transformer.

According to Fig. 2, we have;

$$V_1 = j\omega L_1 I_1 + j\omega M I_2 + j\omega M I_3 \tag{1}$$

$$V_2 = j\omega M I_1 + j\omega L_2 I_2 + j\omega M_{23} I_3 \tag{2}$$

$$V_3 = j\omega M I_1 + j\omega M_{23} I_2 + j\omega L_3 I_3 \tag{3}$$

$$V_2 = -Z_{L2} I_2 \tag{4}$$

$$V_3 = -Z_{L3} I_3 \tag{5}$$

Then, from Eq. (2) to (5), we have;

$$I_3 = I_2[\frac{j\omega L_2 + Z_{L2} - j\omega M_{23}}{j\omega L_3 + Z_{L3} - j\omega M_{23}}] = T_1 I_2 \tag{6}$$

By substituting Eq. (6) in (1),

$$I_2 = [\frac{-j\omega M}{j\omega L_2 + Z_{L2} + j\omega M_{23} T_1}] I_1 = T_2 I_1 \tag{7}$$

where T_1 and T_2 are defined as;

$$T_1 = \frac{j\omega L_2 + Z_{L2} - j\omega M_{23}}{j\omega L_3 + Z_{L3} - j\omega M_{23}} \tag{8}$$

$$T_2 = \frac{-j\omega M}{j\omega L_2 + Z_{L2} + j\omega M_{23} T_1} \tag{9}$$

By substituting Eq. (6) and (7) in (1), the input impedance of Z_{in} can be found as;

$$Z_{in} = j\omega L_1 + j\omega M T_2 (1 + T_1) \Rightarrow \tag{10}$$

$$Z_{in} = j\omega L_1 + \frac{\omega^2 M^2 (j\omega L_2 + j\omega L_3 + Z_{L2} + Z_{L3} - j2\omega M_{23})}{\omega^2 {M_{23}}^2 - \omega^2 L_2 L_3 + Z_{L2} Z_{L3} + j\omega L_2 Z_{L3} + j\omega L_3 Z_{L2}} \tag{11}$$

Note that equation (10) (when expanded to (11)) is symmetric with respect to L_2 and L_3 and is valid for all switch states. However, the simplifying assumptions, which are valid and applicable in the frequency band of interest, mentioned next may affect the symmetry of the equations.

In the case where both switches are on, Z_{L2} and Z_{L3} are equal to (R_S+R_{ON}). This term is relatively small and is negligible as compared to other terms in both the numerator and denominator of Eq. (8), and thus T_1 becomes,

$$T_1 \approx \frac{L_2 - M_{23}}{L_3 - M_{23}} \tag{12}$$

Then, the input impedance in this case is calculated as,

$$Z_{in} \approx j\omega L_1 + \frac{\omega^2 M^2}{j\omega L_2 + Z_L + j\omega M_{23} T_1} (1 + T_1) \tag{13}$$

Next, defining A and B as;

$$A = \frac{[L_2 + L_3 - 2M_{23}]}{L_3 - M_{23}} \tag{14}$$

$$B = M_{23} \times \frac{L_2 - M_{23}}{L_3 - M_{23}} \tag{15}$$

The final equation of the input impedance can be written as;

$$Z_{in} \approx j\omega L_1 + \frac{A.\omega^2.M^2}{(R_S + R_{ON}) + j\omega(L_2 + B)} \tag{16}$$

Equation (16) is not symmetric with respect to L_2 and L_3 (it can be shown that it has a symmetric imaginary part while its real part is not symmetric), however, in the frequency band of interest (16) offers a good approximation of the original equation which is symmetric.

In the case where both switches are off, Z_{L2} and Z_{L3} are equal to $(R_S - \frac{j}{\omega C_{off}})$. Given that the quality factors are high, R_S can be neglected as compared to other terms. Thus, the simplified T_1 becomes,

$$T_1 \approx \frac{L_2 - (\omega^2 C_{off})^{-1} - M_{23}}{L_3 - (\omega^2 C_{off})^{-1} - M_{23}} \tag{17}$$

Then, the input impedance in this case can be calculated as;

$$Z_{in} \approx j\omega L_1 + \frac{\omega^2 M^2}{j\omega L_2 - j(\omega C_{off})^{-1} + j\omega M_{23} T_1}(1 + T_1) \tag{18}$$

Again, By defining A' and B' as;

$$A' = \frac{[L_2 + L_3 - 2(\omega^2 C_{off})^{-1} - 2M_{23}]}{L_3 - (\omega^2 C_{off})^{-1} - M_{23}} \tag{19}$$

$$B' = M_{23} \times \frac{L_2 - (\omega^2 C_{off})^{-1} - M_{23}}{L_3 - (\omega^2 C_{off})^{-1} - M_{23}} \tag{20}$$

In this case, the input impedance can be written as;

$$Z_{in} \approx j\omega L_1 + \frac{A'.\omega^2.M^2}{j\omega(L_2 + B') - j(\omega C_{off})^{-1}} \tag{21}$$

This equation is indeed symmetric with respect to L_2 and L_3.

In the case where SW_1 is on and SW_2 is off, we have $Z_{L2} = R_{on} + R_S$ and $Z_{L3} = \frac{1}{j\omega C_{off}} + R_S$. Thus, the input impedance of Z_{in} (please refer to Eq. (10)) can be found as;

$$Z_{in} = j\omega L_1 + \frac{\omega^2 M^2}{j\omega L_2 + (R_{on} + R_S) + j\omega M_{23} T_1}(1 + T_1) \tag{22}$$

where T_1 is defined as;

$$T_1 \approx \frac{L_2 - M_{23}}{L_3 - (\omega^2 C_{off})^{-1} - M_{23}} \tag{23}$$

Thus, the equivalent inductance and resistance can be found as;

$$L_{eq} \approx L_1 - \frac{\omega M^2}{\omega L_2 + \dfrac{\omega^2 M_{23}(L_2 - M_{23})}{\omega L_3 - (\omega C_{off})^{-1} - \omega M_{23}}} \cdot \frac{L_2 + L_3 - 2M_{23} - (\omega^2 C_{off})^{-1}}{L_3 - (\omega^2 C_{off})^{-1} - M_{23}} \tag{24}$$

$$R_{eq} \approx \frac{\omega^2 M^2}{(\omega L_2 + \dfrac{\omega^2 M_{23}(L_2 - M_{23})}{\omega L_3 - (\omega C_{off})^{-1} - \omega M_{23}})^2} \cdot \frac{L_2 + L_3 - 2M_{23} - (\omega^2 C_{off})^{-1}}{L_3 - (\omega^2 C_{off})^{-1} - M_{23}} \cdot (R_S + R_{on}) \tag{25}$$

Equation (25) indicate that the coupling of the third coil still impacts the equivalent quality factor at the primary even when the switch is off. The additional terms containing M_{23} in (25) is manipulated to further lower R_{eq} in this sub-band. Similar behavior can be seen for the remaining sub-bands.

The assumption of M_{12}=M_{13}=M was made as it greatly simplifies the expressions and also in the implemented prototype, the values of M_{12} and M_{13} are indeed close to each other. However, this is not a necessary design choice and in general M_{12} and M_{13} can be different. Eqs. (24) and (25) represent the case where the secondary coil is shorted and the tertiary one is open. For the other case where the secondary coil is open and the tertiary one is shorted, we have;

$$Z_{L2} = \frac{1}{j\omega C_{off}} + R_S \tag{26}$$

$$Z_{L3} = R_S + R_{ON} \tag{27}$$

Thus, the equivalent inductance and resistance can be found as;

$$L_{eq} \approx L_1 - \frac{\omega M^2}{\omega L_3 + \frac{\omega^2 M_{23}(L_3 - M_{23})}{\omega L_2 - (\omega C_{off})^{-1} - \omega M_{23}}} \cdot \frac{L_2 + L_3 - 2M_{23} - (\omega^2 C_{off})^{-1}}{L_2 - (\omega^2 C_{off})^{-1} - M_{23}} \tag{28}$$

$$R_{eq} \approx \frac{\omega^2 M^2}{(\omega L_3 + \frac{\omega^2 M_{23}(L_3 - M_{23})}{\omega L_2 - (\omega C_{off})^{-1} - \omega M_{23}})^2} \cdot \frac{L_2 + L_3 - 2M_{23} - (\omega^2 C_{off})^{-1}}{L_2 - (\omega^2 C_{off})^{-1} - M_{23}} \cdot (R_S + R_{on}) \tag{29}$$

By comparing Eqs. (28) and (24) and considering that L_2 is not equal to L_3, we can conclude that the center frequency of the second and third sub-bands are different. It is worth noting that in our design L_2 and L_3 (and also k_{12} and k_{13}) are not equal, however, M_{12} is approximately equal to M_{13}. Refer to Eq. (10), the input impedance at the primary coil becomes,

$$Z_{in} = j\omega L_1 + \frac{\omega^2 M^2}{j\omega L_2 + Z_{L2} + j\omega M_{23} T}(1+T) \tag{30}$$

where ω is the frequency and T defined as:

$$T = \frac{j\omega L_2 + Z_{L2} - j\omega M_{23}}{j\omega L_3 + Z_{L3} - j\omega M_{23}} \tag{31}$$

Fig. 1(b) illustrates the case in which both switches are on. In this circuit, taking into account assumption (ii), we have $Z_{L2} = Z_{L3} = Z_L$. Substituting Z_L by $(R_{on} + R_S)$, the equivalent inductance and resistance seen by the primary coil are written as;

$$L_{eq} \approx L_1 - \frac{\omega^2 M^2 . (1 + \frac{L_2 - M_{23}}{L_3 - M_{23}}) . (L_2 + M_{23} . \frac{L_2 - M_{23}}{L_3 - M_{23}})}{(R_S + R_{on})^2 + \omega^2 (L_2 + M_{23} . \frac{L_2 - M_{23}}{L_3 - M_{23}})^2} \approx L_1 - C_2 \tag{32}$$

$$R_{eq} \approx \frac{\omega^2 . M^2 . (1 + \frac{L_2 - M_{23}}{L_3 - M_{23}}) . (R_S + R_{on})}{(R_S + R_{on})^2 + \omega^2 (L_2 + M_{23} \frac{L_2 - M_{23}}{L_3 - M_{23}})^2} \approx (R_S + R_{on}) . C_1 \tag{33}$$

where C_1 and C_2 are defined as;

$$C_1 = \frac{M^2\left(1+\frac{L_2-M_{23}}{L_3-M_{23}}\right)}{\left(L_2+M_{23}\frac{L_2-M_{23}}{L_3-M_{23}}\right)^2} \tag{34}$$

$$C_2 = \frac{M^2\left(1+\frac{L_2-M_{23}}{L_3-M_{23}}\right)}{\left(L_2+M_{23}\frac{L_2-M_{23}}{L_3-M_{23}}\right)} \tag{35}$$

The approximations in (32) and (33) hold if $(R_{on}+R_S)$ is small compared to the second term in the denominator which is a reasonable assumption in the frequency band of interest. From (32) and (33), one can manipulate C_1 and C_2 to improve R_{eq} and in turn the resulted quality factor at the cost of a slightly degraded tuning range. Shown in Fig. 3, C_1 and C_2 are plotted versus the coupling factor between the secondary and tertiary coils (k_{23}) for given design parameters. This figure implies that an increase in the value of k_{23} drops the equivalent resistance while slightly increasing the minimum achievable inductance, thereby improving the quality factor. For instance, if k_{23} increases from 0.3 to 0.5, the equivalent resistance reduces by ~20% while the corresponding inductance increases by only ~7%.

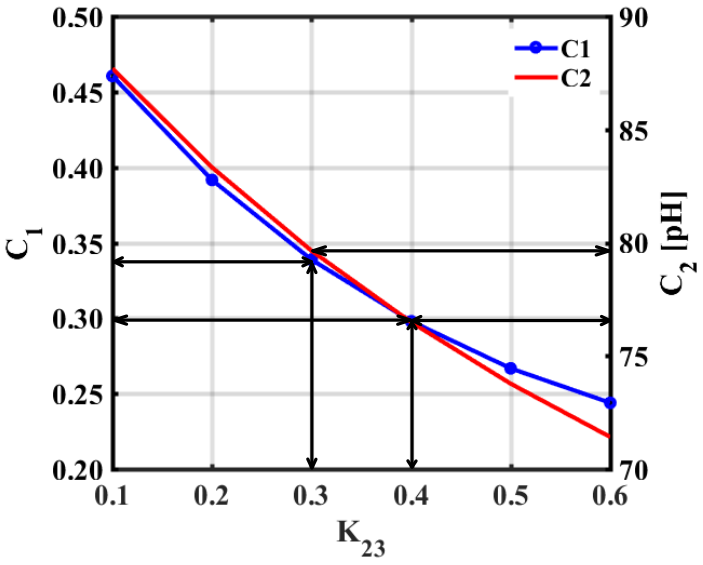

Figure 3. Plotted C1 and C2 versus k23 with L2=210 pH, L3=250 pH, and M=115 pH.

The intuitive verification of the above concept can be explained using Fig. 4 (a) and (b). This figure presents two ideal cases where $k_{23} = 0$ and $k_{23} = 1$. In Fig. 4(a), assuming $L_2 = L_3 = L$ and $Z_{L2} = Z_{L3} \approx R_{on}$, the equivalent inductance and resistance seen by the primary coil are derived as $L_{eq} = 0.5L - M$ and $R_{eq} = 0.5R_{on}$ while the corresponding values for the same parameters are obtained as $L_{eq} = L - M$ and $R_{eq} = 0.5R_{on}$ in Fig. 4(b) where $k_{23} = 1$. This clearly shows that the quality factor seen by the primary side is doubled approximately if the two circuits are perfectly coupled. This confirms our previous observation that increasing k_{23} results in improving the quality factor of the tank.

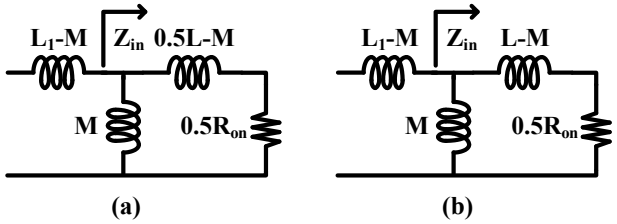

Figure 4. Simplified π-model of the transformer when; (a) K23=0. (b) K23=1.

Fig. 5 shows the schematic diagram of the cases where both switches are either on or off (that is, Z_{L2}=Z_{L3}). For simplicity, we assume that L_2=L_3=L and R_{S2}=R_{S3}=R_S. Thus, we have V_2=V_3 and I_2=I_3=I. Also, we assume that the transformer is designed such that the coupling factors are approximately the same, that is, M_{12}≈M_{13}≈M,

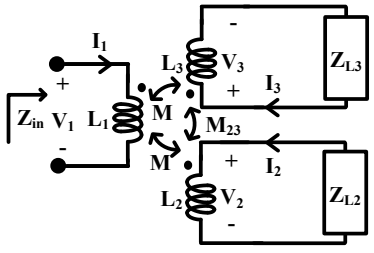

Figure 5. Simplified model of the transformer where both switches are on (or off).

we have,

$$V_1 = j\omega L_1 I_1 + j\omega M I_2 + j\omega M I_3 \tag{36}$$

$$V_2 = j\omega M I_1 + j\omega L I_2 + j\omega M_{23} I_3 \tag{37}$$

$$V_3 = j\omega M I_1 + j\omega M_{23} I_2 + j\omega L I_3 \tag{38}$$

If we assume the following equivalent circuit (Fig. 6) for three-coil structure:

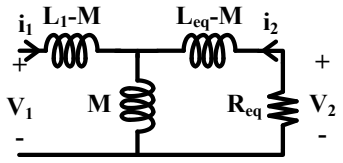

Figure 6. Simplified pi-model for one of transformers.

According to Fig. 6, we then have

$$V_1 = j\omega L_1 i_1 + j\omega M i_2 \tag{39}$$

$$V_2 = j\omega M i_1 + j\omega L_{eq} i_2 \tag{40}$$

If k_{23}=0, from Eq. (36) to (38) we have;

$$V_1 = j\omega L_1 I_1 + j\omega M (2I) \tag{41}$$

$$V_2 = j\omega M I_1 + j\omega (0.5L)(2I) \tag{42}$$

By comparing Eq. (41) with (39), and also (42) with (40), the right hand side of (42) should be equal to that of (40). Then; L_{eq}=0.5L and i_2=2I=2I_2. Also, we have $\frac{V_2}{I_2} = \frac{V_2}{I} = R_{ON}$ and $R_{eq} = \frac{V_2}{i_2}$. Considering that i_2=2I=2I_2, we can conclude that R_{eq}=0.5R_{ON}. For the other case where k_{23}=1,

$$V_1 = j\omega L_1 I_1 + j\omega M (2I) \tag{43}$$

$$V_2 = j\omega M I_1 + j\omega L (2I) \tag{44}$$

By comparing Eq. (44) with (40), and also (43) with (39), the right hand side of (44) should be equal to that of (40). Then; L_{eq}=0.5L and i_2=2I=2I_2. Also, we have $\frac{V_2}{I_2} = \frac{V_2}{I} = R_{ON}$ and $R_{eq} = \frac{V_2}{i_2}$. Considering that i_2=2I=2I_2, we can conclude that R_{eq}=0.5R_{ON}.

As mentioned earlier and also according to the aforementioned analysis, increasing the coupling factor between the loads can improve the phase noise by reducing the loading effect of the switches. To increase k_{23}, the second and third coils are implemented in different adjacent metal layers. This is to circumvent the minimum distance between two adjacent traces that are in the same metal layer (as dictated by the design rules). Furthermore, such an implementation can satisfy $M_{13} \approx M_{12} = M$ as the secondary and tertiary coils are separated from the primary coil by an approximately equal distance. Note that k_{23} is not linked to the primary coil. In other words, to increase K_{23}, instead of utilizing the same M_8 layer to implement the two auxiliary coils, we implement them in M_8 and AP. In this configuration, the minimum distance between two adjacent traces with the same metal layer, enforced by DRC, is irrelevant as the coils are on different metal layers. Therefore, the coupling factor is improved due to the smaller distance between the implemented coils. Thus, the proposed three dimensional transformer achieves a higher coupling factor as compared to the simple planar implementation. Additionally, such an implementation can satisfy M_{13}=M_{12}=M as the secondary and tertiary coils are separated from the primary coil by an approximately equal distance (in the technology used in this work). The proposed transformer is built using the topmost three metal layers. In such a configuration, as compared to planar implementation, the coupling factor is improved and the occupied area is reduced.

From (32) and (33), the equivalent inductance and resistance at the primary coil are also dependent on the values of L_2 and L_3 in addition to k_{23}. Figs. 7 and 8 show the plot of C_1 and C_2 for different values of L_2 and L_3. As can be seen from the plots, to reduce the loading effect of the switches, L_3

should increase. In other words, for a given k_{23}, increasing L_3 lowers R_{eq}. However, increasing L_3 to any arbitrary high value is not reasonable as it leads to a larger occupied area, higher parasitic capacitance, and higher loss with only marginal improvement in R_{eq} beyond a certain point. Therefore, L_3 is optimized to achieve a low phase noise while having minimal impact on the tuning range. Fig. 9 shows that k remains almost intact if the original structure of the coils is preserved even if L_3 varies.

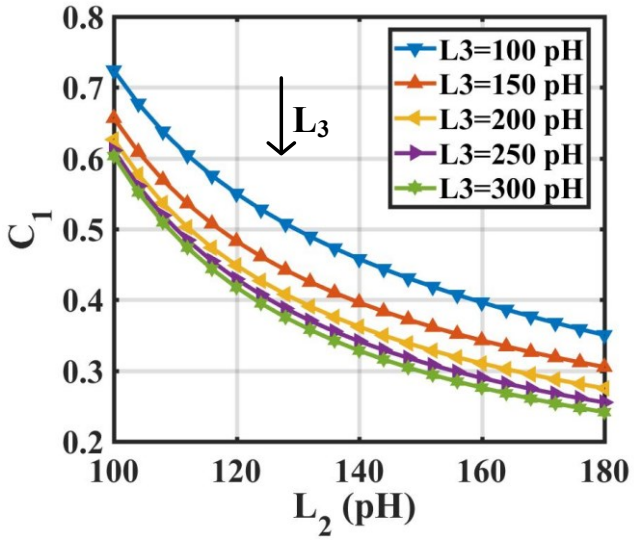

Figure 7. Simulated C_1 versus different values of L_2 and L_3.

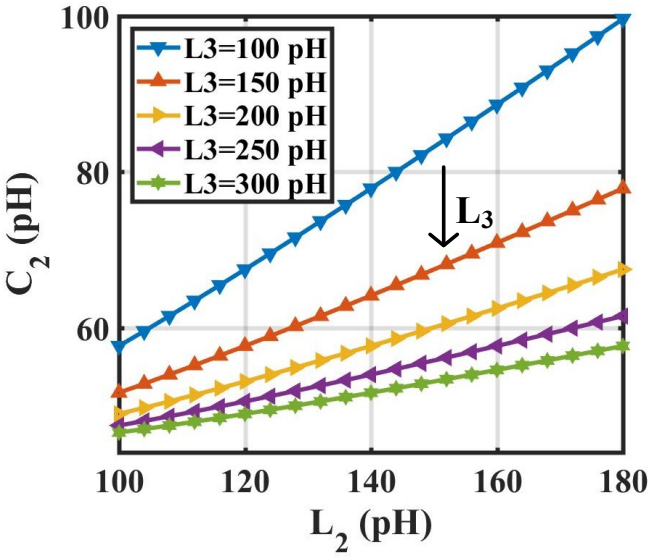

Figure 8. Simulated C_2 versus different values of L_2 and L_3.

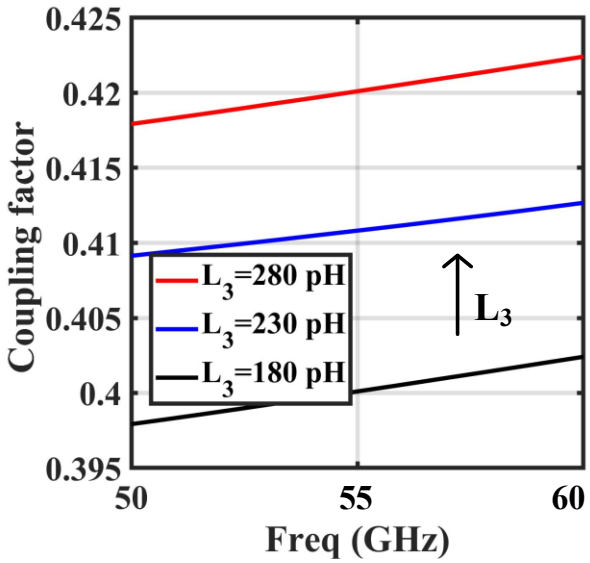

Figure 9. Dependency of the coupling factor on L_3.

2.3. Summary of The Design Procedure

The two additional coils that are added to the main (primary coil) and can be switched on or off results in 4 distinct sub-bands (off-off, on-off, off-on, and on-on states). The 4 possible states are analyzed by presenting the equivalent inductance and resistance seen by the primary coil in each state. As a summary of design procedure, after designing a conventional oscillator, the continuous frequency tuning range (FTR) in each sub-band should be determined by the varactor size (taking into account the trade-off between the TR and Q of the varactor). To implement the secondary coil, the first and third sub-bands should be considered. L_2 is chosen to satisfy the target continuous FTR. Then, L_3 should be designed to cover the gap between the 1st and 3rd sub-bands. The next step is to maximize the coupling factor between the coils especially k_{23}. The next step is to iterate (if necessary) the design parameters to meet the design specifications and optimize the performance taking into account the trade-off between the PN and TR. Based on the formulas discussed earlier, the value of L_2 and L_3 are optimized based on the width and the choice of the

metal layer for each coil. Figs. 7 and 8 can help the designer to gain an insight about the optimum value of L_2 and L_3. The value of the inductances are chosen (based on the formulas) to achieve a wide tuning range with minimal adverse effect on the phase noise. Finally, design and layout techniques are used to achieve the maximum quality factor over the desired frequency band. The quality factor and effective inductance simulation results are presented in Figs. 10 and 11, respectively.

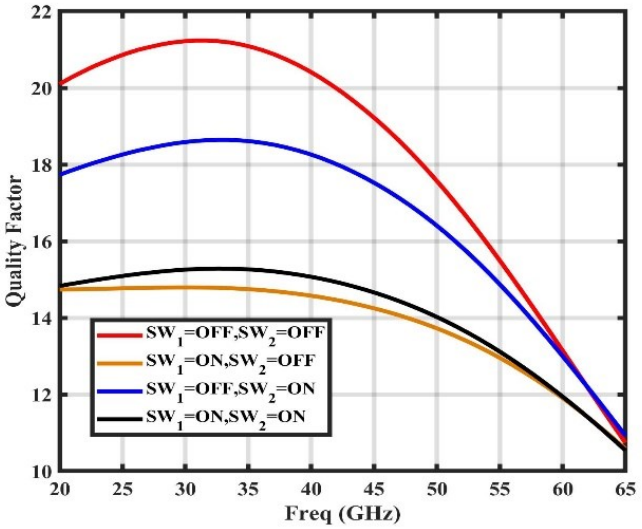

Figure 10. The simulated Q-factor over all switch states.

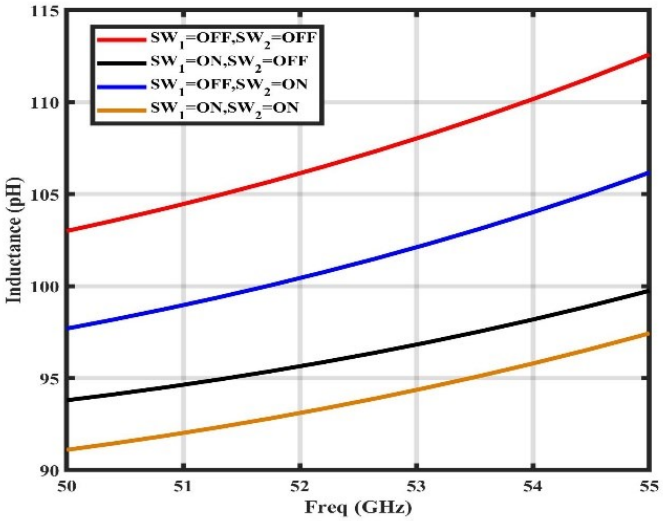

Figure 11. Simulated effective inductance over the whole frequency tuning range.

As can be seen, when both switches are off, the auxiliary coils have minimum effect on the primary coil due to the relatively high-impedance of off-state parasitic capacitance of switches, and thus, the quality factor and effective inductance in the off-off state are the highest amongst the all possible states. When SW_1 is off and SW_2 is on, the outermost coil, which is implemented by AP, is shorted while L_2 is open. This configuration achieves the second highest effective inductance and quality factor due to the higher quality factor of AP and also lower coupling factor due to larger distance to the primary coil. When SW_1 is on and SW_2 is off, because of the higher coupling factor which is the corollary of a shorter distance to the primary coil, the effective inductance of this sub-band is lower than that of the previous sub-band. However, the quality factor is the worst amongst that of other states due to the lower quality factor of M_8 and also lower effective inductance of this sub-band. Finally, for the state when both switches are on, the effect of both auxiliary coils are added to further reduce the effective inductance. The quality factor of this setting is better than that of the previous sub-band (SW_1 on and SW_2 off), because the effective inductance is reduced while the loading effect is further reduced (we can intuitively say that the loads are in parallel which in turn results in a lower loss), which reduces the Q-factor degradation. Thus, the on-on state achieves a lower effective inductance along with a larger quality factor as compared to on-off state.

Moreover, according to Fig. 10, the Q-factor differences among the four states would impact the performance. However, in our design, we are trying to reduce this effect by proposing a three dimensional tank. The 3^{rd} and 4^{th} sub-bands (on-off state and on-on state, respectively) have the worst case quality factor (refer to Fig. 10) due to larger loading effect and also lower effective inductance (refer to Fig. 11). The PN performance is further degraded in such sub-bands as the oscillation frequency is higher. To ameliorate these issues, we have implemented the auxiliary coils in different metal layers to increase the coupling factor (k_{23}) and in turn improve the quality

factor in the 2nd, 3rd ,4th sub-bands. Besides, the AP layer can achieve a higher quality factor compared to M_8 thanks to its thicker metal and larger skin depth. Thus, the third coil is implemented in AP layer rather than M_8 to improve the PN in the two sub-bands (2nd and 4th) to which the third coil contributes.

2.4. VCO Design And Implementation

The schematic of the proposed VCO is shown in Fig. 12 (a). In this figure, M_1 and M_2 are the cross-coupled transistors in the g_m-cell of the VCO. C_{d1} and C_{d2} are chosen large enough to lower the loop gain degradation. The combination of control voltage and digital inputs allows for having fine and coarse control over the range of oscillation frequency. To achieve a better quality factor, and in turn, phase noise, a larger size switch should be utilized [13-14]. However, at mm-wave frequencies, the off-state parasitic capacitance of the switch limits the tuning range. To ameliorate this limitation, NMOS switches are designed differentially to lower the corresponding on-state resistance, thereby achieving a better phase noise. The switch sizes are optimized to achieve a reasonable trade-off between phase noise and tuning range. The schematic of the implemented switch is presented in Fig. 12(b).

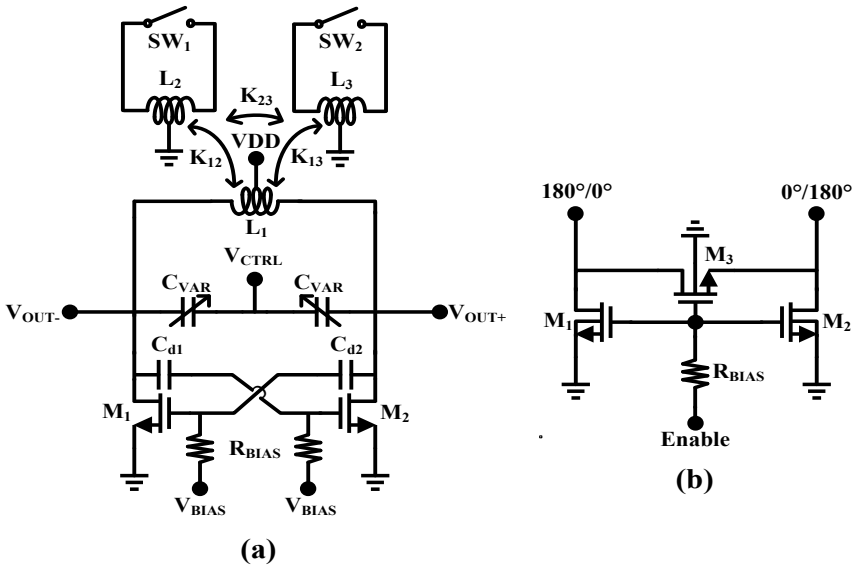

Figure 12. Schematic of the proposed (a) VCO. (b) The proposed switch architecture.

To achieve a lower loss and thus a better *Q*, the thicker topmost metal layers are employed to implement mm-wave inductors. In the 65-nm CMOS process used in this work, the thickest metal layer is metal 9 (M_9). Although implementation of mutually coupled planar inductors utilizing M_9 shows a higher quality factor, there are challenges associated with such a planar configuration. First, the occupied area is larger due to the minimum required spacing between side-by-side M_9 layers enforced by the design rules. This also results in a lower coupling factor, and in turn, a higher magnetic loss. Second, a relatively large number of required vias to avoid metal overlaps introduces higher losses. Third, the current crowding (i.e., the proximity effect) of the adjacent inductor traces results in a lower quality factor at mm-wave frequencies. Finally, there is a parasitic capacitance between adjacent traces of planar inductors which limits the self-resonance frequency (SRF) and quality factor at high frequencies. The proposed mutually coupled inductors ameliorate these challenges by implementing the three coupled inductors in three top-most metal layers, that is, Metal 8 (M_8), M_9, and the top aluminum layer (AP). The M_8 layer is utilized to implement the secondary coil where a larger inductance with smaller inner radius is required due to have a higher inductance per unit length. Moreover, the skin effect degrades the quality factor at high

frequencies. In this regard, AP has the advantage of a larger skin depth and thus a lower quality factor degradation. Furthermore, the substrate loss is reduced if AP layer is employed (due to its farther distance from the substrate).

The cross-sectional and top views of the proposed switchable transformer which consists of three mutually coupled one-turn inductors are shown in Figs. 13 and 14, respectively. The design parameters r, W_i, and S_i are the inner radius, width of i^{th} inductor, and the spacing between adjacent traces, respectively. The inner radius and widths of the inductors are chosen to satisfy the conditions for the inductances mentioned in the previous section. S_2 and S_3 are chosen to be zero in order to maximize the coupling factor without increasing the inter-layer parasitic capacitance. S_1 is chosen to maximize the quality factor of the overall tank at the target frequency.

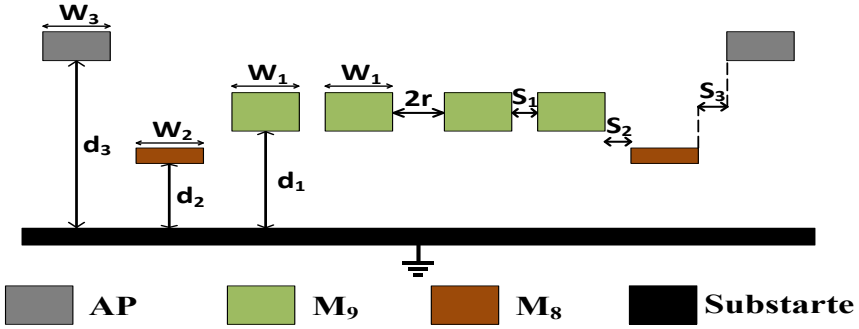

Figure 13. Cross section view of the proposed switchable transformer.

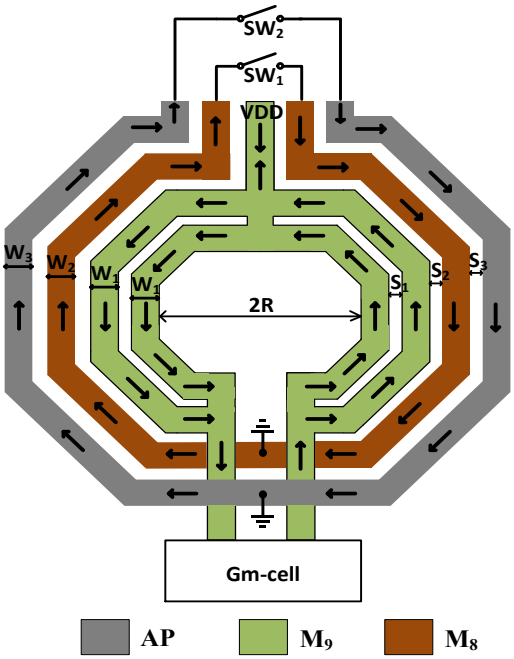

Figure 14. Top view of the proposed switchable transformer.

The center-tapped inductor is designed in the tank to facilitate DC biasing and save the area. Moreover, to lower the parasitic resistance, a striped inductor structure is used to improve the phase noise [16]. In the proposed transformer, a grounded shield ring using M_9 is designed to further enhance the quality factor at the desired frequency. This shielding layer significantly reduces the loss associated with the lossy substrate at high frequencies which results in a higher quality factor. This structure functions similar to a coplanar waveguide in which the space between the ground and signal planes is optimized to achieve the maximum possible quality factor at the frequency band of interest. The optimized distance in our design is 25 μm. This structure functions similar to a coplanar waveguide (CPW) in which the space between the ground and signal planes is optimized to achieve the maximum possible quality factor at the frequency band of interest. Electromagnetic (EM) simulations are performed using Keysight's Advanced Design System (ADS) Momentum to validate the performance of the proposed transformer architecture. Figs. 15 and 16 show the simulated coupling factor, k, and Q for various possible configurations, respectively. In these configurations, the secondary coil is implemented in M_8 layer and the tertiary

coil is either implemented with M_8 (planar structure) or with AP (the proposed structure). For a fair comparison, the spacing between the secondary and tertiary coils is chosen to be the minimum distance allowed by the design rules for the planar implementation. Note that in the proposed design we have used S_2=S_3=0, which would further improve the coupling factor. Figs. 10 and 11 show the simulated effective inductance and quality factor over the entire 4 sub-bands.

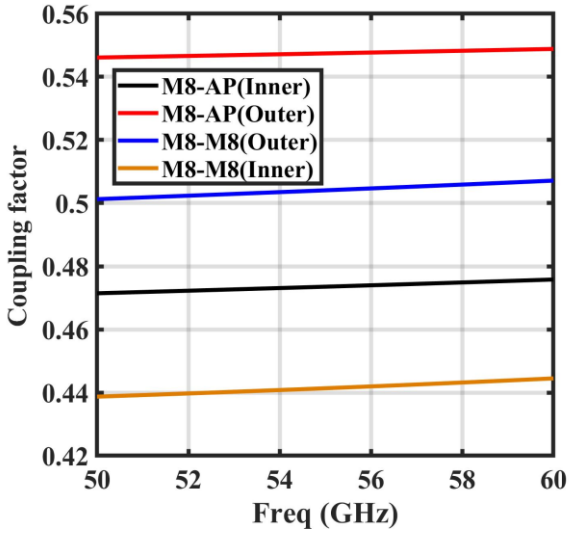

Figure 15. Simulated coupling factor (k23) for different configurations.

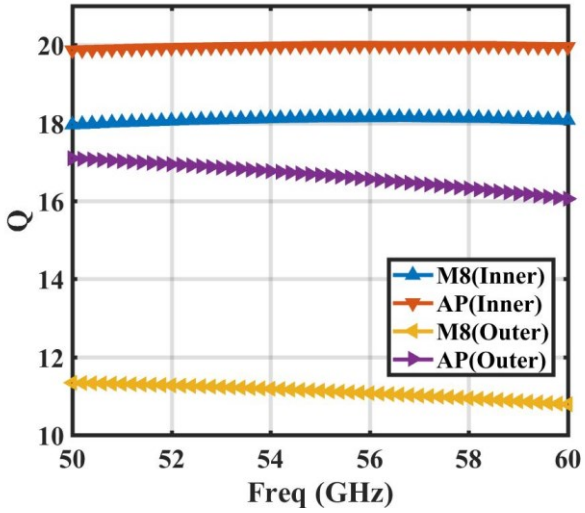

Figure 16. Simulated quality factor for different configurations.

The layout of the fabricated VCO is completely symmetric. This feature is facilitated by using the following design techniques. The differential switches shown in Fig. 12(b) are used to keep the

symmetry of the layout and to reduce the on-state switch resistance. The main switch is located exactly in the middle to keep the symmetry of the layout. The switches connected to ground and the G_m-cell are mirrored to keep the vertical symmetry of the layout. The primary coil is implemented with its center-tap connected to the supply voltage. The secondary and tertiary coils are designed using standard symmetric inductors provided by the technology.

2.5. Verification Of The Proposed Model

Although the proposed circuit model of the proposed three coils transformer is simple, however, as it has been mentioned above, the objective of using the simplified model is to provide some insights and intuitions on the advantages of the proposed technique. The high-frequency effects will definitely affect the performance, however, including them when we just want to motivate the idea will complicate the derivations and perhaps will cause more confusion. In other words, the simplified model is used to simplify analysis and the guidance for the simulations. A more elaborate model of an individual inductor is shown in Fig. 17. This model is more appropriate for modelling the high-frequency effects. To analyze an inductor individually, the high-frequency effects should certainly be considered. However, when analyzing a circuit including inductors, such as a VCO, especially when the frequency of operation is (much) lower than the self-resonance frequency, considering only L and R as a model of inductor is a reasonable choice, because in such cases one can ignore the effect of parasitic capacitance C_X , which affects the self-resonance frequency (SRF). Moreover, the substrate loss and parasitic capacitance C_P affect the quality factor of the inductor which is considered in the simulation results shown in Fig. 18.

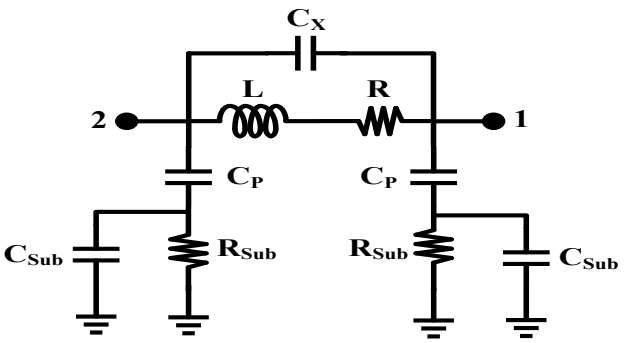

Figure 17. A high frequency circuit model of an inductor.

To further justify the statements mentioned earlier, we present simulation results for two cases of inductors modelled in Keyshight's ADS momentum on the layout of the proposed transformer and the case using the simplified R and L model for each coil of the transformer with constant mutual coupling in the schematic simulations. The schematic view simulation results of the simplified model (in which L and R of each inductor are extracted from EM simulation of the corresponding individual inductor) are compared to EM simulation results of the laid out transformer. Fig. 18 compares the simulated quality factor seen by the primary coil in two cases when $k_{23} = 0$ and 0.5, respectively. As can be seen from the figure, the quality factor seen by the primary coil is improved as the coupling factor between the loads increases (in this case from 0 to 0.5). Both EM simulations on the layout and simulations on the simplified schematic view confirm the same trend. Thus, although the quality factor extracted from the simplified model is different from that of the EM layout (because it does not take into account high-frequency effects), however, the trend predicted in equations derived from the simplified circuit are still valid and the quality factor improves as the coupling factor increases. Same conclusion can be drawn for the effective inductance seen at the primary.

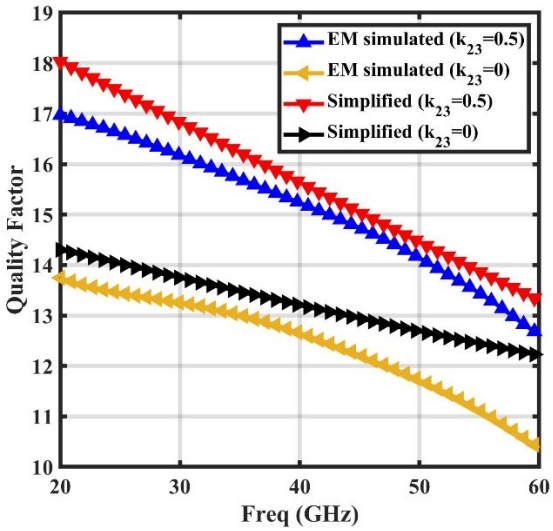

Figure 18. Q factor comparison between that of the proposed model and transformer.

2.6. Discussion On The Pulling Effect Of The Proposed VCO

In this design, by turning switches on and off, the output loading of the VCO suddenly changes, which could result in the change of frequency of operation. Thus in what follows we will address the issue of the frequency pulling. In this work, there are four switching states and all of them have been modeled. In the proposed model, the off-state and on-state effects of the switches are considered and then the oscillation frequency in each state is analyzed by taking into account the inductance and resistance that are seen by the tank in each state. The analysis shows that the oscillation frequency in all sub-bands are controllable by the user utilizing two bits. To validate the transient response, a pulse signal with a rising edge (which turns on the switch) is applied to one of the switches at 15 ns and the simulated output voltage and oscillation frequency are shown in Figs. 19 and 20, respectively. These plots show that the VCO settles to its steady state after ~0.3 ns.

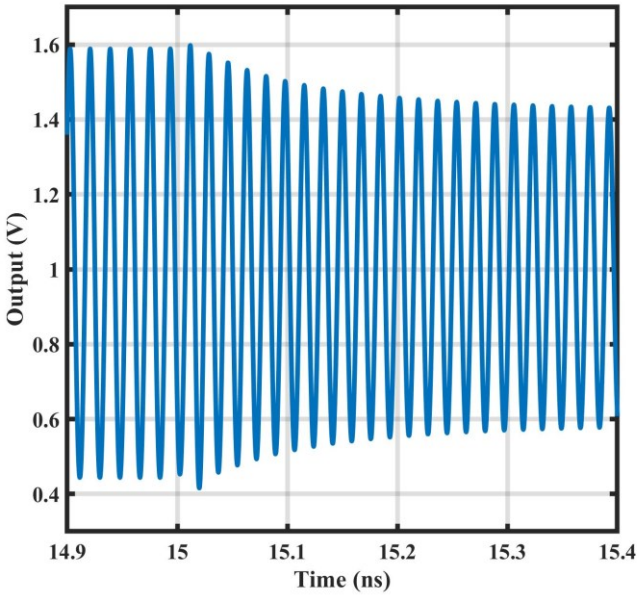

Figure 19. Simulated output signal after applying a pulse at the gate of the switch.

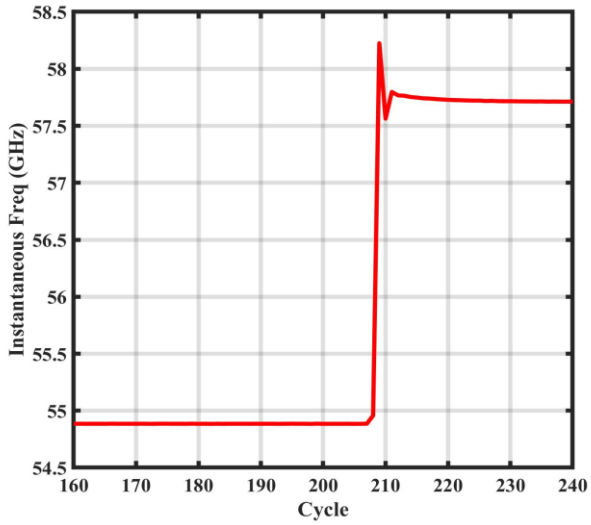

Figure 20. Transient response of the oscillation frequency after applying a pulse at the gate of the switch.

Chapter 3. Low-Power Wide-Tuning-Range Mm-wave CMOS VCO

3.1. Introduction and Overview of Recently Published Works

Scaling of the cost effective CMOS process attracts designers to implement mm-wave building blocks in recent years. Due to the insatiable demand for high data-rate communication capacity, the radio-frequency integrated circuits (RFICs) operating in higher frequency bands has attracted more attention. In this regard, the 5th generation of wireless systems (5G) has extended its operation frequency to millimeter-wave (mm-wave) band in order to benefit from more signal bandwidth [1]. Voltage-controlled oscillators (VCOs) play an important role in the operation of integrated mm-wave transceivers. The generation of a wideband, low phase noise signal while maintaining low power consumption is one of the challenges in designing RF and mm-wave VCOs. Furthermore, power consumption is one of the most important challenges in designing mm-wave VCOs. As the frequency goes up, the noise performance of active and passive devices deteriorates the phase noise of the VCO. Also, due to the trade-off between power consumption and phase noise, more power should be consumed to have an acceptable noise performance.

Several techniques have been introduced to improve the tuning range and phase noise performance of different VCO topologies [21–25]. To extend the tuning range in [21], even and odd operation modes of a transformer-based resonator are combined to generate two overlapping frequency sub-bands. However, in this technique achieving an overlap between the two bands becomes a major challenge at high frequencies. Moreover, due to the complicated fabrication processes and layout, utilizing integrated passive device (IPD) process, used in [21], is challenging for applications with operation frequencies higher than 10 GHz. An inductor-loaded transformer is designed in [22] with switches placed at different positions to increase the number of sub-bands, and the resulting tuning range. However, the relatively large number of switches required for a

symmetric implementation increases the parasitic capacitance seen by the resonator. In [8], switchable coupled VCO cores are designed to realize a dual mode operation at the cost of a higher power consumption and larger area. The design also suffers from a low output power. In [9][15][26], switched coupled inductors are utilized to change the effective inductance of the tank, thereby extending the tuning range at the cost of a degraded noise performance. The design also requires a relatively large area and high power consumption. In [27], by using analog tuning varactors connected to the g_m-cell a wide tuning range is achieved, however, such varactors have a poor performance at mm-wave frequencies.

In this thesis, we introduce a new structure which simultaneously improves the tuning range and phase noise while consuming lower power as compared to the conventional RF and mm-wave Colpitts VCOs. The tuning range is enhanced by using a switched-capacitor bank which has less adverse effects on the noise performance. In the proposed architecture, the switches in the capacitor bank minimally load the tank. That is, during the switching action, low impedance path to ground which would degrade the tank quality factor is avoided. In addition, two inter-stage inductors between the tank and G_m-cell are employed to relax the start-up issues at the cost of a larger area. The proposed approach not only reduces the power consumption, but also improves the tuning range by partially cancelling the parasitic capacitances seen by the tank. Also, the dynamic body bias technique is applied to the VCO core transistors to improve the phase noise and to lower the power consumption. Given that Colpitts VCOs show better behavior in terms of noise performance than those of traditional cross-coupled LC-VCOs [7], we have used the Colpitts structure for the core oscillator.

To confirm the effectiveness of the proposed techniques, the small-signal analysis in conjunction with simulation results in different regimes of operation are presented. Furthermore, the

performance of the overall architecture is validated through measurements of a proof-of-concept prototype chip fabricated in a 65-nm CMOS process. The organization of the rest of the paper is as follows: Sections II and III describe the proposed techniques and the VCO implementation, respectively. Measurement results are presented in Section IV and concluding remarks are provided in Section V.

3.2. The Proposed Architecture

3.2.1. The Proposed Variable Capacitive Feedback Colpitts [23]

The quality factor of the tank has a pronounced effect on the phase noise of the oscillator. Typically, the tank quality factor is limited by the quality factor of the tank inductor at low frequencies and by that of the varactor at mm-wave frequencies. Thus, at high frequencies, the varactor should be chosen as small as possible in order to minimize the degradation of the tank quality factor. To achieve a wide-tuning range and overcome this limitation, discrete tuning method by using digitally controlled capacitor banks have been used [13-14]. However, the design of switches and capacitors has its own challenges (such as the effect of parasitic capacitances of switches at high frequencies as well as loading the tank). To ameliorate these challenges, several techniques such as differential capacitor banks and differential switches have been proposed [13-14]. Although these techniques have shown better performance with respect to the single-ended switching stage, they load the tank by creating a low impedance path to ground. In addition, the conventional capacitor banks typically use large switches (to minimize the switch resistance) which in turn adversely affect the tuning range. An advantage of the proposed switching structure is that as compared to the conventional capacitor banks, the parasitic capacitance of the switches seen by the tank is lower. Furthermore, in the proposed technique in which the capacitor bank is being added in parallel with one of the feedback capacitors, the effective incremental capacitance

of the capacitor bank can be made lower. This would result in a lower rate of frequency change (i.e., lower VCO gain, k_{VCO}) which in turn would lead to a better frequency resolution and a lower sensitivity to noise on the control voltage [33]. Moreover, due to this lower rate of frequency change, the proposed structure has a better suppression of the flicker noise [4][16][17]. To be more specific, for the same value of the branch capacitance in the proposed and conventional capacitor banks, the coarse tuning range due to activating each branch of the capacitor bank would be narrower in the proposed technique, thereby requiring a smaller varactor with lower K_{VCO} for fine tuning (to cover the overlap between different frequency bands). To summarize, the proposed technique offers lower flicker noise, higher frequency resolution, and lower sensitivity to the noise of the control voltage. The schematics of both conventional and the proposed capacitor banks, implemented in a differential Colpitts VCO, are shown in Fig. 21 (a) and (b).

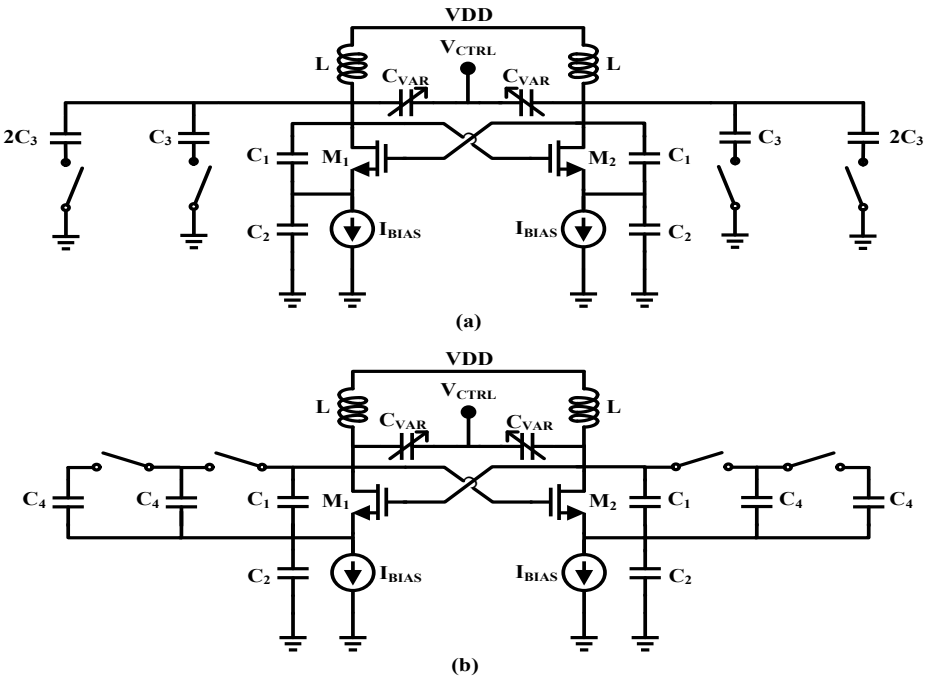

Figure 21. Schematic of the Colpitts VCO with (a) Conventional (b) Proposed capacitor bank.

To have a fair comparison of the phase noise between these two VCOs, we consider the same frequency of oscillation and switch size for both cases. In the conventional structure, because of

the extra capacitor that is in parallel with the output node, the oscillation frequency will be lower than that of the proposed circuit, if they both have the same incremental capacitor values. Thus, one can choose a bigger capacitor value for the proposed technique to have the same oscillation frequency. To analyze the circuits shown in Fig. 22 (a) and (b), the following simplifying assumptions and circuit parameters are considered:

$$C_1 = C_2 = c \tag{45}$$

$$R_{ON3} = R_{ON4} = R_{ON} \tag{46}$$

$$Q_{C3} = Q_{C4} = Q \tag{47}$$

$$R_{ONP} = R_{ON}\,\frac{1+\omega^2 C_3{}^2 R_{ON}{}^2}{\omega^2 C_3{}^2 R_{ON}{}^2} \tag{48}$$

$$C_{P3} = \frac{C_3}{1+\omega^2 C_3{}^2 R_{ON}{}^2} \tag{49}$$

$$R_{ONP} >> \frac{1}{\omega c} \tag{50}$$

$$\frac{C_1 C_2}{C_1 + C_2} + C_{P3} = \frac{(C_1 + C_{P4})C_2}{C_1 + C_2 + C_{P4}} \tag{51}$$

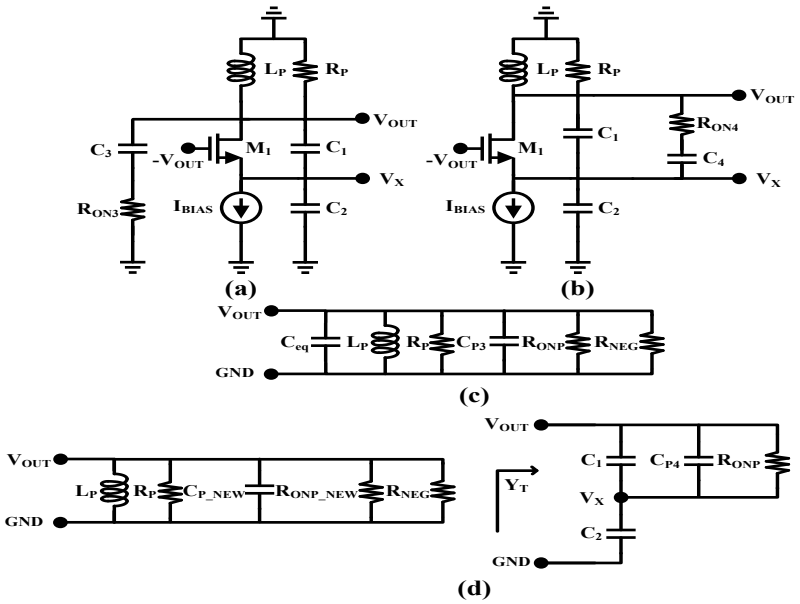

Figure 22. Half-circuit and small-signal models of : (a, c) conventional switching network (b, d) proposed switching network.

It is worth mentioning that as shown in (47) we assume that the quality factor of the capacitors of the bank in both approaches (refer to Fig. 22 (a) and (b)) are the same. As given by Equation (50), we assume that the impedance of the Colpitts feedback capacitor, C_1, is much lower than the impedance of the switches and thus, the switches do not impact the start-up condition. Note that this condition is usually satisfied at high frequency of operation. Equation (51) is based on the assumption that the oscillation frequency is equal in both conventional and the proposed structures. In addition, R_{ONP} and C_{P3} are the equivalent parallel resistance and capacitance of the series RC network in the conventional circuit. The small-signal model of conventional and proposed Colpitts oscillators with a one-branch capacitor bank are illustrated in Fig. 22 (c) and (d), respectively.

The total admittance of the network illustrated in Fig. 22 (d) can be expressed as in (52). The real and imaginary parts indicate the total parallel resistance and capacitance seen by the tank as stated in (53) to (55). By comparing (48) and (54) which show the equivalent parallel resistance of the two structures, it can be concluded that in the conventional capacitor bank the quality factor of the tank is worse than that of the proposed approach due to having a lower equivalent parallel

resistance. The equivalent parallel resistance in the proposed technique is at least 3 times larger than that of the conventional bank. Therefore, this technique can achieve lower phase noise. Another advantage of the proposed approach is that for the same perceived parallel resistance (which translates to approximately the same phase noise) the proposed approach can use a smaller switch. Furthermore, because of cascaded switches in the proposed approach (refer to Fig. 21), the effect of the parasitic capacitance of the switches at the output node is significantly decreased. This, in turn, would result in a wider tuning range.

$$Y_T = \frac{\omega^2 c^2}{\frac{1}{R_{ONP}} + R_{ONP}\omega^2 (2c + C_{P4})^2} + j\frac{\omega c + {R_{ONP}}^2 \omega^3 c(c + C_{P4})(2c + C_{P4})}{1 + \omega^2 (2c + C_{P4})^2 {R_{ONP}}^2} \tag{52}$$

$$\mathrm{Re}[Y_T] = \frac{\omega^2 c^2}{\frac{1}{R_{ONP}} + R_{ONP}\omega^2 (2c + C_{P4})^2} => \tag{53}$$

$$R_{ONP\_NEW} = 4R_{ONP} + \frac{1}{R_{ONP}\omega^2 c^2} + \frac{R_{ONP}{C_{P4}}^2}{c^2} + \frac{4R_{ONP}C_{P4}}{c} \tag{54}$$

$$C_{P\_NEW} = \frac{c + {R_{ONP}}^2 \omega^2 c(c + C_{P4})(2c + C_{P4})}{1 + \omega^2 (2c + C_{P4})^2 {R_{ONP}}^2} \tag{55}$$

Based on the above-mentioned analysis, the proposed capacitor bank can be added in parallel to either C_1 or C_2. However, due to the following three reasons, it makes more sense to have the bank in parallel with C_1. First, in order to suppress the flicker noise up-conversion, the bias current of the VCO and the parasitic capacitance at the sources of transistors M_1 and M_2 should be as small

as possible [13-14]. Adding the capacitor bank to C_1 will result in less parasitic capacitance at the source of transistors M_1 and M_2. Second, the parasitic capacitance at the sources of M_1 and M_2 is larger than that of the drains of these transistors, thus adding the capacitor bank to C_2 will result in further increase of the parasitic capacitance and thus reduces the tuning range. Third, based on (58), increasing C_1 reduces the noise factor and in turn the phase noise, while increasing C_2 would increase these parameters. Therefore, increasing C_1 would be a better choice for the purpose of this work where the focus is on lowering the phase noise. Note that in (56) to (58), 'A',' η ', and 'F' are the oscillation amplitude, power efficiency, and noise factor of the conventional Colpitts oscillator, respectively.

$$A = 2I_{BIAS}\frac{C_2}{C_1 + C_2}R_P \tag{56}$$

$$\eta = \frac{C_2}{C_1 + C_2}\frac{A}{VDD} \tag{57}$$

$$F = 1 + \frac{C_2}{C_1} \tag{58}$$

In other words, the conventional capacitor banks typically load the tank by creating a low impedance path to ground which significantly degrades the noise performance. To overcome this challenge, one can use large switches to minimize the on-state resistance of switches which, in turn, adversely affect the tuning range by increasing the switch off-state capacitance. To ameliorate these challenges, the capacitor bank based on variable capacitive feedback technique, i.e, the capacitor bank is being added in parallel with one of the feedback capacitors, is introduced in [23]. As shown in [23] by using the variable capacitive feedback technique, larger value of perceived parallel resistance, i.e., less loading, can be achieved compared to a conventional topology using

similar switch sizes in the tank. This technique improves the tuning range with a minimal degradation of the tank quality factor. The schematics of both conventional and the proposed capacitor banks, implemented in a differential Colpitts VCO, for simplicity only one capacitor branch is shown in Figs. 23 (a) and (b).

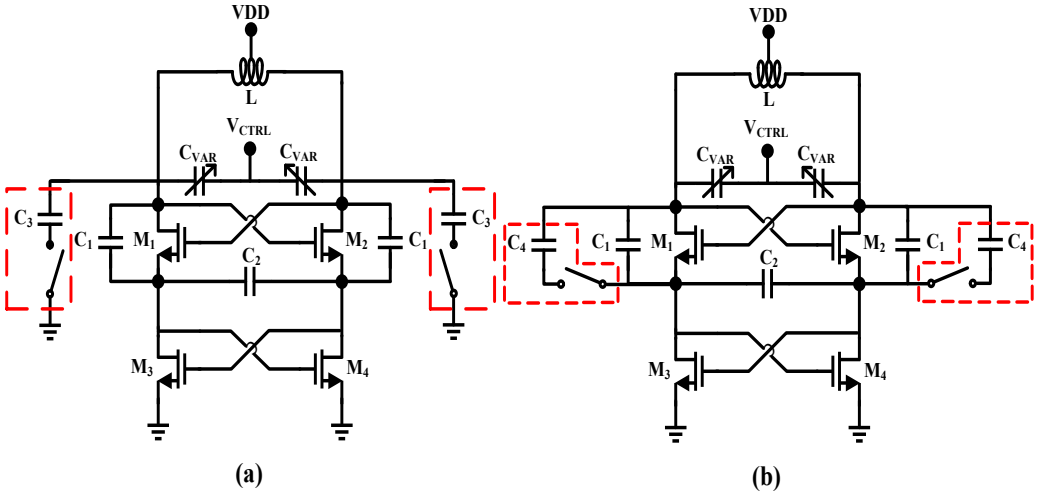

Figure 23. Schematic of the conventional differential Colpitts VCO with a one-branch capacitor bank (a) conventional; (b) proposed.

As discussed earlier, the equivalent parallel resistance seen by the tank in the conventional and proposed structures can be summarized here as;

$$R_{ONP\_conv} = R_{ON}\frac{1+\omega^2 C_3{}^2 R_{ON}{}^2}{\omega^2 C_3{}^2 R_{ON}{}^2} \tag{59}$$

$$R_{ONP\_proposed} = 4R_{ONP\_conv} + \frac{1}{R_{ONP\_conv}\omega^2 c^2} + \frac{R_{ONP\_conv} C_{P4}{}^2}{c^2} + \frac{4R_{ONP\_conv} C_{P4}}{c} \tag{60}$$

where ω, R_{ON}, R_{ONP}. C_{P4}, and c are the frequency, on-state resistance of the switch, the equivalent parallel on-state resistance of the switch, the equivalent parallel capacitance of the added capacitor in the proposed topology, and the value of feedback capacitors ($c = C_1 = C_2$), respectively. Comparing (59) and (60) reveals that the equivalent parallel resistance achieved by the tank in the proposed approach is at least three times larger than that of the conventional one due to the additional terms of (60). To show the effectiveness of this switching technique, a combination of

post-layout and electromagnetic (EM) simulations using Cadence and Keysight Advanced Design System (ADS) Momentum are performed. The simulated loss of the tank (R_p) is plotted in Fig. 24 for the conventional and proposed topologies and over different switch states. This plot suggests that the proposed method has a lower tank loss when the switch is on which in turn results in a lower phase noise.

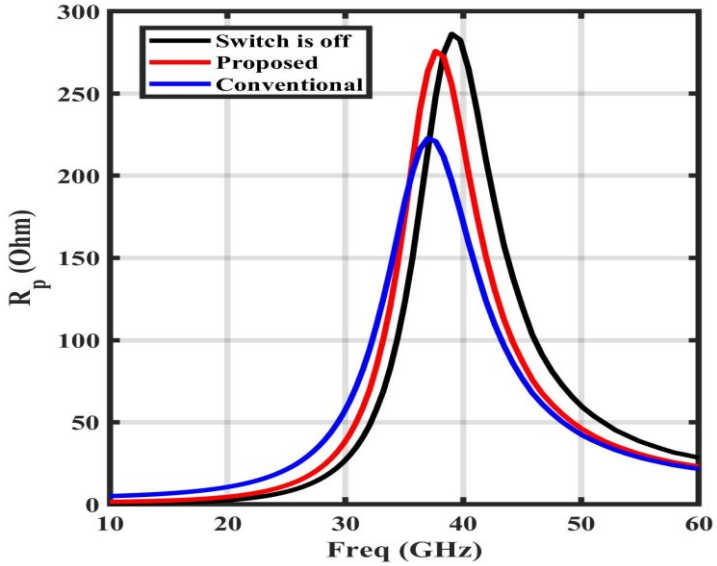

Figure 24.The simulated loss of the tank in conventional and proposed structures.

3.2.2. The Proposed G_m-boosting Technique

The conventional Colpitts VCOs usually have a high power consumption and also suffer from start-up issue [28][31-32][34-37]. To overcome these challenges, the negative transconductance generated by the G_m-cell should be improved. A typical solution to boost the negative transconductance is to increase the injection current to the tank by increasing the size of the cross-coupled transistors. However, larger power would be required to generate larger injection current which would result in a degraded figure-of-merit (FOM) suggested for VCOs [25][27][30]. The use of large devices also limits the tuning range of VCO due to their large parasitic capacitances.

An alternative method is to decrease the capacitive loading of the tank in order to achieve a larger transconductance. To this end, we propose a G_m-boosting technique that splits the tank inductor (as shown in Fig. 25) to achieve an improved negative transconductance with a low power consumption and a wide tuning range.

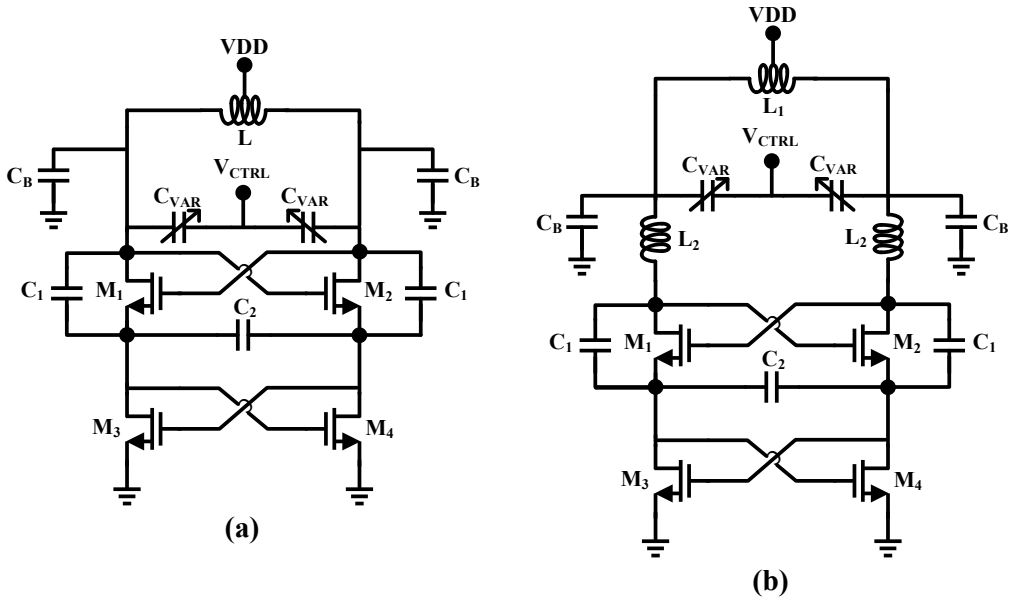

Figure 25. Schematic of the (a) conventional Colpitts VCO; (b) proposed gm-boosted Colpitts VCO.

The proposed G_m-boosting technique significantly enhances the generated negative transconductance by adding two inter-stage inductors between the G_m-cell and the tank. In other words, the splitting of the tank inductor into two parts and placing the varactors between them is utilized in the tank in order to relax the start-up of the VCO while reducing the parasitic capacitance and power consumption. As can be seen in Fig. 25, the inductor L_2 is used to distribute the capacitive loading of the tank. The output buffers are connected to the interconnection node between L_1 and L_2 and their parasitic capacitance has been modeled by C_B. To analyze the effect of the inter-stage inductors, simplified schematic diagrams and small-signal models of the conventional and proposed structure are shown in Fig. 26 (a, b, c, and d). In these figures C_p, G_{eq},

and C_{eq} are the drain parasitic capacitance of M_1, equivalent parallel conductance of the G_m-cell, and the equivalent parallel capacitance of the G_m-cell, respectively.

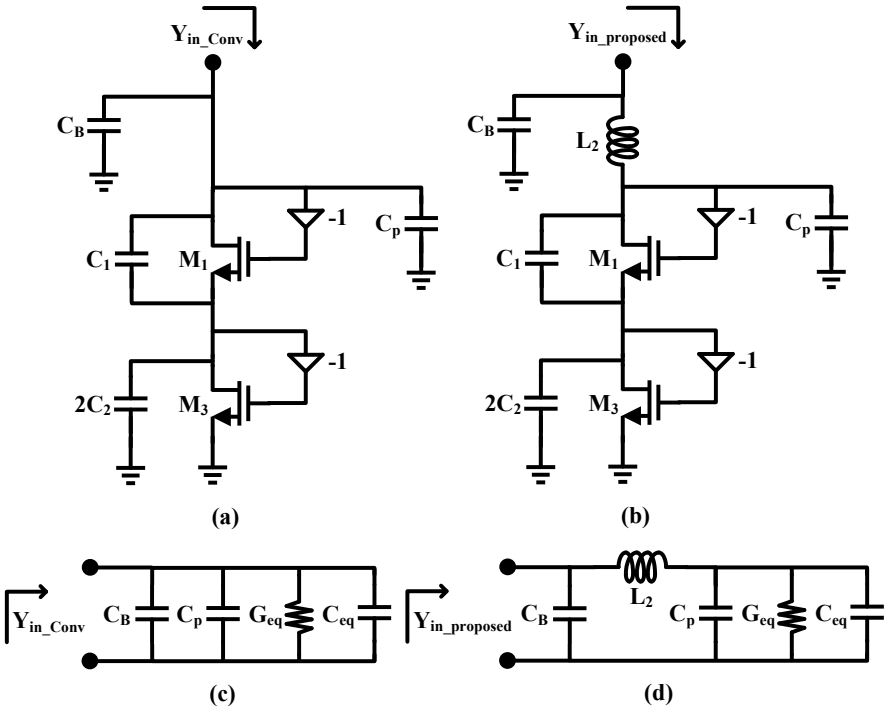

Figure 26. The simplified and small signal model of the (a, c) conventional Colpitts VCO; (b, d) proposed Colpitts VCO.

According to Fig. 26(c), the real and imaginary parts of the input admittance of the conventional VCO can be written as;

$$\mathrm{Re}[Y_{in\_Conv}] = G_{eq} \tag{61}$$

$$\mathrm{Im}[Y_{in\_Conv}] = \omega C_B + \omega(C_p + C_{eq}) \tag{62}$$

Similar calculations can be carried out for the circuit of Fig. 26(d) and the corresponding parameters are as follows:

$$\mathrm{Re}[Y_{in\_proposed}] = \frac{\frac{G_{eq}}{\omega^2 L_2^{\,2}}}{G_{eq}^{\,2} + [\omega(C_p + C_{eq}) - \frac{1}{\omega L_2}]^2} \approx \frac{1}{G_{eq}\omega^2 L_2^{\,2}} \tag{63}$$

$$\mathrm{Im}[Y_{in\_proposed}] = \omega C_B +$$

$$\omega(C_p + C_{eq})[\frac{\omega(C_p + C_{eq}) - \frac{1}{\omega L_2}}{\omega L_2 G_{eq}^{\,2} + \omega L_2[\omega(C_p + C_{eq}) - \frac{1}{\omega L_2}]^2}] \tag{64}$$

$$-\frac{G_{eq}^{\,2}}{\omega L_2 G_{eq}^{\,2} + \omega L_2[\omega(C_p + C_{eq}) - \frac{1}{\omega L_2}]^2} \approx \omega C_B - \frac{1}{\omega L_2}$$

The approximations in (63) and (64) hold if $\omega(C_p + C_{eq}) - \frac{1}{\omega L_2} \approx 0$ which means that L_2 should resonate with (C_p + C_{eq}) within the frequency band of interest. Comparing (61) and (63), we advocate that the equivalent negative transconductance in the proposed approach can be designed to be much larger than that of the conventional one within the frequency band of interest. Also, it can be shown that the value of L_2 required to satisfy the above-mentioned condition also leads to $\frac{1}{G_{eq}\omega^2 L_2^2} > G_{eq}$ which means that the proposed approach offers a larger equivalent conductance. Moreover, from (62) and (64), the proposed method also reduces the overall parasitic capacitance seen by the tank. As can be observed from the first term of expression in (64), for all values of L_2 the coefficient of $\omega(C_p + C_{eq})$ is less than one (and also the third term is negative) showing that the imaginary part of admittance is smaller as compared to (62). The simulated small-signal equivalent negative transconductance versus frequency is plotted in Fig. 27. As can be seen, the

generated negative transconductance is boosted significantly at the frequency band of interest provided by tuning the value of L_2.

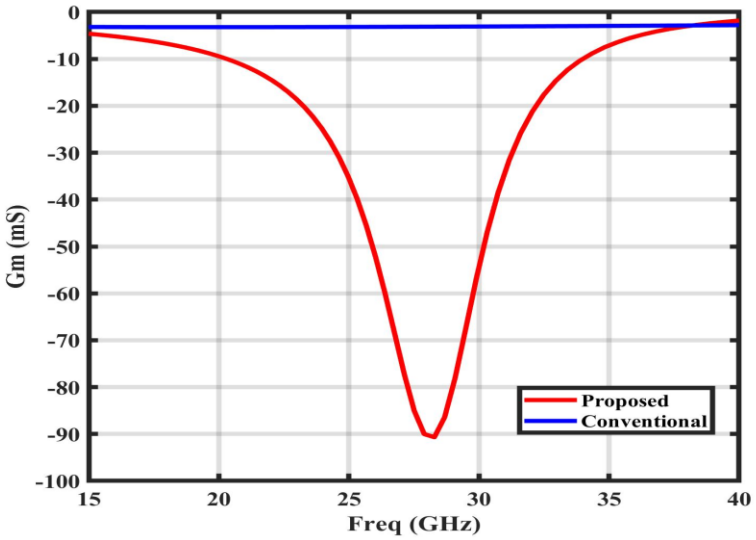

Figure 27. Comparison of the simulated small-signal negative transconductance in conventional and proposed topology.

Due to the fact that oscillators show a non-linear large signal behavior, the large signal S-parameters simulation (LSSP) is performed to validate the aforementioned analysis. Fig. 28 and 29 present the simulated large-signal negative resistance and transconductance of the proposed gm-cell versus the applied differential voltage at 28-GHz. These plots show that the negative resistance decreases when the amplitude increases such that the resistance becomes positive beyond a certain point. This also would result in a sharp transition in the transconductance showing that the oscillation amplitude must be lower than the zero crossing point in order to satisfy start-up conditions.

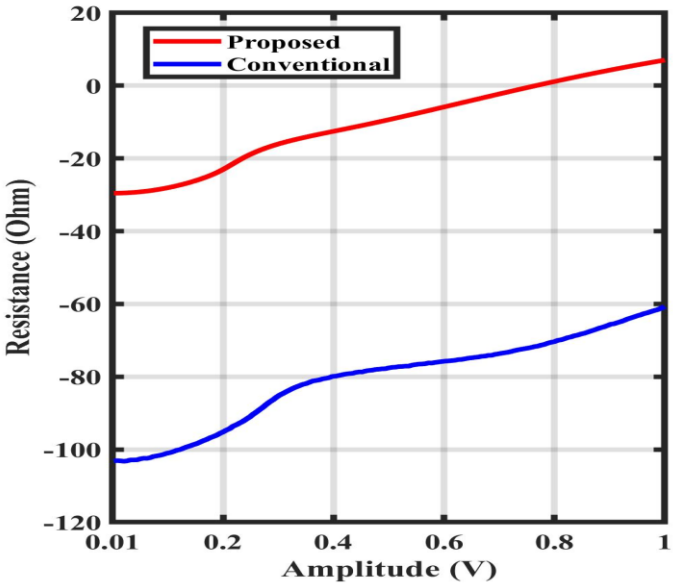

Figure 28. Comparison of simulated equivalent parallel resistance in Conventional and proposed technique.

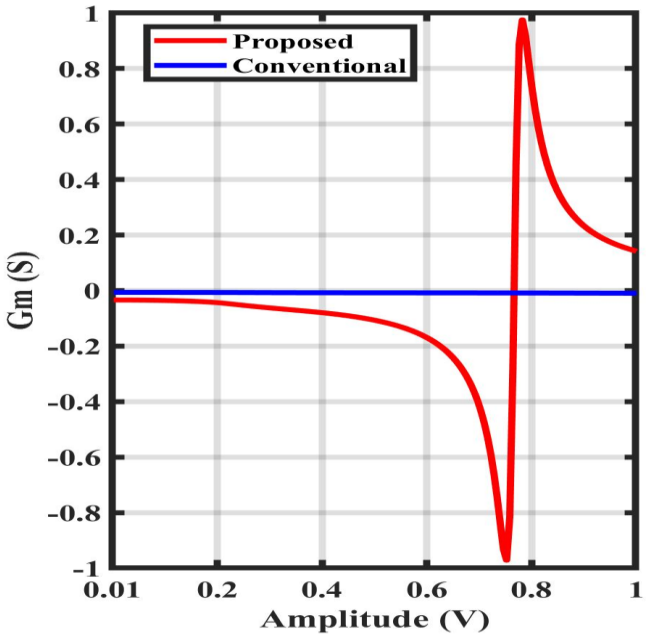

Figure 29. Comparison of simulated equivalent parallel transconductance in Conventional and proposed technique.

Another interesting advantage of the proposed technique is that the inter-stage inductors act as an impedance transformer network as shown in Fig. 30 (a). As discussed earlier, the total admittance seen by the tank is substantially larger than that seen by L_2, which translates to $abs(Y_1) > abs(Y_2)$.

Applying ohm's law and considering that $I_1 = I_2 = I$ (assuming that C_p is compensated mostly by L_2 and does not draw current), it can be concluded that $V_2 > V_1$. This observation asserts that the swing voltage across the gate of M_1 is also boosted resulting in a sharper edges and faster switching of the cross-coupled pair hence a lower phase noise. The simulated transient signals at both ends of L_2 are presented in Fig. 30 (b). To summarize, contrary to the conventional Gm-boosting techniques, the proposed technique simultaneously enhances the negative transconductance, lowers the power consumption and phase noise, and extends the tuning range at the cost of a larger occupied area.

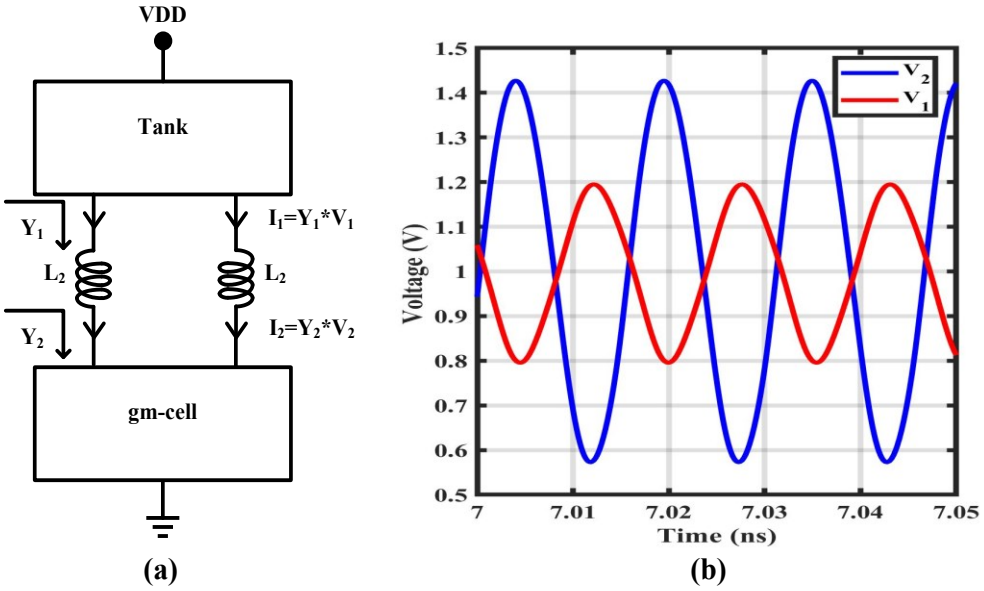

Figure 30. System-level model of the proposed gm-boosting technique. (b) Simulated transient signals at V1 and V2.

3.2.3. The Proposed Body Bias Technique

The proposed dynamic forward-body self-biased technique is shown in Fig. 31 (a). In this approach, the bodies of the transistors, including M_1, M_2, M_3, and M_4, are biased through a cross-coupled structure.

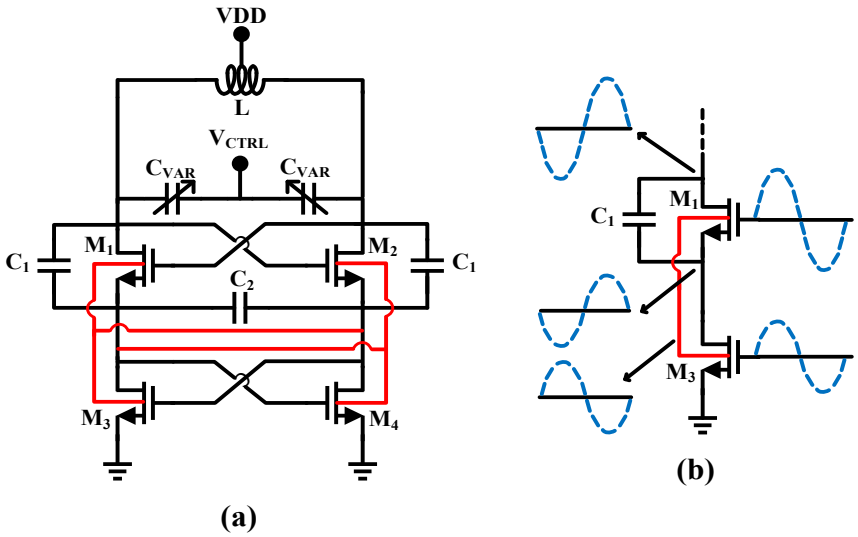

Figure 31. The proposed body bias technique; (a) schematic (b) corresponding signals.

There are several advantages associated with the proposed topology compared to the conventional one, i.e. all substrate nodes connected to ground. First, the forward body bias reduces the threshold voltage of the transistors which results in a larger generated negative transconductance. The simulated large signal negative transconductance generated at 28-GHz in conventional and proposed topology are plotted and compared in Fig. 32. Second, this technique also improves the noise performance of the VCO. To better illustrate this, the corresponding waveforms are depicted in Fig. 31 (b) and Fig. 33.

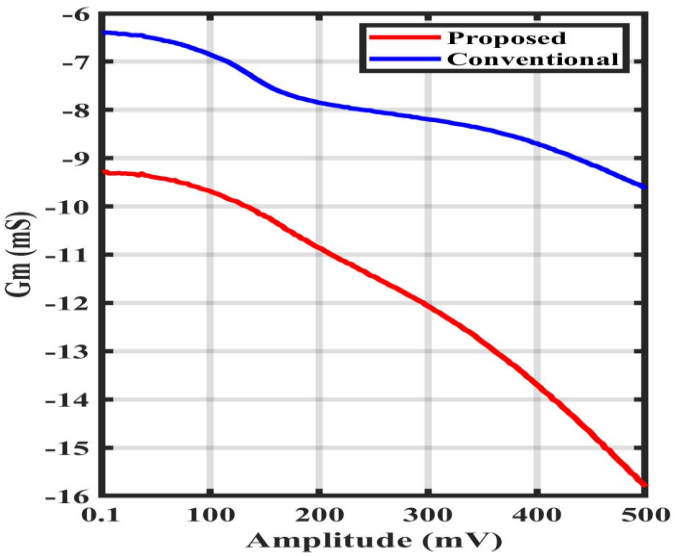

Figure 32. Comparison of the simulated negative transconductance in conventional and proposed body bias technique.

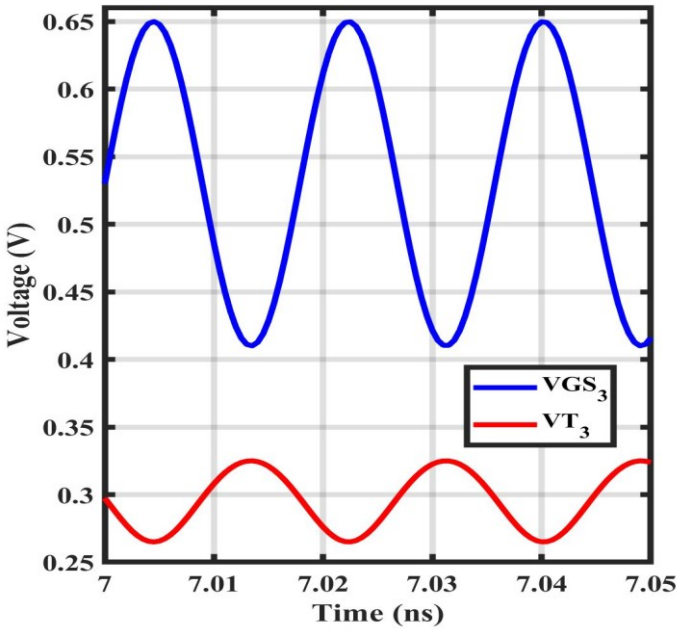

Figure 33. Simulated transient response of the proposed body bias technique.

As can be seen from Fig. 31 (b), the gate voltages of M_3 and M_4 are in phase with the corresponding signals applied to their bodies and their sources are connected to the ground. Thus, the threshold voltage variation only depends on the variation of the body signal. Moreover, the threshold voltage variation is in opposite phase with that of the body signal. Therefore, when the gate voltage

decreases, the threshold voltage increases to turn the corresponding transistor off faster. On the other way, when the gate voltage rises, the threshold voltage goes down to turn the transistor on faster. Fig. 33 shows the transient threshold and gate-source voltages of M_3 verifying the above-mentioned observations. This feature facilitates a sharper transition between on and off-state of the cross-coupled pair reducing the conduction time of the transistors, and in turn leads to a more impulse-shaped drain current compared to that of the conventional topology. This not only improves the phase noise, but also lowers the power consumption. Fig. 34 shows the simulated transient drain current of M_1.

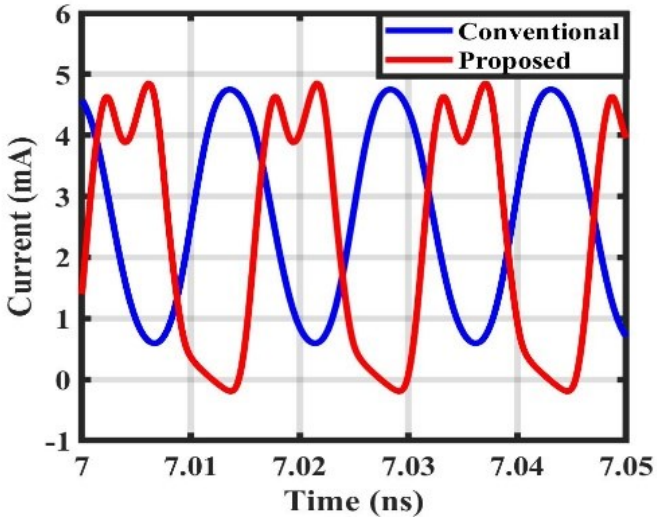

Figure 34. The simulated transient drain current of M1.

In this plot, given some certain values, the current has a negative value which is the effect of the parasitic capacitances. The frequency of oscillation in the proposed technique is slightly lower due to existing more parasitic capacitance associated with the bulk. The average current per cycle in the proposed technique is lower than that of the conventional which results in a lower power consumption. Finally, the first and third harmonic of the output current are in opposite phases shown by its behavior at its positive peak values which is one of the characteristics of the square waves. Overall, the proposed body bias technique facilitates sharper switching which

simultaneously lowers conduction time and, in turn, power consumption which leads to a better noise performance.

3.2.4. VCO Design and Implementation

The proposed VCO architecture is shown in Fig. 35. The transistors M_1 and M_2 form the main cross-coupled pair of the g_m-cell of the proposed VCO generating a negative resistance in order to compensate for the loss of the tank. The capacitors C_1 and C_2 realize the capacitive feedback network of the Colpitts oscillator which are selected to be equal so as to have a compromise trade-off between the noise performance and output power [13]. The cross-coupled pair of M_3 and M_4 form current switches which result in an improved generated negative resistance by providing larger loop gain [8], although they limit the oscillation amplitude. Moreover, adding M_3 and M_4 in the source of the main cross-coupled pair lowers the $1/f^3$ phase noise [13][14]. The NMOS switches SW_1 and SW_2 are employed to effectively change the feedback coefficient of the Colpitts capacitive feedback network. Depending on the switch states, three overlapping frequency sub-bands are introduced to extend the tuning range. Additionally, by avoiding the use of any switches connected between the output node and ground, the degradation due to lossy switches are considerably lower. The combination of control voltage and digital inputs allows for having fine and coarse control over the range of oscillation frequency. Considering process variations, due to the trade-off between the tuning range and quality factor of varactors, length and width of MOS varactors are tuned just large enough to guarantee non-zero overlap between the adjacent frequency sub-bands in all process corners. Two open-drain output buffers are designed at the tank output for measurement purposes. The drain biases are provided using external Bias-Tees through a separate 1-V supply voltage. To avoid limiting the tuning range by increasing the parasitic

capacitance, the buffers are connected directly to the VCO output without employing DC-coupling capacitors.

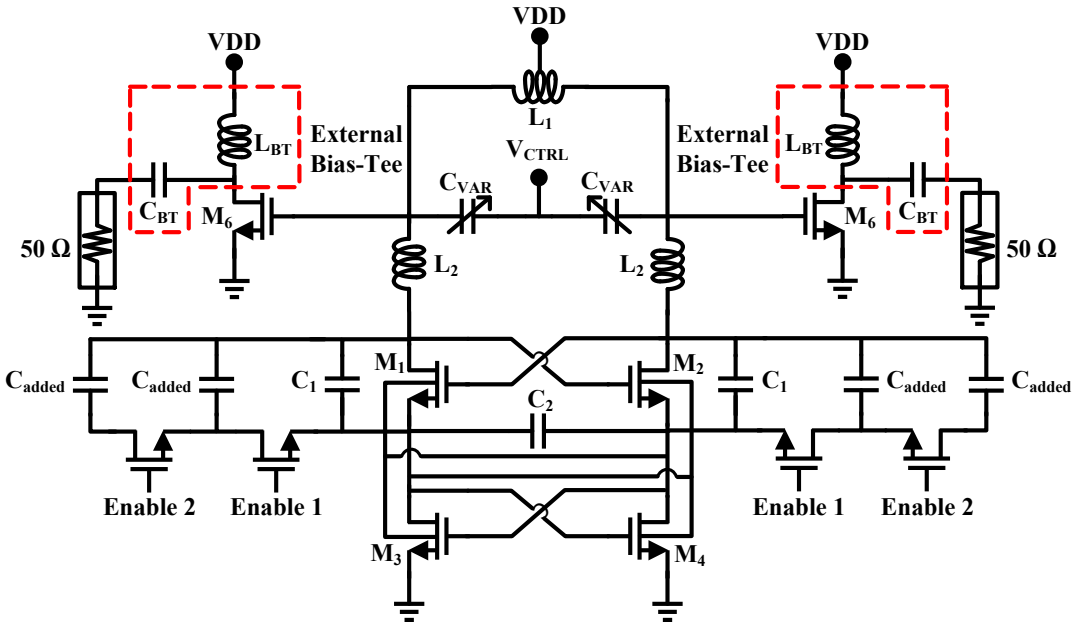

Figure 35. Schematic of the fabricated VCO.

To sustain oscillation at high frequencies without increasing the transistors' size, the inter-stage inductors, L_2, are designed. These inductors boost the negative transconductance and extend the tuning range, resulting in a low-power wide-tuning-range VCO. The center-tapped inductor is designed in the tank to facilitate DC biasing and save area. Moreover, to reduce the parasitic resistance and, in turn, achieve a higher quality factor, a striped inductor structure [12] is used in the tank. The top and cross sectional view of the implemented coil are shown in Figs. 36 (a) and (b), respectively.

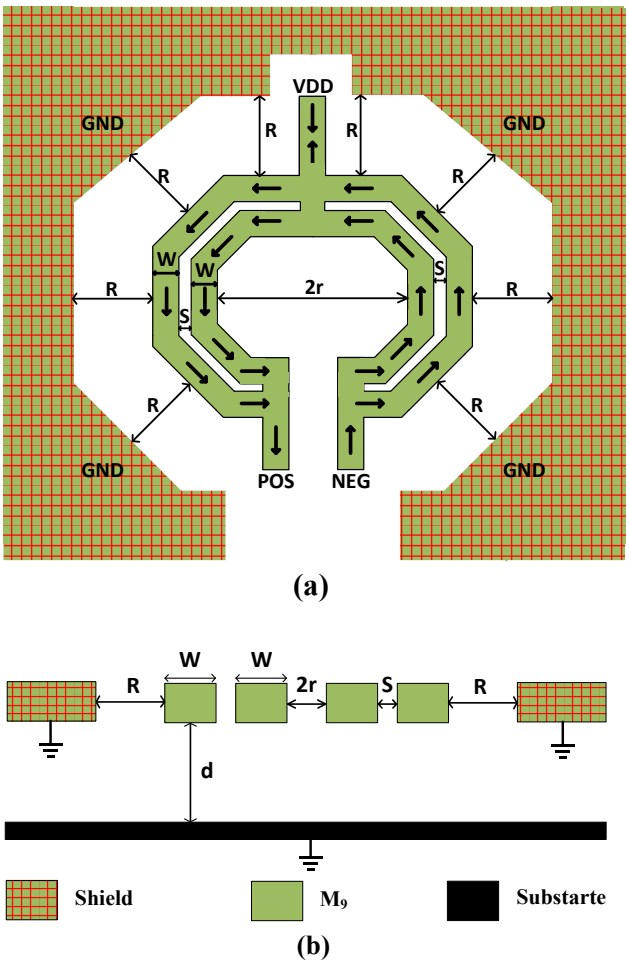

Figure 36. Different views of the proposed tank; (a) top; b) cross sectional.

The design parameters are *r*, *W*, *S*, and *R* which are the inner radius, width of the two parallel inductor traces, space between the two traces, and the outer radius, respectively. They are optimized to achieve the maximum possible quality factor in the frequency band of interest. Furthermore, a grounded shield ring using M_9 is designed to further enhance the quality factor at the desired frequency. This shielding layer significantly reduces the loss associated with the lossy substrate at high frequencies which results in a higher quality factor at the cost of lower inductance and higher parasitic capacitance. Full-wave Electromagnetic simulations using ADS Momentum are performed to evaluate the performance of the proposed tank.

Considering the process variations, the performance of the proposed VCO is simulated in different process corners. In order to improve the accuracy of simulations, a combination of post-layout and electromagnetic simulations are performed using Cadence and ADS Momentum. The simulation results are summarized in Table I verifying that the proposed VCO shows a robust performance over all process corners.

Table 1. The simulated performance summary of the proposed VCO over the process corners.

Corner	SS	TT	FF
TR (GHz)	24.8-29.4	25.1-29.9	25.3-30.3
TR (%)	17	17.5	18
Average PN (dBc/Hz)	–118.4	–120.3	–121.5
Average Power (mW)	1.65	2.3	3.35
Average FOM (dBc/Hz)	–183.9	–184.4	–184.9
Average FOM_T (dBc/Hz)	–188.5	–189.2	–190

Chapter 4. Measurement Results

4.1. Low-Phase-Noise Wide-Tuning-Range Mm-wave CMOS VCO

To validate the proposed architecture, a VCO with a tuning range from 50.1 to 59.8 GHz is designed and implemented in a 65-nm CMOS process. Fig. 37 shows the micrograph of the fabricated VCO. The area of the circuit excluding the pads is 260 μm × 250 μm. The supply voltage is 1 V and the power consumption for the VCO core is 6.2 mW. Two open-drain output buffers, biased using external Bias-Tees, are designed at the tank output for measurement purposes. These buffers collectively draw 8 mA from a 1-V supply. The VCO output is measured using on-wafer probing while the DC biasing of the circuit is supplied by bond wires. The measured output spectrum is illustrated in Fig. 38 showing that the center frequency of the fabricated VCO is ~55 GHz with the calibrated output power of –6.4 dBm. At the center frequency, VCO achieves a phase noise of –89.9 and –111.72 dBc/Hz at 1 and 10-MHz offset, respectively as depicted in Fig. 39. The measured PN at 10-MHz offset over the entire frequency tuning range is plotted in Fig. 40. The measured calibrated output power over the entire frequency tuning range is also shown in Fig. 41. Furthermore, based on Fig. 42, over different states of the switches, the tuning range including four frequency bands is over 18% resulting in a figure of merit (FOM) and FOM with tuning range (FOM_T) of –178.9 and –184 dBc/Hz at 10-MHz offset, respectively. Table III summarizes the performance of the proposed design along with comparison to that of the state-of-the-art designs also implemented in 65-nm CMOS. As can be seen from the table, the performance of the proposed design, particularly in terms of FOM and FOM_T compares favorably with other designs.

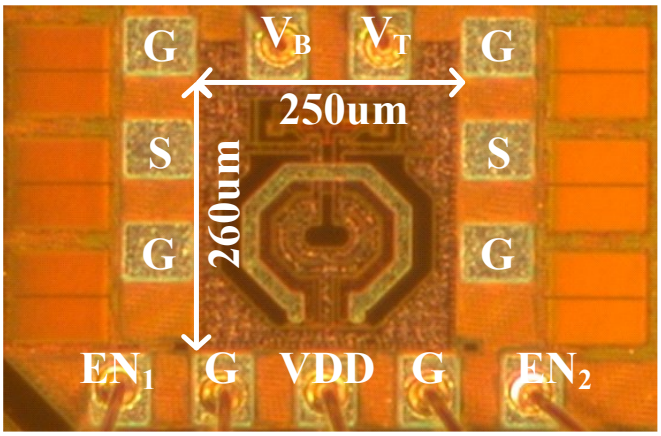

Figure 37. Micrograph of the fabricated 60-GHz VCO.

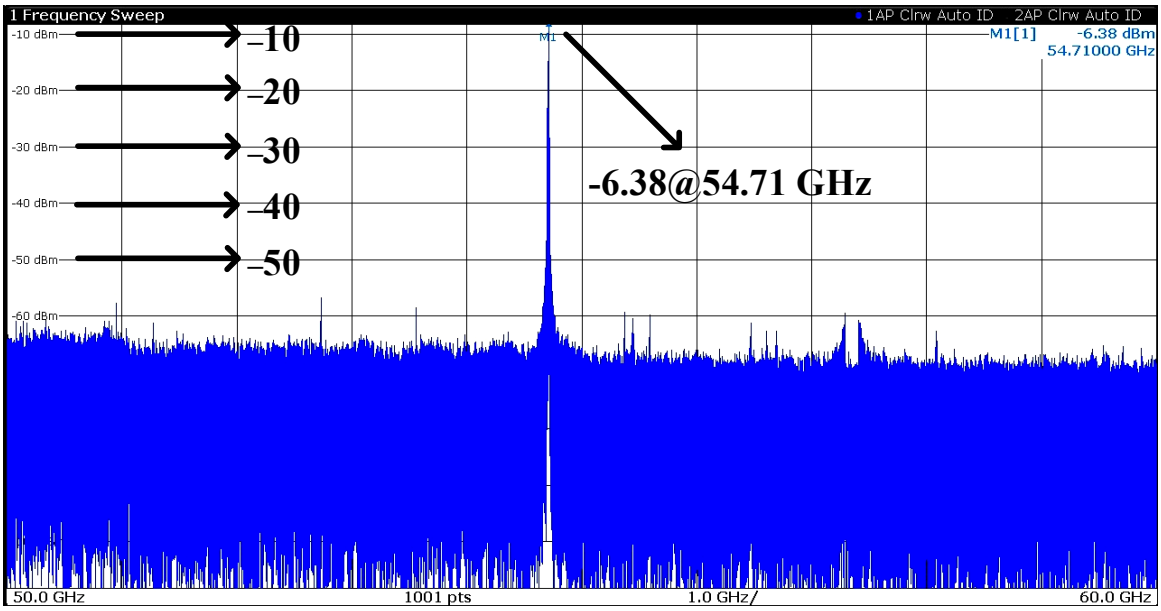

Figure 38. Output spectrum of the fabricated VCO.

The fabricated VCO is measured using a Rohde & Schwarz (R&S) FSW 26.5 GHz spectrum analyzer. A V-band external harmonic mixer, R&S Z75, is used as the frequency extender. The loss of the external mixer, probe (ZPROBE GSG 67 GHz), and the cable are measured and then inputted into the spectrum analyzer to de-embed the measured data. As mentioned in the paper,

two open-drain output buffers are designed at the VCO output for the measurement purpose which draw a total of 8 mA current from a 1-V supply.

The phase noise reported here is measured at the center frequency of oscillation. In our design, this reported phase noise is close to the average phase noise over the tuning range. The measured phase noise at 10-MHz offset over the entire frequency tuning range is also plotted in Fig. 40. Based on this figure, the best, average, and the worst case phase noise are –114.2, –111.9, and –109.9 dBc/Hz, respectively.

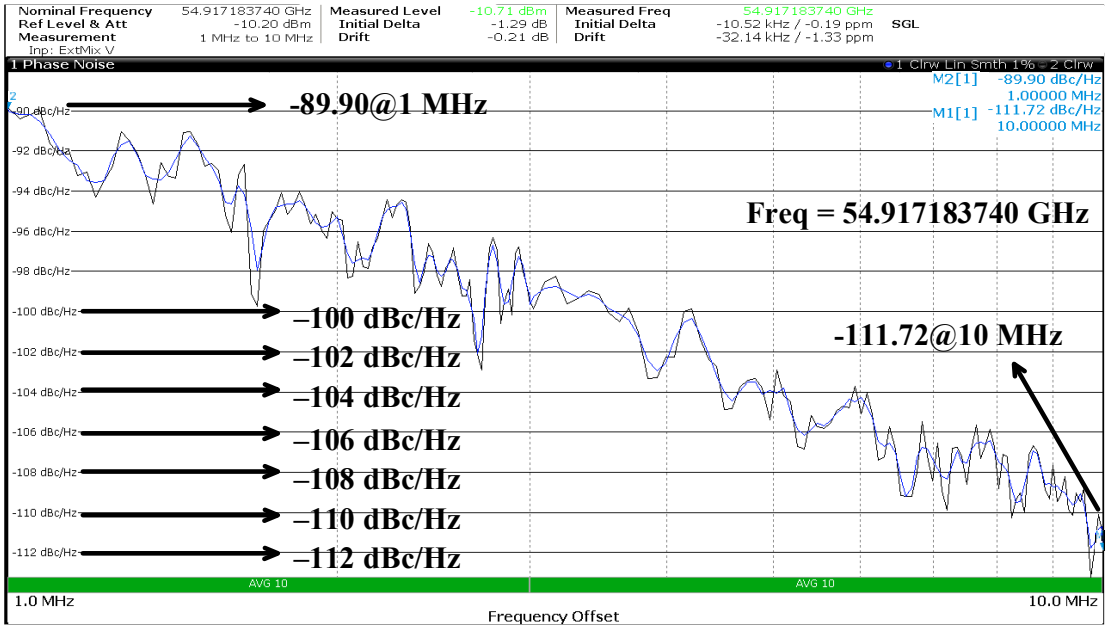

Figure 39. Measured phase noise at the center frequency of oscillation.

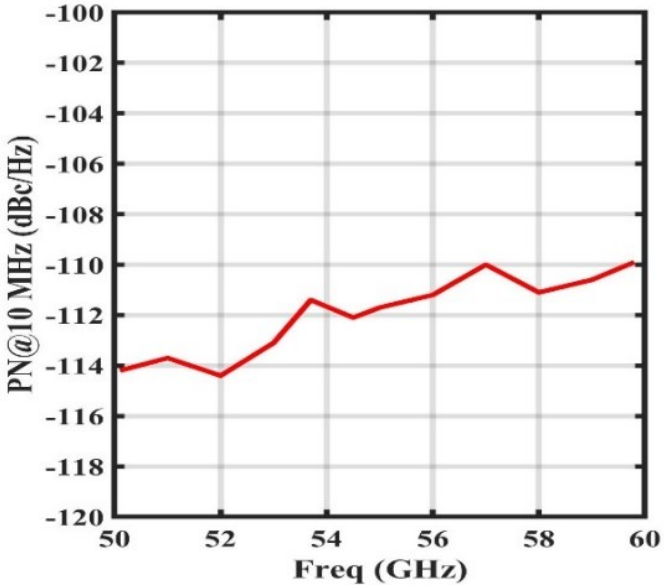

Figure 40. The measured PN at 10-MHz offset over the whole frequency tuning range.

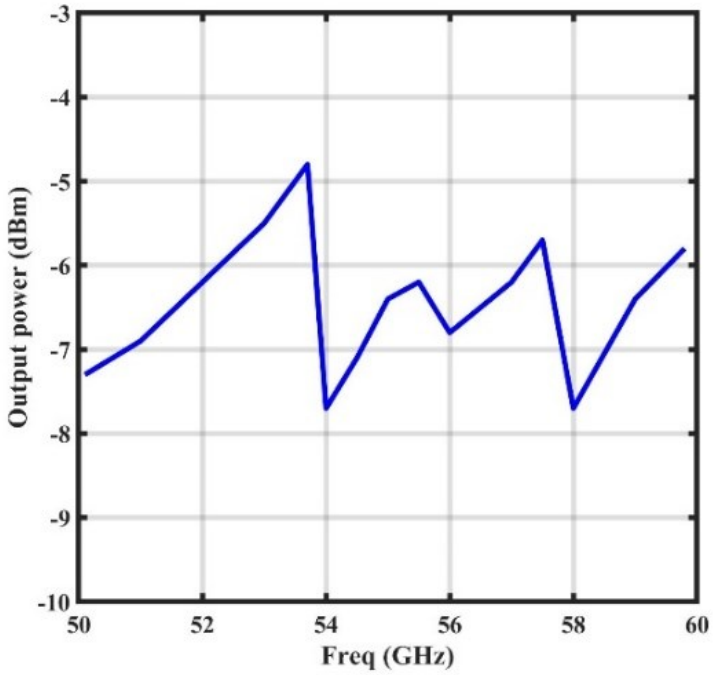

Figure 41. The measured output power over the whole frequency tuning range.

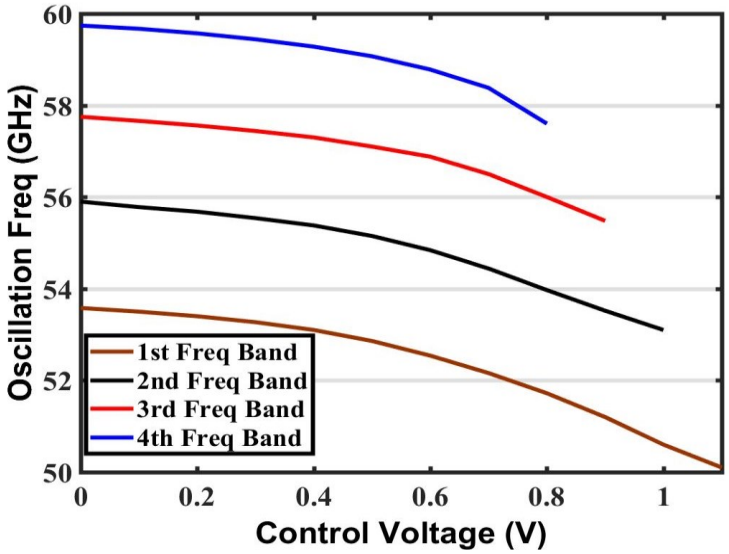

Figure 42. Measured frequency tuning range over different control voltages.

4.2. Low-Power Wide-Tuning-Range Mm-wave CMOS VCO

To validate the proposed architecture, a 28-GHz VCO suitable for 5G applications is designed and implemented in a 65-nm CMOS process. Fig. 43 shows the micrograph of the fabricated VCO laid in a CFP-24 package with bonding wires. The area of the circuit excluding the pads is 460 μm × 480 μm. The supply voltage is 1 V and the power consumption for the VCO core is 2.3 mW. The output buffers collectively draw 10 mA from a separate 1-V supply. The measurements were performed with the package mounted on a printed circuit board (PCB) and tested using on-wafer probing along with the bond wires for the DC biasing of the circuit. Also, large values of decoupling capacitors is realized using SMD capacitors placed in parallel between the supply voltage (VDD) and ground to relax the VCO from the supply noise in different frequency bands. The measured output spectrum is illustrated in Fig. 44 showing that the center frequency of the fabricated VCO is ~26 GHz with an uncalibrated output power of –17.8 dBm. The total loss of the probe and cable is measured as ~3 dB in the frequency band of interest. At the center frequency,

VCO achieves a phase noise of –86 and –122.1 dBc/Hz at 300-KHz and 10-MHz offset, respectively as depicted in Fig. 45. Furthermore, based on Fig. 46, over different states of the switches and sweeping the control voltage, the tuning range including three frequency bands is over 20%, from 23.7-GHz to 29-GHz resulting in a FOM and FOM with tuning range (FOM_T) of –187 and –193 dBc/Hz at 10-MHz offset from the center frequency of oscillation, respectively. Table IV summarizes the performance of the proposed design along with comparison to those of the state-of-the-art designs. As can be seen from the table, the performance of the proposed design, particularly in terms of phase noise, power, FOM, FOM_T, and FOM with considering the chip area (FOM_A) compares favorably with state-of-the-art.

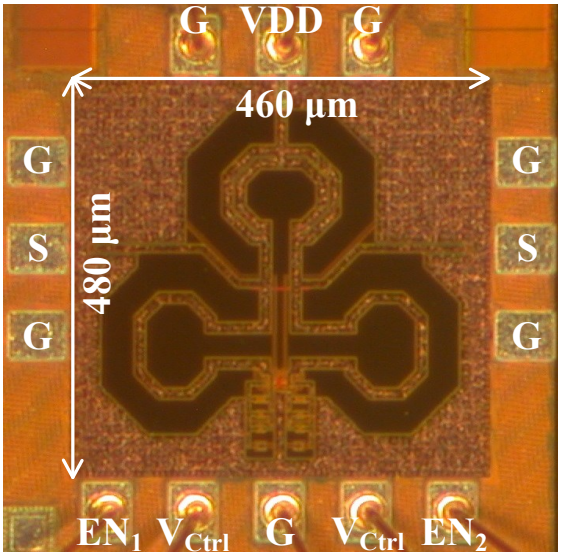

Figure 43. Micrograph of the fabricated 28-GHz VCO.

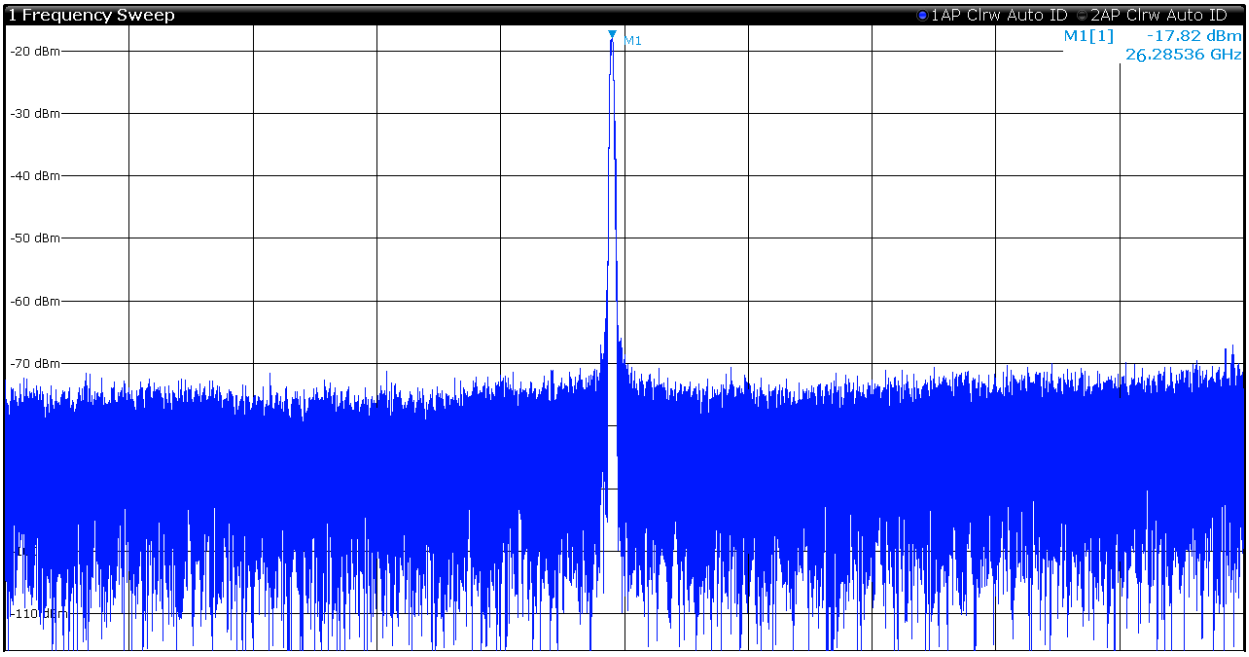

Figure 44. Measured output spectrum of the fabricated VCO.

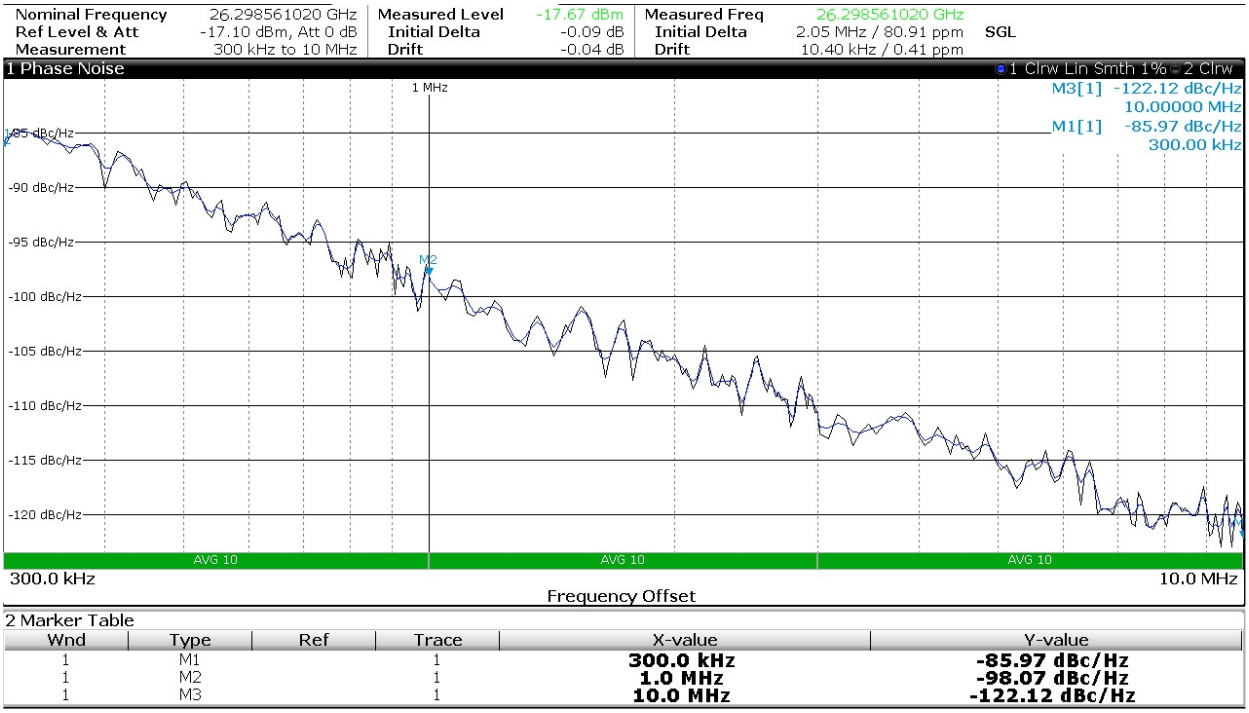

Figure 45. Measured phase noise of the fabricated VCO at the center frequency of oscillation.

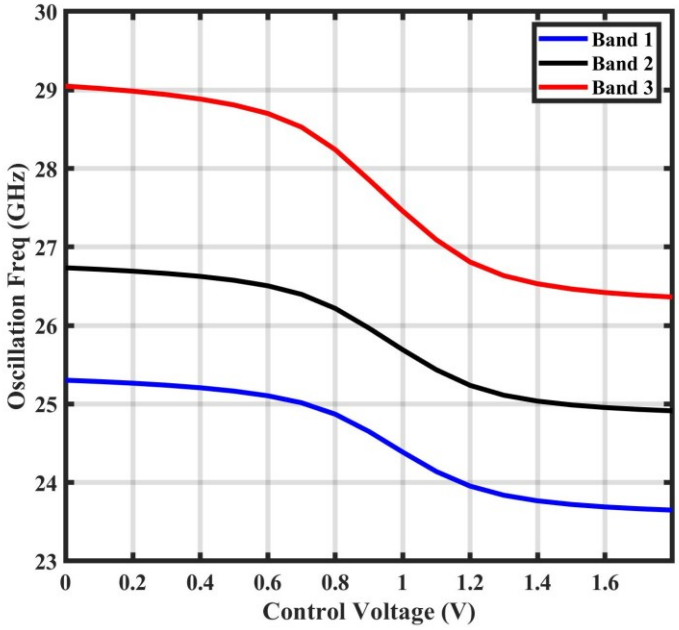

Figure 46. Measured tuning range of the fabricated VCO.

To evaluate the robustness of the fabricated VCO, the measured phase noise variation over the entire tuning range is plotted in Fig. 47. This figure shows that phase noise has a small variation of 2.8 dBc/Hz over the frequency band of interest.

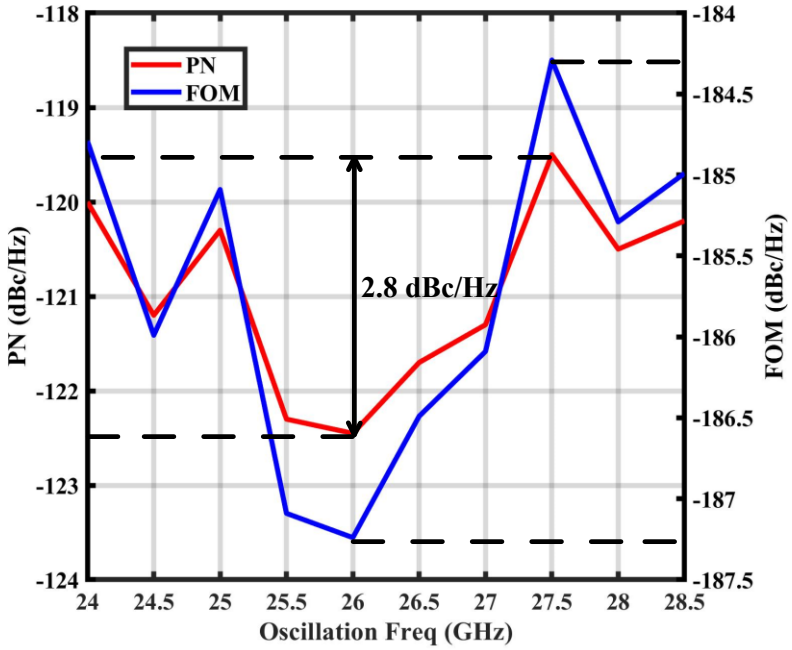

Figure 47. Measured PN and FOM at 10-MHz offset from the carrier over the entire tuning range.

To validate the sensitivity of the proposed VCO performance on the supply voltage, the measurement results for different values of supply voltage is presented in Table II. According to this table, although the overall performance is better for 1-V supply, the VCO still shows a satisfying performance for a supply of 0.8-V verifying the usefulness of the proposed VCO in both low-voltage and low-power applications. Note that for supplies less than 0.8 V, the VCO would not oscillate.

Table 2. The performance summary of the fabricated VCO for different supply voltages.

Supply (V)	0.8	0.9	**1**
TR (GHz)	25.5-30.2	25.1-30	**23.7-29**
TR (%)	16.9	17.8	**20.1**
Average PN (dBc/Hz)	–116.6	–119.1	**–121**
PN Variation (dBc/Hz)	9.6	5.3	**2.8**
Average Power (mW)	1.25	1.8	**2.3**
Average FOM (dBc/Hz)	–184.8	–185.1	**–185.8**
Average FOM_T (dBc/Hz)	–189.3	–190.1	**–191.8**

Chapter 5. Conclusions

5.1. Low-Phase-Noise Wide-Tuning-Range Mm-wave CMOS VCO

A transformer-based mm-wave VCO with wide tuning range and low phase noise is presented. It is shown that optimization of the secondary and tertiary coils inductances and the coupling factor between them improve the phase noise substantially as compared to the conventional designs. By switching in and/or out the secondary and the tertiary coils of the transformer, 4 overlapping frequency sub-bands are implemented which collectively result in a wide tuning range. Design techniques that are proposed to implement a high-Q tunable inductor for the tank allow the VCO to achieve a competitive phase noise performance. As a proof of concept, a 55-GHz VCO is implemented in a 65-nm CMOS process. The following Table summarizes the performance of the proposed design and compares it with that of the state-of-the-art.

Table 3. Performance summary of 60-GHz VCOs in 65-nm CMOS.

VCO	[7]	[18]	[19]*	[20]	**This work**
Center Freq. (GHz)	61	77	63	66.1	**55**
Average PN @10 MHz (dBc/Hz)	–108.3	–108.4	–92.2	–103	**–111.9**
TR (%)	14.2	15.8	24.6	27.9	**18**
Power (mW)	6	14.3	21.5#	13	**6.2**
[1]FOM@10MHz (dBc/Hz)	–176.2	–174.5	–174.8	–168.3	**–178.9**
[2]FOM_T@10MHz (dBc/Hz)	–179.3	–178.5	–182.6	–177.2	**–184**

*Measured at 1-MHz offset from the carrier frequency
#Including the output buffer

[1] $FOM = PN|_{f_{offset}} - 20\log[\frac{f_{osc}}{f_{offset}}] + 10\log[\frac{P_{DC}}{1mW}]$

[2] $FOM_T = FOM + 20\log[\frac{TR(\%)}{10}]$

5.2. Low-Power Wide-Tuning-Range Mm-wave CMOS VCO

A mm-wave VCO architecture based on Colpitts design and achieving wide tuning range and low phase noise is presented. A novel capacitor bank design substantially minimizes the phase noise degradation as compared to the conventional designs. By switching in and/or out the capacitor bank, 3 overlapping frequency sub-bands are implemented which collectively result in a wide tuning range. Moreover, inter-stage inductors are designed and placed between the gm-cell and the tank as the gm-booster. The proposed technique not only relaxes the start-up and power consumption issues common to conventional Colpitts oscillators, but it also improves the tuning range by reducing the parasitic capacitance seen by the tank. Furthermore, a body bias technique is utilized to further reduce the power consumption and improve the phase noise. As a proof of concept, a 28-GHz VCO suitable for 5G applications is implemented in a 65-nm CMOS process. Design techniques proposed to implement a high-performance mm-wave VCO allows for achieving a competitive FOM, FOM_T, and FOM_A in comparison with state-of-the-art designs. Table IV summarizes the performance of the fabricated VCO.

Table 4. Performance comparison with that of the state-of-the-art designs.

VCO	Tech (nm)	Freq (GHz)	PN (dBc/Hz)	Power (mW)	TR (%)	Area mm^2	FOM[1] (dBc/Hz)	FOM_T[2] (dBc/Hz	FOM_A[3]
MTT'17 [1]	65	26.3	-119.1	4.3	40.3	0.25	-180	-192.1	-186
MWCL'14 [9]	65	27.5	–113	6	43.3	0.81	-174.3	–187	-175.2
TCASII'13[25]	130	40	–95	12	27	1.93	-176.3	–184.9	-173.4
MTT'17 [26]*	90	20.85	-100.7	8.1	15.8	0.48	-177.8	-181.8	-183.3
IMS'09 [28]*	130	23	-100	4	2	0.32	-181	-167	-186
MWCL'17 [29]*	180	24	-101.3	25#	12.6	0.23	-174.9	-176.9	-181.5
This work	**65**	**26.3**	**–122.1**	**2.3**	**20.1**	**0.22**	**–187**	**–193**	**-193.6**

*Measured at 1-MHz offset from the carrier frequency #Including the output buffer

[1] $FOM = PN|_{f_{offset}} - 20\log[\frac{f_{osc}}{f_{offset}}] + 10\log[\frac{P_{DC}}{1mW}]$ [2] $FOM_T = FOM + 20\log[\frac{TR(\%)}{10}]$ [3] $FOM_A = FOM + 10\log[\frac{Area(mm^2)}{1mm^2}]$

Future Work

The performance of the proposed VCOs can be further improved in terms of efficiency and output power. For efficiency, one can investigate techniques to improve the DC to RF efficiency of the proposed mm-wave VCO. In the context of output power, one can explore design techniques for providing output power in the range of 0 dBm and more to eliminate the use of LO buffer stages. Eliminating the buffers in turn help reducing the overall power consumption.

Another interesting path is to look into techniques to increase the operation frequency. The operation frequency extension to 100 GHz and beyond requires elaborate techniques as the operation frequency becomes closer to the cut-off frequency of the transistors. For example, in the technology used in this research, which is 65-nm CMOS technology, the cut-off frequency is about 120 GHz. Designing a robust VCO operating in frequencies in the vicinity or higher than 120 GHz is still challenging.

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