Smart Electronic Loads for Harmonic Compensation in Future Electrical Distribution Systems

by

Hua Chang

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Abstract

Common solutions to mitigating harmonics and improving power quality of power systems would include installing dedicated passive or active harmonic filters at the point of common coupling (PCC). However, as the complexity of energy systems increases with integration of renewables and storage systems on the one side, and the number of electronic loads increases rapidly on the other, the centralized compensation of harmonics may not be cost effective. At the same time, many modern loads and energy sources have high–bandwidth front–end power converters that present an opportunity for alternative solutions to improve power quality.

This thesis presents a new methodology to compensate harmonics. Utilizing widely deployed smart meters, the measured information of harmonics can be transmitted in real time through the internet to smart electronic loads, where the loads can inject out–of–phase harmonics for compensation in a distributed fashion. First, this thesis investigates the feasibility of using smart meter measurements in the Fred Kaiser Building on the University of British Columbia (UBC) Vancouver campus, which are then used to demonstrate potential harmonic compensation using installed grid–tied converters. Next, since many modern single–phase electronic loads include a power factor correction (PFC) stage, this thesis develops a PFC controller algorithm to inject typical harmonics (i.e. 3^{rd}, 5^{th}, and 7^{th}) at different levels and phase angles for compensation. This concept is further extended to smart LED drivers that also have a PFC stage, which are envisioned to have advanced power quality features. Such smart electronic loads and LED drivers can be integrated into future distribution systems of residential/commercial

buildings, microgrids, etc., with distributed controls and communications through Internet of Things (IoT)/advanced user interfaces.

Lay Summary

Harmonics introduce a power quality issue and are typically associated with additional losses while threatening to damage other equipment. This thesis presents a new methodology to compensate harmonics in electrical distribution systems. Utilizing widely deployed smart meters capable of measuring harmonics, this information can be transmitted through the internet to smart electronic loads, and these loads can compensate harmonics in a distributed fashion. This thesis investigates the feasibility of using smart meter measurements in commercial buildings for harmonic compensation using pre–installed devices. Next, since many modern electronic loads are capable of integrating harmonic compensation features, this thesis develops an algorithm for modifying the controller of these devices. Lastly, this concept is further extended to smart LED drivers. It is envisioned that such smart electronic loads and LED lighting can be integrated into future distribution systems of residential/commercial buildings, microgrids, etc., with distributed controls and communications.

Preface

Some of the contents and results presented in this thesis have been published in conference proceedings and presented at conferences. I am the primary contributor responsible for deriving formulations, developing computer models, running simulations, designing experimental prototypes, and conducting hardware experiments, which have been used in all manuscripts. Part of this thesis, specifically the work in Chapter 3, was completed in collaboration with and supported by Alpha Technologies Ltd., whose engineers, Victor Goncalves and Rahul Khandekar, supplied the project with the industrial rectifier prototype and the core software codes used in their controller. The work presented in Chapter 4 was done in collaboration with OmniSolu Ltd., and I received very helpful design tips and advice from their engineers, Yan Zhang, Jane Wang, and Antonio Wang, for designing my own LED driver prototype.

My research advisor at UBC, Dr. J. Jatskevich, has been interactively providing feedback on all of my manuscripts, including formulating ideas and iterating on the drafts of publications. I have also received help from the other co–authors, Yingwei Huang and Seyyedmilad Ebrahimi, in the form of critical discussions, iterating and editing the drafts of papers, and analyzing and presenting the results.

A version of Chapter 2 has been published; H. Chang, Y. Huang, S. Ebrahimi and J. Jatskevich, “Smart Meter Based Selective Harmonics Compensation in Buildings Distribution Systems with AC/DC Microgrids” in *Proc. IEEE Power Energy Soc. Gen. Meet*., Chicago, IL, USA, Jul. 2017. Further, Dr. Jatskevich, Seyyedmilad Ebrahimi, and Yingwei Huang provided useful feedback and revised this manuscript.

A version of Chapter 3 has also been published; H. Chang, Y. Huang, S. Ebrahimi and J. Jatskevich, “Harmonic Compensation in AC Distribution Systems Using Smart Electronic Loads with PFC Converters” in *Proc. 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics*, San Francisco, CA, USA, Jul. 2017. Dr. Jatskevich, Seyyedmilad Ebrahimi, and Yingwei Huang also provided great insight on this manuscript and helped with manuscript revisions.

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List of Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
AHF	Active Harmonic Filter
CCM	Continuous Conduction Mode
CFL	Compact Fluorescent Light
CRM	Critical Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DG	Distributed Generation
EMI	Electromagnetic Interference
GTI	Grid–tie Inverter
HCL	Harmonic Correction Loop
HDC	Harmonic Distortion Coefficient
ICT	Information and Communication Technology
IoT	Internet of Things
LED	Light Emitting Diode
MCU	Microcontroller unit
PC	Personal Computer
PCC	Point of Common Coupling
PFC	Power Factor Correction
PLL	Phase Lock Loop

PWM	Pulse Width Modulation
RHM	Relative Harmonic Magnitude
SCADA	Supervisor Control and Data Acquisition
SMPS	Switched Mode Power Supplies
THD	Total Harmonic Distortion
UART	Universal Asynchronous Receiver–Transmitter
VFD	Variable Frequency Drive

Acknowledgements

First of all, I would like to express my endless appreciation and gratitude to my research supervisor, Dr. Juri Jatskevich. Without his vision, expertise, guidance, and continuous encouragement that he provided to me during all of my years at UBC since my baccalaureate degree, I would not have come this far in my education and professional development. He encouraged me to pursue the advanced MASc degree, and I can see and appreciate now how much of a difference this degree has made in my life so far, and for my professional career in the future.

I also would like to acknowledge the financial support I received for this research which came from the Natural Science and Engineering Research Council (NSERC) of Canada, under the Strategic Project Grant (SPG) entitled "Advanced Integrated AC–DC Systems for Energy Efficient Buildings and Communities in Canada," and under the Engage Grant entitled "Smart Harmonic Compensation based on LED Lighting Systems," both led by Dr. Juri Jatskevich as the principal investigator.

What made the present research particularly interesting to me is that it had both futuristic technological vision and practical industrial applications. In this regard, I also would like to acknowledge the contributions and collaboration of my industrial partners. I would like to thank Victor Goncalves and Rahul Khandekar from Alpha Technologies Ltd., for sharing with me their ideas and vision about the future of the telecom power supply industry and related challenges, and for providing me the necessary hardware prototypes of industrial state–of–the–art rectifiers as a platform to conduct my research experiments and demonstrations of the control algorithms. I would also like to thank Yan Zhang, Jane Wang, and Antonio Wang from OmniSolu Ltd., for

enlightening me with their visions for the integrated LED systems and the IoT, and for helping me design my own experimental LED drive prototype with advanced features and capabilities.

I am also grateful to Dr. Jose Marti and Dr. William Dunford for dedicating their valuable time and effort to serve on my examining committee, and for all of their useful feedback that contributed to the improvement of my thesis.

I owe a sincere debt of gratitude to many of my friends and fellow graduate students from the UBC's Electric Power and Energy Systems research group, including Yingwei Huang, Milad Ebrahimi, Saeed Rezaee, Navid Amiri, Zhi Qu, Jiayue Xu, Zejun Yang, Shuai Xu, Xiaotong Wang, Zemeng, Wang, Dr. Zhenyu Shan, Alex Piznuir, and many others, with whom I collaborated on research and spent countless hours in the lab.

Lastly, I would like to express my deepest gratitude to my parents, Qing Chang and Yun Hua, and family members, Hong Chang, Jian Chen, Jiang Chang, Xuan Zhao, Binzhe Chang, Wenhui Sun, Chen Chen, Yue Chang, and Xin Chang, for their endless encouragement and support of my education in Canada at UBC.

Chapter 1: Introduction

1.1 Smart Grid and Internet of Things

The existing power grid has a history spanning over 100 years, which now faces many challenges as the demand for power and the integration of renewable energy increase. The next generation of power grid, often referred to as the "smart grid" and many of its elements, is currently being deployed across the world [1]. The smart grid, together with rapidly advancing information and communication technology (ICT), will enhance utilities with full visibility and pervasive control over their infrastructures, achieve better efficiency, reliability and safety, and will enable many new features and functionalities for increased consumer participation [2].

Another technology theme, called the Internet of Things (IoT), also based on ICT, offers a broader vision to oversee the physical world and control of individual devices within a distributed network [3] [4]. Within this IoT theme, devices are envisioned to access more information and embed sophisticated controllers which will possess some level of "intelligence". As IoT technology develops, more and more devices will start to utilize the benefit of interconnections with each other and share information. Applications such as electrical distribution systems and electronic loads are envisioned to evolve with the IoT, and one day traditional wired switches may be replaced by wirelessly–controlled switches. LED lighting is strongly positioned to replace conventional incandescent or compact florescent lighting, and to achieve a close integration within the working or living environment for consumers or industrial customers. Users will be provided with new features such as light dimming and color adjusting though their cellphones or systems of sensors. Many companies are taking innovative steps to propose future devices with such enhanced capabilities through the IoT.

Both smart grid and IoT are promoting more interconnection and information sharing across the large–scale power network and small consumer–level devices, which will enable many smart grid applications. For instance, many utilities have been upgrading conventional electricity meters to smart meters, which are capable of informing utilities of electricity usage and even harmonics in nearly real–time, so that further actions can be taken. For example, UBC's Fred Kaiser building is currently equipped with a Schneider Electric ION 7330 smart meter, shown in Figure 1.1. This meter is installed at the 600V bus where power enters the building, which is often referred to as the point of common coupling (PCC). Modern smart meters may be also equipped with features such as harmonic monitoring (up to 31st harmonic), total harmonic distortion (THD) calculation, as well as real–time data reporting as often as every second through the internet [37]. As a result, modern smart meters may be integrated through the IoT with other devices used in smart grid enabling other applications and functionalities.

Figure 1.1 Example of Schneider Electric ION 7330 smart meter installed in Kaiser building on UBC campus.

1.2 Power Quality and Harmonic Filters

One of the trends of modern electrical systems is the increased proliferation of non–linear electronic loads. Although some of these loads are designed with sophisticated rectifiers and are

supposed to produce a signature very closely resembling that of a simple resistive load, many or most inexpensive electronic loads produce large harmonics and introduce various additional power quality problems. Power quality can be categorized by various aspects like voltage sag, swell, overvoltage, under–voltage, harmonics, transients, noise, etc. [5] [44]. In this thesis we consider harmonics generated by grid–connected devices, as excess harmonics may cause heating and increase losses in some equipment (e.g. transformers) [6]. Overall, harmonics such as 3^{rd}, 5^{th} and 7^{th} are often significant and may result in poor THD at the PCC, which ultimately leads to voltage distortion and worsens power quality.

In modern utility grids, electronic loads can produce current harmonics due to the common use of front–end line–commutated rectifiers. Loads such as computers with switched mode power supply (SMPS), ventilation with variable frequency drive (VFD), lighting with compact florescent light (CFL) and light emitting diode (LED), etc., may contain line–commutated rectifiers [7]–[9]. Furthermore, traditional linear loads such as directly-fed induction motors, incandescent lighting, uncontrolled heaters, etc., generally lack control functions. Because of this, these loads are being replaced with electronically controlled modern equivalents. Therefore, there is a tendency towards increased harmonics in distribution systems of modern buildings, industrial or commercial sites, office buildings, and communities.

Loads in distribution systems generally must adhere to IEEE standards and regulations [29], [38], and the amount of harmonics is not supposed to exceed specified levels. For instance, a typical fluorescent light ballast with less than 20% THD and PF greater than 0.9 can be accepted in the North American consumer market [10]. Equipment consisting of the new generation of SMPS generally produces low THD with relatively high PF at full load. However, many examples of equipment, such as PCs [11] [12], may not achieve the same power quality

performance in idle mode due to the discontinuous conduction mode (DCM) in a typical PFC stage. Overall, harmonics such as 5^{th} and 7^{th} are often significant, which may result in poor THD at the PCC.

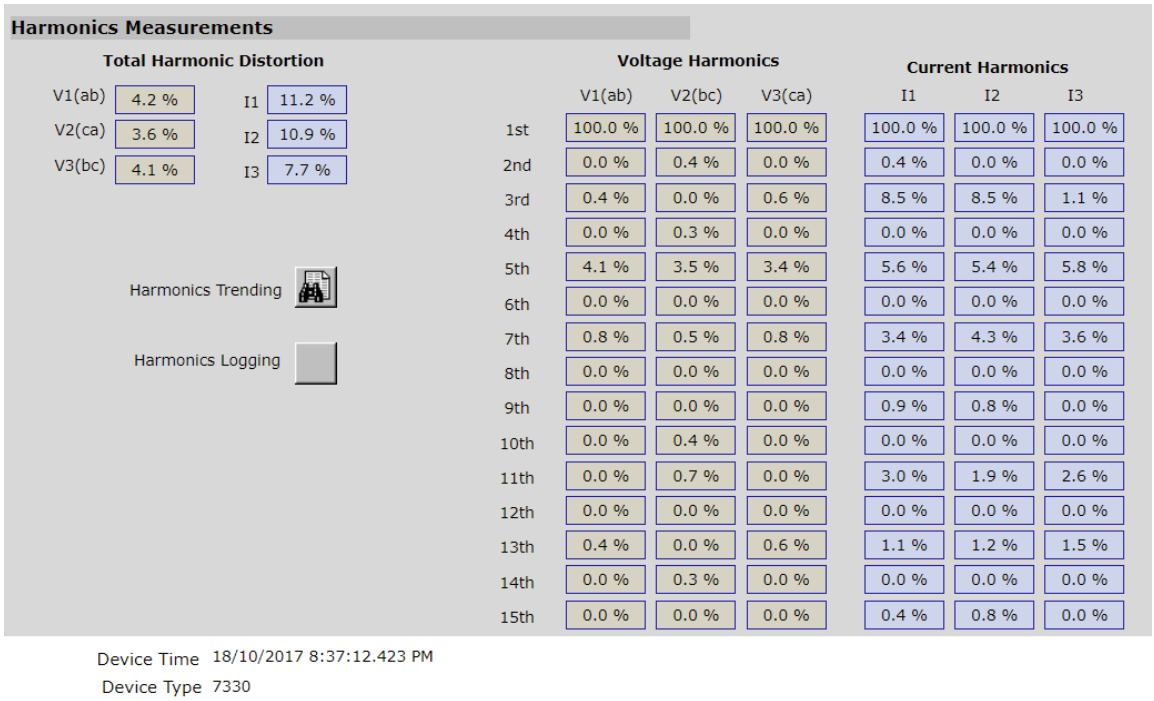
In addition to standards and regulations, passive and active harmonic filter (AHF) may be used for system level compensation [13]–[15] [43], and many of such methods have been presented in literature. Generally, both methods require installing additional devices or large filters at the PCC. Passive filters, usually the RLC type, occupy large space and need to be well–tuned. Also, they are only functional at certain operating regions and therefore may further lower power quality when the device operates out of the designated region. In contrast, power–electronics–based active filters have a much wider range of operating regions and more power density. However, they are more complex than passive devices, require installation of additional voltage/current sensors at PCC, and have high cost. As a result, both methods have significant drawbacks in terms of compensation capacity, additional space, and cost.

1.3 Motivation

To integrate increasing penetration of DGs such as solar and wind power generation, as well as growing numbers of energy storage and backup power systems, the co–existence of traditional AC grids with evolving DC systems becomes inevitable [7]–[9]. Moreover, modern systems are more complex due to increasing utilization of nonlinear electronically–interfaced loads such as SMPS, VFD, CFL and LED lighting, etc. Microgrid systems, as a part of smart grid, are becoming very attractive for many applications [16]. However, preserving the power quality of such hybrid AC/DC systems becomes more challenging as complexity increases.

It is envisioned that traditional centralized passive and active harmonic filter methods cannot adapt to fast growing hybrid AC/DC systems as the number of loads and interconnections increases. Therefore, effective harmonic compensation is still out of reach for many users in practice, including many existing residential, commercial, and office buildings. To give the reader a specific idea of power quality for some of the existing and relatively new buildings on the UBC Vancouver campus, measured harmonic data snapshots for three example buildings are shown in Figure 1.2, Figure 1.3, and Figure 1.4, respectively. These buildings were built in an ascending order: ICICS concluded in 1993; Kaiser was finished in 2005; and Pharmaceutical was finished very recently in 2012. As can be seen in these figures, a fairly noticeable harmonic and phase unbalance exists in all three buildings. Specifically, the THD of the phase currents in the ICICS building ranges from 7.7% to 11.2%. The THD for currents in Kaiser ranges from 4.8% to 8.9%, which is slightly better than in ICICS. Finally, the newest building, Pharmaceutical, demonstrates the highest current THD, ranging from 15.8% to 17.9%. Indeed, this new building has more electronic equipment and loads that are clearly contributing to the worst power quality of the three examples.

Thus, it is essential to develop new approaches that are cost–effective and scalable, together with the growing electrical infrastructure of buildings and communities. Moreover, embracing the vision for a smart electrical grid and advanced ICT and IoT, the solution to power quality and management of harmonics may be found through the use of many smart electronic loads and devices that are installed in a distributed manner and are interconnected among themselves through their advanced controls.



Harmonics Measurements

Total Harmonic Distortion

V1(ab)	4.2 %	I1	11.2 %
V2(ca)	3.6 %	I2	10.9 %
V3(bc)	4.1 %	I3	7.7 %

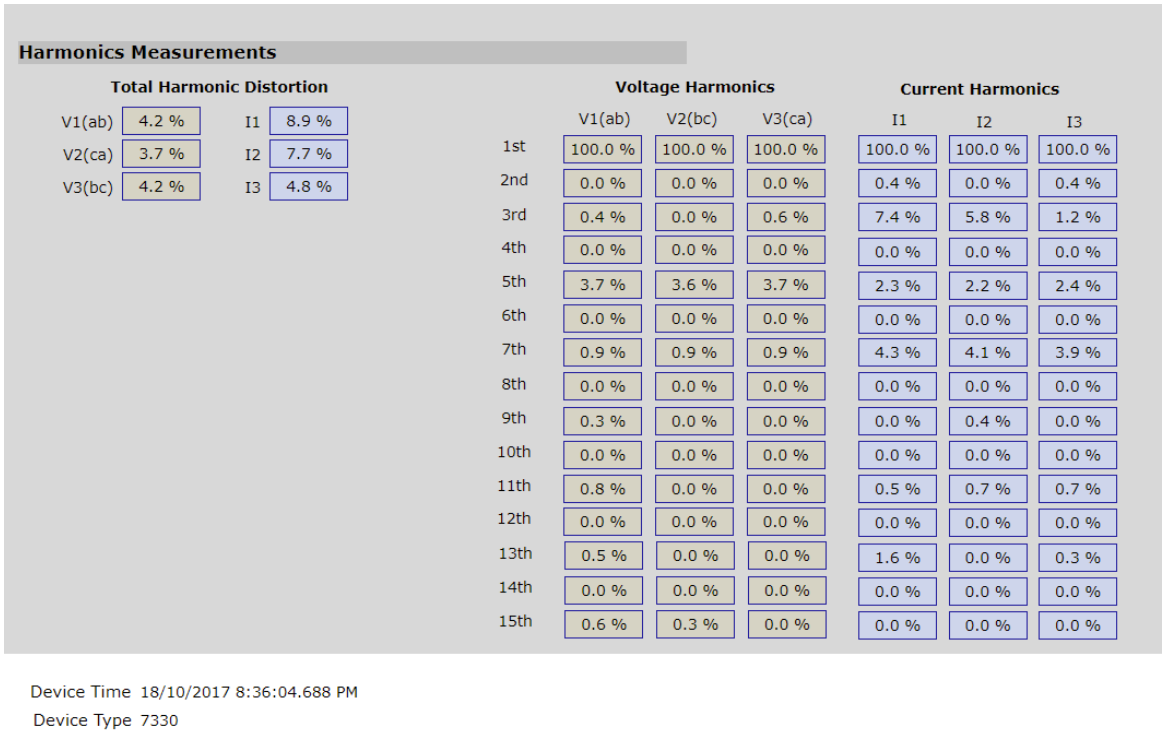
Harmonics Trending

Harmonics Logging

	Voltage Harmonics			Current Harmonics		
	V1(ab)	V2(bc)	V3(ca)	I1	I2	I3
1st	100.0 %	100.0 %	100.0 %	100.0 %	100.0 %	100.0 %
2nd	0.0 %	0.4 %	0.0 %	0.4 %	0.0 %	0.0 %
3rd	0.4 %	0.0 %	0.6 %	8.5 %	8.5 %	1.1 %
4th	0.0 %	0.3 %	0.0 %	0.0 %	0.0 %	0.0 %
5th	4.1 %	3.5 %	3.4 %	5.6 %	5.4 %	5.8 %
6th	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %
7th	0.8 %	0.5 %	0.8 %	3.4 %	4.3 %	3.6 %
8th	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %
9th	0.0 %	0.0 %	0.0 %	0.9 %	0.8 %	0.0 %
10th	0.0 %	0.4 %	0.0 %	0.0 %	0.0 %	0.0 %
11th	0.0 %	0.7 %	0.0 %	3.0 %	1.9 %	2.6 %
12th	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %
13th	0.4 %	0.0 %	0.6 %	1.1 %	1.2 %	1.5 %
14th	0.0 %	0.3 %	0.0 %	0.0 %	0.0 %	0.0 %
15th	0.0 %	0.0 %	0.0 %	0.4 %	0.8 %	0.0 %

Device Time 18/10/2017 8:37:12.423 PM
Device Type 7330

Figure 1.2 Smart meter harmonic data capture for the ICICS building.



Harmonics Measurements

Total Harmonic Distortion

V1(ab)	4.2 %	I1	8.9 %
V2(ca)	3.7 %	I2	7.7 %
V3(bc)	4.2 %	I3	4.8 %

	Voltage Harmonics			Current Harmonics		
	V1(ab)	V2(bc)	V3(ca)	I1	I2	I3
1st	100.0 %	100.0 %	100.0 %	100.0 %	100.0 %	100.0 %
2nd	0.0 %	0.0 %	0.0 %	0.4 %	0.0 %	0.4 %
3rd	0.4 %	0.0 %	0.6 %	7.4 %	5.8 %	1.2 %
4th	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %
5th	3.7 %	3.6 %	3.7 %	2.3 %	2.2 %	2.4 %
6th	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %
7th	0.9 %	0.9 %	0.9 %	4.3 %	4.1 %	3.9 %
8th	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %
9th	0.3 %	0.0 %	0.0 %	0.0 %	0.4 %	0.0 %
10th	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %
11th	0.8 %	0.0 %	0.0 %	0.5 %	0.7 %	0.7 %
12th	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %
13th	0.5 %	0.0 %	0.0 %	1.6 %	0.0 %	0.3 %
14th	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %	0.0 %
15th	0.6 %	0.3 %	0.0 %	0.0 %	0.0 %	0.0 %

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Device Type 7330

Figure 1.3 Smart meter harmonic data capture for the Kaiser building.

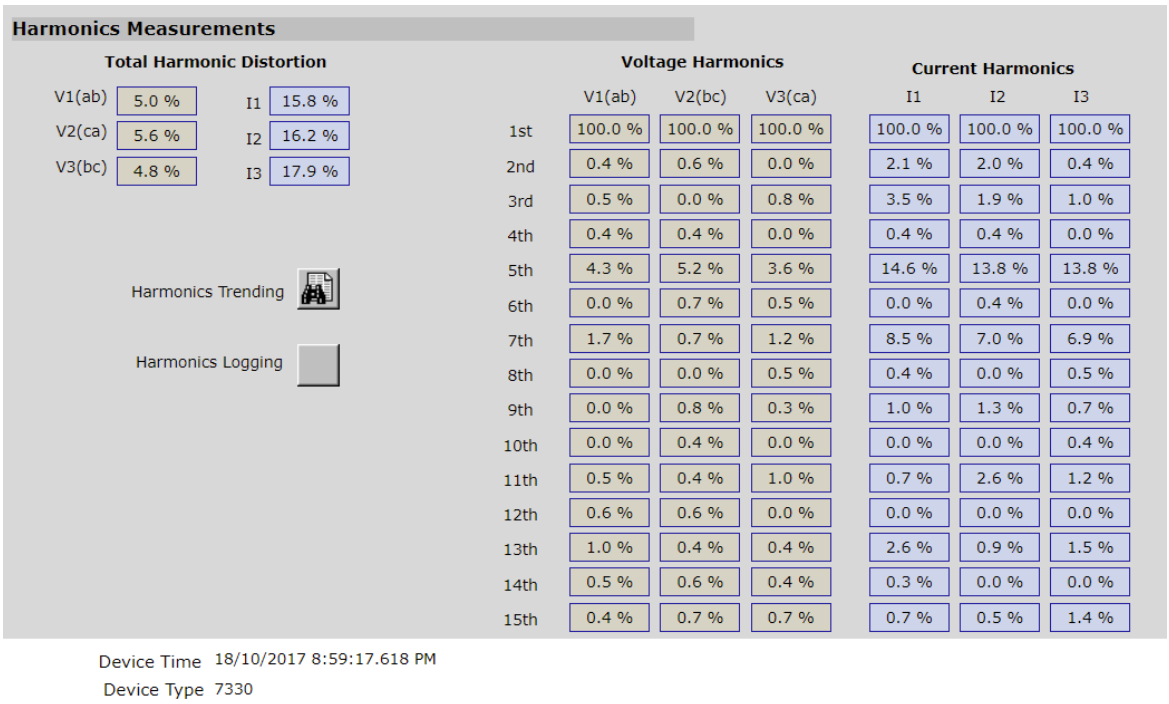

Figure 1.4 Smart meter harmonic data capture for the Pharmaceutical building.

1.4 Research Objectives

The main aim of this research is to develop "smart electronic loads" that are able to communicate with smart meter, each other, and customers via the IoT, and together fulfill the power quality control function of harmonic compensation within a given distribution system or microgrid. The work presented in this thesis includes simulations and experimental studies that are carried out on commercial devices and specially constructed hardware prototypes. Therefore, the overall goal of this project may be subdivided into the following research objectives:

1.4.1 Objective 1: Feasibility of smart loads in existing AC/DC distribution systems of buildings

Objective 1 is to investigate the feasibility of improving power quality in a building distribution system that has hybrid AC/DC loads and energy storage, and/or large electronically–interfaced uninterruptable power supplies. The measurements here are assumed to come from a smart meter. The Kaiser building on the UBC campus has a smart meter installed at its PCC, from which information including harmonic measurement is available to the public via the internet. Moreover, this building is equipped with integrated energy storage as well as an AC/DC microgrid system for research and operational needs. This objective involves collecting historical smart meter data and modeling the building's electrical distribution system based on accessible documentation. The studies are conducted based on measured harmonic data and detailed models of the overall system implemented in Matlab/Simulink.

1.4.2 Objective 2: Demonstration of a commercial device as a smart load for harmonic compensation

In a conventional building or house, the AC distribution system wiring is done in single phase, where most of the loads are also single phase AC loads. Many advanced electronic loads will have an input stage with a power factor correction (PFC) converter. Using the existing electronic loads with PFC capability for harmonic compensation purposes may appear as an attractive and low-cost option for monitoring and controlling power quality in a distributed manner. Thus, this objective investigates the feasibility of reprogramming the controller of one existing commercially-available rectifier load with a front–end PFC converter for harmonic compensation. This investigation is carried out using detailed simulation of the test system

developed in MATLAB/Simulink using PLECS. Experimental results of objective 2 are carried out using a commercial rectifier with PFC based on the Alpha Technologies, Ltd. product that was provided by the company for this research. The existing digital controller of the Alpha PFC–based rectifier has been re–programmed to include the injection of compensating harmonics and to validate the proposed approach.

1.4.3 Objective 3: Design and demonstration of a smart LED driver for future lighting applications with harmonic compensation capabilities

LED lighting is posed to quickly replace remaining incandescent lighting, and potentially more recent compact florescent lighting, in homes, commercial and office buildings, and street lighting. At the same time, lighting load may represent a considerable portion (10 to 30%) of the overall electronic load. This suggests that there is potential for utilizing LED drivers with PFC front–end converters for harmonic compensation in single phase AC distribution systems. The vision for the future is that smart LED drivers can be equipped with harmonic compensation features in addition to dimming and color changing, all of which can be controlled through a wireless network of sensors via IoT. Therefore, the aim of Objective 3 is to develop a demonstration smart LED driver prototype with support from OmniSolu Ltd. (a Vancouver-based LED lighting company) that will incorporate these advanced features. This objective includes detailed simulation, controller loop design, design and construction of model-based hardware circuits, and demonstrations with the industrial partner.

Chapter 2: Feasibility of Smart Loads in AC/DC Microgrid System for Harmonic Compensation

In this chapter, a smart meter-based harmonic compensation method is proposed to improve the power quality of building distribution systems with hybrid AC/DC microgrids, energy storage, and/or large electronically–interfaced uninterruptable power supplies. This method is demonstrated in the distribution system of a typical building on the UBC campus. The chosen building is equipped with integrated energy storage as well as an AC/DC microgrid system for research and operational needs. The methodology is verified using the collected smart meter data and representative loads in the building. It is also assumed that the inverters in the installed AC/DC microgrid can be configured and controlled to absorb/inject additional harmonics into the system. The conducted studies are completed using detailed models of the overall system implemented in Matlab/Simulink. No additional passive/active filters or voltage/current measurements are required. The existing smart meter is used to obtain information about all significant harmonics.

2.1 Case Study Based on Distribution in the Kaiser Building aton UBC Campus

A simplified power system of the Kaiser building considering the AC/DC microgrid is depicted in Figure 2.1. The single line diagram represents a hybrid AC/DC commercial building, which is a typical three–phase four–wire system in North America. The building power system has four isolated 208 V buses as well as a DC sub–system (battery bank) for peak shaving purposes [39]. For a more detailed electrical system diagram, the reader is referred to Appendix A.

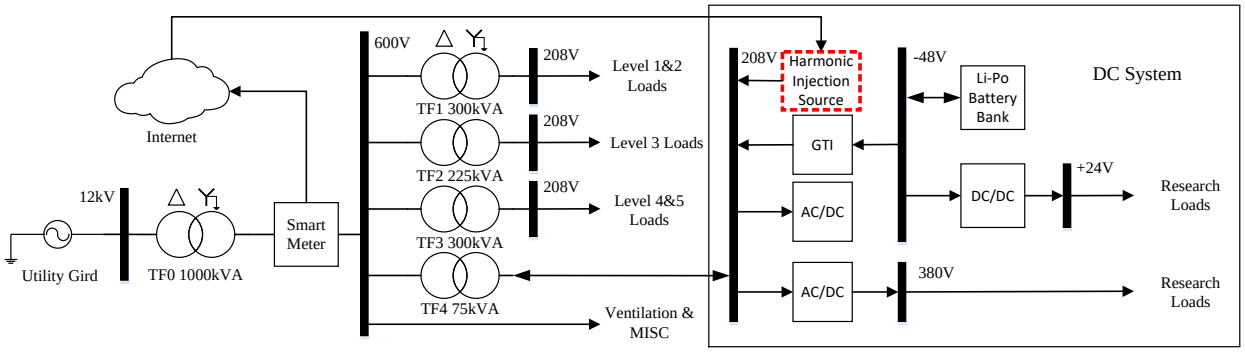

Figure 2.1 A simplified single–line diagram of electrical system in Kaiser building at UBC.

2.1.1 Survey of system configuration

A survey of loads in the building has been conducted. The data is sourced from UBC Kaiser building electrical system diagrams and service manuals. Table 2.1 illustrates a summary of load types and the estimated total loading power at peak time.

It is worth mentioning that many of the surveyed loads are likely to have line–commutated rectifiers as their front–ends. Additionally, the Kaiser building has a 1MW main distribution transformer at its power entry. As a result, all loads may add up to only 25% transformer capacity.

Load Type	Estimated Total Loading Power at Peak Time
Lighting	91.396kW
Office Appliance (e.g. PC, Monitor, Laptop…)	130.7kW

Table 2.1 Summary of electrical loads in Kaiser building.

2.1.2 Model of system and loads

The considered building, after the main distribution transformer, has four sub–distribution transformers, as shown in Figure 2.1. All of the transformers have a delta–wye configuration, which prevents 3rd current harmonic flow between the different buses. For the purpose of simulation, the delta–wye transformer models with saturation have been used. The parameters of the transformers are obtained from original datasheets which can be found in Appendix A. It is noted that for the purpose of simulation studies, the impedance of cables is neglected since it is negligible compared to the transformer series impedances. In order to implement various loads in the considered building, the loads can be categorized into several classes (models) [19] based on their assumed operation and internal structure. For the Kaiser building, the assumed load types are depicted in Figure 2.2. For the purpose of analysis in this chapter, only steady state operation is considered.

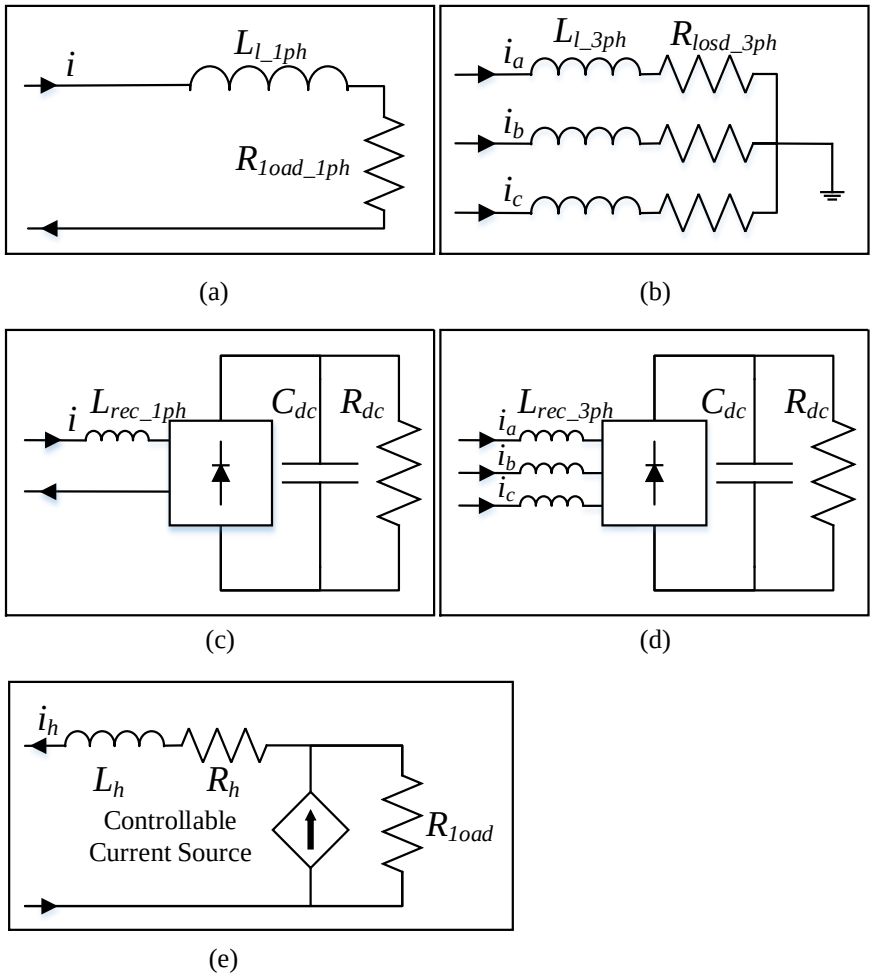

Figure 2.2 Models of different types of loads: (a) and (b) single and three phase inductive loads; (c) and (d) single and three phase rectifier loads; and (e) single phase harmonics injection loads.

2.1.2.1 Single and three–phase inductive loads

The ventilation system in Kasier building consumes a significant amount of power throughout the day. However, most motors in the building are three phase induction motors without VFDs, and therefore they do not produce harmonics. These types of motor loads are represented as inductive loads depicted in Figure 2.2 (b), which only affect the system's power factor.

2.1.2.2 Single and three–phase rectifier loads

Most of the single–phase loads in the considered system contain full bridge rectifiers, and are of the type shown in Figure 2.2 (c). Three–phase VFD motor loads can be represented using the load type shown in Figure 2.2 (d). Typical examples of full bridge rectifiers include SMPSs which exist in most PCs, laptops, monitors, lighting, and variable frequency drives. For the purpose of this chapter, a combined (aggregate) load is introduced for simulating computers and lighting loads. This combined load is represented by a linear component [as depicted in Figure 2.2 (a)] and a nonlinear component [as depicted in Figure 2.2 (e)]. The linear component is used to adjust the power consumption of the load. The nonlinear component is designed to produce the desired harmonics (e.g. 5^{th}, 7^{th} …), and can be used to emulate the injections of the harmonics according to the measurements obtained from the smart meter.

2.1.2.3 Single–phase smart loads with harmonic injection

A full–bridge grid tie inverter (GTI) is considered as the harmonic injection source. This GTI can be powered by the 380V DC bus, which is available as part of the AC/DC system in the building. For the purpose of this chapter, a generic inverter model is used. Each phase of the inverter is simplified and modeled as an ideal current source with a line filter as shown in Figure 2.2 (e). The inverter is assumed to operate in current controlled mode [20], and it is placed at the 600V bus at the PCC. Additional current sources of the type shown in Figure 2.2 (e) may be added to the PCC in order to emulate the harmonics produced by other miscellaneous loads.

2.2 Proposed Harmonic Compensation Methodology

In a typical commercial/academic building, there are many nonlinear electrical loads that inject unwanted lower–order harmonics into the system, wherein the typical harmonics may include 3rd, 5th, 7th, etc. [20]. At the PCC, the n^{th} current harmonic can be characterized as

$$i_n(t) = A_n \sin(\omega_n t + \varphi_n), \tag{2.1}$$

where ω_n, A_n and φ_n are the n^{th} harmonic frequency, magnitude, and the associated phase, respectively. Intuitively, the n^{th} harmonic current at the PCC can be directly canceled by injecting a compensating harmonic current $i_c(t)$, which possesses identical magnitude but an opposite phase

$$i_c(t) = -i_n(t) = A_c \sin(\omega_n t + \varphi_c), \tag{2.2}$$

where

$$\varphi_C = \varphi_n + \pi . \tag{2.3}$$

Therefore, the information of A_n and φ_n are required. Ideally, this can be done by setting up a fast feedback loop from the smart meter installed at the PCC, which continuously tracks the current waveforms and sends back the required information at a (close to) real-time sampling speed (similar to the working scheme of most active harmonic compensators [20]). However, this is a challenging endeavor as even modern smart meters have the following properties: 1) they may not be able to compute the harmonic phase angles φ_i due to design limitations; and 2) they have a relatively slow update rate, e.g., one sample per second (not including network communication delays, which may add up to hundreds of milliseconds or longer).

To overcome these limitations, this chapter first proposes a feasible solution to identify the phase angles of harmonics. It is noted that in a typical electrical system, the behavior of

harmonics can vary due to the change in loads. On the one hand, in a 24–hour period, some loads, such as CFLs, may constantly be on and consume constant power. On the other hand, some load consumptions such as PCs and monitors, may differ greatly depending on usage. Therefore, (2.1) is decoupled into two parts, assuming fixed and varying components as

$$i_n(t) = A_{nf}\sin(\omega_n t + \varphi_{nf}) + A_{nv}\sin(\omega_n t + \varphi_{nv}) \quad \textbf{(2.4)}$$

where A_{nf} and φ_{nf} denote the magnitude and phase angle of the n^{th} fixed harmonics; A_{nv} and φ_{nv} are the magnitude and phase angle of the n^{th} varying harmonics, respectively.

When the system is operating in a quasi–steady state condition, A_{nv} is assumed to be zero. Therefore, knowing A_{nf} is sufficient for compensating the n^{th} harmonic, and the key is to find the angle φ_{nf} (without receiving its value from the smart meter).

2.2.1 Harmonic angles computation algorithm

For the purpose of this chapter, a trial-and-error iterative methodology is proposed, and its flow chart is depicted in Figure 2.3. This approach assumes that the smart meter feeds back magnitude information A_{nf}, which is then passed as A_c to the compensating current source $i_c(t)$ as formulated in (2.2). The initial value of φ_c is set to $\varphi_c = \varphi_{nf} + \pi$. Next, in a real-time or fast simulation environment, the tested system modeled using the component models discussed in Section 2.2, and the compensating current source $i_c(t)$ as formulated in (2.2), are jointed and simulated together to obtain the new harmonic value A_{nf}. If the new A_{nf} is small, this indicates that the injected $i_c(t)$ is compensating system harmonics, i.e. φ_c is close to being

determined. A tolerance A_{tol} is specified by the user depending on the desired compensation performance.

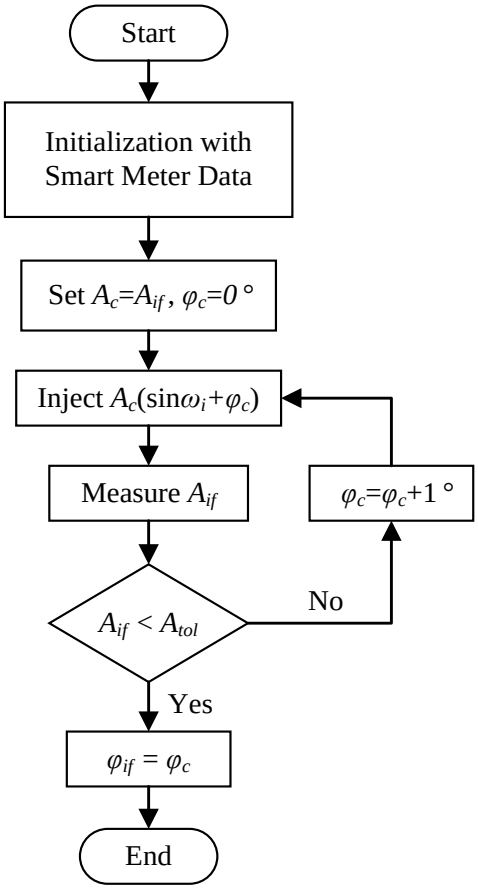

Figure 2.3 Flow chart depicting algorithm for computing φ_{if} in a static condition.

In the Kaiser building, the lights, computer servers, and ventilation system are rarely turned off. Therefore, at night the system is very close to a steady state operating condition, i.e., A_{nv} is close to zero. Therefore, the harmonic current can be approximated as

$$i_n(t) \approx A_{nf} \sin(\omega_n t + \varphi_{nf}). \quad \textbf{(2.5)}$$

It is assumed that the smart meter provides A_{if} as its measurement. The angle φ_C needs to be estimated, and therefore the fixed component of i^{th} harmonic can be completely compensated at night. If compensation continues during the day, the new i^{th} harmonic will be as the following

$$i_i^{new}(t) \approx A_{iv} \sin(\omega_i t + \varphi_{iv}), \quad \textbf{(2.6)}$$

$$\varphi_{if} \approx \begin{cases} \varphi_{iv}, & then \quad i_i^{new}(t) < i, \\ \varphi_{iv} + \pi, & then \quad i_i^{new}(t) > i_{i.} \end{cases} \quad \textbf{(2.7)}$$

In general, the proposed method can lower the selected current harmonics on a daily basis, in which it is essential that the steady state period is determined first based on smart meter data. It is also noted that the applied compensation may increase harmonics during the day due to the possibility that some harmonics in the system may naturally cancel each other (2.7). If the harmonics from some loads in the system naturally have opposing phases and cancel (or partly cancel), the additional compensation may no longer be required, or its amount can be reduced. At the same time, the compensation does not have to be implemented at the PCC, and the compensator can be physical installed at a remote location in the system.

2.3 Computer Studies

Power quality historical data has been captured from the smart meter in the Kaiser building, and the collected data set has been analyzed and utilized in the following computer studies.

2.3.1 Historical harmonics data analysis

A typical 24-hour period of building power consumption and dominant harmonics has been recorded and is shown in Figure 2.4. In the recorded 24-hour period, only the computer server, some lighting, and ventilation systems are assumed to remain fully functional. The captured data indicate the following harmonic signatures:

- 3^{rd} harmonic is not balanced and does not change significantly with respect to system load changes
- 5^{th} and 7^{th} harmonics change with respect to the system's loading conditions

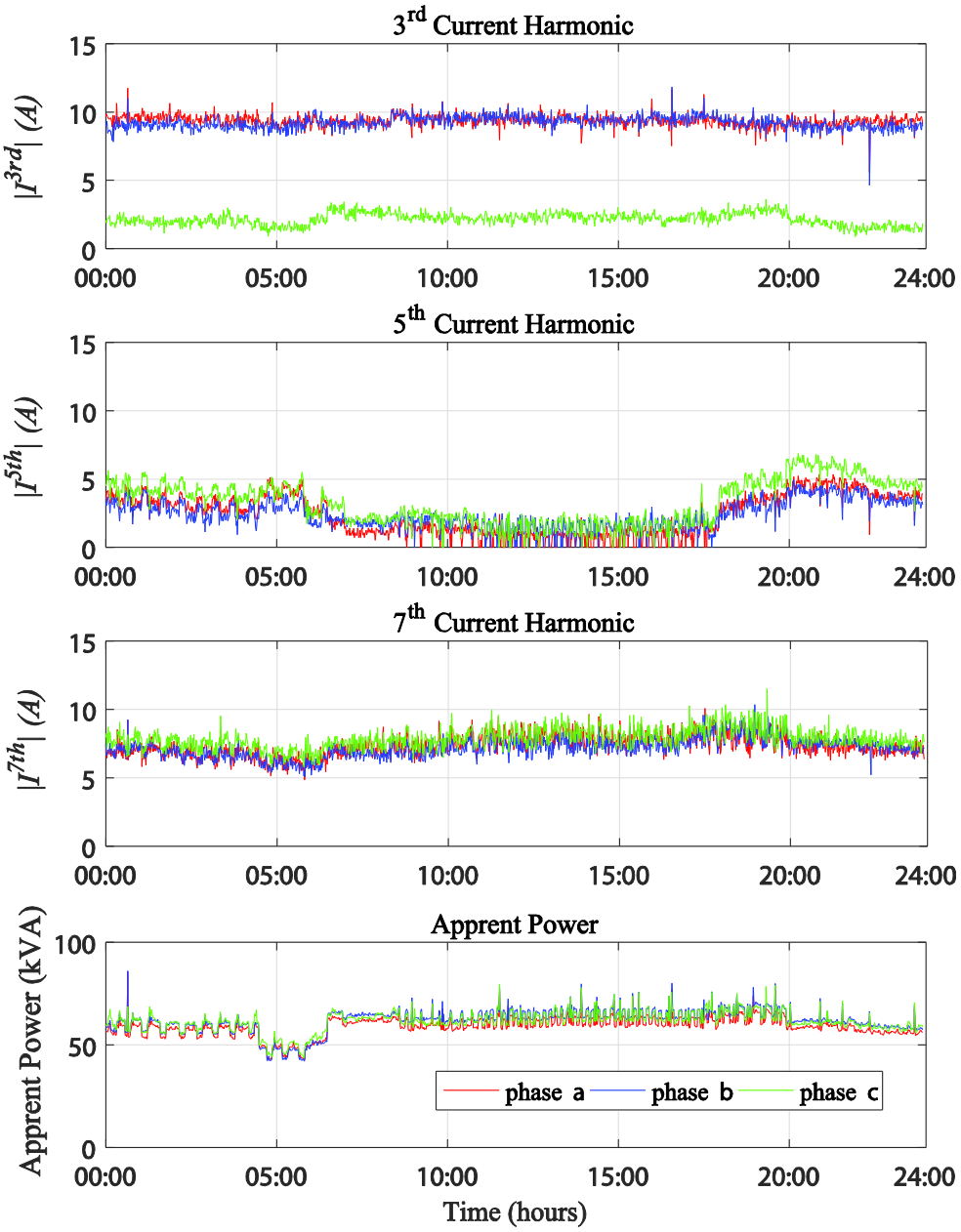

Figure 2.4 Real–time smart meter data: power consumption and selected harmonics measured at the sample rate of once per second over a 24–hour period.

Based on the above observations, the following conclusions can be summarized:

- Transformer saturation may contribute to the unbalanced 3rd harmonics in the system [21][21]
- As the lighting system of the building is operational for 24 hours continuously, and the magnitude of the 7th harmonic does not fluctuate significantly with respect to time, the lighting system may be the dominant source of the 7th harmonic currents.
- 5th harmonic currents remain lower during the day and higher at night. This may be attributed to some 5th harmonic currents that are out of phase and which cancel each other more during the day. The system's apparent power is relatively balanced across the three phases. To model the system, the loads' distribution scheme and their types must be known. A load survey (Chapter 2.1.1) has been conducted with the following list summary:
    - The lighting system is highly consistent in the Kaiser building. Identical florescent lights have been used for the entire building. Also, the THD information is known from the respective manufacturing documents.
    - The ventilation system mostly uses three–phase induction motors (without the VFDs). Ideally, this system should not emit harmonics.
    - Except for the ventilation system, all other loads are connected to the 208V buses, which have no direct connections to the building main service transformer. This prevents any 3rd harmonic currents to flow back from the 208V bus to the 600V bus and PCC.

2.3.2 Compensation strategy

The detailed model of the system in Figure 2.1 has been implemented in Matlab/Simulink [22] using PLECS library components [23]. The combinations of different loads as discussed previously in Section 2.1 are used in the simulation. The loading scheme is chosen to be close to the measured load in the Kaiser building. During the day, only the 7^{th} harmonic is chosen to be compensated. At night, both 5^{th} and 7^{th} harmonics are compensated simultaneously, due to the following reasons:

- The system uses delta–wye configured transformers and the 3^{rd} harmonic currents cannot propagate through delta windings of transformers. Therefore, 3^{rd} harmonic currents are not required to be compensated.
- During the day, the 5^{th} harmonic currents have lower THD which may be attributed to partial self–compensation of various loads that produce 5^{th} harmonics out of phase. Thus, the 5^{th} harmonic currents are not required to be compensated during the day. However, since there are several loads that do not operate at night, the system does not have self–cancelation and the 5^{th} harmonic currents should be compensated.
- The 7^{th} harmonic currents are present in the system during the day and at night. Therefore, the compensation of 7^{th} harmonic currents is required for 24 hours.

2.3.3 Simulation results

The harmonic content of different phases is summarized in Table 2.2 (for 6:00) and Table 2.3 (for 19:00), respectively. At 6:00, the system is considered in a steady state condition. Therefore, the magnitude of the 7^{th} harmonic current at 6:00 is determined as the reference

magnitude of the 7^{th} compensating harmonic current, which is used to compensate the 7^{th} harmonic at 19:00.

In the considered simulation, the 5^{th} and 7^{th} harmonics are selected to be compensated for night–time, and only the 7^{th} harmonic for the day–time. The reference fixed components are determined when the system is operating in static condition at 06:00. The variable components of harmonics are also considered by modeling them as current sources whose magnitudes are estimated based on the simulated loads. The 7^{th} harmonic currents at 19.00 are compensated using the reference compensating values determined at 06:00.

The effectiveness of the proposed harmonic compensation method in compensating the 7^{th} harmonic during the day is illustrated in Figure 2.5. As observed, the magnitudes of uncompensated harmonics obtained from simulating the power system model match the measured smart meter data at 19:00. Also, Figure 2.5 illustrates the compensated and uncompensated magnitudes for the 7^{th} current harmonic, which verify the proposed method in decreasing the selected harmonic. Moreover, the figure clearly illustrates a significant reduction in the 7^{th} harmonic after applying the compensation. The capability of this proposed method in compensating the 5^{th} and 7^{th} harmonic at night is also verified and shown in Figure 2.6. As observed here, the proposed method is able to compensate the harmonic currents almost ideally when the system is operating in a static condition. It is worth mentioning that the proposed method can be applied to compensate for any desired harmonics.

Phase	Phase *a*	Phase *b*	Phase *c*
3rd Harmonics	8.614A	9.344A	2.310A
5th Harmonics	2.920A	2.628A	2.772A
7th Harmonics	6.570A	6.278A	6.776A

Table 2.2 Smart meter data for harmonic current magnitudes at 06:00.

Phase	Phase *a*	Phase *b*	Phase *c*
3rd Harmonics	8.883A	9.200A	2.376A
5th Harmonics	3.591A	2.600A	4.554A
7th Harmonics	8.505A	8.400A	9.108A

Table 2.3 Smart meter data for harmonic current magnitudes at 19:00.

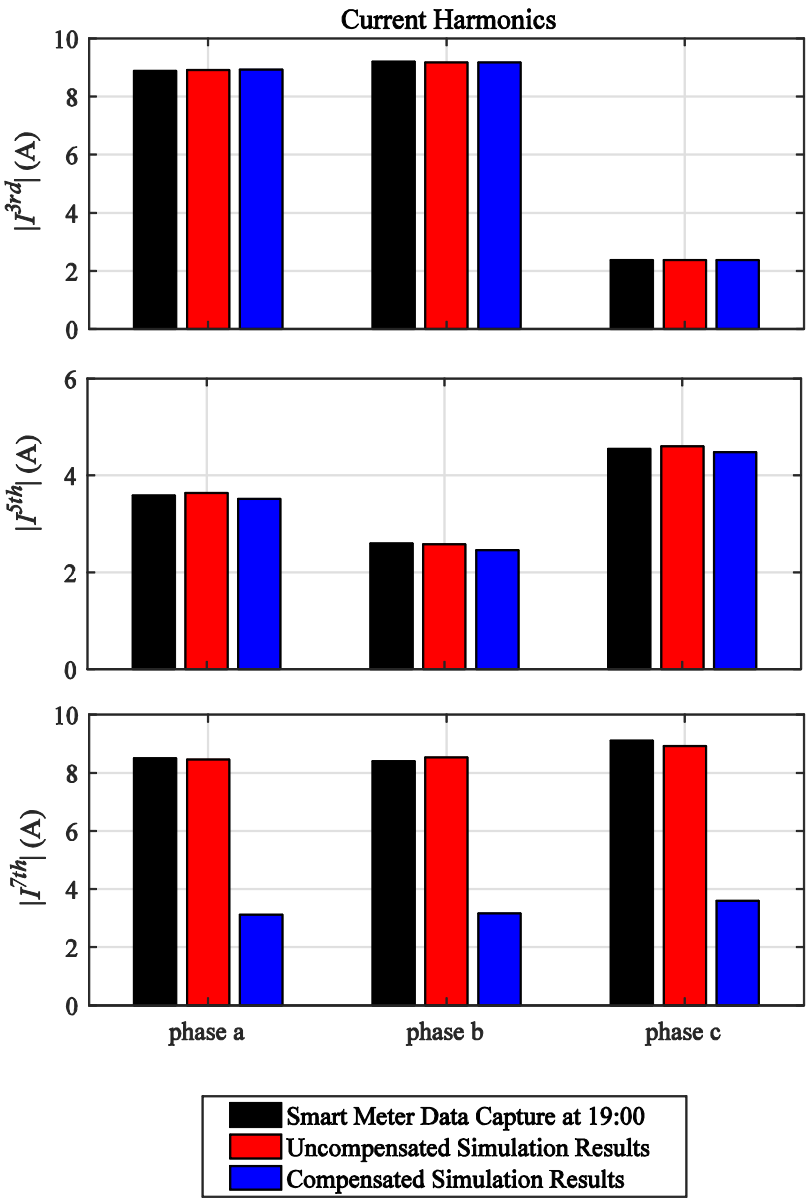

Figure 2.5 Harmonic current magnitude comparisons when the compensation method is applied to mitigate the 7th harmonic currents during the day.

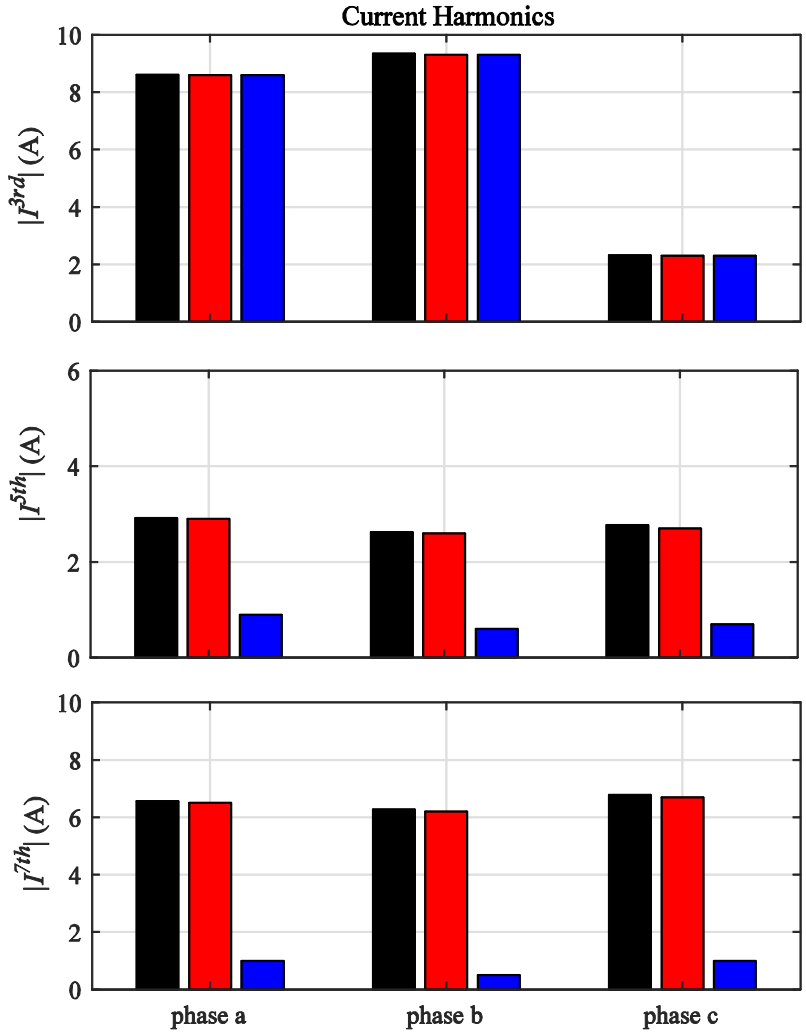

Figure 2.6 Harmonic current magnitude comparisons when the compensation method is applied to mitigate the 5th and 7th harmonic currents during the night.

Chapter 3: Demonstration of a Commercial Device as a Smart Load for Harmonic Compensation

Harmonics in distribution power systems represent a power quality issue and may cause malfunction or even damage to devices [24]. Harmonics may be generated by nonlinear loads such as SMPS, VFDs, line–commutated rectifiers, CFL, and so on [25]–[27]. Traditionally, harmonics are compensated at the PCC using dedicated passive or AHF [20] [28], which may not be economically advantageous for many applications.

The emergence of smart meters and loads with PFC has presented an opportunity to use the PFC stage of existing loads as the AHF [27]. In many loads, the PFC may be installed at the input stage of the converter to meet the required THD regulations such as IEC61000 [29]. Meanwhile, modern smart meters are usually installed at PCC to monitor power flow and power quality. Figure 3.1 depicts a distribution system where nonlinear loads are assumed to generate significant harmonics. In this chapter, it is assumed that the distorted currents can be accurately measured by the smart meter installed at the PCC. The measured amplitude and the phase of each harmonic are then passed via the communication network to the smart electronic loads with PFC that are capable of compensating the desired harmonics. It is envisioned that this method can effectively improve the power quality of future "intelligent" distribution power systems, since PFCs have become mandatory for many devices that are widely used in distribution networks [28].

This chapter extends the idea of [27] by investigating and demonstrating the feasibility of using a single phase PFC-based harmonic compensation in distribution networks, considering the topology and hardware constraints of a generic PFC stage. A detailed simulation of the test

system depicted in Figure 3.1 has been developed in MATLAB/Simulink using PLECS. Experimental results from a commercial rectifier with PFC (based on the Alpha Technologies, Ltd product) are also included. The existing digital controller of the PFC–based rectifier is re–programmed to include the injection of compensating harmonics and validates the proposed approach.

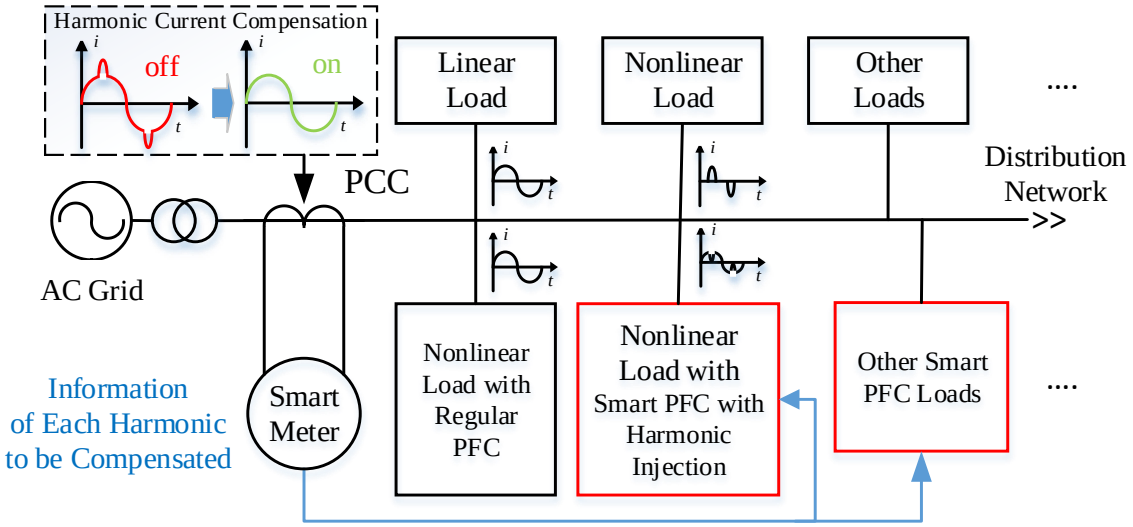

Figure 3.1 AC distribution system with nonlinear loads and smart electronic loads with PFC for harmonic compensation. Smart meter is used for harmonic measurements.

3.1 Loads with Power Factor Correction Stages

In practice, most electronics are DC powered while the existing power grid is AC. Therefore, internal rectification is necessary. However, simple rectification with passive devices such as a diode bridge would create large harmonics and low power factor, thus the PFC stage is indeed required. The PFC is a power electronic front–end for rectifying AC to DC power [44], while maintaining the required power quality, including power factor and harmonics. After rectification, the DC power can be further converted to the required output. Depending on the

topology and application, the PFC can either be unidirectional or bidirectional. Most electronic loads such as SMPS, lighting ballasts, and motor controllers would typically use unidirectional PFC as their front–end, due to its simplicity and lower cost. At the same time, for the interconnection of distributed generation (DG) and energy storage systems (e.g. battery charging/discharging), uninterruptable power supplies (UPS), etc., there may be a need to use a bidirectional PFC to satisfy the application requirement for bidirectional power flow. Furthermore, in the specific applications of the PFC stage, a galvanic isolation can be achieved using a pulse transformer.

3.1.1 Conventional PFC topologies

There are many converter topologies that can be adapted to work as front stage PFC. A brief summary of bridged and bridgeless PFC stages is provided below, as these topologies are commonly used in single phase electronic loads.

For single phase applications, typical PFC would consist of a full diode bridge followed by a DC/DC converter that feeds the internal DC load. Figure 3.2 illustrates a generic bridged PFC with a boost type current converter. This topology is simple and usually low cost, but the tradeoff here is the losses on the diode bridge. For a low power application, usually less than 500W, the losses on the diode are usually acceptable. However, for high power applications, the diode bridge losses may be significant and unacceptable.

To overcome losses on the diode bridge, a bridgeless topology can be considered, as shown in Figure 3.2. This topology does not require a full bridge (uses only two diodes) and has additional switches, thus it is more complicated to control and more expensive than the bridged PFC.

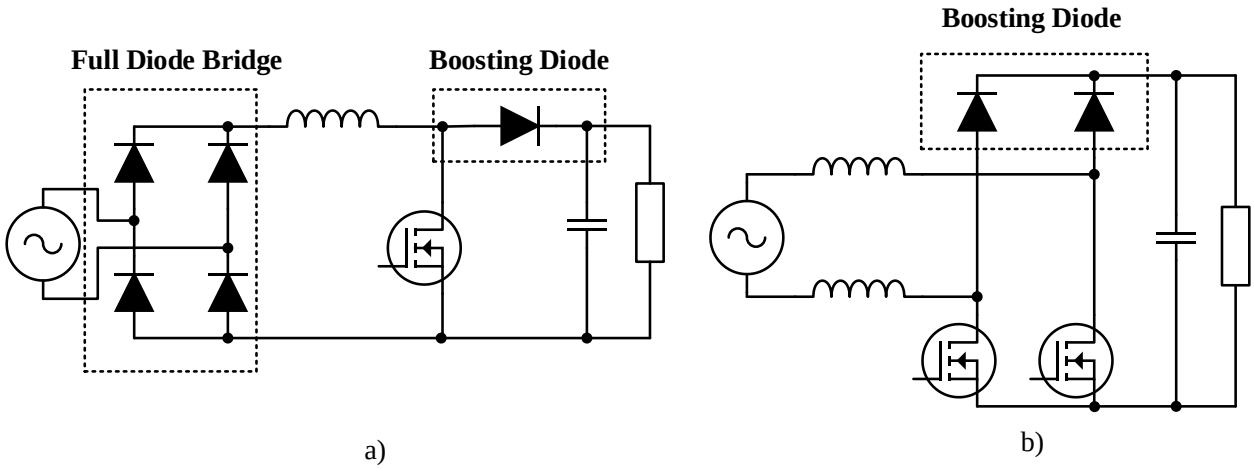

Figure 3.2 Example of generic PFC: (a) bridged type PFC; and (b) bridgeless type PFC.

3.1.2 Conventional PFC control loop

Conventional PFC requires advanced control to operate. Two variables, input current and output voltage, must be controlled to maintain normal operation. A typical cascade controller, such as one shown in Figure 3.3, is often used. The inner loop is for controlling input current denoted by i_{PFC}, and the outer loop is for controlling DC voltage denoted by v_{dc}.

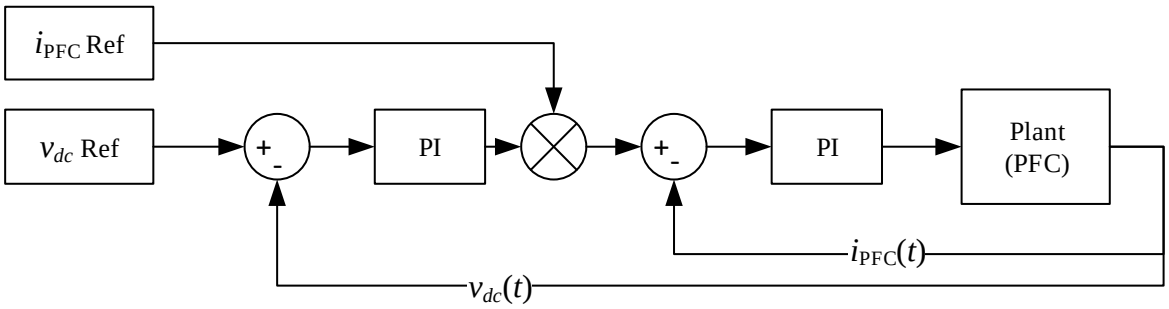

Figure 3.3 Generic cascaded controller for PFC.

3.2 Topology Constraints of Conventional PFC for Harmonic Compensation

For analyzing operating conditions, a generic single–phase PFC stage, as depicted in Figure 3.4, is considered. This PFC consists of a diode bridge and a boost converter. By proper control of the boost converter, the input AC current is modulated to be a sinewave in phase with the input voltage, thus achieving the power factor correction [30]–[32]. Assuming the converter bandwidth is sufficiently high (up to several hundred Hertz), the modulation can be appropriately modified to inject/absorb additional low–order harmonics (i.e. 3rd, 5th and 7th) in the AC grid. Without loss of generality, the system frequency is assumed to be ω_e = 377rad/s (60Hz), and only the dominant AC harmonics (i.e. 3rd, 5th, and 7th) are considered. In addition, it is assumed that the input voltage is purely sinusoidal.

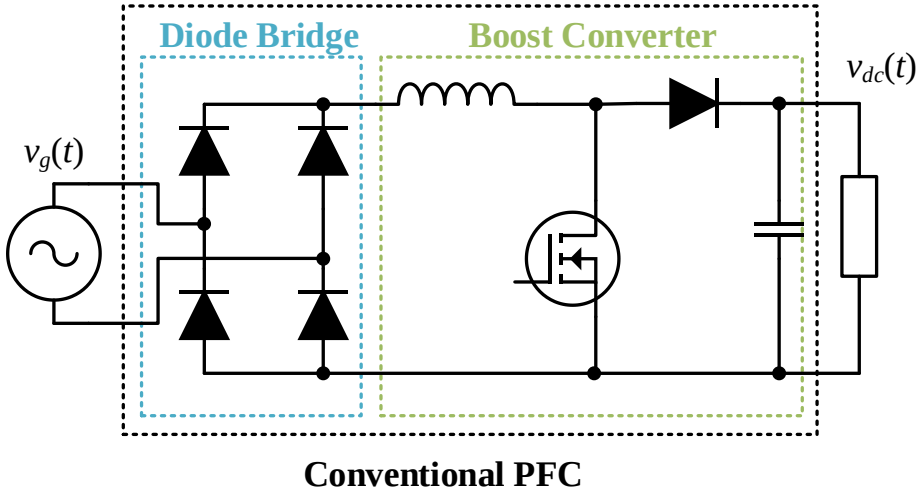

Figure 3.4 A generic topology of a conventional PFC.

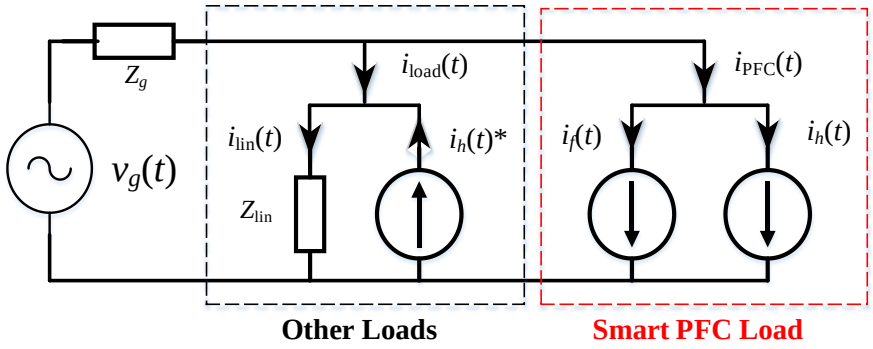

Figure 3.5 Simplified circuit diagram of the proposed PFC-based harmonic compensation.

For the purpose of this chapter, and for consistency with [7], the distribution system in Figure 3.1 is simplified to the diagram shown in Figure 3.7. Therein, the AC grid is represented by its Thevenin equivalent source $v_g(t)$ and impedance Z_g. The conventional nonlinear loads are modeled as a linear impedance Z_{lin} drawing current $i_{\text{lin}}(t)$ and a harmonic current source denoted by $i_h(t)$*, with the total load current denoted as $i_{\text{load}}(t)$. It is the current $i_h(t)$* that needs to be compensated.

To consider the smart PFC load with harmonic compensation features, the PFC input current $i_{\text{PFC}}(t)$ is assumed to be composed of its fundamental and harmonic as

$$i_{\text{PFC}}(t) = i_f(t) + i_h(t) = I_f \sin(\omega_e t) + i_h(t). \quad \textbf{(3.1)}$$

Here, $i_f(t)$ represents the PFC load nominal current which only contains the fundamental component, and where $i_h(t)$ is the additional current that compensates the grid harmonics $i_h(t)$*. For a harmonic current that contains 3rd, 5th, 7th, etc., we can express this as

$$i_h(t) = \sum_{n \in N} I_{h,n} \sin(n\omega_e t + \varphi_{h,n}) \quad \textbf{(3.2)}$$

where $n \in N = \{3,5,7,\ldots\}$ denotes the harmonic order, $I_{h,n}$ is the harmonic magnitude, and $\varphi_{h,n}$ is the harmonic phase.

Ideally, for full compensation, the PFC should inject equal magnitude harmonic currents for each harmonic, but with a 180–degree phase shift, such that the harmonics generated by the nonlinear loads are canceled, i.e. $i_h(t) = i_h(t)^*$. However, this may not always be possible due to the diode bridge and boost converter of the PFC that prevents bidirectional power flow. In other words, the conventional PFC is not capable of conducting the negative current during the positive voltage cycle, or positive current during the negative voltage cycle. Therefore, the following constraints apply:

$$\begin{cases} i_{\mathrm{PFC}}(t) \geq 0 & t \in [0, \pi/\omega_e), \\ i_{\mathrm{PFC}}(t) \leq 0 & t \in (\pi/\omega_e, 2\pi/\omega_e]. \end{cases} \quad \textbf{(3.3)}$$

If the constraint (3.3) is violated by the PFC controller command, the current $i_{\mathrm{PFC}}(t)$ will be clamped to zero due to the operation of diodes shown in Figure 3.4. This will cause current discontinuity [operation in discontinuous conduction mode (DCM)] and introduce additional unwanted harmonic distortions.

To avoid current discontinuity $i_{\mathrm{PFC}}(t)$, combining (3.1) and (3.2) and assuming only harmonic order *n*, the harmonic phase angle $\varphi_{h,n}$ and magnitude $I_{h,n}$ should satisfy the following constraint within the positive voltage cycle

$$\frac{I_{h,\,n}}{I_f} > -\frac{\sin(\omega_e t)}{\sin(n\omega_e t + \varphi_{h,\,n})}. \quad \textbf{(3.4)}$$

Equation (3.4) gives the harmonic compensation capability of the PFC converter while operating in continuous conduction mode (CCM) and avoiding the current discontinuity, i.e. DCM. To

better visualize this limitation, Figure 3.8 depicts the relative harmonic magnitude (RHM) defined as

$$\text{RHM} = I_{h,n} / I_f \,. \tag{3.5}$$

In Figure 3.6, the RHM is plotted as a function of phase angle φ_h for the considered 3rd, 5th, and 7th harmonics, respectively. Here, the PFC current (3.1) will be at the boundary between the CCM and DCM. As can be seen in Figure 3.6, when φ_h is in the range from 20 ° to 170 °, the resulted RHM becomes negligible, which makes the PFC–based harmonic compensation highly ineffective in this range. However, in the regions close to $\varphi_h = 0$ or $\varphi_h = 180^\circ$, the compensation capability becomes significant. The maximum harmonic magnitudes for 3rd, 5th, and 7th harmonics have been computed assuming a boundary at the CCM/DCM and are summarized in Table 3.1. It is also worth mentioning that Figure 3.6 only illustrates harmonic angle from 0 to 180 degree. A mirrored image is expected for –180 to 0 degree due to symmetry.

To illustrate the operation before discontinuity in CCM and after discontinuity in DCM, Figure 3.7 shows an ideal case based on the 3rd harmonic injection, which assumes $\varphi_h = 180^\circ$. As seen in Figure 3.7, when RHM = 0.3, the injected 3rd harmonic does not introduce discontinuity in the line current. However, when RHM is increased to 1, the discontinuity occurs in the line current due to the constraint and operation of diodes. This current discontinuity can be eliminated if a bidirectional converter topology is used, which gives the ideal injection waveform as shown by the green line in the corresponding figure.

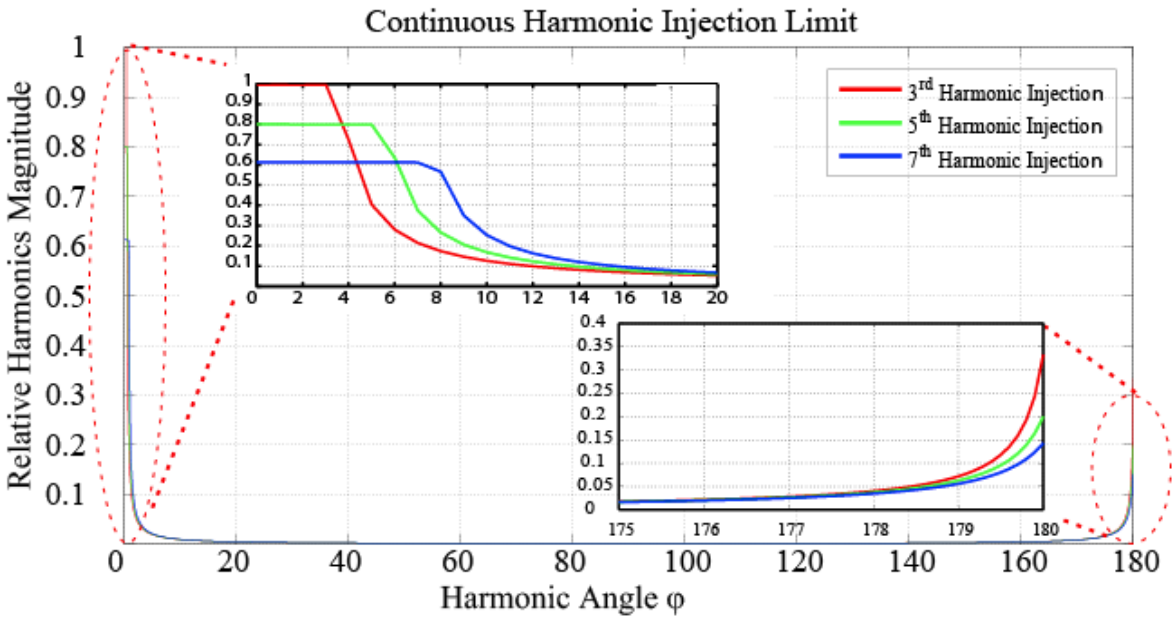

Figure 3.6 Maximum relative harmonic magnitude that can be injected without distortions in CCM as a function of harmonic angle.

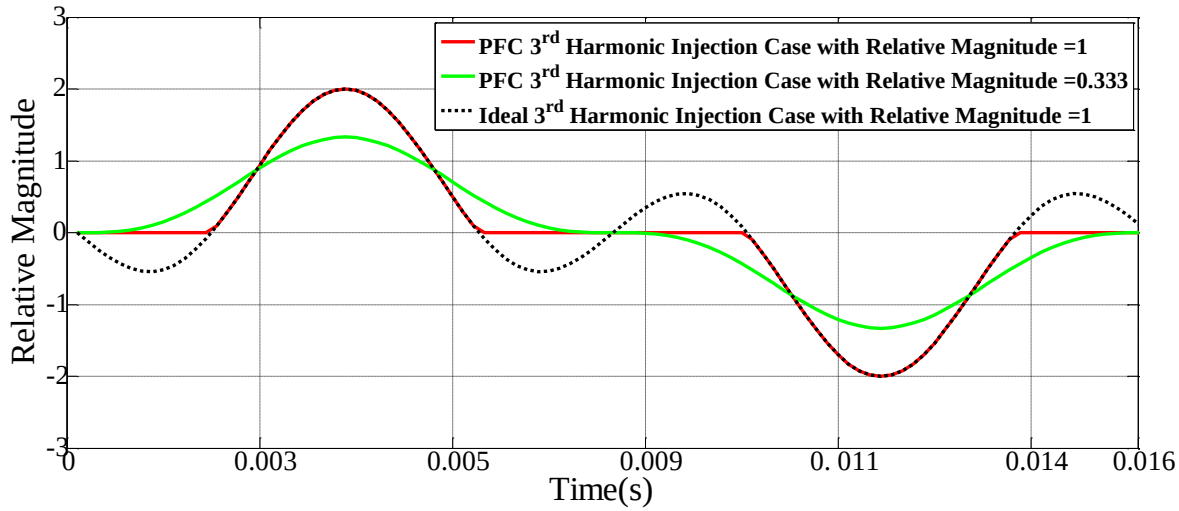

Figure 3.7 Example of waveform showing 3rd harmonic comparison before (in CCM) and after the discontinuity constraint (in DCM).

Harmonic Order	$\omega_{h,3}=3\omega_e$		$\omega_{h,5}=5\omega_e$		$\omega_{h,7}=7\omega_e$	
Harmonic Angle $\varphi_{h,n}$	0	π	0	π	0	π
Relative Harmonic Magnitude	1	0.333	0.8	0.2	0.613	0.143

Table 3.1 Maximum capability of PFC–based harmonic compensation for harmonics of angles 0 and 180 degrees.

3.3 Extending Range of Harmonic Compensation in DCM

The occurrence of discontinuity in PFC line current is undesirable since this injects additional unwanted harmonics into the grid. Specifically in DCM, the PFC line current $i_{\mathrm{PFC}}(t)$ can be formulated as

$$i_{\mathrm{PFC}}(t)=\begin{cases} 0, & t\in[0,\pi/\omega_e) \ \cap \ i_f(t)+i_h(t)<0. \\ 0, & t\in(\pi/\omega_e,2\pi/\omega_e] \ \cap \ i_f(t)+i_h(t)>0. \\ i_f(t)+i_h(t), & \text{otherwise.} \end{cases} \quad \textbf{(3.6)}$$

where it is recalled that $i_f(t)$ and $i_h(t)$ are given by (1) and (2), respectively.

It should be noted that the requirement (3.4) of CCM imposes a strict limitation on PFC–based harmonic compensation. However, a small discontinuity in $i_{\mathrm{PFC}}(t)$ will only result in small THD, which may be acceptable overall. Therefore, to increase the harmonic compensation capability (i.e., RHM at different harmonic angles as shown in Figure 3.8), it is possible to allow for a small increase in the level of THD of the input current (within a threshold that can be set), while still compensating for the desired harmonics in DCM. Assuming that a full compensation of a particular harmonic is achieved by the PFC control, it is possible to quantify the contribution

of unwanted additional harmonics resulting only from the discontinuity. With this in mind, a harmonic distortion coefficient (HDC) is introduced here and defined as

$$\mathrm{HDC}\% = \frac{\sqrt{\sum_{n=2}^{\infty} |I_n|^2 - |I_x|^2}}{|I_1|} \times 100\%, \tag{3.7}$$

where I_n is the magnitude of n^{th} current harmonic, and I_x is the injected harmonic current magnitude. The definition (3.7) considers only the distortion of line current due to the DCM operation of the PFC stage, and assumes one harmonic injection at a time.

Therefore, by assuming a proper threshold for the HDC, it becomes possible to compensate the harmonics in a wider range. To illustrate this, the RMH is formulated as a parametric function with inputs of the harmonic angle and the HDC threshold, i.e.

$$\mathrm{RHM} = f(\mathrm{HDC}\%, \varphi_{h,n}). \tag{3.8}$$

Combining (5) and (8) then yields

$$I_{h,n} = I_f \cdot f(\mathrm{HDC}\%, \varphi_{h,n}), \tag{3.9}$$

which indicates the PFC–based harmonic compensation capability for the n^{th} harmonic. It is also noted that the parametric function $f(\cdot)$ in (8) is established based on the actual PFC topology and current limit.

To evaluate the harmonic compensation capability of the PFC, for the considered system with parameters summarized in Appendix B, the contribution of harmonic currents resulting from discontinuity are represented as the HDC for 3rd, 5th and 7th harmonic injection in steady state operations, as depicted in Figure 3.8, which is also an interpretation of parametric function (3.7). As can be seen in Figure 3.8, the computed HDC has a non–linear relationship with the phase angle and magnitude of the desired harmonic current injection. It can also be observed that

HDC increases with increasing magnitude of harmonic injection due to the line current discontinuity. In particular, Figure 3.8 indicates a roughly 10% HDC threshold for practical compensation of the unwanted harmonics, which validates the effectiveness of the proposed method to compensate any harmonic of interest.

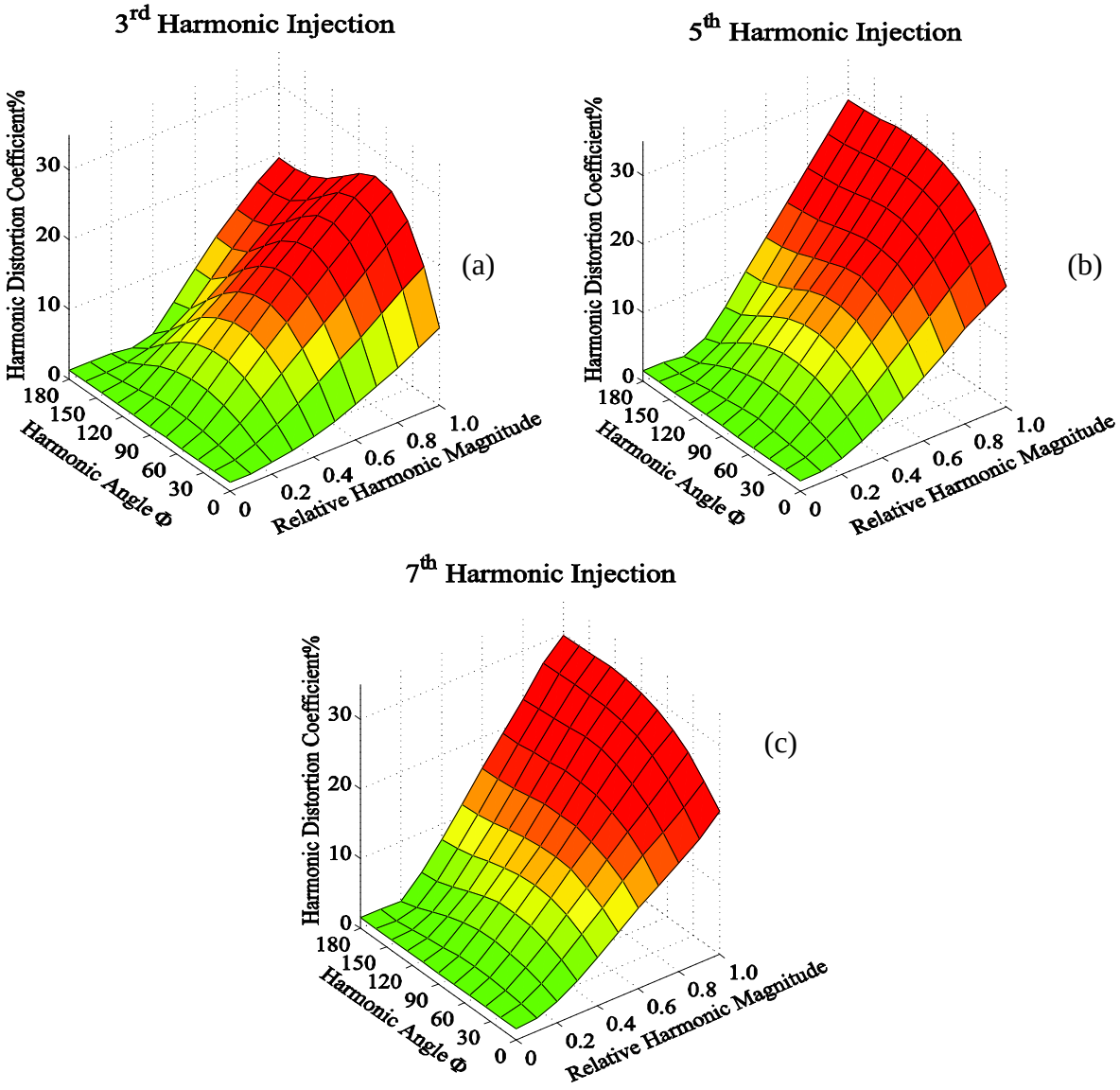

Figure 3.8 Computed HDC results in terms of magnitude and phase angle of injected harmonic for: (a) 3rd, (b) 5th, and (c) 7th harmonics.

3.4 Proposed Controller

To design a controller for such a harmonic compensation method assuming a practical/typical PFC stage, a commercial bridgeless PFC prototype (by Alpha Technology Ltd.) as shown in Figure 3.4 is considered in this chapter. This bridgeless PFC has very similar capability constraints as the typical bridged PFC shown in Figure 3.2 (with fewer semiconductors and thus higher efficiency [33]), and is deemed acceptable and representative for the controller design. This bridgeless PFC topology uses a generic cascade controller, illustrated in Figure 3.3.

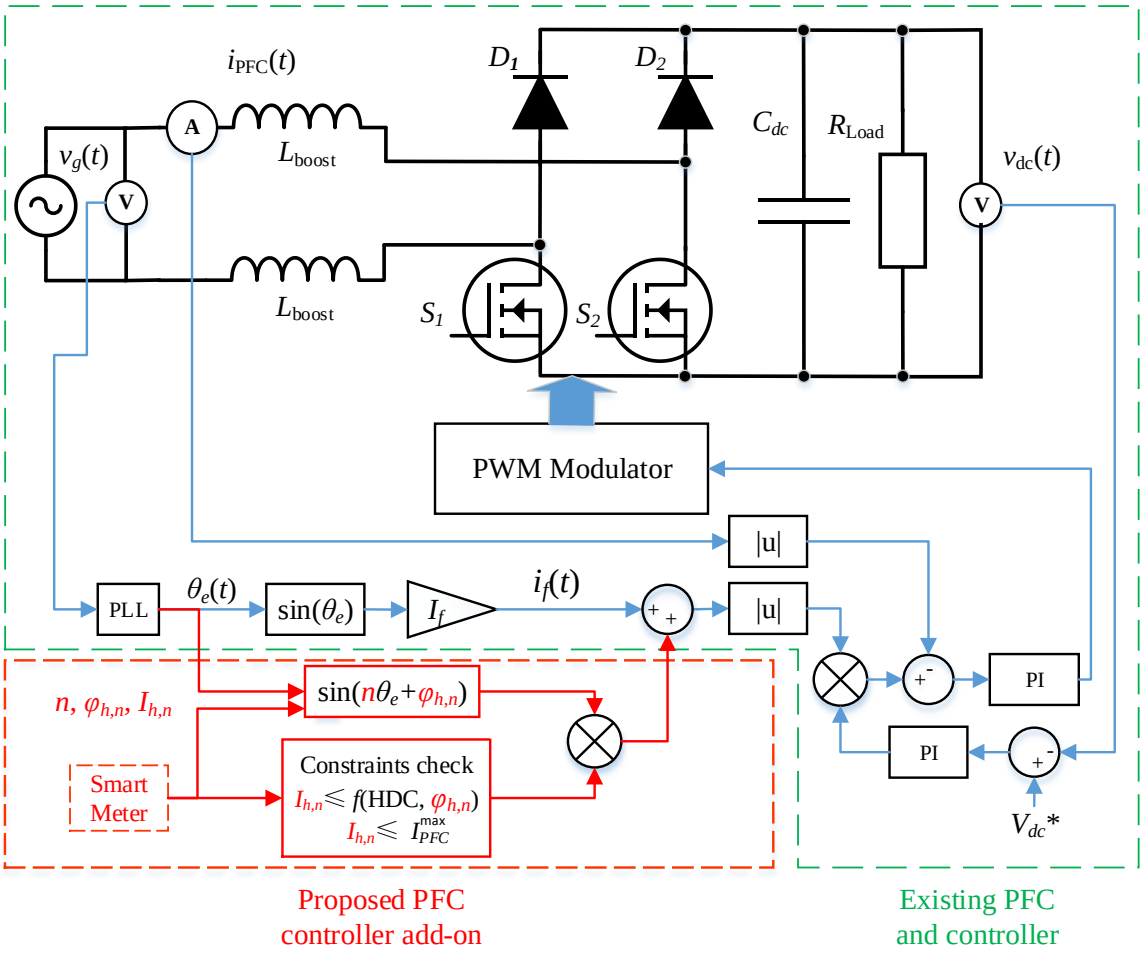

Figure 3.9 Proposed PFC controller with harmonic injection assuming operation in CCM and DCM.

In order to include the harmonic injection feature, an auxiliary loop, herein referred to as the harmonic correction loop (HCL), is augmented into the original current control scheme. This HCL is shown in Figure 3.9 and is highlighted in red. Therein, it is seen that the HCL input consists of: 1) the voltage phase angle $\theta(t)$ which is extracted from phase voltage $v_g(t)$ via a phase lock loop (PLL); and 2) the measured information of each harmonic (harmonic order *n*, phase shift φ_h, and magnitude I_h) as fed from the smart meter. Inside the harmonic correction loop, two control paths exist. First, the harmonic waveform is computed. Second, the harmonic magnitude $I_{h,n}$ is checked against constraints. In particular, to consider a practical PFC, the peak value of the line current $i_{PFC}(t)$ should be limited by the device's maximum allowable current, $I_{\mathrm{PFC}}^{\max}$. This limit may be attributed to the boost inductor L_{boost} saturation current or the switching device current limit. Therefore, in addition to the HDC constraint (3.9), the PFC is also limited to the overloading constraint as

$$\left|i_{\mathrm{PFC}}(t)\right| < I_{\mathrm{PFC}}^{\max}, \tag{3.10}$$

3.5 Simulation Studies

To verify the effectiveness of the PFC–based harmonic compensation at a system level, a small–scale distribution system shown in Figure 3.10 has been simulated. This study assumes that the nonlinear load injects harmonics of various orders (i.e. 3rd, 5th, 7th, etc.). The nonlinear load is simulated as a resistor in parallel with the harmonic current source. The system parameters together with the PFC loads are summarized in Appendix B. The harmonic content of

the nonlinear load is summarized in Table 3.2. The line current at the PCC is shown in Figure 3.11. To compensate these harmonics, an array of smart PFC loads is connected as well, where each PFC is used to compensate a specific harmonic. As seen in Figure 3.11 (left side), the original current at PCC has a THD of 9.5%. When the harmonic compensation by smart PFC loads is activated at t = 0.335s, the current waveform immediately becomes smoother, resulting in the improved THD = 4.7%.

Harmonic Order	$\omega_{h,3} = 3\omega_e$	$\omega_{h,5} = 5\omega_e$	$\omega_{h,7} = 7\omega_e$
Harmonic Magnitude(A)	2.4	1.2	1.8
Harmonic Angle φ (rad)	1.54	0.96	2.51

Table 3.2 Harmonic contents of nonlinear load.

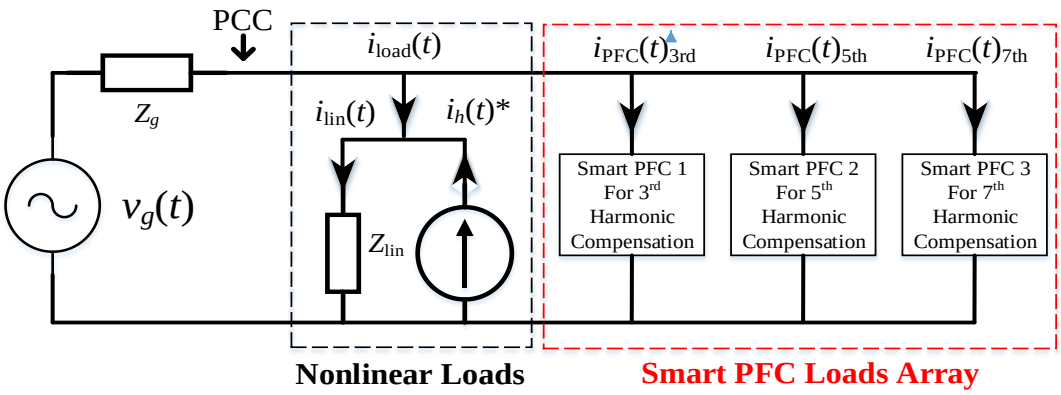

Figure 3.10 Small–scale setup for verifying PFC–based harmonic compensation using smart PFC loads with compensation of 3rd ,5th, and 7th harmonics.

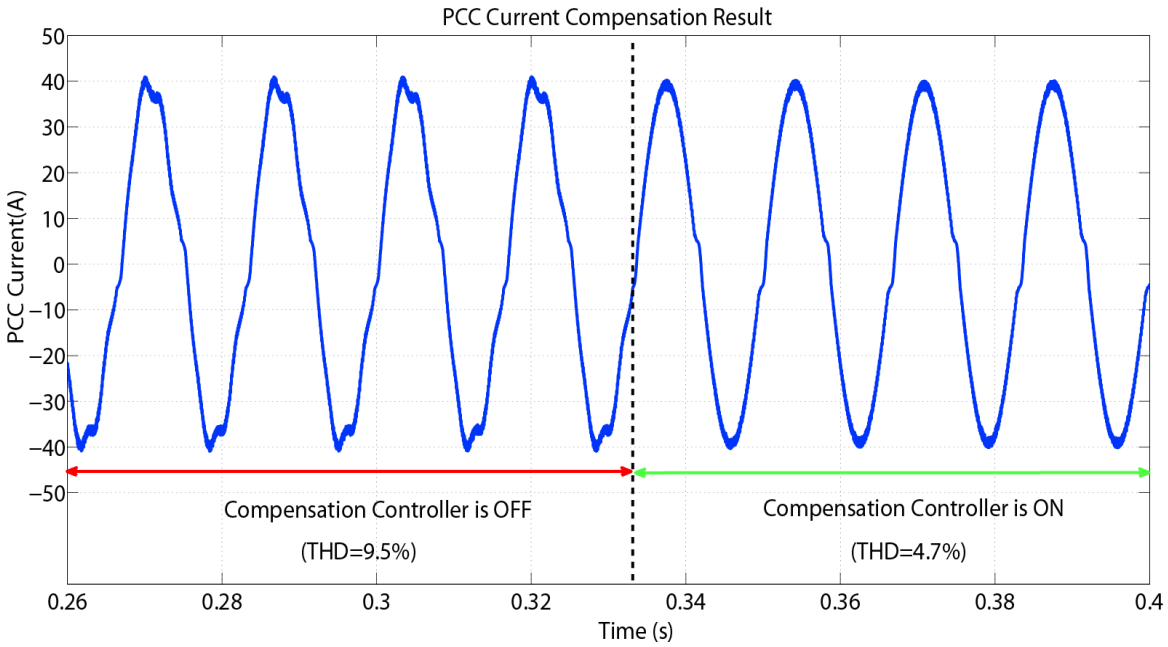

Figure 3.11 Results of harmonic compensation at PCC using three smart PFC loads with compensation of 3^{rd} ,5^{th}, 7^{th} harmonics at t = 0.335 s.

3.6 Experimental Results

To emulate a single PFC with harmonic compensation, the system with controller shown in Figure 3.11 has been implemented in the PELCS toolbox in MATLAB/Simulink [13][14]. The system parameters are summarized in Appendix B. To verify the harmonic inject feature using the proposed controller, the experimental tests are carried out on the Alpha Technology Ltd. bridgeless PFC prototype shown in Figure 3.12. This prototype is a digitally controlled PFC based on the Texas instrument C2000 microcontroller (F28035), which is reprogrammed to have the capability of injecting lower order harmonics ($n \leq 8$) at any given amplitude and phase angle. To demonstrate the operation, an example of injecting 20% RHM of 3^{rd}, 5^{th} and 7^{th} harmonic at a 180–degree phase angle is shown in Figure 3.13. Therein, it can be seen that despite the fact that the AC grid voltage v_g naturally contains 5^{th} and other harmonics, it is possible to inject

harmonic currents of other orders by simply reprogramming the existing PFC controller. This modification of the controller code also avoids any hardware modifications.

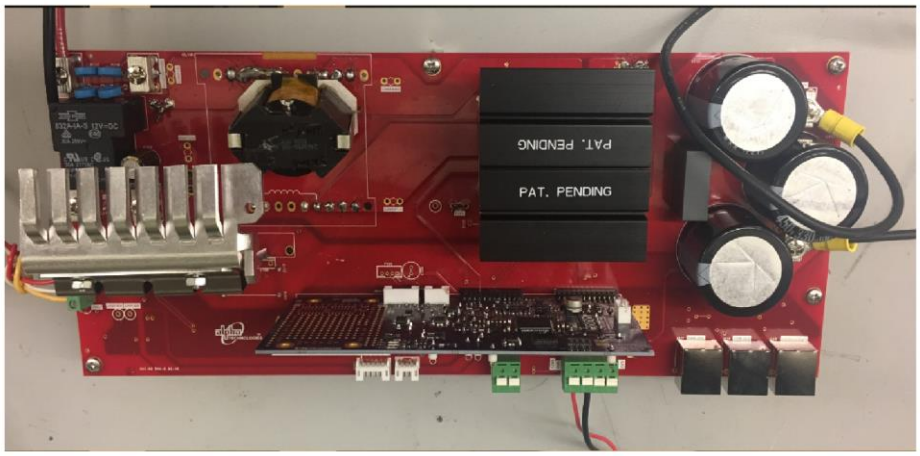

Figure 3.12 Alpha Technologies Ltd. PFC prototype used in experimental studies in this chapter.

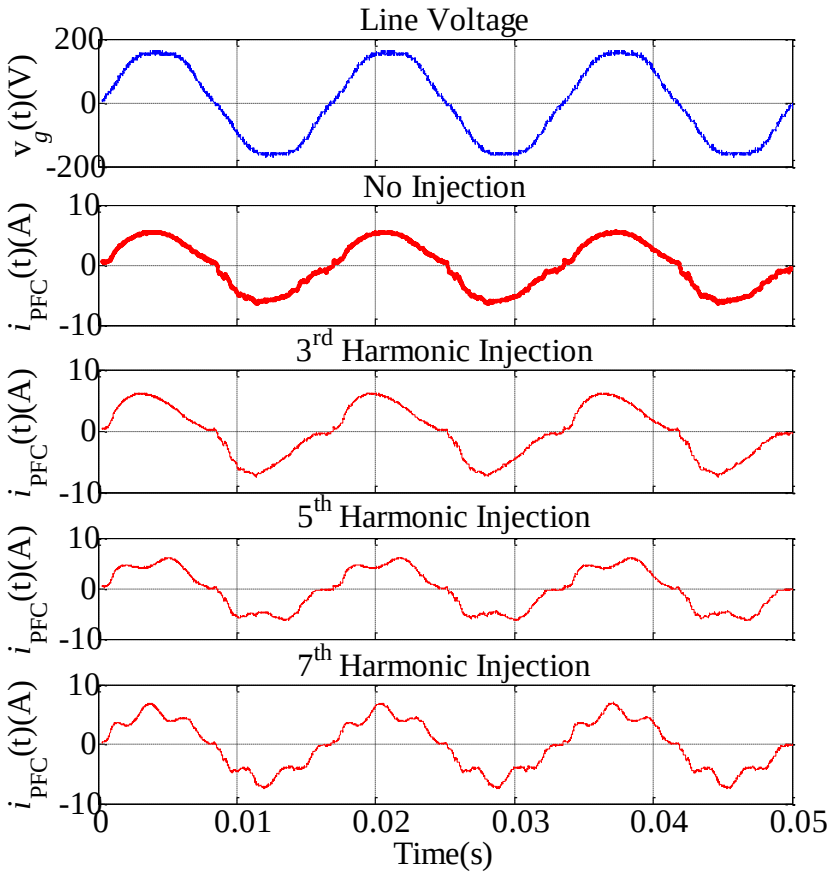

Figure 3.13 Experimental results of harmonic injection using Alpha PFC stage.

Chapter 4: Design and Demonstration of Smart LED Lighting for Harmonic Compensation

The LED lighting industry has been advancing rapidly in recent years. As the manufacturing cost of LED die drops, this technology is strongly positioned to replace CFL and incandescent light solutions. LED lighting has remarkable advantages over other types of lighting solutions. For example, it converts electricity to light with efficiencies approaching 50% [34]. Although LED has a history of over 50 years since its invention along with other transistors [17], LED lighting has only been introduced in the recent decade. Other than the cost of LED itself, the requirement of a proper driver is one of the many reasons that have limited this technology. For many modern lighting applications, most LED drivers now require a PFC as the first stage, followed by a DC/DC stage for dimming and other purposes. This first PFC stage potentially enables harmonic compensation in a similar way as other PFC devices discussed in the previous chapter.

As the LED market expands, it is envisioned that LED lighting loads soon will become a significant portion of total electricity consumption in the power grid. Therefore, a great impact could be made if future LED drivers have harmonic compensation capabilities. Additionally, there are other benefits for integrating harmonic compensation into the application of LED lighting. For instance, lighting is widely and evenly distributed in the power grid, which could allow wide and distributed compensation coverage. At the same time, while it may be difficult to convince consumers to install dedicated AHFs, it would be much easier to promote LED lighting as a common trend. Moreover, industry envisions that future LED lighting devices will be wirelessly controlled through networks of sensors and IoT to enable advanced features and user

control. Thus, smart LED lighting with harmonic compensation seems a highly viable endeavor in the near future.

4.1 LED Lighting System Configuration

The industrial partner, OmniSolu Ltd., has entered the LED lighting industry with their IoT feature, where each LED lamp can be wirelessly controlled by users through the Zigbee network. Users can dim lighting and/or change the color as needed, and have the freedom to switch off the light completely to save power. In addition, each lamp has the capability to measure and report its power consumption in real time. OmniSolu offers a front-end attachment to the LED driver in order to realize the wireless reading and control features. A generic OmniSolu system configuration is depicted in Figure 4.1. The modular design allows OmniSolu to wirelessly control most drivers and LEDs in the market and have the freedom to integrate new features. However, this configuration can only allow certain features to be added to LED lighting due to the fact that the driver itself is not accessible.

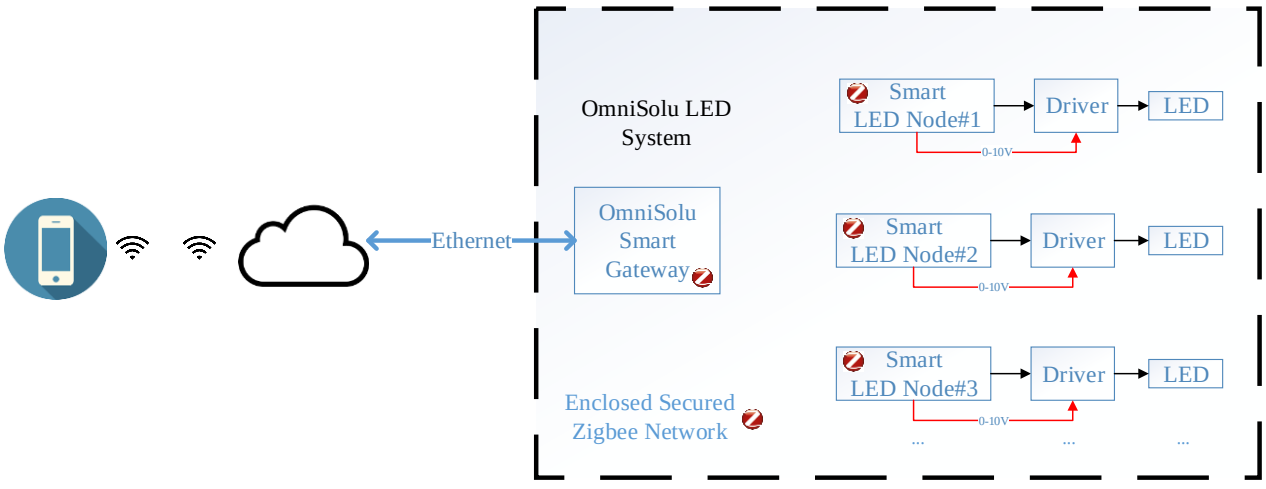

Figure 4.1 A generic OmniSolu LED lighting system configuration.

4.2 Requirement of the Design

In order to integrate the harmonic compensation feature, the existing OmniSolu front–end features need to be integrated into the driver, eventually simplifying the system and saving manufacturing cost. Therefore, a brief requirement is made with Omnisolu for the prototyping stage as following:

- Driver must be equipped with Zigbee for wireless control
- Driver should work with input voltages 90V – 240V AC
- Driver must provide constant output current up to 750mA
- Dimming and on/off are required
- Harmonic injection is required
- Power consumption measurements and reporting is required

The above features can be implemented in a new system configuration shown in Figure 4.2. As the study in Chapter 2 demonstrated, system harmonics can be compensated by the PFC of smart loads. In this case, LED lighting will become a truly smart load with communication and harmonic compensation capabilities, in addition to providing controllable light. It is envisioned that a large collection of such LED devices communicating with each other, along with advanced control via the IoT, will provide enhanced functions and capabilities to consumers.

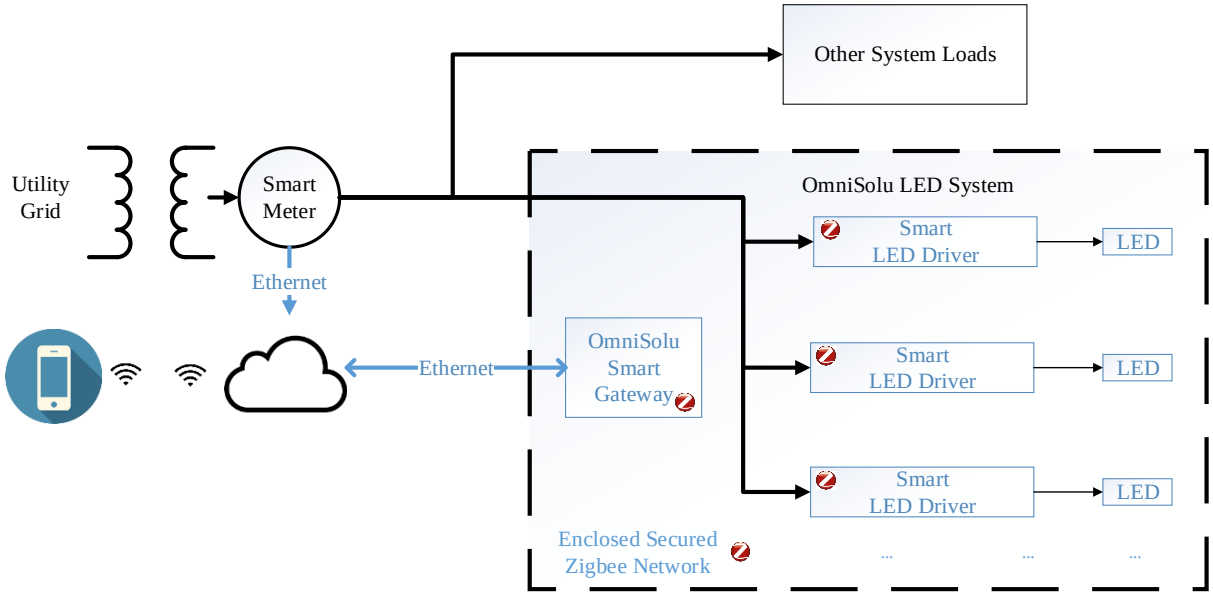

Figure 4.2 Envisioned desired LED lighting system configuration.

4.2.1 Topology selection

For LED driver design, many topologies can be used. In order to comply with industrial standards for driving LED lamps, the driver should commonly consist of two stages; the first stage is usually a PFC, and the second stage is a DC/DC converter that supplies constant current to the LED. Without loss of generality, in this thesis a full bridge Flyback converter as shown in Figure 4.3 has been selected. This topology is beneficial due to its simplicity and use of only one transistor, while also offering galvanic isolation and delivering power up to 250W. However, this case still involves a unidirectional converter and thus the topology constraints analyzed in chapter 3.2 still apply here. Overall, this topology has been considered an ideal candidate for prototyping the PFC stage.

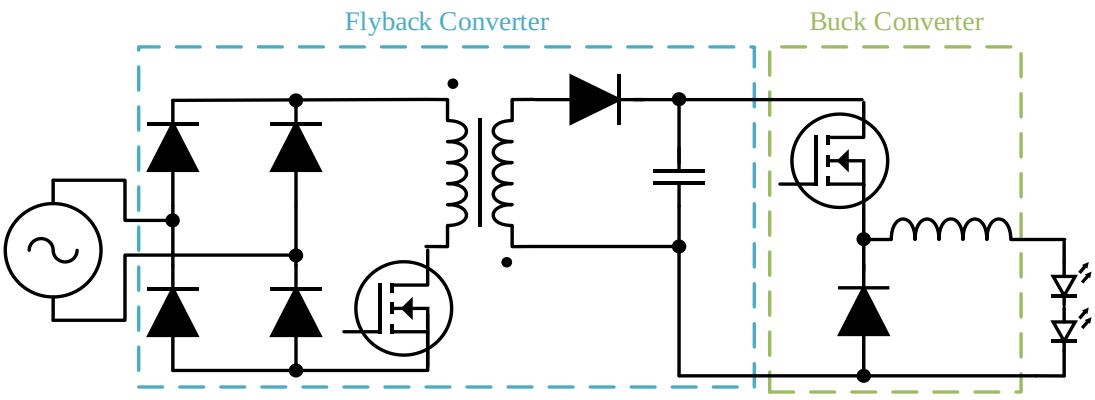

Figure 4.3 Flyback and Buck topology.

In order to dim the LED, the second stage DC/DC converter has to operate in a current control mode. The DC/DC stage must also accept a wide input voltage range at double the line frequency ripple (120Hz for 60Hz grid), while maintaining a constant current at its output to drive the LED [35]. A Boost or Buck topology can meet this requirement. In this thesis, a Buck topology is selected, as shown in Figure 4.3. A Texas Instrument commercial IC LM3409 [42] is used in this case. It is important to note that this stage would not affect the performance and capabilities of harmonic compensation, which is determined by the front stage and its modulation.

4.2.2 Microcontroller unit selection

Most commercial LED drivers use analog control to save cost. However, in order to enable advanced features such as harmonic compensation and fully evolve to the level of true IoT power electronics, digital control is essential. The desired microcontroller unit (MCU) must be sufficiently fast to satisfy the requirements of both phase lock loop (PLL) and harmonic modulation, and process all calculations. As the injected harmonic order increases, the

discretized control loop must have sufficient control loop band width (e.g. 50kHz for 420Hz injection). This imposes a challenge for MCU computing power. Furthermore, the MCU must contain peripherals such as a high resolution analog to digital converter (ADC), pulse width modulation (PWM), and a serial communication port. After conducting ample literature research, the Texas Instrument C2000 MCU family, F28377s [40] has been chosen for experimental prototyping. This MCU has an extensive supporting software library and appropriate specifications, such as 200MHz core speed and 32 bit floating number processing power.

4.2.3 Discretized PI controller with limiter

The proportional and integral (PI) controller is used in this design. A continuous PI controller is shown in Figure 4.4. According to the Texas Instrument C2000 Digital Controller Library User's Guide [41], the discretized PI controller with output limiter is implemented according to Figure 4.5. This implementation is used in MCU and simulation.

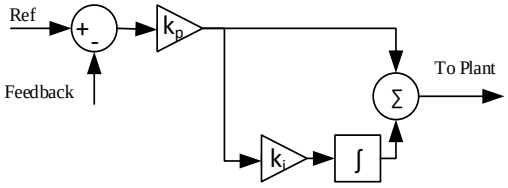

Figure 4.4 Conventional PI controller.

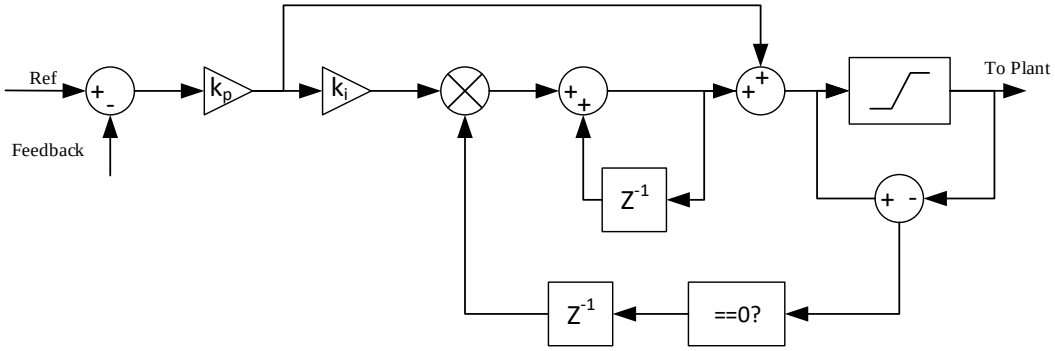

Figure 4.5 Discretized implementation of PI controller with output limiter.

4.3 Simulation Studies

Prior to prototyping, the topology considered in Figure 4.3 has been implemented in PELCS toolbox in the MATLAB/Simulink environment. The controller proposed in Chapter 3.4 can be used as illustrated in Figure 4.6. The overall model consists of a detailed model for the Flyback and Buck converter along with the necessary filters. To simplify the diagram, the filters are not shown in Figure 4.6. A detailed PLECS model and parameters can be found in Appendix C. The harmonic controller is implemented according to Section 3.4.

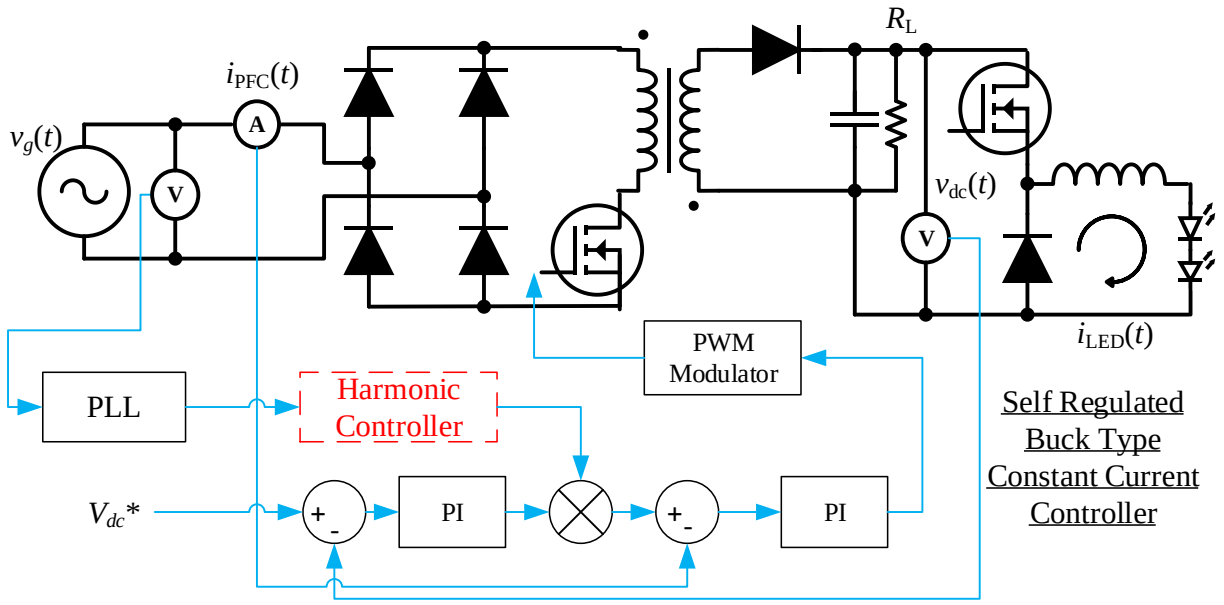

Figure 4.6 Proposed controller design for the considered Flyback PFC smart LED driver.

4.4 Design of Hardware Prototype

A picture of the hardware prototype is shown in Figure 4.7. This prototype is capable of delivering up to 50W power and can accept universal voltage input (120V ~ 240V AC). It is

equipped with a Texas Instrument LM3409 constant current regulator at the DC/DC stage to drive the LEDs. In this design, the controller stage is galvanic-isolated from the AC side for safety and noise immunity. Lastly, the relevant PCB schematics and other parameters and components are provided in Appendix D.

This hardware prototype is capable of injecting harmonics and dimming the LED, and it can be attached to a Zigbee module through a Universal Asynchronous Receiver–Transmitter (UART) for wireless control purposes. To test thermal performance under a load, a thermal image of the developed smart LED driver prototype captured by a FlirOne infrared camera is shown in Figure 4.8. As can be seen from Figure 4.8, the DC/DC current regulator generates most of the heat. Although this may be addressed in future improved design, this does not affect the overall performance of the driver, or its PFC input stage in particular.

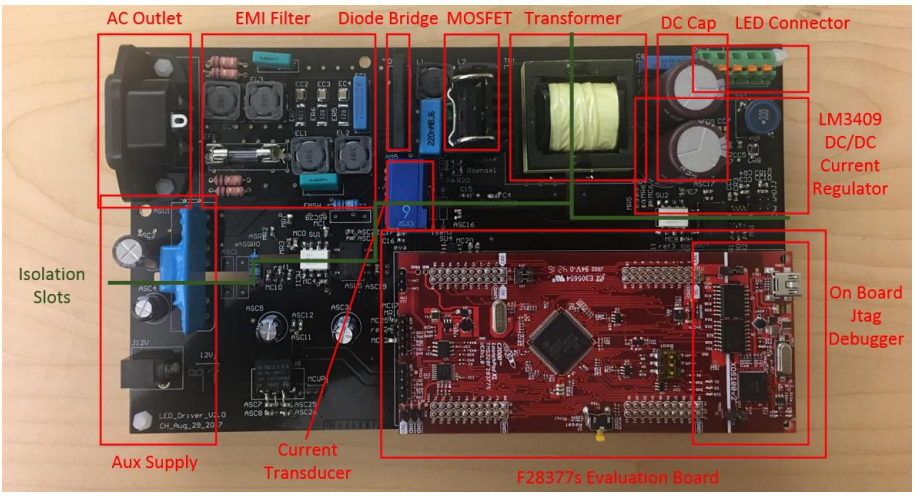

Figure 4.7 Prototype of smart LED driver showing details of PCB and components.

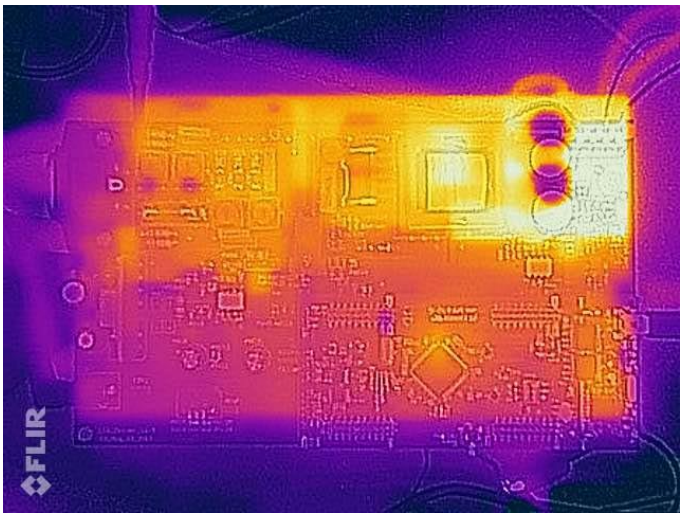

Figure 4.8 Thermal image of the developed smart LED driver prototype.

4.5 Simulation and Experimental Results

Due to the presence of voltage harmonics in the AC mains of UBC's Kaiser building, where the experimental setup has taken place, the actual non–ideal voltages have been recorded and used in simulations as the source, in order to match the later experimental results. The model is tested under 120V AC input and 55V DC output. Due to safety precautions and ease of experimentation, the circuit is loaded to 30W (60% of designed power rating). As a result, the driver is loaded with a combination of one resistor (R_L =124Ω) and one LED, and the current of LED is regulated at $i_{LED}(t)$=0.1A.

The experimental set up and the detailed simulation summarized in Appendix C closely match the circuit schematics shown in Appendix D. Corresponding simulations and experimental results are shown in Figure 4.9 through Figure 4.12. Waveforms were captured by a Tektronix DPO 2014B oscilloscope equipped with a Tektronix TCPA300 current probe.

Several case studies have been considered in order to verify the methodology described in Chapter 3. In Figure 3.6, the allowable injected RHM is relatively high when the harmonic angle φ is close to 0 and π. Injecting harmonics when φ is close to π/2 will result in DCM operation of the line current and additional harmonics, as discussed in Chapter 3.

In the first study presented in Figure 4.9, the PFC stage operates conventionally and no additional harmonics are injected. However, due to non–ideal supply of AC voltages in the experiment setup, which contains a significant 5^{th} harmonic, the PFC line current (even without injection of additional harmonics) has some distortion and follows fairly closely to the voltage waveform, as can be seen in the figure. Although the input PFC current has noise caused by the hardware current feedback loop, overall this is considered acceptable for the purpose of injecting other harmonics.

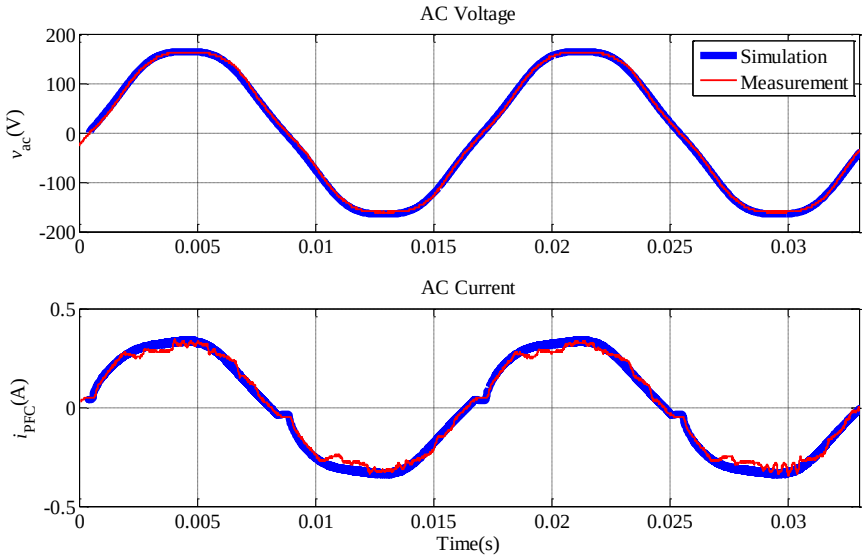

Figure 4.9 LED driver PFC operation without harmonic injection.

Next, the study presented in Figure 4.10 depicts the results of injecting additional harmonics, one at a time, with the angle φ = 0. In particular, Figure 4.10 (first subplot), illustrates

the line current waveform (measured and simulated) and its spectrum resulting from injecting the 3rd harmonic. As can be seen in Figure 4.10 (first subplot), the 3rd harmonic reaches an RHM of approximately 0.5 in the measured current, which demonstrates the concept of injection. Figure 4.10 (second subplot) shows the measured and simulated results of modulating and injecting the 5th harmonic, which reaches an RMH of approximately 0.45 in the measured line current of the PFC stage. Similarly, Figure 4.10 (third subplot) shows the measured and simulated results of modulating and injecting the 7th harmonic, which reaches approximately 0.3 in the measured current. In all three cases, we can see that in addition to the injected harmonics, there exists other harmonics up to the 9th, which may be attributed to the non-ideal supply voltage, limited resolution, bandwidth of the controller, hardware and measurement noise, etc.

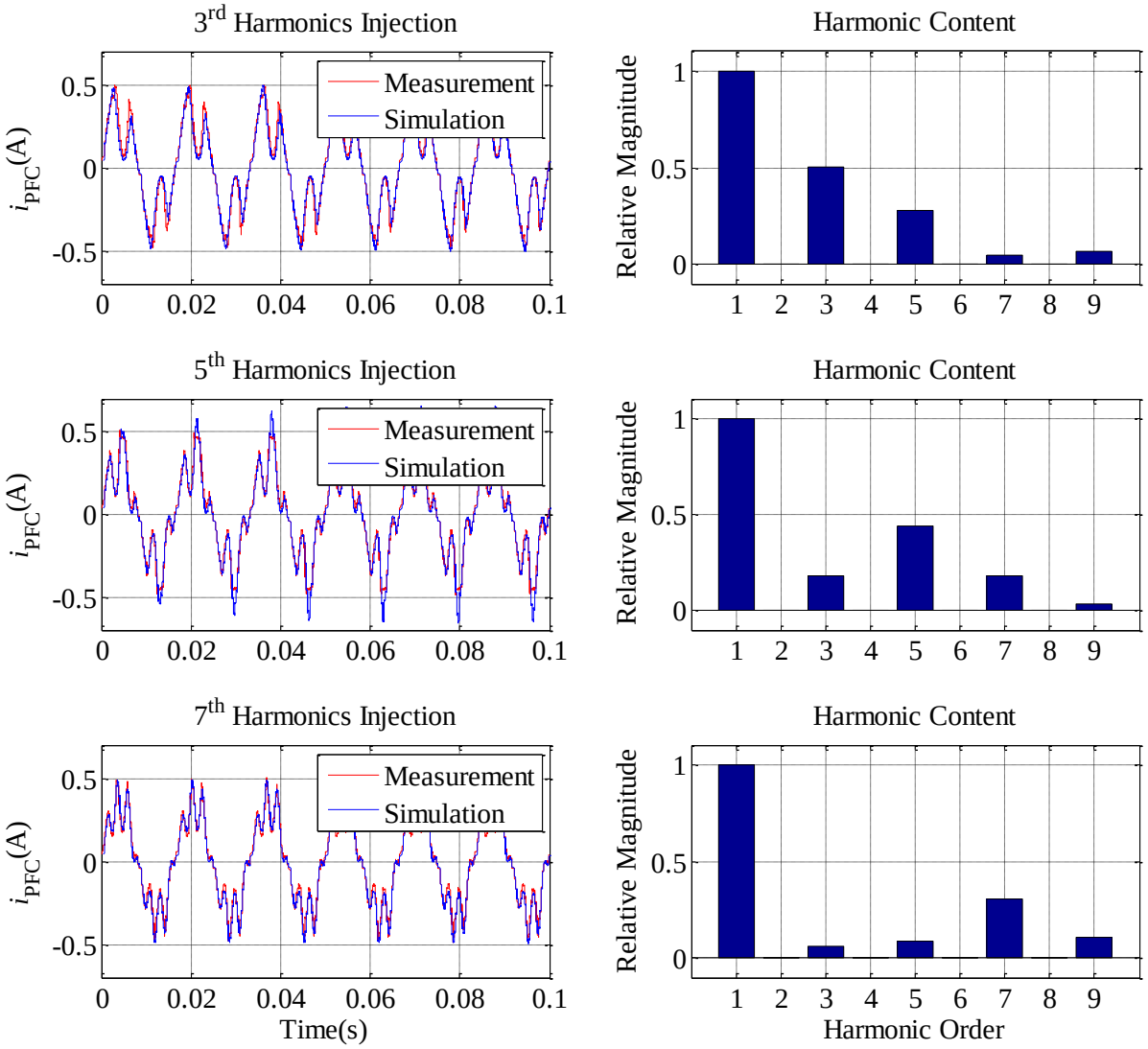

Figure 4.10 LED driver front PFC operation with injection of harmonics under φ = 0.

To demonstrate harmonic injection at different angles, the study presented in Figure 4.11 depicts the results of injecting additional harmonics, one at a time, with an angle $\varphi = \pi/2$. In particular, Figure 4.11 (first subplot), shows the measured and simulated PFC current waveform and its spectrum resulting from injecting the 3rd harmonic. As Figure 4.11 shows (first subplot),

the 3rd harmonic in the measured current reaches approximately 0.35, but the other harmonics such as the 5th and 7th are also presented at lower magnitudes. Figure 4.11 (second subplot) shows the measured and simulated results of injecting the 5th harmonic, which reaches approximately 0.25 in the measured current. Next, Figure 4.11 (third subplot) shows the measured and simulated results of injecting the 7th harmonic, which reaches approximately 0.22 in the measured current. In all three cases, we see that the injected harmonic is always the largest, which proves the concept and capability of injecting desired harmonics even at large angles. At the same time, one can clearly observe in Figure 4.11 that the PFC line current enters the DCM, which further distorts the waveforms and leads to the presence of other harmonics.

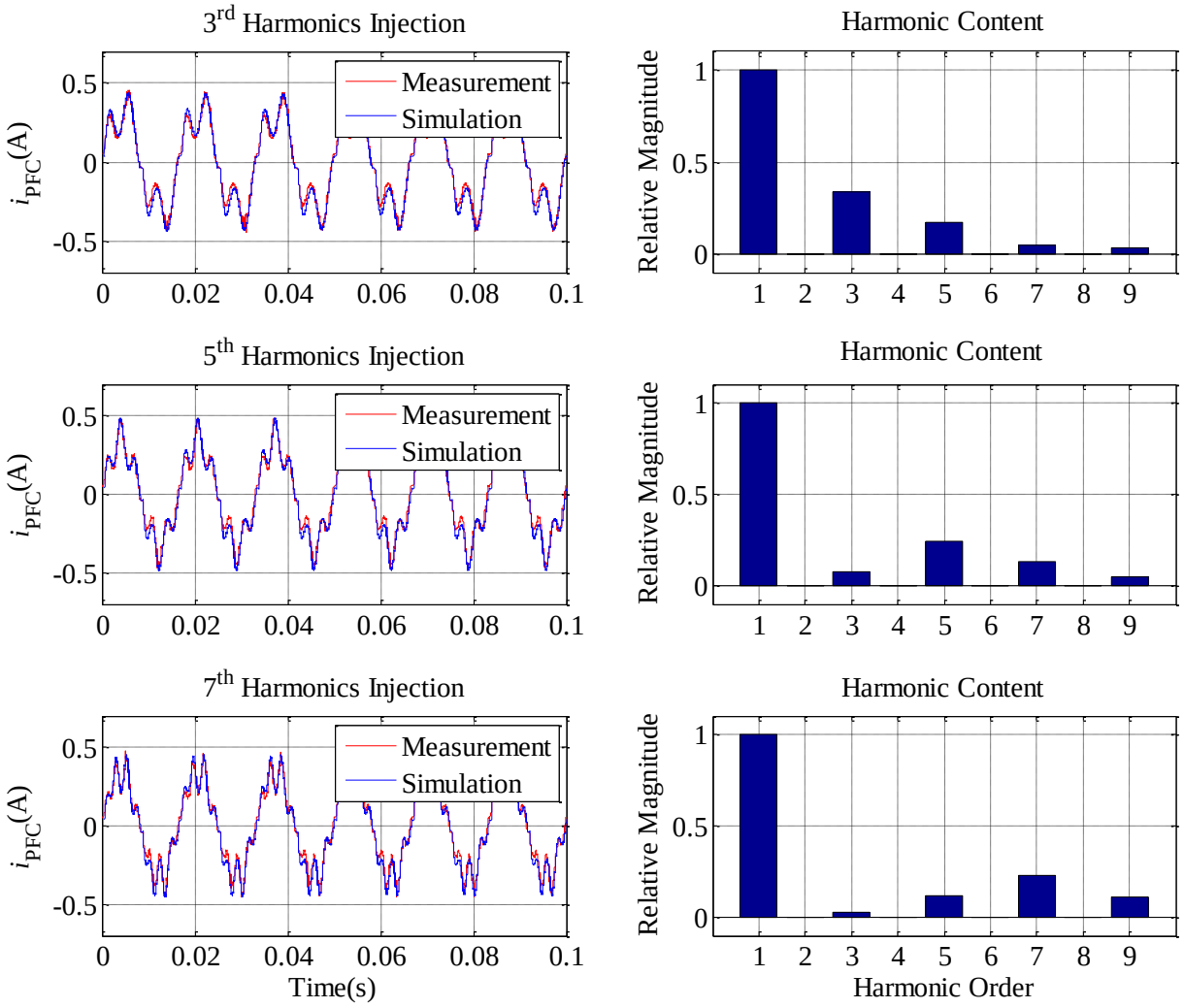

Figure 4.11 LED driver front PFC operation with injection of harmonics under φ = π/2.

Next, Figure 4.12 depicts the results of injecting additional harmonics, one at a time, with angle φ = π. Specifically, Figure 4.12 (first subplot), shows the measured and simulated PFC current waveform and its spectrum resulting from injecting the 3rd harmonic. As can be seen in Figure 4.12 (first subplot), the 3rd harmonic reaches approximately 2.8, and the other harmonics, such as 5th and 7th, are also present at much lower magnitudes. Figure 4.12 (second subplot)

shows the measured and simulated results of injecting the 5^{th} harmonic, which reaches approximately 0.14 in the measured current. Next, Figure 4.12 (third subplot) shows the measured and simulated results of injecting the 7^{th} harmonic, which reaches approximately 0.09. In all three of these cases, again the injected harmonic is always the largest, which here proves the capability of injecting the desired harmonics at angle $\varphi = \pi$. It can also be observed in Figure 4.12 that the PFC line current is in CCM, and the waveforms are not as distorted as they are in Figure 4.11.

Overall, the results presented in Figures 4.9 – Figure 4.12 demonstrate the capability of the LED drive's PFC front stage to inject significant harmonics (i.e. 3^{rd}, 5^{th}, and 7^{th}) at different angles and with different magnitudes. It has also been observed experimentally and in simulation that in order to achieve the desired injected harmonic magnitude, the current controller (and the underlying current control loop) has to be sufficiently fast in terms of its response (bandwidth) as well as sampling time. If the overall current controller does not have sufficient bandwidth, then one observes that the injected harmonics may fall below their corresponding reference signal.

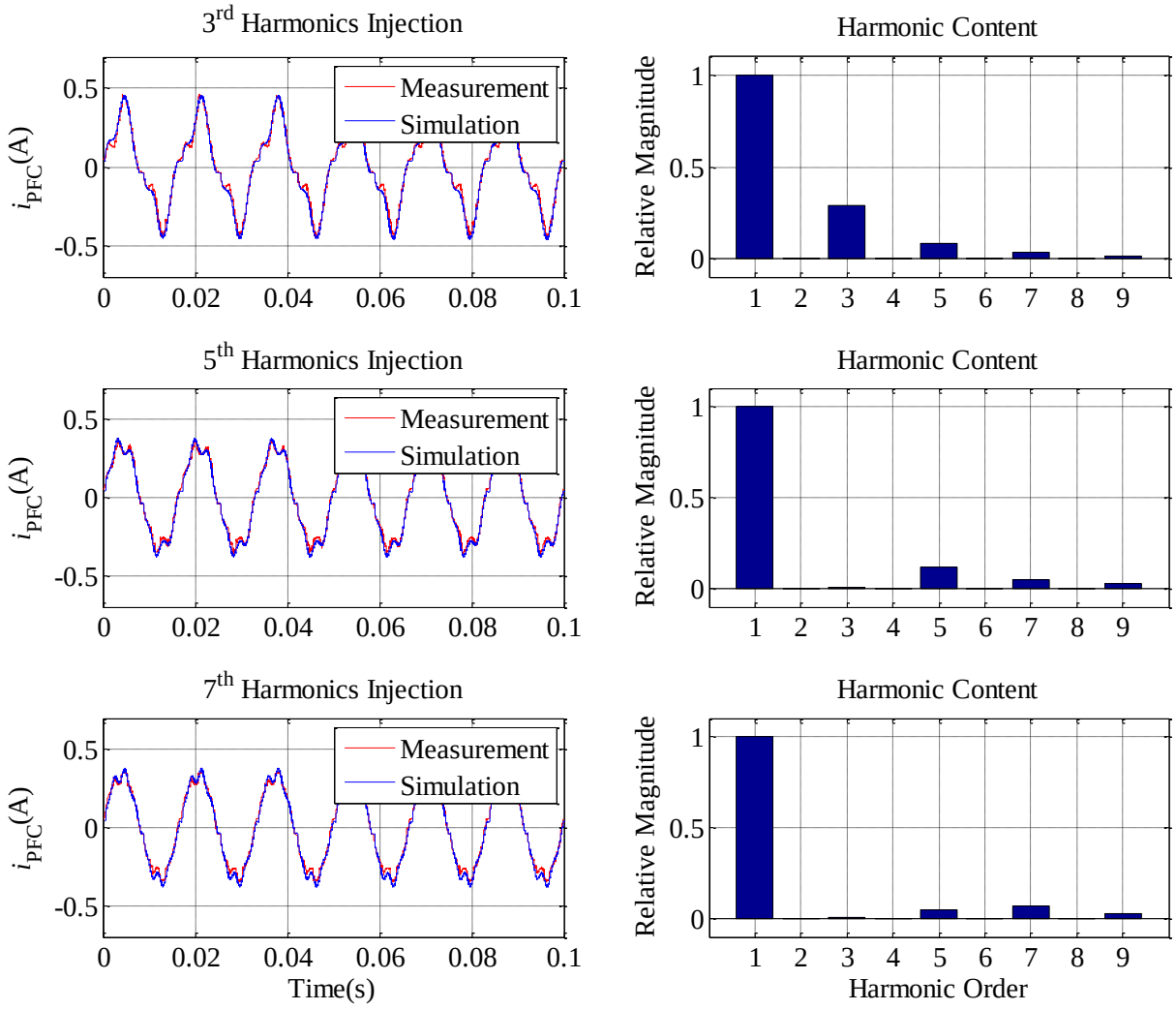

Figure 4.12 LED driver front PFC operation with injection of harmonics under φ = π.

Chapter 5: Conclusions and Future Work

As distribution systems become more sophisticated the number of electronic loads increases rapidly, and it is envisioned that these increased loads will communicate with smart meters installed at PCC to gather harmonic data in real time. If the frond–end rectifier and PFC stage of power electronic loads can carry the compensation tasks, the compensation of harmonics may be achieved in a distributed fashion and we can avoid installing dedicated AHFs. In light of this, the present thesis explores and proposes an innovative method of harmonic compensation based on distributed smart electronic loads. This concept is demonstrated through simulation studies, a commercial PFC rectifier, and prototype LED drivers.

5.1 Contributions and Anticipated Impact

To set the stage for the considered research, a feasibility study was first performed to validate the concept of harmonic compensation in a building-type distribution system, as we achieved in **Objective 1**. The contributions of this research step lays in departing from the concept of using dedicated harmonic filters and instead using the available smart meter measurements and existing (installed) power electronic devices. Computer modeling of a benchmark electrical distribution system was developed based on the UBC Kaiser building. Using measured harmonic data fed by the building's smart meter, a grid–tie inverter was emulated to inject the out–of–phase current harmonics. Compensation strategies were proposed by analyzing collected historical data and the building's electrical distribution system based on the accessible documentation. Simulation studies were conducted in Section 2.3 to verify the effectiveness of the proposed method. It is envisioned that this method may be applied to

commercial and residential buildings equipped with smart meters and controllable (modifiable) AC/DC loads or integrated energy storage such as UPS.

The next research step addressed the question of possible modification of typical single phase commercial PFC devices, as achieved in **Objective 2**. Based on a commercial bridgeless PFC provided by Alpha Technologies Ltd, a detailed model of the device and the controller were developed. The harmonic injection features were successfully integrated to the PFC by re–programing the controller algorithm without hardware modification. The contribution of this step was the analysis of topological constraints imposed by the front–end PFC rectifier diodes, and deriving the possible range of injecting harmonics of various orders, magnitudes, and phase angles in continuous and discontinuous conduction modes of the line current. Simulation and experimental studies presented in Sections 3.5 and 3.6 validate the proposed approach and the controller modifications. It is envisioned that, due to economic viability, PFC-based harmonic compensation by smart electronic loads may become widely applied to commercial and industrial applications with minimum modifications to power hardware.

Lastly, the presented concept was extended to PFC-based LED drivers, as achieved in **Objective 3**. In collaboration with OmniSolu Ltd., a Vancouver-based LED lightning company, a smart LED driver was developed and experimentally prototyped. The driver was designed as a two–stage full bridge Flyback type converter, which differs from the topology used for the PFC rectifier by Alpha Technologies, Ltd. Here, the developed driver possessed advanced capabilities of harmonic compensation and wireless communication, and is thus suitable for both residential and industrial lighting applications. This step extends the proposed methodology to other devices with high–bandwidth power electronic converters at the front stage. It is envisioned that such advanced smart LED drivers with harmonic compensation and networking capabilities may

become part of a decentralized and distributed solution to the power quality of electrical distribution systems with smart meters, sensors, and advanced user interfaces.

5.2 Future Work

The proposed concept of harmonic compensation in distribution systems is an innovative idea, and as such it has many aspects that need further research. So far, the concept has only been demonstrated through simulations and experimental tests on standalone devices. The following aspects should be further investigated, developed, and demonstrated:

- Simultaneous harmonic compensation in distribution systems where multiple smart electronics loads communicate together with metering devices.
- Centralized and decentralized algorithms to coordinate and adjust the injections from all participating smart electronic loads in real time to achieve improvement of power quality on a system–wide and/or "globally sensitive" level.
- Explore wireless communication and IoT for further integration of smart electronic loads with advanced capabilities and features with metering sensors into a distributed and decentralized coexistence of scalable distribution systems.

Research in the above directions will greatly facilitate the development of smart grid and energy efficient technologies for buildings and communities in Canada.

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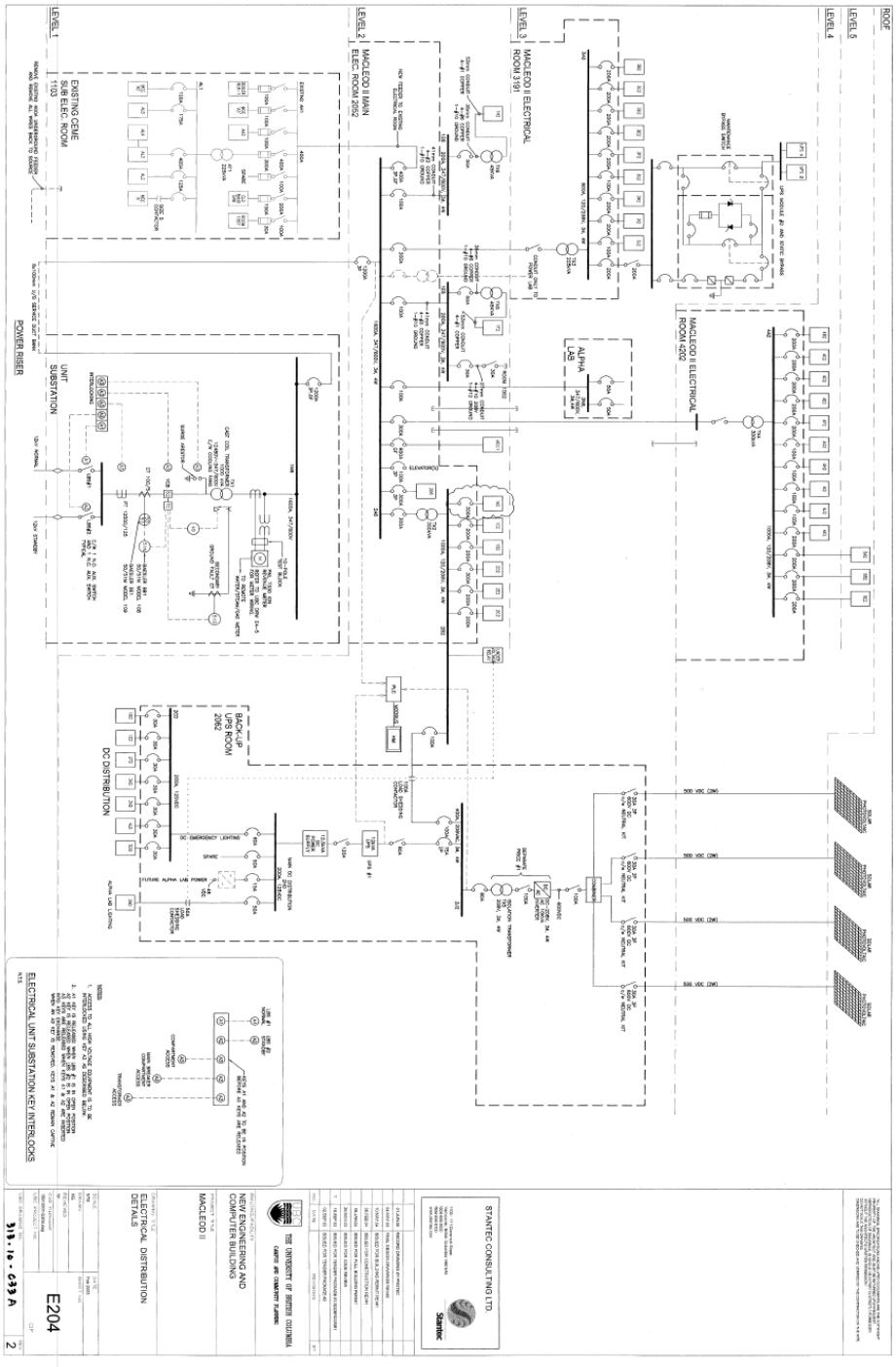
Appendices

Appendix A Kaiser Building Electrical Distribution System and Transformer Ratings.

A.1 Single Line Diagram of Kaiser Building Electrical Distribution System



A.2 Main distribution transformer TR0:

Capacity –1000KVA;

Primary – 12KV;

Secondary – 600V;

Impedance – 5.75%;

No Load Losses – 2900W;

Load Losses – 9000W.

A.3 Transformers TR1&3:

Capacity – 300KVA;

Primary – 600V;

Secondary – 208V;

Impedance – 2.2%;

No Load Losses – 1281W;

Load Losses – 6219W.

A.4 Transformer TR2:

Capacity – 225KVA;

Primary – 600V;

Secondary – 208V;

Impedance – 3.3%;

No Load Losses – 1415W;

Load Losses – 4412W;

Appendix B Test condition and Bridgeless PFC Parameters

B.1 Test system parameters:

V_g = 120V, L_{boost} = 120 µH,

R_{load} = 150Ω, C_{dc} = 990 µF,

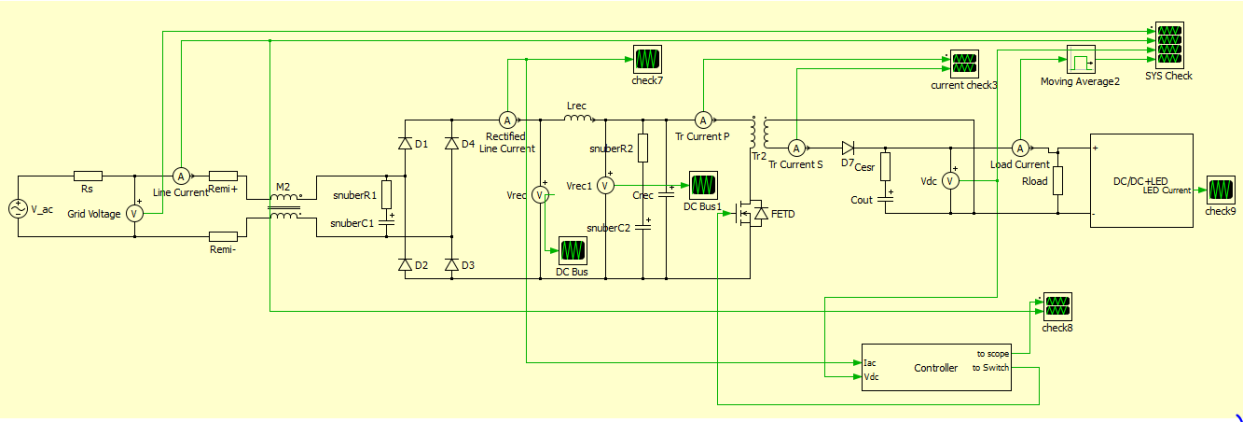
f_s = 70kHz, V^*_{dc} = 380V.

B.2 Small–scale setup parameters:

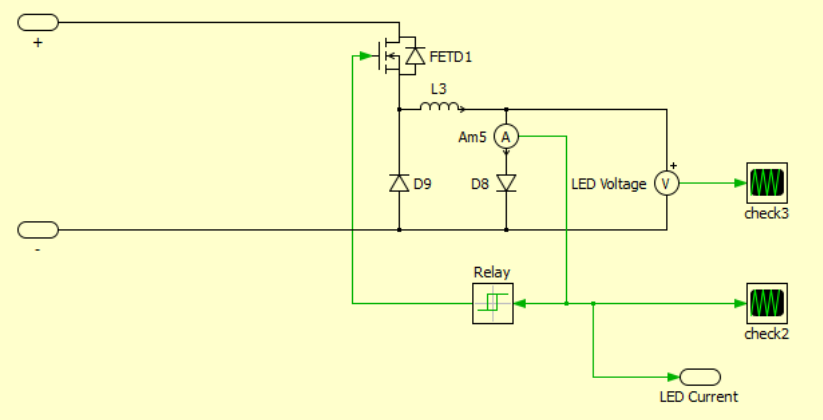
The PFC loads are rated at 2.4kW, and each is assumed loaded at 1kW;
other load Z_{lin}=37Ω; source V_g = 120V, Z_g =0.1Ω.

Appendix C PLECS Model of the Flyback PFC and System Parameters

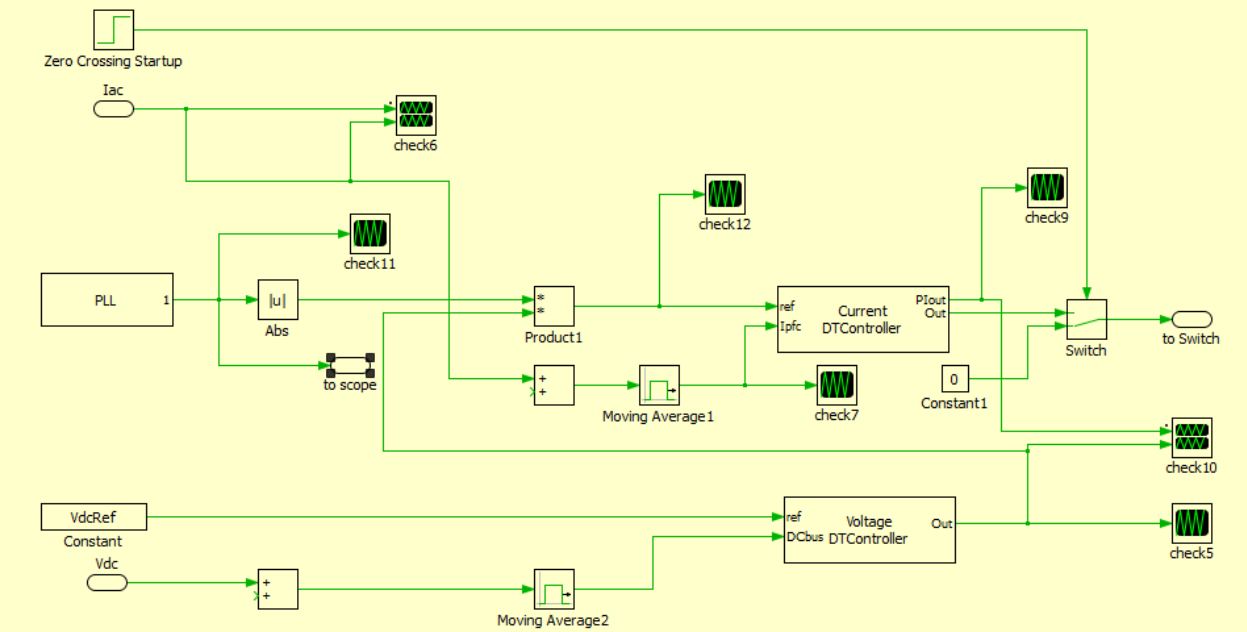
C.1 PLECS model of Flyback PFC



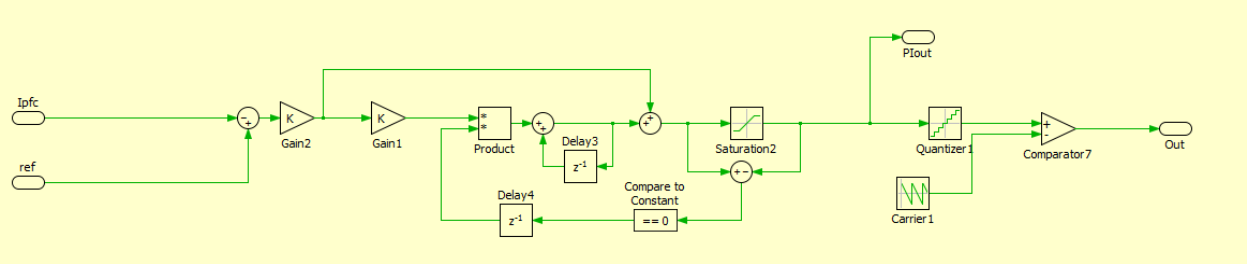
C.2 PLECS Model of the DC/DC converter and LED subsystem model:



C.3 PLECS model of controller subsystem:

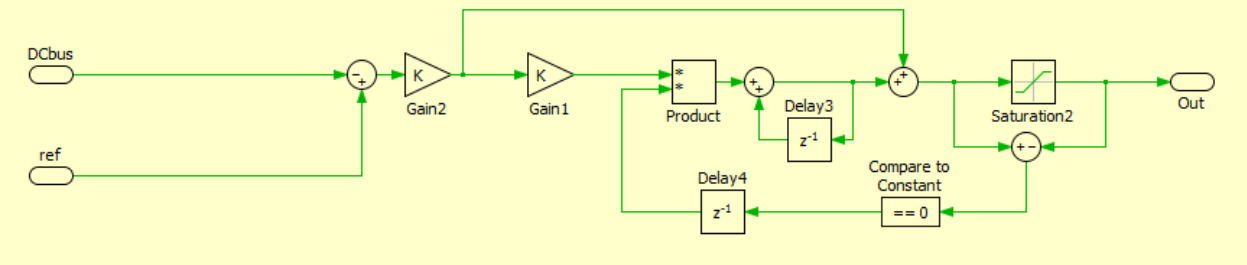


C.4 PLECS model of current DTController subsystem:



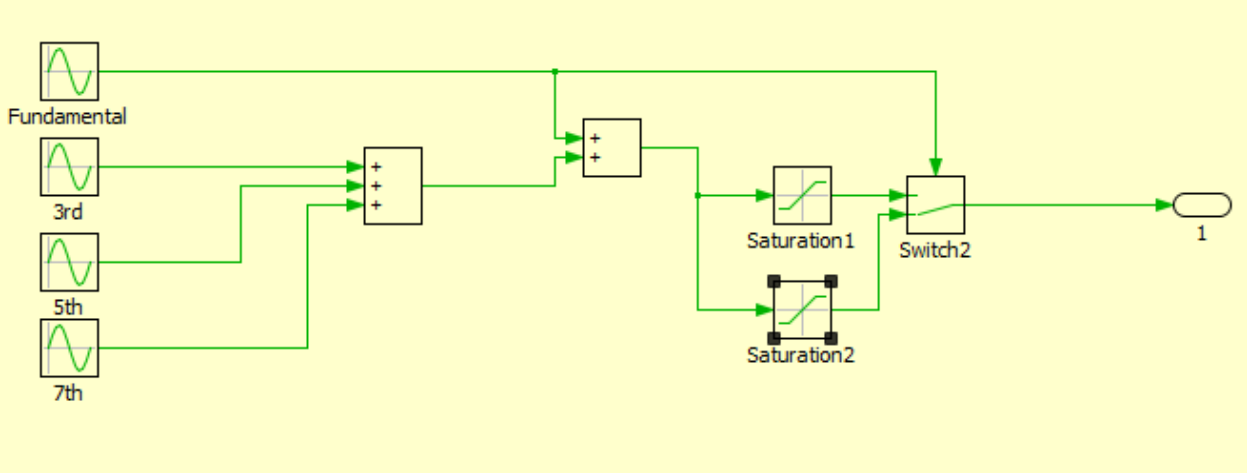
Sampling Frequency: 50kHz;

C.5 PLECS Model of voltage DTController subsystem:



Sampling Frequency: 1kHz;

C.6 PLECS Model of PLL subsystem:



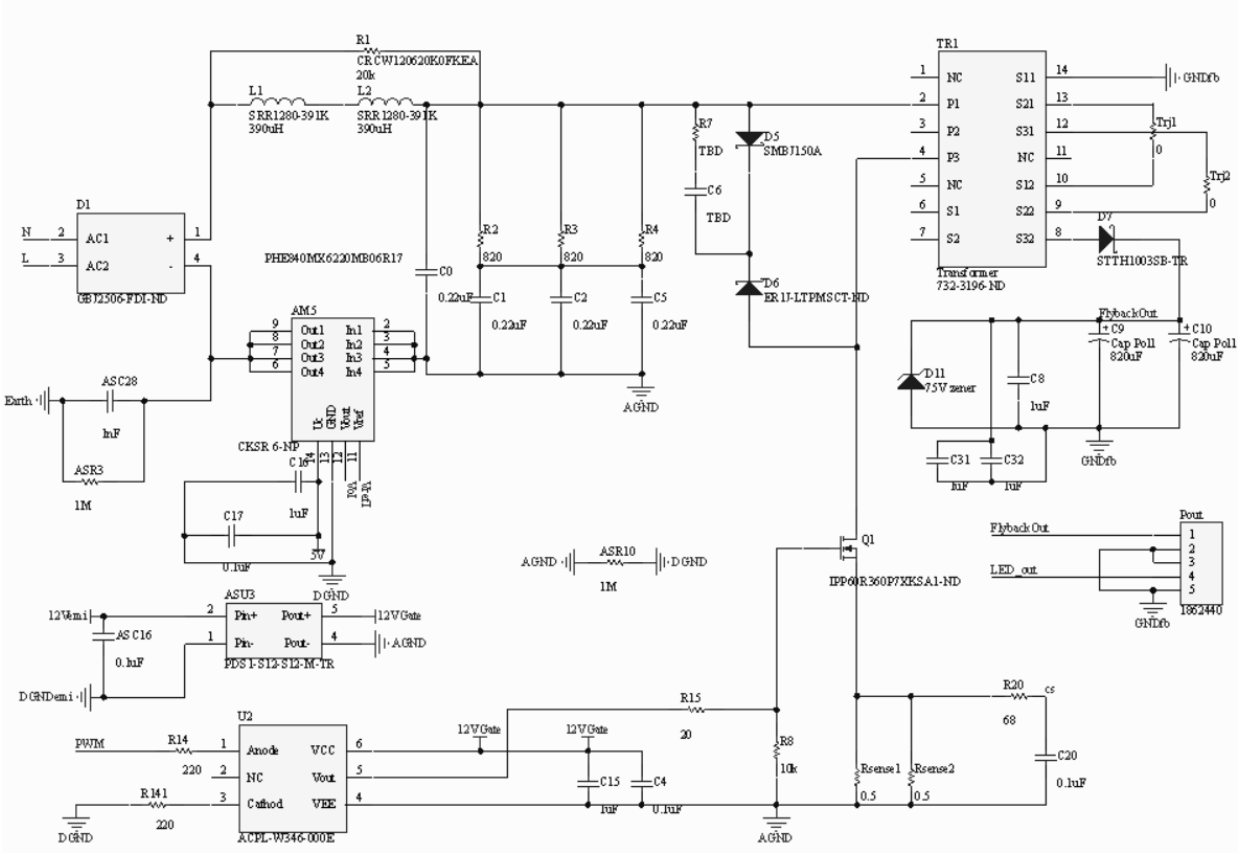
C.7 System parameters:

R_s=0.1Ω,	R_{emi}=1 Ω,	L_e=390uH,
V_d=0.7V,	L_{rec}=780μH,	C_{rec}=0.22μF,
L_m=180uH,	C_{dc}=1.64mF,	V_{dc_Ref}=55V,
V_{LED}=45V,	f_s=90kHz,	R_{load}=124 Ω,
R_{sunber}=227 Ω,	C_{sunber}=0.66μF,	i_{LED}=0.1A,

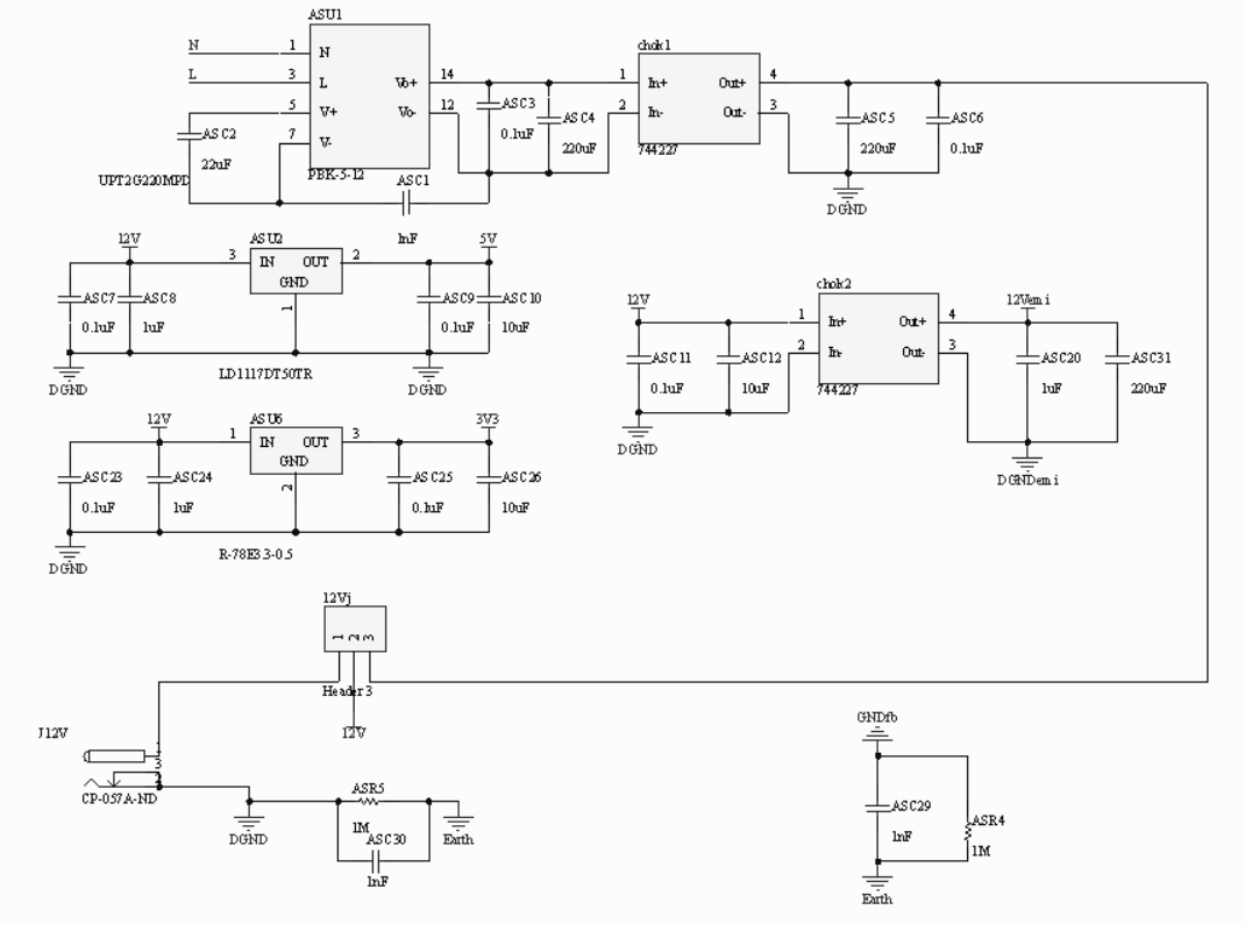
Transformer turn ratio a = 4:3.

Appendix D Flyback PFC Circuit Schematic

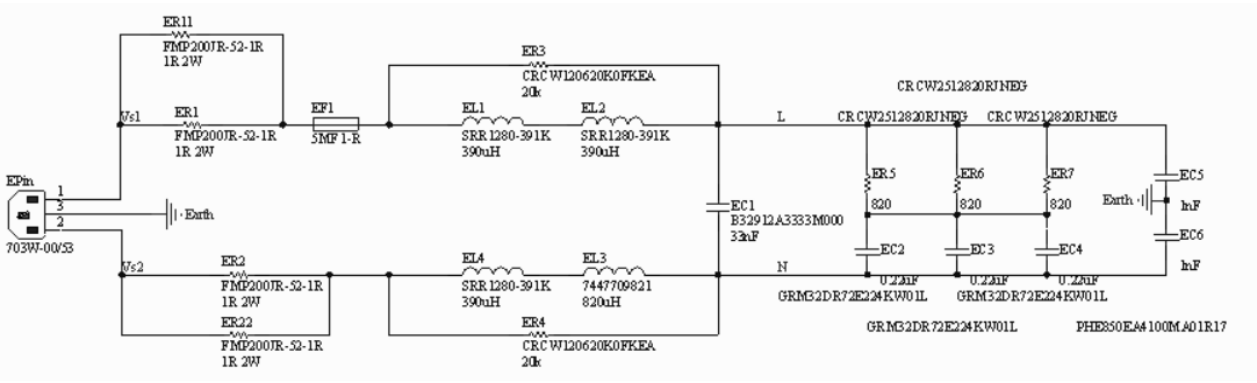
D.1 Altium Designer schematic of Flyback PFC circuit:



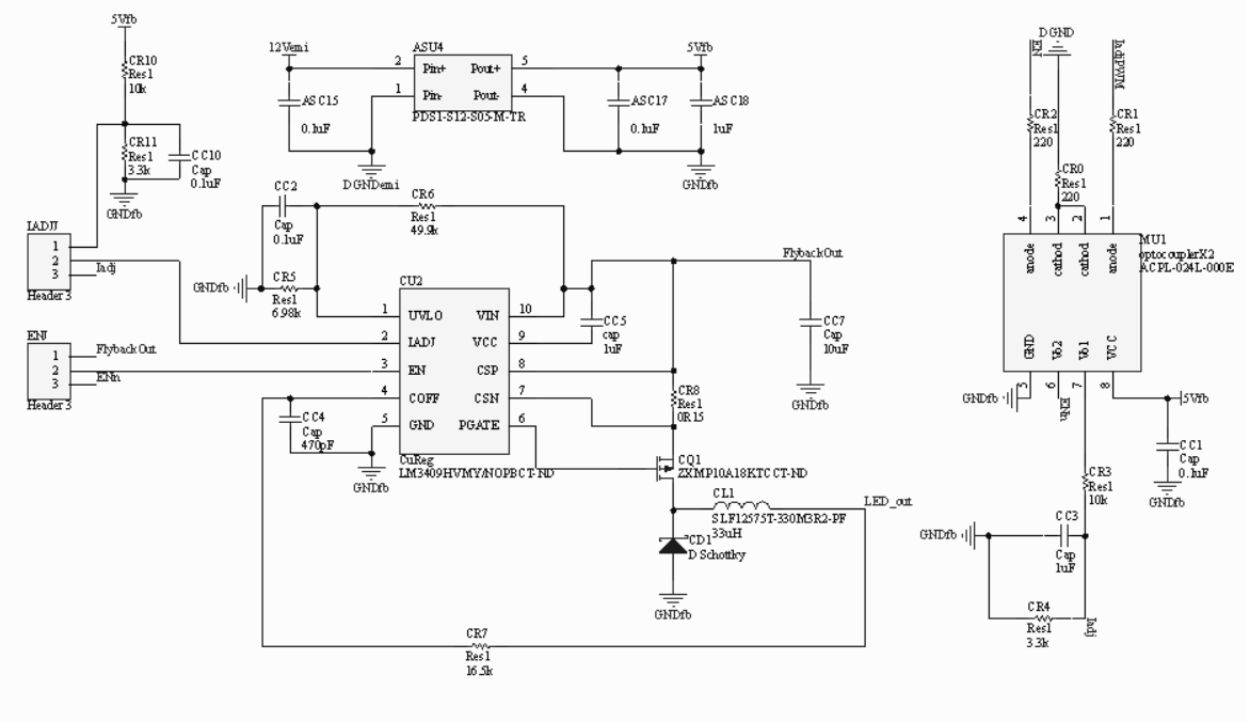
D.2 Altium Designer schematic of auxiliary power supply circuits:



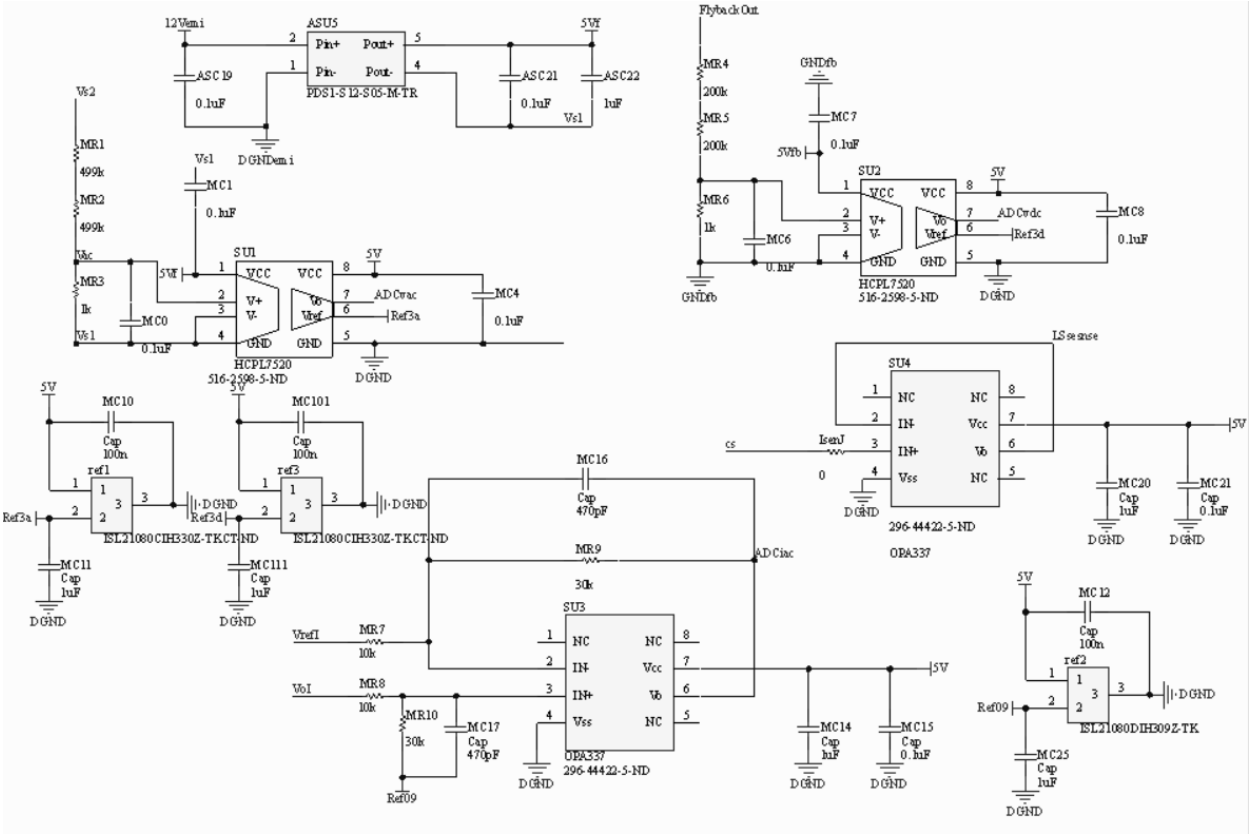
D.3 Altium Designer schematic of EMI filter circuits:



D.4 Altium Designer schematic of DC/DC current regulator circuits:



D.5 Altium Designer schematic of data acquisition circuits:



D.6 Altium Designer schematic of connector circuits: