# SYNCHRONOUS RECTIFICATION FOR LLC RESONANT CONVERTER IN BATTERY CHARGING APPLICATION

by

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**SYNCHRONOUS RECTIFICATION FOR LLC RESONANT CONVERTER IN BATTERY CHARGING APPLICATION**

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# Abstract

Everyday the number of devices with a battery inside is increasing. From smartphones to electric vehicles, batteries are widely used in different power ratings. Charging time is one of the major obstacles in widespread use of battery powered electric vehicles. Developing high power chargers is one of the key steps to achieve fast charging.

Developing high power chargers requires design of compact and high efficiency converters. LLC Resonant converter is widely used in the structure of medium to high power chargers. Utilizing synchronous rectification technique, along with the converter intrinsic soft switching characteristic, has led to above 95% efficiency for LLC resonant converter.

Due to presence of magnetizing inductance in the structure of resonant tank in LLC resonant converter, the secondary side currents are not completely synchronous with the primary side gate signals. This makes the control of secondary MOSFETs complicated.

Although synchronous rectification for LLC resonant converter has been the focus of research for at least a decade, most of the methods developed for synchronous rectification focus on fixed output voltage applications. However, in battery charging process, the output voltage of the converter varies in a wide range. As a result, new flexible synchronous rectification methods are needed to work in different operating points during the charging process.

In this research, the requirements for LLC resonant converter in battery charging application are investigated. Based on these requirements, an LLC converter with 24V rated output voltage and maximum 650W output power is designed. Next, the control requirements for LLC resonant converter in battery charging application are explained. Additionally, the settings for an analog integrated circuit from Infineon Technologies are modified to meet the requirement for battery charging application. At the end, experimental results are presented to show the effectiveness of the control settings in different operating conditions.

# Preface

This thesis is an unpublished, original work by Peyman Amiri, who has been responsible for literature review, theoretical analysis, design and experimental results. This research has been supervised by Dr. Liwei Wang. Additionally, the author has received technical guidance from Mr. Marian Craciun, Mr. Dan O' Leary and Mr. Chris Botting from Delta-Q Technologies.

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# List of Abbreviations

| | |
|---|---|
| BM | Burst Mode |
| CCM | Continuous Conduction Mode |
| CPU | Central Processing Unit |
| CT | Current Transformer |
| DC | Direct Current |
| EV | Electric Vehicle |
| FFVOT | Fixed Frequency variable On Time |
| FHA | First Harmonic Approximation |
| IC | Integrated Circuit |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| PCB | Printed Circuit Board |
| PDM | Pulse Density Modulation |
| PFC | Power Factor Correction |
| PHEV | Plug in Hybrid Electric Vehicle |
| PLL | Phase Locked Loop |
| PRC | Parallel Resonant Converter |

| | |
|---|---|
| PWM | Pulse Width Modulation |
| RMS | Root Mean Square |
| SOC | State of Charge |
| SR | Synchronous Rectification |
| SRC | Series Resonant Converter |
| SSOC | Self Sustained Oscillation Control |
| VCOC | Voltage Controlled Oscillation Control |
| VFFOT | Variable Frequency Fixed On Time |
| ZCS | Zero Current Switching |
| ZVS | Zero Voltage Switching |

# List of Symbols

| | |
|---|---|
| $C_{in}$ | Input Capacitor |
| $C_o$ | Output Capacitor |
| $C_{oss\ (eff,tr)}$ | Time Related Effective MOSFET Drain to Source Capacitance |
| $C_r$ | Resonant Capacitor |
| $f_s$ | Switching Frequency |
| $f_{s\ (min)}$ | Minimum Switching Frequency |
| $f_{s\ (max)}$ | Maximum Switching Frequency |
| $G_{dc\ (min)}$ | Minimum DC Gain |
| $I_d$ | Drain Current |
| $I_{sr}$ | Synchronous Rectification Current |
| $L_m$ | Magnetizing Inductance |
| $L_o$ | Output Inductor |
| $L_r$ | Resonant Inductor |
| n | Transformer Turns Ratio |
| $N_p$ | Transformer Primary Side Number of Turns |
| $N_s$ | Transformer Secondary Side Number of Turns |

| | |
|---|---|
| $P_o$ | Output Power |
| Q | Quality Factor |
| $Q_{min}$ | Minimum Quality Factor |
| $R_{ac}$ | Equivalent AC Resistor |
| $R_{ac\ (max)}$ | Maximum Equivalent AC Resistor |
| $R_o$ | Load Resistor |
| T | Switching Period |
| $t_d$ | Dead Time |
| $V_{ds}$ | Drain to Source Voltage |
| $V_F$ | Diode Forward Voltage Drop |
| $V_{in}$ | Input Voltage |
| $V_{in\ (max)}$ | Maximum Input Voltage |
| $V_{in\ (min)}$ | Minimum Input Voltage |
| $V_{in\ (nom)}$ | Rated Input Voltage |
| $V_o$ | Output Voltage |
| $V_{o\ (max)}$ | Maximum Output Voltage |
| $V_{o\ (min)}$ | Minimum Output Voltage |

| | |
|---|---|
| $V_{o\ (nom)}$ | Rated Output Voltage |
| $W_{s\ (max)}$ | Maximum Switching Angular Speed |
| $Z_o$ | Characteristic Impedance |

# Acknowledgement

First, I would like to express my sincere gratitude and appreciation to my supervisor, Dr. Liwei Wang, for his endless support and technical guidance. I will be always inspired by his hard work and professional dedication.

Additionally, I am very much obliged for the technical support of my research committee member, Dr. Wilson Eberle, without whom this research would not be possible. I am also grateful for remote and on-site technical support from Chris Botting, Marian Craciun and Dan O'Leary at Delta-Q Technologies.

Last but not the least, I will be forever thankful to my parents, Mohammad and Zohreh, for their limitless support from thousands miles away.

# Dedication

*To Niloofar for her love and support.*

# Chapter 1 Introduction

## 1.1. Background

Electric Vehicles (EVs) and Plug-in Hybrid Electric Vehicles (PHEVs) have recently attracted significant attention in automobile industry [1]. Low carbon footprint and minimum environmental effects, make these vehicles a favorable candidate for the future of transportation.

Rapid charging and long-range performance is one of the main challenges for potential manufacturers of electric vehicles. This motivates experts in power electronics to aim for developing high efficiency and high power density chargers.

Increasing the efficiency of power converters requires the understanding of semiconductor physics and the precise modeling of these semiconductor devices used in switching converters. This will help us improve the energy efficiency of power converters.

## 1.2. Energy Dissipation in MOSFETs[1]

MOSFETs are of the most important building blocks in high efficiency and high frequency power electronic applications [2]. MOSFETs are used either in their on state or off state for shaping the voltage and/or current waveforms. Figure 1.1 shows the symbol of an n-channel MOSFET. An ideal MOSFET has zero on state resistance and infinite off

[1] Metal Oxide Semiconductor Field Effect Transistor

state resistance. In addition, the transition between the on state and off state should ideally happen instantly. Furthermore, for an ideal MOSFET, there is no limitation on the switching frequency, current conduction and reverse blocking voltage capability.

However, manufacturing limitations and parasitic elements limit the boundaries of operation for MOSFETs. Due to the presence of parasitic elements and junction capacitances, the turn on and turn off transition of MOSFETs do not happen instantly. The transition during turn on and turn off in a MOSFET is depicted in Figure 1.2 in an exaggerated way.

Figure 1.2 shows that during turn on and turn off in a MOSFET, both current and voltage of the switch have non-zero values for a short period. This transition results in switching loss in the MOSFET. In addition to switching loss, non-zero resistance of the MOSFET in the on state will result in conduction loss. Nowadays, power MOSFETs with on state resistance of a few milliohms are widely available, which results in extremely low conduction loss. As a result, switching loss is the dominant factor in overall energy efficiency in a conventional switching converter.

In order to decrease the weight and volume of magnetic parts in power electronic converters, high switching frequency is favorable in high power applications. With the switching frequency increase, the switching transitions happen more often and the average power dissipation can go beyond the heat sink capability of the MOSFET package and the conventional thermal management techniques. This increases the risk of MOSFET thermal runaway and system failure [3].

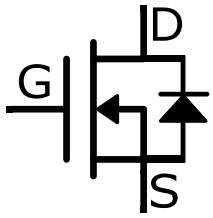



Figure 1.1 - MOSFET symbol

Zero voltage switching (ZVS) and zero current switching (ZCS), are the techniques used to reduce the switching loss in a MOSFET. ZVS can happen during turn-on of a MOSFET. In this method, the drain to source voltage of the MOSFET should have a value close to zero right before the turn-on process to avoid the simultaneous transition of large voltage and current in the MOSFET. On the other hand, ZCS can happen during turn-off. In this technique, the current through the MOSFET becomes zero right before the transition.

Converters with ZVS and/or ZCS are called soft switching converters. In contrast to conventional hard-switching converters such as the boost converter, soft switching converters such as resonant converters can operate with higher switching frequencies in range of a few hundred kilohertz [3].

## 1.3. Battery Charger Technology

The output current of the battery charger changes significantly from the rated value at the beginning to almost zero at the end of the charging process. The output voltage of a battery charger also needs to vary in a wide range from nearly zero for depleted batteries to the rated value when the batteries are fully charged. As a result, the converter used in a

charger, should be flexible enough to operate in a very wide range of operating points with high efficiency.

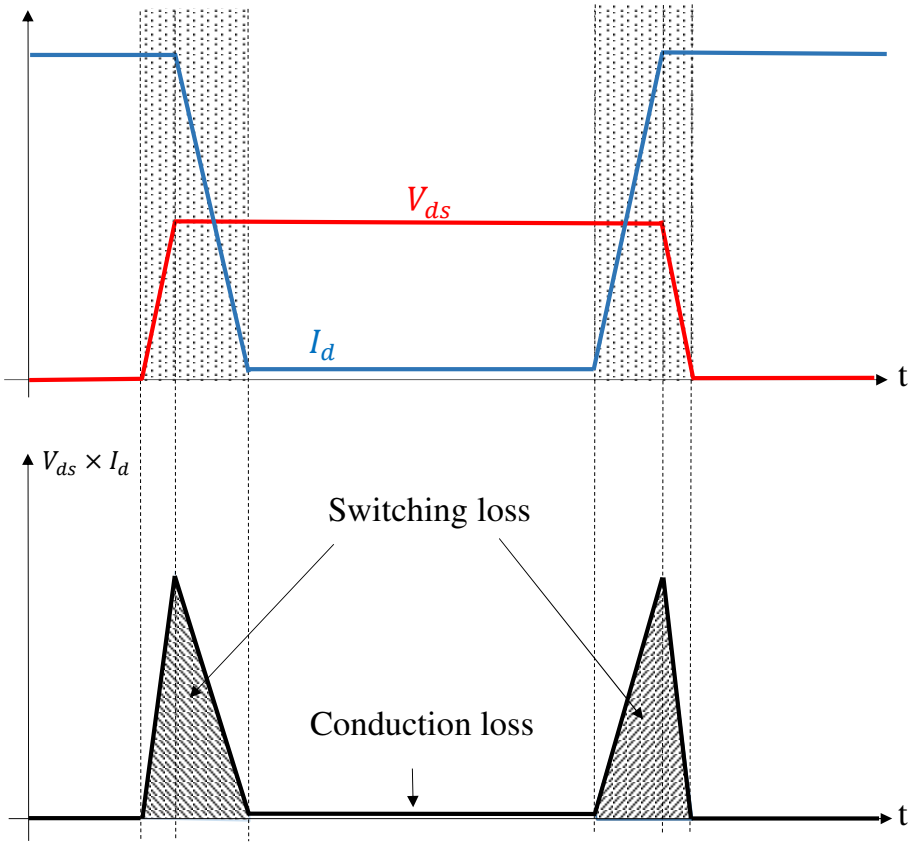



Figure 1.2 - Energy dissipation during turn on and turn off transition in a MOSFET [2]

A two-stage smart converter shown in figure 1.3 is a widely accepted concept in battery charging technology. In this topology, in order to regulate the input current, a rectifier is followed by a power factor correction (PFC) boost converter. The boost converter operates in continuous conduction mode (CCM) [4].

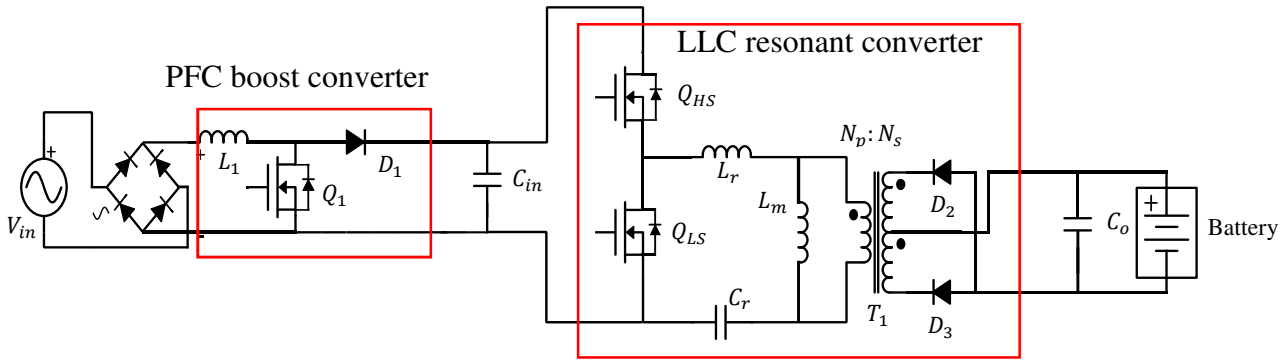



Figure 1.3 - A two-stage smart battery charger structure [4]

The DC front-end technology in chargers is a converter called LLC resonant converter. This converter is used to regulate the output voltage and current. The LLC resonant converter is composed of a square wave generator and a resonant tank made of two inductors (LL) and one capacitor (C). A high frequency transformer, which is cascaded with a rectifier stage, connects the converter to the battery.

This converter is able to have ZVS turn on for the primary side switches in different loading conditions and input voltage levels. Additionally, it can provides low current turn off and ZCS turn off for primary and secondary side switches, respectively. This significantly reduces the switching loss compared to conventional pulse width modulation (PWM) converters. However, the amplitude of current in the secondary side switches is so high that makes the conduction loss the dominant factor to achieve high efficiency.

## 1.4. Synchronous Rectification in LLC Resonant Converters for Battery Charging Application

Using MOSFETs with lower on-state voltage drop compared to power diodes in the rectifier stage in LLC resonant converter, is promising to solve the high conduction loss

problem in the converter. This technique, which is called Synchronous Rectification (SR), is widely used in conventional PWM converter.

However, due to the presence of magnetizing current, the secondary side current is not completely synchronous with the primary side gate signals. As a result finding the right moments to turn on and turn off the secondary side MOSFETs is complicated. The requirement of wide output voltage and current in battery charging application adds to the complexity of the secondary side control of LLC resonant converter in this application.

This research is focused on finding new ways of synchronous rectification control that are flexible enough to have a safe performance in wide operating range of chargers.

## 1.5. Thesis Outline

This thesis includes five chapters. The first chapter explained the motivation for the research and the technical background of the topic. It gives an insight on energy dissipation principals in power electronic converters. Additionally, it explains the reason for the use of resonant converters, briefly.

Chapter 2 explains the operation of resonant converters and specifically LLC resonant converters in detail. The chapter presents recently proposed control methods for the primary side MOSFETs in LLC resonant converters, as well as synchronous rectification methods.

Chapter 3 investigates the requirement of an LLC resonant converter to be used in battery chargers. In this chapter, complete design process of a 650W LLC resonant

converter with 24V rated output voltage is explained. Additionally, the main features of ICE2HS01G controller are briefly explained. This controller is designed by Infineon Technologies for LLC resonant converter with synchronous rectification. Based on the requirement of the LLC resonant converter and features of ICE2HS01G, control settings suitable for wide operating range of the LLC converter are proposed in this chapter.

Chapter 4 includes the stress calculation and part selection for the experimental prototype. Additionally, technical design considerations are briefly mentioned in this chapter. Finally, experimental waveforms from the primary and secondary side of the converter are presented. Furthermore, the efficiency results of the converter in body diode conduction and synchronous rectification mode are compared. The result show a significant improvement in efficiency in most of the operating points.

Based on the experimental result, the overall performance of ICE2HS01G controller with improved control setting for battery charging application is evaluated in the final chapter. Additionally, possible future works, which facilitates further improvement in efficiency of chargers, are explained.

# Chapter 2 Literature Review

## 2.1. Overview

In the following sections, we will focus on resonant converters and specifically LLC resonant converter's principle of operation, modeling techniques and the recently proposed control strategies. At the end, the previously reported analog and digital control techniques applied to synchronous rectification in LLC resonant converter are presented.

## 2.2. Resonant Converters

Resonant converts are used to reduce the switching loss in electric power converters. They take advantage of oscillations in the resonant tank to turn the switches on or off when the voltage or current is zero [3]. Resonant DC-DC converters are composed of a square wave generator circuit, followed by a resonant tank and cascaded with a rectifier stage. The rectifier stage is interfaced with the resonant tank through a high frequency transformer to provide isolation and step-up or step-down characteristic. Based on the square wave generator structure, resonant converters are categorized into the following two groups.

- Half-Bridge
- Full-Bridge

These converters can also be grouped based on the structure of the rectifier stage.

- Center tapped half wave
- Full wave

- Voltage doubler

Most importantly, resonant DC-DC converters are categorized into the following three groups based on the structure of the resonant tank:

- Series resonant DC-DC converters
- Parallel resonant DC-DC converters
- Series-parallel resonant DC-DC converters

### 2.2.1. Series Resonant Converters

A series resonant DC-DC converter is depicted in figure 2.1. In this type, the combination of the two $\frac{C_s}{2}$ capacitors forms the series resonant capacitor. These capacitors also split the DC side voltage equally. The series capacitance also acts as a DC blocker in the case of unbalanced switching and protects the transformer from saturation.

The current in the resonant tank decreases in light load condition and the converter has a relatively good partial load efficiency. Furthermore, the converter is able to handle short circuit current by increasing the switching frequency. However, the output voltage cannot be regulated at no load condition in this configuration type. The output capacitive filter should be able to withstand high level of current ripple. As a result, this topology is suitable for high voltage low current applications [3], [5] .

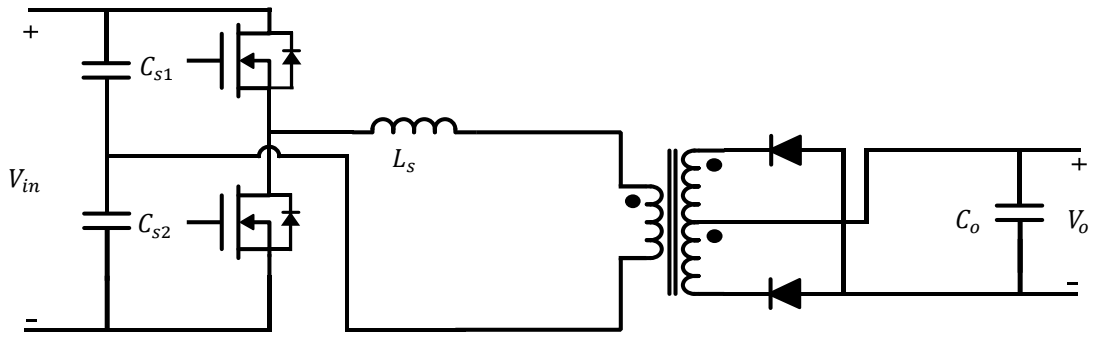



Figure 2.1 - Series resonant converter [5]

### 2.2.2. Parallel Resonant Converters

In a parallel resonant converter, shown in figure 2.2, the two capacitors $\frac{C_{in}}{2}$ are only used to split the DC side voltage equally. In this topology, the output voltage regulation at no load can be achieved. Additionally, there is no need for a filter at the output to be able to withstand a high level of current ripple. In this topology, the circulating current is independent from the load, which results in low light load efficiency [3], [5] .

### 2.2.3. Series-Parallel Resonant Converters

In a series-parallel resonant converter, shown in figure 2.3, series and parallel resonant converters are combined. In contrast to parallel resonant converter, $C_{s1}$ and $C_{s2}$ participate in resonance and form a multi-resonant structure. This results in good partial load efficiency and voltage regulation at light loading conditions [3], [5].

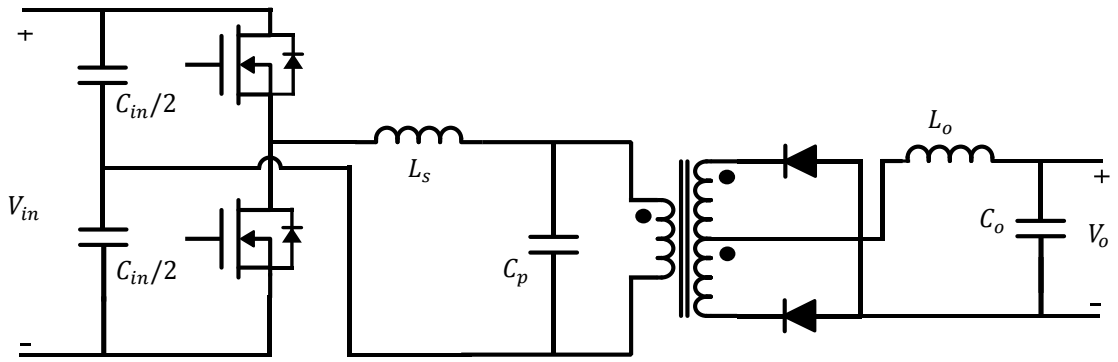



Figure 2.2 - Parallel resonant converter [5]

In the topology shown in figure 2.3, it is desired to operate the system above resonant frequency. In this condition, ZVS turn on of the primary side switches is assured. Although turn off loss will not be eliminated, it can be reduced significantly by utilizing a lossless capacitive snubber across the MOSFETs. The stored energy in the capacitors of the snubber will go back to the DC power source, when the opposite side MOSFET turns off. Additionally, the topology allows the optimization of the magnetic parts based on the minimum switching frequency [7].

## 2.3. LLC Resonant Converters

LLC resonant converter is a special kind of series parallel resonant converter. In this converter, the output is regulated over a wide range of line voltage and load variations with a small deviation in switching frequency. Moreover, ZVS turn on and low current turn off capability of the converter can be maintained for the most of operating points. Additionally, magnetic parts can be integrated into a high frequency transformer. Low voltage stress and ZCS turn off for secondary side diodes are also available [6], [7].

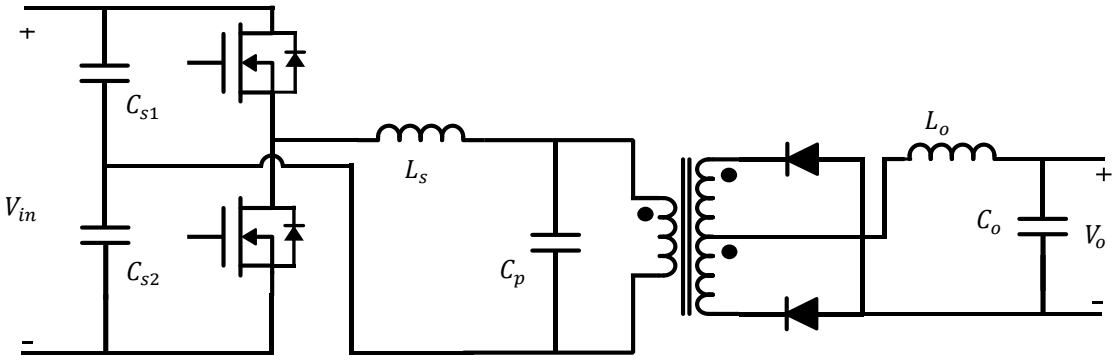



Figure 2.3 - Series-parallel resonant converter [5]

## 2.3.1. Analysis of Operation

LLC resonant converter, shown in figure 2.4, is a variation of the series-parallel resonant converter. As a result, the converter demonstrate multi resonance operation.

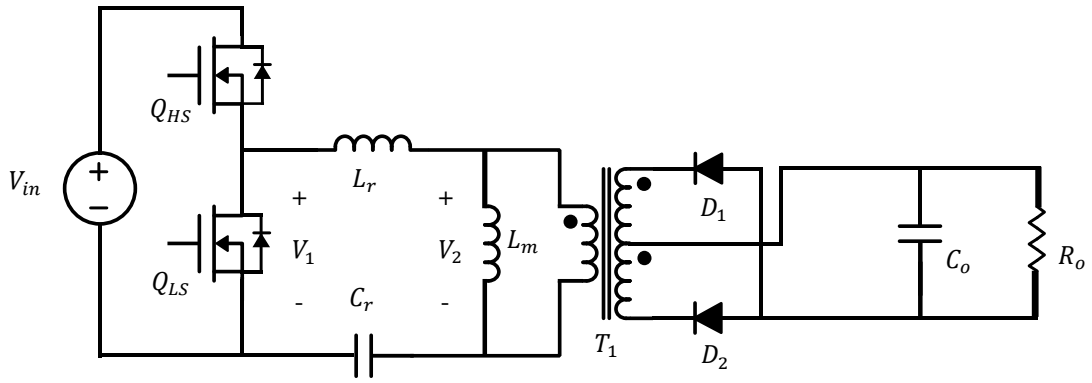



Figure 2.4 - LLC resonant converter [6]

The two resonant frequencies are defined in (2.1) and (2.2).

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.1}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m) C_r}} \tag{2.2}$$

$L_r$, $L_m$ and $C_r$ represent the series inductance, parallel inductance and the series capacitance, respectively. The load factor is defined as:

$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{\frac{8n^2}{\pi^2} R_o} \tag{2.3}$$

$R_o$ and n are the load resistance and the primary to secondary ratio of the HF transformer, respectively. Using first harmonic approximation (FHA), we can determine the gain of the converter ($V_2/V_1$) in different frequencies and in different loading conditions as in figure 2.5.

As the load becomes lighter (Q decreases), the peak of the gain curve moves toward the resonant frequency $f_{r2}$. On the other hand, in heavy load condition, the peak happens close to the resonant frequency $f_{r1}$. For heavy loadings, the characteristic of the converter is similar to a series resonant converter (SRC). Whereas, in light loading condition, the characteristic of the converter is close to a parallel resonant converter (PRC).

In the points to the right of the dashed line, the primary MOSFETs take advantage of ZVS during turn on. On the other hand, ZCS is available for primary MOSFETs in the points to the left of the dashed line. Different regions can be considered for the operation of LLC resonant converter, as specified in figure 2.5 and discussed below.

- **Region 1 (Single Resonance Operation)**:

The switching frequency is above $f_{r1}$ and the magnetizing inductance does not participate in resonance. In this region, ZVS is assured.

- **Region 2 (Multi Resonance Operation)**:

The switching frequency is between $f_{r1}$ and $f_{r2}$. The ZVS or ZCS operation of the primary MOSFETs depends on the loading condition. $L_r$ and $C_r$ are chosen in a way to maintain ZVS at heavy loadings. The choice of $L_m$ determines the turn off current of the primary MOSFETs. With a small $L_m$, we benefit from a limited switching frequency range. However, the turn off current will be high.

- **Region 3 (Overload region)**:

The switching frequency is below $f_{r2}$. The primary MOSFETs work in ZCS mode. In this condition, the design of filters is based on the lowest switching frequency and cannot be optimized.

The authors in [8] investigate the effect of transformer secondary side leakage inductance on the converter gain characteristic. They believe that neglecting this inductance can result in confusion in determining $f_{r1}$. They offer a simple design procedure that takes into account the effect of the transformer secondary side leakage inductance in designing the converter.

The effect of parasitic junction capacitance of the rectifier diodes on the regulation of output voltage at very light loadings is investigated in [7]. Using FHA, the authors propose to limit the switching frequency in order to avoid unregulated output voltage at light loading condition.

The authors of [9] use the time domain analysis to determine the reason for unregulated output voltage at light load condition. They find that adding to the parasitic junction capacitance of the primary MOSFETs is a good way to enhance the regulation of output voltage at light loading condition. However, this approach may lead to loss of ZVS primary MOSFETs if designed improperly.

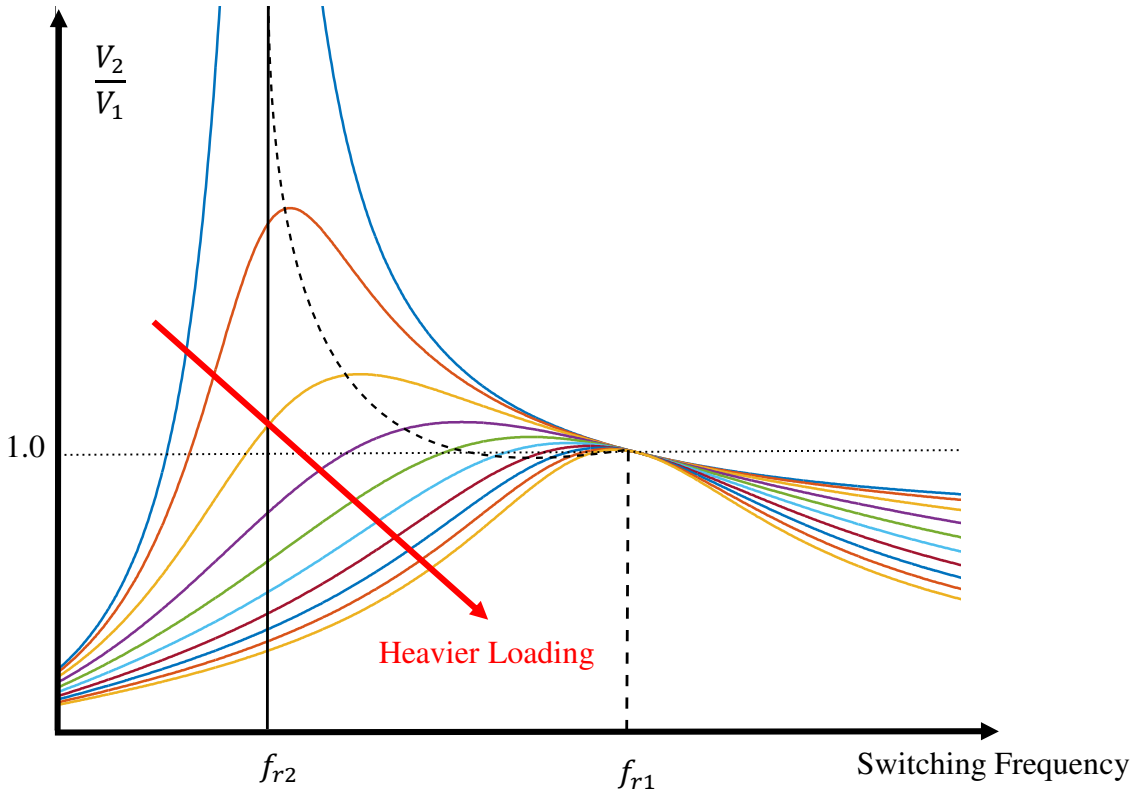



Figure 2.5 - LLC converter gain characteristic [6]

## 2.3.2. Control Strategies

Different control strategies for LLC resonant converters are categorized below [10].

- **Variable frequency control**

**A. Voltage controlled oscillation control (VCOC):**

In this control scheme, the switching frequency of the square wave generator is changed to compensate for line voltage and load variations. In this method, compensated output voltage error is fed to a voltage-controlled oscillator (VCO), which controls the square wave generator switching frequency.

**B. Self-sustained oscillation control (SSOC):**

In this method, the delay between zero crossing of the resonant tank current and the switching pulse of the chopper is tuned to regulate the output voltage. Usually at full load, the delay is set to the minimum value, which results in operation close to the resonant frequency $f_{r1}$. In this scheme, the ZVS is assured for the whole load range. However, sensing the resonant current requires an expensive and bulky sensing equipment, which increases the conduction loss in the resonant tank.

- **Fixed frequency control**

**A. Asymmetric pulse width modulation (PWM) control:**

In this method, the switching frequency is kept constant and the output is regulated by changing the on time of the switches. In this scheme, the compensated output voltage error is compared with a saw tooth waveform to generate pulses with a variable duty cycle. In this method, the magnetic parts can be designed in an optimum manner. However, the current waveform will be distorted.

### B. Pulse density modulation (PDM) control

This method, which is also called burst mode control, tunes the period in which the gate pulses of the square wave generator are active. In this way, the efficiency can be improved in the light load conditions. However, transition between the burst time and the blocked time causes a number of hard switchings in the converter.

### C. Secondary side control:

In this method, Full wave rectification is needed in the secondary side and diodes are replaced with MOSFETs. The square wave generator is ran at the resonance frequency with 50% duty cycle. The output voltage is regulated by changing the on time of the secondary side switches. In this way, the switching loss will be decreased both at the primary and secondary sides.

A number of new control schemes have been recently proposed. A Combination of control schemes is presented in [11] to control LLC Resonant based DC-DC converter suitable for battery charging application. This control strategy takes advantage of fixed frequency variable on time (FFVOT), variable frequency fixed on time (VFFOT) and continuous conduction control approach. This control approach addresses all the issues with battery chargers of this type.

A novel burst mode control is proposed in [12] for LLC resonant converters. In this scheme, the burst time remains constant and the turn off time is modulated to regulate the output. The switching pattern is also optimized to reduce the switching loss.

A dual closed-loop control for LLC resonant converters is proposed in [13]. This control strategy controls both the full bridge square wave generator and the PFC converter. The method uses variable frequency control for the square wave generator.

The authors of [14] propose a nonlinear model for LLC resonant converters, based on which an observer-based controller is designed. This model is derived through combining frequency domain and time domain analysis.

A phase locked loop (PLL) based closed-loop control is presented in [15] to transfer the maximum power from LLC converter to the battery.

Researchers in [16], propose a practical bang-bang charge control (BBCC) for LLC resonant converters. In this method, the input charge to the series capacitor in the resonant tank is monitored. By defining two boundaries for the voltage of the series capacitor, they can model the LLC converter as a first order system and handle different transients with a simple control design.

### 2.3.3. Synchronous Rectification

In high current application, the conduction loss in the secondary side diodes is so high that virtually eliminates the most valuable characteristic of resonant converters, which is low loss. Synchronous Rectification (SR) is used to reduce the conduction loss of the rectifier stage. Figure 2.6 shows a LLC resonant converter with synchronous rectification.

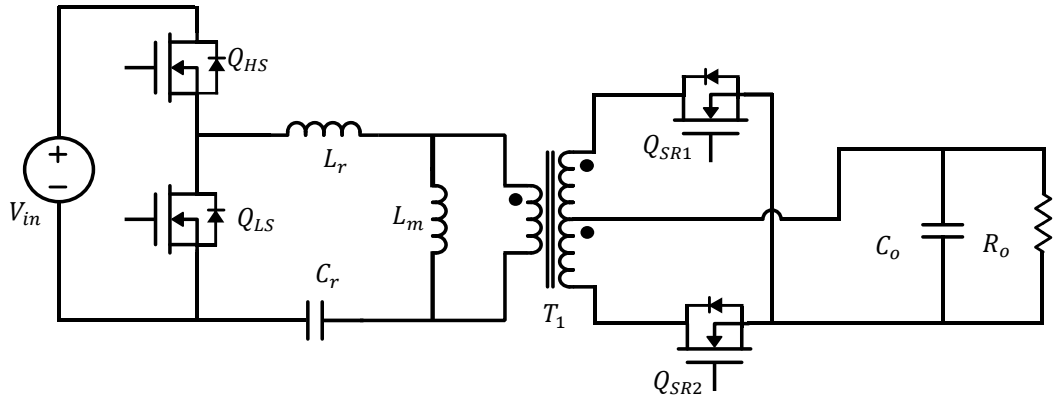



Figure 2.6 - LLC resonant converter with synchronous rectification [6]

In contrast to the SR implemented in conventional PWM converters, implementing SR in LLC resonant converters is rather challenging. This is because of the asynchronous switching times of the primary and secondary side MOSFETs, caused by the magnetizing current effect.

A SR scheme based on sensing the secondary side current is presented in [17]. Although this is a precise method, sensing the high amplitude secondary side current leads to an increase in conduction loss in the current transformer (CT). This can cancel a portion or the whole advantage achieved with synchronous rectification

In order to decrease the conduction loss in the CT, sensing the transformer primary side current is recommended in [18]. However, this will require the use of separate magnetic components for the resonant tank that increases the size and cost of the converter.

Synchronous rectification method based on sensing the resonant tank current is explained in [19], which eliminates the need for using separate magnetic parts. However, this method requires the use of a complicated auxiliary circuit.

The researchers in [20] propose a SR driving scheme based on the fact that the product of the output voltage and duty cycle of secondary MOSFETs always remain constant at a fixed switching frequency. Thus, by sensing the output voltage and knowing the frequency they can control the switching times of the secondary side switch properly. This control method is used along with switching frequency control of the LLC resonant converter to regulate the output voltage.

The manufacturing process of power MOSFET results in presence of an antiparallel body diode. In case of late turn on or early turn off for the SR MOSFET, the body diode conduction occurs. A number of methods propose synchronous rectification method based on sensing the drain to source voltage of the secondary side power MOSFETs. In these methods, the moment when the voltage drop across drain to source goes below the body diode conduction threshold, the MOSFET will be turned on. Then, when the current decreases in the MOSFET, the resistive voltage drop on the MOSFET will become close to zero. By defining another voltage threshold, the MOSFET can be turned off at the right moment.

SR methods based on sensing drain to source voltage of the MOSFET have three major issues. As shown in figure 2.7, MOSFETs demonstrate an inductive effect caused by the geometry of drain and source leads. This effect is modeled as a lumped inductor at the drain. Because of the MOSFET stray inductance, the sensed $V_{d's}$ voltage leads the actual voltage across drain to source of the MOSFET i.e. $V_{ds}$. Figure 2.8 shows the sensed drain to source voltage of a MOSFET with and without a 5nH stray inductance. In this

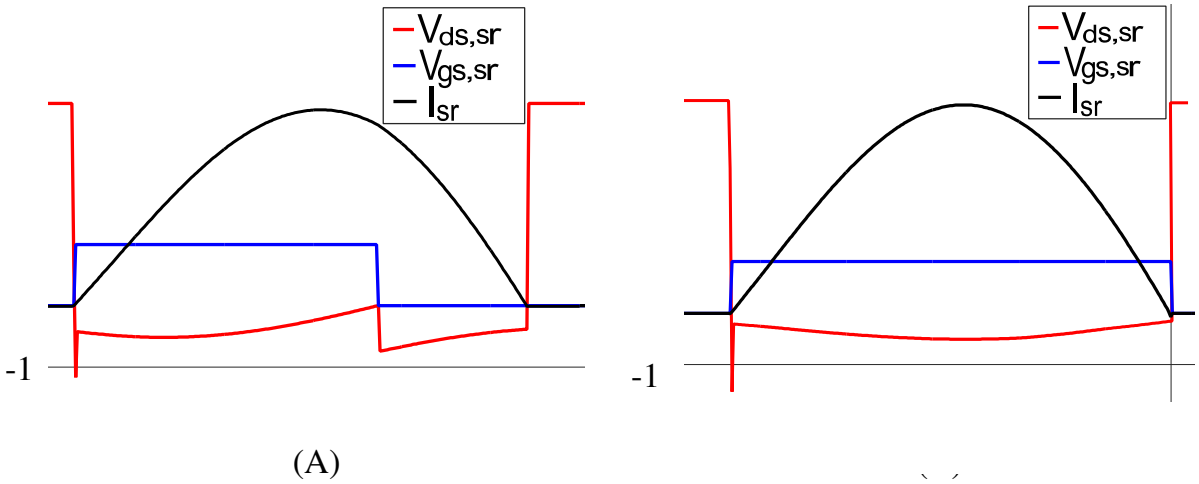
simulation figure, the switching frequency and MOSFET on state resistance are set to 200 kHz and 2.5 mΩ, respectively. In figure 2.8 the MOSFET will be turned off early because of stray inductance.


(A) (B)

Figure 2.7 - (A) Modeling of MOSFET with stray inductance (B) ON state equivalent circuit for a MOSFET with stray inductance

Additionally, when both MOSFETs are turned off, the leakage inductance of the transformer and the junction capacitance of the MOSFETs experience resonance. As a result, the voltage across the junction capacitance has high frequency ringing and if the peak of the ringing reaches the threshold level for turning the MOSFET on, the MOSFET will experience a false turn on. This will cause reverse current following to the transformer and decreases the efficiency.

The third issue with this method is the turn on and turn off voltage threshold for MOSFET that are in order of millivolts. These voltage levels are difficult to be sensed by most of analog and some digital devices.




(A)

Figure 2.8 - (A) Drain to source voltage in presence of stray inductance (B) Drain to source voltage without stray inductance

Authors in [21] propose to add an active low pass filter to compensate for early turn off problem associated with drain to source voltage sensing synchronous rectification method. The circuit shown in figure 2.9 is proposed in this paper.

In this method, when the MOSFET is turned off, $S_a$ is open and $S_b$ is closed. In this condition, the voltage across $C_{cs}$ is kept at zero, the body diode conduction can be sensed and the MOSFET will be turned on immediately. At this moment, $S_a$ will be closed and $S_b$ will be opened. In this way, by tuning the RC filter, it can compensate for the lead effect of stray inductance and prevent early turn off. After the switch is turned off, the signal switches will be returned to their initial condition to be ready for next cycle.

Using this method requires information of the value for stray inductance and on state resistance. However, the equivalent stray inductance value can be different for every

single MOSFET and it is dependent on the design of printed circuit board (PCB) as well. On state resistance also varies widely with the junction temperature. Additionally, this method requires the use of two active switches that reduces the reliability of the circuit.

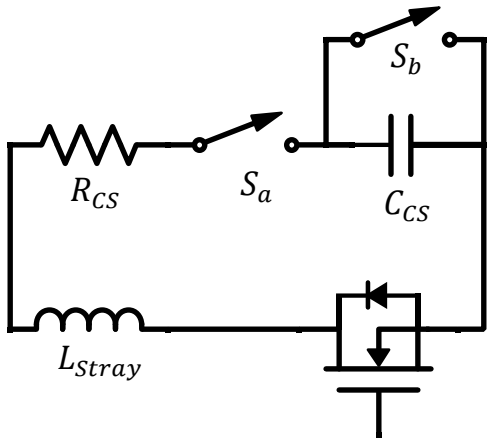



Figure 2.9 - Synchronous rectification using active filter method in [21]

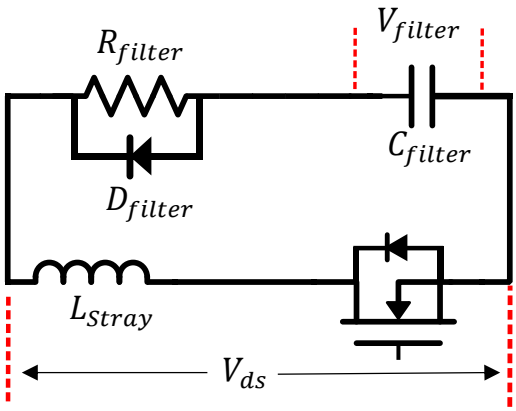



Figure 2.10 - Synchronous rectification based on zero-crossing noise filter [22]

Researchers in [22] offer a similar method by proposing the circuit in figure 2.10 . This method is able to not only remove the early turn off effect, but also filters the high frequency ringing that causes the false turn on. In this circuit, the forward voltage drop of

the filter diode, $D_{filter}$, is a little larger than the forward voltage drop of the MOSFET body diode. Figure 2.11 shows the key operating waveforms of this circuit.

Before $t_0$, the two MOSFETs and the primary side switches are all turned off. $C_{filter}$is charged to double of the output voltage and $D_{filter}$ is reversely biased. When the high side primary switch is turned on at $t_0$, the circuit filters out the high frequency ringing on $V_{DS}$. From $t_0$ to $t_1$, the current in the secondary side starts to increase from zero. The body diode conducts and $-V_{bd}$, which is the forward voltage drop of the body diode, is applied across the MOSFET. $D_{filter}$ will be forward biased and $C_{filter}$will be discharged to $V_{fd} - V_{fb}$. $V_{fd}$ is the forward voltage drop of $D_{filter}$. From $t_1$ to $t_2$, $C_{filter}$ will be discharged through $R_{filter}$. When the voltage of $C_{filter}$ reaches zero, the MOSFET will be turned on. During the discharge period of $C_{filter}$, the voltage across $C_{filter}$ is limited to $-V_{bd}$. From the moment the MOSFET is turned on, the circuit compensates for the leading effect of the stray inductance and the controller is able to turn the MOSFET off at the right moment.

Although the compensator works well for removing early turn off and only contains passive parts, it still suffers from lack of dependable information on value of equivalent stray inductance and on state resistance. Additionally, it introduces a delay in turn on because the capacitor needs to be discharged. This will be an issue especially in high frequency operation.

The drain to source voltage of the SR MOSFETs is utilized to detect the body diode conduction and to decide whether to increase or decrease the SR on time in [23]. In this method, a predefined on time is applied to the secondary MOSFET at first. Next, the control circuit will increase the on time of the SR if body diode conduction occurs at turn off of the MOSFET. Otherwise the control circuit decreases the on time. After a few switching cycles the circuit reaches an equilibrium point with optimum SR on time. However, the pulse width of the SR driving signal cannot be longer than the one for the primary side switch. As a result, this scheme will not be effective in all switching frequencies.

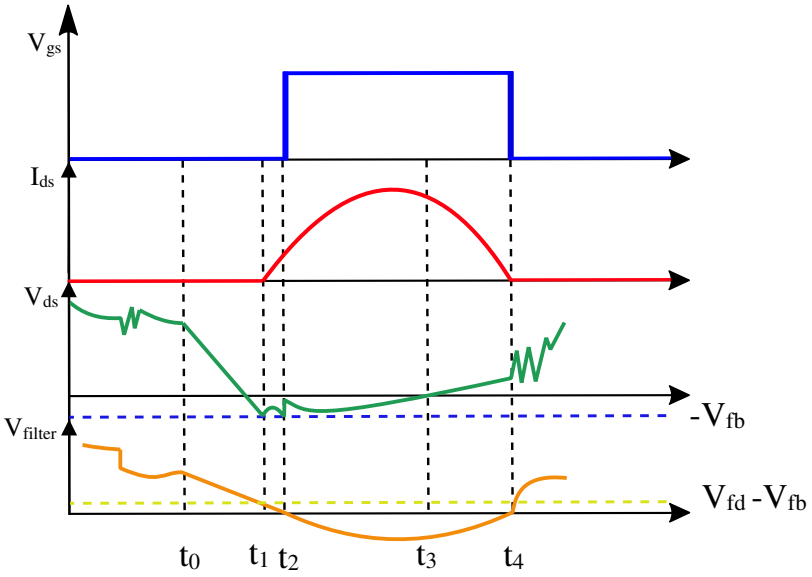



Figure 2.11 - Key waveform of synchronous rectification method using zero crossing noise filter [22]

By digital implementation of the control scheme in [23], [24] makes the scheme to be effective in a broader frequency range and simplifies the implementation of the control circuit.

Researchers in [25] have improved the method in [24] to be easily implemented in conventional digital controllers. In this method, in order to have the lowest possible computation resources usage, the body diode conduction is only activated in a window that starts before the turn-off of the related primary side switch and ends after that. The researcher states that by using a 100 MHz digital controller for a 150 kHz LLC converter, this method only uses 6.5% of the CPU computational resources.

This paper also investigates the performance of this method in very high frequency LLC converters. In order to have the lowest possible computation resources usage, this paper proposes counting the body diode conductions in a number of switching cycles and then decide to decrease or increase the conduction time of the MOSFETs. The researcher reports CPU usage reduction of 37% through updating the SR conduction duty cycle every 3 switching cycles.

The main problem with this method is that in case of a sudden frequency increase, the control method is not fast enough and the secondary switch will be turned off too late. This can result in a shoot through between primary and secondary side MSOFETs.

The authors in [26] have proposed an improved version of [24]. It keeps the record of the delay between rising edge of the primary side gate signal and the falling zero crossing of SR current. Moreover, the time delay between falling edge of the primary side gate signal and falling zero crossing of the SR current is recorded. Using these two signals, the shoot through problem of [24] in sharp frequency transitions is resolved.

The authors of [27] propose a digital controller for synchronous rectification, which stores the turn on delay and turn off delay of MOSFET switches in a look up table. By sensing the switching frequency and loading condition, the right turn on and turn off delays can be determined. It uses an efficiency scan block to determine the best turn on and turn off delay for the operation. This is a very simple SR driving scheme. However, the turn on and turn off delays are pulled out of simulations which is sensitive to the models used for simulation. Furthermore, updating the look up tables based on each individual product is a time consuming and inefficient manufacturing procedure. With the change of frequency the conduction time of the MOSFETs are initially set according to the highest allowed frequency. As a result, long settling time is needed for the SR controller with a small frequency drift.

## 2.4. Summary

In this chapter, the concept of LLC resonant converter, different modes of operation and control strategies were presented. In addition, recently proposed synchronous rectification techniques were discussed.

Analog solutions for synchronous rectification are generally simple. However, these methods are not very accurate and do not result in best performance for all of the operating conditions of a converter. A few modifications on the SR switches were reported that enhance the performance of analog methods. However, these modifications result in increased complexity and reduced dependability of the converter.

Compared to analog solutions, digital synchronous rectification techniques offer better flexibility and accuracy in controlling secondary side MOSFETs. The advanced methods, presented in this chapter, work well in steady state operation. However, using a digital controller adds to the complexity and manufacturing cost of battery chargers. Additionally, digital synchronous rectification methods may cause instability in transient operation of the converter.

Although synchronous rectification for switched mode power supplies has been widely discussed in the literature, less attention has been paid to finding synchronous rectification control scheme for wide output range applications such as battery charging. There is a need for finding synchronous rectification methods that can flexibly work in a wide range of switching frequency in below and above resonance frequency. Additionally these methods should be able to handle sharp frequency change caused by transient operation of the circuit. Furthermore, the implementation of this method should not result in significant increase of manufacturing cost.

In this thesis, we focus on the features of ICE2HS01G from Infineon Technologies that is designed for LLC resonant converter with synchronous rectification for fixed output voltage. Based on the specific requirements of the LLC resonant converter in battery charging application, we propose modifications in the control setting of this controller. In this way, the application of this controller can be expanded to wide output range applications. The method will introduce an affordable and quick solution for synchronous rectification in battery charging application.

# Chapter 3 Synchronous Rectification Solution for Battery Chargers

## 3.1. Overview

Although synchronous rectification for switched mode power supplies has been widely discussed in the literature, less attention has been paid to finding synchronous rectification control scheme for wide output voltage range applications such as battery charging.

In this chapter, the requirements for an LLC converter to operate in the DC front end for a battery charger is elaborated. In section 3.3, the complete process of designing parameters in LLC resonant converter for a 650W 24V charger is explained. Next, the features of ICE2HS01G resonant mode controller are briefly discussed. In section 3.6, the proposed modification in ICE2HS01 control settings are illustrated. These modifications expand the application of this controller to wide output voltage range LLC resonant converters such as battery chargers.

## 3.2. LLC Requirements for Battery Charging Application

In battery charging application, the output voltage of the charger changes significantly from one states of charge (SOC) to the other [4]. Figure 3.1 shows the different stages in charging of a pack of 24V lithium acid battery. It consists of four different operating conditions.

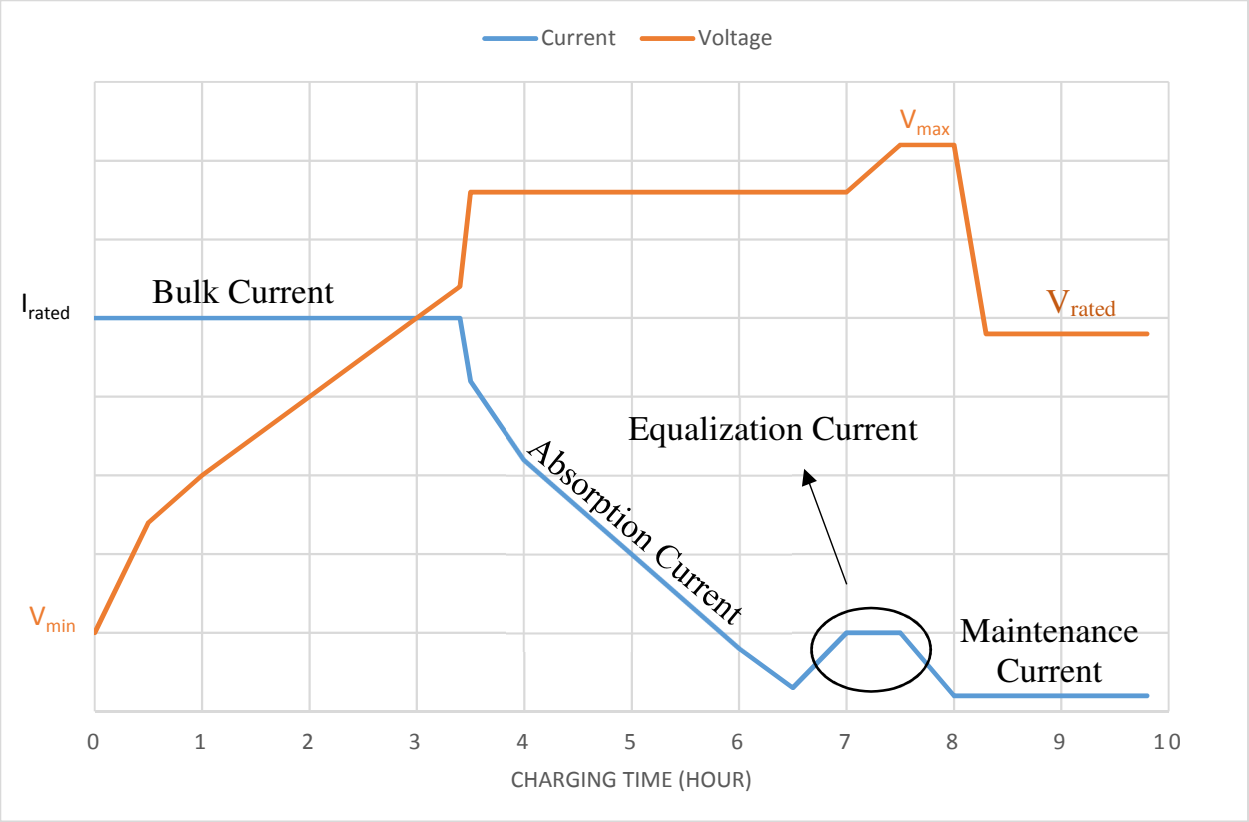



Figure 3.1 - Lithium-Acid battery charging characteristic [4]

In bulk mode, the charger provides the maximum current and closely monitors the voltage. The voltage of the battery pack is very low in this mode. Specifically in depleted batteries, the voltage across the terminal of the battery is close to zero at the very beginning of the charging process [4].

In the absorption mode, the battery voltage is increased up to a little below gassing voltage, after which the battery reaches 100% SOC [4]. In the equalization mode, the current is used to equalize the voltage on different battery cells. In this mode, the output voltage can increase up to 50% above the rated value.

In the maintenance mode, the current is only used to compensate for internal self-discharging and keep the voltage constant [4]. In this last part, the voltage is fixed at rated value and output current of the charger is very small.

In figure 3.1, the output of the battery charger needs to range from nearly zero to 50% above the rated voltage value. Additionally, the current also varies from the rated amount at the beginning of charging process to nearly zero at the end of charging. The wide operating range of chargers requires the switching frequency of LLC converter to vary from below resonance frequencies to frequencies well above the resonant point. Working in a wide switching frequency range, makes the design and control of primary and secondary switches complex.

## 3.3. Prototype Design

Designing a control mechanism for LLC resonant converter with synchronous rectification will be possible only by knowing the exact parameters of the converter. This section explains the design procedure for a 650W, 24V battery charger. The converter shown in figure 3.2 will be designed in a way to support 18-volt to 36-volt output in continuous working mode. In battery charging application, the input of the LLC resonant converter is connected to the output of a power factor correction (PFC) unit, with a double line frequency oscillation in the voltage. As a result, input voltage of the LLC converter has a typical value of 390V and it varies between 370V and 410V [4]. Based on battery charging application requirements, we consider the output voltage to vary up to 36V with

a rated value of 24V. With the specified power rating, the maximum output current will be 27.1A.

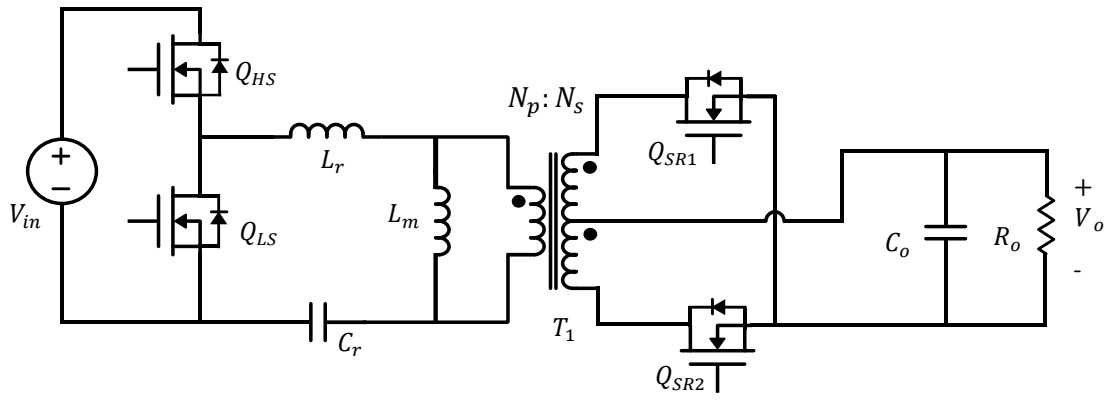



Figure 3.2 - Structure of prototype LLC resonant converter

In order to maximize efficiency, we determine the transformer turns ration in a way that in the nominal output voltage and full loading condition the converter works in the resonant frequency. In the below equation $V_F$ is the forward voltage drop of antiparallel body diodes of the secondary MOSFETs.

$$\mathrm{n} \triangleq \frac{\mathrm{N_p}}{\mathrm{N_s}} = \frac{\mathrm{V_{in(nom)}}}{2\left(\mathrm{V_{o(nom)}} + \mathrm{V_F}\right)} = \frac{390}{2(24+1)} \approx 8 \tag{3.1}$$

Then, we choose $\mathrm{L_r}$ in a way that the output short circuit current is limited to the nominal output current.

$$\frac{\frac{\mathrm{V_{in}}}{2}}{\mathrm{L_r}} \times \frac{\mathrm{T}}{4} \leq \frac{\mathrm{P_o}}{\mathrm{V_o}} \times \frac{1}{\mathrm{n}} \tag{3.2}$$

From (3.2) we can write:

$$L_r = \frac{nV_{o(nom)}V_{in(nom)}}{8f_{s(max)}P_o} = \frac{8 \times 24 \times 390}{8 \times 450 \times 10^3 \times 650} \approx 32\ \mu H \tag{3.3}$$

In (3.3) we limit the frequency to approximately double of the resonant frequency. We set the resonant inductor to $35\ \mu H$ to satisfy (3.3). By choosing the resonant frequency to be 200 kHz, we can calculate the amount of resonant capacitor in (3.4).

$$C_r = \frac{1}{(2\pi f_{r1})^2 L_r} = \frac{1}{(2\pi \times 200 \times 10^3)^2 35 \times 10^{-6}} \approx 18.1\ nF \tag{3.4}$$

We use two standard $8.2$ nF capacitor in a split structure. With the resonant tank parameters in hand, we can calculate the characteristic impedance of the resonant tank and minimum quality factor.

$$Z_o = \sqrt{\frac{L_r}{C_r}} = \sqrt{\frac{35 \times 10^{-6}}{16.4 \times 10^{-9}}} = 46.19 \tag{3.5}$$

$$Q_{min} = \frac{Z_o}{R_{ac(max)}} = \frac{Z_o}{\frac{8n^2}{\pi^2} \times \frac{V_{o,max}^2}{P_o}} = \frac{46.19}{\frac{8 \times 8^2}{\pi^2} \times \frac{36^2}{650}} \approx 0.45 \tag{3.6}$$

The choice of magnetizing inductance should facilitate the following:

- ZVS at no load
- Required gain range

At no load and during the dead time when both primary switches are turned off, the magnetizing current should be high enough to discharge the output capacitance of one switch and charge the output capacitance of the other one.

$$I_{Lm(peak)} \times t_d \geq V_{in(max)} \times 2C_{oss(eff,tr)} \tag{3.7}$$

In other words:

$$\frac{nV_{o(min)}}{L_m}\left(\frac{1}{4f_{s(max)}}-\frac{t_d}{2}\right)\times t_d \geq V_{in(max)}\times 2C_{oss(eff,tr)} \tag{3.8}$$

In (3.9) we assume that the converter can lower the output voltage to 18V in continuous mode operation. By considering 400 ns dead time, the maximum $L_m$ from the ZVS point of view will be:

$$L_{mZVS(max)}=\frac{nV_{o(min)}}{V_{in(max)}\times 2C_{oss(eff,tr)}}\left(\frac{1}{4f_{s(max)}}-\frac{t_d}{2}\right)\times t_d = 102.16\ \mu H \tag{3.9}$$

In the above equation, $C_{oss,eff}$ is the time related effective drain to source junction capacitance of IPX65R110CFD from Infineon Technologies. We intend to use this MOSFET in the primary side of the converter.

Additionally the magnetizing inductance should be chosen in a way to facilitate the maximum DC gain required. The maximum required gain considering 10% overload is calculated in (3.10).

$$G_{DC,max}=n\frac{V_{o(max)}+V_F}{\frac{V_{in(min)}}{2}}=8\times\frac{36+1}{\frac{370}{2}}(110\%)=1.76 \tag{3.10}$$

From [28] we know:

$$\frac{V_{in}}{2nV_o}=1+\frac{\pi^2}{4}\times\frac{L_r}{L_m}\left(1-\frac{f_{r1}}{f_s}\right) \tag{3.11}$$

Then by considering minimum switching frequency to be 130 kHz, we have:

$$L_{m_{Gain(max)}} = L_r \frac{\pi^2}{4} \times \frac{\left(\frac{f_{r1}}{f_{s(min)}} - 1\right)}{\left(1 - \frac{1}{G_{dc(max)}}\right)} \tag{3.12}$$

$$L_{m_{Gain(max)}} = 35 \times 10^{-6} \frac{\pi^2}{4} \times \frac{\left(\frac{200 \times 10^3}{130 \times 10^3} - 1\right)}{\left(1 - \frac{1}{1.76}\right)} = 107.68\ \mu H \tag{3.13}$$

The final value of $L_m$ is the minimum between the values in (3.9) and (3.12). We will use a transformer with a magnetizing inductance of approximately $103\ \mu H$ for this design.

The output capacitance should be designed in a way that it keeps the output voltage ripple within the desired band. For this purpose, the maximum equivalent series resistant (ESR) should be specified. If we consider maximum 2% peak-to-peak voltage ripple, we have:

$$ESR_{(max)} = \frac{2\% \times V_{o(nom)}}{\frac{\pi}{2} I_{o(max)}} = \frac{2\% \times 24}{\frac{\pi}{2} 27} = 11.32\ m\Omega \tag{3.14}$$

In order to choose the output capacitance we have:

$$C_o \Delta V = \int i_{c_o} dt \tag{3.15}$$

With 1% peak voltage deviation, we have:

$$\begin{aligned} C_o(1\% \times 24) = & \int_{\pi - \sin^{-1}\frac{2}{\pi}}^{\sin^{-1}\frac{2}{\pi}} 27 \times \frac{\pi}{2} \sin\left(\omega_{s(\max)} t\right) d\left(\omega_{s(max)} t\right) \\ & - \int_{\frac{\pi - \sin^{-1}\frac{2}{\pi}}{\omega_{smax}}}^{\frac{\sin^{-1}\frac{2}{\pi}}{\omega_{smax}}} 27 dt \end{aligned} \tag{3.16}$$

The minimum amount of output capacitance is $248\ \mu F$. However, using five standard 1000 $\mu F$ capacitors will facilitate finding suitable parts in order to meet voltage and current rating requirements. Table 3.1 list the design parameters for the prototype.

Table 3.1 - Prototype parameters

| Parameter | Min. | Typ. | Max. |
|---|---|---|---|
| Power | - | - | 650 W |
| Input Voltage | 370 V | 390 V | 410 V |
| Continuous Operation Output Voltage | 18 V | 24 V | 36 V |
| Switching Frequency | 130 kHz | | 450 kHz |
| Resonant Frequency | - | 210 kHz | - |
| Resonant Inductor | - | 35 µH | - |
| Resonant Capacitor | - | 2×8.2 nF | - |
| Magnetizing Inductance | - | 103 µH | - |
| Transformer Turn Ratio | - | 32:4:4 | - |
| Output Capacitance | - | 5×1000 µF | - |

## 3.4. ICE2HS01G Analog Solution for Synchronous Rectification in LLC Resonant Converter

Analog solutions for LLC resonant converters are generally favorable choices for battery charger manufacturers. It provides simplicity in design with low cost of production.

There are a few analog integrated circuits (ICs), which are commercially available for LLC resonant converter control with synchronous rectification. In this

section, we are going to investigate the features of ICE2HS01G controller from Infineon Technologies in battery charging application.

ICE2HS01G is an analog IC designed by Infineon Technologies to be used in LLC resonant converters with synchronous rectification [29]. It is designed to work in frequencies up to 1 MHz. The IC does not require any external circuit for driving secondary side MOSFETs [30]. Additionally, the controller provides adjustable minimum and maximum switching frequency and dead time. Furthermore, the device supports burst mode control and missing cycle control to be used in no load and light loading condition, respectively [29].

- **Primary side control**

The ICE2HS10G controller is equipped with current controlled pulse frequency modulator to regulate the output voltage of LLC resonant converter. In typical applications, resonant tank current information is used for protection. The controller provides adjustable minimum and maximum switching frequency. Additionally, the dead time can be tuned to assure ZVS at primary [29]. During the start up, the control mechanism is able to sweep the frequency from a very high adjustable value to the point that the control loop takes over the frequency adjustment. In this way, the output voltage is gradually built and the resonant current will be limited during start up [29].

- **Current sense and protection**

In the typical application for this controller, the current is observed by sensing the rectified version of the voltage of the resonant tank capacitor. In response to overload, either the switching frequency will be increased quickly or the gate signals will be latched off for a certain period. The protective act takes place based on duration and level of overload [29].

- **Light load operation**

Light load and no load operation of LLC converter can push the switching frequency to very high values. High switching frequency will result in increased switching loss, transformer core loss and gate drive loss. To avoid high frequencies in light load condition, missing cycle technique is implemented in Infineon controller. In this technique, every two of five switching cycles is blanked to decrease the effective gain of the converter [29].

Burst mode control feature is also implemented in this controller to facilitate no load control. In this method, when the switching frequency reaches an adjustable maximum level, the gate signals will be disabled. The output voltage will be decreased that will also decrease the switching frequency through voltage feedback control loop. The moment, in which the switching frequency reaches a minimum adjustable level, the gate signals will be enabled again. This will result in periodic enabling and disabling of gate signals that helps the converter to operate in extremely light loading with limited switching frequency [29].

- **Synchronous rectification control**

Synchronous rectification control unit is the key component that makes the Infineon an outstanding analog solution compared to other controllers. The synchronous rectification in this controller has three units named as turn on delay, on time control and turn off delay. The controller also provides protection for SR gate signals.

The current drawn from the SRD pin of the controller determines the on time of the secondary side switches. Adjusting this current based on the current in the resonant tank lets the controller to shrink the gate pulse for low output currents [29].

By assuming that the converter works below resonance frequency in the normal operating condition, the controller applies a non-adjustable 250 ns delay in turn on. This will let enough time for the recovery of SR body diodes in CCM mode that happens in high input voltages in above resonance region [29].

The ICE2HS01G is a primary side LLC controller. As a result, there are propagation delays for the secondary side gate signal caused by the optocoupler and gate driver circuit. In order to compensate for the propagation delay, an adjustable turn off delay is defined. Additionally, in order to ensure safe operation of the converter, synchronous rectification is disabled in over load condition and at start up.

## 3.5. Design of Control Parameters Recommended by Infineon

Figure 3.3 shows the pinout of ICE2HS01G analog controller. This IC offers a wide range of adjustable settings for controlling the LLC resonant converter with synchronous

rectification. Figure 3.4 show the simplified control circuit used in typical application for ICE2HS01G. In the following sections, the settings in this figure suitable for the designed prototype in section 3.3 are discussed in detail.

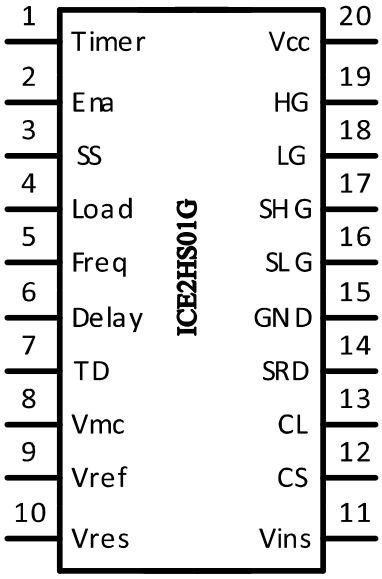



Figure 3.3 - ICE2HS01G pinout [29]

### 3.5.1. Frequency Regulation

In figure 3.4, the frequency pin at the ICE2HS01G controller is regulated at 2V. The output current of this pin determines the switching frequency. Figure 3.5 shows the relationship between the effective resistance connected to this pin, $R_{freq}$, and the switching frequency [30].

Assuming the 400 ns dead time we can formulate the switching frequency relationship with the output current ($I_{freq}$) of frequency pin as shown below.

$$f_s = \frac{0.5}{\frac{k_1}{I_{freq}} + 400 \times 10^{-9}} \tag{3.17}$$

In the above equation $k_1$ is equal to $8.92 \times 10^{-10}$. In order to reach frequencies as low as 130 kHz we set $R_{f,min}$ to 14 kΩ. Saturation voltage of the secondary side of the optocoupler is the limit for high frequency operation. By setting $R_{reg}$ to 2.8 kΩ, we can go to frequencies as high as 350 kHz.

### 3.5.2. Dead Time Setting

In figure 3.4, the current going into the TD pin determines the dead time. Figure 3.6 shows the relationship between dead time and the effective resistor connected to TD pin. By setting $R_{TD}$ to 220 kΩ, we set the dead time to approximately 400 ns. This assures ZVS for all switching frequencies. In figure 3.4, $V_{ref}$ is regulated at 5V.

### 3.5.3. Missing Cycle Control

Missing cycle control mechanism disables two cycles out of every five switching cycle to prevent the circuit from working at extremely high frequencies in light loading condition. This feature works based on the voltage on CS pin. In figure 3.4, the entering and exiting level for missing cycle control can be adjusted by setting the resistors connected to $V_{mc}$ pin. Setting for entering and leaving the mode are shown in (3.18) and (3.19), respectively.

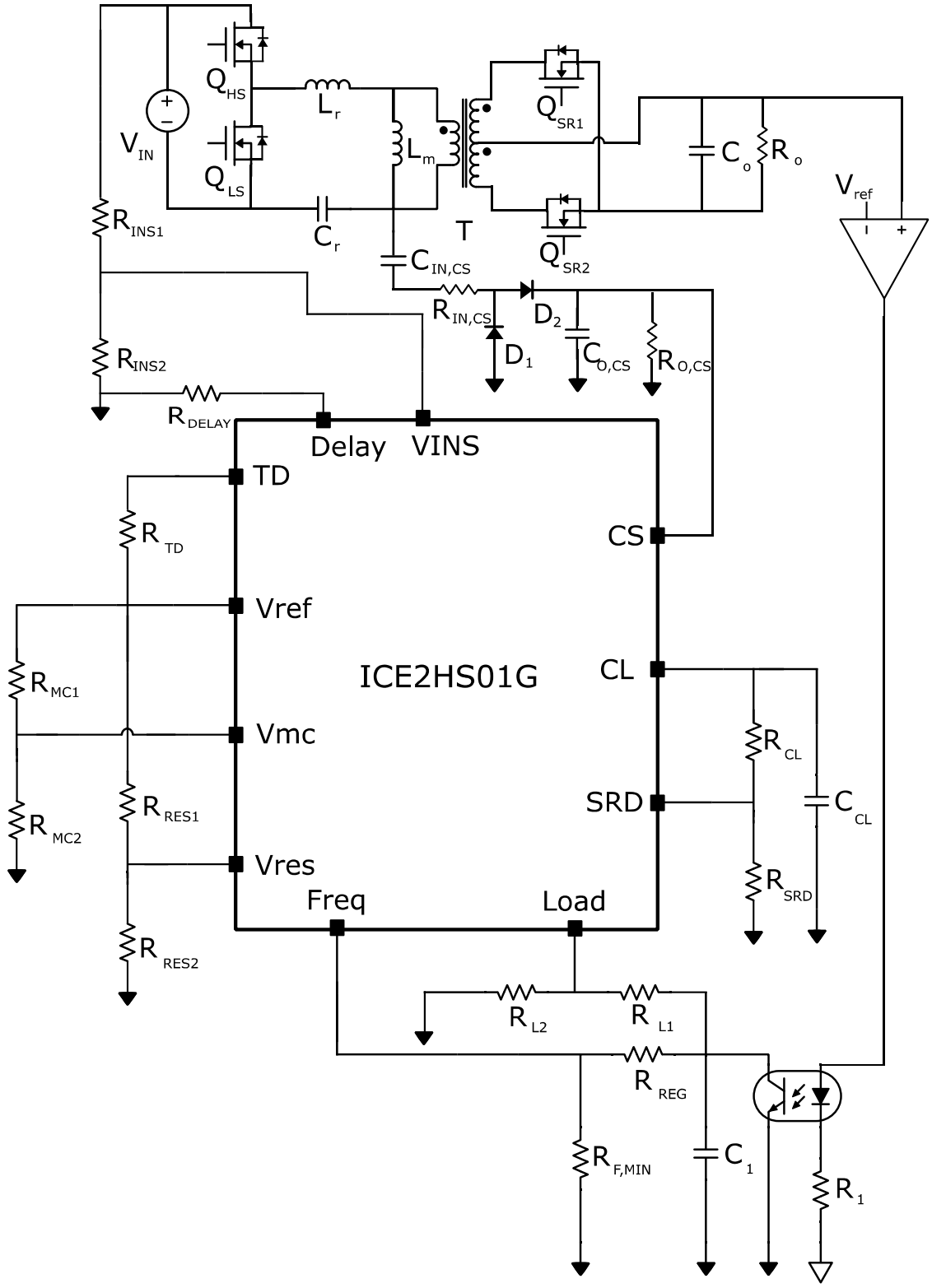



Figure 3.4 - Simplified control mechanism in ICE2HS01G

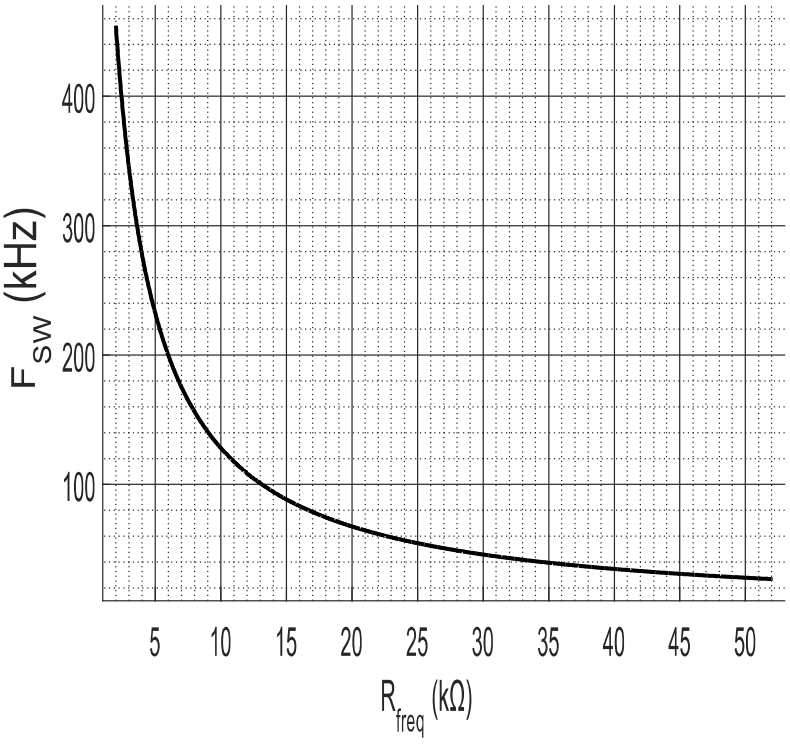



Figure 3.5 - Relationship between effective resistance at frequency pin and switching frequency [30]

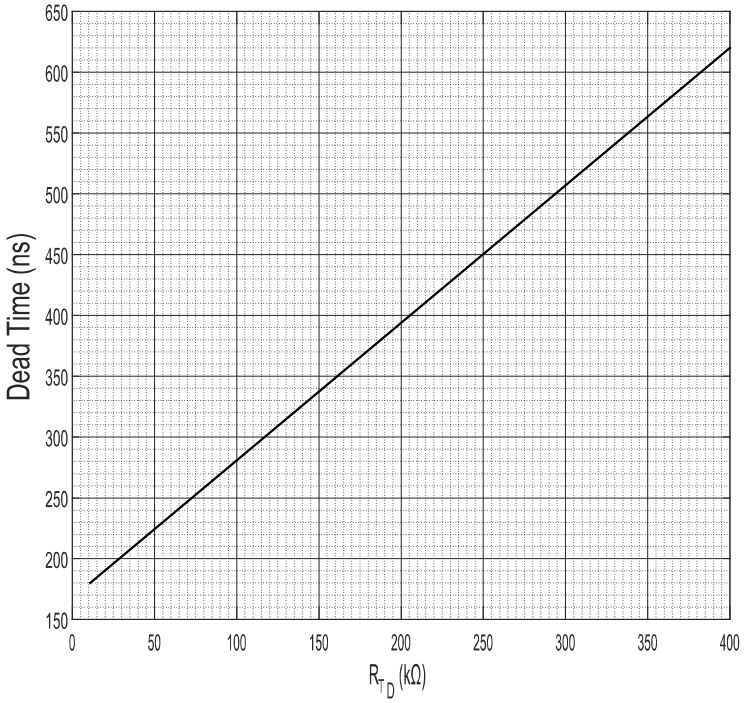



Figure 3.6 - Dead time relationship with $R_{TD}$ [30]

$$V_{E,mc} = V_{ref} \frac{R_{mc,2}}{R_{mc1} + R_{mc2}} \tag{3.18}$$

$$V_{L,mc} = V_{ref} \frac{R_{mc2}}{R_{mc1} + R_{mc2}} + I_{mc} \frac{R_{mc2} R_{mc1}}{R_{mc1} + R_{mc2}} \tag{3.19}$$

In the above equation, $I_{mc}$ is equal to 50 μA. By setting $R_{mc1}$ to 20KΩ and $R_{mc2}$ to 200Ω, we can set the entering and leaving missing cycle control to be 50 mV and 60 mV respectively.

### 3.5.4. Burst Mode Control Setting

The Burst Mode (BM) operation in ICE2HS01G is implemented with LOAD pin in figure 3.4. If the voltage on LOAD pin is lower than 0.1V, all the gate drives will be pulled low after the next high side switching cycle is finished. If the LOAD pin voltage increases higher than 0.15V, IC will resume switching [30]. Every time IC resumes switching from burst mode, the first pulse will be high gate with reduced duty cycle. In order to inspect the operation of the controller in a wide frequency range, the burst mode is intentionally disabled for this application.

### 3.5.5. SR On Time Control

Figure 3.7 shows the relationship between the effective resistance on SRD pin and the synchronous rectification on time. The secondary side on time is determined by either the value set through SRD pin or the falling edge of corresponding primary side gate signal. The one that comes first will determine the turn off time of the secondary MOSFET. By

using a fixed resistor at SRD pin in figure 3.4, we can apply a maximum on time for the secondary MOSFETs.

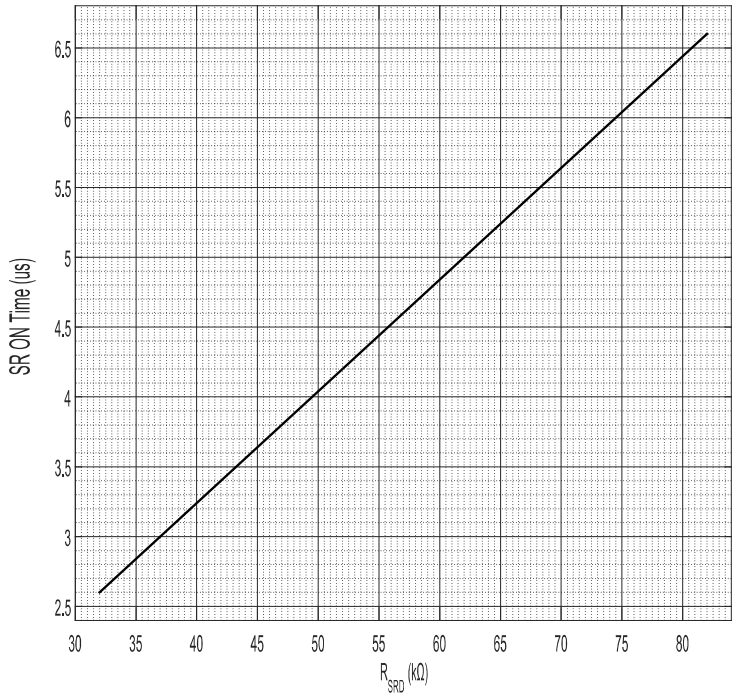



Figure 3.7 - Relationship between effective resistance on SRD pin and ON time of the SR MOSFETs [30]

A simple fixed on time control cannot provide the best response for different loading conditions. In constant output voltage applications, Infineon recommends to use the information of resonant tank current to take into account the changes in the load. The controller uses the information of DC value of rectified resonant tank current on CS pin in figure 3.4 to observe the level of output current.

In light load condition, the current in the resonant tank is decreased. This results in lower voltage on CS pin. Figure 3.8 shows the relationship between the voltages of CL and CS pins. The voltage on CL pin increase as the voltage on CS pin increases and it is

clamped at 2V. Using the CL pin, Infineon recommends implementing two mechanisms to determine secondary MOSFETs on time.

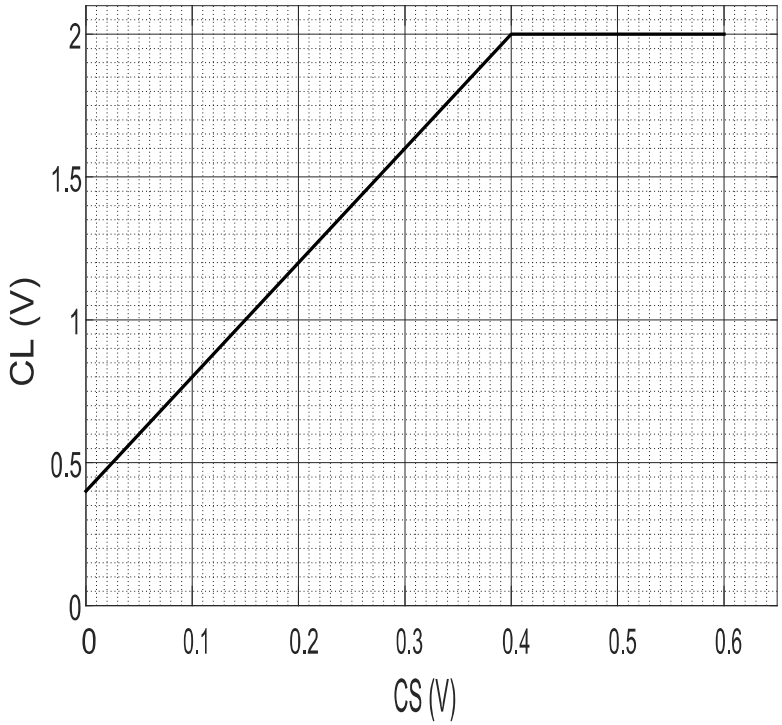



Figure 3.8 - Relationship between CS and CL

- **Maximum on time**

Maximum SR on happens when the least amount of current is drawn from the SRD pin. This happens when no current is drawn through $R_{CL}$. Infineon recommends to design this operating point for the rated output voltage and the heaviest loading in which the voltage of CL pin is clamped at 2V. The value of maximum on time can be tuned with $R_{SRD.}$

- **On time reduction**

In lighter loadings, the CL voltage decreases and draws more current from the SRD pin, which decreases the on time for light loading condition.

### 3.5.6. Turn On and Turn Off Delay

In addition to on time control, turn on and turn off advance delay are the synchronous rectification control features in Infineon controller. As discussed earlier a non-adjustable 250 ns turn on delay can be activated to account for SR MOSFET body diode recovery time in above resonance operation. Due to the broad frequency range of the chargers, making this delay adjustable would result in better performance for this application.

Turn off advanced delay is also available on Infineon controller to account for the propagation delay of the secondary gate signal. This turn off delay can be adjusted by the resistor connected to the delay pin in figure 3.4. Figure 3.17 shows the relationship between the connected resistor to delay pin and the turn off advanced delay. For this application, we use a 7.5 kΩ resistor to apply a delay close to 60 ns.

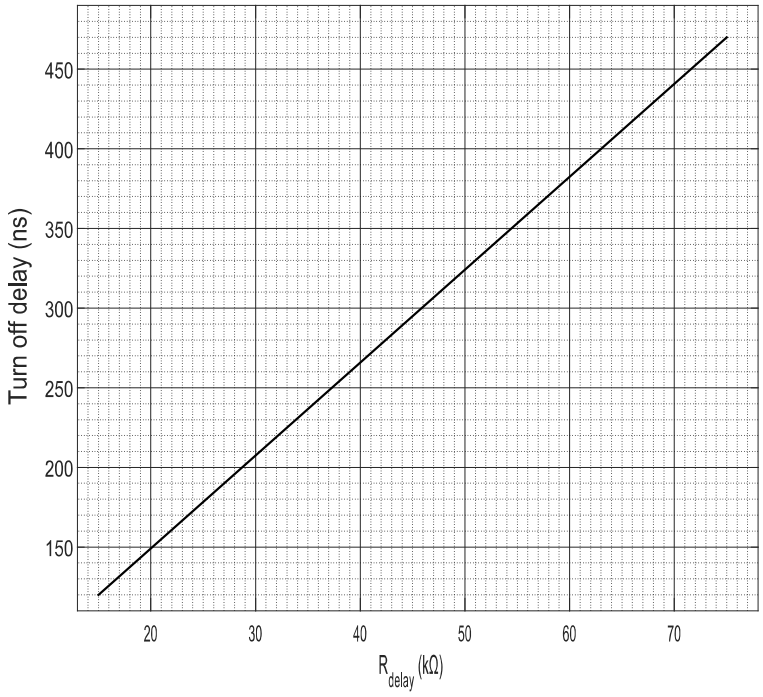



Figure 3.9 - Relationship between $R_{delay}$ and turn off advanced delay [30]

## 3.6. Proposed Modifications in Control Setting for Battery Charging Application

The proposed method by Infineon works great for fixed output voltage. However, the output voltage also has influence on the sensed voltage on CS pin that should be taken into account when designing the SR on time control circuit.

In order to reflect the change in the operating condition on the CS pin voltage, the parameter in the current sense circuit connected to CS pin should be modified. In contrast to recommended solution by Infineon, we propose considering the 0.4 level on CS pin for full loading at highest output voltage i.e. 36V. In this way, we will be able to use the on time reduction mechanism through $R_{CL}$. However, the voltage on CS pin will not exceed the 0.4 boundary and results in loss of over current protection. In this application, we

propose implementing an external over current protection using an Op-Amp. With this circuit shown in blue color in figure 3.13, we can pull down the voltage on Vins pin in case of an over current, which disables the gate signals.

Additionally, any change in the output voltage will result in change in magnetizing current in battery charging application. Magnetizing current and secondary side current are not synchronous. As a result, formulating the rate of change in the tank current due to change in output voltage or current is not straightforward.

Figure 3.10 includes simulation results from PSIM showing the relation between the change in optimum SR on time and DC component of rectified resonant tank current in response to change in the output current. The figure shows that the slope of change for 24V and 36V output are close with average amount of 40.35 ns/A. However, in the 18V case the change is sharp with the slope of 89.9 ns/A.

On the other hand, change in the voltage will also result in change in DC value of rectified resonant tank current. Figure 3.11 includes simulation results showing the relation between the change in optimum SR on time and dc component of rectified resonant tank current in response to change in the output voltage between 24V and 36V. The figure shows that the highest rate of change happens at 50% loading condition. Using this slope with the value of 62.5 ns/A can guarantee the safe operation of converter in all other operating conditions. However, the high rate of change will result in partial synchronous rectification in other cases that lowers the efficiency.

Figure 3.12 includes simulation results showing the relation between optimum SR on time and DC component of rectified resonant tank current in response to change in the output voltage between 18V and 24V. The figure shows that the slopes for this range of output voltage are bigger compared to those in 24V to 36V region. Below 24V output, the converter works above resonance and ZCS is not available for this switching region. In this mode, the corresponding primary side gate signal will have priority over the on time control mechanism and the converter will operate safely in this region as well. As a result, we need to only adjust the on time for change in the output current and voltage change between 24V and 36V.

With the recommended method in Infineon application note, only one change rate can be used for adjusting SR on time. With this technique, we have to choose the biggest desired change ratio for SR on time and the change with smaller desired ratio will result in partial synchronous rectification.

In this converter, the change in switching frequency due to the change in output current is much smaller compared to the change required for adjusting the voltage in below resonance region. We can use the information on frequency control pin to add a second mechanism for adjusting the SR on time.

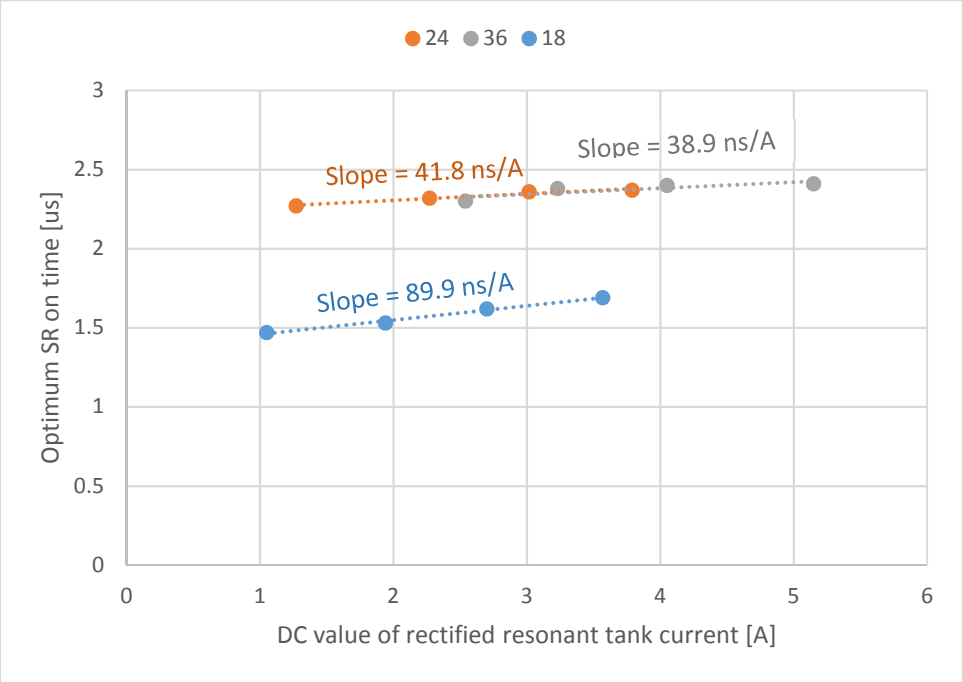



Figure 3.10 - Relation between rate of change of optimum SR on time and DC value of rectified resonant tank current in response to change in output current from 25% to 100% for different output voltages

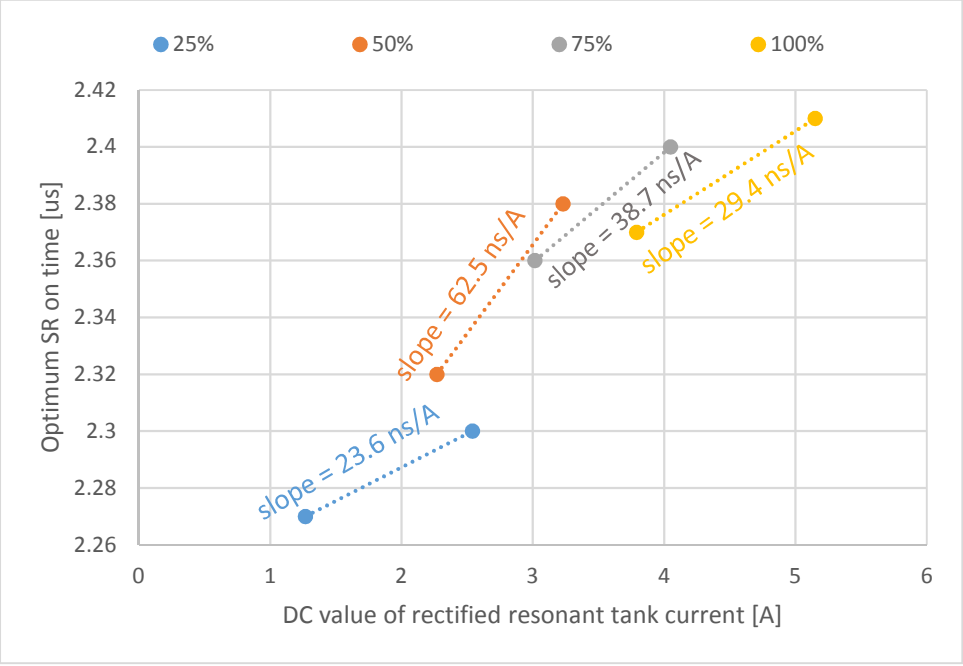



Figure 3.11 - Relation between rate of change of optimum SR on time and DC value of rectified resonant tank current in response to change in output voltage between 24V and 36V for different output currents

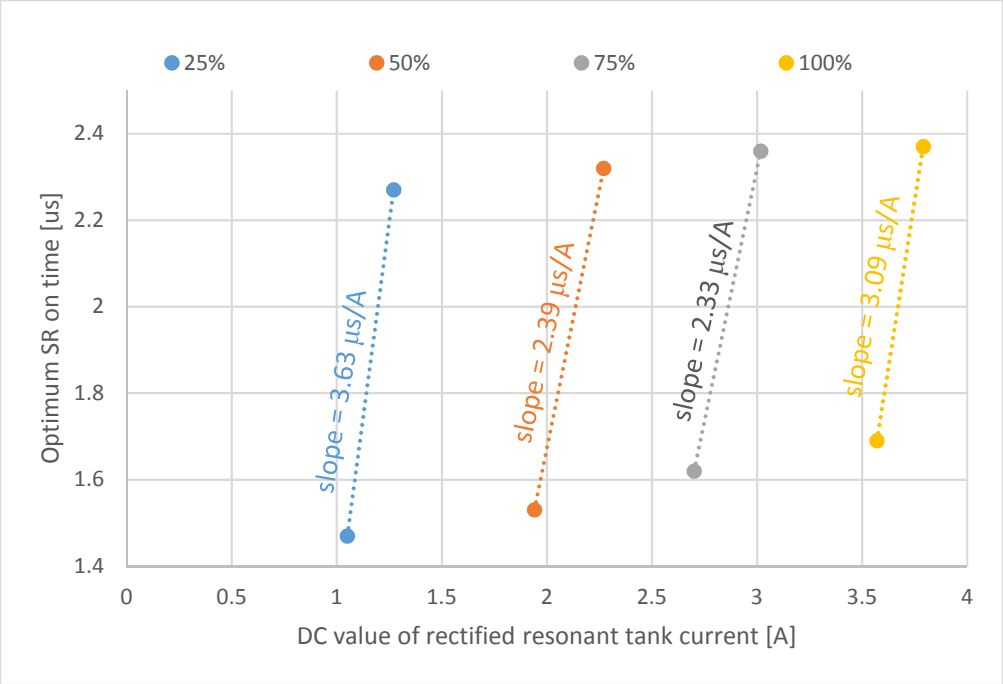



Figure 3.12 - Relation between rate of change of optimum SR on time and DC value of rectified resonant tank current in response to change in output voltage between 18V and 24V for different output currents

The added path for current on SRD pin shown in blue color in figure 3.13 is the proposed modification in SR on time control setting for LLC resonant converter as a battery charger. In this mechanism, we can use $R_{SRD}$ and $R_{CL}$ for implementing maximum on time and the smaller average change ratio (40.35 ns/A) for adjustment of on time due to change in current. Additionally, we can use $D_V$ and $R_v$ to implement the difference in the change ratio (62.5 – 40.35 ns/A) in on time due to the change in output voltage.

In order to tune the on time control setting for this application, we need to know the relationship between the DC value of rectified resonant tank current and voltage of CS pin. Based on figure 3.13 there is a capacitive current divider for the resonant tank current.

$$V_{CS} = R_o \frac{C_{IN,CS}}{C_r} I_{tank(DC)} \tag{3.20}$$

In order to have negligible effect on the operation of converter, $C_{in}$ should be at least 100 time smaller than the resonant capacitor. $C_{IN,CS}$ also should be able to withstand the AC and DC (for split capacitor structure) voltage of the resonant capacitor. To meet those two requirement we can use three 330-pF capacitors in series. For $R_{IN,CS}$ we use a typical value of 220 Ω. Choosing $R_o$ with the value of 15Ω will enable us keep the CS voltage below 0.4 for all of the operating conditions. Table 3.2 lists the parameters in the current sense circuit. With these parameters, we will not be able to use the over current feature of the controller. This feature is added externally through sensing the output current and pulling down the Vins pin in case of overcurrent.

As a result, we have

$$V_{CS} = 0.1\ I_{tank\ (DC)} \tag{3.21}$$

According to figure 3.8, the relationship between CL and CS is

$$V_{CL} = 4V_{CS} + 0.4 \tag{3.22}$$

The current drawn by CL pin is equal to

$$I_{CL} = \frac{2 - V_{CL}}{R_{CL}} \tag{3.23}$$

According to figure 3.7, the relationship between the current drawn from SRD pin and the SR on time is equal to:

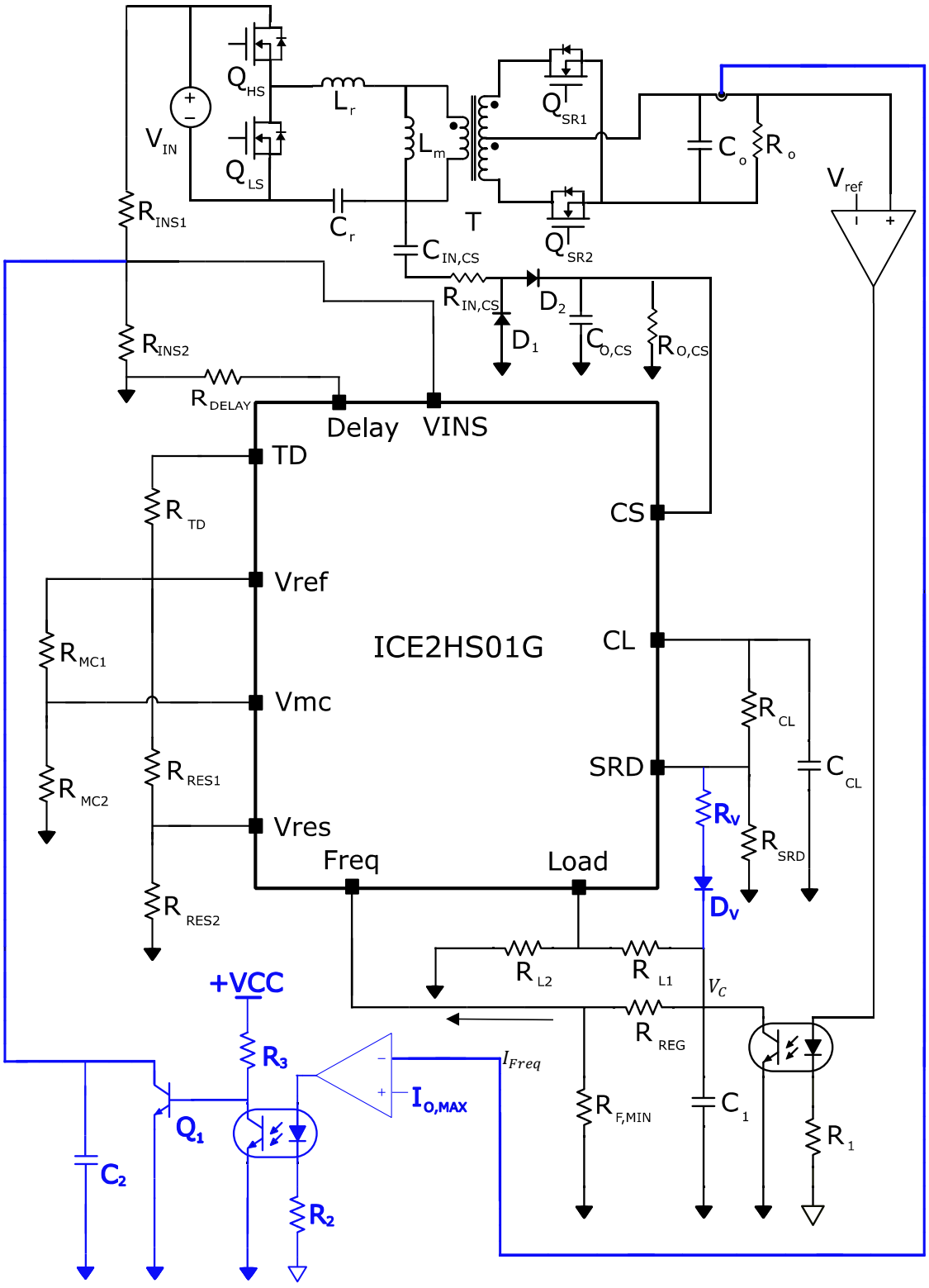



Figure 3.13 - Proposed modification in control setting for SR on time control

$$t_{on} = -0.1 I_{SRD} + 8.5 \tag{3.24}$$

In the above equation, the SR on time is in μs and the SRD pin current is in μA. The maximum on time for the converter is 2.41 μs. By using (3.24) we can set the value of $R_{SRD}$ to 32.84 kΩ.

Table 3.2 - Parameters in current sense circuit

| **Parameter** | **Value** |
|---|---|
| $C_{IN,CS}$ | 110 pF |
| $R_{IN,CS}$ | 220 Ω |
| $C_{O,CS}$ | 1 μF |
| $R_{O,CS}$ | 15 Ω |

The rate of change in the on time due to the change in current can be formulated as:

$$\frac{\partial t_{SR,on}}{\partial I_{dc,tank}} = \frac{\partial t_{SR,on}}{\partial I_{CL}} \times \frac{\partial I_{CL}}{\partial V_{CL}} \times \frac{\partial V_{CL}}{\partial V_{CS}} \times \frac{\partial V_{CS}}{\partial I_{dc,tank}} \tag{3.25}$$

Based on (3.21) to (3.24), we can write:

$$\frac{\partial t_{SR,on}}{\partial I_{dc,tank}} = -0.1 \frac{\mu s}{\mu A} \times \frac{-1}{R_{CL}} \frac{A}{V} \times 4 \times 0.1 \frac{V}{A} = \frac{40 \times 10^3}{R_{CL}} [\frac{\mu s}{A}] \tag{3.26}$$

In order to set the ratio to 40.35 ns/A, $R_{CL}$ is set to 991 kΩ.

Now we need to set $R_v$ in a way that it implements the additional 22.15 ns/A change rate for the times when the output voltage changes. $R_{reg}$ is 2.8 kΩ. By choosing a diode with suitable voltage drop, at 36V output, the current following through $R_v$ resistor is close to zero and the second on time adjustment has no effect. When the output voltage decreases, $V_c$ is decreased and the on time will be decreased accordingly. Any unwanted bias in the on time setting is adjusted through adjusting $R_{SRD}$ in the real prototype.

According to the data from simulation the average ratio between the change in DC value of rectified resonant tank current and the current drawn from the frequency pin when changing the voltage from 24V to 36V are listed in table 3.3 for different loading conditions.

Table 3.3 - The average ratio between the change in DC value of rectified resonant tank current and the current drawn from the frequency pin when changing the output voltage from 24V to 36V

| Loading | 25% | 50% | 75% | 100% |
|---|---|---|---|---|
| ratio | $-94.5\times10^{-6}$ | $-126.8\times10^{-6}$ | $-116.2\times10^{-6}$ | $-88.23\times10^{-6}$ |

The highest vale for the ratio happens at 50% loading. Using this value will result in smaller reduction in on time in other loading condition. This helps us to get closer to the ideal on times recorded with simulation. Equation (3.27) shows the relation between $V_c$ and the frequency pin current.

$$V_c = 2 - R_{reg}(I_{freq} - \frac{2}{R_{f,min}}) \quad (3.27)$$

By considering the forward voltage drop on $D_1$ in figure 3.13, the relation between $V_c$ and the current in $R_v$ can be formulated in (3.28). The diode forward voltage drop will be chosen in a way to avoid reduction in on time at heaviest loading condition.

$$I_{R_v} = \frac{2 - (V_c + V_{fd})}{R_v} \tag{3.28}$$

The rate of change due to change in voltage implemented with current through $R_v$ can be formulated as:

$$\frac{\partial t_{SR,on}}{\partial I_{dc,tank}} = \frac{\partial t_{SR,on}}{\partial I_{R_v}} \times \frac{\partial I_{R_v}}{\partial V_C} \times \frac{\partial V_C}{\partial I_{freq}} \times \frac{\partial I_{freq}}{\partial I_{dc,tank}} \tag{3.29}$$

By using equations (3.27) and (3.28) and the value for 50% loading in table 3.3, we can write:

$$\begin{aligned} \frac{\partial t_{SR,on}}{\partial I_{dc,tank}} &= -0.1\frac{\mu s}{\mu A} \times \frac{-1}{R_v}\frac{A}{V} \times -R_{reg}\frac{V}{A} \times -126.8 \times 10^{-6} \\ &= \frac{35.5 \times 10^3}{R_v}\left[\frac{\mu s}{A}\right] \end{aligned} \tag{3.30}$$

In order to set the additional rate of change to 22.15 ns/A, $R_v$ can be set to 1603 kΩ. It is clear that with the big amount of resistance for $R_v$, the effect of the added path for current will be negligible on the output of the optocoupler.

## 3.7. Summary

In this chapter, the complete design process of a 650W battery charger with rated output voltage of 24V is explained. Additionally, the control setting for ICE2HS01G

controller for this converter are presented. In order to enable the use of this controller in wide output voltage applications, a modified SR on time control mechanism is proposed. The modifications enable the controller to set optimum SR on time for different output voltages and currents. The modifications facilitate an affordable solution for synchronous rectification in LLC resonant converter in wide output voltage applications.

# Chapter 4 Prototype Design and Experimental Results

## 4.1. Overview

In this chapter, the voltage and current stresses in semiconductor parts are calculated. Based on the results, the parts with the best performance are chosen. Additionally the printed circuit board design technical considerations are explained. At the final part, experimental waveforms and efficiency test results are presented.

## 4.2. Stress Calculation, Simulation and Part Selection

### 4.2.1. Power Stage

Figure 4.1 shows the simulated power stage in PSIM. In this simulation, split resonant capacitor structure has been used. The magnetic parts have been implemented separately so that current sensing can be done easier. Ideal synchronous rectification method is used in this simulation which is based on sensing secondary side current.

The rectified secondary side current of the transformer supplies the output current. As a result, the maximum root mean square (RMS) value of the transformer primary side current in 10% overload condition can be calculated in (4.1).

$$I_{Pri(RMS)} = \frac{\pi}{2\sqrt{2}}\left(\frac{I_{o(max)} \times 110\%}{n}\right) = \frac{\pi}{2\sqrt{2}}\left(\frac{27 \times 110\%}{8}\right) = 4.12\ A \quad (4.1)$$

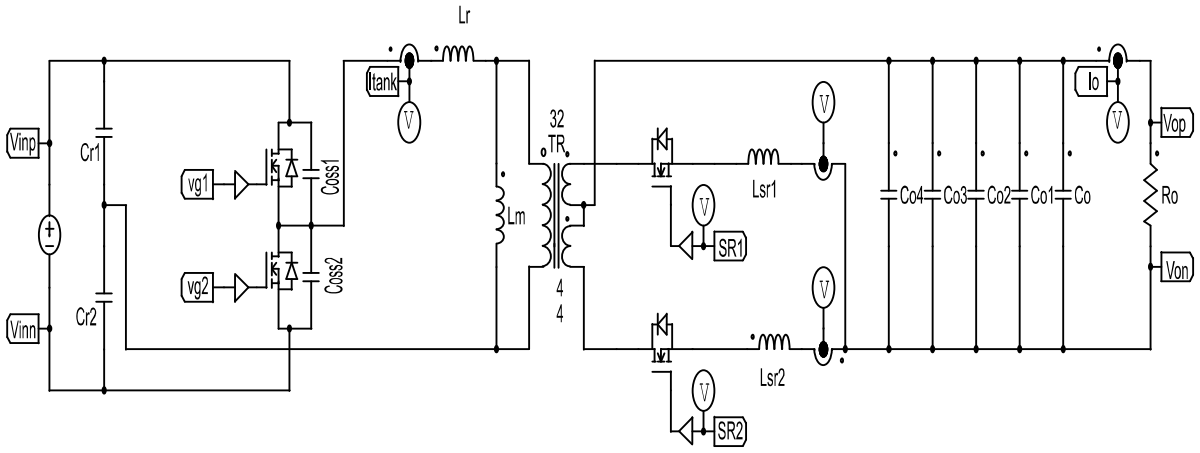



Figure 4.1 - Simulated power stage

The maximum RMS value for magnetizing current is calculated in (4.2).

$$I_{mag(RMS)} = \frac{1}{\sqrt{3}} I_{mag(\,peak)} = \frac{1}{\sqrt{3}} \times \frac{nV_{o(max)}}{4f_{s(min)}L_m} = 3.10\ A \tag{4.2}$$

Then the maximum RMS value for resonant tank current can be calculated as:

$$I_{res,RMS} = \sqrt{4.12^2 + 3.10^2} = 5.15\ A \tag{4.3}$$

The primary side switches carry half of the resonant tank current each. However, in transient condition one switch may carry the resonant tank current completely for a short period. As a result the primary side switch should be capable of carrying the current calculated in (4.3) i.e. at least 6.18 A, considering 20% safety margin. In addition, the primary side switch should be capable of blocking the input voltage. By considering the conventional safety margin, the blocking voltage of the primary side MOSFETs should be as high as 700 V.

Simulation results also verify the stress calculation. As we can calculate from figure 4.2 the RMS current going through the upper side primary switch, when the input voltage is set to minimum and the output power is set to maximum, is about 2.7 A. It is shown in figure 4.3 that the maximum reverse voltage applied to each switch is 410 V, when the input voltage is set to the maximum value.

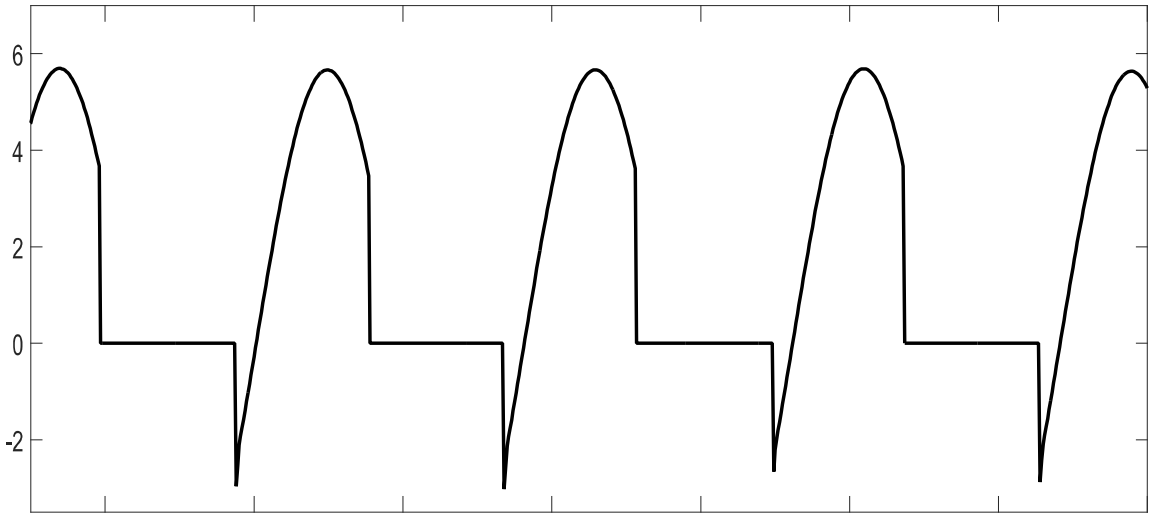



Figure 4.2 - Current stress in primary side MOSFETs

IPP65R110CFD, a MOSFET from Infineon is suitable for this application. The main specifications of the primary side switch are listed in table 4.1 [31].

Secondary side switches need to carry half of the transformer secondary side current. Based on (4.1), (4.4) can be used to calculate the maximum RMS value for current going through the secondary side switches.

$$I_{RMS,max} = \frac{1}{\sqrt{2}} \times n \times I_{Pri,RMS} = \frac{1}{\sqrt{2}} \times 8 \times 4.12 = 23.54\,A \qquad (4.4)$$

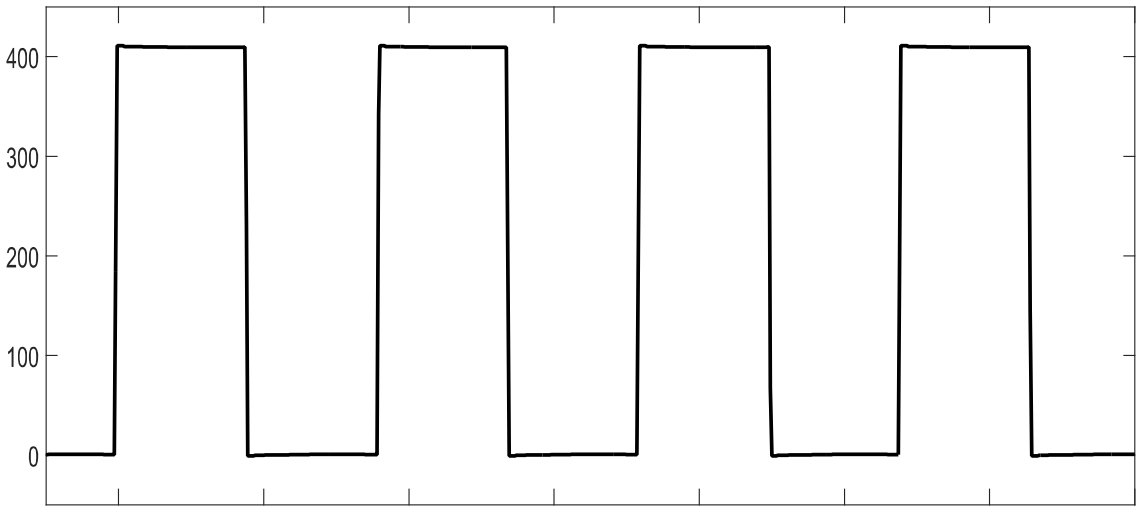



Figure 4.3 - Voltage stress in primary side MOSFETs

Table 4.1 - Specification of primary side switch (IPP65R110CFD)

| Parameter | Value | Unit |
|---|---|---|
| $V_{ds,max}$ | 700 | V |
| $I_{ds,max}$ @ $T = 25^{o}$ | 31.2 | A |
| $C_{oss,eff}$ | 586 | nF |
| $R_{DSon,max}$ | 110 | mΩ |

The switch also needs to block a reverse voltage as high as double of the maximum output voltage i.e. 72V. The maximum RMS output current is 32.53A when the input voltage is set to minimum value and the output current is at the maximum amount. During start up, all of the secondary side current may go through one MOSFET only.

Considering a safety margin, we need to use a switch capable of carrying 39 A RMS current, 100 A pulse current and 100 V of reverse voltage. BSC035N10NS5A from Infineon is suitable for this purpose. The key specifications of this switch are listed in table 4.2 [32].

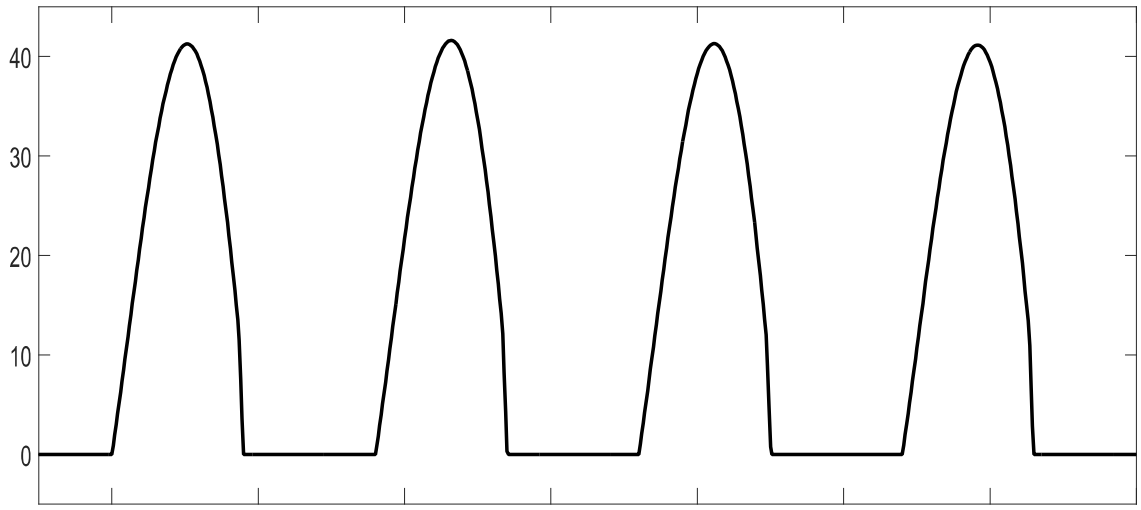



Figure 4.4 - Current stress secondary side MOSFETs

Table 4.2 - Secondary side switch specifications (BSC035N10NS5A)

| Parameter | Value |
|---|---|
| $V_{ds,max}$ | 100 |
| $I_{ds,max}$ @ $T = 25^{o}$ | 100 |
| $C_{oss,eff}$ | 1000 |
| $R_{DSon,max}$ | 3.5 |

At the secondary side, the RMS current going through the output capacitance can be calculated:

$$I_{Co,RMS,max} = \sqrt{\left(\frac{\pi}{2} I_{o(max)}\right)^2 - {I_{o(max)}}^2} = 32.70\ A \tag{4.5}$$

By using five 1000 µF capacitors at the output, we can find suitable part number for capacitors to withstand this high ripple in current. All other parts of the prototype that were not mentioned in this section were chosen based on the values presented in table 3.1.

### 4.2.2. Control Circuit

Few control parameters were modified due to implementation limitations. The value for $R_{reg}$ was decreased to 2.2 kΩ in order to avoid saturation in the output of the optocoupler. To maintain the same slope of change in the on time, $R_v$ is modified and an standard value resistor is used. This also required us to use a low voltage drop diode in place of $D_v$. In contrast to the simulation, ICE2HS01G controller turns on the secondary MOSFETs with a delay after corresponding primary side MOSFETs. In order to account for the 250 ns non-adjustable turn on delay, $R_{SRD}$ is set to 30 kΩ. The modifications are listed in table 4.3 . Other control circuit parameters were implemented according to the calculations in the previous chapter.

Table 4.3 - Modifications in the control board

| Parameter | Calculated | Implemented |
|---|---|---|
| $R_{reg}$ | 2.8 kΩ | 2.2 kΩ |
| $R_{SRD}$ | 32.8 kΩ | 30 kΩ |
| $R_{CL}$ | 991 kΩ | 1 MΩ |
| $R_v$ | 1603 kΩ | 1.2 MΩ |

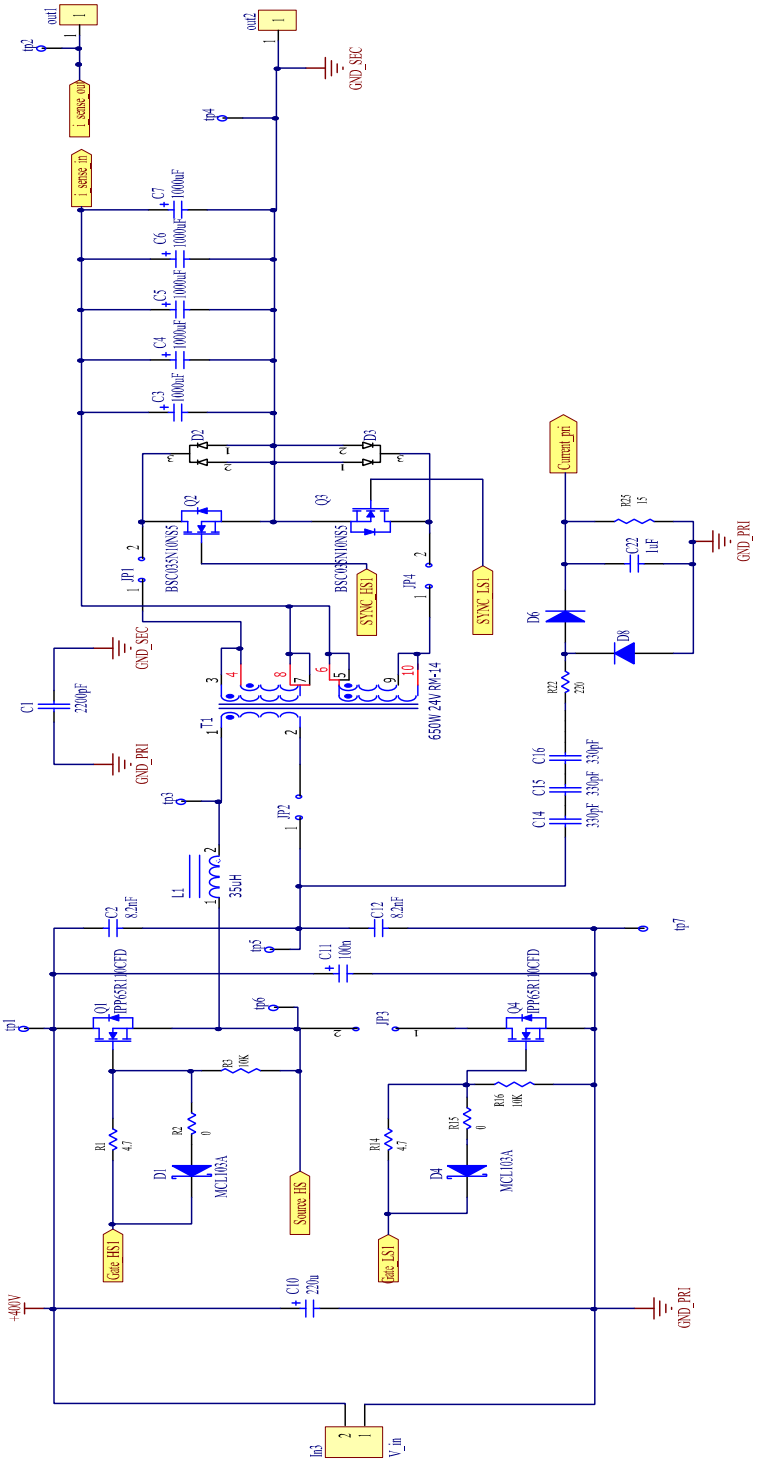


Figure 4.5 - Prototype schematic

## 4.3. Printed Circuit Board Design Considerations

Figure 4.5 shows the schematic design of the prototype. The split resonant capacitor structure is used in this design to make the converter robust in transient conditions. The resonant capacitor voltage is sensed to tune the secondary side MOSFET on time. This helps us avoid using a bulky current transformer.

At the secondary side, parallel diodes with the MOSFETs are used. This will enable us to compare the efficiency of the converter in diode conduction mode with synchronous rectification mode.

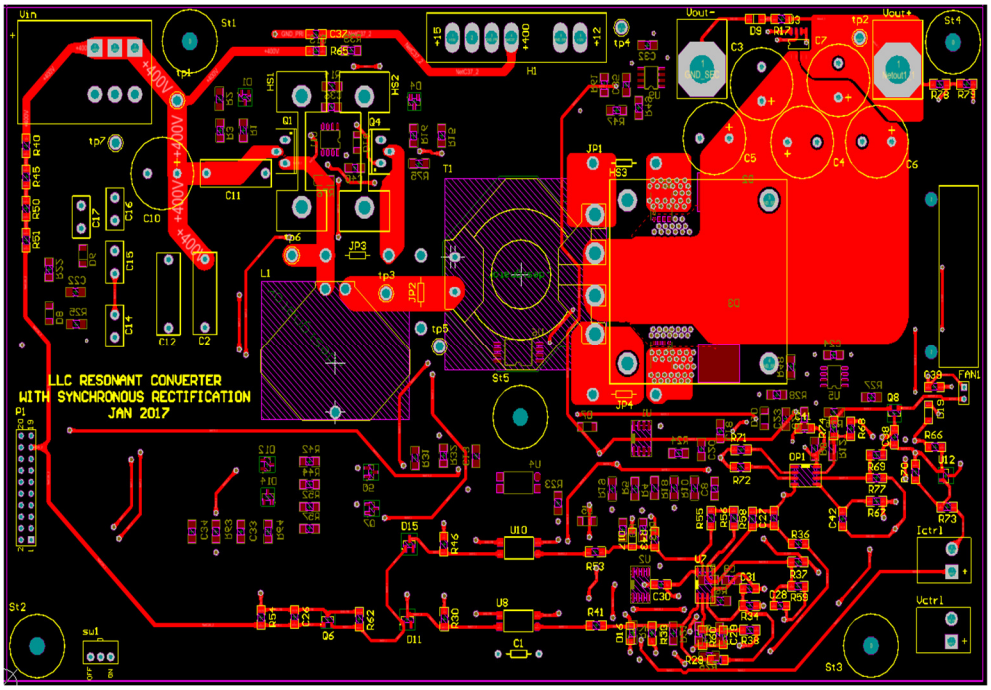



Figure 4.6 - Printed circuit board design for top layer

In order to maximize the efficiency and to have the chance to manipulate parameters on the board, the prototype was designed as a 15cm by 25 cm in four 2-ounce copper layers. The layers are shown in figure 4.6 to figure 4.8. The two internal layers are used for ground

connection and auxiliary voltage supply. The two outer layers are used for power stage connection and control signal routing.

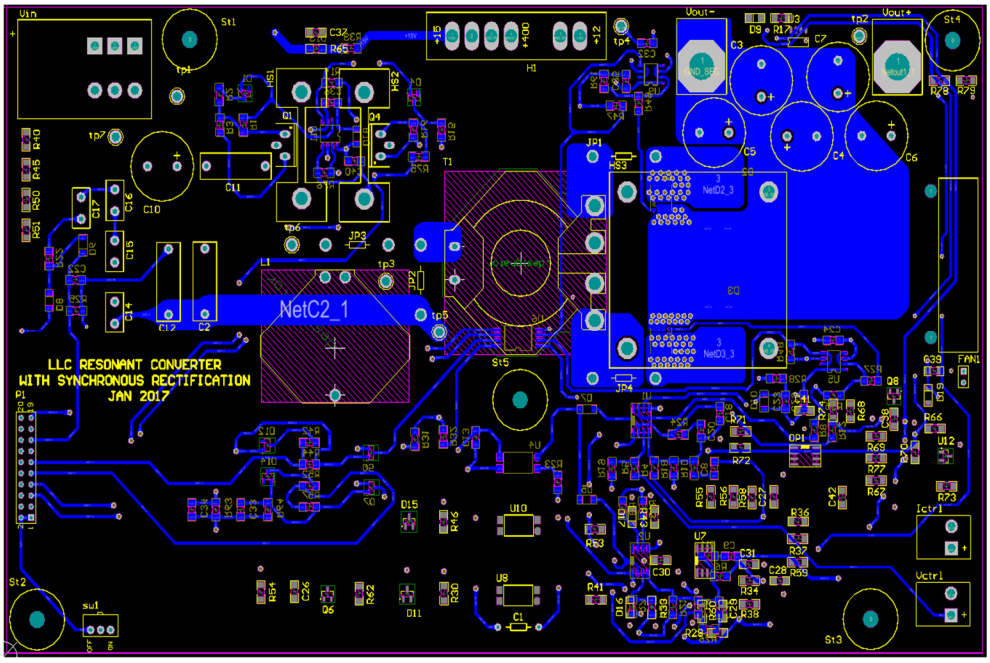



Figure 4.7 - Printed circuit board design for bottom layer

To-220 package is used for primary MOSFETs in order to have easy replacement and better heat transfer.

## 4.4. Experimental Results

Figure 4.10 shows the analog prototype. The prototype was built as a 4-layer PCB. The following figures show the experimental waveform in different loading conditions.

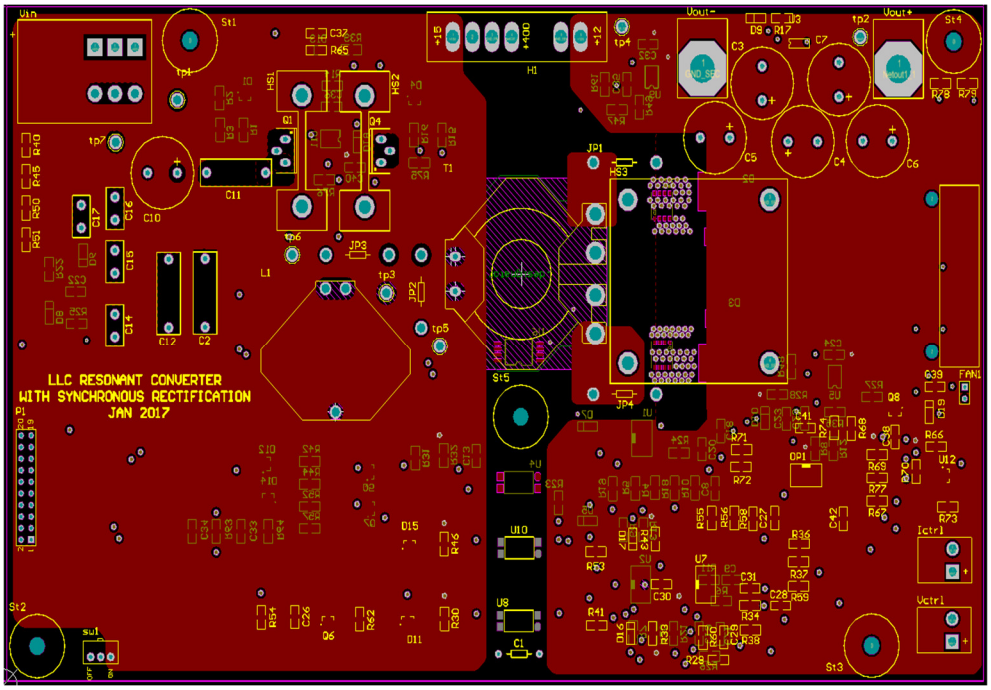



Figure 4.8 - Printed circuit board design for internal layer 1

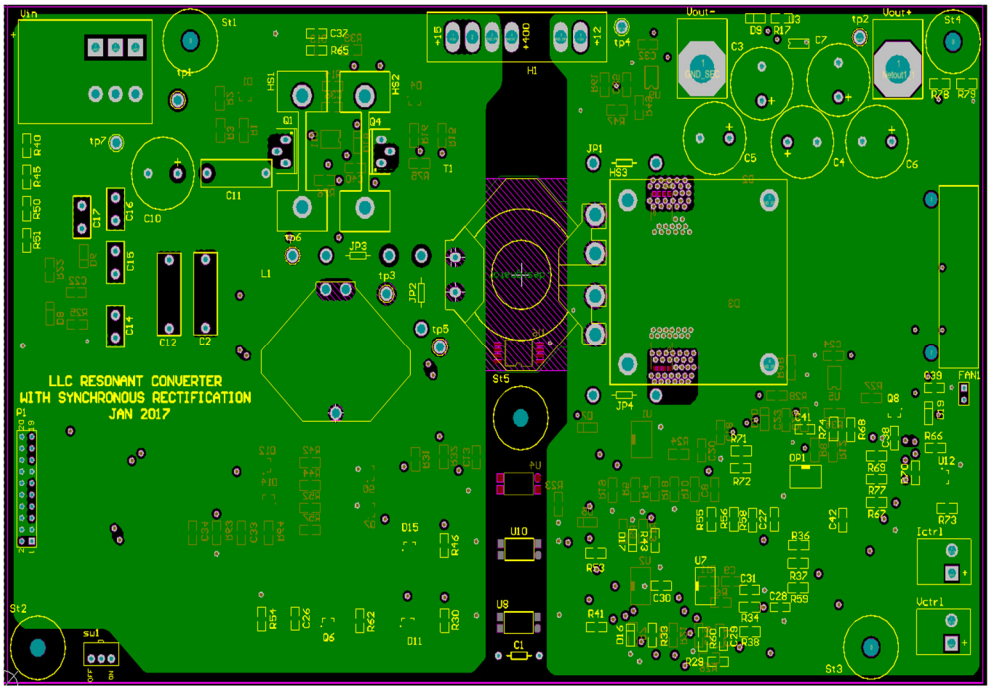



Figure 4.9 - Printed circuit board design for internal layer 2

Figure 4.11 shows the primary side waveforms at 36V and 13.5A loading. The waveforms show that the drain to source voltage of the MOSFET goes to zero right before

turn on and ZVS happens at this loading condition. Turn on and turn off transition in the primary MOSFETs are reasonably fast. In this waveform, the effect of magnetizing current on the on time of secondary side MOSFET is clear.

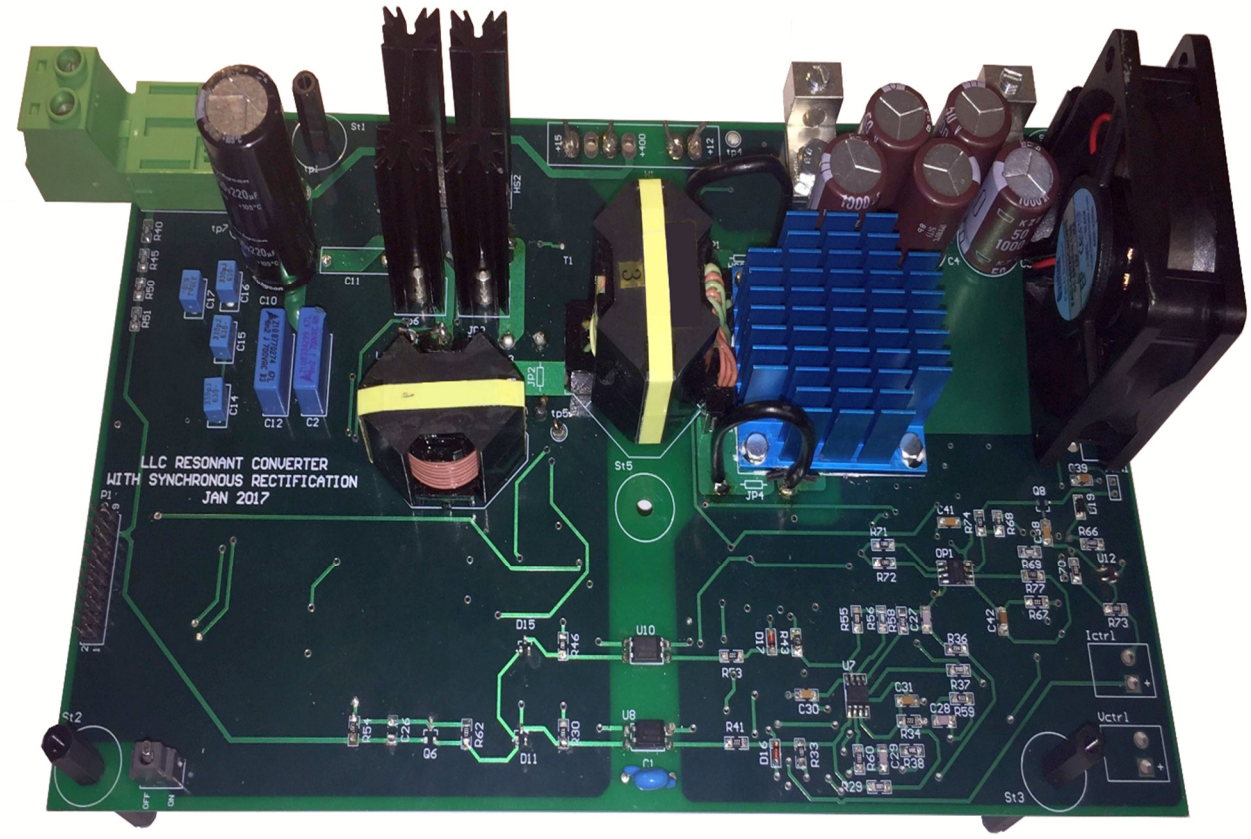



Figure 4.10 - The experimental prototype

Figure 4.12 shows the secondary waveforms at 36V and 13.5A loading. The non-adjustable 250 ns turn on delay and optimum turn off is clear in the waveform.

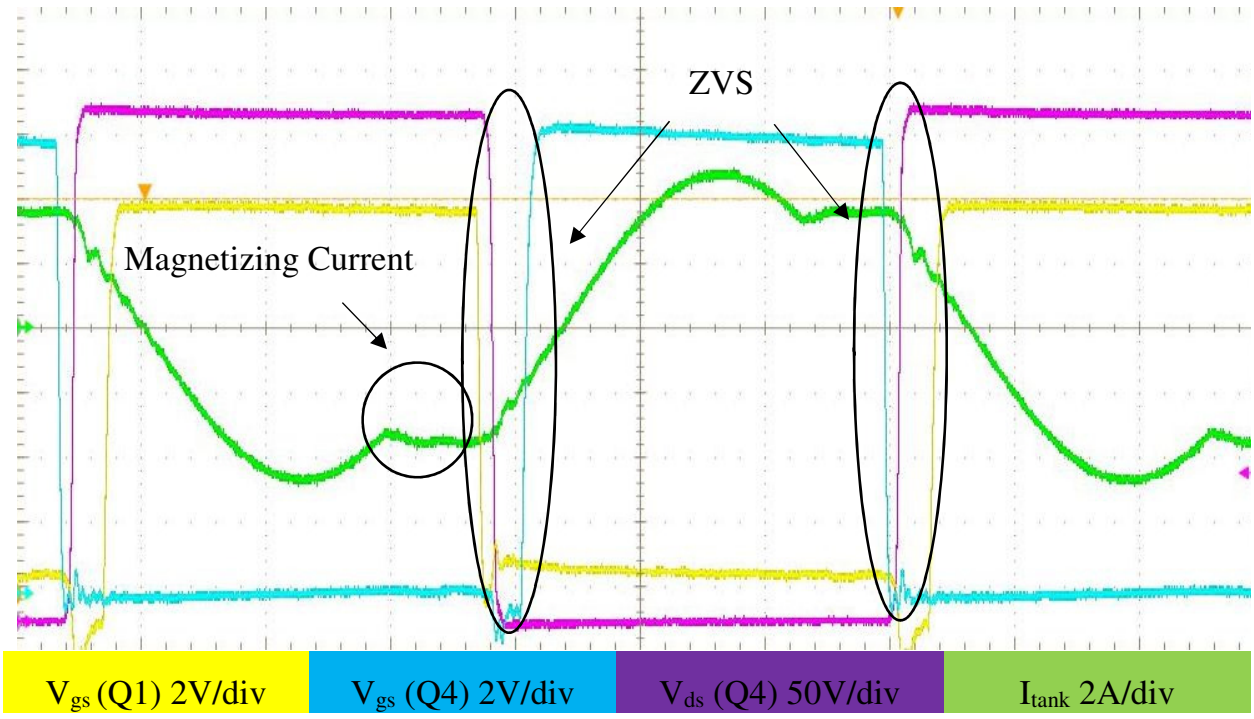



Figure 4.11 - Primary side waveforms at 36V and 13.5A output (1µs/div)

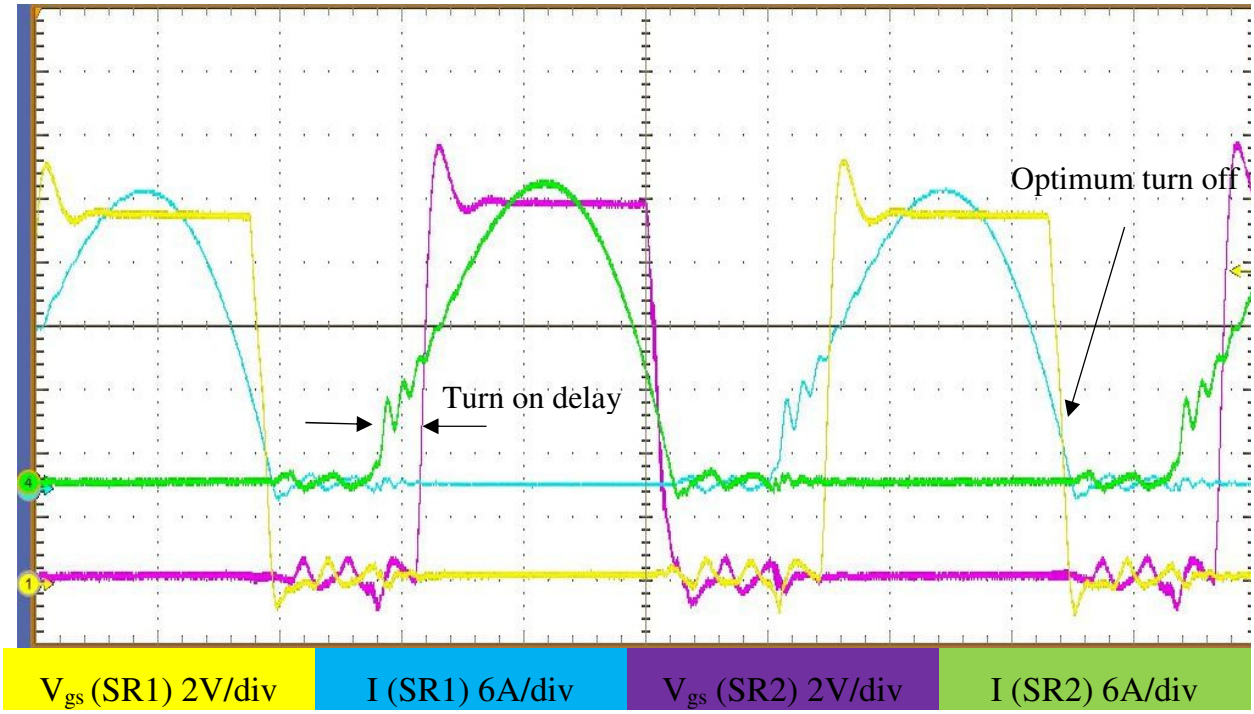



Figure 4.12 - Secondary waveforms at 36V and 13.5A output (1µs/div)

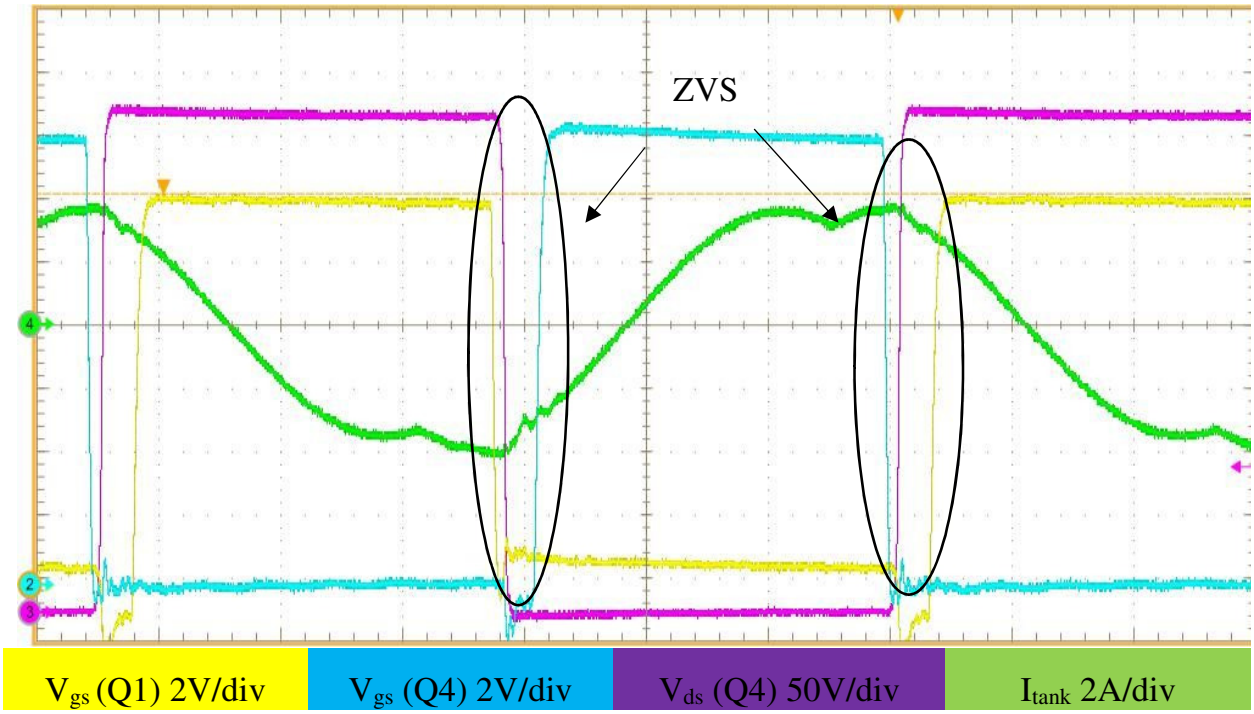



Figure 4.13 - Primary side waveforms at 36V and 6.75A output (1µs/div)

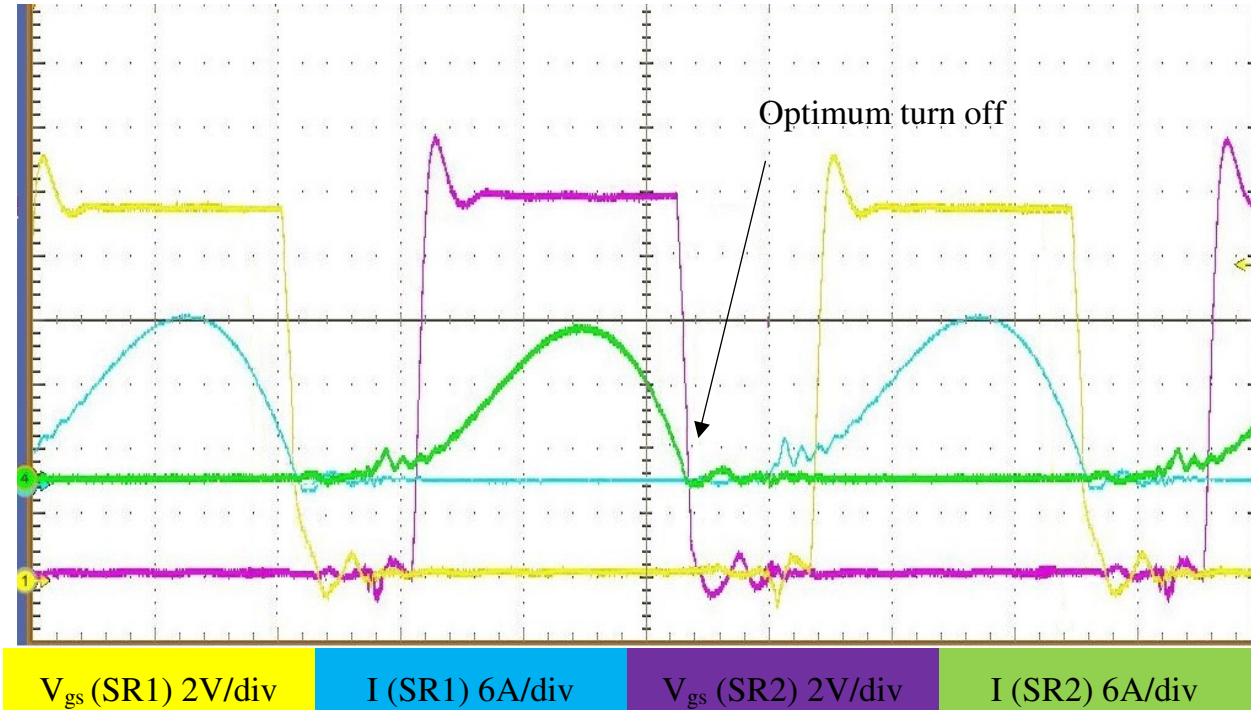



Figure 4.14 - Secondary side waveforms at 36V and 6.75A loading (1µs/div)

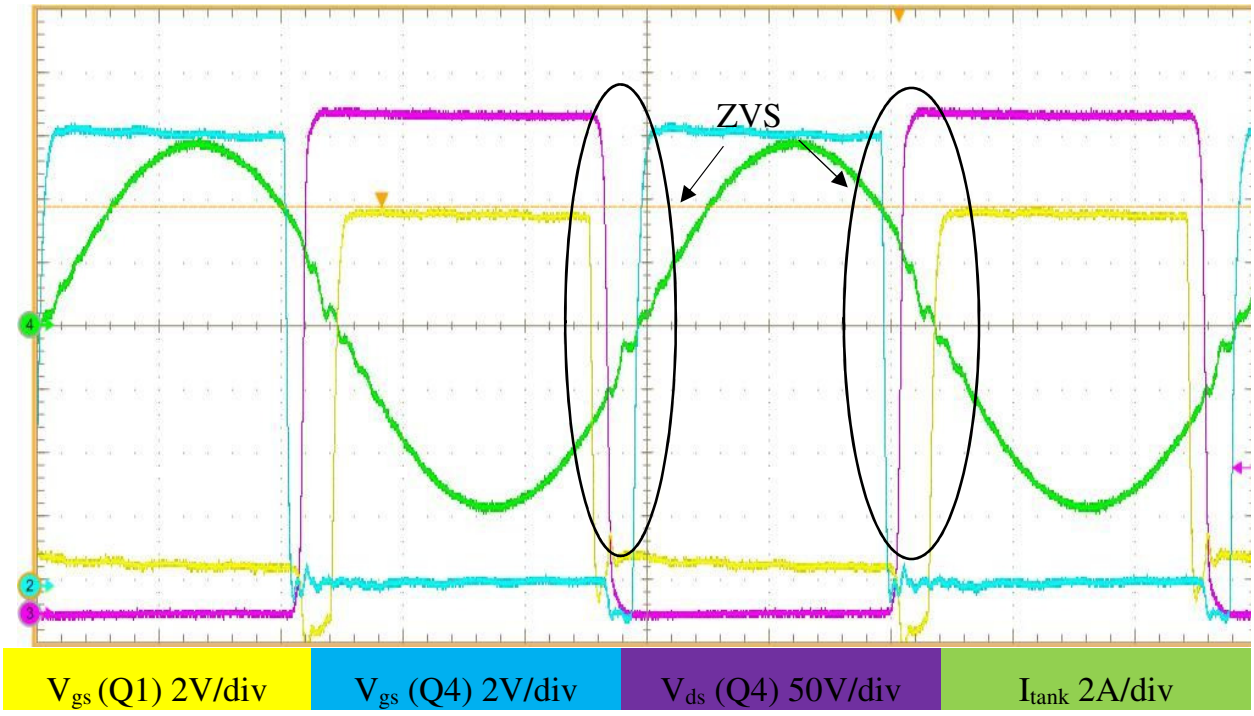



Figure 4.15 - Primary waveforms for 24V and 27A output (1µs/div)

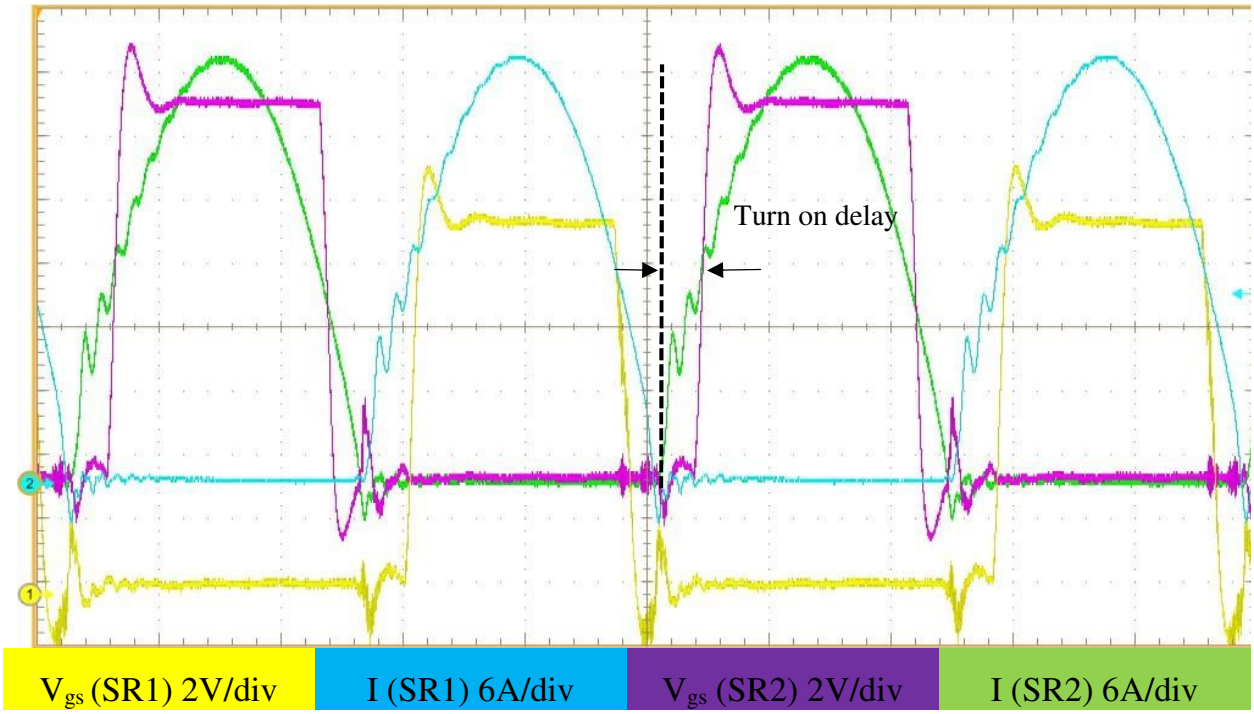



Figure 4.16 - Secondary waveforms for 24V and 27A output (1µs/div)

In contrast to other applications, light load efficiency is important in battery charging application where fully charging the battery requires the converter to work in light loading condition. Figure 4.13 shows the primary side waveform in 36V output and 25% loading condition. ZVS turn on is achieved in this mode. The resonant tank current is very close to the triangular shape of the magnetizing current, which results in low efficiency.

Figure 4.14 shows the secondary side waveform at light loading for 36V output. Because of the low current at the secondary side, the effect of turn on delay in not as noticeable as it is in the 13.5A loading case. The turn off time is optimum in this loading condition as well.

Figure 4.15 and 4.17 shows the primary waveform at 24V for 27A and 6.75A loading condition, respectively. In these waveforms, the transition of drain to source voltage of primary MOSFETs is without any overshoot and ZVS is achieved. In the waveforms the resonant tank current is very close to a sinusoidal shape and the effect of magnetizing current cannot be seen in the tank current.

Figure 4.16 and 4.18 shows the secondary side waveform at 24V for 27A and 6.75A loading condition, respectively. In these two figures, the turn off is close to the optimum moment. However, the turn on delay has a significant impact on the efficiency.

At the very beginning of a charging cycle, the converter works in low output voltage and high output current. Figure 4.19 and 4.21 show the primary side waveform

at 18V for 27A and 6.75A loading condition, respectively. In these waveforms, the sinusoidal trend of the resonant tank current is changed at the points where the secondary side current is forced to zero. Figure 4.20 and 4.22 show the secondary side waveform at 18V for 27A and 6.75A loading condition, respectively. In both cases, there is a large difference between the optimum and actual gate signal. In this output voltage, the controller lets the primary side gate falling edge control the secondary gate signal that results in poor synchronous rectification performance.

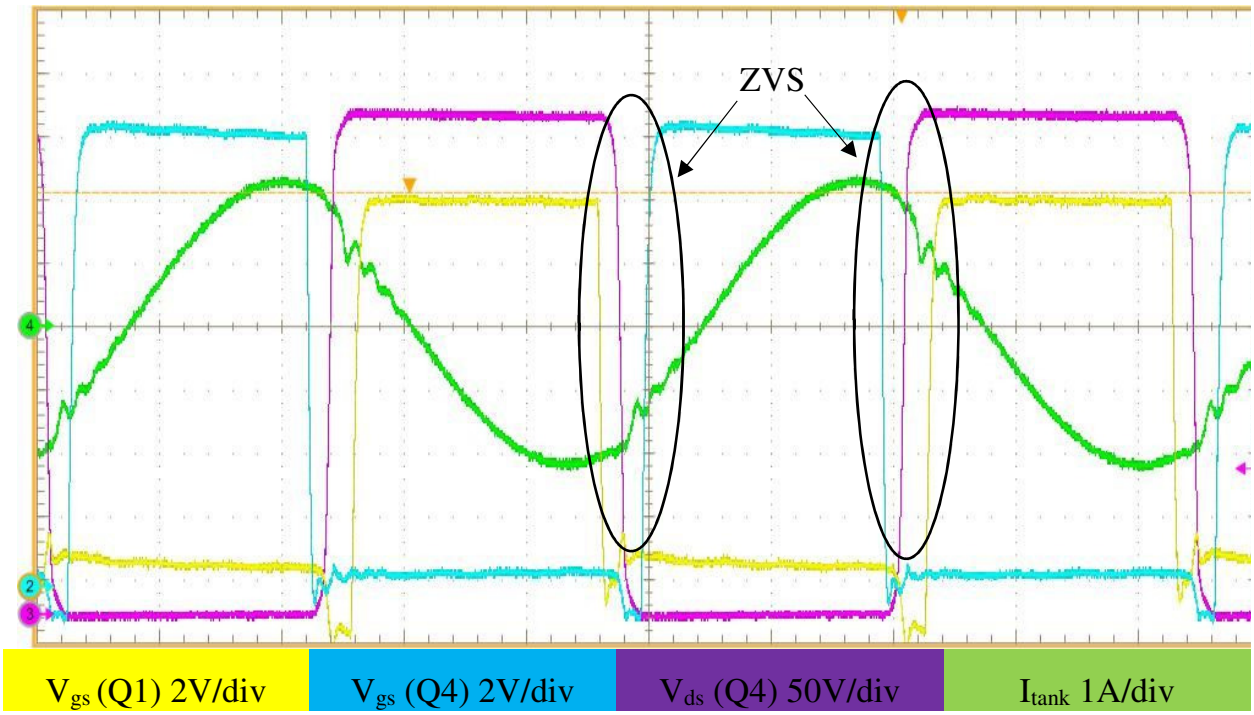



Figure 4.17 - Primary waveforms at 24V and 6.75A output (1µs/div)

In figure 4.20 and 4.22, the time difference between turn off for one gate signal and turn on for the other gate signal is approximately 650 ns. This time difference shows the 400 ns dead time between primary gate signals in addition to 250 ns turn on delay, which proves that the on time is controlled by the corresponding primary side gate signal.

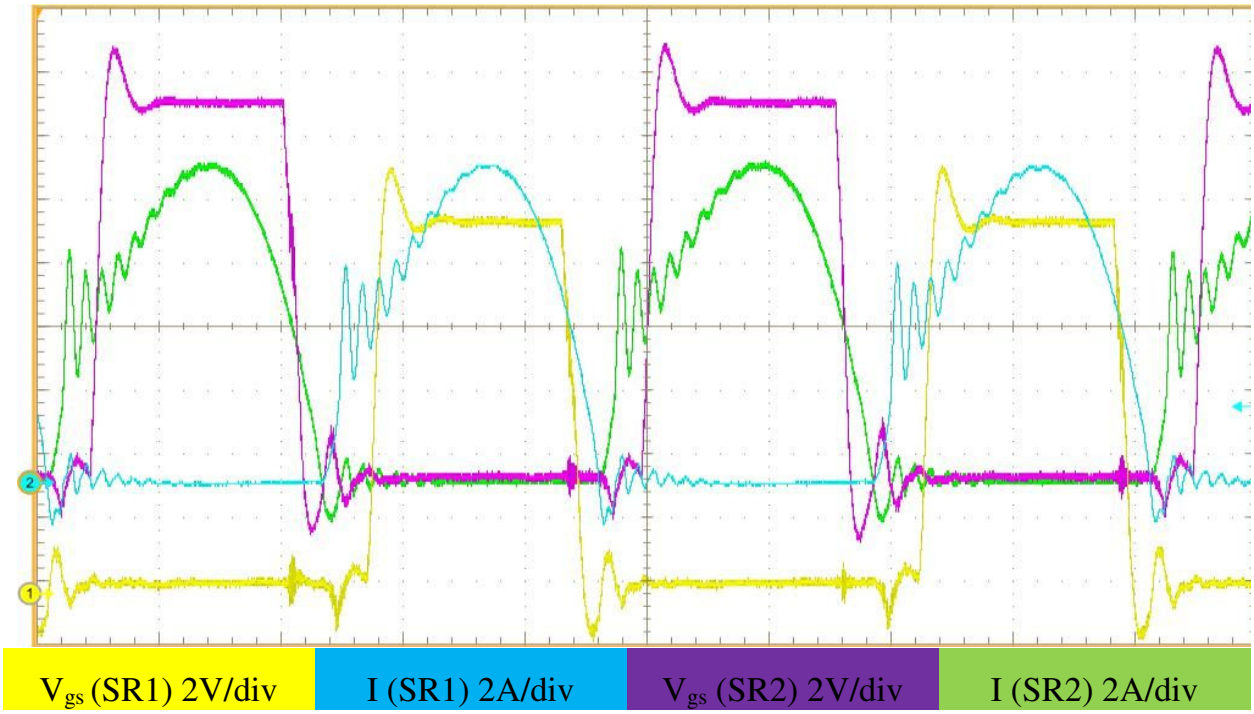



Figure 4.18 - Secondary waveforms at 24V and 6.75A output (1µs/div)

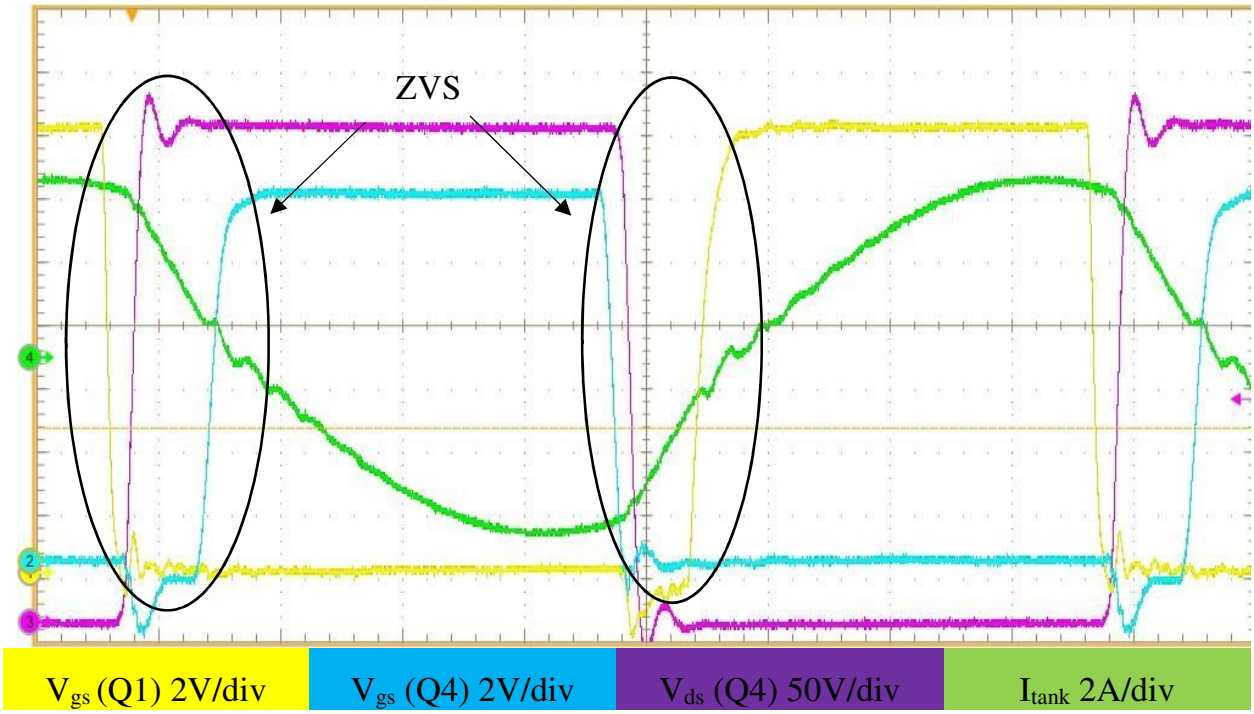



Figure 4.19 - Primary waveforms at 18V and 27A output (500 ns/div)

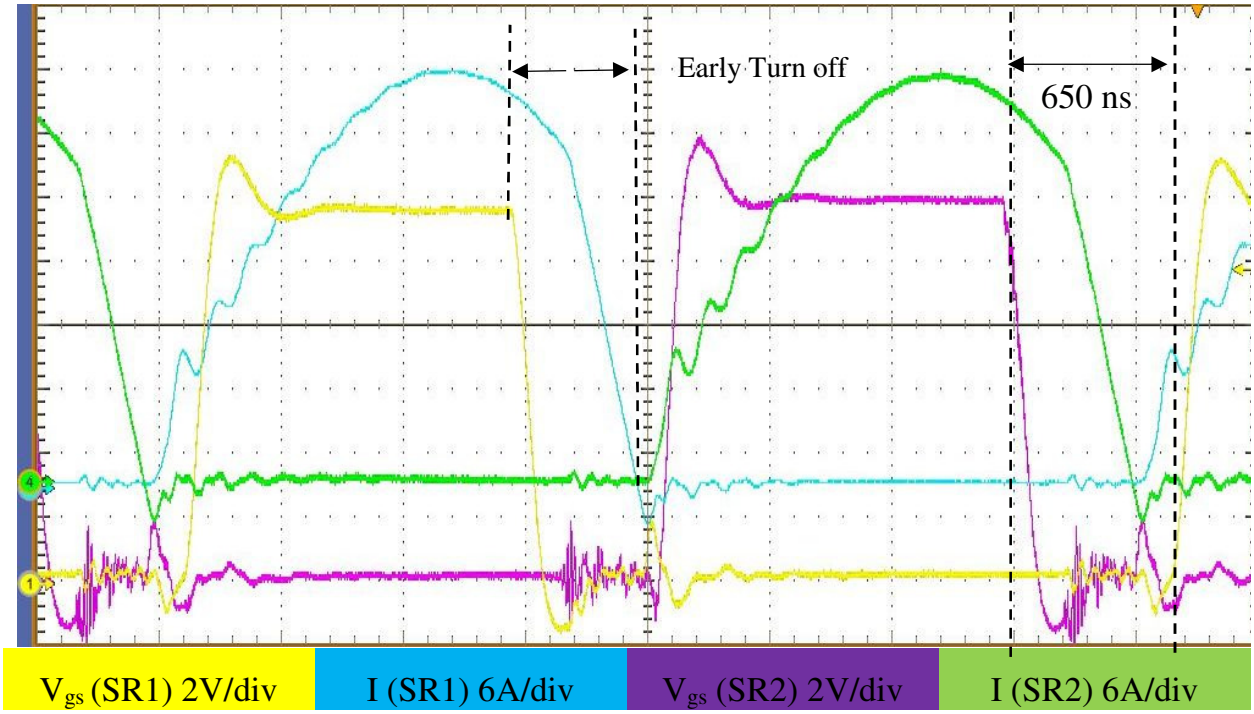



Figure 4.20 - Secondary waveforms at 18V and 27A output (500 ns/div)

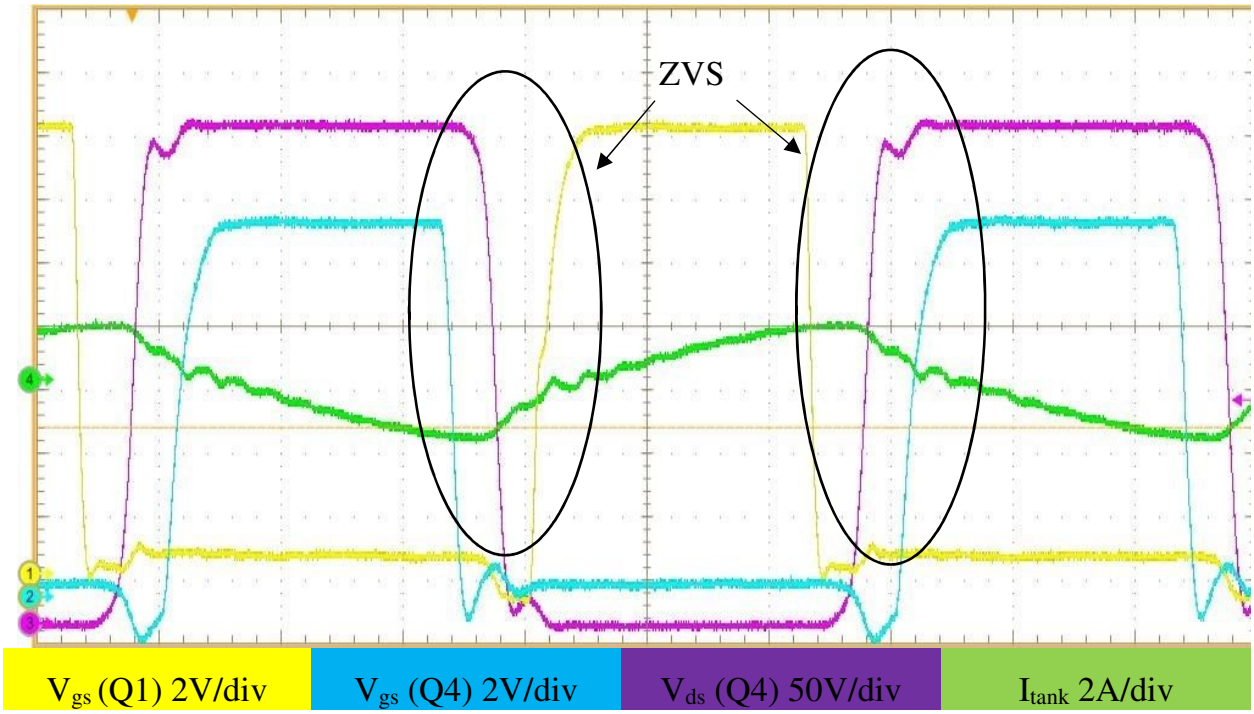



Figure 4.21- Primary side waveforms at 18V and 6.75A output (500 ns/div)

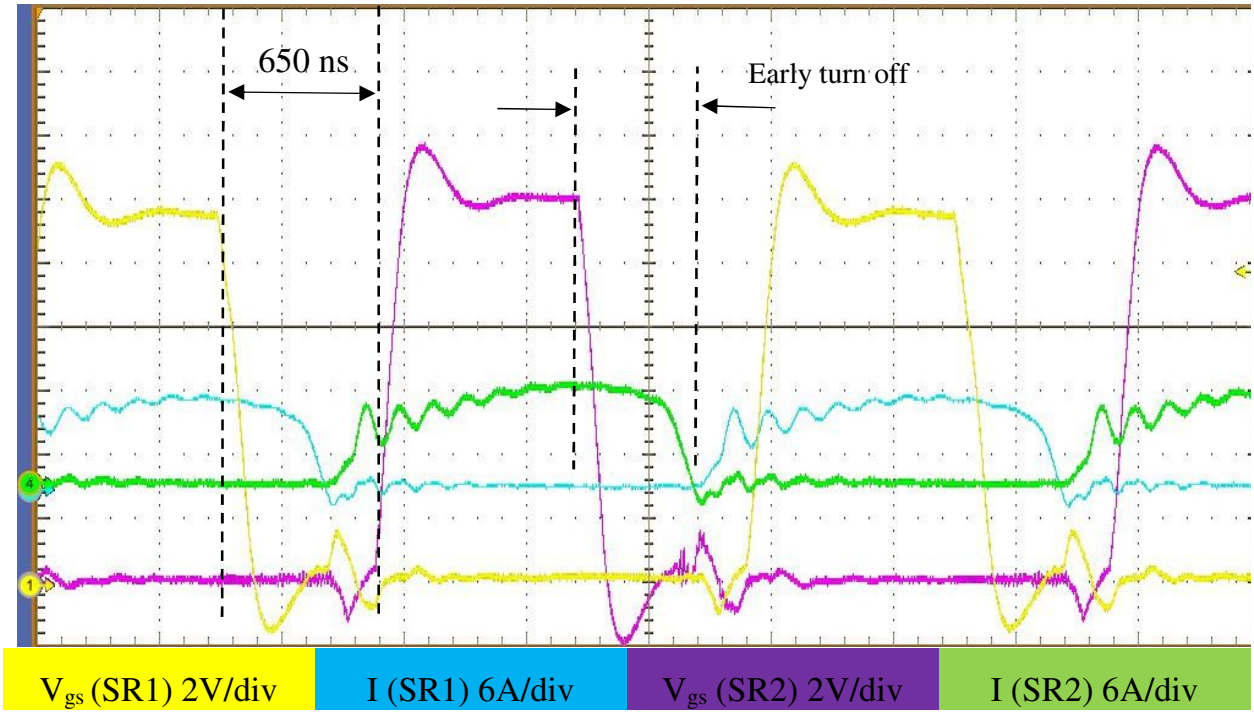



Figure 4.22 - Secondary side waveforms at 18V and 6.75A output (500 ns/div)

Figure 4.23 shows the efficiency results for 36V output condition. The efficiency is maximized at 50% loading for both diode conduction and synchronous rectification. The efficiency is enhanced by 1.23% at 13.5A output. In this case, the SR unit should be turned off below 25% loading. Below this point, the gate drive loss eliminates the synchronous rectification benefit.

Figure 4.24 shows the efficiency results for 24V output condition. The efficiency is maximized at 50% loading for both diode conduction and synchronous rectification. The efficiency is enhanced by 1.75% at 13.5A output.

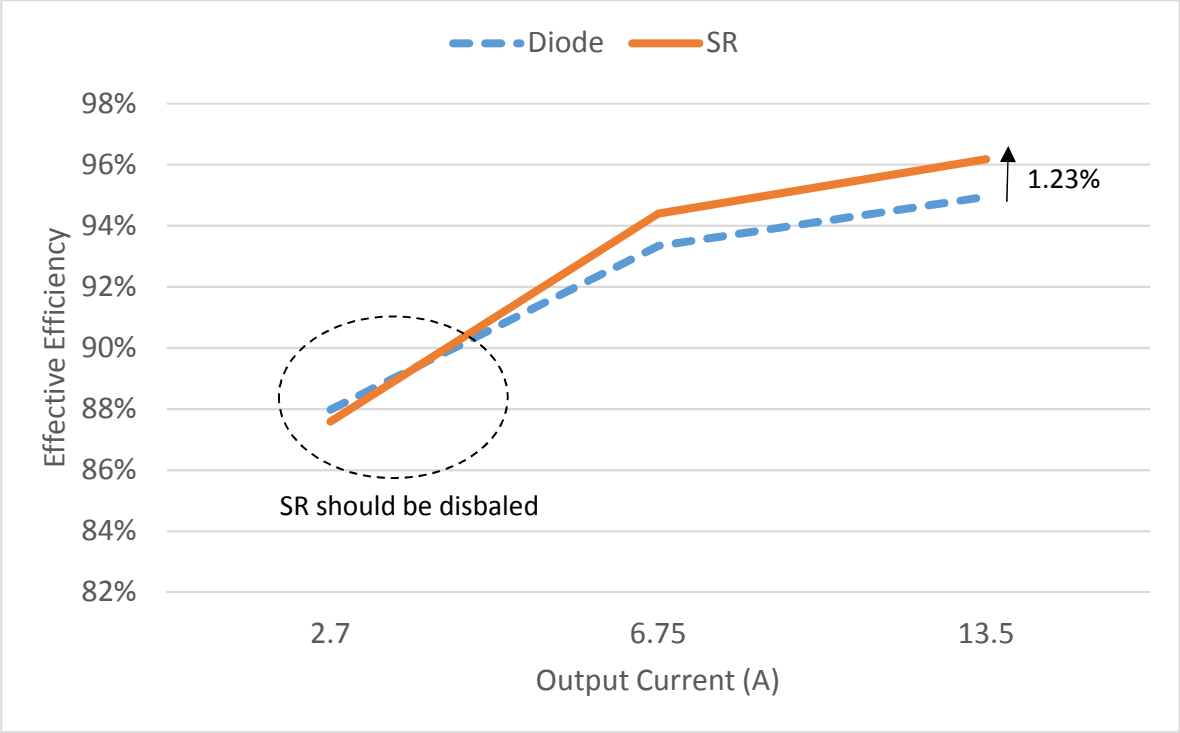



Figure 4.23 - Efficiency comparison between SR and body diode conduction for 36V output

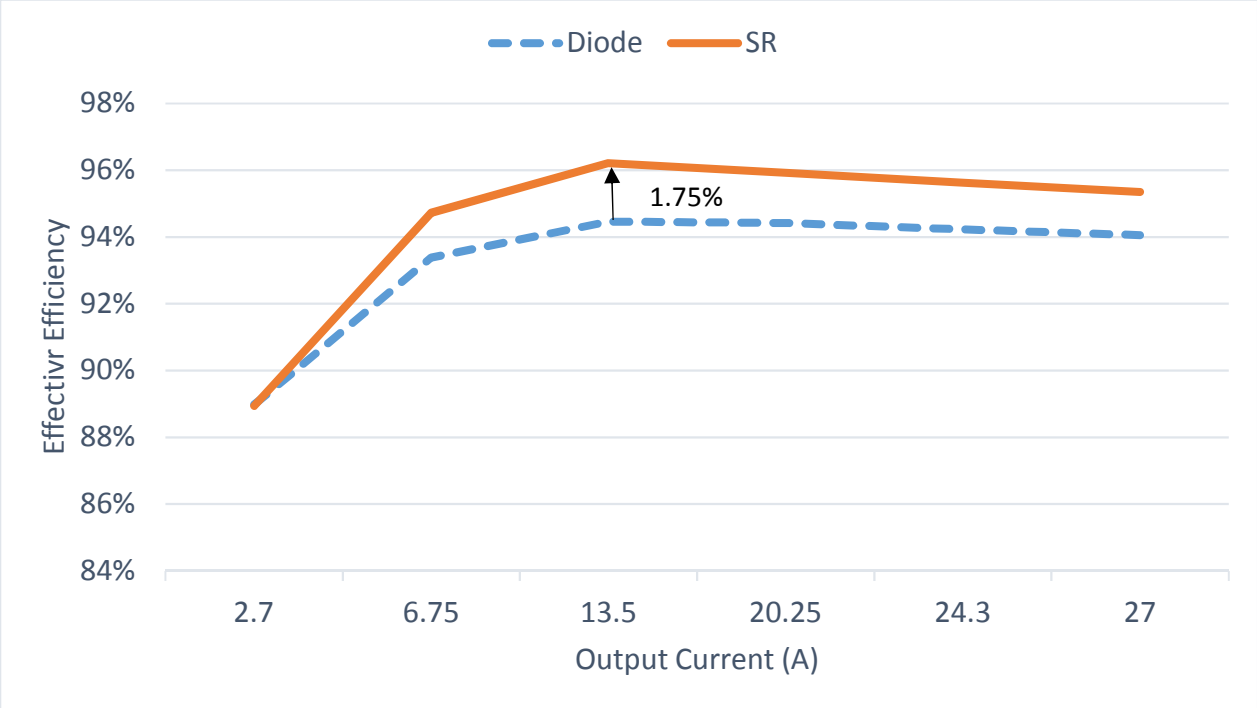



Figure 4.24 - Efficiency comparison between SR and body diode conduction for 24V output

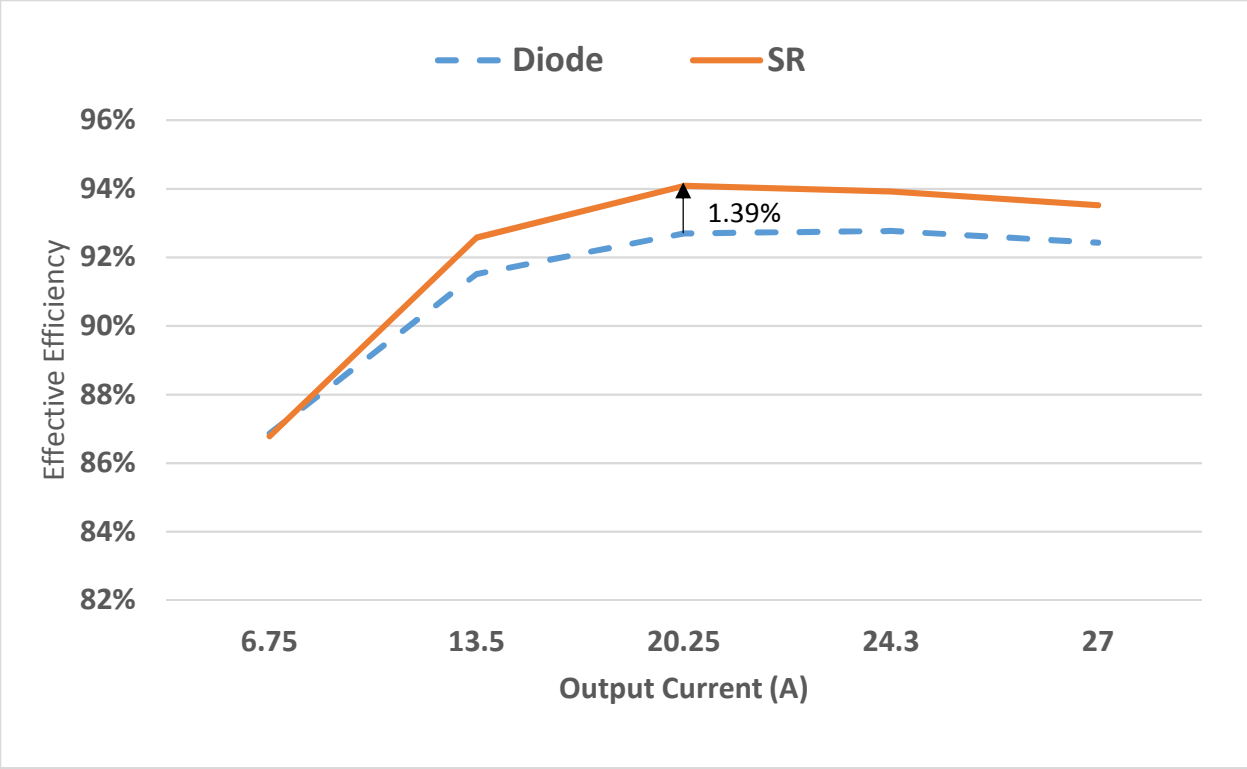



Figure 4.25 - Efficiency comparison between SR and body diode conduction for 18V output

Figure 4.25 shows the efficiency results for 18V output condition. The efficiency is maximized at 50% loading for both diode conduction and synchronous rectification. The efficiency is enhanced by 1.39% at 13.5A output. The efficiency boost is smaller in this output voltage level. This is due to non-optimum turn off moments at this voltage level.

In 24V and 18V cases, the efficiency drops after 13.5A, which shows that after the point the conduction loss in secondary MOSFETs becomes dominant in the efficiency of the converter. Paralleling MOSFETs at the secondary side will help increase the efficiency in heavy loading condition as well.

## 4.5. Summary

In this chapter performance of ICE2HS01G controller for battery charging application was evaluated. With the help of a thorough understanding of battery charging requirement. We were able to modify the control setting and expand the application of this controller to wide output range LLC converters.

Experimental result show that the converter operates safely in all of the output voltage and current conditions. Additionally, efficiency results show up to 1.75% efficiency increase compared to body diode conduction. However, the performance of the converter in below resonant frequency is not optimum and can be improved by other synchronous rectification techniques.

# Chapter 5 Conclusion and Future Works

## 5.1. Overview

This chapter presents a summary of the topics covered in this research. It also provides information on possible future research work that can be done based on the results in this thesis.

## 5.2. Overview of the Thesis

LLC resonant converters are widely used in battery chargers for electric vehicles. These converters take advantage of soft switching techniques and have high power efficiency. Reducing the conduction loss in these converters will help manufacturers increase the power rating of their converters. This will result in development of rapid high power chargers that expand the application of electric powered vehicles.

Synchronous rectification in LLC resonant converts can significantly reduce the conduction loss and increase the efficiency of these converters. In chapter, 2 the operation of resonant converters and specifically LLC resonant converters were explained in detail. The chapter presented recently proposed control methods for the primary side MOSFETs in LLC resonant converters, as well as synchronous rectification methods.

Chapter 3 illustrated the requirement of a LLC resonant converter to be used in battery chargers. In this chapter, complete design process of a 650W LLC resonant converter with 24V rated output voltage was explained. Additionally, the main features of

ICE2HS01G controller are briefly explained. Based on the requirement of the LLC resonant converter and features of ICE2HS01G, control settings suitable for wide operating range of the LLC converter are proposed in this chapter.

Chapter 4 presented the stress calculation and part selection for the experimental prototype. Additionally, technical design considerations were briefly mentioned and the experimental waveforms from the primary and secondary side of the converter were presented.

Experimental result showed that the converter operates safely in all of the output voltage and current conditions. Additionally, efficiency results showed up to 1.75% efficiency increase compared to body diode conduction. However, the performance of the converter in below resonant frequency was not optimum and can be improved by other synchronous rectification techniques.

## 5.3. Future Work

In this research, the application of an analog controller for LLC resonant converter was expanded to wide output voltage applications. The controller had a good performance in all of the operating conditions. However, a few non-adjustable settings prevented the converter to have optimum performance in below resonance region.

Modifying other analog solutions or investigating the application of digital synchronous rectification methods in battery charging application is an interesting topic for future research work. Efficiency boost utilizing other synchronous rectification

methods can be compared with the efficiency boost of this modified analog solution in future research work.

# References


[1] S. S. Williamson, A. K. Rathore and F. Musavi, "Industrial Electronics for Electric Transportation: Current State-of-the-Art and Future Challenges," *IEEE Transactions on Industrial Electronics,* vol. 62, *(5),* pp. 3021-3032, 2015.

[2] Laszlo Balogh, "Fundamental of MOSFET and IGBT Driver Circuit Application Report". SLUA618, Texas Instrument, Dallas Texas, March. 2017.

[3] D. Hart, "Resonant converters," in *Power Electronics*Anonymous New York: McGraw Hill, 2011, .

[4] F. Musavi *et al*, "An LLC Resonant DC–DC Converter for Wide Output Voltage Range Battery Charging Applications," *IEEE Transactions on Power Electronics,* vol. 28, *(12),* pp. 5437-5445, 2013.

[5] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Transactions on Power Electronics,* vol. 3, *(2),* pp. 174-182, 1988.

[6] Jee-hoon Jung and Joong-gi Kwon, "Theoretical analysis and optimal design of LLC resonant converter," in *Power Electronics and Applications, 2007 European Conference On,* 2007, pp. 1-10.

[7] B. H. Lee *et al*, "Analysis of LLC resonant converter considering effects of parasitic components," in *Telecommunications Energy Conference, 2009. INTELEC 2009. 31st International,* 2009, pp. 1-6.

[8] H. Choi, "Analysis and design of LLC resonant converter with integrated transformer," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE,* 2007, pp. 1630-1635.

[9] J. H. Kim *et al*, "Analysis for LLC resonant converter considering parasitic components at very light load condition," in *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference On,* 2011, pp. 1863-1868.

[10] P. Kowstubha, K. Krishnaveni and K. Ramesh Reddy, "Review on different control strategies of LLC series resonant converters," in *Advances in Electrical Engineering (ICAEE), 2014 International Conference On,* 2014, pp. 1-4.

[11] F. Musavi *et al*, "Control Strategies for Wide Output Voltage Range LLC Resonant DC–DC Converters in Battery Chargers," *IEEE Transactions on Vehicular Technology,* vol. 63, *(3),* pp. 1117-1125, 2014.

[12] W. Feng *et al*, "LLC resonant converter burst mode control with constant burst time and optimal switching pattern," in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE,* 2011, pp. 6-12.

[13] K. Colak, E. Asa and D. Czarkowski, "Dual closed loop control of LLC resonant converter for EV battery charger," in *Renewable Energy Research and Applications (ICRERA), 2013 International Conference On,* 2013, pp. 811-815.

[14] C. Buccella *et al*, "Observer-Based Control of *LLC* DC/DC Resonant Converter Using Extended Describing Functions," *IEEE Transactions on Power Electronics,* vol. 30, *(10),* pp. 5881-5891, 2015.

[15] E. Asa *et al*, "PLL control technique of LLC resonant converter for EVs battery charger," in *Power Engineering, Energy and Electrical Drives (POWERENG), 2013 Fourth International Conference On,* 2013, pp. 1382-1386.

[16] Z. Hu, Y. F. Liu and P. C. Sen, "Bang-Bang Charge Control for LLC Resonant Converters," *IEEE Transactions on Power Electronics,* vol. 30, *(2),* pp. 1093-1108, 2015.

[17] Xuefei Xie *et al*, "A novel high frequency current-driven synchronous rectifier applicable to most switching topologies," *IEEE Transactions on Power Electronics,* vol. 16, *(5),* pp. 635-648, 2001.

[18] D. Huang, D. Fu and F. C. Lee, "High switching frequency, high efficiency CLL resonant converter with synchronous rectifier," *Proc.IEEE ECCE,* pp. 804-809, 2009.

[19] X. Wu *et al*, "A New Current-Driven Synchronous Rectifier for Series–Parallel Resonant () DC–DC Converter," *Industrial Electronics, IEEE Transactions On,* vol. 58, *(1),* pp. 289-297, 2011.

[20] S. Abe *et al*, "Adaptive driving of synchronous rectifier for LLC converter without signal sensing," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE,* 2013, pp. 1370-1375.

[21] Dianbo Fu *et al*, "An improved novel driving scheme of synchronous rectifiers for LLC resonant converters," in *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE,* 2008, pp. 510-516.

[22] D. Wang and Y. F. Liu, "A Zero-Crossing Noise Filter for Driving Synchronous Rectifiers of LLC Resonant Converter," *IEEE Transactions on Power Electronics,* vol. 29, *(4),* pp. 1953-1965, 2014.

[23] "Adaptive synchronous rectification control circuit and method thereof,"L. Chen, T. Liu, H. Gan and Ying j., US7495934 B2L. Chen, T. Liu, H. Gan and Ying j., "Adaptive synchronous rectification control circuit and method thereof," US7495934 B2, 2009.

[24] W. Feng *et al*, "A Universal Adaptive Driving Scheme for Synchronous Rectification in LLC Resonant Converters," *IEEE Transactions on Power Electronics,* vol. 27, *(8),* pp. 3775-3781, 2012.

[25] C. Fei, F. C. Lee and Q. Li, "Digital implementation of adaptive synchronous rectifier (SR) driving scheme for LLC resonant converters," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC),* 2016, pp. 322-328.

[26] H. Choi, "Dual edge tracking control for synchronous rectification (SR) of LLC resonant converter," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC),* 2015, pp. 15-20.

[27] C. Duan *et al*, "Design of a 2.5-kW 400/12-V High-Efficiency DC/DC Converter Using a Novel Synchronous Rectification Control for Electric Vehicles," *IEEE Transactions on Transportation Electrification,* vol. 1, *(1),* pp. 106-114, 2015.

[28] Yilei Gu, Zhengyu Lu and Zhaoming Qian, "Three level LLC series resonant DC/DC converter," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE,* 2004, pp. 1652 Vol.3.

[29] Infineon Technologies, "ICE2HS01G High Performance Resonant Mode Controller Datasheet", Rev 2.1, Munich Germany, May 11, 2010.

[30] Infineon Technologies, "Design Guide for LLC Converter with ICE2HS10G Application Note", Rev 1.0, Munich, Germany, July 06, 2011.

[31] Infineon Technologies, "650V Cool MOS Team CFD2 Power Transistor IPx65R110CFD Datasheet", Rev 2.6, Munich Germany, Aug 11, 2011.

[32] Infineon Technologies, "Optimus Team 5 Power Transistor 100V, BSC035N10NS5 Datasheet", Rev 2.0, Munich, Germany, Dec 17, 2014.