UNDERSAMPLED DIFFERENTIAL PHASE SHIFT ON-OFF KEYING FOR OPTICAL CAMERA COMMUNICATIONS WITH PHASE ERROR DETECTION

by

NIU LIU

B.Eng., Nanjing University of Aeronautics and Astronautics, P. R. China, 2010 M.Eng., Lanzhou University, P. R. China, 2012

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The undersigned certify that they have read, and recommend to the College of Graduate Studies for acceptance, a thesis entitled: UNDERSAM-PLED DIFFERENTIAL PHASE SHIFT ON-OFF KEYING FOR OPTICAL CAMERA COMMUNICATIONS WITH PHASE ERROR DETECTION submitted by NIU LIU in partial fulfilment of the requirements of the degree of MASTER OF APPLIED SCIENCE

Julian Cheng, Faculty of Applied Science/School of Engineering Supervisor, Professor (please print name and faculty/school above the line)

Ayman Elnaggar, Faculty of Applied Science/School of Engineering Supervisory Committee Member, Professor (please print name and faculty/school above the line)

Jonathan Holzman, Faculty of Applied Science/School of Engineering Supervisory Committee Member, Professor (please print name and faculty/school above the line)

Zheng Liu, Faculty of Applied Science/School of Engineering University Examiner, Professor (please print name and faculty/school above the line)

External Examiner, Professor (please print name and faculty/school above the line)

December 19, 2016 (Date Submitted to Grad Studies)

Additional Committee Members include:

(please print name and faculty/school above the line)

(please print name and faculty/school above the line)

Abstract

This thesis introduces the design and implementation of an optical camera communication (OCC) system. Phase uncertainty and phase slipping caused by camera sampling are the two major challenges for OCC. In this thesis, we propose a novel modulation scheme to overcome these problems. The undersampled differential phase shift on-off keying is capable of encoding binary data bits without exhibiting any flicker to human eyes. The phase difference between two consecutive samples conveys one-bit information which can be decoded by a low frame rate camera receiver. Error detection techniques are also introduced in the thesis to enhance the reliability of the system. Furthermore, we present the hardware and software design of the proposed system. This low-cost communication system has been implemented with a Xilinx FPGA and a Logitech commercial camera. Experimental results demonstrate that a bit-error rate of 10^{-5} can be achieved with 7.15 microwatts received signal power over a link distance of 15 centimeters.

Preface

This thesis is original, unpublished, independent work by the author, Niu Liu.

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List of Acronyms

Acronyms	Definitions
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ADC	Analog-to-Digital Converter
AR	Augmented Reality
BER	Bit-Error Rate
bps	Bits Per Second
CCD	Charge Coupled Device
CFF	Critical Flicker Frequency
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DPSK	Differential Phase-Shift Keying
FPGA	Field-Programmable Gate Array
FSM	Finite State Machine
HDL	Hardware Description Language
I2V	Infrastructure-to-Vehicle
I/O	Input/Output

ITS	Intelligent Transport Systems
LED	Light Emitting Diode
MIMO	Multiple-Input Multiple-Output
OOK	On-Off Keying
PAM	Pulse Amplitude Modulation
PAR	Project Authorization Request
PIN	Positive-Intrinsic-Negative
RTL	Register-Transfer Level
PSK	Phase-Shift Keying
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
UDPSOOK	Undersampled Differential Phase Shift On-Off Keying
UFSOOK	Undersampled Frequency Shift On-Off Keying
UPSOOK	Undersampled Phase Shift On-Off Keying
VICS	Vehicle Information and Communication System
VLC	Visible Light Communication
VLCC	Visual Light Communication Consortium
V2I	Vehicle-to-Infrastructure
V2V	Vehicle-to-Vehicle

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Chapter 1

Introduction

1.1 Background and Motivation

Visible light communication (VLC) is a data communication technology based on the visible light spectrum (between 400 and 800 THz), which is traditionally used for illumination. The history of using visible light for communication dates back to thousands of years ago when ancient Chinese people used beacon towers on the Great Wall to deliver military information. In 1867, Captain Philip Colomb invented signal lamps, which employed different flashing patterns to communicate over a long distance. On June 3rd 1880, Alexander Graham Bell transmitted the world's first VLC message on his invention, the "Photophone" [1]. During World War I, German army used optical Morse transmitters as a secure communication technique, since wired communication was often cut off [2]. Even though radio frequency (RF) had a dominant position in the past 100 years, a great deal of effort has been made towards VLC. It is widely believed that VLC has great potential to be a complementary technology for RF communication.

In recent years, with the increasing concerns regarding energy consumption and environmental protection, the light emitting diode (LED) has become the choice for sustainable illumination. LEDs are now gradually taking the place of incandescent lamps. This green technology offers more brightness, lower energy consumption, and longer lifespan, making it well-suited for architectural decoration, traffic control, general lighting etc.

The development of illumination technology offers great opportunities for transmitting data by LEDs. Relevant research originated in Japan around 2003 with the establishment of the Visual Light Communication Consortium (VLCC). After that, VLC has been attracting growing interest worldwide.

In comparison with RF communication, VLC is more friendly to the environment. Using an illumination device for communication can reduce energy consumption and greenhouse emissions. It is estimated that by replacing all the existing lighting sources with LEDs, the world electricity energy consumption can be dramatically reduced by 50% [3]. Another motivation to use VLC is the increasing demand for high-speed wireless connectivity. With the emergence of smart devices, the requirement for big data transfer is growing exponentially. VLC can be a complementary technology for traditional wireless communication systems in many application scenarios.

1.1.1 Applications of VLC

VLC technology applies to a number of scenarios. Some applications of VLC are described as follows.

Indoor Communication: Nowadays, as people are carrying multiple wireless devices, WiFi has become a necessity in every step of our lives. Internet service users demand not only faster communication speed, but also better connection quality, especially for high-definition videos and real-time online games. When it comes to urban areas or an office building, where users tend to spend most of their time indoors, VLC is a powerful technique to enhance the capacity of the existing network infrastructure. Figure 1.1 illustrates a typical indoor VLC environment. LED bulbs provide internet access to laptops, smart phones, TVs and other devices. In this case, VLC can either perform as a complement to WiFi networks, or provide wireless connections independently when other communication links are not available.



Figure 1.1: Indoor VLC.

Inter-Vehicle Communication: The concept of intelligent transport systems (ITS) has been proposed in recent years. It aims at improving road utilization and providing innovative services to traffic participants [4]. The key approach is to establish wireless connectivity between vehicles and road infrastructure such as traffic lights, speed limit signs, and electronic road pricing gantries etc. In Japan, a vehicle information and communication system (VICS) was developed as an application of ITS [5]. Real-time traffic information was broadcasted by infrared beacons and radio beacons installed on road shoulders [6]. Such a communication system is of high cost and consumes huge quantities of electric energy. Nowadays, LEDs are widely used in automotive headlights and traffic signals as an energy-saving and reliable light source. As shown in Fig. 1.2, VLC is adopted for vehicle-tovehicle (V2V), vehicle-to-infrastructure (V2I) and infrastructure-to-vehicle (I2V) communications. Traffic and weather information can be efficiently broadcasted via traffic lights and billboards. Collision avoidance systems can also be implemented by setting up VLC links between vehicles.



Figure 1.2: A VLC application.

Wireless Communication in Hospitals: Modern medical communities are equipped with a variety of state-of-the-art technology. Medical equipment is critical to our healthcare delivery system. However, diagnostic and treatment devices are sensitive to radio wave signals. Some of these devices rely on WiFi and cellular networks to transfer vital data, which could be interfered by nearby RF communications. Thus, there are certain areas in the hospital where wireless communication devices are strictly forbidden. As a reliable solution to the electromagnetic interference problem [7], VLC works in the range of the visible light frequency spectrum and does not interfere with other electrical equipment.

Information Display and Communication: LEDs are used extensively in building decoration and advertising. Those billboards, which are often made up of hundreds of LEDs, are perfect VLC transmitters [8]. For example, the outdoor sign of a restaurant may send food menus to pedestrians, and a department store may wish to push new electronic coupons to potential buyers. In this situation, a camera from the user's cellphone could be used as a VLC receiver. By detecting the intensity change of the outdoor LEDs, customers are able to receive promotion messages without entering a grocery store or a shopping center.

Toys and Entertainment: Another interesting application is that VLC can be used in toys, theme parks, and public entertainment facilities. Toy manufacturer Disney [9] has already devoted itself to connecting toys to smart devices wirelessly via LEDs. Existing light sources in theme parks also provide ample opportunities for using VLC as part of the tourist location system and entertainment networks [10]. Since high-speed data communication is not required for this application, hardware and communication protocols have lower complexity than the aforementioned applications.

1.1.2 Motivation

VLC systems can be divided into two categories by different types of receivers: non-imaging receiver and imaging receiver. Non-imaging receivers are widely used in VLC systems. For example, photodiode receivers are often employed when high data rate or high sensitivity is required, and for a bidirectional communication system requiring low complexity and low cost, an LED can be simply used for both transmission and reception [11]. However, researchers have shown the limitations of non-imaging receivers. It has been proved that imaging receivers can provide better performance when multiple LEDs are deployed [12].

An imaging receiver, namely an image sensor, which consists of hundreds of photodiodes (i.e. pixels), is also capable of receiving data from LEDs by taking continuous images. Nowadays cameras can be found not only on laptops and tablets but also in wearable devices such as smartwatches and smart glasses. Optical communications for cameras (OCC) is proposed in recent years to employ these embedded cameras as VLC receivers. For instance, in grocery stores, product information and coupons can be easily obtained by a smartphone camera or an image sensor installed on shopping carts. Since no expensive hardware is required, camera receivers have shown advantages over photodiodes in many applications.

However, challenges and technical problems still exist for OCC. Firstly, the sample rate of a commercial camera is typically 30 frames per second (fps). As LED lighting flicker may induce biological human response, it is suggested that flickering in the 3 Hz to 70 Hz range should be avoided [13]. So a flicker-free OCC transmitter has to operate at frequencies that exceed the camera's frame rate, and the receiver has to undersample the transmitted signals, which cannot be easily reconstructed. In addition, the transmitters and the receivers are not strictly synchronized, and it is difficult to know the phase difference between the transmitted signal and the camera receiver, so the received on-off keying (OOK) waveform slowly slips with respect to the sampling point [14]. All OCC systems suffer from the phase slipping problem [14], which can cause more error bits and degenerate the system performance. For these reasons, demodulation of OCC is more challenging than that of non-imaging systems. The objective of this research is to develop a low-cost VLC system that uses camera receivers. The target system must realize data transmission without causing any LED flicker to human eyes. A new modulation technique for OCC needs to be proposed in order to overcome the phase uncertainty and phase slipping problems.

1.2 Literature Review

Smart devices have been changing our lives dramatically in the past decade. With the existing billions of devices that carry image sensors, it was proposed years ago that an image sensor can be used as a receiver for communication. In fact, as early as the year 2004, researchers from Japan [15] explored the possibility of using a camera as a VLC receiver. In the following years, cameras became popular in the topics related to intelligent traffic systems (ITS). For example, the authors in [16] and [17] proposed to establish connectivity between road infrastructure and vehicles via traffic lights and high-speed cameras, and the system was also known as I2V-VLC. The authors in [18] introduced V2V-VLC using tail lights and cameras equipped on vehicles.

Initiated in 2008 and completed in 2011, IEEE 802.15.7 was the first VLC standard. After years of waiting, there are few commercialized VLC products on the market. Some researchers [19] believed that this slow adoption was due to not taking image sensor communication into consideration in the standard. Due to the increasing popularity of portable smart devices, camera communication seems to be much closer to the market than photodiodes. More interest has been attracted to utilize embedded commercial cameras as VLC receivers [20].



Figure 1.3: Block diagram of a VLC system that uses image sensor receivers.

Considering camera data reception is a necessary and significant amendment to the VLC standard, a revision to 802.15.7 is currently being undertaken by a task group called IEEE 802.15.7r1 OWC TG. The name of OCC has been officially proposed in the IEEE P802.15.7 Project Authorization Request (PAR). This revision is expected to be published by 2018. Engineers are looking forward to extending OCC technology to billions of existing smart devices with the new VLC standard, without requiring any hardware modification.

Figure 1.3 shows the block diagram of a typical VLC system using LED transmitters and camera receivers. The data stream generated by the information source is modulated electrically by a modulator. In order to provide a constant quantity of power to the LED transmitters, an LED driver circuit is applied prior to the transmitters. A camera receiver captures the intensity

change of the LEDs at its frame rate. It converts the intensity into digital luminance values which are then demodulated by the demodulator.

The Nyquist-Shannon theorem states that to reconstruct an analog signal, the sampling rate should be at least two times its maximum frequency component [21]. Assuming that the frame rate of an image sensor is R_s , the frequency of the transmitted signal should be no greater than $R_s/2$ to avoid aliasing. To put it another way, if we have a camera receiver which samples at 30 fps, the corresponding transmitted carrier has an upper limit of 15 Hz in order to meet the sampling theorem. Operating at such a low frequency can be easily sensed by human eyes as flicker, which is not desirable in any OCC system. Another challenge for OCC is that the camera receiver samples at a fixed frame rate, which cannot be synchronized with the transmitters. This gives rise to an unknown sampling phase to the demodulator. For these reasons, a simple OOK modulation cannot be used in OCC systems. Several new modulation techniques have been proposed for OCC in recent years [22–26].

Undersampled frequency shift on-off keying (UFSOOK) [23] uses a pair of discrete OOK frequencies to transmit logic ones and zeros respectively. Different symbols present different patterns to the camera. The demodulator uses two image frames to decode one-bit information. Because of this, the bit rate could not exceed half of the camera sample rate. To be more specific, if UFSOOK is applied to a 30 fps camera receiver, the data rate was limited to 15 bits per second (bps).

The authors in [24] and [25] introduced pulse amplitude modulation (PAM) and quadrature amplitude modulation (QAM) into OCC. Image sensors are not linear devices. The operation of encoding and decoding luminance values, which is known as gamma correction, is nonlinear [27]. As

more than two amplitude levels are used in [24] and [25], the nonlinearity introduced by gamma correction had to be taken into consideration. Received images need to be compensated before demodulation in order to mitigate the non-linear effect. A special frame head sequence was introduced to detect the camera sample phase and obtain the gamma curve.

Undersampled phase shift on-off keying (UPSOOK) [26] is a dual-LED modulation technique that can reach a higher transmission speed. The modulation relies on different combinations of the ON/OFF status of two LEDs. Thus, the demodulator is required to know the exact sample phase of the camera. To do so, the authors designed a special frame head which is examined before every frame is demodulated. If an incorrect sample phase is detected, all sampled values in the same data frame have to be inverted.

OCC is sensitive to ambient light. Sunlight or other background noise could degrade the system performance. In addition, a disturbing problem that can increase the system bit-error rate (BER) for OCC is that the transmitters and receivers operate at asynchronous frequencies. To the best of our knowledge, only a small number of error detection techniques have been proposed for OCC. The authors in [14] proposed a space-time forward error correction scheme based on USFOOK when dimming control was required. Multiple-phase sampling was employed to detect and correct the erroneous sample phase. This requires the transmitter to repeat the same data frame three times, either spatially or temporally, which will reduce the communication efficiency.

1.3 Thesis Organization and Contributions

This thesis consists of six chapters. A summary of each chapter and its contributions are presented as follows:

In Chapter 1, we introduce necessary backgrounds and applications of VLC and OCC. As an attractive technology, VLC can be applied to a great number of application scenarios. We provide a comprehensive literature review of OCC in this chapter. The motivation and objective of this research are also stated.

In Chapter 2, essential technical background for this thesis is provided. We review some fundamental principles of image sensors as well as image sensor communication. After an overview of charge coupled device (CCD) image sensors and complementary metal oxide semiconductor (CMOS) image sensors, we briefly introduce the image sensor as a VLC receiver. The major challenges and requirements of designing an OCC system are also presented.

Chapter 3 focuses on the modulation and demodulation. A novel modulation scheme undersampled differential phase shift on-off keying (UDPS-OOK) is proposed to overcome the phase uncertainty problem and increase the data rate. The UDPSOOK demodulator does not need to know the sampling phase of the camera, and theoretically, it can double the data rate of UFSOOK. Furthermore, a novel error detection mechanism is proposed to help reduce the error bits caused by phase slipping. In addition, the data frame structure and multiple-input and multiple-output (MIMO) are discussed in Chapter 3.

Chapter 4 and Chapter 5 focus on the experiments. Chapter 4 describes the experimental setups for the proposed system. We discuss the finite state machine of the transmitter and the software flow chart of the receiver. Details of implementation are included in this chapter. Chapter 5 presents the experimental results. Data rates and received optical power are measured. It is shown that UDPSOOK has doubled the data rate of UFSOOK. The BER performance demonstrates that UDPSOOKED can effectively detect phase errors and can considerably enhance the reliability of UDPSOOK.

Finally, we summarize the thesis in Chapter 6 and suggest some future research work that may further improve the performance of the proposed camera communication system.

Chapter 2

Image Sensors and OCC

Nowadays image sensors are widely equipped in a variety of media, medical and other electronic devices. The applications for image sensors are changing rapidly. Drones, robots, vehicles and augmented reality (AR) are among the fastest growing market shares for image sensors. In addition, image sensors can also be used for communication purposes. In this chapter, we will give a brief introduction to CCD and CMOS image sensors as well as optical camera communications.

2.1 Image Sensors

An image sensor is a device that detects and conveys information of an optical image by converting attenuation of light waves into electrical signals. An image sensor contains an array of pixels. The size of the array varies from 100×100 (10,000 pixels) to 15700×18000 (2,826,000,000 pixels) [28]. Each pixel consists of a photodiode and a readout circuit. The readout circuit determines how fast camera capturing can be performed, i.e. the frame rate. For commercial cameras, it is typically 30 frame per second.

CCD and CMOS image sensors are the two major technologies for image capturing [29]. Both types are capable of converting light into electrical signals. These two technologies are comparable to each other in most respects. Neither of them has a compelling advantage over the other in image quality. However, as CMOS sensors cost less for fabrication and consume less power than CCD, they have been increasingly used in recent years. We will give a brief introduction to both of them.

2.1.1 CCD Image Sensors

In a CCD sensor, pixels are organized in a two-dimensional array. Charges are accumulated in each photosite when light strikes. Those charges must be transferred to a readout node before they get measured. A shift mechanism is used to sequentially transfer charges towards the readout stage where they are converted into voltages by an amplifier. As shown in Fig. 2.1, the transfer circuit functions similar to a shift register. Since the number of readout nodes is usually limited, the CCD is overshadowed by CMOS technology when it comes to the capturing speed.

2.1.2 CMOS Image Sensors

CMOS image sensors have a different readout structure. Each pixel in a CMOS image sensor has its own individual amplifier integrated inside. As shown in Fig. 2.2, at each photosite, there is a PD to carry out the photon-to-electron conversion along with extra circuitry to convert the charges immediately into a voltage. At the output stage, there is usually an analog-to-digital converter (ADC) so that the image sensor is able to output digital values. CMOS sensors allow parallel operations and provide much faster readout speeds at the cost of a higher complexity of circuit design. Nowadays, the CMOS sensor has become more popular than its competitor in the fast-growing market.



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2.2 Optical Communications for Cameras

2.2.1 Advantages of OCC

An image sensor consists of a lens and a two-dimensional PD array. As shown in Fig. 2.3, light first passes through a lens and then strikes a grid of photosites, where current has been generated. After the electron-to-voltage conversion, the luminance value of every pixel is obtained. In this way, a full image of the LEDs is presented. The image sensor refreshes all the pixels at a fixed frame rate.

When it comes to data transmission, a single PD receiver can achieve a higher data rate compared to a low frame rate image sensor. The readout time is mainly responsible for the relatively slow operation of the image sensor. Since no readout circuit is deployed, a single photodiode can obtain the output voltage more easily. However, there are also many competitive advantages of image sensor receivers.



Figure 2.3: A multiple-LED OCC system.

The most important advantage is that cameras are capable of receiving and processing data from multiple transmitters. The lens can spatially separate multiple transmitted signals. Having thousands and even millions of pixels, an image sensor is able to receive signals from multiple channels. So technically, each pixel can be modulated independently. As shown in Fig. 2.3, there are two LED transmitters in this OCC system sending different information simultaneously. The data is received in parallel even when two transmitters are using different modulation schemes.

Another great advantage of OCC is the ability to transfer visible light signals along with the position information. Every pixel has a row and column position, which can be used to identify itself. That means we can modulate the data by using the position information. Some VLC location and communication systems have been proposed using this feature [30],[31].

2.2.2 Design Requirements

The design of an OCC system is limited by many factors. For OCC transmitters, the modulation is subject to users' demand for illumination. For OCC receivers, the hardware should be no more than an unmodified commercial embedded camera [23]. As a consequence, an OCC system must meet the following requirements.

First, an OCC system cannot affect the illumination performance of LEDs. As a common light source in daily life, LEDs are required to exhibit stable intensity to users. It is well-known that images updating at a sufficiently high frame rate can appear steady. This rate is known as the critical flicker fusion rate (CFF) [32]. We are making good use of this important phenomenon everywhere in everyday life. Experiments have shown that the

maximum observable rate for humans is 50 to 90 Hz [33]. On the other hand, the camera's cutoff frequency ranges from 1/8000 to several seconds long [34], depending on the shutter speed setting. For an embedded commercial camera, the upper limit is in the vicinity of 1/1000 seconds. As a result, in order to avoid visible flicker to human eyes, the modulation frequency for OCC is in the range of 90 to 1,000 Hz.

Second, the receiver hardware must be a smartphone camera running at a common commercial frame rate, e.g. 30fps, since cellphones are scarcely equipped with extremely expensive high-speed cameras. As OCC aims at the commercial electronics market, a high frame rate receiver will absolutely narrow the market for this technology.

Moreover, OCC should offer accessible dimming control to users. When an intermittent light source has a frequency above the CFF, the Talbot-Plateau Law takes effect. It states that above CFF, a flash sequence is perceived as a steady light source which has the exact same average brightness as the former [35]. That is, assuming a 50% duty cycle is applied to an OOK signal, the LED will exhibit half intensity to human eyes. In other words, in order to offer controllable dimming levels to users, the OCC must be tolerant to any deviation from the designed duty cycle.

In the following chapters, we will discuss the design and implementation of such an OCC system.

2.3 Summary

In this chapter, we presented essential technical background knowledge for the entire thesis. CCD and CMOS image sensors were introduced. We also provided a brief description of optical camera communications. Finally, we discussed the design requirements of OCC systems.

Chapter 3

Modulation/Demodulation

In this chapter, a new modulation scheme termed undersampled differential phase shift on-off keying is proposed for OCC. The basic idea of UDPSOOK is to modulate binary bits by changing the phase difference between two consecutive frames. We also introduce an error detection technique to improve the bit-error rate of the system. The data frame structure of UDPSOOK is introduced at the end of the chapter.

3.1 UDPSOOK

To prevent human eyes from photobiological hazard, OCC systems are required to exhibit no flicker to users with different dimming requirements. As discussed in Chapter 2, the typical operation frequency of an OCC system is between 90 Hz and 1,000 Hz. Assuming the frame rate of a commercial camera is f_s and the frequency of the OOK square wave carrier is f_c , we can always find an integer n for UDPSOOK to ensure

$$f_c = n \times f_s, 90Hz < f_c < 1000Hz.$$
(3.1)

The transmitted UDPSOOK signal $s(t, \theta)$ can be expressed as

$$s(t,\theta) = sgn[\sin(f_c t + \theta)]$$
(3.2)

where f_c is chosen by (3.1), θ is the phase of the OOK carrier, and sign function is defined as follows:

$$sgn(x) = \begin{cases} 1 & x \ge 0 \\ 0 & x < 0 \end{cases}$$
 (3.3)

Every $1/f_s$ seconds the modulator changes the value of θ depending on the binary bit to be transmitted. A bit "1" is transmitted by adding 180° phase shift to the current signal, while a "0" is transmitted by adding 0° to θ . In other words, one bit of information is represented by a change of phase between two consecutive frames.

Figure 3.1 illustrates the modulated waveform of binary sequence "110". In the figure, we assume f_s is the camera sample rate and n = 4 so that $f_c = 4f_s$. Every frame consists of 4 cycles of the OOK carrier. Dashed lines represent $1/f_s$ seconds interval. The phase of the square waveform has been toggled twice in the first two $1/f_s$ seconds in order to transmit two logic ones. Similarly, the phase stays unchanged for the last frame to send a logic zero.

The red lines represent the sampling moments of the receiver. At the demodulator, received bits are determined by comparing the phase between two consecutive samples. The demodulation rule can be simply expressed as

$$\theta_k - \theta_{k-1} = \theta_\Delta = \begin{cases} 0 & \text{``0''} \\ \pi & \text{``1''} \end{cases}$$
(3.4)

where θ_k is the carrier phase of the *kth* sampling. This rule can be imple-




mented by using an exclusive OR operation as

$$b_{k-1} = s_k \oplus s_{k-1} \tag{3.5}$$

where s_k is the *kth* sampled value of the camera. We map s_k to "1" when the LED is on and s_k to "0" when the LED is off. The structure of the demodulator can be simplified as shown in Fig. 3.2.



Figure 3.2: UDPSOOK demodulation.



Figure 3.3: Different sampling timing for UDPSOOK.

UDPSOOK transmits signals by controlling the phases difference of two consecutive samples, so that n camera frames carry n-1 bits information. The theoretical maximum data rate R_{max} can be obtained by

$$R_{max} = f_s \times \lim_{n \to \infty} \frac{n-1}{n} = f_s \tag{3.6}$$

which has been doubled compared to the maximum achieved data rate in [23].

On the other hand, in a practical OCC system, it is difficult to predict the sampling phase of the camera. Fig. 3.3 is an example of camera sampling. In the figure the horizontal axis indicates the time. The time difference between two consecutive arrows with the same colour is $1/f_s$. As the sampling can occur at any position regarding the timeline, most modulation schemes [24–26] require extra algorithms to detect the phase relation between the camera sampling and the received signal waveforms. But UDPSOOK is totally immune from the camera phase uncertainty since the demodulation is based on the phase difference between two frames rather than when the camera sampling occurs. In Fig. 3.3, red arrows indicate one set of possible samples for the transmitted sequence "110". If the sampling takes place at the green positions, which have a π phase shift from the red arrows, the sampled values will be fully inverted. However, the UDPSOOK demodulator obtains the same bit sequence "110" from the green samples because the phase difference between two consecutive frames does not change.

UDPSOOK also supports dimming control. The LED brightness can be changed by increasing or decreasing the duty cycle of the OOK signal. A fixed 50% duty cycle is not practicable in reality. But for some OCC systems [23–25], non-50% duty cycle modulation is not feasible or causes improper sampling phases and hence more error bits. Assuming a logic one is transmitted by UFSOOK (Fig. 3.4(a)) and UDPSOOK (Fig. 3.4(b))



(a) non-50% duty cycle decoding for UFSOOK



(b) non-50% duty cycle decoding for UDPSOOK

Figure 3.4: Non-50% duty cycle demodulation

respectively, it is shown that UFSOOK is more likely to have an erroneous sampling result (green arrows) when the duty cycle is greater than 50%, but UDPSOOK can adapt to any different duty cycle.

Another problem introduced by image sensors is phase slipping. For a typical OCC system, as the receiver and the transmitter are not strictly synchronized, the sampling points are gradually slipping regarding the OOK waveforms. A sampling phase error occurs when a π phase shift comes. In our experiment, phase slipping is a major source of error bits.

3.2 UDPSOOK with Error Detection

As phase slipping degenerates the performance of OCC systems, we propose an error detection technique for UDPSOOK to reduce the system BER. In this proposed system, two LEDs are employed. We use one LED to accomplish data transmission and an extra LED to carry out error detection. The data transmission LED is a UDPSOOK transmitter as introduced in Chapter 3.1, and the error detection LED keeps sending bit "0"s during the data transmission. As an all "0" UDPSOOK bit sequence triggers no phase toggling on the LED, the demodulator expects to see no phase difference on received image samples. Since this LED suffers from the same channel noise and phase slipping problem, if any sampling error occurs, it can precisely indicate the incorrect samples by looking for a sudden phase change. Then the demodulator corrects the sampling errors by simply flipping the erroneous sampled values.

As shown in Fig. 3.5, the red arrows indicate a correct sampled sequence [ON, OFF], which is decoded as a bit "1". When a phase error occurs, the second red sampling point slips to the green arrow position and gives rise

to an incorrect sampled sequence [ON, ON], which will be decoded as a bit "0". This error can be observed by the receiver due to the phase change of the error detection LED. The demodulator will invert the second sampled value to get the correct decoded bit.



Figure 3.5: UDPSOOKED sampling

3.3 Framing Structure

In order to detect the start of a transmission, the UDPSOOK data is preceded by a start frame delimiter (SFD). An extra bit is added to the end of the payload for parity check to further enhance the system reliability. A data frame is shown in Fig. 3.6.

The SFD consists of two parts. The first part is a high-frequency OOK symbol that lasts for two frames. This high frequency is required to be greater than the cutoff frequency of the camera so that it can be recognized neither as a fully ON nor as a fully OFF. Instead, the camera extracts an





Figure 3.6: Frame structure of the proposed OCC system

average intensity information from it [23] and interprets this status as a half ON assuming a 50% duty cycle is used.

The second part of SFD for a data transmission LED is a UDPSOOK bit "1" (Fig. 3.6). If a logic "1" is not observed during the demodulation of an SFD, the data frame might have been corrupted and should be discarded. The error detection LED has a different second part of SFD. After the first $2/f_s$ seconds, it starts to transmit a bit "0", i.e. two frames of OOK signals which have identical phase. In this way, the SFD not only starts a frame but also helps the receiver distinguish between the two different functioning LEDs. If a receiver observes a logic "0" after the $2/f_s$ seconds half ON, it will recognize this LED as an error detection transmitter.

Following the SFD is the payload of the data frame. The data frame ends when the receiver detects another SFD. The last bit of a data frame is a parity bit used to detect the possible transmission errors. The receiver calculates the number of "1"s when a full data frame is received. When parity check fails, all the data in current frame will be discarded.

3.4 MIMO



Figure 3.7: A possible MIMO scheme for UDPSOOKED

UDPSOOKED doubles the overhead of a single LED OCC system by introducing an extra transmitter. However, multiple LEDs can share an error detection LED in a MIMO system. In this case, the efficiency can be significantly improved compared to the case with a single LED. Fig. 3.7 illustrates one of the possible MIMO schemes for UDPSOOKED. In the figure, LED 1 to LED 8 act as data transmission LEDs. Instead of using another 8 LEDs to accomplish error detection, a common LED (LED 9) is sufficient to offer a better quality of service. Those transmitters are required to operate at a synchronous frequency.

3.5 Summary

This chapter focused on the modulation and demodulation scheme of UDPSOOK. Two consecutive frames were used to determine one-bit information. By introducing an extra error detection transmitter, we were able to detect the phase slipping errors. UDPSOOKED applies when a highly reliable transmission link is required. MIMO and data frame structure were also discussed in this chapter.

Chapter 4

Experimental Setup

We provide details of our experimental setup in this chapter. At the transmitter, a Xilinx Virtex-7 field-programmable gate array (FPGA) modulates the low power consumption LEDs. At the receiver, images are captured by a Logitech 30 fps camera. Video frames have been recorded for demodulation and further performance evaluation.

4.1 Hardware Design

Figure 4.1 demonstrates our experimental setup. A Xilinx VC707 evaluation board is used to modulate information and carry out logical operations for transmitters. As shown in the figure, a breadboard provides connections between the evaluation board and the Digilent PmodLED LED module, which is powered by 2mA 3.3V FPGA input/output (I/O) pins. A camera receiver continually records videos on the other side. Image processing is then performed off-line in Matlab. We will introduce the transmitter and the receiver hardware in the following sections.

4.2 Transmitter

Figure 4.2 illustrates the block diagram of the transmitter. The data is initially stored in a read-only memory (ROM) created by the Xilinx Block



Figure 4.1: Experimental setup.

Memory Generator core. A parallel-to-serial converter fetches byte data from the memory and converts them into a serial bit stream. The modulator is responsible for generating the OOK carrier and encoding binary bits into UDPSOOK symbols. The modulated signals are then sent to an LED driver circuit which provides sufficient transmission power for driving the LEDs.



Figure 4.2: Block diagram of the transmitter.

4.2.1 Modulator

The modulation algorithm is implemented on a Xilinx Virtex-7 FPGA. A finite state machine (FSM) is designed to control the transmission process as shown in Fig. 4.3. When transmission starts, the modulator first sends a high frequency signal as part of the SFD. Followed is a UDPSOOK bit "1", i.e. two frames of OOK with π phase difference. The modulator then changes the phase of the carrier every $1/f_s$ seconds according to the next input bit. At the end of the transmission, a parity bit will be calculated and added to the end of the frame. This modulation FSM is implemented in Verilog hardware description language (HDL). Appendix A gives a small snippet of the FSM implementation. Xilinx Vivado Design Suite performs register-transfer level (RTL) synthesis and timing analysis etc., and the inbuilt simulator provides reliable behavioral verification before testing on hardware. The simulation result is shown in Fig. 4.4. An *enRead* pulse reads one bit from the memory and LED_En enables the I/O ports on and off according to the modulation rules. Note that the time scale has been shrunk by 1000 times to improve simulation efficiency and the figure only demonstrates the initial 300 us after reset.



Figure 4.3: The transmission control finite state machine.

4.2.2 LED Driver Circuit

The LED driver circuit is a power supply whose output may vary to match the electrical characteristics of the LEDs. We select the Digilent PmodLED LED module as our solution for transmitters. The PmodLED LED module integrates four high-bright monochrome red LEDs with the





Figure 4.4: The simulation results in Xilinx Vivado simulator.

necessary driver circuits. Those low power consumption LEDs can be driven by less than 1 mA current. The schematic of the LED driver circuit is shown in Fig. 4.5.

4.3 Receiver

At the receiver, videos are recorded by a Logitech Pro 900 camera. The camera is then connected to a PC where captured images are processed via MATLAB. Auto white balance and other optimization options need to be disabled. With proper configurations, the influence of ambient light can be reduced, so that the camera can identify the transmitted image with lower error rate.

After frames being sampled, we need to map the LED status into binary bits. Demodulation is performed on the sampled sequence. Fig. 4.6 explains the UDPSOOK demodulation algorithm. It starts with monitoring the first SFD, which indicates the beginning of a new data frame. After an SFD is found, the demodulator begins to compare two consecutive samples to determine the transmitted bit. This process repeats until the next SFD is





Figure 4.5: The PmodLED LED module [36].

detected. We have to check the parity bit before proceeding to the next data frame.

For UDPSOOKED, the algorithm presented in Fig. 4.6 needs to be performed on both LEDs. Assuming the decoded bit sequences on two LEDs are respectively $\{R_{d0}, R_{d1}, R_{d2}, \dots, R_{dk}\}$ and $\{R_{e0}, R_{e1}, R_{e2}, \dots, R_{ek}\}$, the final decoded sequence is given by

$$B_k = R_{dk} \oplus R_{ek}. \tag{4.1}$$

4.4 Summary

In this chapter, we introduced our experimental setups for the proposed OCC system. Hardware selection and software flow chart are described. We designed the transmitter and the receiver in a very inexpensive way in order



Figure 4.6: A flow chart of the UDPSOOK receiver.

to lower the entry barrier to the market. We will present the experimental results in Chapter 5.

Chapter 5

Experimental Results

In this chapter, we present the experimental results of the proposed OCC system. Data rates are given as well as the BER performance. The received optical power is also measured.

5.1 Received Optical Power

Before we quantify the system performance by measuring the BER, it is important to specify the experimental parameters. As the LED electrical power consumption is only on the order of mW, one of our central concerns is how much optical power has reached the camera. Fig. 5.1 shows the experimental setup used to measure the optical power at the receiver. In the figure, d is the transmission distance and f is the focal length of the one-inchdiameter lens. We employ a high-speed photodetector (Thorlabs DET36A) for the measurement. The voltage difference across the load resistor R_L is directly measured in the experiment. We select a $10M\Omega$ resistor since a low generated photocurrent can be expected. Table 5.1 gives the voltage results over three different transmission distances.

The responsivity curves of the selected photodetector can be obtained from the product specification as shown in Fig. 5.2 [37]. The PmodLED module only emits red light (wavelength in the vicinity of 650 nm), and



Figure 5.1: Optical power measurement setup.

Table 5.1: Received optical intensity for the proposed OCC system

Distance	Voltage	Current	Incident power	Intensity
15 cm	2.36 V	$2.36~\mu\mathrm{A}$	$7.15 \ \mu W$	$1.41 \ \mu W/cm^2$
50 cm	220 mV	22 nA	$66.67 \mathrm{~nW}$	$13.16nW/cm^2$
100 cm	$60.8 \mathrm{mV}$	6.08 nA	18.42 nW	$3.64 \ nW/cm^2$

accordingly, we select responsivity R = 0.33A/W. As the responsivity of a photodiode is defined as a ratio of the photocurrent to the incident light power at a given wavelength, to calculate the received optical power, we use

$$P_{inc} = \frac{I_{PD}}{R} \tag{5.1}$$

where P_{inc} is the incident power and I_{PD} is the photocurrent, which can be calculated from

$$I_{PD} = \frac{V_L}{R_L} \tag{5.2}$$

where V_L is the voltage across the load resistor R_L . The result is also shown in Table 5.1. As expected, the received power dramatically drops when we increase the transmission distance.

Furthermore, the area of a one-inch-diameter lens is $\pi \times (25.4mm/2)^2$, so the signal intensity at the receiver can be estimated. Over the distance



Figure 5.2: DET36A responsivity [37].

of 1 meter we have signal intensity

$$Int_{d=1m} = \frac{(P_{inc})_{d=1m}}{A} = \frac{18.42 \, nW}{\pi \times (25.4mm/2)^2} \approx 3.64 \, nW/cm^2.$$
(5.3)

Similarly, we can calculate the signal intensity for 15 cm and 50 cm, which is shown in Table 5.1. As the ambient intensity is on the order of $0.1nW/cm^2$ [38], we have approximately 10 dB of dynamic range.

5.2 BER and Bit Rate

The modulator has been implemented on a Xilinx VC707 Evaluation board. We use a logic analyzer to verify the modulated signals. The captured waveforms are shown in Fig. 5.3. The blue waveform represents the data transmission channel and the yellow waveform represents the error detection



5.2. BER and Bit Rate

Figure 5.3: Captured waveforms from the logic analyzer.

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channel. In the figure, a new data frame starts at 296 ms with a 66 ms 12 KHz high-frequency OOK. A bit "1" has been transmitted between 362ms and 429 ms on the blue channel as part of the SFD, which is followed by more UDPSOOK symbols. As we can see from the figure, there is no phase change on the error detection channel.

Then we use the modulated electrical signals to drive the LED circuits. Digilent PmodLED is a high-brightness LED module with low power requirements. In our experiment, for each LED the electrical power consumption is $3.30V \times 2.45mA = 8.10mW$.

At the receiver, videos have been recorded by a Logitech Pro 900 camera. The camera has been set up in a normal indoor environment with noise from sunlight outside of the room. We set the frame rate as 30 fps and all collected images are processed by MATLAB. In the experiment, the auto focus and auto white balance function of the camera are disabled. Key experimental parameters are shown in Table 5.2. We collect approximate 20,000 frames for each measurement. Fig. 5.4 demonstrates different LED status captured

	<u>*</u>
Parameter	Value
Camera frame rate	30 fps
Resolution	640×480
Saturation	0
LED DC offset	$1.65 { m V}$
LED peak-to-peak voltage	3.3 V

Table 5.2: Key experimental parameters

by our camera within a data transmission. On the left hand side is a data transmission LED and on the right hand side is an error detection LED. Fig.

5.4(c) reflects the status of both LEDs when they are modulated by the highfrequency signal in an SFD frame head, which can only be interpreted by its average intensity. Fig. 5.4(a) and Fig. 5.4(b) present the fully ON and fully OFF status of the data transmission LED respectively, which compose a UDPSOOK symbol "1". As one might expect, the status of the error detection LED stays unchanged during the bit transmission.







Figure 5.4: UDPSOOKED symbols captured by camera.

We have tested three different communication distances for both UDPS-OOK and UDPSOOKED. The BER results are shown in Table 5.3. It is suggested that UDPSOOK provides acceptable BER performance under all three distances considered, and UDPSOOKED can lower the BER efficiently, especially for the distances of 15 cm and 50 cm. The result also shows that when transmission distance increases, the system BER increases.

Table 5.5: Experimental results 1				
Distance	Modulation	BER		
15 cm	UDPSOOK	2.48×10^{-4}		
$15~\mathrm{cm}$	UDPSOOKED	4.96×10^{-5}		
50 cm	UDPSOOK	$4.25{ imes}10^{-4}$		
$50~{\rm cm}$	UDPSOOKED	6.08×10^{-5}		
1 m	UDPSOOK	8.15×10^{-3}		
1 m	UDPSOOKED	1.88×10^{-3}		

Table 5.3: Experimental results I

We have also implemented UFSOOK in the same experimental environment. The data rate comparison is shown in Table 5.4. The experimental results demonstrate that UDPSOOK has indeed doubled the data rate of UFSOOK as expected in Chapter 3.1.

Table 5.4: Experimental results II					
Distance	Modulation	Data Rate (bps)			
15 cm	UFSOOK	11.06			
15 cm	UDPSOOK	23.02			

Table 5.4: Experimental results II

5.3 Summary

In this chapter, we presented the experimental results of the proposed OCC system. The received optical power has been measured. By comparing the BER performance of UDPSOOK and UDPSOOKED, we can conclude that the second LED can efficiently enhance the reliability of the proposed system. The data rate has doubled compared to the UFSOOK system.

Chapter 6

Conclusions

In this chapter, we summarize the accomplished work and propose some future research topics.

6.1 Summary of Accomplished Work

In this thesis, we have proposed a novel modulation technique called UDPSOOK for OCC. By introducing this new scheme, the theoretical communication data rate has doubled compared with [23]. We have also designed an error detection scheme for UDPSOOK, i.e. to use a second LED as a detector of phase slipping errors. This method mitigates the asynchronization problem of OCC that other researchers are concerned with.

On the other hand, an experimental communication link has been established by using monochrome LEDs and an inexpensive commercial camera. Experiments have demonstrated that a BER of 10^{-5} has been achieved by such low overheads. Experimental work shows that UDPSOOKED can provide excellent robustness and reliability for OCC systems.

In Chapter 3, we proposed UDPSOOK and UDPSOOKED for OCC. We provided the details on modulation and demodulation. In order to reduce the BER of the system, an error detection LED was employed. A MIMO scheme was also introduced in this chapter. In Chapter 4, we introduced our experimental setups for the proposed OCC system. Both hardware selection and software flow chart were detailed. We have designed the transmitter and the receiver in a very inexpensive way in order to lower the entry barrier to the consumer electronics market.

Chapter 5 presented the experimental results of the proposed OCC system. By comparing the BER performance of UDPSOOK and UDPS-OOKED, we found the proposed error detection scheme can reduce the error bits efficiently. The communication data rate was doubled compared to UFSOOK systems.

6.2 Suggested Future Work

The low data rate is still the bottleneck for the OCC technology due to the relatively low frame rate of the receiver. However, there are still some approaches that we can use to improve the communication data rate. MIMO can be one of the major solutions. Another potential future initiative is to design a real-time OCC system. Currently, we use captured videos for demodulation in our experiments. In real use cases, users will be unsatisfied with the delay of video capturing. To this end, an easy-to-use smartphone application is necessary. How to select appropriate hardware for real-time OCC would be another interesting topic in the future.

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Appendix

Appendix A

To implement the FSM described in Chapter 4.2, we have the following code snippet. This is a three-always-block style Verilog DHL implementation with registered outputs, which is consistent with industry practice.

```
fsm for transimitter
****************************/
parameter TX_IDLE = 2'b00;
parameter TX_SFD = 2'b01;
parameter TX_MARK = 2'b10;
parameter TX_SPACE = 2'b11;
reg [1:0] TxPreStatus;
reg [1:0] TxNxtStatus;
always @ (TxPreStatus or isSFD or pCounter or Counter or
   fSize or Nxt_Bit)
begin
   case (TxPreStatus)
  TX_IDLE:
   begin
   TxNxtStatus = TX\_SFD;
   end
  TX_SFD:
   begin
   if(isSFD \& (pCounter = SFD_LEN - 1'b1)
  && (Counter == TMS_SFD -1'b1))
   TxNxtStatus = TX_MARK;
```

Appendix A.

```
else
  TxNxtStatus = TX\_SFD;
  end
  TX_MARK:
  begin
   if((fSize >= FRAME_SIZE - 1'b1) && (pCounter >= BIT_LEN -
      1'b1) && (Counter >= TMS_BIT -1'd1))
  TxNxtStatus = TX\_SFD;
   else if ((pCounter >= BIT_LEN - 1'b1)
  && (Counter >= TMS_BIT -1'd1) & Nxt_Bit)
  TxNxtStatus = TX_MARK;
   else if ((pCounter >= BIT_LEN - 1'b1)
  && (Counter >= TMS_BIT -1'd1) & ~Nxt_Bit)
  TxNxtStatus = TX\_SPACE;
   else
  TxNxtStatus = TX.MARK;
  end
  TX_SPACE:
  begin
   if((fSize >= FRAME_SIZE - 1'b1) && (pCounter >= BIT_LEN -
      1'b1) && (Counter >= TMS_BIT -1'd1))
  TxNxtStatus = TX\_SFD;
   else if ((pCounter >= BIT_LEN - 1'b1)
  && (Counter >= TMS_BIT -1'd1) & Nxt_Bit)
  TxNxtStatus = TX_MARK;
   else if ((pCounter == BIT_LEN - 1'b1)
  && (Counter >= TMS_BIT -1'd1) & ~Nxt_Bit)
  TxNxtStatus = TX\_SPACE;
   else
  TxNxtStatus = TX\_SPACE;
  end
   default : TxNxtStatus = TX_SFD;
endcase
```

Appendix A.

```
end
always @ (posedge CLK or posedge RST)
begin
if(RST)
TxPreStatus \ll TX_IDLE;
else
TxPreStatus <= TxNxtStatus;
end
always @ (posedge CLK)
begin
case (TxPreStatus)
   TX_IDLE:
   begin
   Counter \leq 24'b0;
   pCounter <= 24'd1;
   isSFD \ll 1'b1;
   cbit <= 1'b0;
   fSize \ll 8'd0;
   isOver \le 1'b0;
   led_state \ll 1'b0;
   \mathbf{end}
   TX\_SFD:
   begin
   fSize <= 8'd0;
   \texttt{led\_state} \ <= \ \texttt{l'b0};
   if(isSFD)
   begin
   if((pCounter >= SFD_LEN - 1'b1) \&\&
   (Counter >= TMS\_SFD -1'b1))
   begin
   Counter <= 24'b0;
```
```
pCounter \leq 24'd0;
cbit <= 1'b1;
isSFD \ll 1'b0;
end
else if (Counter >= TMS_SFD -1'b1)
begin
Counter <= 24'b0;
pCounter <= pCounter + 1'b1;
\mathbf{end}
else
Counter <= Counter + 1'b1;
\mathbf{end}
end
TX_MARK, TX_SPACE:
begin
if((fSize >= FRAME_SIZE - 1'b1) && (pCounter >= BIT_LEN -
    1'b1) && (Counter >= TMS_BIT -1'd1))
begin
fSize <= 8'd0;
isSFD \leq 1'b1;
Counter \leq 24'b0;
pCounter <= 24'd0;
cbit <= Nxt_Bit;
isOver \ll 1'b1;
if(Nxt_Bit)
led_state <= ~led_state;</pre>
\mathbf{end}
else if ((pCounter >= BIT_LEN - 1'b1)
&& (Counter >= TMS_BIT -1'b1))
begin
Counter <= 24'b0;
pCounter <= 24'd0;
isOver \le 1'b1;
```

```
Appendix A.
```

```
cbit <= Nxt_Bit;
   fSize \ll fSize + 1'b1;
   if(Nxt_Bit)
   led_state <= ~led_state;</pre>
   \mathbf{end}
   else if(Counter >= TMS_BIT -1'b1)
   begin
   Counter <= 24'b0;
   pCounter <= pCounter + 1'b1;
   \mathbf{end}
   else
   begin
   Counter <= Counter + 1'b1;
   isOver <= 1'b0;
   \mathbf{end}
   \mathbf{end}
endcase
\mathbf{end}
```