Efficient Power and Data Converter Circuits for RFID Applications

by

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Abstract

The basic concept of radio-frequency identification (RFID) as a means of wireless identification of physical objects has existed for over half a century. However, the technology became economically feasible during the mid-90s mainly due to proliferation of low-cost integrated circuits. Since its emergence, RFID technology has gained extensive attraction and has been used in numerous industrial applications. To facilitate widespread deployment, RFID tags as the backbone of such identification systems have to fulfil two general requirements, namely, low power consumption and small form factor. In this thesis, with an emphasis on power and area efficient architectures, efficient data and power converters as the two major building blocks of sensor-enabled RFID tags are investigated.

In the context of data conversion, by using two low-power analog buffers instead of the conventional binary weighted capacitive array, a low-power 8-bit successive-approximation register (SAR) analog-to-digital converter (ADC) with an area efficient digital-to-analog converter (DAC) architecture is proposed. Furthermore, time-mode ADC as an alternative area and power-efficient structure is discussed and a highly linear, wide-input-range voltage-to-time converter (VTC) is presented and experimentally evaluated.

In the context of efficient power converters, through optimizing the bias voltage of the gate of switching transistors in a conventional differential rectifier, three high-efficiency RF rectifier architectures, namely, gate-boosted, auxiliary-cell biased, and quasi-floating-gate (QFG)-biased rectifiers are proposed. Furthermore, through dynamically adjusting the input capacitance, a dual-band matching approach for RF rectifiers is presented. In a practical

application scenario, the incorporation of the proposed high-efficiency rectifiers in complete wireless monitoring systems is briefly discussed.

The proposed QFG-biased rectifier is incorporated and analyzed in a wake-up radio front-end. Also, backscattering method as a power efficient scheme during the transmit mode is studied in the context of biomedical implants. Furthermore, based on the techniques developed for enhancing the efficiency of the rectifiers, an ultra-low-power complementary metal-oxide-semiconductor (CMOS) voltage-controlled ring oscillator architecture is proposed.

The proposed building blocks and systems, namely, ADC, rectifiers, wake-up radio structure, and voltage-controlled ring-oscillator architecture are designed in a 0.13-μm CMOS technology and their performances are verified through post-layout simulation and/or measurement results.

Preface

I, Pouya Kamalinejad, am the principle contributor to all six chapters, except for Chapter 4 (Section 4.2) where Kamyar Keikhosravy is the main contributor and for this section, I have assisted him with the design of the test setup, measurement of backscattering scheme and preparing the manuscript for the dissemination of the results.

Kamyar Keikhosravy has assisted me with the design of the voltage-to-time converter of Chapter 2 (Section 2.4), the auxiliary-boosted rectifier of Chapter 3 (Section 3.3), the QFG-boosted rectifier of Chapter 3 (Section 3.4), the dual-band matching technique of Chapter 3 (Section 3.6), the wake-up radio architecture of Chapter 4 (Section 4.1) and the ring-oscillator of Chapter 5 (Section 5.1).

Reza Molavi has assisted me in the design of the voltage-to-time converter of Chapter 2 (Section 2.4), the dual-band matching technique of Chapter 3 (Section 3.6) and the ring-oscillator of Chapter 5 (Section 5.1).

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Professor Shahriar Mirabbasi and Professor Victor Leung, who co-supervised the research, have provided technical consultation and editorial assistance on the

manuscripts.

Below is the list of accepted and submitted journal and conference papers that are resulted from this work:

Refereed Conference Contributions

1. K. Keikhosravy, **P. Kamalinejad**, A. Zargaran-Yazd, Kenichi Takahata and S. Mirabbasi "A Fully Integrated Telemonitoring System for Diagnosing In-Stent Restenosis," to be presented at IEEE Biomedical Circuits and Systems Conference (BIOCAS), Laussane, Switzerland, October 2014.

2. **P. Kamalinejad**, K. Keikhosravy, R. Molavi, S. Mirabbasi and V. C.M. Leung "An Ultra-Low-Power CMOS Voltage-Controlled Ring Oscillator for Passive RFID Tags," IEEE International New Circuits and Systems Conference (NEWCAS), Trois-Rivières, Canada, June 2014. (Chapter 5. Section 5.1)

3. **P. Kamalinejad**, K. Keikhosravy, R. Molavi, S. Mirabbasi and V. C.M. Leung "Efficiency Enhancement Techniques and a Dual-Band Approach in RF Rectifiers for Wireless Power Harvesting," IEEE International Symposium on Circuits and Systems (ISCAS), special session on Circuital Aspects of Emergent Application-Driven Wireless Power Transfer Systems, Melbourne, Australia. June 2014. (Chapter 3. Section 3.6,[1])

4. **P. Kamalinejad**, K. Keikhosravy, M. Magno, S. Mirabbasi, V. C.M. Leung and L. Benini "A High-Sensitivity Fully Passive Wake-Up Radio Front-End for Wireless Sensor Nodes," IEEE International Conference on Consumer Electronics (ICCE), pp. 209-210, Las Vegas, USA, Jan. 2014. (Chapter 4. Section 4.1,[2])

5. K. Keikhosravy, **P. Kamalinejad**, S. Mirabbasi, V. C.M. Leung "A Wideband Unity-Gain Buffer in 0.13 μm CMOS," IEEE International Conference on Electronics, Circuits and Systems (ICECS), Abu Dhabi, UAE, December 2013.

6. **P. Kamalinejad**, K. Keikhosravy, S. Mirabbasi and V. C.M Leung "A CMOS Rectifier with Extended High-Efficiency Region of Operation," IEEE International Conference on RFID Technologies and Applications (RFID-TA), pp. 1-6, Johor Bahru, Malaysia, September 2013. (Chapter 3. Section 3.4[3])

7. **P. Kamalinejad**, K. Keikhosravy, S. Mirabbasi and V. C.M Leung "An Efficiency Enhancement Technique for CMOS Rectifiers with Low Start-Up Voltage for UHF RFID Tags," International Green Computing Conference (IGCC), pp. 1-6 Arlington, USA, June 2013. (Chapter 3. Section 3.3,[4])

8. K. Keikhosravy, **P. Kamalinejad**, S. Mirabbasi, K. Takahata and V. C.M. Leung "An Ultra-Low-Power Monitoring System for Inductively Coupled Biomedical Implants," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2283-2286, Beijing, China, 19-23 May 2013. (Chapter 3. Section 3.7, [5])

9. **P. Kamalinejad**, S. Mirabbasi and V. C.M. Leung, "An Ultra-Low-Power SAR ADC with an Area-Efficient DAC Architecture," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 15-18, Rio de Janeiro, Brazil, May 2011. (Chapter 2. Section 2.2, [6])

10. **P. Kamalinejad**, S. Mirabbasi and V. C.M. Leung, "An Efficient CMOS Rectifier with Low-Voltage Operation for RFID Tags," International Green Computing Conference (IGCC), pp. 25-28, Orlando, USA, July 2011. (Chapter 3. Section 3.2, [7])

Refereed Journal Submissions

1. **P. Kamalinejad**, C. Mahapatra, Z. Sheng, Y. L. Guan, S. Mirabbasi, and V. C.M. Leung "Wireless Energy Harvesting for Internet of Things," Submitted.

2. K. Keikhosravy, D. S. Brox, **P. Kamalinejad**, S. Mirabbasi and K. Takahata "An Ultra-Low-Power 35-nW Wireless Monitoring System for Biomedical Applications," Submitted.

Table of Contents

List of Tables

List of Figures

Glossary

ADC analog-to-digital converter

CMOS complementary metal-oxide-semiconductor

CPU central processing unit

CS current-starved

DLL delay locked loops

DNL differential nonlinearity

DTC digital-to-time converter

ENOB effective number of bits

FCC federal communications commission

FDM frequency-division multiplexing

FOM figure of merit

FSK frequency shift keying

HF high-frequency

IC integrated circuits

INL integral nonlinearity

ISM industrial scientific and medical

KBPS	kilo-bit per second
LF	low-frequency
LNA	low noise amplifier
LSB	least significant bit
MAC	medium access control
MCU	microcontroller unit
MF	medium-frequency
MIM	metal-insulator-metal
MOS	metal-oxide-semiconductor
MSB	most significant bit
MSPS	Mega-samples per second
OCR	optical character recognition
OOK	on-off keying
PCE	power conversion efficiency
PD	pseudo-differential
PLL	phase locked loop
PMU	power management unit
PSK	phase shift keying
QAM	quadrature amplitude modulation
RF	radio frequency
RFID	Radio frequency identification
RO	ring oscillator

SAR	successive approximation register
SC	switched-capacitor
SMA	sub-miniature version A
SNDR	signal-to-noise and distortion ratio
SRO	single-ended ring-oscillator
TDC	time-to-digital converter
TMSP	time mode signal processing
TVC	time-to-voltage converter
UHF	ultra-high-frequency
VCDU	voltage-controlled delay unit
VCRO	voltage-controlled ring oscillator
VHF	very-high-frequency
WUR	wake-up radio

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Chapter 1

Introduction

1.1 RFID Technology Overview

Radio frequency identification (RFID) is a communication technology that uses electromagnetic waves to transfer data between a reader and a tag for the purpose of contactless identification, tracking and data collection. The concept of using radio communication to identify physical objects has existed for over half a century [9]. However, the widespread use of this technology became a possibility only after the emergence of inexpensive integrated circuits (IC). RFID technology can be considered as the predecessor to the two widely used optical identification systems namely *bar code* and optical character recognition (OCR). Bar code and OCR use an optical transducer to extract data from the identifying mark (one-dimensional in the case of bar code and two-dimensional in the case of OCR) [9]. Although optical identification methods are being prevalently used in virtue of their simplicity and low cost, they come with many drawbacks. Most importantly, such systems require a *line of sight* between the reader device and the identification mark which severely limits their usefulness in applications where a large number of objects are spread over a wide area. Some other shortcomings of optical identification systems include readability degradation as the result of mechanical damage to the marks, short interrogation distance and limited storage capacity.

RFID technology on the other hand uses electromagnetic waves to establish a

communication link between the reader and the physical object and therefore alleviates the need for line of sight. The non-line-of-sight operation of RFID systems allows simultaneous identification of multiple objects in a wide area. Moreover, RFID systems offer many more advantages over optical identification systems which could be summarized as RFID advantages[1] [10]:

- Robustness and reliability: Objects can be identified in tough environments and difficult scenarios.
- Speed: The transponders (objects) respond to the interrogation command at a very short time (on the order of miliseconds).
- Bidirectional communication: The transponders are writable (i.e., the identity code can be edited in real time). Also, depending on the application, some transponders can initiate a communication with the reader.
- High storage capacity: The transponders can accommodate semiconductor memory (flash) and are therefore, capable of offering a higher storage capacity compared to optical identification systems.
- Data process capability: The transponders can be equipped with a processing unit which allows them to detect more elaborate interrogation commands and transmit more detailed environmental/sensory data.

The aforementioned advantages combined with the emergence of low-cost integrated circuits have made RFID technology a very attractive candidate for numerous real world applications. According to IDTechEx[2] report, the total market for RFID technology was worth $6.98 billion and $7.88 billion in 2012 and 2013 respectively and will grow to $9.2 billion in 2014. The report forecasts the market value to rise $30.24 billion in 2024 [11]. Major applications of RFID technology include [12]:

- Logistics: Facilitates supply chain management and product delivery.

[1] http://www.brooks.com/applications-by-industry/rfid/rfid-basics/rfid-advantages
[2] http://www.idtechex.com/

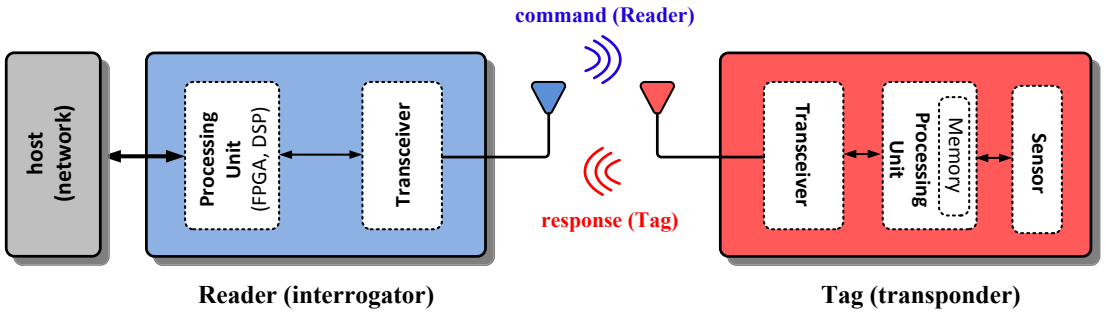


Figure 1.1: Block diagram of a generic RFID system.

- Toll systems: Provides a fast, contactless, secure and convenient check in/out.
- Ticket: Enables contactless automatic identification. Also allows further data collection (allocation, flow of ticket holders, etc.).
- Health care: Facilitates the automation of admittance, screening and treating. Enables wireless personal health monitoring.
- Security and Identification: Provides a reliable storage of identification information (ID cards, passports, etc.).

A generic RFID system consists of three main components, namely reader (interrogator), tag (transponder) and the host computer (network) as schematically shown in Figure 1.1. The reader and the antenna tags establish the wireless communication between the reader and the tag. The reader antenna can be integrated with the reader or connected with a cable, while the tag antenna is generally integrated in the tag. Most tags incorporate an IC which contains the tag ID (in a silicon memory) and performs the processing required for communication with the reader and sensory data interfacing. Note that the sensor (and the associated interface) is not an integral part of all RFID tags and may or may not be incorporated in the tag depending on the application. The reader and tag transceivers are responsible for receiving/transmitting (modulation/demodulation) the interrogation commands and tag responses respectively. There are some tags in the technology that do not use an IC and only transmit an identification code in response to an interrogation command. Also, depending on the application, the reader may support a user interface or may be connected to a host for further processing and storage of the received responses [9].

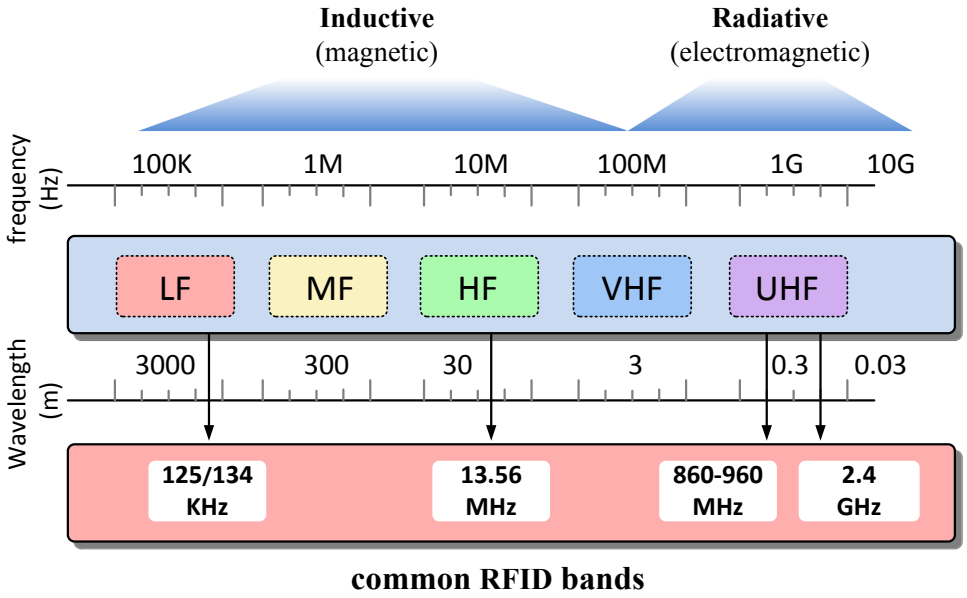


Figure 1.2: RFID frequency bands.

1.2 RFID Classification

RFID systems are generally categorized based on three characteristics, their frequency of operation, the method they use to deliver power to the tags and the protocol they use to for the communication between the tag and the reader. The frequency band, power delivery method and communication protocol are dictated by the application and directly influence the important aspects of the entire system such as cost, communication range and functionality [9].

1.2.1 RFID Frequency Bands

RFID operates in the unlicensed spectrum space also known as the industrial scientific and medical (ISM) band. ISM bands are reserved for the use of radio frequency (RF) energy for industrial, scientific and medical purposes only (rather than telecommunication)[3] and their use are governed by part 18 of federal communications commission (FCC) rules[4] [13].

Figure 1.2 shows the operating frequencies used by RFID systems [9]. As shown in the figure, the most common frequency bands used by RFID systems are 125/134 kHz[5], 13.56 MHz and 2.4-2.45 GHz. The systems operating in the first frequency band (125/134 kHz) are referred to as low-frequency (LF) RFID

[3] http://en.wikipedia.org/w/index.php?title=Special:Cite&page=ISM_band&id=603492296

[4] http://www.ecfr.gov/cgi-bin/text-idx?SID=758038852bf8e27b362820cc4a3ae5da&node=47:1.0.1.1.18&rgn=div5

[5] The two distinct frequencies are used for frequency-shift-keying scheme.

systems, those operating at 13.56 MHz are known as high-frequency (HF) systems and finally readers and tags operating at 900 MHz and 2.4-2.45 GHz range are characterized as ultra-high-frequency (UHF) systems. To distinguish between the 900 MHz and 2.4-2.45 GHz bands, the former category of tags and readers are referred to as UHF devices while the latter category are known as microwave RFID system [9]. As shown in Figure 1.2, medium-frequency (MF) and very-high-frequency (VHF) bands are not used for RFID application.

Note that in Figure 1.2, the frequency band is partitioned into inductive and radiative regions. Generally, the systems in which the wavelength is much larger than typical antenna sizes are *inductively coupled*. The systems in the inductive range have a wavelength of 3000 to 3 meters. Therefore, for a typical antenna size (on the order of 1 meter or less), such systems fall into the category of inductively (magnetically) coupled devices. The inductively coupled reader-tag system practically forms a magnetic transformer which provides a coupling between the current flowing in the reader antenna (primary) and the voltage induced in the tag antenna (secondary). For a fixed transmitted energy from the reader, the received energy at the tag antenna drops with the cube of the communication distance (or faster in practical scenarios). Such a coupling can be used to transfer data between the reader and the tag and also power from the reader to the tag.

Radiative (electromagnetic) coupling is referred to systems in which the antenna size is comparable to the wavelength. Generally, in electromagnetically coupled systems, the reader-tag distance is much longer than a single wavelength and a weak version of the transmitted signal (by the reader) is received at the tag antenna. Note that in many practical scenarios, multipath fading further exacerbates the detection of the received signal, making it a heavily dependent function of the tag's location [14]. For a fixed transmitted energy from the reader, the received energy at the tags antenna falls off with the square of the communication distance (or faster in practical scenarios).

Apart from the distinction in the frequency of operation, the adoption of the coupling method (inductive versus radiative) directly affects the behavior of the entire RFID system. Generally, inductive coupling is a reliable method when the distance between the reader and the tag antenna is short (on the order of the reader antenna size). However, inductive coupling is very sensitive to both the

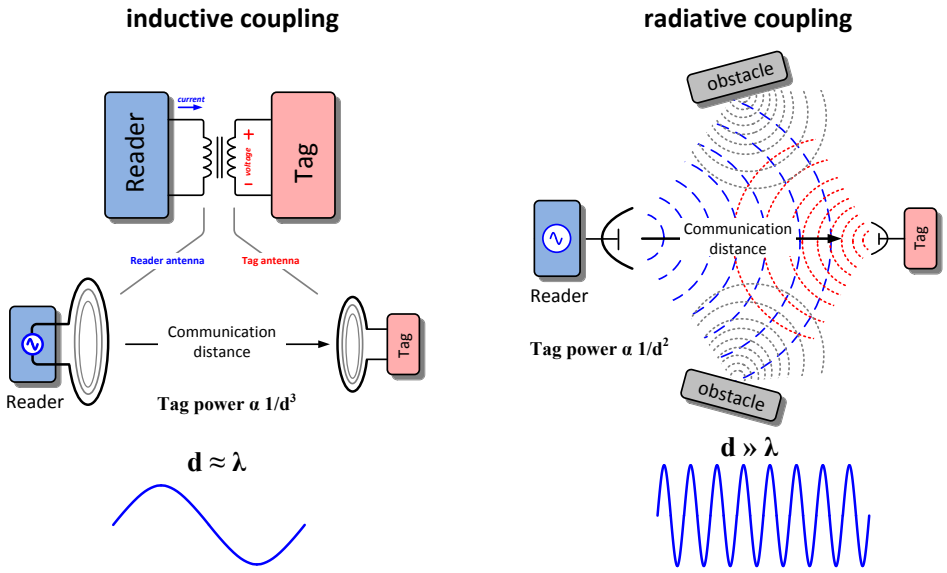


Figure 1.3: Schematic diagram of the operation principles of inductive and radiative coupling in RFID systems.

communication distance and the relative displacement (orientation) of the antennas. Therefore, such systems are essentially suitable for applications where the communication distance is short and the orientation of the antennas (coils) can be easily defined by the user. Examples of such applications include health-care monitoring devices (animal and human ID) and access control (ID card readers). On the other hand, electromagnetically coupled RFID systems provide a longer communication distance at the cost of more complex propagation channel which typically requires a more sophisticated receiver for the RFID tag. The operation principles of inductive coupling and radiative coupling methods are schematically shown in Figure 1.3 [9].

The choice of frequency band has many implications on other performance metrics of the RFID system. Inductively coupled systems use coil antennas. For a fixed primary coil (reader antenna) current, the voltage induced on the secondary coil (tag antenna) is proportional to the frequency of operation, the size and the number of the turns of the coil. Therefore, systems operating at LF (125 kHz) require larger coils with more number of turns (on the order of 10 to 100 turns). Systems operating at HF (13 MHz) also use coil antennas with less number of turns (3 to 6 turns) compared to LF systems. At UHF/microwave frequencies, tags generally used dipole antennas. The size of a dipole antenna (typically about half the wavelength) is inversely proportional to the frequency of operation.

The frequency of operation also affects how the waves interact with materials

Table 1.1: Summary of RFID frequency bands and characteristics.

Band	**LF**	**HF**	**UHF**	**Microwave**
Frequency	30 - 300 kHz	3 - 30 MHz	0.3-3 GHz	2-30 GHz
Typical RFID Frequency	125 - 134 kHz	13.56 MHz	433 MHz^{UHF_1} 860 - 960 MHz^{UHF_2}	2.45 GHz$\sim$
Communication Range	$<$ 0.5 m	$\leq$ 1.5 m	UHF_1: $\leq$100 m UHF_2: 0.5 m$\sim$5 m	$\leq$ 10 m
Data Transfer Rate	$<$ 1 kbps	$\approx$ 25 kbps	$\approx$ 30 kbps	$\leq$ 100 kbps
Characteristics	Short range. Low data rate. Penetrates water but not metal.	Mid range. Mid data rate. Penetrates water but not metal.	Long range. High data rate. No water/metal penetration.	long range. High data rate. No water/metal penetration.
Application	Animal ID. Access control. Car immobiliser.	Smart labels. Contactless travel cards, Access Security, Apparel.	Logistics, Baggage, Handling, Electronic toll collection.	Electronic toll collection.

present in the communication medium. The two most common materials RFID waves encounter with are water and metallic objects. Generally, the waves penetration distance (also known as skin depth) both for water and metallic objects drops as the frequency increases. This follows that LF and HF systems are more suitable for human and animal identification where the waves need to penetrate through water containing materials (body tissue).

The data rate of an RFID system is also a function of the frequency of operation. More specifically for a frequency modulation scheme, the signal detection accuracy is directly proportional to the number of the cycles that the reader/tag receives for each binary bit (0 or 1), in order to be able to differentiate between the two frequencies the represent each bit. Therefore, for higher frequencies, less time is required to accurately detect a transmitted bit, which in turn corresponds to a higher data rate. The data rate of LF systems is on the order of a few kilo-bit per second (KBPS) while UHF tags operate and a few tens of kbps data rate [9]. Table 1.1 summarizes RFID frequency bands, their characteristics and common applications [15].

1.2.2 RFID Power Delivery Methods

As mentioned earlier, RFID systems are also categorized based on the power (energy) delivery methods to the tags. From the perspective of manufacturing cost and form factor, it is particularly desirable to remove the dedicated energy source (battery) of the tags. Battery-less tags also provide a long and maintenance-free life time. Depending on the presence or absence of the dedicated power source and the extent to which the power source is used, RFID tags are classified into three groups of passive, semi-passive and active tags.

Passive tags do not have an independent power source and do not use a conventional transmitter. These class of tags harvest their required energy by rectifying the transmitted power from the reader. In order to send information back to the reader, passive tags practically reflect the transmitted waves in a scheme known as *backscattering* [16] .

Semi-passive tags (also referred to as *battery-assisted passive* tags) incorporate a battery. However, the battery is only used to power the tag's internal circuitry. In order to transmit information back to the reader, semi-passive tags also use the backscattering communication method and therefore do not employ a conventional transmitter.

Active tags on the other hand, use a battery both to power the tag circuitry and signal transmission. They incorporate a conventional transmitter and establish a bidirectional communication with the reader.

As mentioned above, passive tags extract power from the received waves by means of a block called rectifier (also known as RF-to-DC converter). The rectified voltage is regulated to produce a rather stable supply for the succeeding circuitries. These category of tags generally perform *envelope detection* method to demodulate and detect the received signal. In order to transmit information back to the reader, passive tags change the electrical characteristics of their antenna by modulating the impedance of the antenna with respect to the data bits. A common method for realizing antenna impedance modulation is through switching the antenna terminal between two states (short an open in the extreme case). Such variations in the impedance of the antenna can be detected by the sophisticated receiver at the reader side. The absence of battery and dedicated transmitter (and

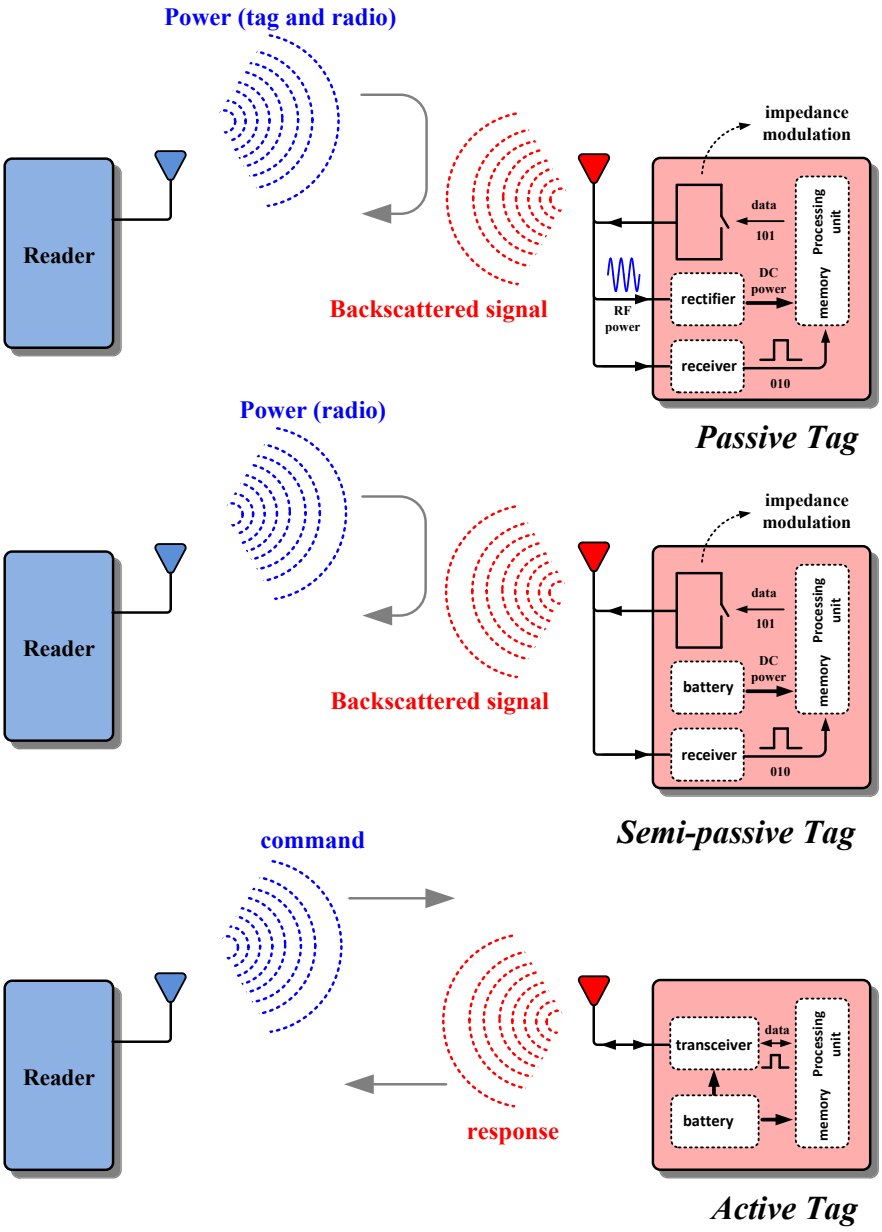


Figure 1.4: Schematic diagram of the operation principles of passive, semi-passive and active RFID tags.

associated analog blocks such as frequency synthesizers, power amplifiers, low noise amplifiers, etc.), facilitates low cost implementation of passive tags which is of paramount importance in many RFID applications. However, such simplicity and low cost offered by passive tags come at the expense of short read range (on the order of 2 to 20 meters). Also, since passive tags rely on the transmitted power (from the reader) as the sole source of energy, they are unable to support

complicated communication protocols and are typically designed to perform basic computational tasks.

Semi-passive tags use a battery to power the internal circuitry and are therefore capable of accommodating a more elaborate IC. Although they use backscattering for re-transmitting information to the reader, availability of a dedicated power source allows inclusion of some RF blocks (such as RF amplifiers) at the receiver front-end. A more elaborate receiver provides a longer read range (on the order of 10 to 100 meters) for semi-passive tags. Semi-passive tags have a rather long life time as they sink their battery at a very low duty cycle and spend most of their time in idle/sleep mode. Nevertheless, incorporation of a battery imposes a higher manufacturing cost, larger aspect ratio and maintenance requirements.

Active tags are practically complete radios with all the required circuitry including power source, receiver, transmitter and processing unit [9]. They typically incorporate the complete transceiver chain and are capable of realizing more complex modulation schemes, such as frequency-division multiplexing (FDM) which is beneficial in scenarios where multiple tags want to communicate with the reader simultaneously. In virtue of their powerful receiver, active tags can support sophisticated modulation schemes such as phase shift keying (PSK), frequency shift keying (FSK) and quadrature amplitude modulation (QAM) and therefore achieve a much longer read range (on the order of hundreds of meter and higher) compared to their passive and semi-passive counterparts. Evidently, this advantage comes with a high cost, large size and maintenance requirements for the tags.

Figure 1.4 schematically shows the operation principles of passive, semi-passive and active tags [9].

1.2.3 RFID Protocols

Protocols generally define a set of rules on how information is exchanged between two nodes. They address the type of signals and symbols and also determine how the channel is allocated among different transmitters. In the context of RFID

systems, EPCglobal®[6] is in charge of establishing standards for supply chain and related applications. There are different protocols for different systems and classes. These protocols were developed independently and the systems adopting them, are not necessarily mutually compatible. In terms of RFID frequency bands, different classes inevitably require different coding and modulation schemes, and therefore adopt distinct protocols. As discussed earlier, LF systems use FSK while HF and UHF tags use amplitude modulation. Also, different power delivery methods entail specific standards. For example, as discussed earlier, passive tags employ a simple receiver and are therefore incapable of realizing spectrally efficient modulation schemes such as PSK and QAM. Note that apart from modulation scheme, medium access control (MAC) layer architecture, packet structure and coding schemes are also defined as elements of RFID protocols [17]. RFID communication protocols are beyond the scope of this thesis and were only discussed briefly in this section.

1.3 Challenges and Motivation

RFID technology covers a wide range of applications, each with its specific set of requirements. Some applications require sophisticated tag/reader with complex circuitries and high processing capabilities. Such applications allocate sufficient power budget for the system and usually cost is not a matter of concern for them. Such applications span a relatively narrow range of RFID potentials. In most applications, an RFID system is expected to involve a very large quantity of tags with unique IDs in an architecture known as *Internet of things* [18]. Internet of things is a term referred to the network of a large number of uniquely identifiable objects in an Internet-like structure. Each identifiable object is equipped with a sort of embedded intelligence which allows an interaction with internal or external environment. Internet of things relies on RFID technology as its infrastructure.

Due to several reasons, active tags do not simply lend themselves to large scale deployment. Unfortunately, battery technology has progressed slowly and is lagging behind the requirements expected for low maintenance systems. Printed batteries and power packs exist in the technology, however, the amount of energy

[6] http://www.gs1.org/gsmp/kc/epcglobal

they store and deliver to the tag is far less than what is required to run an active tag for a reasonable amount of time. Apart from manufacturing cost, maintenance requirements and power considerations, battery-powered tags are problematic in many RFID applications which are size-sensitive. Passive tags on the other hand, are very attractive candidates for large scale deployment in virtue of their simplicity, low manufacturing cost and zero maintenance requirements. They can operate at any RFID frequency band, however they could be designed in smaller form factor at higher frequencies. In virtue of the essential advantages mentioned above, passive IC-based RFID tags are considered to be the dominant RFID technology in near future manufactured and deployed in very large quantities.

As mentioned in Section 1.2, passive tags extract their required energy from the incident power transmitted by the reader (or from environmental sources in the form of heat, light or vibrations) and the absence of a dedicated energy source in passive tags poses stringent design challenges. The most important problem arises when the tag is located at a far distance from the reader (in electromagnetically coupled systems) or is misaligned with respect to the reader (in inductively coupled systems). As discussed in Section 1.2, the power received by the tag (from the reader) drops with the cube and the square of the communication distance in inductively coupled and electromagnetically coupled systems respectively. The received power by the tag is even less in the presence of environmental obstacles and multipath fading. Therefore, if the reader and the tag are located far enough from one another such that a minimum power is not received by the tag, the entire operation of the system would be compromised. Such scenarios occur frequently in practice, when the reader, the tag and/or the environmental objects are in motion. Since a long read range is of paramount importance in many RFID applications, meticulous architectures (both at system and circuit levels) need to be devised in order to guarantee that the tag receives sufficient amount of energy at any circumstance and to avoid potential malfunctions.

From a circuit level perspective, two major paths has to be followed in order to guarantee that sufficient power is delivered to the passive tag. Primarily, a high performance power harvesting unit is required to receive the incoming energy and to convert it to a stable form to supply the tag's circuitry. Furthermore, intelligent

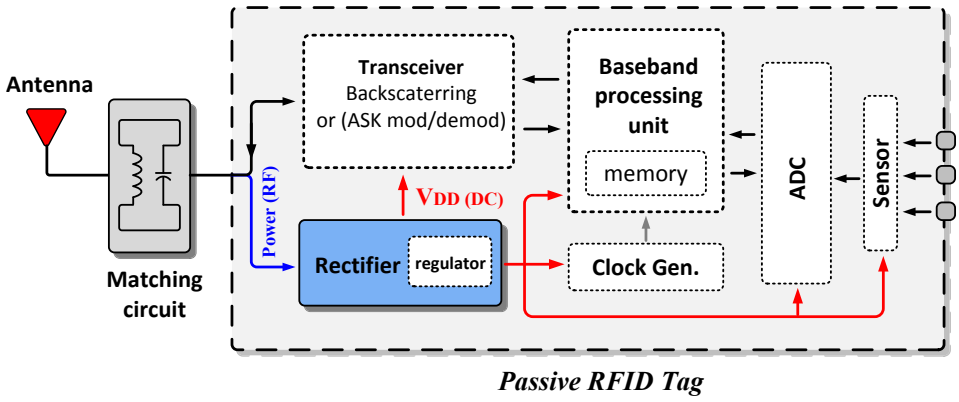


Figure 1.5: Schematic diagram of a sensor-enabled passive RFID tag.

design techniques have to be devised and applied to the tag's circuitry in order to minimize the minimum required power proper operation.

Figure 1.5 shows the block diagram of a generic sensor-enabled passive RFID tag. As shown in the figure, a passive tag comprises an antenna, an impedance matching circuit (typically embedded in the antenna structure), a transceiver (backscattering or ASK modulator/demodulator), a baseband processing unit and memory, a clock generator, an analog-to-digital converter (ADC) and a sensor(s). Note that excluding some specific applications where the tag transmits simple ID information (code), a sensor (and the associated interface including the ADC) is an integral part of a passive RFID tag. The sensor and the ADC are required if the tag is to interact with its internal environment and collect data (e.g., in wireless sensor networks and Internet of things). The baseband processor controls the operation of the tag. Its main task is to process the received data (from the receiver) and to generate an appropriate response (for the transmitter) using the information stored in the memory or from the data collected by the sensor. The clock generator (typically in the form of a simple local oscillator) synchronizes the operation of the ADC, processor and the transmitter.

An important block in the passive RFID tag is the rectifier (also known as RF-to-DC converter). Rectifier as the core of the power harvesting unit is responsible for receiving RF energy from the tag antenna and to convert it to an stable DC voltage to supply the building block of tag. The most crucial performance metric of a rectifier is its power conversion efficiency (PCE) which directly affects the overall operation of the entire tag. PCE is defined as:

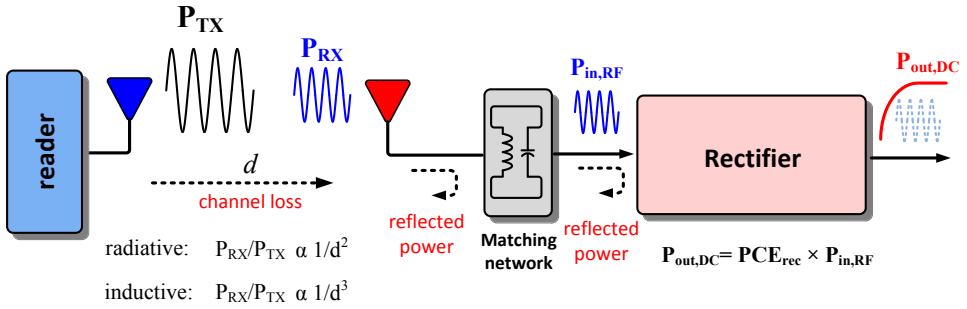


Figure 1.6: Schematic diagram of the power levels along the path from the reader to the output of the rectifier.

$$\mathrm{PCE_{rec}} = \frac{\mathrm{P_{out,DC}}}{\mathrm{P_{in,\,RF}}} \tag{1.1}$$

where, $\mathrm{P_{in,RF}}$ is the RF power available at the input of the rectifier and $\mathrm{P_{out,DC}}$ is the rectified DC output power of the rectifier. In order for the tag to operate properly, $\mathrm{P_{out}}$ has to be larger than the summation of the required power for all the building blocks including transceiver, processor, clock generator, ADC and the sensor.

Figure 1.6 schematically shows how the power level drops from the transmitter (reader) on its way to the output of the rectifier. As shown in the figure, the highest degradation occurs across the communication channel ($\mathrm{P_{TX}}$-to-$\mathrm{OP_{RX}}$) due to channel loss. As mentioned in Section 1.2.1, the channel loss is proportional to the square of distance and to the cube of distance in radiative and inductive coupling respectively. Note that these dependencies are optimistic estimations and do not include the adverse effects of the obstacles and multipath fading (for radiative coupling) and misalignment (inductive coupling). The received power at the tag antenna ($\mathrm{P_{RX}}$) further drops due to the potential impedance mismatch between the output of the antenna and the input of the tag (rectifier and transceiver). Note that a perfect impedance matching, even in the presence of the matching network is not practically feasible due to geometric limitations of the antenna and the variable input impedance of the tag. The final power level degradation occurs in the process of rectification the implication of which is represented by an imperfect PCE (i.e., PCE% $\neq$ 100). For an ideal channel (no environmental obstacle) and for a perfect impedance matching (no reflection from the input of the tag), Friis equation shows how the tag's power is

Table 1.2: Comparison of ADC types characteristics.

Architecture	Latency	Speed	Resolution	Area
Flash	Low	High	Low	High
SAR	Low	Low-medium	Medium-high	Low
Folding/interpolation	Low	Medium-high	Medium	High
Delta-sigma	High	Low	High	Medium
Pipeline	High	Medium-high	Medium-high	Medium

related to the transmitted power [19]:

$$P_{out,DC} = P_{tag} = P_{TX} \cdot G_{tag} \cdot PCE_{rec} \cdot \left(\frac{\lambda}{4\pi d}\right)^2 \tag{1.2}$$

where, P_{tag} is the minimum required power for the tag circuitry, P_{TX} is the transmitted power by the reader (as in Equation 1.1), G_{tag} the the gain of tag antenna, PCE_{rec} is the efficiency of the rectifier (as in Equation 1.1), λ is the wavelength of the transmitted waves and d is the communication distance. Note that in Equation 1.2, the maximum P_{TX} is governed by FCC to 4 W ([13]), G_{tag} is dictated by antenna geometry and tag's size limitations and λ (and accordingly the frequency of operation) and the read range. d are set by the application. Also, P_{tag} is dictated by the application, sensitivity of the tag receiver and baseband processing requirements of the tag (typically on the order of a few micro-Watts to hundreds of micro-Watts). Therefore for a fixed P_{tag}, the efficiency of the rectifier, PCE_{rec} turns out to be the only design parameter in order to guarantee a reliable tag operation and to increase the read range, d. Extensive studies have been carried out in the literature in an attempt to improve the performance of the power harvesting unit and to propose high efficiency rectifiers for passive RFID tags. Enhancing the power conversion efficiency of the rectifier at a circuit level perspective will be discussed in details in Chapter 3.

Another important building block of a sensor enabled passive RFID tag is the analog to digital converter. Environmental data collected by the sensors (e.g., temperature, humidity, gas, blood pressure, etc.) are analog in nature and have to be converted to the digital domain to be processed by the processing unit of the tag and consequently transmitted to the reader. The ADC can consume a large

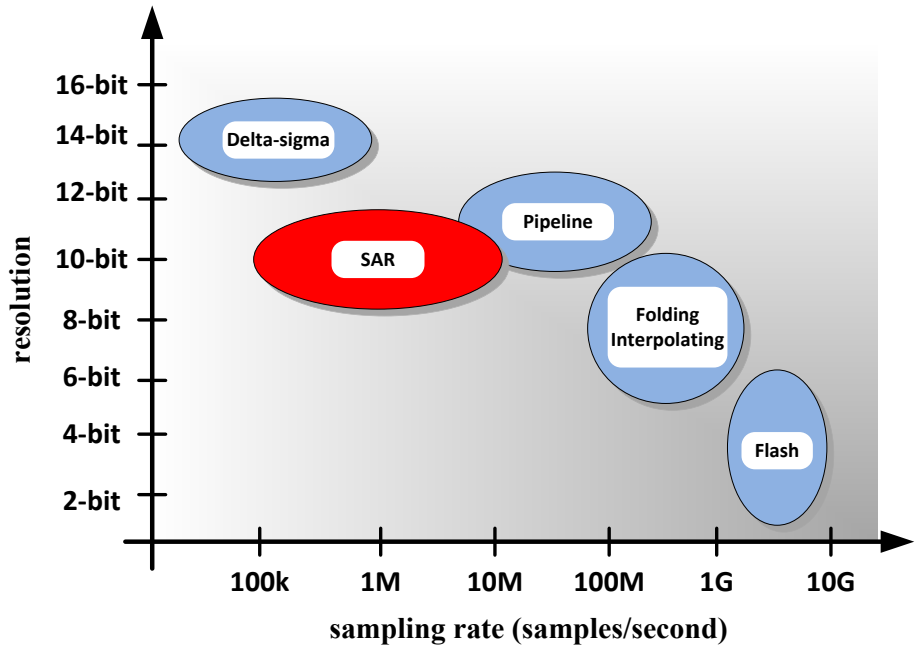


Figure 1.7: Comparison of different ADC architectures in terms of sampling rate and resolution.

percentage of both the power and the silicon area available for the passive RFID tag. Therefore, the selection of the right topology and specification of the ADC requires a keen attention. ADC topologies are classified into five major categories of delta-sigma, successive approximation, pipeline, folding/interpolating and flash. Figure 1.7 and Table 1.2 compare different ADC types in terms of sampling rate, resolution and basic characteristics [20]. It should be noted that most RFID applications (depending on the sensory data that they capture) require a medium sampling rate on the order of a few kilo-samples per second to a few Mega-samples per second (MSPS) with medium resolution on the order of 8 to 10 bits. Such requirement along with its inherent simplicity, make successive approximation register (SAR) ADCs the most attractive candidates for most RFID applications. Among different categories, SAR ADC uses minimal analog circuitry and could be implemented with small silicon area and low power consumption [6]. Many research have been carried out on SAR ADCs at system and circuit levels, to improve their performance in terms of power consumption and area requirements. Improving the performance of SAR ADCs will be discussed in details in Chapter 2.

Another design technique that has proven promising for implementation of the

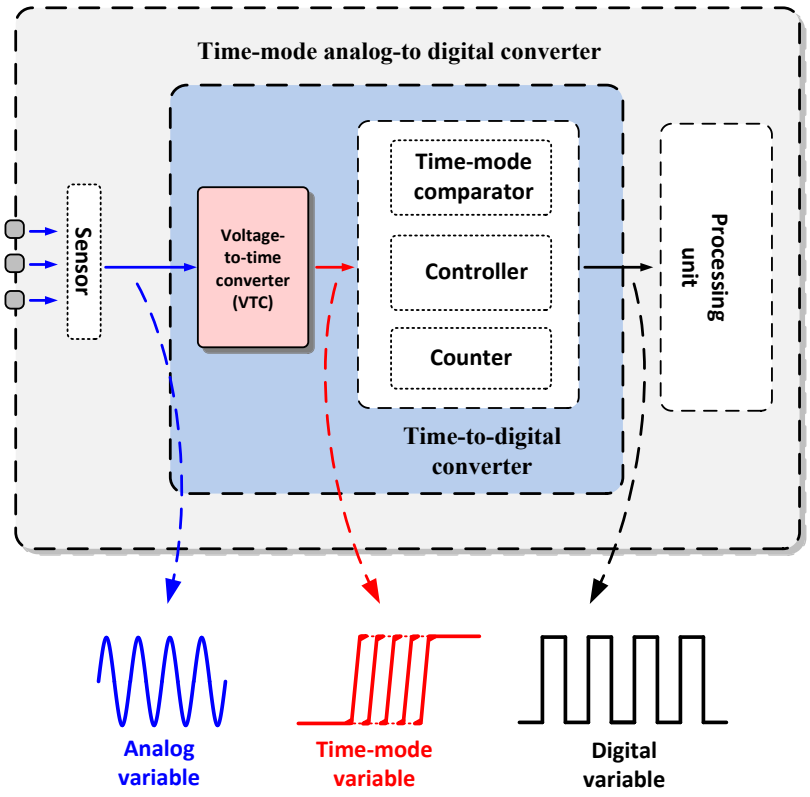


Figure 1.8: Schematic diagram of a time-mode analog-to-digital converter.

ADC block in passive RFID tags, is time mode signal processing (TMSP). In TMSP, voltage and current variables are converted to a time domain variable (i.e., the delay between two edges of a clock signal) [21]. The time domain variable can then be processed through an all-digital circuitry. Processing the information in digital domain facilitates a low power and compact implementation of the processing unit which is specifically beneficial in the context of passive RFID tags.

As shown in Figure 1.8, a crucial building block of a TMSP system (including the time-mode analog-to-digital converter) is the voltage-to-time converter. VTC as the interface between analog and time domain, is responsible to receive the analog signal and to convert it into an accurate time domain representation. The performance of the VTC in terms of linearity, input range, power consumption and layout area directly affects the TMSP system and the overall operation of the RFID tag. Circuit level design techniques to improve the performance of the VTC block are discussed in details in Chapter 2.

1.4 Summary of Contributions

As mentioned in Section 1.3, the building blocks of a passive RFID tag are required to fulfill stringent requirements in order to guarantee a reliable tag operation. Such strict requirements mainly stem from the absence of a dedicated power source for the tags and necessitate sophisticated design technique to cope with the very tight power budget of the passive tag. Apart from low power consumption, the tag circuitries are required to be area efficient. Small form factor for the integrated circuits is of paramount importance in the context of passive RFID tags as it leads to lower manufacturing cost. Also, there are strict limitations on the size of the tags in passive RFID applications (e.g, human health-care monitoring, inventory and supply chain management, etc.).

In this thesis, data and power converter as two crucial building blocks of a passive RFID tag are studied at a circuit level perspective. With an emphasis on low power consumption and small silicon area, design techniques are proposed to improve the performance of these blocks. The circuits using the proposed techniques are designed and their performance are verified through simulation and/or measurement. A summary of the contributions of this work are presented in the following sections.

1.4.1 Proposed Ultra-Low-Power SAR ADC with an Area-Efficient DAC Architecture

To reduce the power consumption and layout area of the SAR ADC, a digital-to-analog converter architecture is proposed that employs two rail-to-rail low-power unity-gain buffers and only 4 minimum-size capacitors instead of the conventional binary-weighted capacitor array. Thereby, power consumption and area are drastically reduced by virtue of lower switching activity and smaller size capacitor array. The proposed 8-bit SAR ADC is designed and simulated in a 0.13μm CMOS process. Simulation results show that for a 2.4 kHz (12.4 kHz) input signal while sampling at 25 kHz, the ADC achieves an effective number of bits (ENOB) of 7.9 (7.8), consumes 290 nW (350 nW) form a 0.8 V analog supply and a 0.6 V digital supply, and achieves a figure of merit (FOM) of 48 fJ/conversion-step (62 fJ/conversion-step). Details of the proposed SAR ADC

design are discussed in Chapter 2.

1.4.2 Proposed Highly Linear Wide Input Range Voltage-to-Time Converter

To achieve good performance for the VTC new design techniques are investigated. High linearity is achieved by re-ordering the charge and discharge cycles, i.e., initially charging the storage capacitor by a current proportional to the input voltage and subsequently discharging it at a constant rate. Through use of degenerated input devices driven by level shifted versions of the input voltage, a linear voltage-to-current converter is proposed to produce a linear voltage dependent current for almost the entire input range. The proposed VTC is designed and fabricated in a standard 0.13 μm CMOS technology. For a supply voltage of 1 V at 80 MHz sampling frequency, the measurement results confirm a small linearity error of below $\pm$ 1.4 % for the entire input range (0$\sim$1 V) while this value is below $\pm$ 0.5 % for the input range between 0 and 0.95 V corresponding to a resolution of 7.38 ENOB. The entire VTC occupies an area of 60μm$\times$60μm. The analog portion of the VTC consumes 16.8 $\sim$22.8 μW for 0 V $\sim$ 1V input range and the digital part consumes 1.8 μA at 80 MHz sampling rate. Details of the proposed VTC design are discussed in Chapter 2.

1.4.3 Efficiency Enhancement Techniques for Rectifiers

Three different techniques to enhance the efficiency of rectifiers for RFID tags are presented. These techniques extend the low-voltage (low-power) operation range of rectifiers.

1. **Proposed Efficient Rectifier with Low-Voltage Operation**: A new switching scheme is proposed to enhance the power efficiency of the conventional 4 transistor (4T)-cell rectifier. By switching the gate of charge-transfer transistors to the intermediate nodes of preceding and succeeding stages, low on-resistance and small leakage current are obtained simultaneously. To further improve the low-voltage operation capability, an external gate-boosting technique is also applied to the proposed design which enables an efficient operation for input voltage levels well below the nominal standard threshold voltage of MOS

transistors. The two proposed rectifier architectures are designed and laid out in a standard 0.13-μm CMOS technology. For a 950 MHz RF input and 10 kΩ output load, post-layout simulation results confirm a PCE of 74% at -10 dBm and 57% at -26 dBm for switched 4T-cell and gate-boosted switched 4T-cell, respectively. While the PCE of the proposed switched 4T-cell rectifier compares favorably with that of the state-of-the-art rectifier designs, the gate-boosted version achieves a relatively high PCE while operating with a very low input power. Details of the proposed rectifier design are discussed in Chapter 3.

2. **Proposed Rectifier with Low Start-Up Voltage**: To enhance the power conversion efficiency of the conventional rectifier when the input voltage (power) is low, appropriate gate-drive voltages for each stage of the rectifier are generated using a chain of auxiliary floating rectifier cells. Floating rectifier cells are optimized to generate shifted versions of the intermediate voltage of each stage to boost the drive voltage of NMOS and PMOS switching transistors and accordingly improve the PCE. The proposed rectifier architecture is designed in a standard 0.13 μm CMOS technology. For a 950 MHz RF input and 50 kΩ output load, simulation results show that the rectifier achieves a PCE of 54 % for a small input signal with an amplitude of 200 mV (-19 dBm) which is well below the nominal standard threshold voltage of MOS transistors in the technology used. Details of the proposed rectifier design are discussed in Chapter 3.

3. **Proposed Rectifier with an Extended High-Efficiency Region of Operation**: Using quasi-floating gate technique, a gate-biasing scheme is proposed to provide a relatively flat power conversion efficiency curve for a wide input voltage (power) range. The proposed technique also enables an efficient operation for input voltage levels well below the standard threshold voltage of the MOS switching transistors. Appropriate bias voltages for different stages of the rectifier are generated through a chain of low-power bandgap reference generators which impose minimal power and area overhead. The proposed rectifier architecture is designed and laid out in a standard 0.13 μm CMOS technology. For a 2.4 GHz RF input frequency and 30 kΩ output load, post-layout simulation results of the circuit show that a maximum PCE of 66.7 % is achieved for an input signal with an amplitude (power) of 0.45 V (-8 dBm). While a high PCE of 60 % is achieved for input voltage (power) levels

as low as 0.25 V (-15 dBm), PCE maintains above 60 % for a wide input voltage (power) range from 0.25 V to 0.7 V (-15 dBm to -3 dBm). Details of the proposed rectifier design are discussed in Chapter 3.

1.4.4 Proposed Dual-Band Approach for Wireless Power Harvesting

A wide band matching network is greatly desired for wireless power harvesting in the context of passive RFID tags. Typically, RFID tags are optimized for a single frequency band. Such an approach makes the tags inoperable at other frequency bands as the power harvesting unit fails to provide sufficient energy for proper operation of the tag due to excessive power reflections at the tags input. Due to geometrical limitations and size issues, it is practically impossible to incorporate an antenna that operate at a wide frequency range, or to allocate separate antennas for different bands. A viable approach is then to modulate the input impedance of the tag (rectifier) in response to the variations of the transmitted frequency rather than adjusting the antenna impedance. Built upon efficiency enhancement techniques developed in this thesis, a dual-band approach in RF rectifiers is proposed. Through dynamically adjusting the input capacitance of the rectifier, a dual-band input matching scheme is developed which enables efficient power delivery at two distinct frequencies. Details of the proposed dual-band approach are discussed in Chapter 3.

1.4.5 Proposed High-Sensitivity Fully Passive Wake-Up Radio

As mentioned in Section 1.3, in power-limited consumer wireless devices such as RFID systems, biomedical implants, wireless sensor networks, wearable components, and Internet of Things, energy saving is a critical design task. These devices are usually battery operated and have a radio transceiver that is typically their most power hungry block. Wake-up radio schemes can be used to achieve a reasonable balance among energy consumption, range, data receiving capabilities and response time. The wake-up radio (WUR) is comprised of a high-efficiency rectifier that rectifies the incident RF signal and drives subsequent circuit blocks including a low-power comparator and potentially a reference generators; and at the same time detects the envelope of the on-off keying (OOK) wake-up signal.

The WUR does not need an external power source as it extracts the entire energy from the RF incident signal received at the antenna. A proof-of-concept system based on a custom 0.13m CMOS rectifier is designed that supports addressing and short commands communication. Experimental results demonstrate the sensitivity of -21 dBm (without matching circuit) at 868 MHz. Using matching circuit a sensitivity of -33 dBm can be achieved. Details of the proposed passive WUR are discussed in Chapter 4.

1.4.6 Feasibility Study of Backscattering For Telemonitoring

As mentioned in Section 1.2, backscattering is a power efficient transmission scheme and is commonly used for passive RFID tags at short communication distances. The feasibility of backscattering for health-care telemonitoring using a stent as a the tag's antenna is investigated. Theoretical analysis suggest that backscattering scheme outperforms telemonitoring schemes based on active transmitters in terms of power consumption and reliability. A proof-of-concept prototype is designed and implemented and a set of experiments are carried out to study the feasibility of backscattering using an antenna stent (inductive stent). Details of this feasibility study are discussed in Chapter 4 and [8].

1.4.7 Proposed Ultra-Low-Power Voltage-Controlled Ring Oscillator

As discussed in Section 1.3, the clock generator is an integral part most passive RFID tags. Simple oscillators typically constitute the core of such clock generator circuits. In the context of RFID tags, the oscillator need to consume low power and should be capable to operate with low supply voltage. As a proof-of-concept to fulfill the aforementioned requirements, an ultra-low-power CMOS voltage-controlled ring oscillator (VCRO) is proposed. The design techniques employed in the high efficiency rectifiers are adopted to achieve the ultra low power consumption. The proposed two-stage VCRO is designed and laid-out in a standard 0.13 μm CMOS technology. A voltage level converter is also presented to interface the output of the proposed VCRO with the succeeding circuitry. The entire VCRO core occupies an area of $25\mu\text{m}\times20\mu\text{m}$. For a supply voltage of as low as 140 mV, an output frequency of 4 MHz is achieved at 3.6 nW power

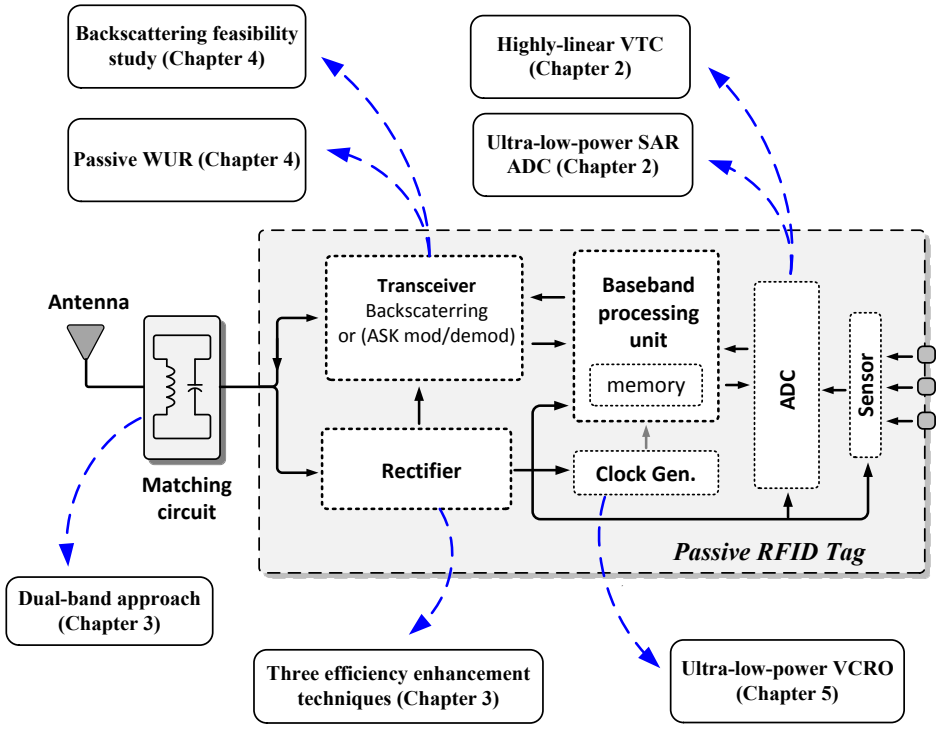


Figure 1.9: Schematic diagram different blocks of a passive RFID tag addressed in this thesis.

consumption. Although the intended application for the proposed VCRO is passive RFID tags, the architecture can be used in other ultra-low-power applications. Details of the proposed Ultra-Low-Power VCRO are discussed in Chapter 5.

1.5 Thesis Outline

In this thesis, design techniques to improve the performance of the main building blocks of a passive RFID tag are presented. The proposed designs involve circuit techniques to improve the performance of the associated blocks with an emphasis on low power consumption and layout area. Figure 1.9 shows how the contribution of this thesis address the different blocks of a passive RFID tag.

The organization of this thesis is as follows: Chapter 2 provides an overview of analog-to-digital converters for RFID tags. An ultra-low-power SAR ADC is proposed. TMSP concept is reviewed and a highly linear wide input range VTC as

the front-end for such systems is introduced and studied in details.

Chapter 3 reviews wireless power harvesting schemes in the context of RFID systems and wireless sensor networks. Three different efficiency enhancement techniques are applied to differential rectifiers and their performances are studied. Based upon the techniques developed, a dual-band approach is introduced which enables efficient power delivery to the tag at two distinct frequencies.

In Chapter 4 wake-up radio as an attractive approach to enable a power efficient receive mode for the passive tags and wireless sensor nodes, is reviewed and a fully-passive high-sensitivity wake-up radio is presented. Also, as a power efficient approach during the transmit mode, feasibility of backscattering in the context of wireless telemonitoring using an antenna stent is studied.

Chapter 5 proposes an ultra-low-power VCRO which serves as the core of the clock generator unit. The proposed VCRO employs the techniques developed for the high efficiency rectifiers to achieve low voltage operation and consequently, low power consumption.

Chapter 6 provides the concluding remarks, summary of achievements and future works.

Chapter 2

Efficient Data Converter Circuits for RFID Applications

As mentioned in Chapter 1, the operation of a sensor-enabled RFID tag is dependant on an on-chip ADC. ADCs are among critical components that are used in most of nature interface systems and usually consume a fair share of the overall power and chip area budget. Therefore, reducing the power consumption and silicon area requirements of the ADC can significantly benefit an efficient and robust tag design.

Among different categories of analog-to-digital converters, successive approximation register ADC is the most attractive candidate in virtue of its minimal use of analog circuity. With the comparator and a capacitive DAC array being the only analog blocks, SAR ADCs perform the conversion in a power efficient manner. SAR ADCs are capable of providing high speeds with medium resolution which suffices the requirements of most RFID applications. Power and area efficient implementation of SAR ADCs will be discussed in this chapter.

Another promising technique to efficiently implement the analog-to-digital conversion is the time-mode converters which will be discussed in this chapter.

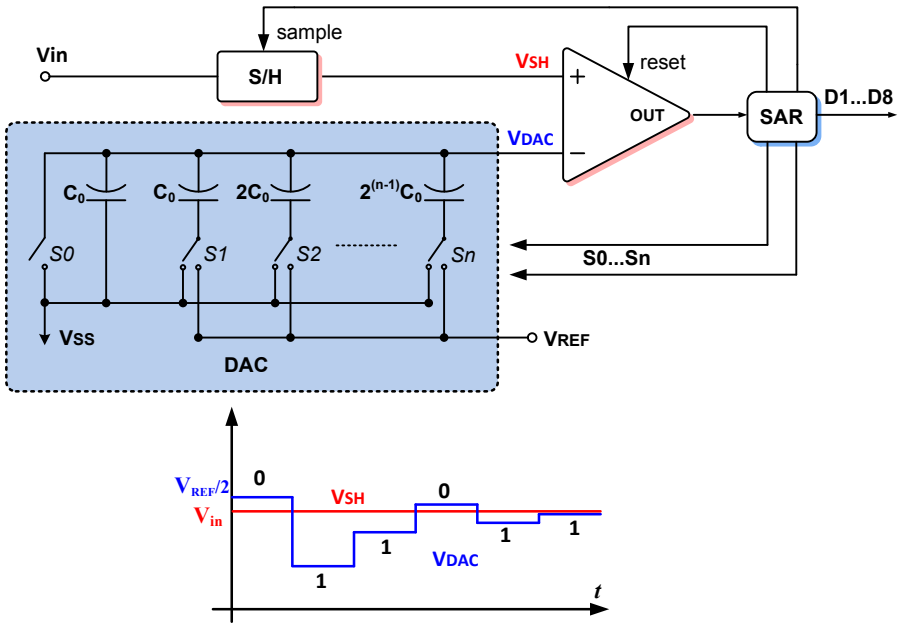


Figure 2.1: Schematic diagram of a conventional SAR ADC [6].

2.1 Overview of Successive Approximation Register Analog-to-Digital Converters

The binary capacitor array SAR ADC architecture was first introduced in 1975 by Gary L. Baldwin in [22] and [23]. SAR ADC performs the binary search algorithm in a feedback fashion in order to resolve the analog input. More specifically, as shown in Figure 2.1, the input is sampled during the first step. The sampled input is initially compared with half the reference voltage ($V_{ref}/2$). Depending on the the output of the comparator, SAR unit provides the appropriate switching signal for the capacitive DAC during the charge recycling step. The sampled input is compared with the updated DAC voltage (V_{DAC}) until all the bits are resolved.

Generally, in a SAR ADC there are two major contributors to power consumption: comparator and charging/discharging of the DAC array. Typical SAR structures use bulky DAC capacitive arrays which are usually the area and power bottleneck of the design. From the power dissipation perspective, in order to sample a full-scale sine wave at the Nyquist frequency, a traditional capacitive array on average consumes [24]:

$$P_{tot} = P_{in} + P_{ref} = \frac{C_T \cdot V_R^2}{T_s} + \frac{C_T \cdot V_R^2}{2T_s} \tag{2.1}$$

where P_{in} is the power drawn from the input, P_{ref} is the average power drawn form the reference generator for charge redistribution, C_T is the total capacitance of the array, V_R is the reference voltage and T_s is the conversion period. Accordingly, layout area and power consumption grow exponentially ($C_T = 2^n \cdot C_0$ where C_0 is the unit capacitor) with the number of bits (n) which compromises the advantage of SAR ADCs, especially as the number of bits increases.

Extensive studies have been carried out on energy-efficient DAC architectures. Ginsburg and Chandrakasan [25] propose the capacitor splitting scheme which reduces the average switching energy of the array by splitting the most significant bit (MSB) capacitor into $n-1$ binary scaled sub-capacitors (where n is the number of bits). Consequently, for down transitions [25], the charge on the MSB capacitor will be restored for further conversions. Although the proposed technique significantly saves the switching energy for small output codes, it fails to perform equally well for higher output codes where less down transitions occur. Moreover, this approach is still dependent on a bulky DAC array and requires twice as many switches as the conventional scheme.

In another structure, Choi and Tsui [26] reduce the average switching energy of the capacitive array by separating the decoding of MSB and least significant bit (LSB) through using two different capacitor arrays with unequal size. However, the low-power consumption is achieved at the cost of two additional clock cycles which poses energy overhead due to additional comparison steps required. Moreover, the layout occupies a higher area than that of the traditional architecture due to MSB DAC, memory storage with logic and the extra comparator.

Sauerbrey *et al.* [27] use an extra shunt capacitor in the capacitive array to adjust the signal levels in order to facilitate low voltage operation. The DAC voltage converges to the input voltage with each conversion and therefore, the leakage of the switches are avoided for small supply voltages. This architecture requires a dedicated sample-an-hold unit as the input voltage is not directly sampled on the capacitive DAC.

Agnes *et al.* [24] use an attenuation capacitor to reduce the total size of the capacitive array and consequently the energy drawn from the reference. Kianpour *et al.* [28] divide the conversion steps into coarse and fine phases while a resistive

DAC is used for coarse conversion and a capacitive DAC is used for fine conversion. Only two capacitors are used for fine binary search and therefore, layout area and power consumption are reduced.

[29] drives the bottom plate of DAC capacitors through inverters and use an attenuation capacitor to keep the peak-to-peak differential output voltage of the DAC within the rail to rail range. Geng *et al.* [30] use a dummy capacitor which is switched between GND and the common-mode voltage therefore reducing the total capacitance of the array to half of the value required for a convectional DAC.

Hu *et al.* [31] samples the input on one DAC use a secondary auxiliary DAC to compensate the voltage error caused by the parasitic capacitors at the main DAC. MSB is resolved by the auxiliary DAC and the rest of the bits are decided by the main DAC. Therefore, the total capacitance of both DACs is the same as that of a conventional DAC. The proposed scheme allows using half the reference voltage to resolve the entire range and therefore brings a significant power reduction.

In general, there are several common techniques to reduce the power consumption and area requirements of the capacitive DAC [31, 32] namely:

1. Use of attenuation capacitor to reduce the size of the DAC [33]. This technique adversely affects the accuracy of the capacitive DAC.

2. Charging the DAC through several intermediate voltages [34]. This method poses extra complexity overhead for intermediate voltage generation.

3. Recycling the charge stored in the capacitors [25, 35]. This scheme requires twice as many switches compared to the conventional approach.

4. Performing monotonic switching scheme [36]. This method in not applicable to single-ended architecture.

5. Using merged capacitor switching method [37]. This method is sensitive to the reference voltage accuracy.

6. Employing V_{CM}-based switching method [38]. This method is sensitive to the reference voltage accuracy.

This report proposes an area-efficient DAC architecture that both reduces the power consumption and the layout area. The proposed DAC architecture consists

of four minimum-sized capacitors and two low-power buffers for which the binary search algorithm is carried out at no extra cost in terms of clock cycles and comparison steps. Also, the use of four minimum-sized capacitor DAC relaxes capacitor mismatch and parasitic requirements. To further save area and power consumption, the two low-power buffers are dually used as the comparator preamplifier blocks in an open-loop fashion [6].

2.2 Ultra-Low-Power SAR ADC with an Area-Efcient DAC Architecture[1]

The operating principles of a SAR converter are well known [22–38]. Simply put, the capacitive DAC main task is to provide the appropriate voltage levels to implement the binary search algorithm as shown in Figure 2.1. The algorithm starts by setting the MSB to 1 and all other bits to 0. Thereby, V_{in} is compared with $V_{ref}/2$. Charge recycling is then carried out based on the output of the comparator, i.e., if D_1 (comparator output) is high, the second largest capacitor is charged to V_{ref} setting $V_{DAC} = \frac{3V_{ref}}{4}$. This is called an up transition. Conversely, if D_1 is low, the largest capacitor is discharged and the second largest one is charged to V_{ref} which is called a down transition. The sequence continues until all the bits are decided. The binary search algorithm described above can be interpreted as follows: two voltage levels are dened as V_{top} and V_{bot} which are the upper and lower voltage bounds at each clock cycle and they converge toward V_{in} with each bit decision. V_{mid} is then produced from V_{top} and V_{bot} as:

$$V_{mid} = \frac{V_{top} + V_{bot}}{2} \tag{2.2}$$

For the m^{th} bit, this voltage, i.e., the output of the DAC, is compared with V_{in} and the comparison result D_m updates the value of V_{top} or V_{bot} in the next clock cycle such that if $D_m = 1$ ('up' transition), V_{top} maintains its old value while V_{bot} is shifted up to V_{mid}. Conversely, if $D_m = 0$ ('down' transition), V_{bot} retains the old value and V_{top} is shifted down to V_{mid}. The procedure continues until all bits are concluded.

[1] The material presented in this section is based on [6].

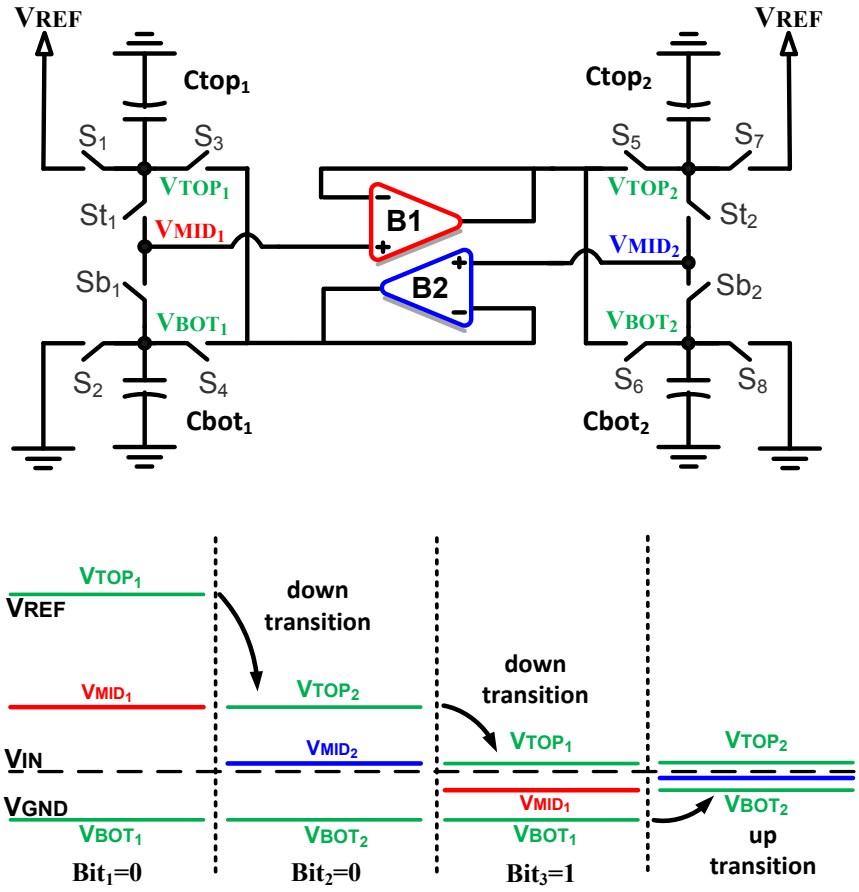


Figure 2.2: Schematic of the proposed DAC architecture and its timing diagram [6].

As shown in Figure 2.2 the algorithm can be implemented using four capacitors and two unity gain buffers. For a given output of '001...' (where the first three bits are evaluated) the operation of the proposed DAC architecture can be described as follows:

Each bit decision cycle is divided into two time slots, comparison cycle and charge recycling cycle. During each comparison cycle one capacitor set (C_{topi}, C_{boti}) performs as a capacitive divider producing $V_{mid} = \frac{V_{top}+V_{bot}}{2}$ and the other set holds the same two voltage levels (V_{top}, V_{bot}) that are being processed (the two capacitor sets interchangeably switch these two tasks in subsequent comparison cycles). Voltage levels are then updated at charge recycling cycle

based on the previous decision. At the beginning of conversion (sampling phase), (S_1, S_7) and (S_2, S_8) are on, charging (C_{top1}, C_{top2}) and (C_{bot1}, C_{bot2}) to V_{REF} and V_{GND}, respectively. Then in the first comparison cycle, (S_1, S_2) and (S_7, S_8) turn off and (S_{t1}, S_{b1}) turn on to form a capacitive divider (from C_{top1}, C_{bot1}) which gives $V_{MID1} = \frac{V_{REf}}{2}$. Note that as stated earlier when each capacitor set is active, i.e., providing V_{MID} for comparison $\left(C_{top1}, C_{bot1}\right)$, it is essential that the other capacitor set $\left(C_{top2}, C_{bot2}\right)$ holds the same voltage levels being searched at the time, which in this case is $V_{TOP2} = V_{REF}$ and $V_{BOT2} = 0$.

Then V_{MID1} is compared with V_{IN} which yields $D_1 = 0$ based on the assumption made for the first three bits. Voltage levels are updated in the succeeding charge recycling cycle. As mentioned earlier for each 'down' transition V_{bot} maintains its value and V_{top} is shifted down to V_{MID}. For this purpose, (S_{t1}, S_{b2}) and (S_4, S_5) are switched on while all other switches are off. Buffer B_1 provides a copy of V_{MID1} for C_{top2} thus shifting V_{top2} down to V_{MID1}. At the same time, buffer B_2 returns C_{bot1} voltage back to $V_{BOT1} = V_{GND}$ in order for $\left(C_{top1}, C_{bot1}\right)$ to have a copy of new voltage levels that are to be processed in the next comparison cycle. At this point, $V_{top1} = V_{top2} = \frac{V_{REF}}{2}$ and $V_{bot1} = V_{bot2} = 0$ and the capacitors are all set for the next comparison cycle where (S_{t2}, S_{b2}) turn on and all other switches are off. The capacitive divider produces $V_{MID2} = \frac{V_{TOP2}+V_{BOT2}}{2} = \frac{V_{REF}}{4}$. This voltage is compared with V_{in} and results in $D_2 = 0$ which corresponds to a 'down' transition. In the next charge recycling cycle, (S_{t2}, S_{b1}) and (S_3, S_6) are switched on. Buffer B_2 shifts V_{TOP1} down to $V_{MID2} = \frac{V_{REF}}{4}$ and buffer B_1 returns V_{BOT2} back to V_{GND} such that $V_{top1} = V_{top2} = \frac{V_{REF}}{4}$ and $V_{bot1} = V_{bot2} = 0$. Therefore, in the next comparison (C_{top1}, C_{bot1}) produce $V_{MID1} = \frac{V_{REF}}{8}$ which yields $D_3 = 1$. In the next charge recycling cycle (S_{t2}, S_{b1}) and (S_3, S_6) are switched on. Buffer B_1 pulls V_{BOT2} up to $V_{MID1} = \frac{V_{REF}}{4}$ and buffer B_2 returns V_{TOP1} back to $\frac{V_{REF}}{2}$. All the next bits are decided in the same manner.

In terms of power, the proposed architecture outperforms the conventional SAR architectures. As the algorithm suggests, during a conversion cycle, each of the two buffers contributes in the charge recycling process for at most n times. So, the total

charge drawn from V_{REF} during the conversion cycle is:

$$Q_{tot} = 4 \cdot n \cdot I_b \cdot T_{CR} \tag{2.3}$$

where n is the number of bits, I_b is the bias current for each buffer stage, T_{CR} is the charge recycling period and the factor '4' accounts for the two, two-stage amplifiers. The two factors governing I_b are the required voltage gain and speed. To achieve the desired resolution, the buffer output has to settle within $\frac{1}{2}$LSB of the input, which for an 8-bit resolution requires an open loop gain on the order of 50 to 60 dB. The two-stage low-power amplifier (described in Section 2.2.1) provides such a gain by drawing only 124 nW from V_{REF}. Regarding speed, since the load capacitance is minimum-sized, slew-rate is not that critical and charge-recycling period (V_{CR}) can be very short.

The aforementioned algorithm is implemented in the proposed ADC with some minor amendments. To further save power, the buffers turn off whenever their service is not required. This is achieved by shutting off the supply current (the buffer architecture is described in Section 2.2.1). An example for such a power saving mode is when the destination voltage, V_{TOP} or V_{BOT} is supposed to be updated to V_{REF} or V_{GND}, respectively. In this situation the respective buffer will not perform the task, instead one of (S_1, S_7) or (S_2, S_8) turns on to update V_{TOP} or V_{BOT} to V_{REF} or V_{GND}, respectively. This power saving scheme proves useful particularly for very large or very small inputs. For instance, for a very small output code starting with several consecutive '0's (0000...), at each charge recycling cycle, one buffer remains inactive until the first '1' is detected. The same goes for very large output codes.

2.2.1 Comparator Architecture

As mentioned in Section 2.2, to further save area and power, the two buffers employed in DAC are used as the preamplifier stages for the comparator by opening the loop through $\overline{CLK_{comp}}$, as shown in Figure 2.3.

At each comparison phase, one capacitor set provides V_{MID} to be compared with V_{IN} for which the appropriate clock (CLK_{comp1} or CLK_{comp2}) goes high. To better utilize the available hardware, the two amplifiers operate simultaneously to

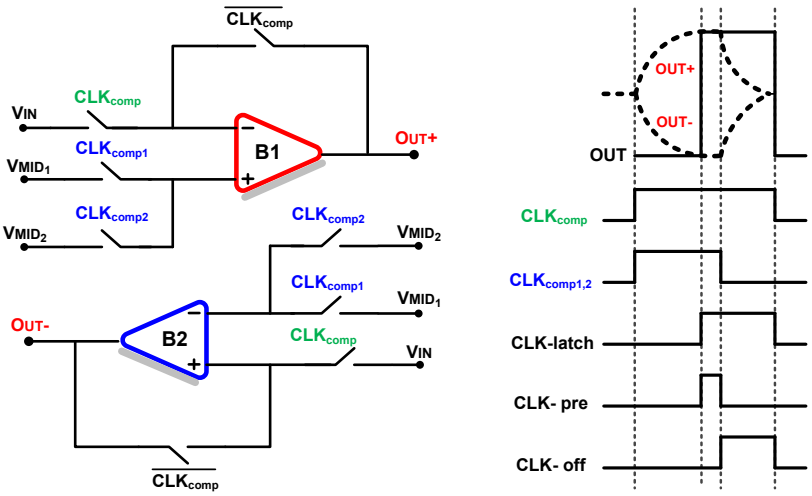


Figure 2.3: Schematic of the proposed comparator and its timing diagram [6].

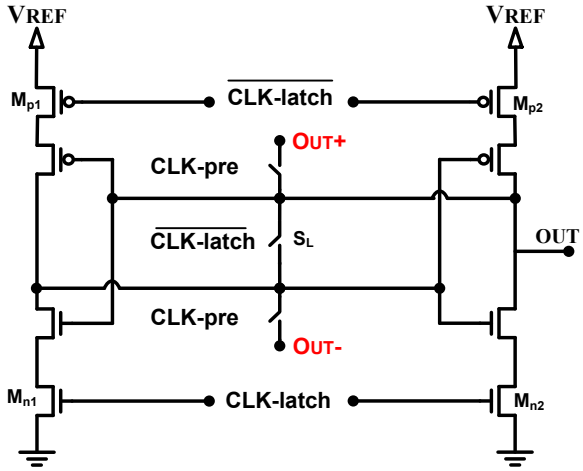


Figure 2.4: Schematic of the low-power latch architecture [6].

amplify the voltage difference between the input voltages. For this purpose V_{IN} and V_{MIDi} are applied to opposite terminals of B_1 and B_2. Thus, as one of OUT+/OUT- charges up to V_{REF}, the other one is pulled down to V_{GND}. This scheme brings a twofold benefit: on one hand, the pre-amplification phase would be twice as fast. On the other hand the overall comparator resolution is improved.

Almost at the end of comparison cycle where OUT+ and OUT- are about their

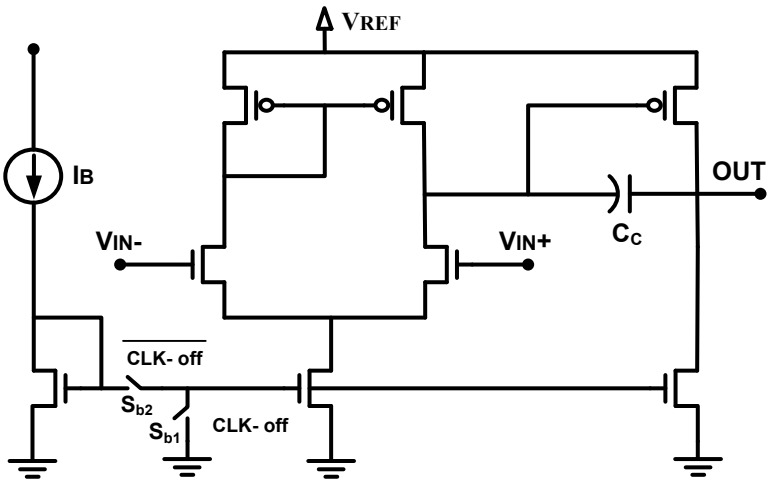


Figure 2.5: Schematic of the low-power amplifier [6].

extreme voltage levels (note that clock periods are not drawn to scale in Figure 2.3), a very short pulse CLK_{pre}, connects OUT+ and OUT- to the input terminals of the regenerative latch as shown in Figure 2.4. CLK_{pre} turns off after a short period so that B_1 and B_2 do not drive the latch for the rest of the latch cycle. The buffer/amplifier architecture is shown in Figure 2.5. After the pre-amplified voltages are properly delivered to the latch at the end of CLK_{pre}, CLK_{off} goes high which turns the amplifiers off by shutting off the bias currents through $S_{b1,2}$.

Latch phase starts simultaneously with CLK_{pre} and the regenerative latch produces a digital level output in a very short interval. At the end of process, S_L resets the latch by connecting the input and output of the back-to-back inverters to set them close to $\frac{V_{REF}}{2}$ which speeds up the next latch operation. To further save power, $M_{n1,2}$ and $M_{p1,2}$ perform the power-gating task by blocking the latch input current in inactive mode when CLK_{latch} is off.

2.2.2 Sample and Hold Architecture

A switched-capacitor clock-boosted architecture is used for the sample-and-hold circuit due to its rail-to-rail capability and low-power operation. As shown in Figure 2.6, after a few clock periods, C_{boost} is charged to V_{REF} and subsequently acts as a floating voltage source. At each sampling phase (CLK_{SAMPLE}), C_{boost} connects the gate-source terminals of M_{sample} in such a way that: $V_{GS} = V_{REF}$. Therefore in sampling phase, the gate voltage of M_{sample} will always be as much

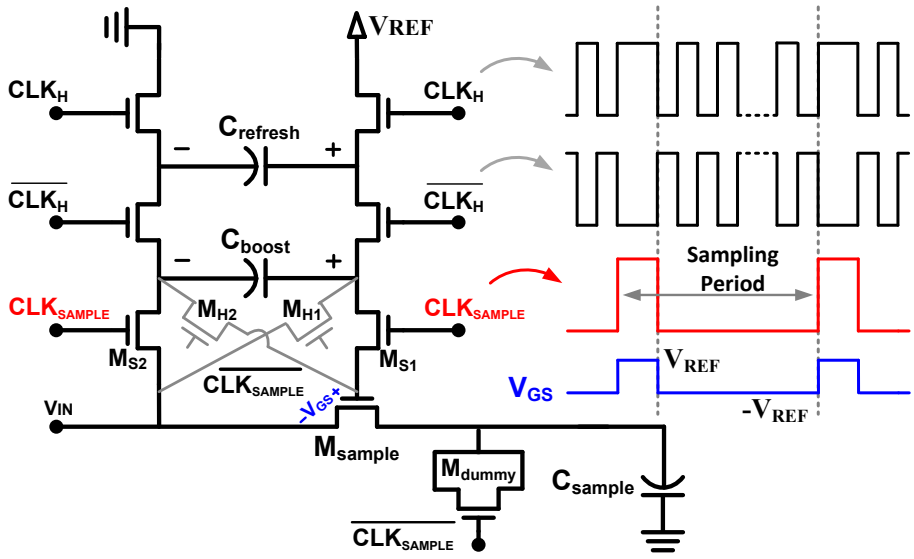


Figure 2.6: Schematic of the Proposed sample-and-hold architecture and timing diagram [6].

as V_{REF} higher than its source voltage, regardless of the value of V_{IN}. This presents a rail-to-rail operation. On the other hand, in the hold phase, M_{H1}, M_{H2} turn on and M_{S1}, M_{S2} turn off, providing a negative voltage between the gate-source terminals of M_{sample} such that for the entire hold phase: $V_{GS} = -V_{REF}$. This negative bias alleviates the leakage current and fully isolates the sampled voltage from input fluctuations.

CLK_H can be picked from any of the clock signals already generated in the circuit, however, for a better performance, it has to be a high frequency clock such as CLK_{comp}. As shown in Figure 2.6, $C_{refresh}$ updates the voltage on C_{boost} at every $\overline{CLK_H}$. M_{dummy} is employed to cancel the charge-injection effect. However, special care has to be given to the size of M_{dummy} which is not the conventional $\frac{Size_{MSample}}{2}$ due to the fact that the gate-source voltages that the two transistors experience are not the same. Note that this architecture almost imposes no power consumption penalty as the current drawn from V_{REF} is limited to the leakage current of C_{boost} and switching transistors and thus is on the order of few nano-Watts.

2.2.3 Simulation Results

The proposed DAC/comparator architecture is designed and laid out in an 8-bit 25kS/s SAR ADC in a 0.13μm CMOS technology. DAC capacitors are

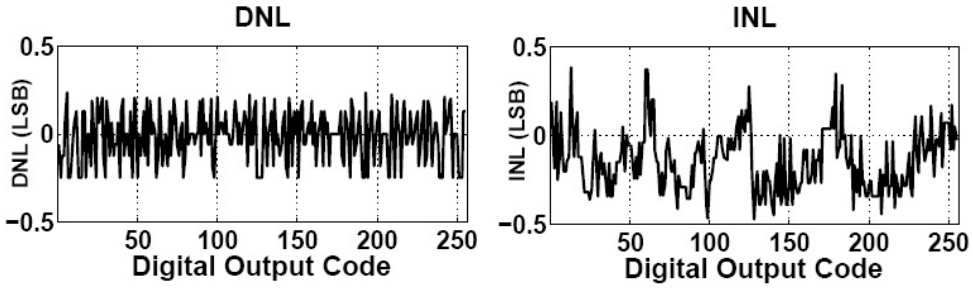


Figure 2.7: Simulated DNL and INL at 25ks/s [6].

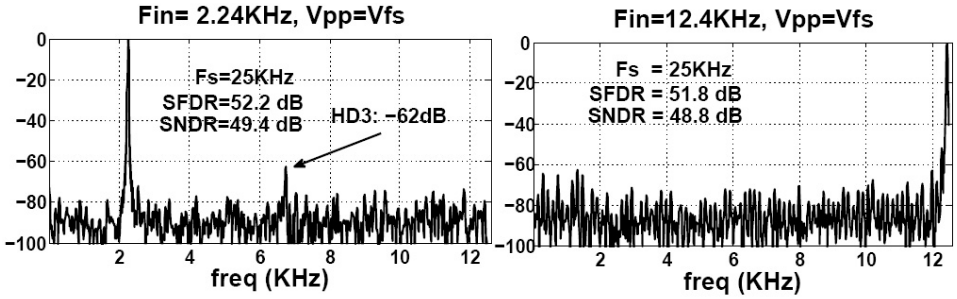


Figure 2.8: Output spectra for input sine wave @ 2.24kHz and 12.4kHz [6].

implemented by a metal-insulator-metal (MIM) structure with the unit capacitor of 50 fF and the sampling capacitor is 500 fF.

As shown in Figure 2.7, at 25kS/s the simulated differential nonlinearity (DNL) and integral nonlinearity (INL) are within 0.25 LSB and 0.5 LSB, respectively. The spectra for an input full-scale sine wave at 2.24 kHz and 12.4 kHz are shown in Figure 2.8, for which the signal-to-noise and distortion ratio (SNDR)s of 49.4 dB (ENOB=7.91) and 48.8 dB (ENOB=7.81) are obtained, respectively.

The entire digital circuitry is custom designed and dissipates 24 nW from a 0.6 V supply. The total power consumption for 2.24 kHz and 12.4 kHz input sine-wave are simulated to be 290 nW and 350 nW which exhibits a FoM of 48 fJ/conversion-step and 62 fJ/conversion-step, respectively. A comparison of the proposed architecture with the state-of-the-art SAR ADCs is provided in Table 2.1.

Table 2.1: Comparison of the proposed SAR ADC with the state-of-the-art results [6].

	[39]*	[40]*	[41]*	[42]**	This work**
Technology (μm)	0.18	0.18	0.13	0.13	0.13
Supply Voltage (V)	1 (1)	0.9	1.2	1	A: 0.8, D: 0.6
Sampling Rate^{f_s} (kS/s)	200 (100)	200	1000	100	25
Input Frequency$^{f_{in}}$ (kHz)	100 (50)	100	101	48.5	12.4
ENOB (@f_{in})	7.96 (10.55)	7.44	8.39	9.17	7.81
Power Dissipation (μW)	19 (25)	2.47	150	1	0.35
FoM† (fJ/conversion-step)	381 (166)	65	437‡	17	62

$\star$Measurement results. $\star\star$ Simulation results. † FoM = $P_{diss}/(2 \cdot f_{in} \cdot 2^{ENOB})$ ‡ FoM = $P_{diss}/(f_s \cdot 2^{ENOB})$

2.3 Overview of Time-Mode Analog-to-Digital Converters

Emerging deep sub-micron CMOS technologies are basically optimized to benefit a digital implementation. As transistor dimensions constantly decrease with each process node to facilitate higher integration, the reduction of applicable voltage levels poses severe challenges to the performance of analog and mixed-signal blocks.

To address the ever-increasing challenges of analog design in deep sub-micron CMOS technologies, TMSP has gained an extensive attention in recent years. A TMSP system converts the voltage/current signal to a modulated pulse width or a proportional time delay (in the form of the time difference between the rising and/or falling edges of a reference clock and delayed clock). The time mode signal (i.e., the proportional delay) could then be processed by a digital processing unit, therefore eliminating the need for the challenging analog blocks such as operational amplifiers and comparators. Furthermore, an all-digital process facilitates the implementation with smaller supply voltages, lower cost and higher integration level. Owing to its numerous advantages over the conventional analog domain processing, TMSP systems are recently being used in a wide range of applications including digital oscilloscopes and digital phase locked loop (PLL)s, implantable biomedical devices, sensor interface units, RADAR applications and

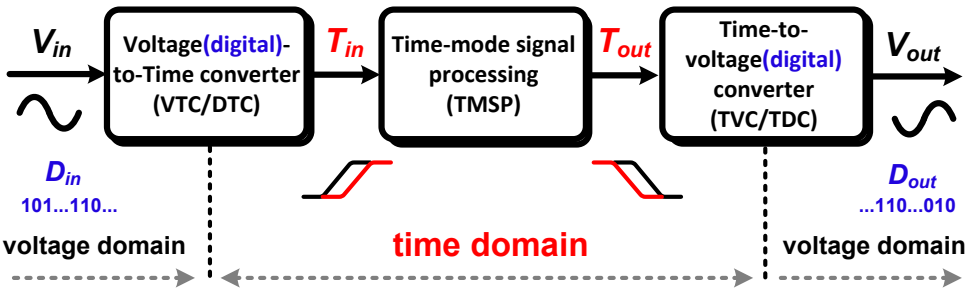


Figure 2.9: Schematic diagram of a generic TMSP system.

many more [21, 43–45].

As schematically shown in Figure 2.9, a TMSP system generally consists of three main building blocks, namely the VTC, the time-mode-signal processing unit and the time-to-voltage converter (TVC). Similarly as shown in the figure, the input to the system and its corresponding output can be digital signals, suggesting a digital-to-time converter (DTC) as the input block and a time-to-digital converter (TDC) as the output block.

As the name suggests, the VTC (DTC) block is mainly responsible for converting the input voltage signal to the proportional time difference (delay). Other useful functions such as voltage-to-time addition and voltage-to-time integration could also be performed at the interface between the voltage and time domain [21, 46].The time-mode signal processor is the core of the TMSP system and allocates the time-mode counterparts of the main building blocks of a conventional analog/mixed-signal system such as comparators, amplifiers, counters, ring oscillators, delay locked loops (DLL)s, etc. [47, 48]. Finally, the TVC (TDC) converts the processed time-mode signal back to an analog (digital) signal by quantizing the time difference (delay) between the appropriate edges of clock signals and producing a proportional analog voltage (digital code). To perform the conversion between time and voltage (digital) domain, the TVC (TDC) unit mainly relies on Vernier delay lines and DLLs to produce accurate reference clock signals [49].

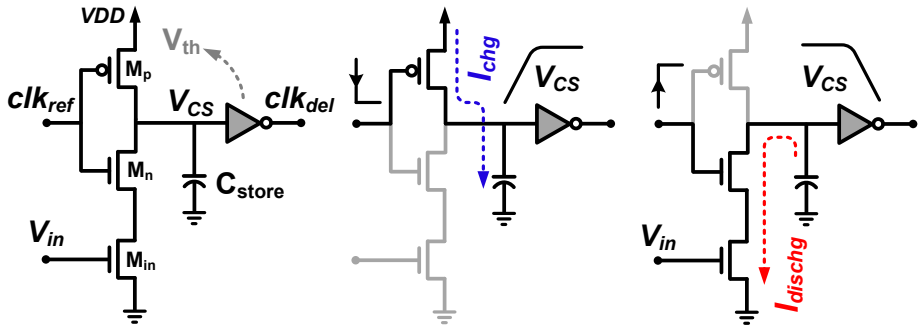
2.4 Highly-Linear Wide Input Range Voltage-to-Time Converter for Time-Mode Signal Processing

As discussed in Section 1.3, TMSP is desirable alternative for voltage domain conventional analog-to-digital converters. Transferring the processing load to digital (time) domain is particularly beneficial in the context of RFID tags as it facilitates low-power and small-area implementation of the analog-to-digital converter. As the interface between the voltage and time domains, the VTC unit plays a key role in TMSP systems and its performance directly affects that of the entire system. Among various criteria, high linearity and wide input range are two crucial performance metrics a VTC has to offer in most of applications (specially in time-mode data converters). In this work, through re-ordering the charge/discharge cycles in conventional current-starved VTC and by using degenerated input devices driven by shifted versions of the input voltage, a VTC is proposed to address both high linearity and wide input range simultaneously.

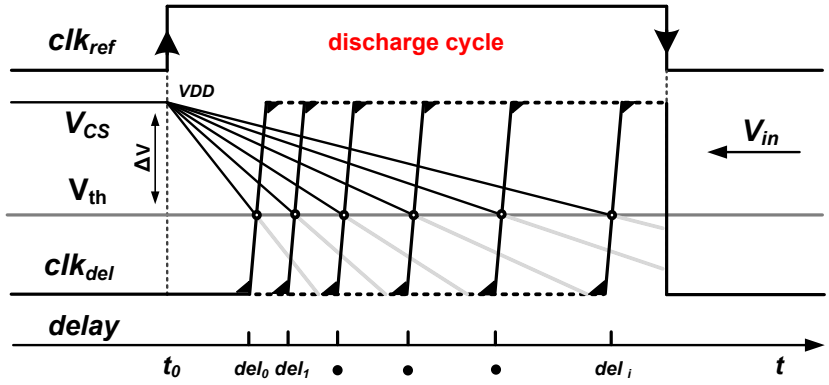
2.4.1 Conventional Current-Starved VTC

As mentioned in Section 2.3, in order to obtain an accurate time domain representation of the input voltage signal, the VTC block has to provide a linear relationship between the input voltage and the corresponding output delay. Typically, the so-called current-starved (CS) inverter is the most attractive candidate to perform the voltage-to-time conversion in many applications due to its simplicity.

A generic current-starved VTC is shown in Figure 2.10a. As seen in the figure, a basic CS-VTC incorporates two inverters in cascade, with a fixed capacitor placed at the output of the first inverter. During the low signal at clk_{ref} (charge cycle), the storage capacitor C_{store} is charged through M_P to VDD setting $clk_{del} = 0$ at the output of the second inverter. Note that M_P and C_{store} are designed so as to guarantee $V_{cs} = VDD$ within the charge cycle. Upon arrival of the rising edge of clk_{ref}, C_{store} starts to discharge through M_n and M_{in}. The second inverter performs as a comparator, mountainously comparing its input voltage V_{cs} with its internal threshold voltage V_{th}. Once the constantly dropping V_{cs} intersects V_{th}, the second inverter triggers to set $clk_{del} = 1$ as schematically shown



(a)



(b)

Figure 2.10: Conventional current-starved VTC. (a) Circuit level schematic for charge and discharge cycles, (b) Timing diagram.

in Figure 2.10b. Note that, as opposed to the charge cycle, the discharge current (i.e., the dropping rate of V_{cs}) is controlled by the input voltage V_{in}, modulating the drain-source resistance of M_{in} or equivalently, the discharge current I_{dischg}. the resulted delay is measured between the rising edge of clk_{ref} (t_0 in Figure 2.10b) and the rising edge of clk_{del} which is (inversely) proportional to the input voltage V_{in}. More specifically, (disregarding the minor effect of V_{cs} variations on I_{dischg}) the delay is given by:

$$\text{delay} = \frac{C_{store} \cdot \Delta V}{I_{dischg}} \tag{2.4}$$

where, $\Delta V = VDD - V_{th}$ (as shown in Figure 2.10b) and I_{dischg} is related to the

input voltage V_{in} by $I_{dischg} = G_{M,in} \times V_{in}$ (where $G_{M,in}$ is the large signal transconductance of the input transistor M_{in}). According to Equation 2.4, there are two issues which severely prevent a linear relation between the resulting delay and the input voltage V_{in}. Firstly, even for a perfectly linear relationship between I_{dischg} and V_{in} (i.e., a constant $G_{M,in}$ for the entire input range), Equation 2.4 suggests that delay is inversely proportional to V_{in}. More specifically, assuming a constant $G_{M,in}$, delay is given by:

$$\text{delay} = \frac{k}{V_{in}} \qquad \left(k = \frac{C_{store} \cdot \Delta V}{G_{M,in}}\right) \tag{2.5}$$

Furthermore, the transconductance of M_{in} ($G_{M,in}$) is not constant during the discharge cycle. In other words, I_{dischg} is a non-linear function of both V_{in} and time. As schematically shown in Figure 2.11, for small enough input voltages ($V_{in} < V_X + V_{th,Min}$), both M_n and M_{in} start conducting in saturation at the beginning of the discharge cycle since $V_{cs} = VDD$. As long as both M_n and M_{in} are in saturation, M_{in} draws a rather constant current proportional to $(V_{in} - V_{th\,M,in})^2$. The cascode transistor M_n assists in establishing a constant current by shielding the drain of M_{in} form the voltage variations of V_{cs} (i.e., $\Delta V_X \ll \Delta V_{cs}$). However, the constantly dropping V_{cs} will eventually push the transistors into triode region compromising the constant discharge current. As the gate of M_n is connected to VDD, it will enter triode before M_{in} does, coupling V_{cs} variations on V_X. With further decrease in V_{cs}, M_{in} enters triode which completely eliminates the established constant current. As schematically shown in Figure 2.11 for a given V_{in}, the transition instants are input dependent and if occur before the trigger point ($V_{cs} = V_{th,inv}$) will exacerbate the non-linearity. Note that typically a weak NMOS with a small aspect ratio (M_{aux} as shown in Figure 2.11) with its gate tied to VDD (or its drain) is placed in parallel with the input transistor to assist discharging the storage capacitor for small input voltages.

Based on the above discussion, discharge current is a non-linear, time-variant function of the input voltage which severely complicates obtaining a closed form expression for I_{dischg} versus V_{in}. For a clock frequency of 80 MHz, $C_{store} = 100$ fF and VDD=1V, the simulated delay time versus input voltage is shown in Figure 2.12. The average discharge current produced by M_{in} (excluding the

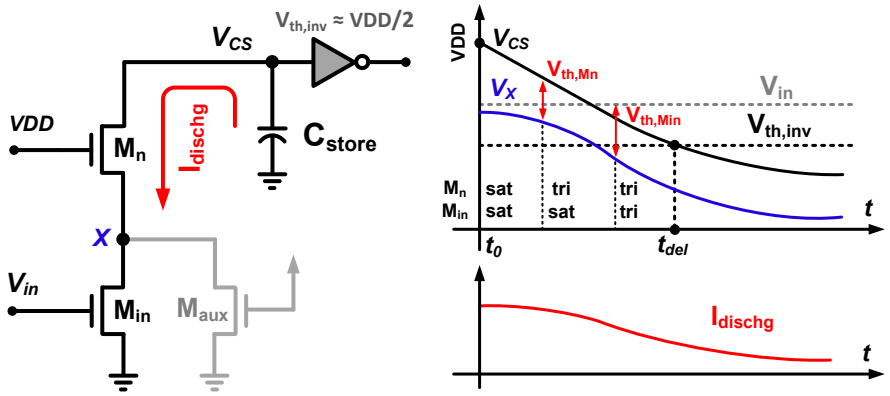


Figure 2.11: Schematic diagram of transient discharge current and voltage levels of the current-starved VTC.

current drawn by M_{aux}) versus the input voltage is also shown in the figure. As shown in the figure, the linear relation between the delay and input voltage occurs for a very narrow range of input voltages typically located in the middle of the input range. The non-linear drain current of the input device (M_{in}) averaged during the discharge cycle is also shown in the figure. As can be seen from the figure, this current complies with the I_d-V_{gs} curve of an NMOS and therefore, the input device fails to contribute in the discharge of the storage capacitors for input values smaller than its threshold voltage, produces a non-linear current in the saturation and is pushed to triode region for large input values.

It is worth mentioning that due to its simplicity, current-starved VTC is still the most attractive candidate in applications where a small input range is required. An example of such applications in which the current-starved VTC is widely used is the voltage-controlled delay unit (VCDU) in DLLs.

Numerous studies exist in the literature targeted to improving the performance of CS-based VTCs. Pekau *et al.* [50] employ several parallel current starving devices along with source degeneration in order to simultaneously improve the linearity and voltage sensitivity. The proposed VTC achieves a linear input range of 200 mV ($0 \sim 200$mV for a supply voltage of 1.2V) at a sensitivity of 2.5 ps/mV (2% error). Keskin [51] enhances the linear range through incorporating two delay lines in parallel such that the input voltage is applied to the positive supply of one and to the negative supply of the other. The desired output delay is extracted from the output of either delay lines according the input voltage through use of two

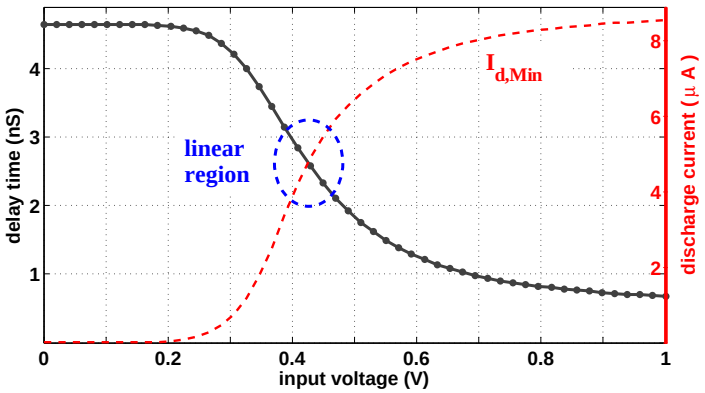


Figure 2.12: Simulated delay-time and discharge current versus input voltage for the conventional current-starved VTC.

decision comparators. Although the design presented in [51] achieves a rail-to-rail input range, the resulted delay is still dependent on the resistance of PMOS/NMOS devices in triode region and is therefore not perfectly linear. Macpherson *et al.* [52] use a voltage controlled tunable MOSCAP in parallel with the starving NMOS to control the gain (sensitivity) of the CS VTC and achieves a 100 mV linear range with a tunable gain.

2.4.2 Proposed Linearization Technique

Based on the discussion provided earlier, in order to achieve a wide linear input range for a dual-slope integrating VTC (which operates based on charging and discharging a capacitor), two requirements have to be satisfied:

1. A linear relation between the delay and the charge (or discharge) current has to be established (as opposed to Equation 2.4).

2. A linear relation between the charge (or discharge) current and the input voltage (i.e., a constant G_m voltage-to-current converter) has to be established.

In view of Equation 2.4, the first requirement (i.e., a linear relation between V_{in} and I_{dischg}) could be met by reversing the order of input proportional charge and discharge, i.e., initially charging the storage capacitor at a rate proportional to the input and subsequently discharging it at a constant rate. Such a scheme

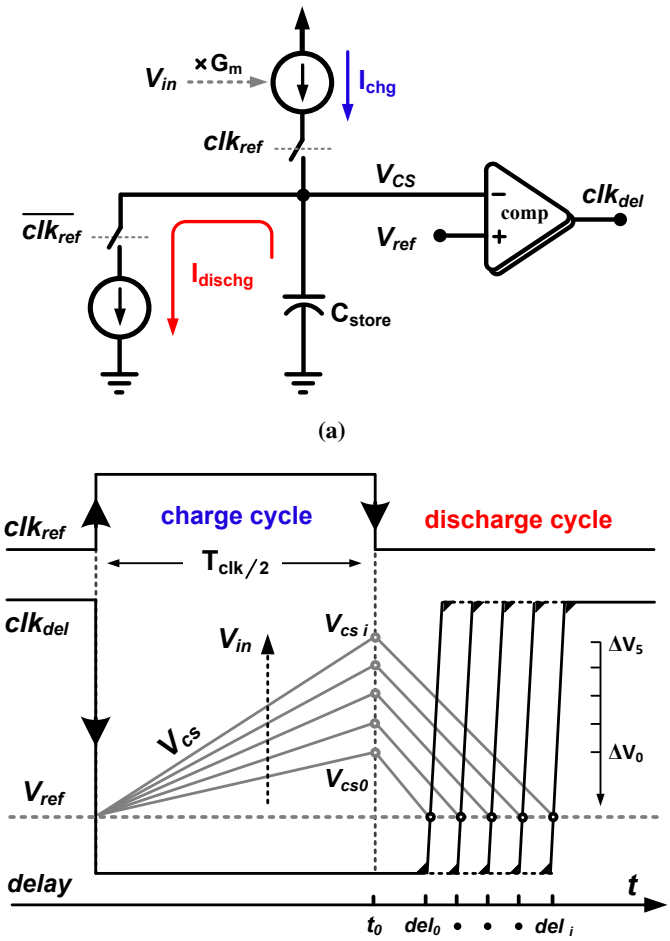


Figure 2.13: Proposed charge and discharge scheme. (a) Circuit level schematic, (b) Timing diagram.

is schematically shown in Figure 2.13a where C_{store} is initially charged through the variable current source at a rate proportional to the input voltage (i.e., $I_{chg} = G_m \times V_{in}$). C_{store} is subsequently discharged at a constant rate and the comparator triggers clk_{del} once $V_{cs} = V_{ref}$. Without lose of generality, one can assume $V_{ref} = 0$, therefore the capacitor voltage at the end of charge cycle is:

$$V_{cs}|_{t_0} = \frac{G_m \cdot V_{in} \cdot \Delta T}{C_{store}} \qquad \left(\Delta T = \frac{T_{clk}}{2}\right) \tag{2.6}$$

Therefore, as shown in Figure 2.13b, the delay is given by:

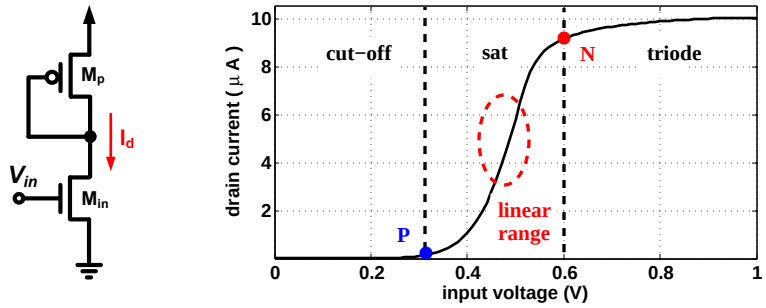


Figure 2.14: NMOS input device with diode-connected load. (a) Circuit level schematic, (b) Drain current versus input voltage.

$$\text{delay} = \frac{C_{\text{store}} \cdot V_{\text{cs},t_0}}{I_{\text{dischg}}} = k' \cdot V_{\text{in}} \quad \left(k' = \frac{G_m \cdot T_{\text{clk}}}{2 \cdot I_{\text{dischg}}} \right) \tag{2.7}$$

According to Equation 2.7, for a constant T_{clk} and I_{dischg}, a linear delay profile could be obtained provided that G_m remains constant regardless of V_{in} variations.

Extensive studies on constant-G_m input stages exist in the literature [53–56]. The well-known complementary input architecture suffers from strict n-channel and p-channel matching requirements and typically needs sophisticated g_m control circuitry. The dual n-channel/p-channel approach also requires a control unit to cancel the undesirable g_m variations. Generally, the complexity associated with such designs stems from the fact that the input stages need to satisfy both small-signal and large-signal requirements simultaneously. However, in the context of an integrating VTC where the input is either sampled or its variations is negligible during a clock cycle, a simpler approach will suffice.

An NMOS input device with a diode-connected load along with its simulated drain current for the entire input range are shown in Figure 2.14a and Figure 2.14b respectively. As shown in the figure, a narrow linear region of the drain current exists in the middle of the range where M_{in} is in saturation. The drain-current curve suggests that if the saturation region is extended and the non-linear sub-threshold (cut-off) and triode regions are avoided, one can get a linear current profile for the entire range. Such an approach is schematically shown in Figure 2.15 where the drain currents (of Figure 2.14b) are primarily linearized (saturation region is

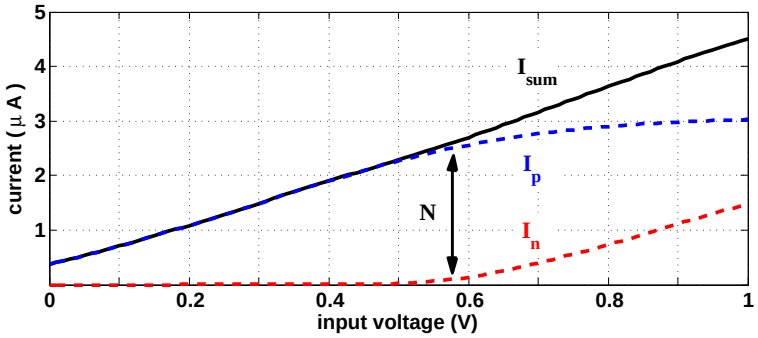


Figure 2.15: shifted drain currents of an NMOS device and summation of the shifted curves versus input voltage.

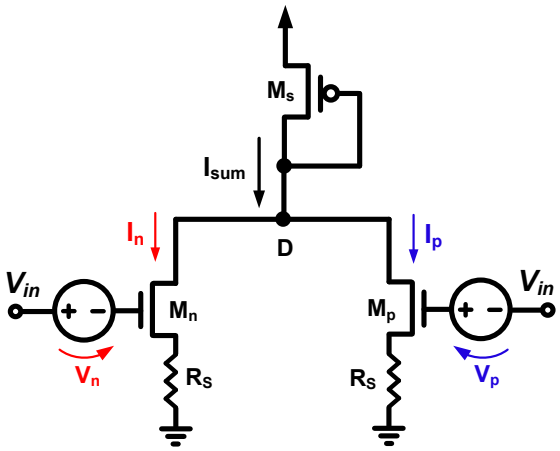


Figure 2.16: Schematic diagram of the circuit level implementation of the proposed constant-G_m voltage-to-current converter.

extended), shifted to the left and right by certain amounts and then added together. As shown in the figure, the summation current I_{sum} is a linear function of the input voltage V_{in}. Figure 2.16 schematically shows the circuit level implementation of the proposed scheme where the input is applied to the two input devices M_n and M_p. The source degeneration resistors R_s, extend the linear region of operation of M_n and M_p. The drain currents are subsequently shifted to the right and left through voltage level-shifters V_n and V_p which add a negative and positive shift to the input voltage V_{in} respectively. Finally, the shifted currents I_n and I_p are summed through the diode-connected PMOS, M_s.

Obviously, in order to obtain a linear current-voltage profile, the value of the shifts V_n and V_p have to be designed carefully. The positive level shifter V_p is responsible to eliminate M_p's sub-threshold (cut-off) region of operation by cancelling its threshold voltage. Ideally, in order to avoid the non-linear behaviour of M_p at the edge of inversion (point P in Figure 2.14b), V_p is designed slightly larger than the threshold voltage of M_p, i.e:

$$V_p = V_{th,p} + V_{off,p} \tag{2.8}$$

where, $V_{off,p}$ is the offset voltage intentionally added to do away with the non-linear portion of I_p at the edge of inversion. The negative level-shifter V_n is designed to push the triode region of M_n out of the input range. More specifically, V_n is responsible for turning M_n on when M_p is entering the triode region as the result of further increase in the input voltage. For a large R_s (to limit I_{sum}) and a large aspect ratio for M_s, V_D variation is negligible (i.e., $V_D \approx VDD - V_{th,s}$). Therefore, M_p enters triode when $V_{in} + V_p - V_{th,p} = VDD - V_{th,s}$ (point N in Figure 2.15). Substituting V_p from Equation 2.8 yields:

$$V_{in}|_N = VDD - V_{th,s} - V_{off,p} \tag{2.9}$$

V_n is accordingly designed to turn on M_n at point N. In other words, at the edge of M_p's triode region, $V_{in} - V_n = V_{th,n}$ which gives:

$$V_n = VDD - (V_{th,s} + V_{th,n} + V_{off,p} + V_{off,n}) \tag{2.10}$$

where, $V_{off,n}$ is the offset voltage added to cancel the non-linear behavior of M_p during transition from saturation to triode.

2.4.3 Implementation of Voltage Level shifters and Source Degeneration Resistors

The two level shifts, V_n and V_p (shown in Figure 2.16) can be implemented through the source-follower architecture as shown in Figure 2.17a [57]. The desired level-shifts V_n and V_p could ideally be obtained by connecting the gate of the current source transistor (M_{cn} and M_{cp}) to V_n and $VDD - V_p$ respectively. Since the loads

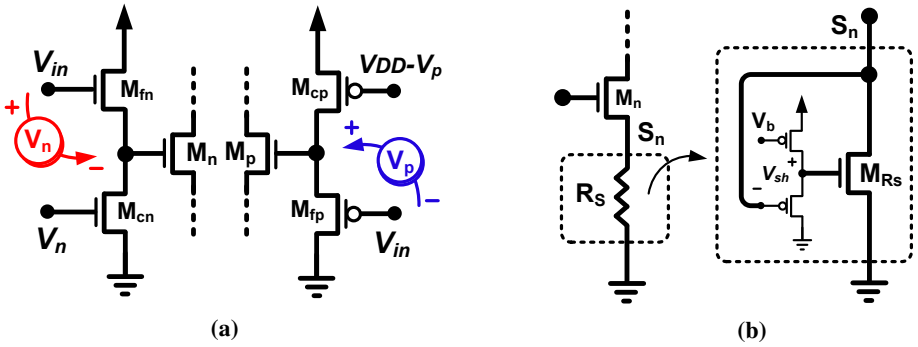


Figure 2.17: CMOS implementation of (a) voltage level shifters and (b) source degeneration resistors.

driven by the source followers (gate terminals of M_n and M_p) do not draw any current, the current source and follower transistors experience the same current and if sized identically will produce identical gate-source voltages, i.e., $V_{gs,fn} = V_{gs,cn} = V_n$ and $V_{sg,fp} = V_{sg,cp} = V_p$.

The large source-degeneration resistors (R_s) are implemented by a small aspect ratio NMOS devices (M_{Rs}) in triode as shown in Figure 2.17b. As shown in the figure, the drain of M_{Rs} is connected to its gate through a positive level-shifter to guarantee that it stays in triode regardless of its drain voltage (V_{Sn}) variations. In addition to the silicon area saved by implementing the large resistors through the triode NMOS, the proposed architecture provides a secondary control mechanism to further linearize the desired currents I_n and I_p. More specifically, for a sufficiently large positive level-shift V_{sh}, M_{Rs} is pushed into deep triode region and therefore its drain-source resistance is given by:

$$R_s \approx \frac{1}{k \cdot (V_{Sn} + V_{sh} - V_{th,Rs})} \tag{2.11}$$

where $k = \mu_n C_{ox}(W/L)_{Rs}$. In view of Equation 2.11, R_s is a weak function of V_{Sn} such that it has a larger value at the beginning of the input range and slightly drops when V_{in} and accordingly V_{Sn} increases. The non-linear dependance of R_s on the source voltage benefits a linear current profile. Specifically, in the vicinity of the transition point N (see Figure 2.15), R_{sp} keeps dropping while R_{sn} is at a higher value which leads to smoother transitions from saturation to triode for I_p and from cut-off to saturation for I_n.

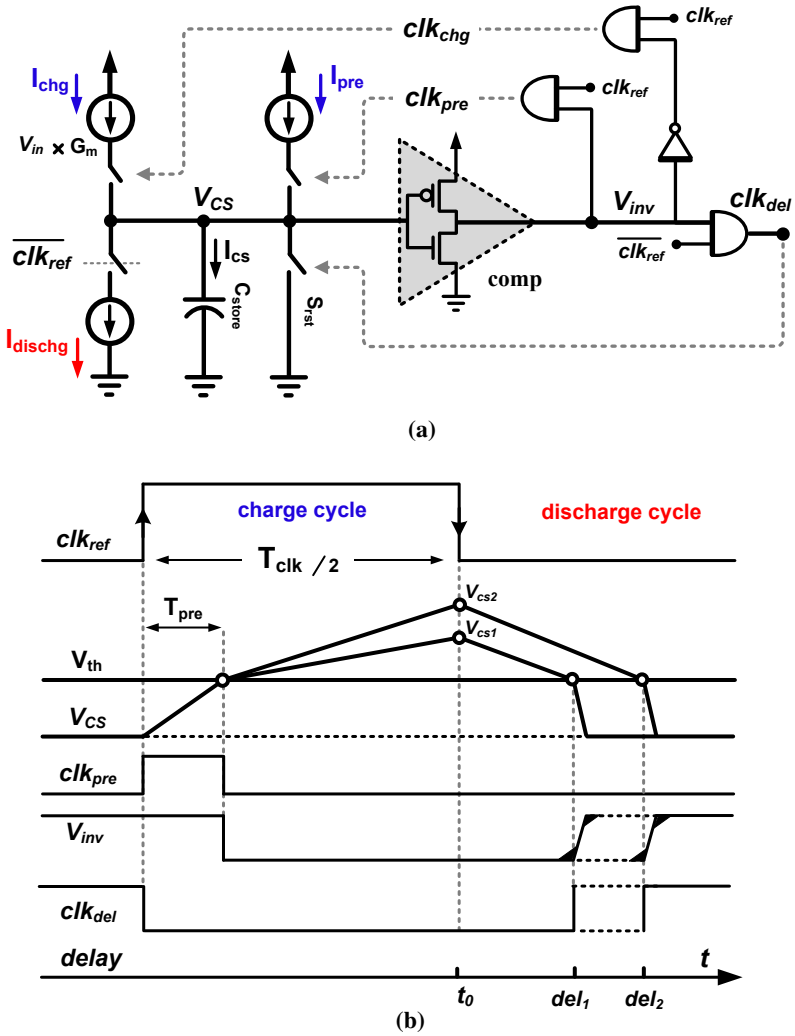


Figure 2.18: Comparator implementation. (a) Schematic diagram and (b) Timing diagram.

2.4.4 Implementation of the Inverter-Based Comparator

In derivation of Equation 2.7, it was assumed that the the comparator compares the capacitor voltage (V_{cs}) with $V_{ref} = 0$. In order to save layout area and power, the comparator could be implemented with a simple inverter (in a a fashion similar to the conventional CS VTC) such that the inverter compares the input voltage with its intrinsic threshold voltage V_{th}. This threshold voltage has to be cancelled prior to input proportional charge cycle. The inverter threshold cancellation scheme

is schematically shown in Figure 2.18a. As shown in the figure, at the start of the charge-cycle where the output of the inverter (V_{inv}) is high, the capacitor is charged with the constant current I_{pre}. Once the voltage on the capacitor equals V_{th}, the inverter toggles to low, deactivating clk_{pre} and activating clk_{chg}. Therefore, C_{store} is being charged at the input proportional rate ($G_m \times V_{in}$) for the rest of the charge cycle. A similar scenario holds for the discharge cycle where the inverter toggles to high once $V_{cs} = V_{th}$ producing clk_{del}. Such a scheme guarantees that the input proportional charging lasts for a constant period regardless of the input value. The timing diagram of the proposed threshold cancellation scheme is shown in Figure 2.18b. Following the same procedure as that of Equation 2.7, V_{th} is cancelled in the derivation of the desired delay which is given by:

$$\text{delay} = k \cdot V_{in} \quad \left(k = \frac{G_m \cdot (T_{clk}/2 - T_{pre})}{I_{dischg}} \right) \tag{2.12}$$

where the constant value T_{pre}, is the time required for the storage capacitor to charge at a constant rate (I_{pre}) from zero to the threshold voltage of the inverter. The three AND gates are designed to produce the appropriate signals to turn the switches on/off at designated times. Note that during the discharge cycle, once the desired delay is obtained (i.e., V_{inv} toggles to high), V_{cs} could be kept intact such that the capacitor starts to charge form a value close to V_{th} at the beginning of the following charge cycle. However, the precharge/reset scheme (i.e., pre-charging the capacitor at the beginning of the charge cycle and resetting it at the end of the discharge cycle) is essential to avoid unnecessary power consumption as keeping the input voltage of the inverter (V_{cs}) at a value close to its threshold voltage provokes a large static current drawn by the inverter.

2.4.5 Design Considerations

The complete circuit-level schematic of the proposed VTC is shown in Figure 2.19. As shown in the figure, the produced linear current is transferred to the charge/discharge unit through a self-cascode current mirror [58]. Note that during the current copying interval (charge cycle), the drain voltage of the mirror PMOS transistor $M_{m1,2}$ (i.e., V_{cs}) varies significantly and therefore, the high

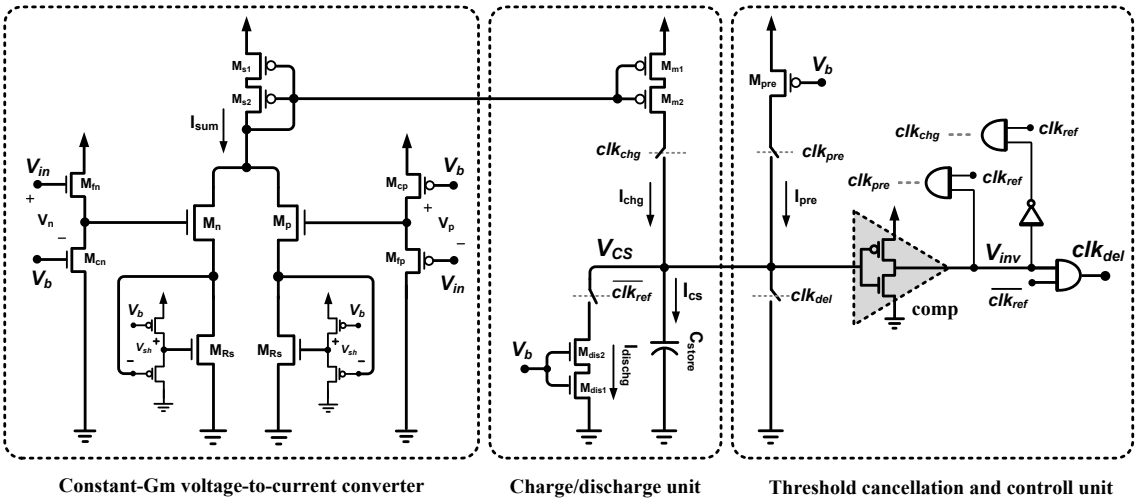


Figure 2.19: Circuit level schematic of the proposed VTC.

output impedance offered by the self-cascode architecture proves beneficial in providing a high-precision copy of the produced linear current to the capacitor. The discharge current is also supplied by the self-cascode NMOS transistor ($M_{dis1,2}$) to guarantee a rather constant current despite V_{cs} variations during discharge cycle. The pre-charge transistor M_{pre} is designed with a large aspect ratio to provide a large current in order to minimize the pre-charge time.

In regards to the proposed VTC architecture, there are some important points and trade-offs to be carefully considered in the design process which are listed as follows:

1. Regarding the charge current transfer scheme, one can directly drive the storage capacitor by a PMOS input voltage-to-current converter and thus avoid the current mirror and the associated complications altogether. However, such an alternative is impractical for two reasons.

First of all, the drain voltage (V_{cs}) variation of input devices will severely affect the linearity of the produced summation current. Secondly, switching off the summation current (I_{chg}) during the discharge cycle pushes the two input devices into deep triode. The input devices require a certain amount of time for the transition from triode to saturation at the start of the next charging cycle. The otherwise unnecessary transition time affects the speed performance of the

voltage-to-current converter and limits the maximum sampling frequency. Moreover, the prolonged setup time leads to a nonlinear and inaccurate transient current at the start of each charging cycle. Although a constantly on input branch (in the proposed design) comes at the cost of extra current consumption, the power overhead is well justified. More specifically, the proposed scheme enables incorporating a current mirror with a high output impedance at the drain of $M_{m1,2}$ to mitigate the effect of V_{cs} variations on I_{ch} accuracy. Furthermore, the aforementioned transition could be much shorter for the mirror current compared to the scenario where the entire input current is switched.

It is worth mentioning that as a viable approach to conserve power, the input branch can be turned off through voltage switching (i.e., grounding the gates of the input devices during the discharge cycle). However, such a scheme is ruled out as an attractive alternative in the proposed design since voltage switching is generally slower than current switching. Moreover, voltage switching produces current spikes at clocks transitions which is undesired in the context of VTC.

2. As described in Section 2.4.2, a linear input dependent current I_{sum}, requires perfectly matched input devices M_n and M_p (see Figure 2.16). the accurate matching is essential to provide identical current slops while each input device operates in saturation (M_p from zero to N and M_n from N to VDD in Figure 2.15). Also for ideal level shifters, matched input devices guarantee that the transition occurs at the desired input level (point N). To achieve a good matching and in order to minimize process and temperature variations, the two input devices are interdigitated and laid out inside a ring of dummy transistors.

3. It was mentioned in Section 2.4.3 that the positive and negative level shifts can be obtained by applying $VDD - V_p$ and V_n to the gates of current source transistors M_{cp} and M_{cn} respectively. However, to avoid the complexity imposed by the two bias generation circuitries, the two current source transistors are designed to generate the desired level shifts while being driven by a single bias voltage V_b. The same bias voltage V_b is also used to drive the source-degeneration resistors, pre-charge and discharge current sources as shown in Figure 2.19.

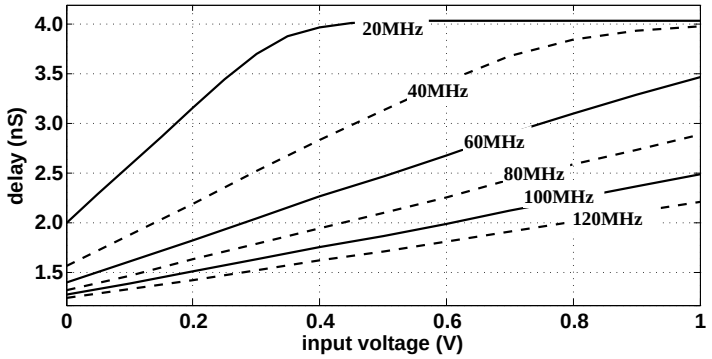


Figure 2.20: Simulated delay for the entire input range for different clock frequencies.

4. Another important issue regarding the operation of the proposed VTC is its dependance on the clock frequency. More specifically, as suggested by Equation 2.12, the conversion gain ($k^{\text{sec/V}}$), is directly proportional to the clock period T_{clk}. This has to be taken into account only if the VTC is to be used in applications with variable clock/sampling frequency. Otherwise, the variable conversion gain could be simply calibrated in digital domain such that the minimum and maximum delays (corresponding to $V_{in} = 0$ and $V_{in} = VDD$ respectively) are extracted prior to the start of operation in order to normalize the resulted slope. Alternatively, the slope variations would be automatically cancelled if all the internal clock frequencies are scaled with respect to the sampling clock (T_{clk}). For instance, if a counter is being used to digitize the delay, the clock frequency of the counter has to be sclaed in accordance with that of the sampling clock (T_{clk}). The conversion gain could also be calibrated in analog domain through adjusting the pre-charge time (T_{pre}) and/or the discharge current (I_{dischg}). As suggested by Equation 2.12, a constant k is obtained provided that $(T_{clk}/2 - T_{pre})/I_{dischg}$ remains constant regardless of T_{clk} variations.

The simulated delay-V_{in} plots for different clock frequencies are shown in Figure 2.20. As shown in the figure, the conversion gain (ns / V) is proportional to the the clock period. In addition to the slope of the delay plots, T_{clk} manifests its effect on the produced delay through a separate mechanism. As shown in Figure 2.20, the delay plots saturate for large input voltages at small clock frequencies (large T_{clk}). For large clock periods and accordingly long charge

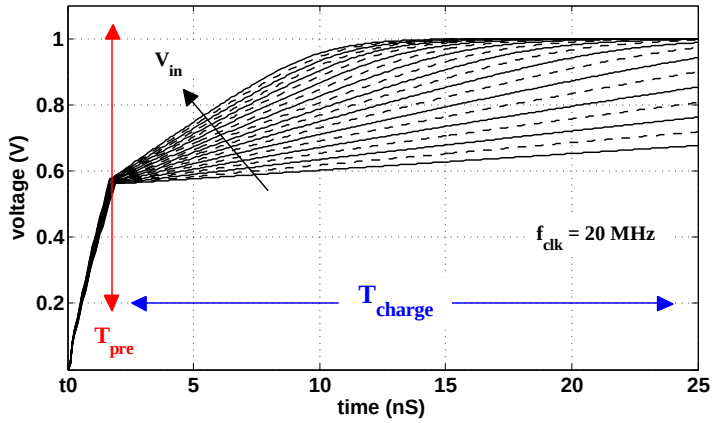


Figure 2.21: Simulated transient voltage of storage capacitor during the charge cycle.

cycles, the storage capacitor will charge up to high values. A high V_{cs} (see Figure 2.19) pushes the mirror transistor $M_{m1,2}$ into triode resulting in I_{chg} degradation which is shown as the curved parts of delay plots for f_{clk} = 40 MHz and f_{clk} = 20 MHz. The simulated transient voltage of the storage capacitor, for the entire input range (at 100mV increment) and for a clock frequency of 20 MHz is shown in Figure 2.21. As shown in the figure, V_{cs} starts to saturate for input voltages larger than 0.3 V. Also for $V_{in} > 0.4$V, V_{cs} is fully charged to VDD at the end of the charge cycle which corresponds to a constant delay ($V_{in} > 0.4$) in Figure 2.20.

To address the nonlinearity ensued as the result of V_{cs} saturation for smaller than nominal sampling frequencies (f_{clk}), a simple approach is to increase the storage capacitance. Note that one can alternatively reduce the charge current or the threshold voltage of the inverter, however, such approaches come at a higher price in terms of complexity. Schematic diagram of C_{store} modification scheme along with the simulated delay are shown in Figure 2.22. As shown, a controller will switch $s_{clk/2}$ on to place an identically sized storage capacitor in parallel with C_{store} if the sampling frequency is to be half of the nominal frequency. The same scenario hold for $s_{clk/4}$ if the sampling frequency is reduced down to a quarter of the designated frequency.

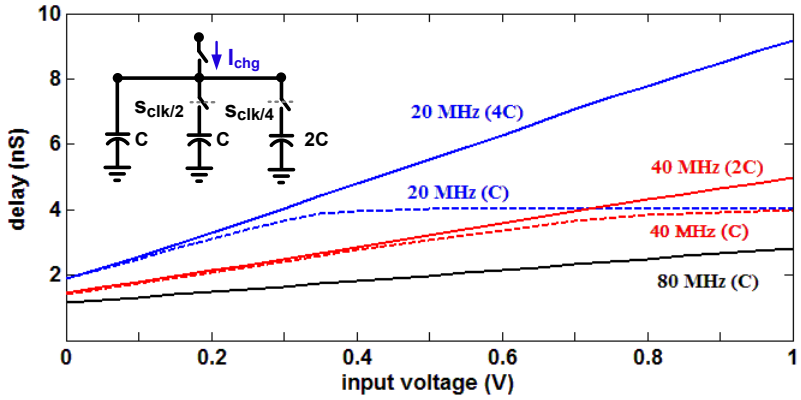


Figure 2.22: Storage capacitor modification scheme along with the simulated delay.

5. As shown in Figure 2.20, the delay plots have a non-zero value for $V_{in}= 0$ (i.e., $\text{delay}|_{V_{in}=0} \neq 0$). This offset is normally not a matter of concern in most applications. Moreover, if a zero delay for $V_{in}= 0$ is desired, the offset can be simply cancelled in digital domain during calibration by subtracting $\text{delay}|_{V_{in}=0}$ from the obtained result. The offset could also be cancelled in analog domain at a higher cost in terms of complexity. To cancel the aforementioned offset, an input current corresponding to $V_{in}= 0$ has to be generated through a replica of the positively level shifted input device (M_p and the associated shifter in Figure 2.19). The replica current has to be subtracted from the summation current I_{sum} at the constant-G_m unit or from the charge current (I_{chg}) at the charge/discharge unit (see Figure 2.19) as shown in Figure 2.23 . Note that subtracting the replica current I_{AZ} form I_{sum} as shown in Figure 2.23a, biases M_s close to the edge of inversion giving rise to nonlinearity for small V_{in} values. Therefore, subtracting I_{AZ} from the mirror current (I_{chg}) as shown in Figure 2.23b is a more attractive alternative provided that I_{AZ} variations as the result of V_{cs} variations do not introduce significant nonlinearity. In order to produce the correct replica current, M_{AZ} has to be sized according to the current mirror ratio.

6. A useful feature of integrating converters is their intrinsic sampling property. If the input voltage to the converter is slow compared to the sampling clock frequency (f_{clk}), the storage capacitor can also perform as a sample-and-hold. In the context of the proposed VTC, if the input voltage variations during the charging cycle are negligible, a sample-and-hold front-end could be avoided

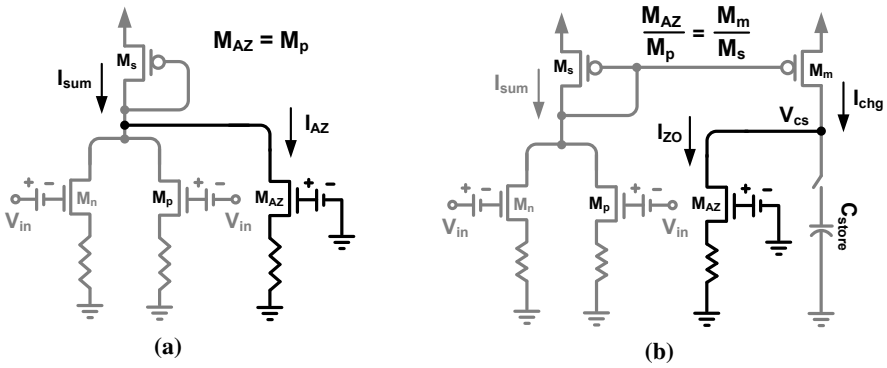


Figure 2.23: Delay offset cancellation by subtracting the replica current from: (a) summation current, (b) charge current.

without compromising the performance. Figure 2.24 shows the simulated spectrum of the output delay for for sinusoidal inputs at different frequencies. The frequencies of input sine waves are non-integer divisors of the sampling frequency (f_{clk}=80 MHz) starting from 1.1 MHz with 1 MHz increments. As shown in the figure, with no sample-and-hold block incorporated, while the fundamental component remains rather unaffected, the harmonics and distortion levels of the output spectrum significantly increase for higher frequencies. Figure 2.25 shows the spectrum of the output delay for a 15.1 MHz input sinusoidal when the input is being sampled (during the discharge cycle) and held (during the charge cycle). As shown, incorporating a sample-and-hold block for higher input frequencies (with respect to the sampling frequency of 80 MHz) improves the dynamic performance of the converter. Specifically as shown in the figure, the second harmonic for a 15.1 MHz sinusoidal input is improved by 10 dB (34 dB to 24 dB) when the input is appropriately sampled and held.

7. As a parting note, it should be mentioned that one can skip the voltage-to-current conversion step by directly sampling the voltage on the storage capacitor (during the charge cycle) to satisfy the requirements of Equation 2.7. Subsequently, the input voltage sampled on the storage capacitor could be discharged through a constant current source until a pre-defined threshold voltage is met. However, in order to support a rail-to-rail input range (0∼VDD), such a scheme requires a sophisticated discharge current source to maintain an accurately constant current over the entire range and/or a negative supply voltage.

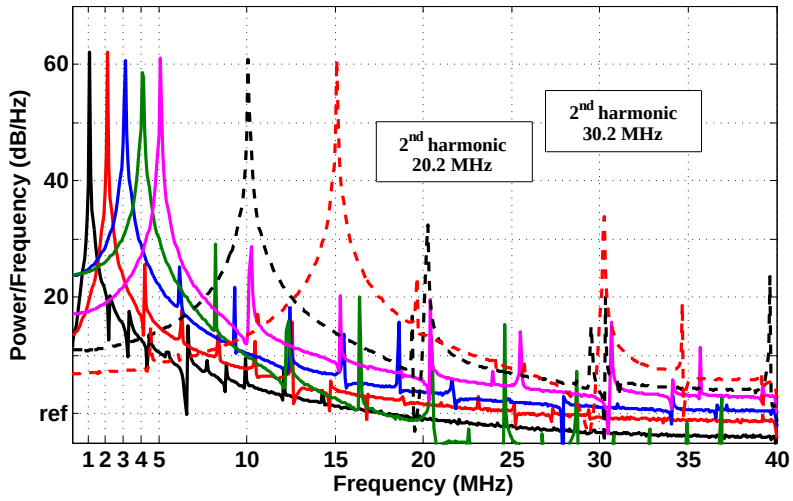


Figure 2.24: Spectrum of the output delay for different input frequencies without sample-and-hold.

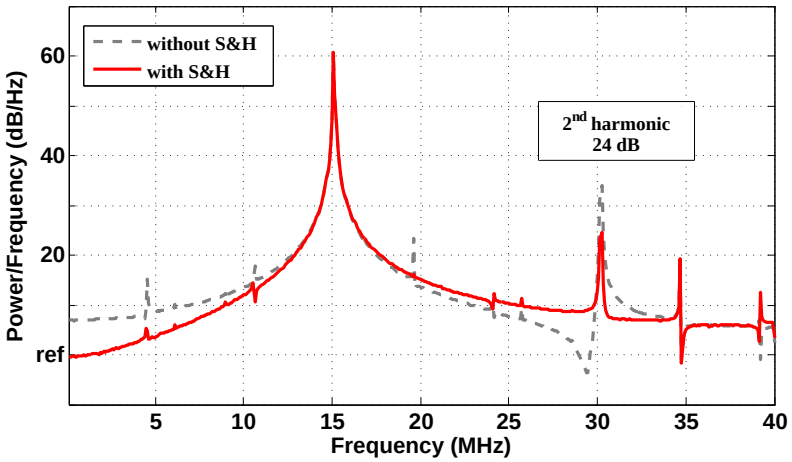


Figure 2.25: Spectrum of the output delay for a 15.1 MHz sinusoidal input with and without sample-and-hold.

2.4.6 Measurement Results

A proof-of-concept prototype of the proposed VTC is designed and fabricated in a 0.13 μm CMOS process. The prototype is packaged in a standard ceramic quad flat package (CQFP). The entire VTC only occupies 60 μm$\times$60 μm (3600 μm^2) of silicon area as shown in Figure 2.26. Analog and digital blocks are separately driven by a supply voltage of 1V (VDD_A = VDD_{DIG} = 1V) and a single bias voltage of 0.5V is used to drive the level shifters, degeneration resistors and the discharge

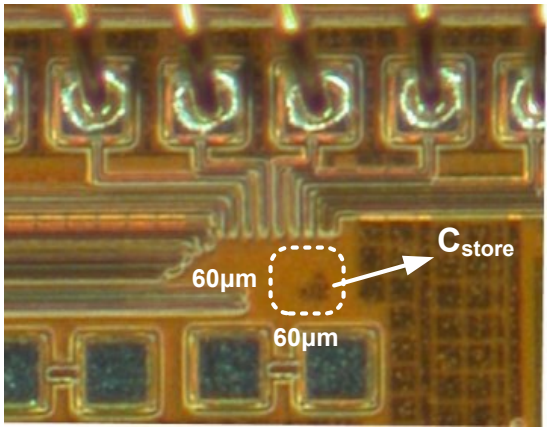


Figure 2.26: Micrograph of the fabricated VTC.

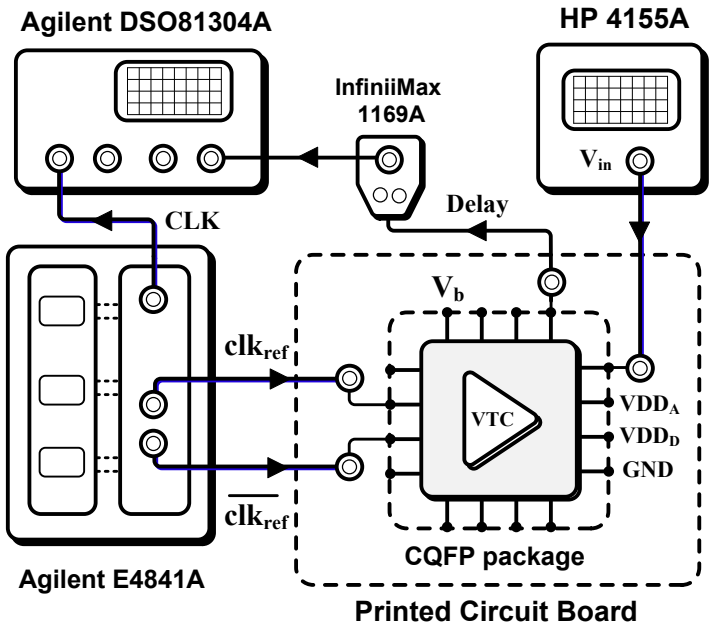


Figure 2.27: Schematic diagram of the measurement setup.

current source (V_b = 0.5V).

The measurement setup used for measuring the performance of the proposed VTC is schematically shown in Figure 2.27. An HP-4155A semiconductor parameter analyzer is used to provide the input ramp (V_{in}), bias voltage V_b and also the supply voltages (to enable current consumption measurement). The clock signals clk_{ref} and $\overline{clk_{ref}}$ are supplied by Agilent-E4841A data Gen./Analyzer. The

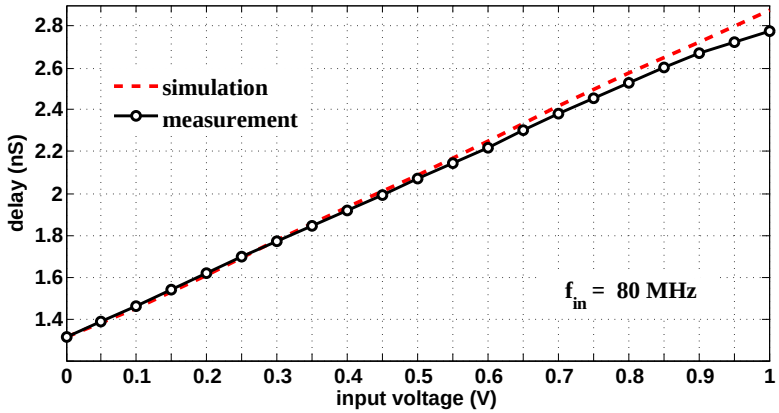


Figure 2.28: Measured and simulated delays for the entire input range.

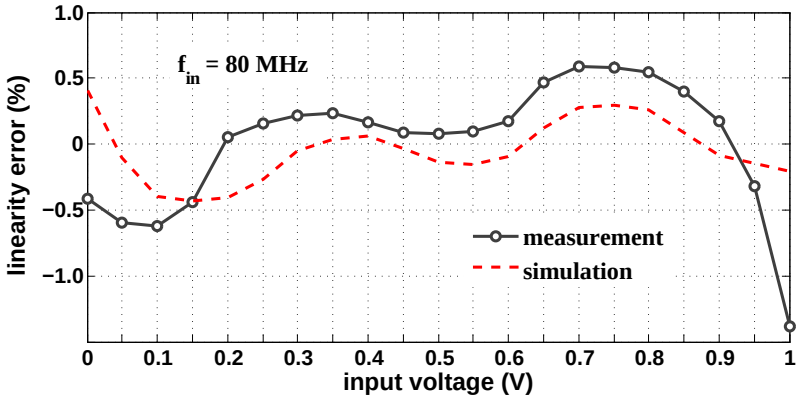


Figure 2.29: Measured and simulated linearity error for the entire input range.

same module is used to provide a copy of $\overline{\text{clk}_{\text{ref}}}$ (shown as CLK in Figure 2.27) for delay measurement. An Agilent 12-GHz InfiiMax-1169A active probe is used to capture the output delay signal and an Agilent 13-GHz Infiniium-DSO81304A oscilloscope is used for delay measurement.

The simulated and measured delay versus input voltage (at 50 mV increments) is shown in Figure 2.28 for an slow ramp as the input voltage and an 80 MHz reference clock. The systematic delay attributed to the length difference between the sub-miniature version A (SMA) cables (those connecting clk_{ref}, $\overline{\text{clk}_{\text{ref}}}$ and CLK in Figure 2.27) and the active probe is measured for $V_{in} = 0$ and de-embedded with respect to the simulated delay profile. Note that it is the linearity of the measured delay profile (i.e., constant slope of the curve) which is of significance

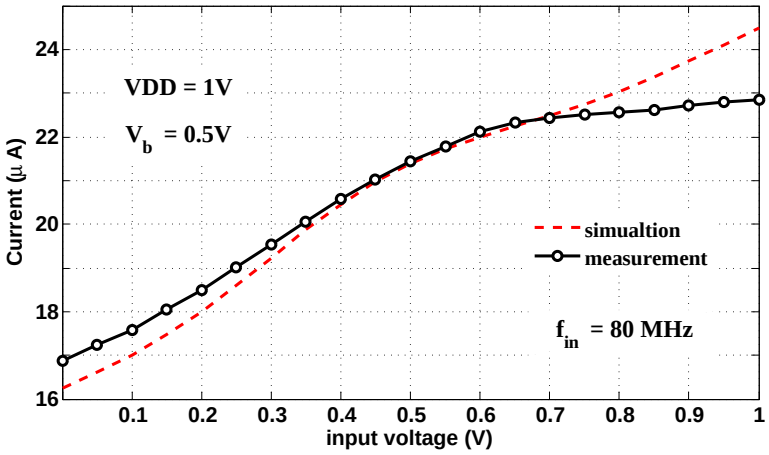


Figure 2.30: Measured and simulated analog current consumption of the VTC for the entire input range.

as a performance metric. As mentioned in Section 2.4.5, the offset (i.e., $\text{delay}|_{V_{in}=0}$) can cancelled in digital domain during calibration. As shown in the figure, the measured delay exhibits a good linearity performance and fits the simulated delay profile for a wide range of input voltages. The measured delay line slightly deviates from the simulated one as the input voltage grows. Such a behaviour observed in measurements can be attributed to the inaccuracy of the current mirror ($M_{m1,2}$ in Figure 2.19) in copying the summation current (I_{sum}) when the voltage of the storage capacitor (V_{CS}) grows too high. With reference to Figure 2.19, a large V_{CS} prevents accurate current mirroring by decreasing the voltage headroom of the mirror transistors ($M_{m1,2}$) and disrupting the balance between the source I_{sum} and the mirror (I_{chg}) branches.

Figure 2.29 shows the simulated and the measured linearity error for the entire input range and a similar setup as that of Figure 2.28. As shown in the figure, the simulated result exhibits a linearity error smaller than $\pm$ 0.5 % for the entire input range which corresponds to $\sim$ 7.64 ENOB. The measured error is within $\pm$ 0.6 % for $V_{in} < 0.95$ V corresponding to $\sim$ 7.38 ENOB. The linearity error percentage grows to $-$ 1.4 % for the full range ($V_{in} =$ 1 V) which degrades the ENOB to $\sim$ 6.16. As discussed above, the linearity degradation at higher end of the input range can be avoided by use of a more accurate current mirror. An example of such a modification to improve the current mirror performance is provided in Section 6.2. Note that the ENOB values reported are those of the VTC only and

in a complete time-mode ADC, other parameters also affect the overall linearity performance of the system.

For a 1 V supply voltage at 80 Mhz clock frequency, Figure 2.30 shows the measured and simulated average current (power) drawn by the analog portion of the VTC (constant G_m voltage-to-current converter, charge and discharge unit and the inverter-based comparator in Figure 2.19). Note that for large input values (i.e., $V_{in} > 0.6$ V), the rate of current consumption drops with V_{in}. As discussed above, such a behavior is expected since the small voltage headroom of $M_{m1,2}$ (see Figure 2.19) results a smaller mirrored current for a longer portion of the charge interval. The average current consumption of the digital portion of the VTC (digital gates of the control unit) for a supply of 1 V is measured to ~ 1.8 μA.

Table 2.2 provides a performance summary of the proposed VTC and compares the results with similar works.

Table 2.2: Comparison of the proposed VTC with similar works.

Reference	[50]*	[52]**	[59]**	This work **
Technology	0.13 μm	90 nm	90 nm	0.13 μm
Conversion gain	2.5 ns/V	250 ps/V	$\sim$ 400 ps/V	$\sim$ 1.25 nS/V
Linear range	200 mV	100 mV	150 mV	1 V ^{a}
Linearity error	2 %	N/A	$<$ 0.05LSB ^{b}	$<$ 1.4%
Power consumption	N/A	2.7 mW ^{c}	5.7 mW ^{c}	16.8 μW $\sim$ 22.8 μW ^{d}

$\star$ Simulation results. $\star\star$ Maesurement results. *a* Entire input range. *b* LSB = 6.25 ps. *c* At 5 GHz sampling frequency. *d* At 80 MHz sampling frequency for 0 $\sim$ 1 V input. The digital power consumption is 1.8 μW.

2.5 Conclusion

In this chapter, first, an ultra-low-power SAR ADC is presented. The proposed DAC architecture allows operation of the SAR ADC with only four minimum sized capacitors which in turn, facilitates an small area and low power consumption. In order to further save power and layout area, the two buffers incorporated in the DAC architecture are dually used as the pre-amplifier stage for the comparators. The proposed SAR ADC is designed in a 0.13 μm CMOS technology and its performance is verified by post-layout simulation results.

Furthermore, an important building block of a time-mode ADC, namely, a highly linear wide input range VTC is discussed. Circuit-level design techniques are used to provide a linear performance for the output delay for a wide range of input voltages. The proposed VTC is fabricated in 0.13 μm CMOS technology and its performance is validated through measurement results.

Although SAR ADCs are widely used in RFID tags to perform the analog-to-digital conversion, they are still dependent on capacitive DAC and analog comparators which are typically area consuming and power hungry blocks. Time-mode ADCs on the other hand, are more compatible with all-digital CMOS implementation which is specifically beneficial in the context of passive RFID tags.

Chapter 3

Efficient Power Converter Circuits for RFID Applications

Wireless energy harvesting (also known as RF energy harvesting) is an merging technology that enables long and maintenance-free operation of low-power electronic devices.[1] The applications for such wirelessly-powered devices span a wide range including wireless chargers, biomedical implants, wireless sensor nodes, RFID tags (semi-passive and passive), etc. Transmission of RF energy has a long history dating back to the experiments of Heinrich Hertz in 1880 [60]. This technology has come back into interest recently in response to the requirements of RFID tags and wireless sensor nodes. RF energy delivery provides numerous advantages over the conventional wired methods the most important of which could be summarized as [61]:

- Eliminating the wiring and battery replacement costs and facilitating a cost-efficient implementation of the device.
- Eliminating service failures due to depleted battery and facilitating a maintenance-free and reliable operation.

RF-to-DC converter (rectifier) is a key building block of an RF energy harvesting system. As discussed in Chapter 1, the main task of the rectifier is to

[1] http://ca.mouser.com/applications/energy_harvesting_wireless/

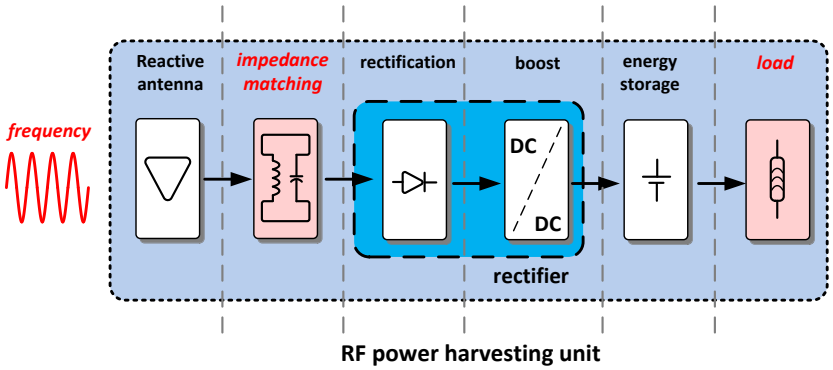


Figure 3.1: Schematic diagram of a generic RF power harvesting unit.

receive the RF energy and to convert it to a stable DC power to supply the wirelessly-powered device. A crucial characteristic of the rectifier is its conversion efficiency which directly determines the available power for the device from the limited transmitted energy. More specifically, the performance of the rectifier interactively decides the harvesting range, frequency range, sensitivity of the device and implementation scalability [62]. Extensive studies have been carried out to improve the efficiency of the rectifiers which will be discussed in the next section.

3.1 Efficiency Analysis of UHF CMOS Rectifiers

Three major parameters directly influence the PCE of a rectifier, namely load requirements, frequency of operation and circuit topology (including antenna, matching network and the rectifier circuitry). Figure 3.1 schematically shows the internal operation of a generic power harvesting unit highlighting the three parameters that affect the PCE of the rectifier. With the first two parameters dictated by the application, the main research to enhance power conversion efficiency is targeted at proposing novel architectures and design techniques at a circuit level.

In a circuit level analysis, PCE is mainly degraded as a result of two major mechanisms, namely forward voltage drop and reverse leakage current in switching devices (diodes or transistors). Note that the matching network efficiency will be covered later in this chapter and the adverse effect of parasitics is of a second order importance and could be minimized through optimal sizing. It is also worth mentioning that Schottky diodes provide a low potential barrier

which is very attractive to implement the switching device for UHF rectifiers [63]. However, any desirable efficiency enhancement technique should avoid incorporation of Schottky diodes, floating gate transistors, low-threshold transistors, etc., as they are not supported in a low cost standard CMOS technology.

Conventional Dickson-based rectifier is a well-known architecture and extensive studies on efficiency enhancement techniques associated with this architecture exists in the literature. Raben *et al.* [64] introduce an active diode-connected metal-oxide-semiconductor (MOS) transistor as the switching device. An adaptive threshold cancellation scheme is proposed by Yo *et al.* [65]. Umeda *et al.* [66] use floating voltage sources to cancel the threshold voltage of switches. Although static cancellation of the threshold voltage improves the forward voltage drop specification of the switches, such a scheme produces a higher leakage current and degrades efficiency performance. Shokrani *et al.* [67] use the bulk connection of MOS switches to reduce their threshold voltage and leakage current.

Lee and Ghovanloo [68] and Guo and Lee [69] propose use of high-speed comparators to detect and control the reverse leakage currents in switches. Considering the power consumption and the complexity overhead, employing high speed comparator limits the usefulness of such techniques to low frequency applications. Comprehensive studies on optimization procedure and design issues associated with conventional (Dickson-based) rectifiers are provided in [70–76].

Dickson-based rectifiers generally fail to perform desirably in terms of efficiency in view of their characteristic inefficient architecture (specifically when Schottky diodes and other high-cost technologies are not available). As a more efficient alternative, differential-drive (4T-cell) architecture has been introduced to simultaneously tackle the impacts of forward voltage drop and reverse leakage current [77]. Differential-drive rectifiers provide a superior efficiency (compared to Dickson-based rectifiers) at no significant cost in terms of complexity. Differential rectifier receives the input RF signals in a differential format and the cross-coupled bridge configuration allows low ON-resistance and small leakage current simultaneously.

The differential-drive rectifier introduced by Kotani *et al.* [78] achieves a high

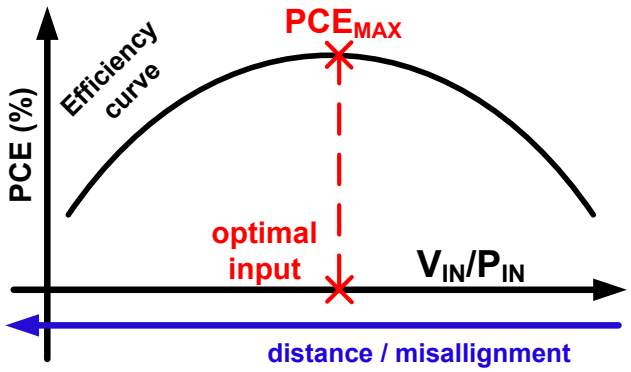
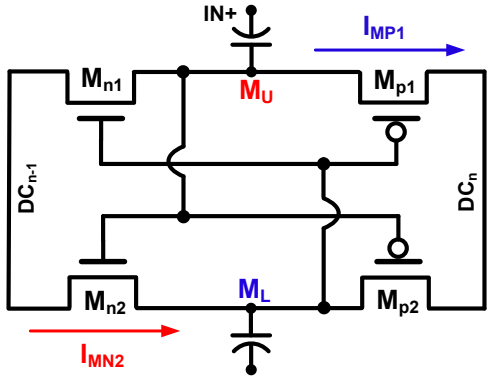


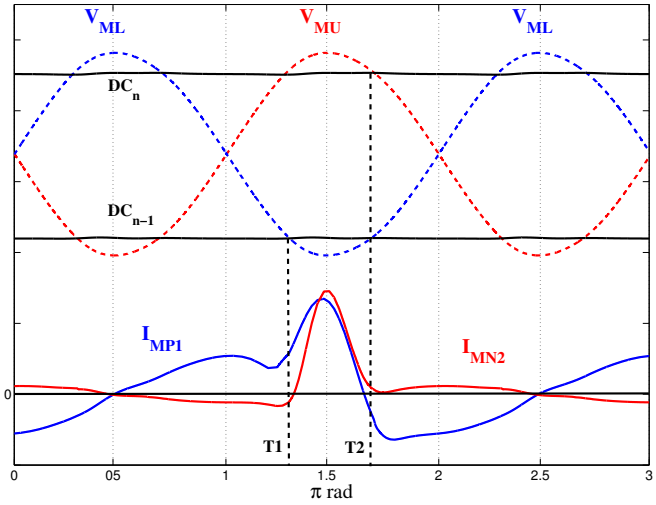
Figure 3.2: Schematic diagram of the PCE curve of a generic rectifier.

PCE of 62% for −6 dBm input power at 953 MHz input frequency. Mandal and Sarpeshkar [79] investigate the potentials of using floating gate switching transistors in a double-poly technology to enhance the efficiency of differential-drive rectifiers through reducing the threshold voltage of switches. Bakhtiar *et al.* [80] propose a biasing scheme to drive the gate of switches and set the effective threshold voltage of transistors to a smaller value, therefore reducing the turn-on voltage of the rectifier (i.e., achieving the maximum efficiency for smaller input voltage). Wong and Chen [81] provide an analytical design approach to enhance the efficiency of multi-stage differential-drive rectifiers. Huang *et al.* [82] use a high voltage-gain charge pump after the differential rectifier to enhance the conversion efficiency. Mazzilli *et al.* [83] provides a design methodology for an efficiency matching and compared various differential rectifier topologies.

Generally, a rectifier is designed and optimized to meet the requirements set by the application. Specifically, optimization is performed mainly on the basis of the load, frequency of operation and communication distance. Optimization parameters include topology, transistor and capacitor sizing, number of stages, etc. For a fixed set of load requirement and frequency of operation, the PCE of a rectifier peaks at an optimal input voltage/power level and drops drastically if the input deviates from the optimal point as schematically shown Figure 3.2. This follows that if the input RF level received by the tag antenna drifts away from the optimal input voltage/power, the abrupt drop in PCE disables the rectifier to sufficiently supply the succeeding tags circuitry. Note that deviation from the optimal input level occurs as the result of variations in the distance between the



(a)



(b)

Figure 3.3: Conventional differential rectifier. (a) Architecture and (b) voltage-current waveforms at UHF.

reader and the tag (in electromagnetically coupled systems) or misalignments between the primary and secondary coils (in inductively coupled systems). As mentioned earlier, forward voltage drop and reverse leakage current are mainly responsible for PCE degradation. Therefore any attempt towards improving PCE has to diminish the adverse effects of the two mechanisms. To this end, a conventional differential rectifier along with the current-voltage waveforms for the two reciprocal PMOS and NMOS transistors (M_{P1} and M_{N2}) are depicted in Figure 3.3 for a 950 MHz input frequency.

Note that, the waveforms are shown for the second stage of three-stage

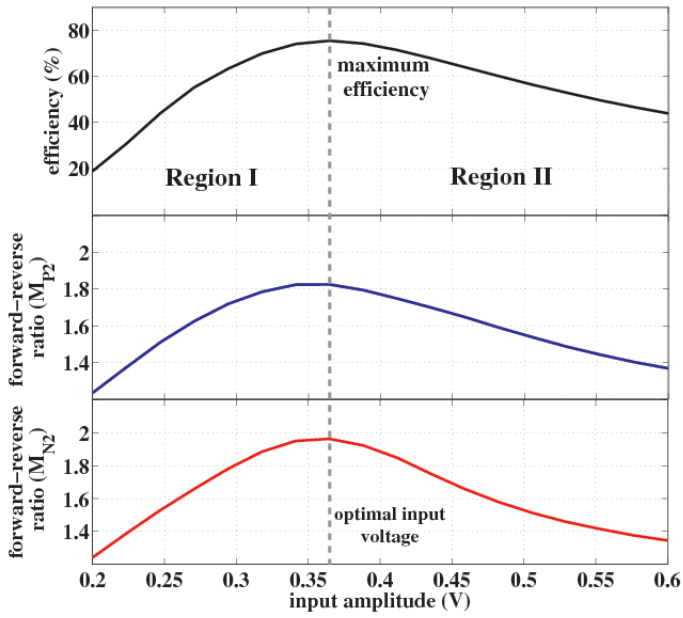


Figure 3.4: PCE curve and forward-to-reverse current ratios of MP2 versus input voltage.

rectifier and the Y-axis is graded arbitrarily. As shown in the figure, due to the RC nature of the circuit, the currents lead the voltages. More specifically, the forward current of I_{MP1} reverses its direction prior to V_{MU} and DC_n intersection at T_2. Note that M_{p1} switches its source and drain at T_2. Prior to T_2, M_U and DC_n serve as the source and drain respectively, while DC_n and M_U switch their tasks after T_2 and function as source and drain respectively. At lower frequencies, current direction reversal occurs subsequent to the intersection point where I_{MP1} starts in triode mode followed by saturation until the gate-source voltage ($V_{ML\text{-}DCn}$) falls below the threshold voltage of I_{MP1} and sub-threshold current keeps flowing until the next current reversal (reverse-to-forward at 2.5 πrad as shown in Figure 3.3b). However, at UHF, currents and voltages are not perfectly in-phase, which substantially complicates the analysis and optimization based on current-voltage waveforms as proposed in [70] and [81]. The same scenario holds for M_{N2}.

As a more practical and straightforward approach, PCE could be studied as a function of forward-to-reverse currents ratio for the entire input range. The PCE of a three-stage rectifier at 950MHz input frequency along with the forward-to-reverse current ratios for the two reciprocal switching transistors (M_{P1} and M_{N2}) are shown Figure 3.4 versus the input voltage. As shown in the figure,

the maximum efficiency point (corresponding to optimal input voltage) is almost perfectly aligned with the maximum forward-to-reverse current ratios for the switching transistors which suggests that maximum PCE is obtained provided that the switches are operating at the maximum forward-to-reverse current ratio mode. Also as shown in Figure 3.4 the input range is divided into two regions, labeled as region-I and region-II. In region-I, the gate of switching transistors are under-driven, i.e., with respect to their threshold voltages, the gate-source voltage of the switches (e.g. V_{ML}-V_{MU} in Figure 3.3a) are insufficient to fully turn the transistors on in order to provide a large forward current to charge the associated node. On the other hand, in region-II, the gate of switching transistors are over-driven, i.e., the gate-source voltage of switches are excessively large which in turn increases the reverse current, giving rise to a smaller forward-to-reverse current ratio and consequently a smaller PCE. Note that with reference to Figure 3.3b, $I_{forward}$ is the average of $I_{Mp1,N2}$ for the intervals of time when $I_{Mp1,N2} > 0$ and $I_{reverse}$ is the average of $I_{Mp1,N2}$ for the intervals of time when $I_{Mp1,N2} < 0$. It can be concluded from Figure 3.4 and the discussion made above that in order to address the PCE drop on the two sides of the maximum PCE point (optimal input voltage), the gate-drive voltage of switches need to be boosted in region-I (where switches are under-driven) while they need to be attenuated in region-II (where switches are over-driven).

This could be further clarified in view of Figure 3.5 where the PCE curve is shown on the top, along with the average source-gate voltage of transistor M_{P1} during the forward conduction interval, and the gate-source voltage of MP1 during the reverse conduction. Forward conduction interval ($T_1 \sim T_2$ in Figure 3.3b) is defined as the time slot in which the intermediate node experiences a higher voltage than the output node (i.e., $V_{MU} > DC_n$ in Figure 3.3a). In other words, the intermediate node, M_U, serves as the source and the output node, DC_n, serves as the drain for M_{P1} such that charge is transferred from the input to the output. Accordingly, the reverse interval is defined as the time window when M_U serves as the drain and DC_n serves as the source ($V_{MU} < DC_n$) and charge is leaked from the output to the input node. As highlighted in the figure, at each stage of the rectifier, there is a certain gate-drive voltage occurring at the optimal input voltage that maximizes the efficiency.

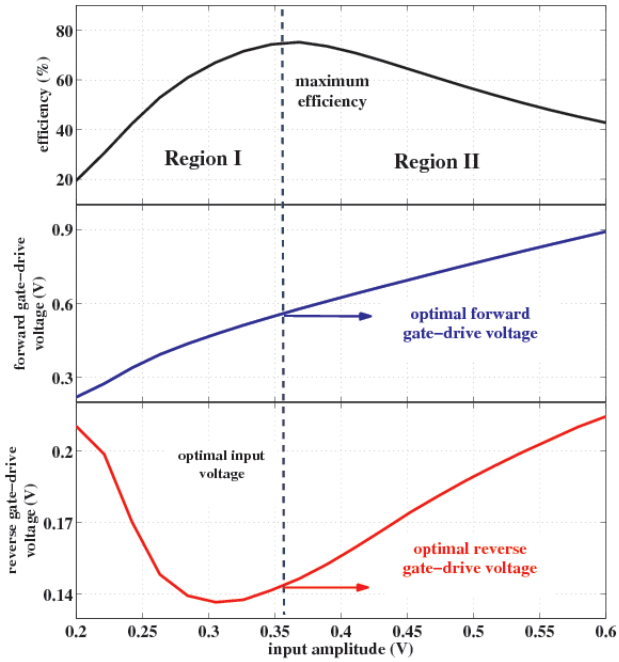
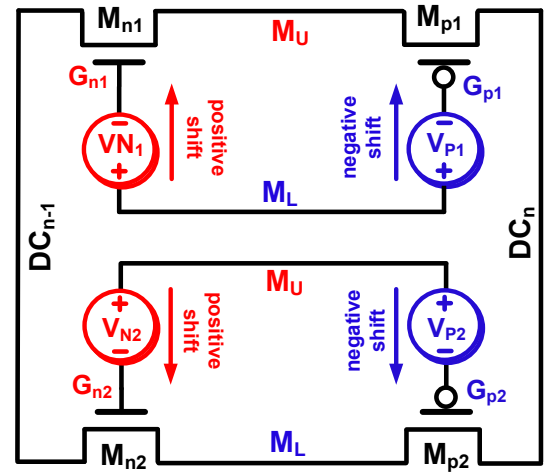


Figure 3.5: PCE curve and average gate-drive voltage during forward and reverse conduction.

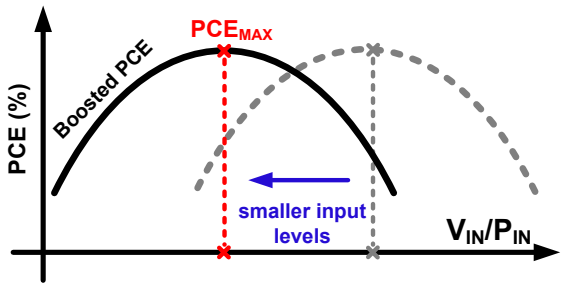
Similar graphs could be obtained for all other switching transistors at different stages.

It can be concluded from the discussion above that in order to achieve high efficiencies for smaller input levels, the gate of transistors need to be biased such that they receive optimal gate-drive voltages at the desired input level. Such a biasing scheme is schematically shown in Figure 3.6a where floating voltage sources are placed between the intermediate nodes ($M_{L,U}$) and the gate of transistors ($G_{p1,2}$, $G_{n1,2}$). The floating voltage sources shift the DC level of the intermediate sinusoidal voltage to provide a boosted gate-drive voltage for the switches. Note that PMOS switches require a negative shift while NMOS switches receive a positive shift. The effect of the proposed biasing scheme as a shift in the PCE curve of the rectifier towards smaller input levels is schematically shown in Figure 3.6b.

Generally the PCE curve of the differential rectifier could be shifted to the left (smaller input levels) and to the right (larger input levels) upon proper biasing of the gate of switches through floating voltage sources. However, the challenging design issue to be addressed is implementation of the floating voltage sources in an area and power efficient manner such that a superior efficiency is obtained at the



(a)



(b)

Figure 3.6: Proposed biasing scheme. (a) Gate-boosted differential rectifier and (b) schematic diagram of the shifted PCE curve.

desired input level with minimal silicon area and power overhead.

As discussed in this section, for a fixed set of requirements dictated by the application, any effort towards increasing the communication distance entails increasing the PCE of the rectifier for small input levels. It was shown that in order to enhance the efficiency of the rectifier, the adverse effect of forward voltage drop and reverse leakage current could be mitigated through proper biasing of the gates of switches. Such a biasing scheme has to provide a boosted gate-drive voltage when the switches are under-driven for a wide range of input levels. In the following sections, efficiency enhancement techniques are presented for UHF differential rectifiers. The efficiency enhancement techniques are mainly based on dynamically biasing the gate of switches through floating voltage

sources connected between the intermediate RF voltage and the gate of switches. The proposed biasing schemes are designed to comply with passive RFID applications and the demand for an external supply (other than the output of the rectifier) is minimized. The proposed schemes are also studied in terms of power overhead and silicon area requirement.

3.2 Proposed Switched Rectifier Scheme[2]

As mentioned in Section 3.1, the input power received by the tags antenna drops rapidly as a function of the distance from the reader (transmitter). Accordingly, insufficient power levels generate small peak-to-peak RF voltages at the input of the rectifier as as the peak voltage available at the chip input, under perfect power matching conditions, is given by [84]:

$$V_{INp} \approx \sqrt{\frac{P_{AV}}{R_{ANT}}} \frac{1}{\omega C} \tag{3.1}$$

where P_{AV} is the available power at the antenna, R_{ANT} is the antenna equivalent resistance, Ω is the antenna resonance frequency and C is the rectifier equivalent capacitance. To enhance the input voltage to the chip, R_{ANT} has to be minimized, however the minimum antenna impedance is dictated by geometrical constraints and maximum efficiency. Therefore as suggested by Equation 3.1, small input RF powers generate insufficient input voltage levels at the input of the rectifier. In order to enhance the resulted deteriorated PCE, gates of switches need to be boosted to shift the PCE curve towards small input levels.

As mentioned in Section 3.1, to boost the gate of switches in region-I, the floating voltage sources need to positively shift the RF gate voltage of NMOS transistors and negatively shift those of PMOS transistors. As a cost efficient candidate to implement the floating voltage sources at each stage of the rectifier, the already generated intermediate voltage of the preceding and succeeding stages could be used in a timely manner.

Note that along with the DC output, the DC level of the intermediate voltage at each stage also builds up along the rectifier chain. Therefore, for each stage, the

[2]The material presented in this section is based on [7]

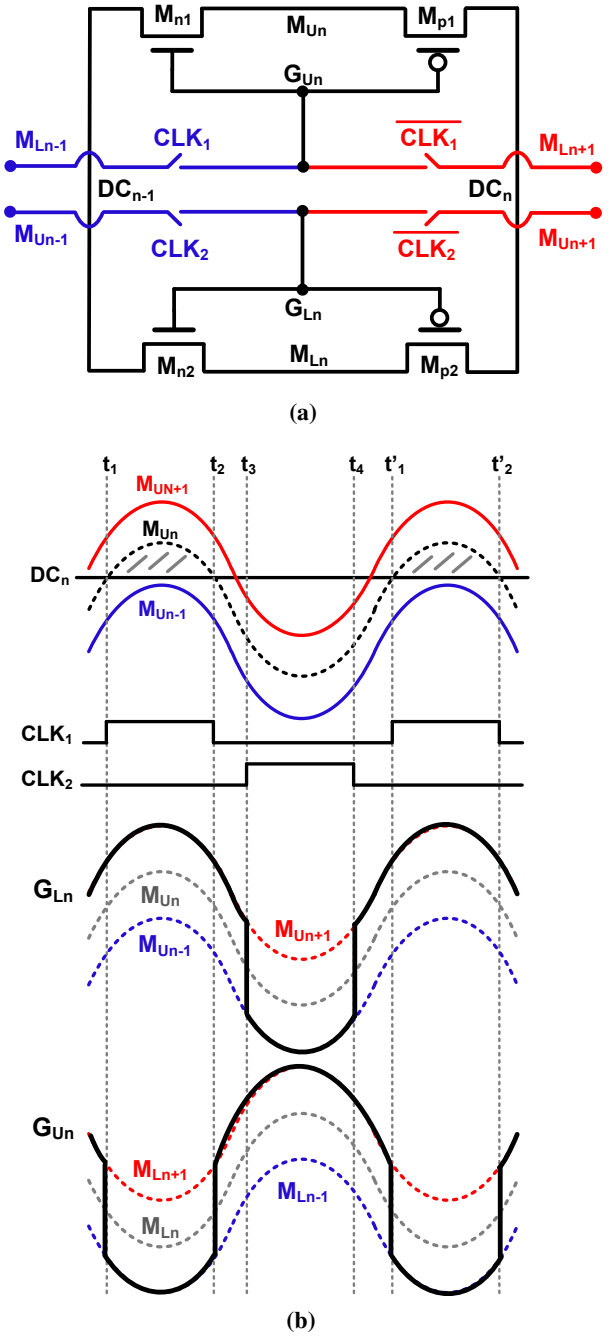


Figure 3.7: Proposed Switched rectifier. (a) Schematic diagram and (b) Timing diagram [7].

intermediate RF voltage of the preceding stage could be exploited as the negatively shifted version, while that of the succeeding stage could be used as the positively shifted version gate-drive voltage. To enhance the performance, these intermediate voltages could be switched in a timely manner to drive the gates of

switches at each stage. The proposed switched rectifier is schematically shown in Figure. 3.7a. During the time interval $t_1 \sim t_2$ ($M_{UN} > DC_n$) when M_{p1} is conducting in forward direction and M_{n1} is isolating, CLK_1 connects the gates of the top branch switches, G_{Un} to the appropriate intermediate voltage of the preceding stage, M_{Ln-1}. Consequently, M_{P1} (which is supposed to conduct) experiences a larger source-gate drive voltage and M_{N1} (which is supposed to isolate) undergoes a larger reverse bias. During the rest of the sinusoidal cycle, $t_1 \sim t'_1$ ($M_{UN} < DC_n$), when M_{p1} is isolating and M_{n1} is conducting, $\overline{CLK_1}$ connects G_{Un} to M_{Ln+1} therefore reinforcing the reverse bias of M_{p1} (which is supposed to isolate) and gate-source drive voltage of M_{n1} (which is supposed to conduct). Same scenario holds for M_{p2} and Mn2 in alternative cycles. The timing diagram of the proposed switching scheme is shown in Figure 3.7b. Assuming an equal voltage increment at each stage, the proposed switching scheme brings a gate-drive boost as large as the DC level increment at each stage i.e.:

$$\begin{aligned} \Delta M_{UL}^{dc} &= \Delta DC_n = cte \\ V_{boost,SWi} &= \Delta M_{UL}^{dc} = \Delta DC_i \end{aligned} \tag{3.2}$$

where ΔM_{UL}^{dc} and ΔDC_n are dc level increments for the intermediate voltage and DC output voltage at each stage respectively and $V_{boost,SWi} =$ is the gate-drive voltage enhancement achieved by the proposed switching scheme at the i^{th} stage of the rectifier. Obviously, the first stage employs its own intermediate voltage ($M_{UL,1}$) for $M_{UL,n-1}$ as there is no preceding stage to the first stage. Accordingly, the last stage uses its own intermediate voltage for $M_{UL,n+1}$. In the proposed switching scheme, the clock signals ($CLK_{1,2}$) at each stage need to be accurately timed to guarantee the maximum charge transfer in forward direction and minimum reverse leakage current. As shown in Figure 3.7b, CLK_1 is ideally on for $t_1 \sim t_2$ interval where $M_{UN} > DC_n$ (shaded area). Although the proposed timing scheme improves forward charge transfer and reverse leakage isolation, it is not perfect since the reverse leakage starts prior to t_2 as shown in Figure 3.3b.

A regenerative amplifier performs the comparison between the DC output of each stage and the intermediate voltage as shown in Figure 3.8.

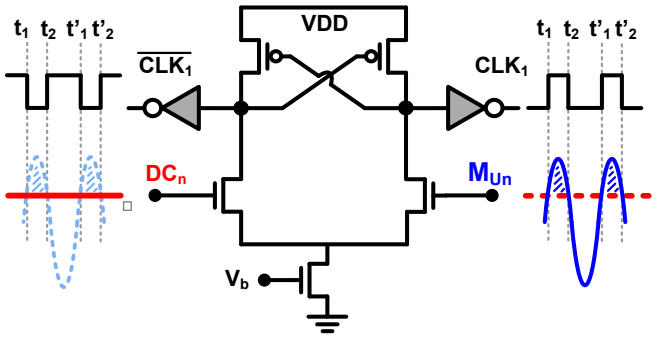


Figure 3.8: Clock generation circuitry [7].

3.2.1 Switched-Capacitor Gate-Boosting Scheme

For small input levels, the rectifier fails to produce substantial voltage increments at each stage which compromises the effectiveness of the switched architecture. Therefore, to enhance the input voltage range of the switched rectifier, additional boosting is required to assist the voltage increment given by Equation 3.2 at each stage.

Accordingly, a floating voltage source is placed between the switched intermediate voltage and the gate of transistors as shown in Figure 3.9a. In order to control the magnified reverse leakage current as the result of the extra voltage shift, it is desirable for the floating voltage source to swap its terminals simultaneous with appropriate clock signals at each stage as shown in Figure 3.9b. During the interval $t_1 \sim t_2$ (CLK_1) when M_{P1} is conducting and M_{N1} is isolating, the floating voltage source adds $-V_{GB1}$ to the switched voltage $V_{M,Ln-1}$ therefore increasing the source-gate drive voltage of M_{P1} and reverse bias voltage of MN1 by $|V_{GB1}|$. During the rest of the sinusoidal cycle, $t_2 \sim t'_1$ (CLK_1) when M_{P1} is isolating and M_{N1} is conducting, the floating voltage source reverses its terminals to add $+V_{GB1}$ to the switched voltage $V_{M,Ln+1}$ therefore increasing the reverse bias voltage of M_{P1} and gate-source drive voltage of M_{N1} by $|V_{GB1}|$. The same scenario holds for the bottom branch at appropriate clock cycles. Therefore, assuming equal voltage increments at each stage, the proposed gate-boosting scheme brings a gate-drive boost as large as:

$$\begin{aligned} \Delta M_{UL}^{dc} &= \Delta DC_n = cte \\ V_{boost,GBi} &= \Delta M_{UL}^{dc} + V_{GBi} \end{aligned} \tag{3.3}$$

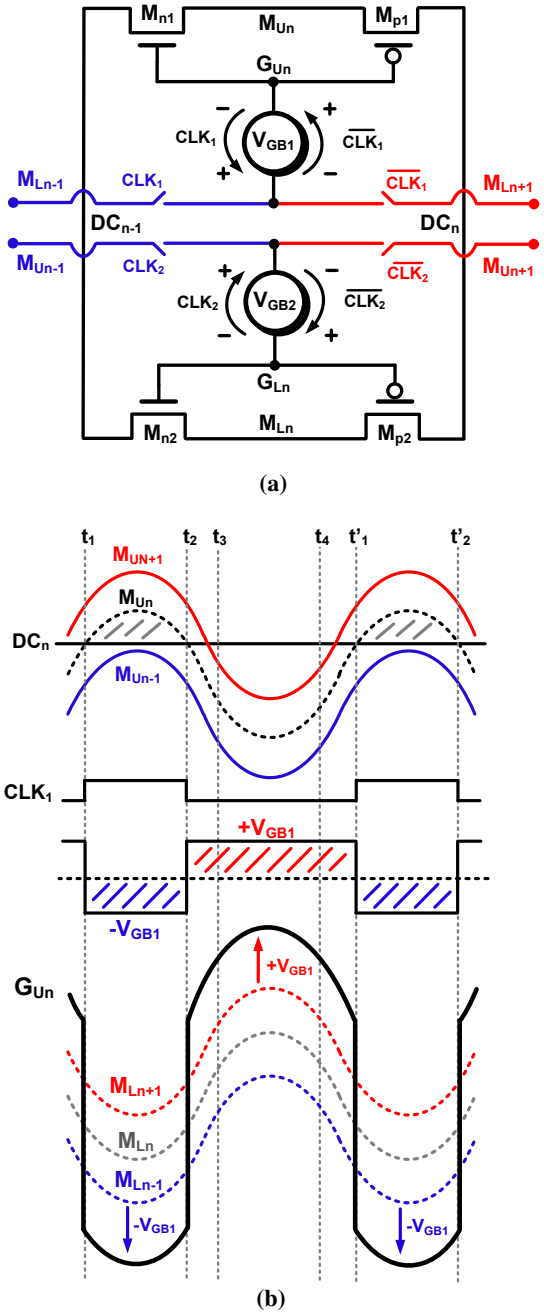


Figure 3.9: Proposed Gate-boosted rectifier. (a) Schematic diagram and (b) Timing diagram [7].

where, ΔM_{UL}^{dc} and ΔDC_n are dc level increments for the intermediate voltage and DC output voltage at each stage respectively, $V_{boost,GBi}$ is the gate-drive voltage enhancement achieved by the proposed gate-boosting scheme for the i^{th} stage and V_{GBi} is the voltage of the floating source at the i^{th} stage.

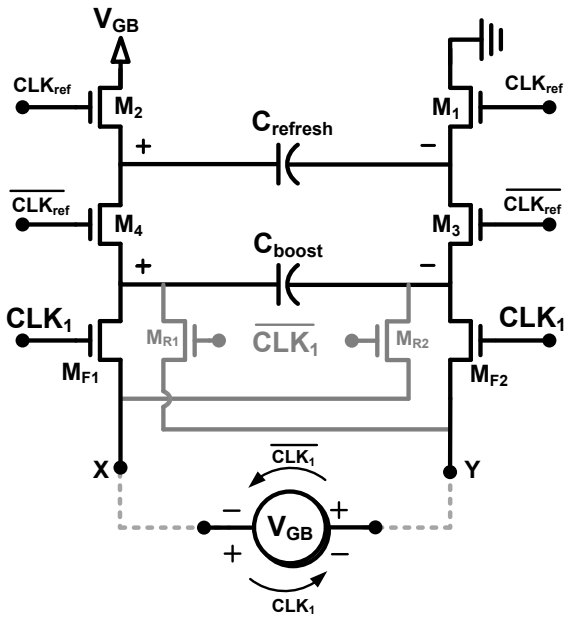


Figure 3.10: Switched-capacitor implementation of the floating voltage source [7].

To implement the floating voltage source capable of interchanging its terminals at appropriate clock cycles, the switched-capacitor (SC) architecture of Figure 3.10 is proposed. C_{boost} is charged to V_{GB} through M_1-M_4 after a few clock cycles and performs as a voltage source subsequently. During CLK_1, M_{F1} and M_{F1} connects C_{boost} between nodes X and Y such that $V_{XY} = +V_{GB}$. During $\overline{CLK_1}$, $M_{F1,2}$ turn off and $M_{R1,2}$ place C_{boost} between nodes Y and X providing a negative voltage between X and Y such that $V_{XY} = -V_{GB}$. $C_{refresh}$ refreshes the voltage on C_{boost} to compensate the charge loss due to leakage current of the switches, the capacitors and the gate parasitics of the main switching transistors to which the SC floating voltage is connected. Note that to drive $M_{1\text{-}4}$ switches for refreshing purpose (CLK_{ref}), a low-frequency clock is more attractive as it leads to smaller power consumption, however if no appropriate low-frequency clock signal exists on the chip, pre-generated CLK_1 can be employed in order to conserve complexity and layout area.

The final configuration of the proposed gate-boosted rectifier is schematically depicted in Figure 3.11 for a three-stage rectifier. Note that Figure 3.11 represents the proposed switched rectifier if V_{GB} generator network and the floating voltage sources are removed.

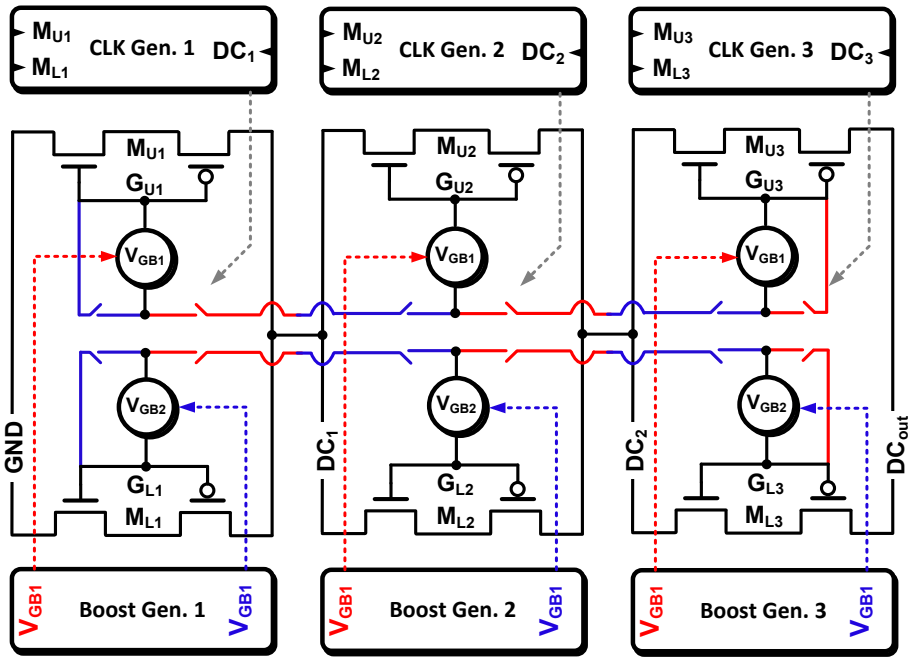


Figure 3.11: Schematic diagram of the proposed gate-boosted rectifier [7].

3.2.2 Design Considerations

1. *Power considerations*: As mentioned in Section 3.1, the biasing schemes incorporated to enhance the efficiency of the rectifier require to be efficient in terms of power overhead they impose on the rectifier and RFID tag. More specifically, the floating voltage sources have to be implemented in a power efficient manner to minimize their loading effect on the rectifier.

The proposed switched rectifier requires two comparators at each stage (total of six comparators for a three-stage rectifier) for clock generation. The two comparators at each stage compare the DC output of the stage with the RF intermediate voltage of the top and bottom branches to produce the clock signals. The relaxed requirements on the accuracy of the comparators facilitate a low-complexity implementation. However, as the comparators are operating at UHF frequencies (950 MHz), they need to be designed carefully to avoid a significant power overhead on the rectifier. In the clock generator of Figure 3.8, the supply voltage could be obtained from the external battery in semi-passive tags. Note that the output of the main rectifier could also be used to supply the comparators in passive tags. However if the input level is too small, the rectifier

may fail to deliver sufficient power to the comparators. To start up the switched rectifier when input level is insufficient, an auxiliary rectifier can be employed to temporarily supply the comparators. The auxiliary rectifier can then be switched off when the output of switched rectifier satisfies the desired value.

The gate-boosted rectifier requires two SC voltage sources (in addition to the two clock generators) at each stage. In the floating voltage source of Figure 3.10, V_{GB} could be supplied from a battery in semi-passive tags. V_{GB} could also be simply extracted from the DC output voltage of an intermediate stage. It should be noted that very small gate-boosting voltages (with respect to voltages being generated at each stage) mitigate the advantages of gate-boosting scheme and very high voltages lead to long, inefficient transitions at the edge of the clock. In passive tags where V_{GB} is supplied by the rectifier, the proposed voltage source does not severely load the intermediate output node to which it is connected in virtue of its small power consumption. The power consumed by the voltage source of Figure 3.10 mainly stems from the leakage current of the two MIM capacitors ($C_{refresh}$ - C_{boost}), switch leakage currents and gate parasitics of the rectifier switching transistors and consequently is in the order of few hundred nano-Watts.

2. *Area considerations*: In addition to small power consumption, the proposed biasing scheme needs to be implemented in an area efficient manner as demanded by the tight silicon area budget of most RFID applications. The comparator incorporated in the switched rectifier consists of an amplifier and two digital buffers and could be implemented in an area efficient manner. The same is not the case for the SC voltage sources as it contains two capacitors. A trade-off exists for the value of the capacitors as dictated by the sizing of the rectifier transistors and frequency of the switching. More specifically, C_{boost} in Figure 3.10 drives the gate capacitance of two switching transistors and therefore has to be significantly larger than the gate capacitances in order not to get fully discharged at each clock cycle. On the other hand, a very large capacitor prolongs the settling time and slows down the switching speed which may cause uncoordinated operation of the switching and gate-boosting.

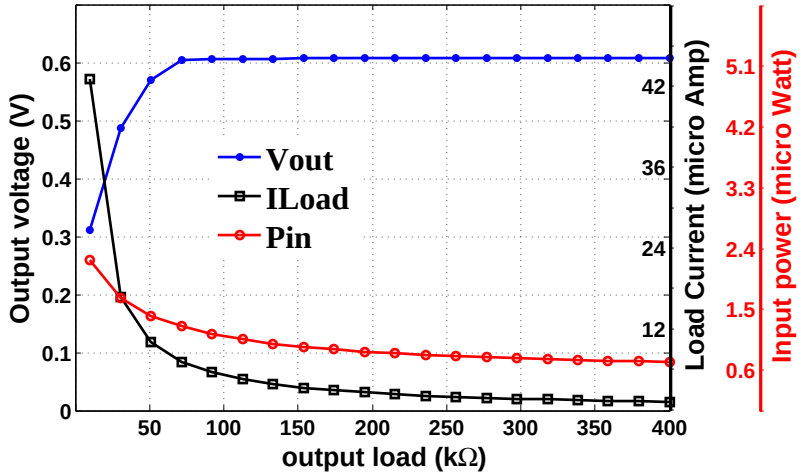


Figure 3.12: Output voltage and current of a rectifier stage versus load values [4].

3.3 Proposed Auxiliary-Cell Boosting Scheme[3]

As shown in Figure 3.5, to achieve a high PCE for small input voltages, the boosting scheme has to positively shift the gate voltage of the NMOS switches and negatively shift the gate voltage of the PMOS switches to decrease their respective effective threshold voltage and accordingly increase their forward current. Switching scheme and SC voltage source can be used to implement the floating voltage sources as described in Section 3.2. However, the complexity, layout area, and power consumption overhead imposed by the required multiple SC voltage sources and the clock generator makes such schemes less attractive in passive RFID applications where area and power efficiency are of paramount importance.

As a more efficient approach, the gate of switching transistors could be driven by the intermediate RF voltages generated at floating (load-less) auxiliary rectifier cells. Note that rectifiers are designed to produce a specific DC current (in a certain voltage range) whose value is dictated by the load specifications. The designated current drive capacity of a rectifier is achieved through proper sizing of the switching transistors and capacitors and optimizing the number of stages. The fixed current drive capacity follows that if the output load (resistance) increases,

[3]The material presented in this section is based on [4].

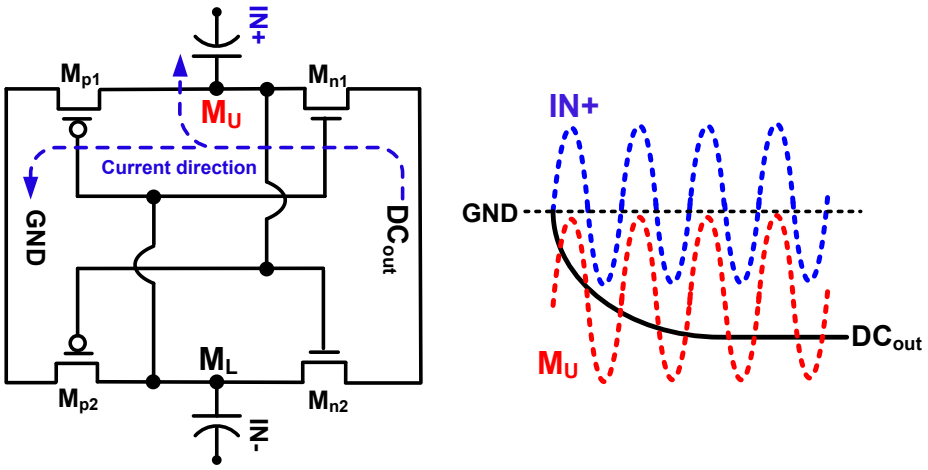


Figure 3.13: Schematic diagram of a reverse-rectifier cell and the associated voltage levels [4].

the output current does not drop at the same rate and therefore, the output voltage grows with the load. This is shown in Figure 3.12 for a single stage rectifier (for an arbitrarily chosen input voltage of 400 mV). As shown in the figure, the output voltage increases as a function of the output load value until it saturates at a specific value. The saturation occurs as the rectifier fails to sufficient current at very large load values and the voltage stops growing with the load value. Note that as the load grows, the rectifier draws smaller currents from the input which in turn reduces the input power of the rectifier cell. This feature will prove beneficial in the proposed scheme as will be explained later.

Based on the above discussion, a floating rectifier cell (i.e., a stage with an open load) will produce a larger output voltage compared to a typical stage which drives the succeeding stage or the output node. Note that the DC level of the intermediate RF voltage at each stage increases in accordance with the output voltage. This characteristic of the rectifier cell could be exploited to obtain positively shifted versions of the intermediate RF voltage to boost the gate of NMOS switches in the main rectifier. However, as mentioned earlier, to boost the gate of PMOS switches, a negatively shifted version of the intermediate voltage is required (see Figure 3.5) which is not readily generated by the conventional differential rectifier. A negative output voltage could be generated by reversing the task of NMOS and PMOS switches, i.e., getting NMOS switches to conduct in the positive cycle of the sinusoidal input and PMOS switches to conduct in the

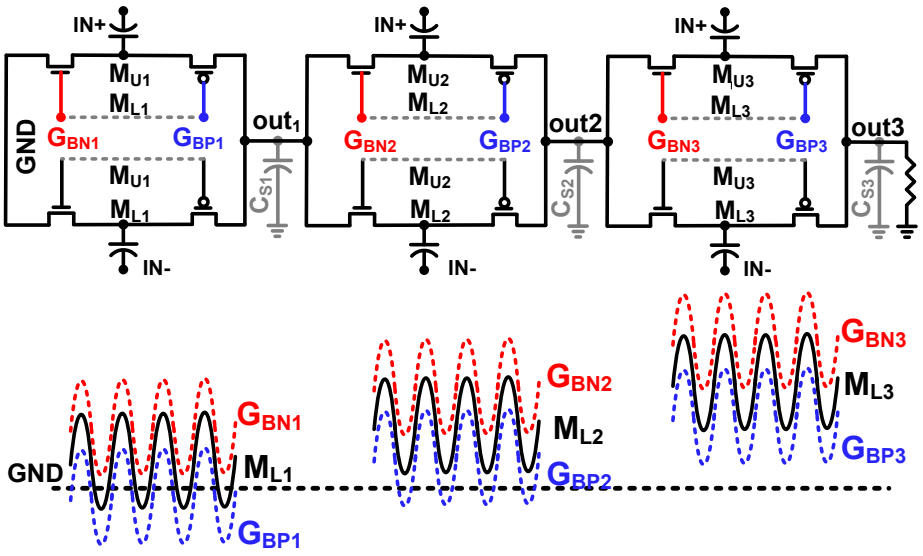


Figure 3.14: Diagram of the intermediate and boosted gate-drive voltages along the rectifier chain [4].

negative cycles of the input signal such that the current drawn from the output node towards the ground discharges the output node and generates a negative DC voltage. Figure 3.13 shows the schematic diagram along with the generated voltage levels and current directions for the top branch of such a rectifier stage which will be referred to as a reverse-rectifier cell.

The floating rectifier and reverse-rectifier cells could be used to provide the required shifted drive voltages for each stage of the main rectifier. As shown in Figure 3.14, the DC level of the intermediate voltages $M_{Li,Ui}$ (and accordingly, the gate voltages) increase along the rectifier chain, i.e., the voltage levels are higher for each stage relative to the previous stage. Therefore, the gate voltages of the switching transistors at each stage need to be boosted separately. In the proposed architecture, two floating rectifier cells are utilized to drive the gate of the switches at each stage of the main rectifier, i.e., one floating rectifier cell to drive NMOS switches (G_{BNi}) and one floating reverse-rectifier cell to drive the PMOS switches (G_{BPi}). G_{BPi} and G_{BNi} are the intermediate node voltages of the floating rectifier cells which are appropriately shifted relative to the intermediate voltages of the main rectifier. With reference to Figure 3.14 the boost values are defined as:

$$\begin{aligned} \mathrm{VBoost_{Pi}} &= \mathrm{VM_{i(DC)}} - \mathrm{VG_{BPi(DC)}} \\ \mathrm{VBoost_{Ni}} &= \mathrm{VG_{BNi(DC)}} - \mathrm{VM_{i(DC)}} \end{aligned} \tag{3.4}$$

Care has to be taken to avoid over-boosting the gate of switches in the main rectifier as over-compensation of the threshold voltage results in an increased reverse leakage current and subsequently degraded PCE. Note that the DC level of the intermediate voltages in a differential rectifier cell directly follow the input DC level. Therefore, the DC level of the intermediate voltages in the floating rectifier cell ($\mathrm{VG_{BPi(DC)}}$ and $\mathrm{VG_{BNi(DC)}}$) could also be adjusted through setting the floating cell's DC input voltage as the reference voltage. In order to guarantee a sufficient boosting level and at the same time avoiding over-boosting the gate of the switches in the main rectifier, the reference (input) voltage of the floating rectifier cells (and consequently the intermediate node voltages $\mathrm{VG_{BPi(DC)}}$ and $\mathrm{VG_{BNi(DC)}}$) have to closely track and follow the intermediate voltages of the main rectifier ($\mathrm{VM_{Ui(DC)}}$ and $\mathrm{VM_{Li(DC)}}$). In other words, in Figure 3.14, $\mathrm{VG_{BPi}}$ and $\mathrm{VG_{BNi}}$ have to trail $\mathrm{VM_{Li}}$ such that a fixed distance between them ($\mathrm{Vboost_{Pi}}$ and $\mathrm{Vboost_{Pi}}$) is always maintained. The tracking could be simply achieved if the reference (input) voltage of the floating rectifier cells is extracted from the voltage levels of the main rectifier cell. For this purpose, in the proposed architecture, the DC input of each stage of the main rectifier (GND, $\mathrm{out_1}$ and $\mathrm{out_2}$ in Figure 3.14) serves as the reference for the associated floating rectifier cell which drives the NMOS switches ($\mathrm{GB_{Ni}}$ generator cells). Likewise, the DC output of each stage ($\mathrm{out_1}$, $\mathrm{out_2}$ and $\mathrm{out_3}$) of the main rectifier provides the reference voltage to the associated floating reverse-rectifier cell which drives the PMOS switches ($\mathrm{GB_{Pi}}$ generator cells).

Figure 3.15 shows the schematic diagram of the proposed auxiliary-cell boosting technique for the second stage of the main rectifier. As seen, the DC input to the second stage,out1 , serves as the reference voltage for the floating rectifier cell (labeled as REF_{N2}) and the DC output of the second stage, $\mathrm{out_2}$, serves as the reference voltage for the reverse rectifier cell (labeled as REF_{P2}). The two floating rectifier and reverse rectifier cells produce the boosted gate-drive voltages $\mathrm{G_{BNL2,U2}}$ and $\mathrm{G_{BPL2,U2}}$ respectively, which are the shifted versions of the

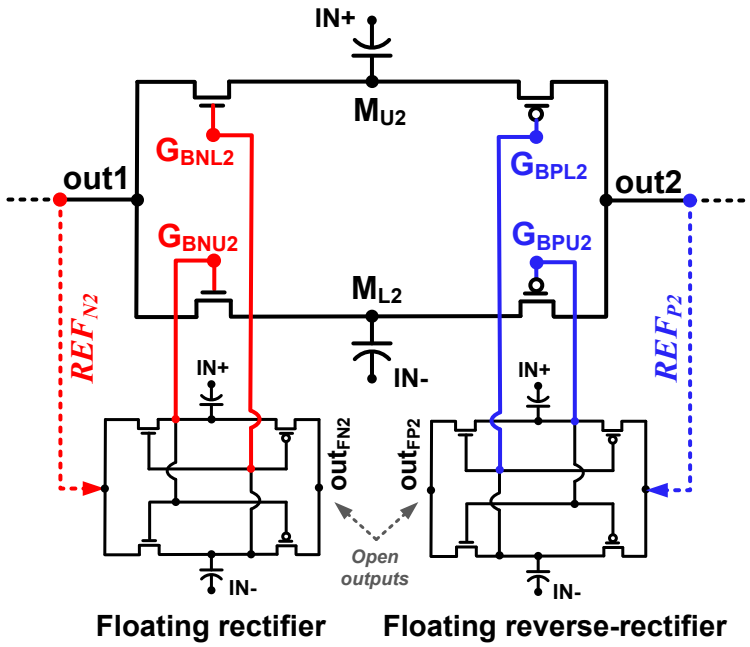


Figure 3.15: Schematic diagram of the proposed auxiliary-cell boosting scheme [4].

intermediate voltages $M_{U2,L2}$ such that the following conditions are satisfied:

$$\begin{aligned} VG_{BNL2(DC)} > VM_{L2(DC)}, VG_{BNU2(DC)} > VM_{U2(DC)} \\ VG_{BPL2(DC)} < VM_{L2(DC)}, VG_{BPU2(DC)} < VM_{U2(DC)} \end{aligned} \tag{3.5}$$

Note that although the second stage of the main rectifier and the floating rectifier cell both receive the same DC input, out1, the floating rectifier cell generates higher DC levels both at its intermediate nodes and the output (Equation 3.5) as it drives an open load while the main rectifier cell drives the succeeding stage. The floating reverse rectifier cell is also designed to generate intermediate voltages with a smaller DC level than that of the main rectifier Equation 3.5.

Figure 3.16 shows the simulated DC voltage levels generated at the second stage of the proposed rectifier. As shown in Figure 3.16a, for different values of the input voltage (in^{+}_{-}), G_{BNL2} and G_{BPL2} are boosted (shifted) with respect to M_{L2} and satisfy the condition mentioned in Equation 3.5. Also as shown in the figure, the output of the floating rectifier, out_{FN2} has a larger DC value compared to

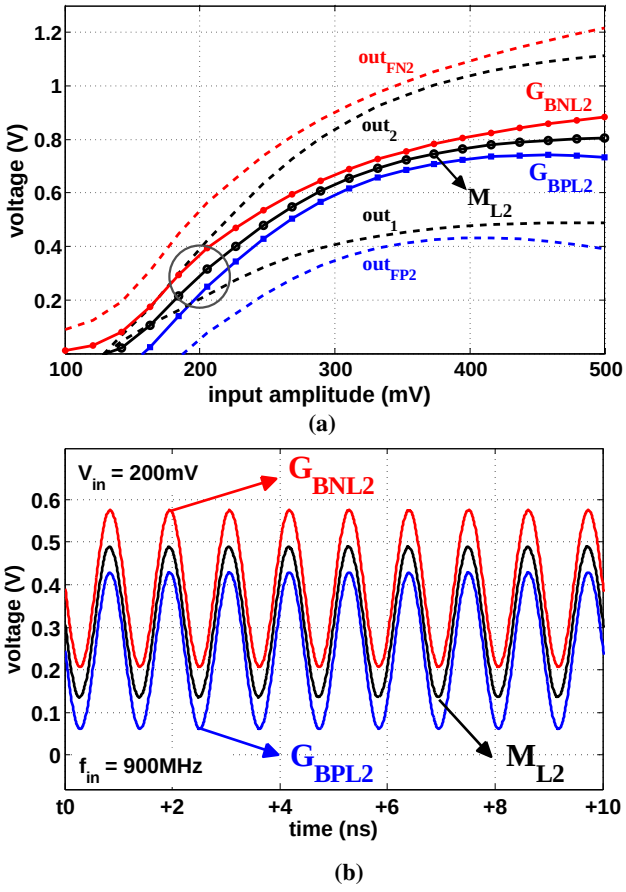


Figure 3.16: Generated voltage waveforms at the second stage of the proposed rectifier. (a) DC level of the boosted gate drive voltages along with the input/output versus input amplitude, (b) Transient waveform of the intermediate node voltage and boosted gate-drive voltages [4].

out_2 and accordingly, out_{FP2} has a smaller DC value than that of out_1. Figure 3.16b shows the transient RF waveforms of the intermediate voltages ML2 along with the boosted gate-drive voltages G_{BNL2} and G_{BPL2} for an input amplitude of 200 mV (circled area in Figure 3.16a) at 950 MHz. As seen, the RF sinusoidal G_{BNL2} and G_{BPL2} are superimposed on their DC values and are negatively and positively shifted versions of M_{L2} respectively.

It should be noted that although the boosting levels ($Vboost_{Pi}$ and $Vboost_{Ni}$ in Equation 3.4) need to maintain a fixed value regardless of the variations $VM_{Li,Ui}$ DC value, their absolute value could be designed through proper sizing of the transistors and capacitors in the floating rectifier cells. If required, higher boosting

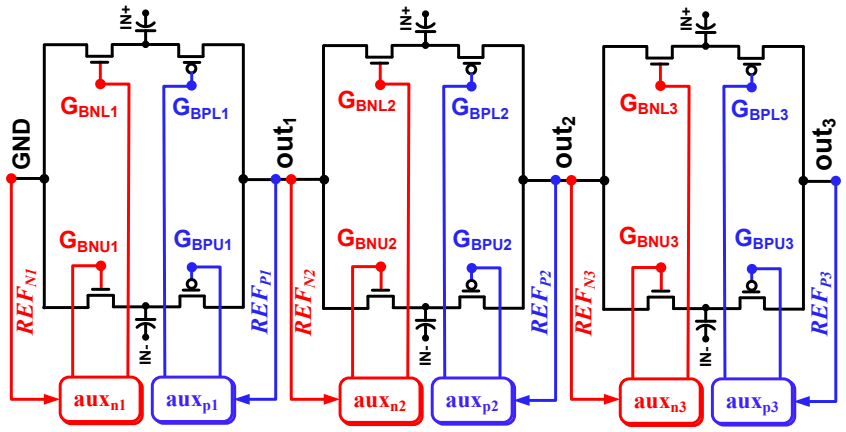


Figure 3.17: Schematic diagram of the proposed auxiliary-cell boosted rectifier [4].

levels could be achieved through adjusting the reference (input) voltage to the floating rectifier cells or by cascading multiple auxiliary cells (where the last stage sees an open load).

Based on the above discussion, the two floating rectifier and reverse floating rectifier cells emulate the operation of the floating voltage sources of Figure 3.6 required for the boosting purpose and consequently efficiency enhancement.

The final configuration of the proposed auxiliary-cell boosting scheme is shown in Figure 3.17 for a three-stage rectifier where each stage receive the boosted gate-drive voltages from the two auxiliary cells allocated to drive the NMOS and PMOS switches separately. All the auxiliary cells receive their inputs from the input/output of nodes of the associated stage.

3.3.1 Design Considerations

1. *Power considerations*: As shown in Figure 3.12, when the resistive load of a rectifier cell increases, its output voltage saturates at some specific voltage while the output current keeps dropping. Since for an open load, the output DC current tends to zero, a floating (load-less) rectifier cell theoretically draws no current (power) from the input. In practice, a very small current is drawn from the input node which is limited to the current required for charging/discharging the parasitic capacitances seen by the input. Therefore, the floating rectifier (reverse rectifier) cells provide boosting at practically no cost in terms of power consumption. Moreover, the proposed auxiliary-cell boosting scheme does not depend on any external power source and performs the boosting in a self-sufficient manner. The

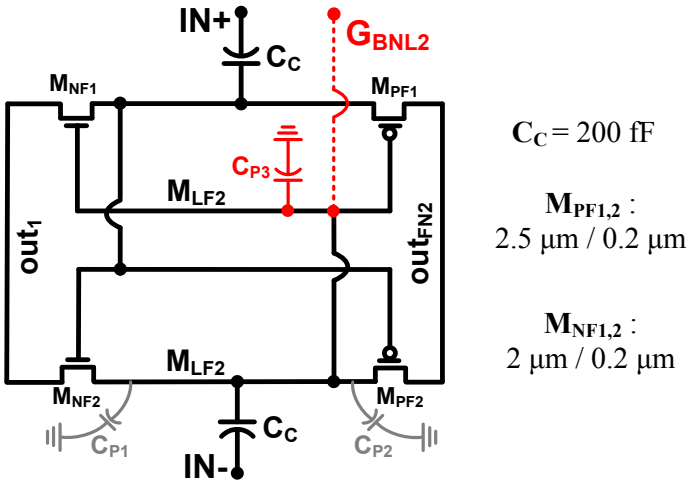


Figure 3.18: Parasitics seen by the coupling capacitors in the floating rectifier [4].

negligible power overhead and independence from external power source makes the proposed auxiliary-cell boosting scheme fully compatible with passive RFID tag applications.

2. *Area considerations*: Since each stage of the rectifier requires two floating rectifier cells (a total of six cells for a three-stage rectifier), layout area overhead imposed by the proposed scheme has to be considered cautiously. To conserve silicon area, the floating rectifier cells can be designed and implemented in much smaller values both for transistors aspect ratios and capacitor sizes. Also note that as opposed to the main rectifier, floating rectifier cells do not require smoothing capacitors at their output. Smaller transistors and coupling capacitors for floating cells (compared to the main rectifier) are allowed since the only load they drive is the capacitance at the gate of switching transistors in the main rectifier (see Figure 3.15). Practically, the coupling capacitors of the floating cells could be very small as long as they maintain a larger value than the summation of the parasitic capacitances they see at the node to which they are connected to. More specifically:

$$C_C \gg C_{P1} + C_{P2} + C_{P3} \tag{3.6}$$

where, as shown in Figure 3.18, C_C is the coupling capacitor of the floating cell,

C_{P1} and C_{P2} are the source/drain parasitic capacitance of M_{NF2} and M_{PF2} respectively and C_{P3} is the summation of the parasitic gate capacitance of M_{NF1} and M_{PF1}, the gate of the switch driven by G_{BNL2} (see Figure 3.15) and the parasitic capacitance associated with C_C itself. Note that M_{LF2} and G_{BNL2} in Figure 3.18 are the same nodes but labeled differently to avoid confusion. The constraint set by Equation 3.6 has to be satisfied in order to guarantee that the amplitude of the boosted (shifted) sinusoidal voltage, G_{BNL2} is not significantly attenuated as the result of the capacitive division between C_C and the parasitics seen at M_{LF2}. Note that amplitude attenuation of the sinusoidal RF gate-drive has to be avoided as it deteriorates the efficiency of the rectifier and compromises the effectiveness of the proposed boosting scheme. More specifically, G_{BNL2} (in Figure 3.17) is given by:

$$G_{BNL2} = \text{IN-} \times \frac{C_C}{C_C + C_{P1} + C_{P2} + C_{P3}} \tag{3.7}$$

Therefore, $C_C \gg C_{P1} + C_{P2} + C_{P3}$ follows that $G_{BNL2} \approx$ IN-. Such a constraint could be easily met with a very small value for the coupling capacitor of the floating rectifier cell relative to that of the main rectifier and thus the proposed architecture could be implemented with minimal area overhead. The typical values of the transistors aspect ratios and the coupling capacitor value of the floating rectifier cell associated with the second stage of the main rectifier are shown in Figure 3.18

3.4 Proposed Quasi-Floating-Gate Boosting Scheme[4]

In the boosting schemes discussed (switched rectifier, SC gate-boosting and auxiliary-cell boosting), the boosting level is a fixed value. The level of boosting (V_{boost}) in the switched rectifier is set by the sizing of the rectifier components (transistors and capacitors) and is given by the DC voltage increments at each stage. In the proposed SC gate-boosting scheme, the boosting level is the summation of the voltage increment per stage and the external voltage (V_{GB}) applied to the SC voltage source. Finally, in the proposed auxiliary-cell scheme,

[4]The material presented in this section is based on [3].

the boosting level is set by sizing of the floating rectifier cells. The fixed boosting levels result in a static biasing. In other words, although the maximum PCE (optimal point) occurs at smaller input levels, the optimal point is only achieved for a single input level (see Figure 3.5). This follows that the PCE curve peaks at a certain input level and drops rapidly at the two sides of the optimal point. However, in many applications where the input level to the rectifier is variable, it is desired to secure a high PCE for multiple points or a wide range of inputs. Such a scheme requires a dynamic biasing mechanism in which the boosting level dynamically adapts with the input level such that the optimum biasing is achieved at multiple or a continuous wide range of input levels.

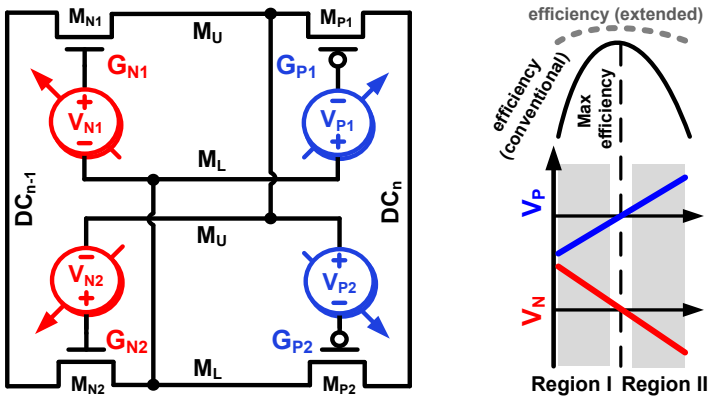
In light of the discussion presented in Section 3.1, to obtain a flat PCE curve (i.e., extended high-efficiency range of operation), a boosting mechanism has to be devised to:

1. Positively boost the gate of switches for input levels smaller than the optimal point (region-I in Figure 3.5), in order to decrease the effective threshold voltage and accordingly increase the forward current.

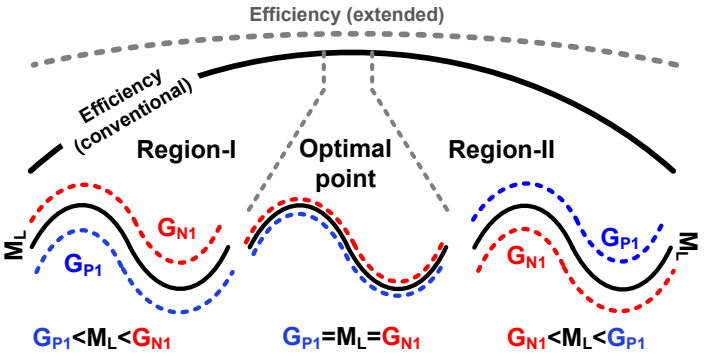
2. Preserve the already generated gate voltages at the optimal point (i.e., provide a zero boost at maximum efficiency point).

3. Negatively boost the gate of switches for input levels larger than the optimal point (see Figure 3.5) in order to increase the effective threshold voltage and accordingly reduce the reverse leakage current.

Such a boosting scheme is schematically depicted in Figure 3.19. Note that as opposed to Figure 3.6, the floating voltage sources are variable with the input level. In region-I, for PMOS switches M_{P1} and M_{P2}, the voltage sources V_{P1} and V_{P2} produce a negative voltage between M_L-M_U and G_{P1}-G_{P2} respectively, therefore providing the appropriate negative offset such that $VG_{P1,2} < VM_{L,U}$. Likewise for NMOS switches M_{N1} and M_{N2}, V_{N1} and V_{N2} produce a positive shift such that $VG_{N1,2} > VM_{L,U}$. With further increase in the input voltage/power, the absolute value of the variable voltage sources decrease and tend to zero such that at the peak of efficiency (optimal input), $V_{P1,2}$=$V_{N1,2}$=0 and $VG_{P1,2}$=$VG_{N1,2}$=$VM_{L,U}$, i.e., the gates of switches receive the optimal DC levels



(a)



(b)

Figure 3.19: The proposed QFG-biased gate-boosting scheme. (a) schematic diagram and (b) PCE curve and the boosted gate-drive voltages for NMOS and PMOS switches [3].

equal to those of a non-boosted rectifier at the maximum efficiency point. Accordingly, in region-II, $V_{P1,2}$ provide a positive offset (negative boost) for PMOS switches $M_{P1,2}$ while $V_{N1,2}$ produce a negative offset (negative boost) for NMOS switches $M_{N1,2}$ such that $VG_{N1,2} < VM_{L,U} < VG_{P1,2}$. The absolute value of the floating voltage sources keep increasing with the input level in region-II as shown in Figure 3.19a. Figure 3.19a shows how the RF gate-drive voltages are superimposed on their boosted DC values in region-I, optimal point and region-II. Obviously in the discussion made above, the PCE curve and the associated regions are those of the conventional (non-boosted) rectifier which is being studied as a basis for the proposed boosting scheme.

Contrary to the static boosting schemes mentioned earlier (where the gates of

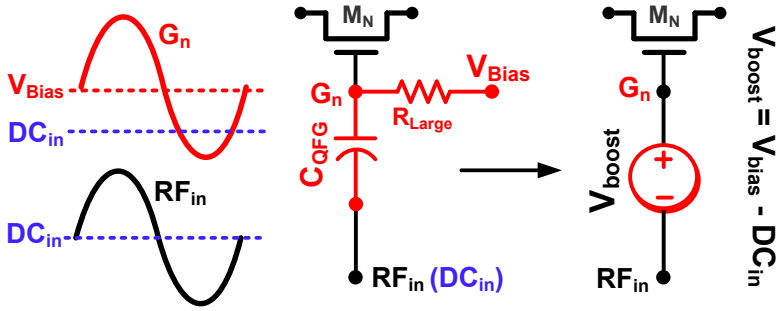


Figure 3.20: Quasi-floating gate biased NMOS transistor [3].

transistor are biased through a switching network, SC voltage source and auxiliary rectifier cells), the dynamic boosting scheme entails a simpler access method to the gate of switches. Quasi-floating gate architecture presented by Ramirez-Angulo *et al.* [85], provides a direct and cost efficient access method to the gate of MOSFET transistors. A QFG biased NMOS transistor is shown in Figure 3.20 along with the associated voltage levels. C_{QFG} capacitively couples the ac signal, RF_{in} to the gate of the NMOS transistor G_n, while a very large resistor, R_{Large} weakly connects V_{Bias} to G_n in order to set the DC voltage of the gate to the desired value. R_{Large} is selected large enough to practically block the ac component of the gate voltage. Therefore, as shown in Figure 3.20, RF_{in} is superimposed on the new DC value (V_{bias}). The combination of C_{QFG} and R_{Large} in the QFG fashion, emulates the function of a floating voltage source placed between RF_{in} and G_n with an offset value as large as $V_{offset} = V_{bias} - DC_{in}$. In practice, R_{Large} is implemented by the large and nonlinear leakage resistance of a reverse-biased p-n junction of a transistor in cut-off region [85]. Figure 3.21 shows a differential rectifier stage in which the gates of switches are biased through QFG scheme.

In order to obtain an extended high-efficiency range of operation (i.e., a flat PCE curve), a dynamic bias generator drives the bias nodes ($Bias_{P,N}$) in the QFG-biased rectifier of Figure 3.21. Also with reference to Figure 3.20, the dynamic bias generator has to set the bias voltages such that the boost value, $V_{N,P}=V_{bias\ N,P}-VM_{L,U(DC)}$ meets all the three specifications listed earlier (see Figure 3.19a). Such bias voltages to satisfy the required specifications for a flat PCE curve are schematically shown in Figure 3.22 in which the DC value of the

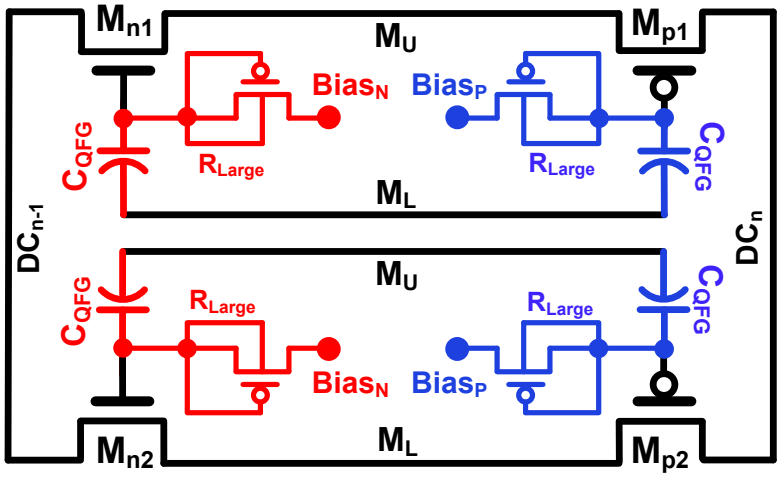


Figure 3.21: Proposed QFG-biased differential rectifier [3].

intermediate voltage at each stage is selected as the reference voltage, upon which $Bias_P$ and $Bias_N$ are generated. Note that at each stage of the rectifier, the DC levels of the intermediate voltages grow almost linearly with the input as schematically shown in Figure 3.22. $Bias_N$ is designed such that V_N provides a positive shift in region-I and a negative shift in region-II while it is zero at the optimal point. Accordingly, $Bias_P$ is selected such that V_P produces negative shift in region-I and positive shift in region-II while it is zero at the optimal point. As shown in Figure 3.22 and assuming a linear growth for the intermediate voltage $DC_{M,L\text{-}U}$, a good candidate for $Bias_N$ is a constant voltage level intersecting with $DC_{M,L\text{-}U}$ at the optimal point. Also, $Bias_P$ has to be set as a linearly increasing voltage with a slope greater than that of $DC_{M,L\text{-}U}$ also intersecting with it at the optimal point.

As mentioned earlier, $DC_{M,L\text{-}U}$ has to be used as the reference for $VBias_{N,P}$ generation. However, $V_{M,\,L\text{-}U}$ is an RF voltage and extracting its DC value requires low-pass filtering which comes at the expense of layout area and power consumption. As a more efficient approach to generate all the bias voltages ($VBias_{N\text{-}1,2,3}$ and $VBias_{P\text{-}1,2,3}$ in a three-stage rectifier), the DC output of the rectifier (OUT_{rec}) could be used at minimal cost in terms of power and area. Such a bias generator is shown in Figure 3.23 where all the bias voltages ($VBias_{N\text{-}1,2,3}$ and $VBias_{P\text{-}1,2,3}$) are generated by a bandgap reference generator.

As shown in Figure 3.23, $M_{1\text{-}5}$ build the core of the bandgap reference

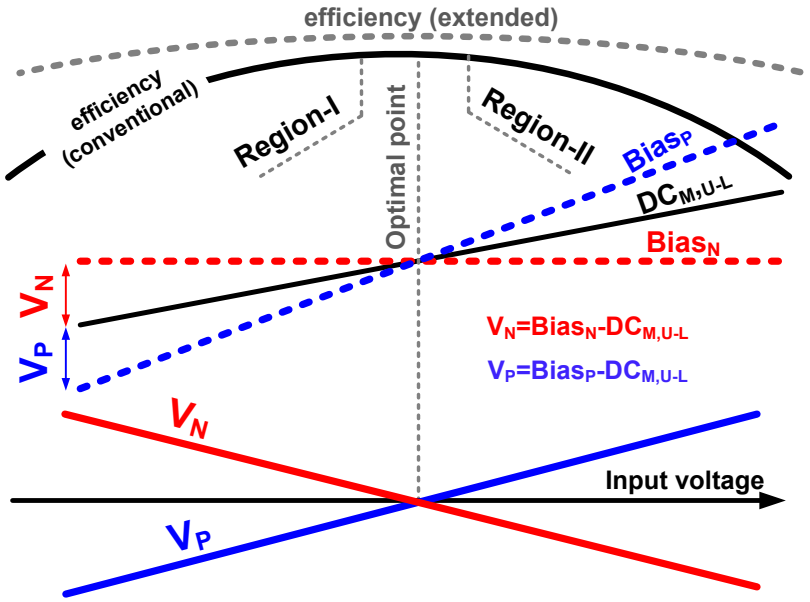


Figure 3.22: Schematic diagram of the intermediate DC voltage, $Bias_P$, $Bias_N$ and the boosting levels of the proposed biasing scheme [3].

generator. At steady state operation (when V_{OUTrec} is already established at the output of the rectifier), node $VBias_{N1}$ produces a fixed, supply insensitive voltage the value of which could be adjusted by proper sizing of the transistors. For a constant $VBias_{N1}$, M_1 and M_2 draw a constant current form OUT_{rec} (i.e., if $M_1 = M_2$, $I_1 = I_2 = cte$) which follows that the overdrop voltage of M_1 is constant and independent of the value of OUT_{rec}. Therefore, $VBias_{P3}$ is established as a negatively shifted version of OUTrec. $M_{6\text{-}9}$ and $M_{8\text{-}11}$ mirror the currents of M_1 and M_5 respectively while $M_{7\text{-}10}$ replicate the function of M_3. Therefore, through proper sizing of $M_{6\text{-}9}$ and $M_{8\text{-}11}$ while M_3=M_7=M_{10}, $VBias_{P2}$ and $VBias_{P1}$ are generated in a similar fashion. Note that $VBias_{P2}$ and $VBias_{P1}$ are also negatively shifted versions of OUT_{rec} with larger shift values respectively (i.e., $VBias_{P3} > VBias_{P2} > VBias_{P1}$). Therefore, M_6 and M_9 are sized larger than M_1 in order to draw larger currents and accordingly higher overdrop voltages. In order to obtain the fixed voltage $VBias_{N2}$ and $VBias_{N3}$, $M_{12\text{-}13}$ and $M_{14\text{-}15}$ replicate $M_{2,4}$ and are sized properly to satisfy $VBias_{N3} > VBias_{N2} > VBias_{N1}$. Note that as opposed to the conventional bandgap reference generator, M_5 and accordingly, $M_{8\text{-}11}$ replace the resistor to further conserve the layout area.

Figure 3.24 shows the simulated output waveforms of the bias generator.

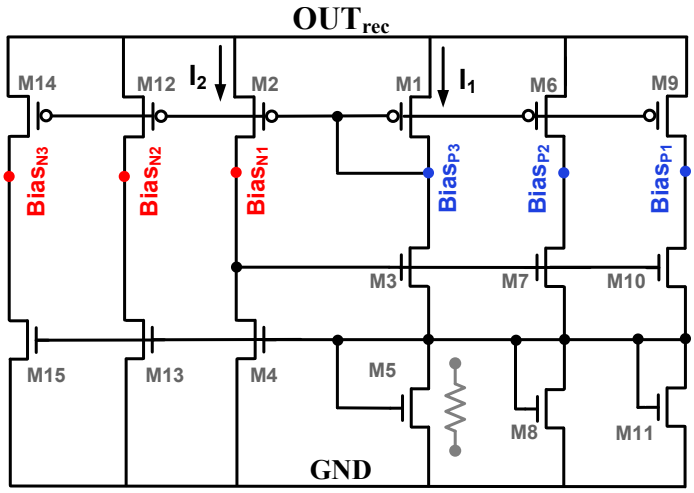


Figure 3.23: The proposed bandgap Bias generator circuitry [3].

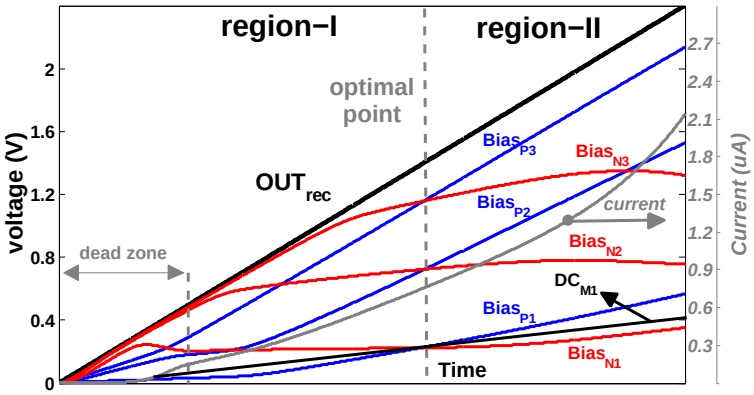


Figure 3.24: Simulated voltage waveforms of the bias generator [3].

Since the output of the rectifier, OUT_{rec} grows linearly with the input voltage, a voltage ramp is used to simulate OUT_{rec}. As seen, the bias voltage pairs ($Bias_{N,P}$) are designed to intersect with the associated intermediate voltage (DC_{Mi}) at the optimal point (only DC_{M1} is shown in the figure). Note that there exists a dead-zone associated with the proposed bias generator, i.e., at the beginning of the ramp, the bias circuitry fails to provide appropriate bias voltages as the supply is insufficient. However, the dead-zone does not interfere with the operation of the rectifier as it occurs at very small output levels where the rectifier is practically inactive. In order to design the intersection points, the DC value of the intermediate voltage of the non-boosted rectifier at the optimal point is selected as

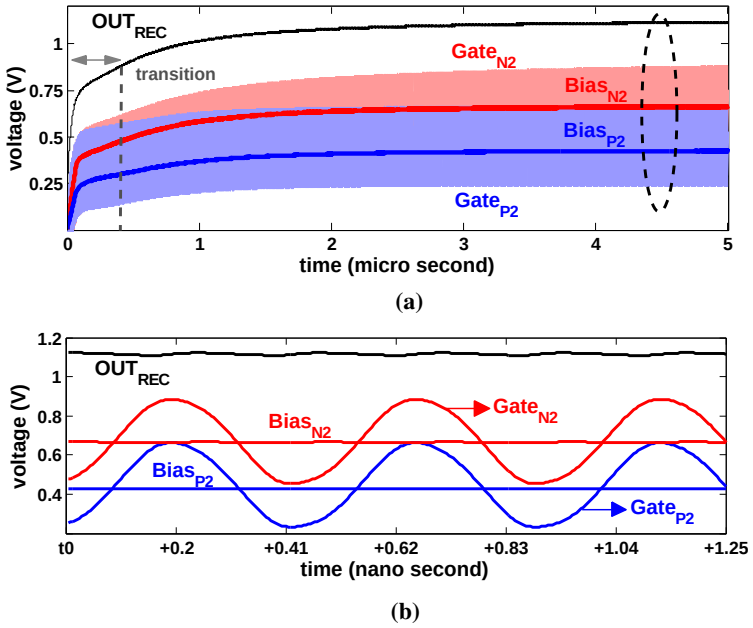


Figure 3.25: (a) Proposed gate boosting scheme. Transient output waveform, and (b) second stage bias and gate voltages [3].

the target and the boosting scheme produces a flat PCE curve at the two sides of the mentioned optimal point.

For an arbitrary input, Figure 3.25a shows the simulated bias voltages $\text{Bias}_{\text{N2,P2}}$ and the QFG-boosted gate-drive voltages $\text{Gate}_{\text{N2,P2}}$ for the second stage of the rectifier. Figure 3.25b showing the enclosed area, depicts in more details how the RF gatedrive voltages ($\text{Gate}_{\text{N2,P2}}$) are superimposed on the boosted DC levels ($\text{Bias}_{\text{N2,P2}}$).

Figure 3.26 shows the schematic diagram of a three-stage QFG biased rectifier. As seen, the output of the rectifier is the only input to the bias generator. Each QFG cell in the figure consists of four QFG resistor-capacitor pair to drive the gate of the four switches at each stage. The cells receive the two intermediate voltages of the stage and shift them towards the delivered bias voltages to produce the boosted gate-drive voltages.

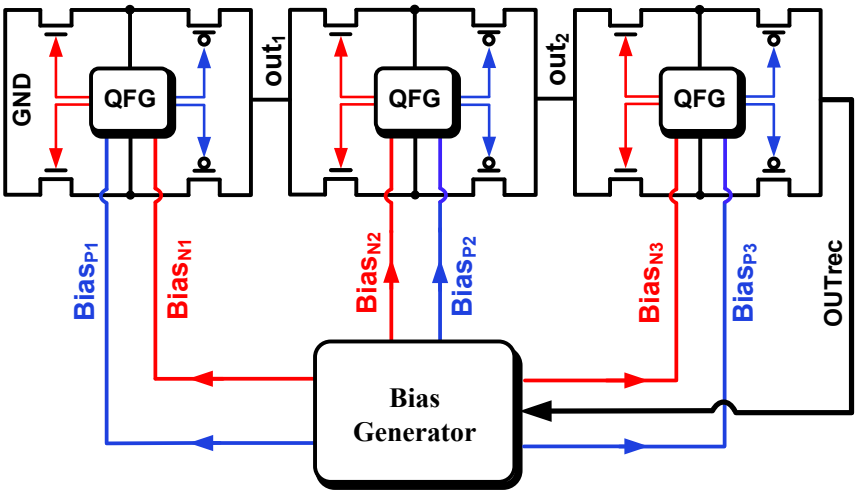


Figure 3.26: Schematic diagram of the proposed QFG boosted rectifier [3].

3.4.1 Design Considerations

1. *Power considerations*: The QFG architecture (combination of R_{Large} and C_{QFG}) facilitates access to the gate of switches at practically no cost in terms of power consumption. R_{Large} could be selected large enough to allow a very small DC current and therefore, its resistive power consumption is negligible. The only source of power consumption in the proposed QFG-boosting scheme is the bias generator (see Figure 3.23). The bias generator draws its required current directly from the output of the rectifier which in turn, degrades the PCE. In order to minimize this effect, it has to be designed with minimal current (power) consumption. However, the bias generator has to readjust the generated bias voltages in response to input level variations and insufficient current results in a slow response time. In a practical RFID application scenario, the rate at which the input level and subsequently the output of the rectifier varies (usually as the result of communication distance variations), is typically on the order of a few milliseconds and is far longer than the settling time of the bias generator.

Slow settling time of the bias generator manifests itself at the start-up when the output capacitor starts to charge up and the output voltage rapidly increases to its final value in a few hundred nanoseconds which is too fast for the bias generator to follow (see the transition region in Figure 3.25a). Therefore, at the start up,

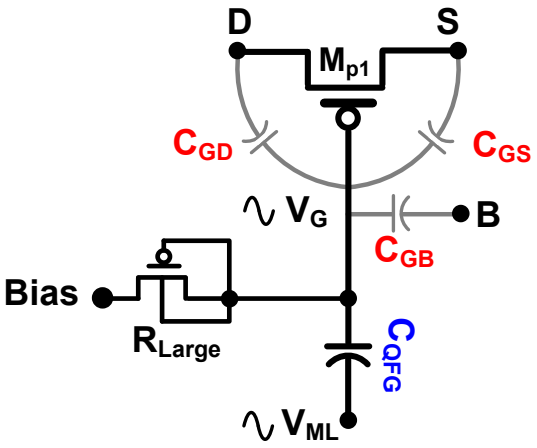


Figure 3.27: Parasitics associated with the gate of a QFG-biased switch.

the rectifier receives incorrect bias voltages. However, this does not interfere with the transient operation, as the QFG delay (which will be explained later) masks the bias voltage and the rectifier functions in a non-boosted fashion without receiving the incorrect bias voltages. It is only long after the output has settled that the gate of switches settle to the generated bias voltages and by then, the correct bias voltages are established. Therefore, as long as the settling time of the bias generator is not longer than that of QFG delay, the latency of the bias generator does not influence the operation of the boosting scheme. This relaxed requirement facilitates designing the bias generator with very small power consumption on the order of one percent of the output power of the rectifier. The current consumption of the bias generator is shown in Figure 3.24.

2. *Area considerations*: Coupling the RF intermediate voltage ($V_{M,\,L\text{-}U}$) to the gate of switches through C_{QFG} slightly attenuates the amplitude of the ac component due to the capacitive division formed between the gate capacitance of the switch, C_G, and the QFG capacitor, C_{QFG}. The ac component attenuation degrades the PCE and has to be minimized. Figure 3.27 shows the QFG-biased switch M_{P1} along with the parasitic capacitances for which the delivered ac component at the gate could be written as [85]:

$$V_G = \frac{s \cdot R_{Large}}{1 + s \cdot R_{Large} \cdot C_{tot}} \times \left(V_{ML} \cdot C_{QFG} + V_S \cdot C_{GS} + V_D \cdot C_{GD} + V_B \cdot C_{GB} \right) \quad (3.8)$$

where C_{tot}, is the total capacitance seen at the RF intermediate voltage node ($V_{M,\,L\text{-}U}$) and is given by:

$$C_{tot} = C_{QFG} + C_{GS} + C_{GD} + C_{GB} \quad (3.9)$$

C_{GS}, C_{GD} and C_{GB} are the gate-source, gate-drain and gate-bulk parasitic capacitances of M_{P1} respectively. For UHF frequencies and assuming $C_{QFG} \gg C_{GS} + C_{GD} + C_{GB}$, Equation 3.8 reduces to:

$$V_G = \frac{C_{QFG}}{C_{tot}} \times V_{ML} \quad (3.10)$$

The assumption $C_{QFG} \gg C_{GS} + C_{GD} + C_{GB}$ follows that $C_{tot} \approx C_{QFG}$ and therefore, $V_G \approx V_{ML}$. It should also be noted that a very large C_{QFG} will result in a longer settling time as will be discussed later. However, this trade-off between ac signal attenuation and settling time is not very challenging since the condition $C_{QFG} \gg C_{GS} + C_{GD} + C_{GB}$ could be easily satisfied with a reasonable settling time.

The QFG architecture of Figure 3.21 forms a low-pass RC filter along the path from the bias node ($Bias_{N,P}$) to the gate of the associated switch ($G_{N,P}$). Therefore, the DC value of the gate experiences a delay before fully settling to the desired value $VBias_{N,P}$. More specifically, as a result of the input level variations, the output of the rectifier (OUT_{rec}) changes and accordingly, the bias generator provides new bias voltages to readjust the boosting levels. However, the new bias values are received at the gate of switches with a delay. As shown in Figure 3.28 , the equivalent capacitance seen by the QFG resistor (R_{Large}) is given by:

$$C_{eq} = C_G + \{C_{QFG} \,||\, \left(C_N + C_{p1} + C_{p2} + C_C \right)\} \quad (3.11)$$

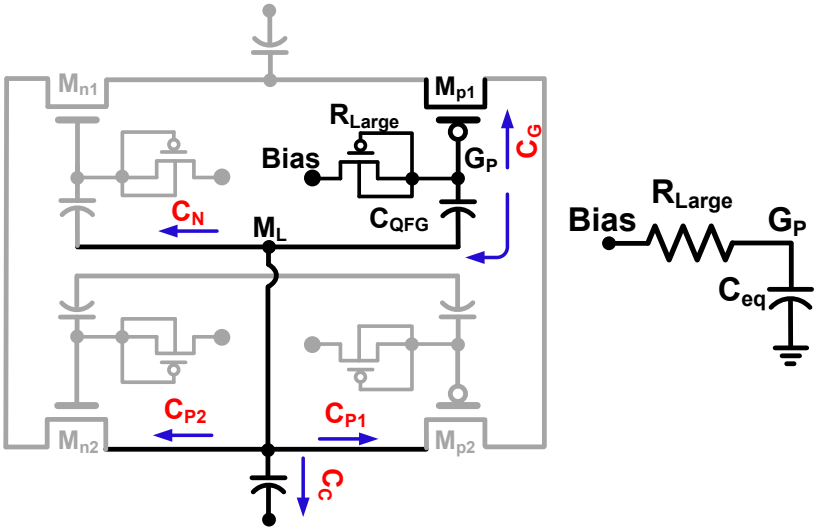


Figure 3.28: Low-pass filtering characteristic of QFG architecture.

where C_{eq} is the capacitance seen by R_{Large}, C_G is the gate capacitance of the switch M_{p1} ($C_G = C_{GS} + C_{GD} + C_{GB}$), C_{QFG} is the QFG capacitance, C_N is the total capacitance node M_L sees toward the switch M_{N1} (i.e., $C_N = C_{QFG} + C_{Gn1}$), C_{p1} and C_{p2} are the parasitic capacitances of the source/drain of M_{p2} and M_{n2} respectively and C_C is the coupling capacitor. The coupling capacitor C_C is typically much larger than all the parasitic components which yields $C_N+C_{p1}+C_{p2}+C_C \approx C_C$.

As mentioned earlier, C_{QFG} could be implemented with a very small value (equal to a quarter of C_C in the proposed scheme). Therefore $C_{eq} \approx C_G+0.2C_C \approx 0.2C_C$ which for a typical C_C=500 fF gives an equivalent capacitance of 100 fF. The average value of R_{Large} is on the order of 1 MΩ∼10 MΩ which gives the average time constant of $T=R_{Large} \times C_{eq}=0.1\mu s \sim 1\mu s$ for the QFG low pass filter. The gate of switches require a few time constant periods to settle to the desired value $V_{BiasN,P}$ (typically $T_{settle}=4 \cdot R_{Large} \times C_{eq}=0.4\mu s \sim 4\mu s$). The settling response time of the QFG architecture approximated above is much faster than the rate of input variations in a practical RFID tag application (typically on the order of a few milliseconds). Therefore, the trade-off associated with the value of C_{QFG} (ac signal attenuation and QFG delay) could be resolved with a reasonably small value of C_{QFG} and consequently minimal layout area overhead. Figure 3.29 shows the settling behavior of the QFG architecture in response to a step function of

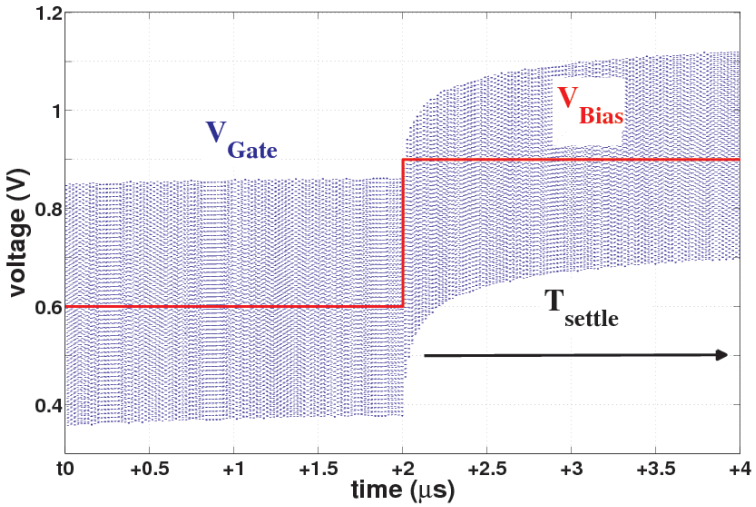


Figure 3.29: Transient response time of QFG architecture.

amplitude 300 mV (600 mV to 900 mV) applied as V_{Bias}. As shown in the figure, the gate of the transistor settles with a good accuracy to the desired value (i.e., 900 mV) within 2 μs.

3. *Bias generator design considerations*: In regards to the operation of the proposed bias generator, there are a few issues in addition to power and area overhead which need to be considered carefully in the design process.

a- The generated bias voltages (as a function of input level) are an approximation of the theoretical ideal values. In order to obtain ideal bias voltages (and consequently optimum effective threshold values for switches) for any given input level, the DC value of the intermediate voltage at each stage has to be extracted and processed. For any given input level, a feedback controller is required to exercise different bias values and continuously monitor the output voltage of the rectifier for a maximum level. The bias voltages associated with the maximum level are the ideal values for the specific input voltage of interest. However, the complexity overhead would compromise the marginal efficiency improvement gained by such an ideal approach.

b- The bias voltages by the bandgap reference generator will deviate from the designated values as the result of process and temperature variations. However, a very robust design for the bandgap reference generator is not mandatory as the

overall efficiency performance of the proposed QFG-boosted scheme is not sensitive to slight variations in the bias voltages. Moreover, an inherent feedback loop partially corrects the generated bias voltages in case of discrepancy. Note that if for any input level in region-I, the generated bias voltages are higher than the desired value, while the PCE drops, the output voltage grows since the switches are over-boosted. However, with reference to Figure 3.23, higher output voltage OUT_{rec} (and consequently higher intermediate voltage level $DC_{M,U\text{-}L}$) produces smaller boost levels as $V_{N,P} = V_{Bias\ N,P} - DC_{M,U\text{-}L}$ and therefore act to correct the over-boosting. In region-II, higher than desired bias voltages signifies under-boosting and therefore results in the decreased OUT_{rec} which in turn works towards decreasing the bias voltages and the negative boost. The reverse scenario occurs if the bias voltages are smaller than what is desired.

c- The resistance of the reversed-biased p-n junction (R_{Large}) is voltage level dependant and changes with V_{Bias} and V_G variations. However, its absolute value does not interfere with proper operation of QFG scheme as long as its impedance maintains large enough to block the ac component of the gate voltage and prevents DC current flow, to or from the bias node. The only effect of the variable R_{Large} manifests itself in the settling time of the QFG architecture. As explained in details earlier, for typical capacitance values, a 10X increase in the value of R_{Large} still gives reasonable settling times.

d- As a final remark, it is worth mentioning that generally maintaining the high PCE for input levels beyond the maximum efficiency point (i.e., region-II) is not as crucial as it is for input levels below it. In particular, a conventional (non-boosted) rectifier is designed to supply a load at the optimal efficiency point. Although the ratio of the output to input power drops beyond the optimal point, the output power keeps growing with the input regardless of the efficiency drop. Thus, the load is guaranteed to receive the required energy for proper operation. A flat PCE curve proves specifically beneficial in applications where the input power (continuous sinusoidal wave) is only transmitted for a short period of time and the rectifier stores the received energy in a battery or a super capacitor. Therefore, higher PCE translates to a higher stored energy to run the tag for a longer time. Moreover, the proposed scheme facilitates optimizing the rectifier for smaller inputs.

3.5 Post-Layout Simulation Results for the Proposed Efficiency Enhancement Techniques

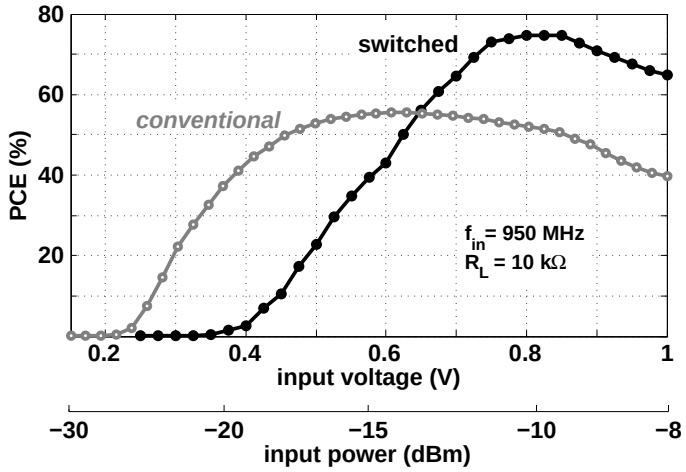
Proof-of-concept prototypes of the three-stage rectifiers incorporating the proposed efficiency enhancement schemes were designed and laid out in a 0.13 μm CMOS technology. The transistor aspect ratios were designed to optimize the performance at the frequency of operation and based on load requirements. Capacitors were implemented by MIM structure. The three proposed efficiency enhanced rectifiers were studied in terms of PCE, output voltage and power, load value and frequency of operation.

3.5.1 Switched Rectifier and switched-capacitor Boosted Rectifier [5]

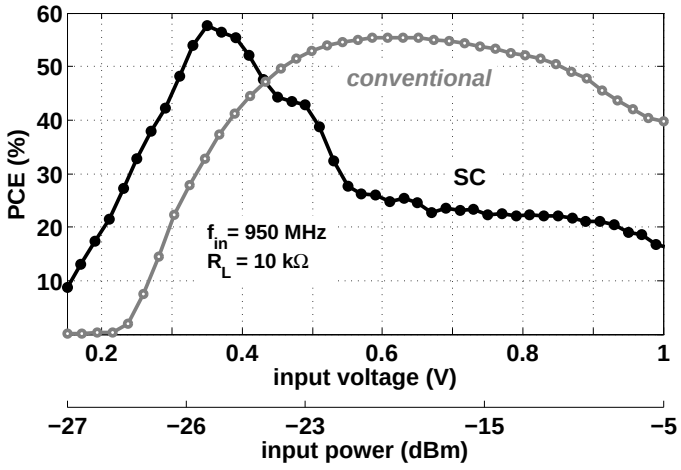
External $V_{DD} = 0.6$ V, $V_B = 0.3$ V and $V_{GB} = 0.2$ V are externally applied as the clock generator supply, the clock generator tail bias voltage and the SC voltage source boost value respectively. For an input frequency of 950 MHz and R_L=10 kΩ, Figure 3.30a and Figure 3.30b show the PCE curves for the switched and SC rectifiers respectively versus the input voltage and power. The PCE curve of the conventional (non-boosted) rectifier is also shown for comparison. Note that the power axis only refers to the proposed rectifiers and does not show the input power of the conventional one. The power consumption of the clock generators and the V_{GB} network are accounted for in obtaining the PCE. The six clock generators (two for each stage) dissipate a total power of 7.2 μW and the six V_{GB} distributers consume 6.5 μW. As shown, the switched rectifier achieves a 74% PCE at -10 dBm which outperforms the conventional rectifier.

It should be noted that compared to the conventional rectifier, the switched rectifier fails to enhance the PCE for small input levels as the voltage increment at each stage is insufficient for proper operation of the proposed boosting scheme. The SC rectifier on the other hand receives the external V_{GB} and outperforms the conventional rectifier at very small input levels (long communication distances). The SC rectifier achieves a PCE of 57% at -26 dBm. In terms of input voltage the maximum efficiency for the gate-boosted rectifier occurs at 350 mV input amplitude which proves a significant enhancement over the corresponding

[5] The material presented in this subsection is based on [7].



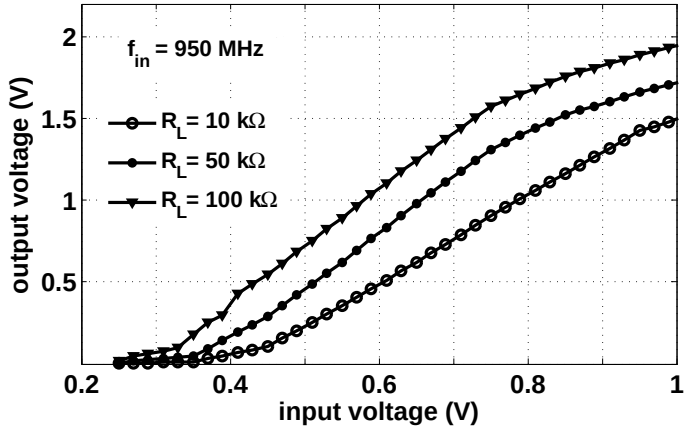
(a)



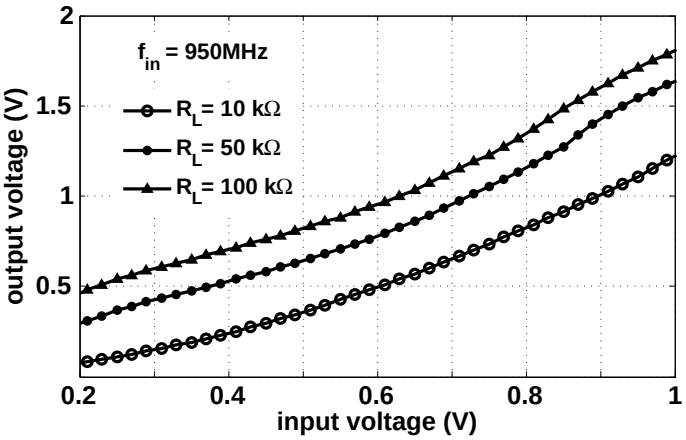
(b)

Figure 3.30: PCE performance (a) Switched rectifier, and (b) switched-capacitor rectifier [7].

maximum efficiency input voltage of 800 mV for its switched rectifier counterpart. Moreover, as inferred from Figure 3.30, the gate-boosted rectifier is capable of providing acceptable PCE for input voltage amplitudes well below the threshold voltage of CMOS transistors in 0.13μm technology where $V_{thn} = 0.355$ V and $V_{thn} = -0.325$ V. However, the input voltage range enhancement is achieved at the cost of more power consumption (exposed by booster network) and consequently smaller overall PCE. Also as shown, with respect to switched rectifier, PCE of gate-boosted rectifier drops for smaller values



(a)

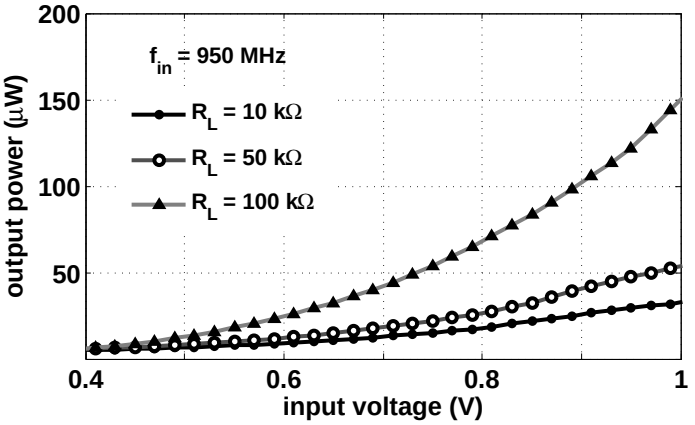


(b)

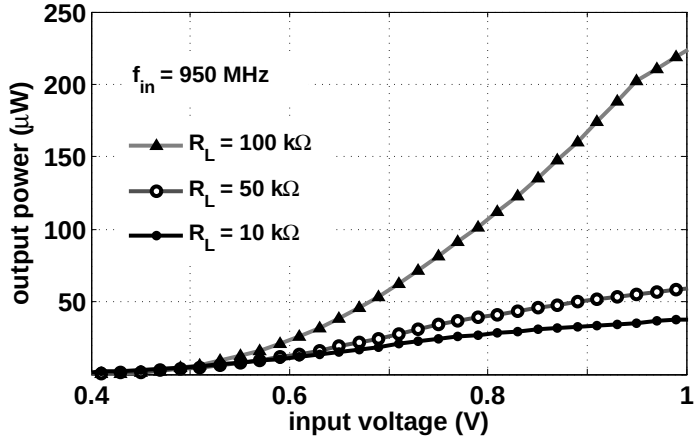
Figure 3.31: Output voltage versus load value. (a) Switched rectifier, and (b) switched-capacitor rectifier [7].

of input power and input voltage, which is due to the fact that beyond a certain point corresponding to maximum efficiency, extra boosting poses additional leakage currents which leads to the observed PCE degradation.

The rectified output voltage versus load value of the switched and SC rectifiers are shown in Figure 3.31a and Figure 3.31b respectively. As shown in the figures, the SC-boosted rectifier provides a lower turn-on voltage compared to the switched rectifier. For a load of 100 kΩ, the output voltage of 0.5 V is achieved at the input voltage of 0.45 V and 0.22 V for the switched rectifier and SC rectifier respectively. Also note that larger load generates larger output voltage and consequently higher



(a)



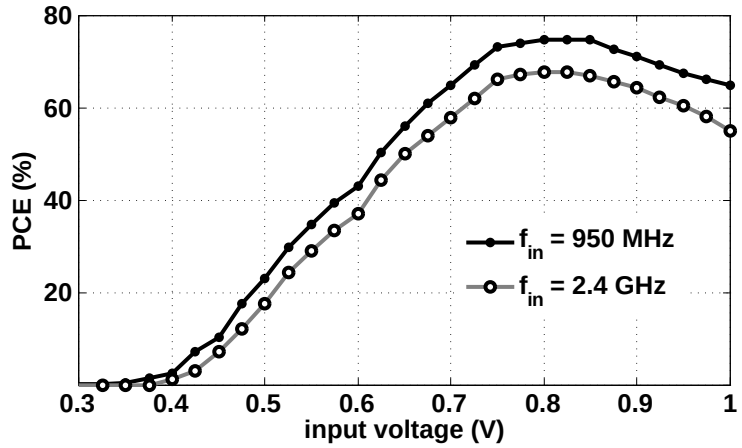
(b)

Figure 3.32: Output power versus load value. (a) Switched rectifier, and (b) switched-capacitor rectifier [7].

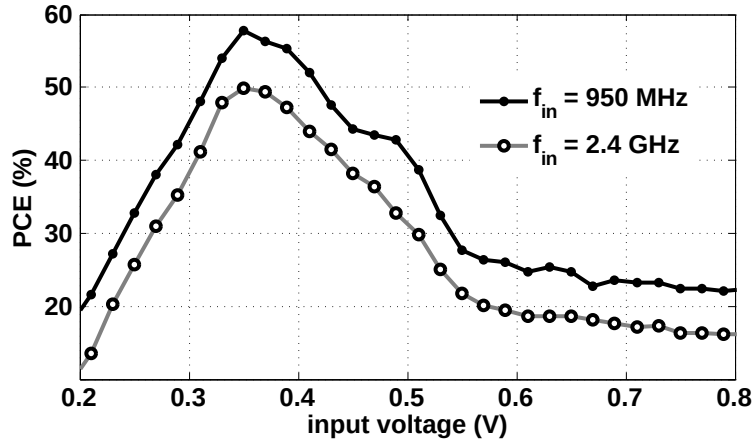
voltage increments at each stage which in turn enhances the switching scheme performance.

The output power versus load value of the switched and SC rectifiers are shown in Figure 3.32a and Figure 3.32b respectively. As shown in the figures, the SC-boosted rectifier provides a higher output power for similar input voltage.

Finally, the frequency performance of the two rectifiers are depicted in Figure 3.33 for 950 MHz and 2.4 GHz input frequencies. As shown, the PCE performance is degraded at higher frequency which is attributed to the higher



(a)



(b)

Figure 3.33: Frequency performance. (a) Switched rectifier, and (b) switched-capacitor rectifier [7].

power consumption of the clock generator. Moreover, the comparator incorporated to provide the clock edges fail to perform as accurately at 2.4 GHz. The adverse effect of parasitic capacitances of both switches and switching transistors also contribute in degradation of PCE at higher frequencies.

3.5.2 Auxiliary-cell Boosted Rectifier [6]

The proposed auxiliary-boosted rectifier is fully compatible with UHF passive RFID applications and requires no external supply or circuitry. For a 950 MHz

[6]The material presented in this subsection is based on [4].

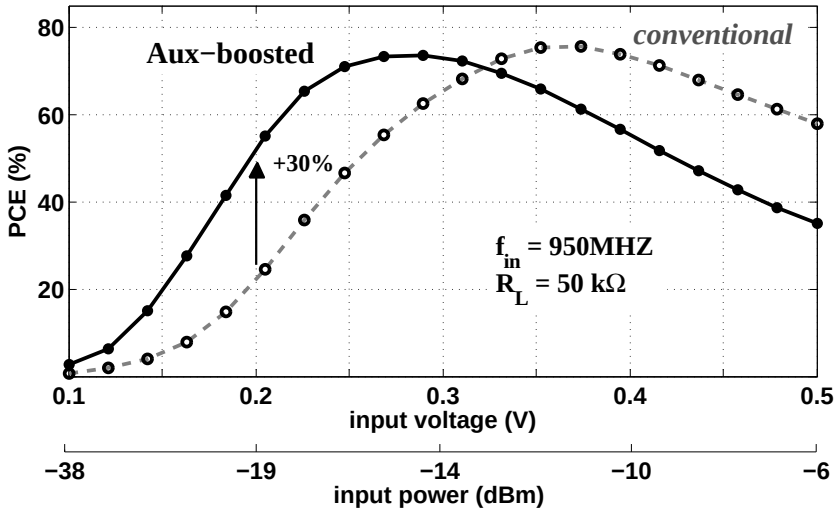


Figure 3.34: PCE of the proposed auxiliary-cell boosted rectifier [4].

input frequency and 50 kΩ load, the PCE of the proposed auxiliary-boosted rectifier along with that of the conventional (non-boosted) rectifier are shown in Figure 3.34. As compared to the conventional architecture, the enhanced efficiency scheme provides a higher PCE for smaller input levels which corresponds to a longer communication distance.

As seen from the figure, the efficiency curve of the proposed rectifier is shifted to the left relative to the convectional rectifier and a PCE of 54% is achieved at the low input voltage/power of 200 mV ($-$ 19 dBm) while the PCE is 24% for its conventional counterpart at the same input level. The PCE curve could be further shifted to the left (towards smaller inputs) through optimizing the floating rectifier cells and therefore manipulating the boosting levels. Note that the peak PCE value for the proposed rectifier is approximately 1% smaller than that of the conventional rectifier which can be attributed to the power consumption of the floating rectifiers (boosting generation circuitry).

For a load of 50 kΩ, the output voltage of the proposed auxiliary-boosted rectifier is compared with that of the conventional rectifier in Figure 3.35. As shown in the figure, the boosted rectifier generates a 0.6 V output at the input level of 0.2 V, while this value is 0.25 V for its conventional counterpart.

As a function of the load resistance, the output voltage, PCE and the output

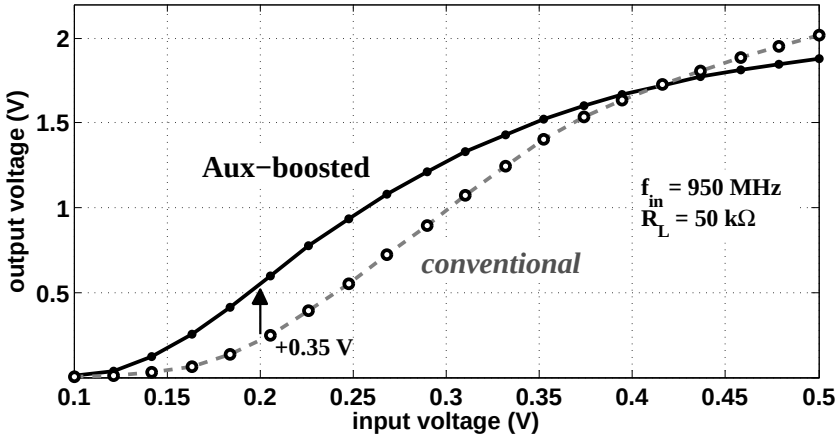


Figure 3.35: Output voltage of the proposed auxiliary-cell boosted rectifier [4].

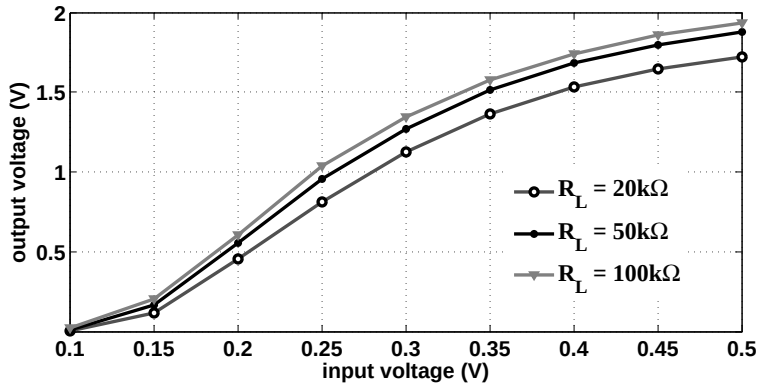
power of the proposed auxiliary-boosted rectifier are shown in Figure 3.36a, Figure 3.36b and Figure 3.36c respectively. Since the boost-generator (floating rectifier cells) receives their reference from the output voltages of the main rectifier stages, they track the DC level variation of the output as the result of load variations. Therefore, the gates of switches receive appropriate boosting regardless of the load (output voltage variations) and the load dependency observed is what is expected from the conventional rectifier. In other words, the boosting generator does not impose additional load dependency.

Finally, the frequency dependency of the proposed auxiliary-boosted rectifier is shown in Figure 3.37 for 950 MHz and 2.4 GHz input frequencies. In virtue of the small aspect ratios of the boosting generator (floating rectifier cells), the proposed rectifier is not severely affected by the increase in the frequency of the input. The minor PCE degradation at 2.4 GHz compared to 950 MHz frequency is attributed to the adverse effect of parasitic of the floating cells as well as the main rectifier.

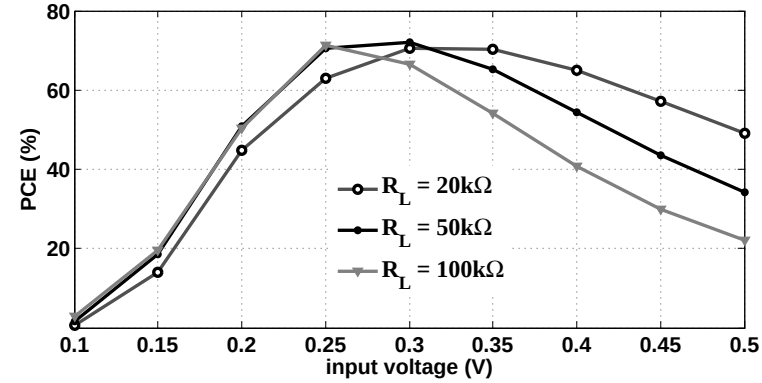
3.5.3 Quasi-Floating-Gate Boosted Rectifier [7]

The proposed QFG-boosted rectifier is fully compatible with UHF passive RFID applications and no external supply or circuitry is used. The bias generator

[7] The material presented in this subsection is based on [3].



(a)



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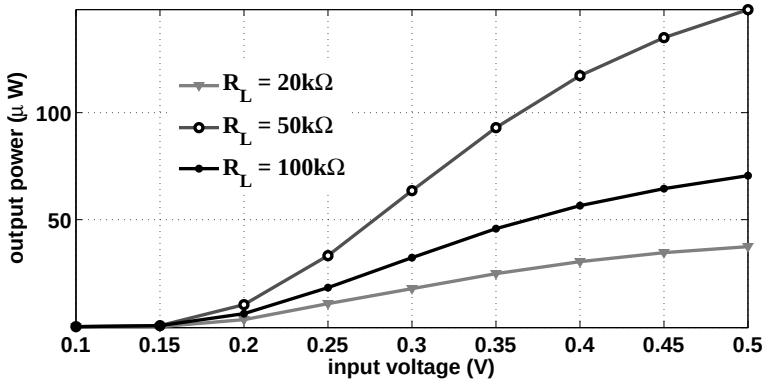


(c)

Figure 3.36: Performance of the proposed auxiliary-cell boosted rectifier as a function of load value. (a) Output voltage, (b) PCE and (c) Output power [4].

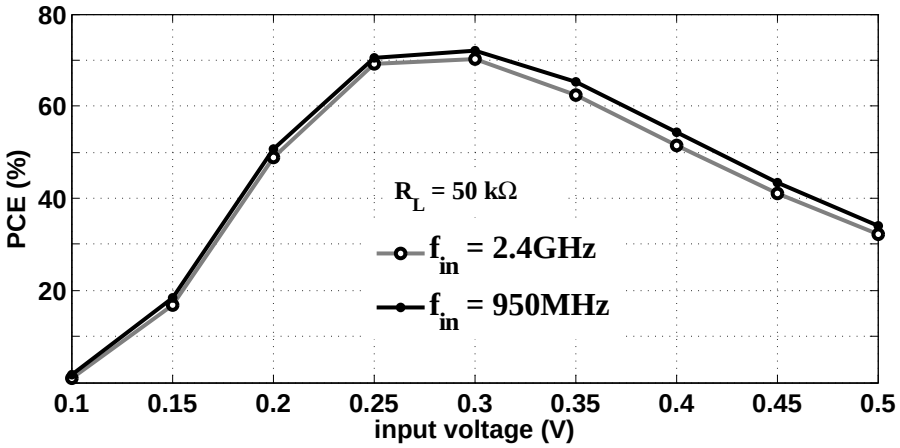


Figure 3.37: Frequency dependency of the proposed auxiliary-cell boosted rectifier [4].

(bandgap reference) is supplied by the main rectifier output.

For a 30 kΩ load and at 2.4 GHz input frequency, the PCE of the proposed QFG-boosted rectifier is shown in Figure 3.38 along with the PCE of the conventional (non-boosted) rectifier. Compared to the conventional rectifier, the QFG-boosting scheme provides a rather flat PCE curve around the maximum efficiency point (V_{in}=0.45 V) by reducing the rate at which efficiency drops through dynamically biasing the gate of switches. The PCE of the proposed rectifier stays over 60% for a wide input range from 0.25 V to 0.7 V (0.45 V voltage range corresponding to 12 dBm) while this range for its conventional counterpart is from 0.38 V to 0.56 V (0.18 V corresponding to 4 dBm). Note that the PCE of the QFG-boosted rectifier at the optimal point is slightly smaller than that of the conventional rectifier (66.6% compared to 68.9%) which is attributed to the power consumption of the bias generator.

As discussed in Section 3.4, at the optimal point, the QFG-boosted rectifier and the non-boosted rectifier receive the same gate-drive voltages. Therefore they theoretically achieve similar efficiency. However, the QFG-boosted rectifier still supplies current to the bandgap reference generator which slightly degrades its PCE performance at the optimal point. The power overhead imposed by the reference generator is overcompensated for the rest of input range by virtue of optimum biasing provided to the gate of switches and the resulted flat PCE curve. As shown

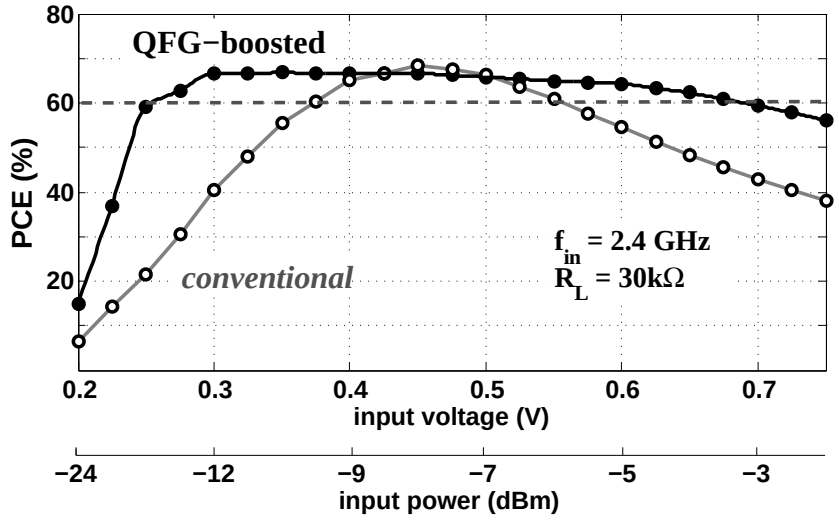


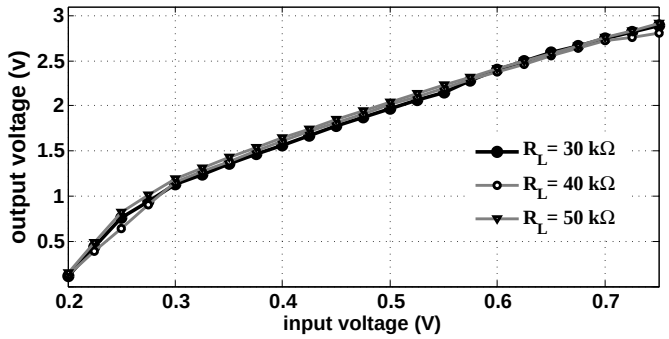
Figure 3.38: PCE of the proposed QFG-boosted rectifier [3].

in Figure 3.38, the PCE of the proposed rectifier drops rapidly for input amplitudes smaller than 0.25 V as the bias generator fails to produce correct bias voltages when the output of the rectifier (OUT_{rec}) is too small (see the dead zone region in Figure 3.24).

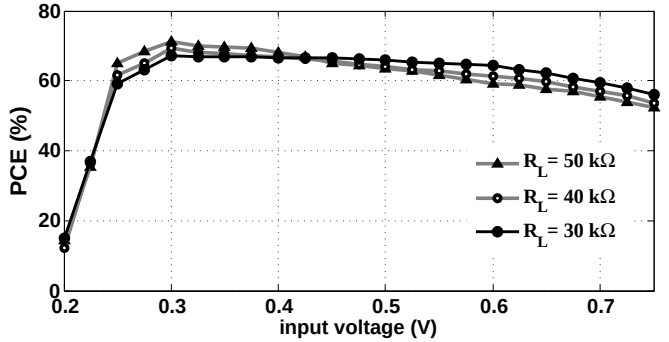
As a function of the load resistance, the output voltage, PCE and the output power of the proposed QFG-boosted rectifier are shown in Figure 3.39a, Figure 3.39b and Figure 3.39c respectively. As shown in the figures, since the bias voltages and the resulted boosting levels are generated in accordance with the output of the rectifier (in a feedback loop fashion as discussed in Section 3.4), the output voltage and PCE of the QFG-boosted rectifier is almost insensitive to load variations. This load independency relaxes the output regulation requirements and is specifically desirable in applications where the load is variable.

The frequency dependency of the proposed QFG-boosted rectifier is shown in Figure 3.40. Note that the bandgap reference is not affected by the frequency of operation as it receives the rectified DC output of the rectifier and generates DC bias voltages. The degraded PCE performance of the rectifier at the higher frequency is due to the parasitics of the main rectifier transistors and coupling capacitors as well as the parasitics of QFG architecture.

Figure 3.41 shows the current drawn by the bandgap bias generator from the



(a)



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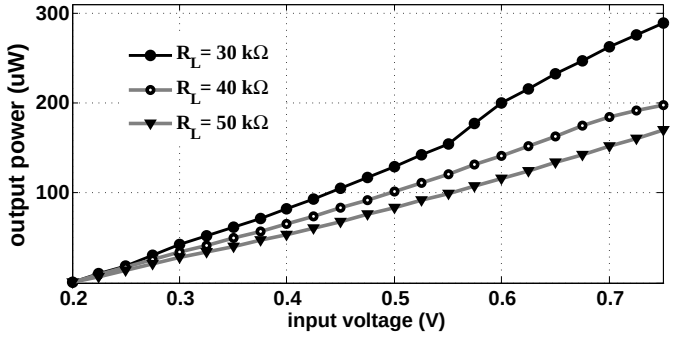


(c)

Figure 3.39: Performance of the proposed QFG-boosted boosted rectifier as a function of load value. (a) Output voltage, (b) PCE and (c) Output power [3].

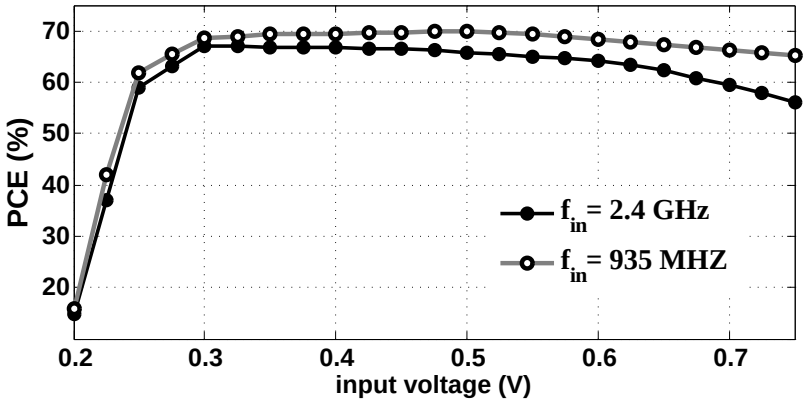


Figure 3.40: Frequency dependence of the proposed QFG-boosted rectifier [3].

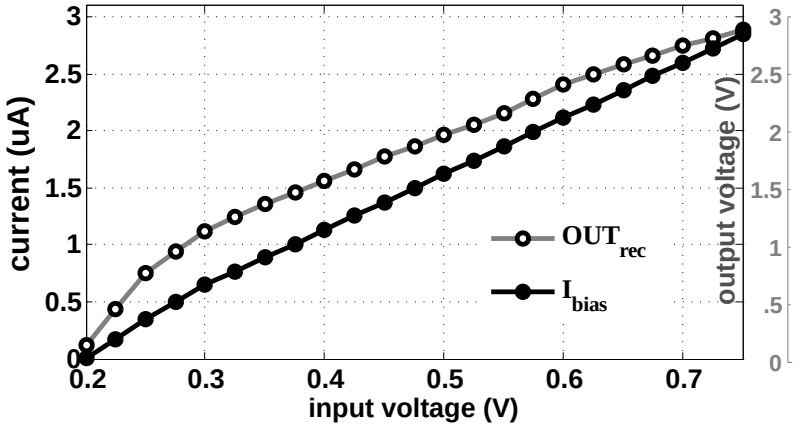


Figure 3.41: Current consumption of the bandgap bias generator [3].

output of the rectifier. As shown, the current consumption of the reference generator grows linearly with its supply voltage (the output of the rectifier, OUT_{rec}). At the optimal point (V_{in} = 0.45V), the bias generator consumes 2.42 μW (corresponding to 1.77 V$\times$1.37 μA) which contributes to the 2.3 % reduction of the efficiency (66.6%) as compared to the conventional rectifier (68.9%).

The layout views of the proposed rectifiers are shown in Fig. 42. As shown in the figure, the switched rectifier area is 280μm$\times$70μm, the switched-capacitor rectifier area is 690μm$\times$420μm, the auxiliary-boosted rectifier area is 300μm$\times$220μm and the QFG-boosted rectifier area is 320μm$\times$140μm.

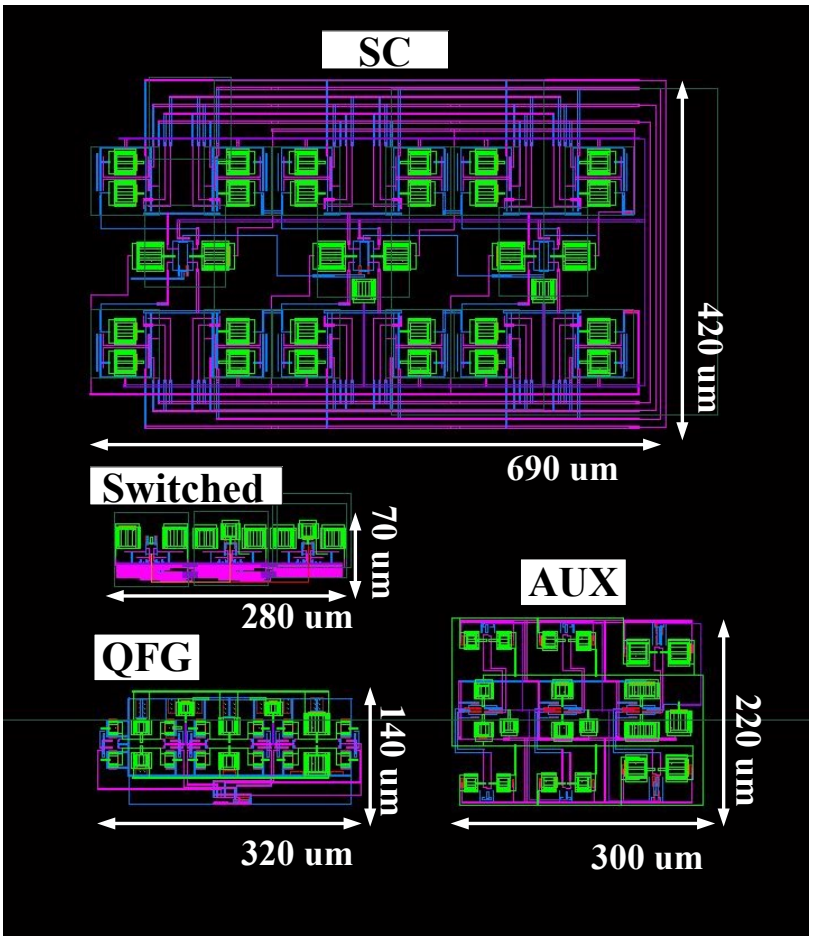


Figure 3.42: Layout view of the proposed rectifiers.

Although the sizing requirements of capacitors associated with each boosting scheme are slightly different (as discussed earlier in this chapter), the number of capacitors per stage for each scheme could be considered as a rough estimation of the area overhead imposed by each technique. The switched rectifier does not require any capacitor and only relies on the clock generator and small-sized switches (see Figure 3.7) and therefore occupies the smallest area among the proposed rectifiers. On the other hand, the SC-boosted rectifier incorporates four SC voltage sources at each stage with two capacitors per voltage source ($C_{refresh}$, C_{Boost} in Figure 3.10), adding up to a total of eight capacitors per stage accounting for its largest layout area. The auxiliary-boosted rectifier requires two rectifier

Table 3.1: Performance summary of the proposed efficiency enhancement techniques and comparison with state-of-the-art [3, 4, 7].

Reference	Technology	Frequency	Load	V_{out} (PCE_{max})	PCE_{max}	PCE (LV)
[78]^{a*}	0.18 μm	953 MHz	10 kΩ	0.6 V ($-$12.5 dBm)	67.5 % ($-$12.5 dBm)	28 % ($-$19 dBm)
[78]^{b*}	0.18 μm	953 MHz	30 kΩ	2.5 V ($-$6 dBm)	62 % ($-$6 dBm)	10 % ($-$19 dBm)
[79]**	0.18 μm	950 MHz	2 μW	0.5 V (0.36 V)	23 % (0.36 V)	23 % (0.36 V)
[80]*	0.18 μm	950 MHz	4 μA	0.5 V (0.36 V)	60 % (0.36 V)	46 % (0.3 V
SW*	0.13 μm	950 MHz	10 kΩ	1.4 V (0.8 V)	74 % ($-$10 dBm)	24 % (0.5 V)
SC*	0.13 μm	950 MHz	10 kΩ	0.6 V (0.34 V)	57 % ($-$26 dBm)	45 % (0.3 V)
AUX*	0.13 μm	950 MHz	50 kΩ	1.25 V (0.29 V)	73 % (0.29 V)	54 % (0.2 V)
QFG*	0.13 μm	2.4 GHz	30 kΩ	1.8 V (0.45 V)	66 % (0.3$\sim$0.5 V)	60 % (0.25 V)

$\star$Post-layout simulation results. $\star\star$ Measurement results.
^{a}single-stage prototype ^{b}three-stage ^{c}whole power extraction system
^{d}PCE$>$60% for 0.25V-to-0.7V

cells per stage with two coupling capacitors each (Figure 3.15), adding up to a total of four capacitors per stage. The QFG-boosted rectifier requires four QFG cells per stage with one capacitor per QFG cell (Figure 3.21) resulting in a total of four capacitors per stage. Note that the auxiliary boosted rectifier occupies a larger area compared to QFG-boosted rectifier since as opposed to the QFG-boosted rectifier, the size of the coupling capacitors in floating rectifier cells grows along the rectifier chain to produce sufficient boosting.

Table 3.1 provides the performance summary of the proposed efficiency enhanced rectifiers along with a comparison with the state-of-the-art designs in the same category of UHF differential rectifiers. As shown in the table, the switched rectifier archives a high PCE of 74% for a moderate input level of -10 dBm while the switched-capacitor rectifier provides a good PCE of 57% at the low input level of -26 dBm. The auxiliary-boosted rectifier also provides a high PCE of 73% for the small input voltage of 0.29 V while the QFG-boosted rectifier achieves a goos PCE of 66% for a wide range of input voltages between 0.3 V to 0.5 V.

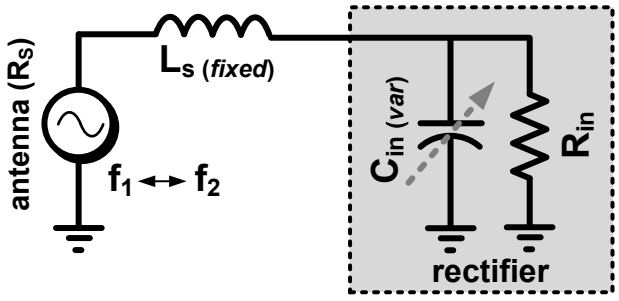


Figure 3.44: Proposed matching scheme.

3.6 Proposed Dual-Band Matching Scheme [8]

Although the rectifier constitutes the core of the wireless power harvesting unit, in practice, it is the combined efficiency of the antenna and the rectifier (*rectenna*) that affects the overall performance of the power harvesting unit. Various architectures have been proposed to facilitate a dual frequency band rectenna [86–89]. However, most of the designs address the problem by using discrete (off-chip) antenna structures which generally need a relatively large footprint and thus may not be applicable to applications that require a small antenna (e.g., biomedical implants).

It should be noted that the input impedance of a CMOS rectifier is a parallel combination of a capacitor C_{in} and a resistor R_{in} as shown in Figure 3.44 [79]. Therefore, for a fixed antenna architecture, one could modify the value of the input capacitance (C_{in}) to obtain the required matching at different frequencies. The resistive (real) part of the input impedance represents the average DC current drawn by the input. As shown in Figure 3.45 for the first stage, the capacitive part of the input impedance accounts for the series combination of the coupling capacitors C_C and the parasitic capacitances seen at the intermediate node, C_{par}. Note that for $C_C \gg C_{par}$, the input capacitance is dominated by C_{par} in which the capacitance of M_{n1} ($C_{S,n1}$) is the biggest contributor. The value of $C_{S,n1}$ is a function of its gate bias voltage. Therefore, the input capacitance of the rectifier can be adjusted by modulating the bias voltage of the NMOS switches of the first stage ($M_{n1,2}$). To avoid the adverse effects of the bias voltage variation on the PCE of the rectifier (as discussed in Section 3.4), an auxiliary floating cell could

[8] The material presented in this subsection is based on [1].

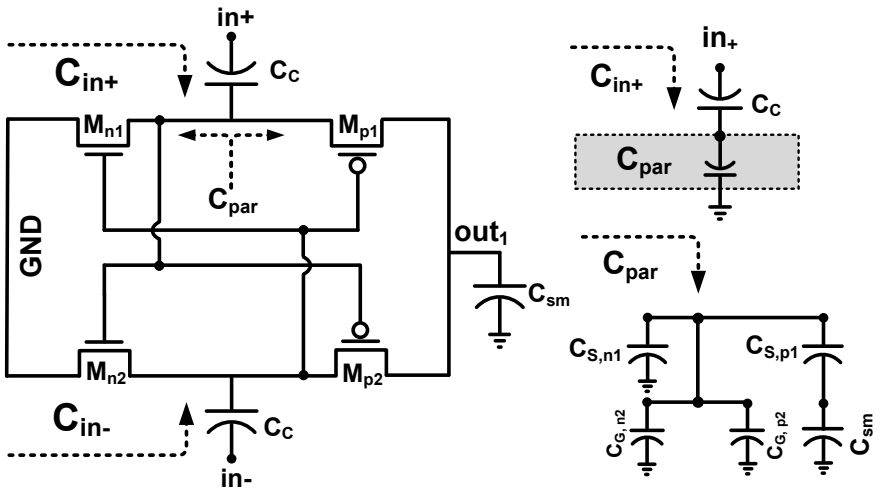


Figure 3.45: Schematic of the first stage of the rectifier and its input capacitance.

be connected in parallel with the main rectifier (similar to the technique proposed in Section 3.3) such that the desired variation in C_{in} is obtained by adjusting the bias voltage of the NMOS switches in a fashion similar to technique used in Section 3.4. The resonance frequency of the matching network in Figure 3.44 is given by $f_{res} = 1/2\pi\sqrt{L_s C_{in}}$. For a fixed L_S, to obtain a voltage matching for two input frequencies f_1 and f_2 (where $f_1 < f_2$), C_{in} has to be adjusted such that $C_{in1}/C_{in2} = (f_2/f_1)^2$.

As shown in Figure 3.46, C_{in} could be increased by connecting the gates of $M_{1,2}$ to a higher voltage (V_{bias}). The rectifier starts in mode-2 ($f_{in} = f_2$) with $C_{in} = C_{in2}$ (as the flip-flop controller has reset $SW = 0$) and the output voltage starts to build up.

The transition from the higher frequency (f_2) to the lower frequency (f_1) is followed by a rapid drop in the output voltage of the rectifier (V_{out}) since the matching network (L_S) does not resonate with C_{in2} at f_1 and the voltage matching is compromised. The drop in the output voltage is sensed by the comparator which subsequently sets $SW = 1$ through the controller. The increase in the gate bias voltage of $M_{1,2}$ increases the input capacitance to C_1 so that it resonates with L_S at frequency f_2 and establishes the voltage matching. The negative edge-triggered flip-flop is connected in a divide-by-two mode to avoid the unnecessary transition of *SW* when the output voltage starts to grow.

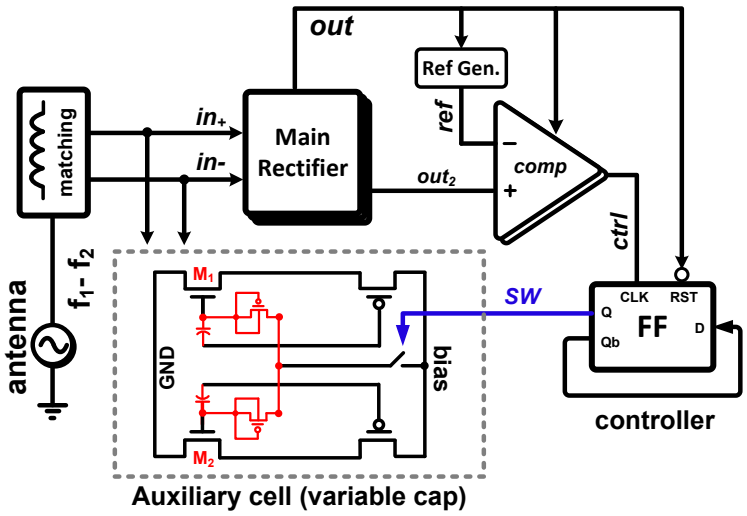


Figure 3.46: Block diagram of the proposed dual-band matching scheme.

The reference voltage of the comparator is generated by a band-gap reference generator. The bias voltage is extracted from the output of the floating auxiliary cell (refer to Section 3.3) and is fed to the gates of $M_{1,2}$ in a QFG fashion (refer to Section 3.4). Note that the value of bias voltage could be designed such that the input capacitance covers the dynamic range of C_{in} and provides a range of resonance frequencies. The comparator, reference generator and the flip-flop controller are supplied by the output of the main rectifier to enable a self-sufficient operation of the proposed matching scheme.

3.6.1 Simulation Results

A proof-of-concept prototype of the proposed dual-band rectifier is designed and simulated in a 0.13 μm CMOS technology. Two 20 nH inductors are used to match the 50 Ω source to the input capacitance of the rectifier. For a 50 kΩ load, Figure 3.47 shows the transient response of the proposed scheme for the source input amplitude of 40 mV (before matching) at two different input frequencies of 950 MHz and 2.4 GHz. As shown, the comparator triggers the control signal, *ctrl*, once out_2 falls below the reference voltage. The flip-flop turns on the switch signal (*SW*), upon sensing the falling edge of *ctrl* to switch the input capacitance to its higher value C_{in1} (mode 1). *SW* turns off at the next falling edge of *ctrl* to switch the rectenna back to mode-2.

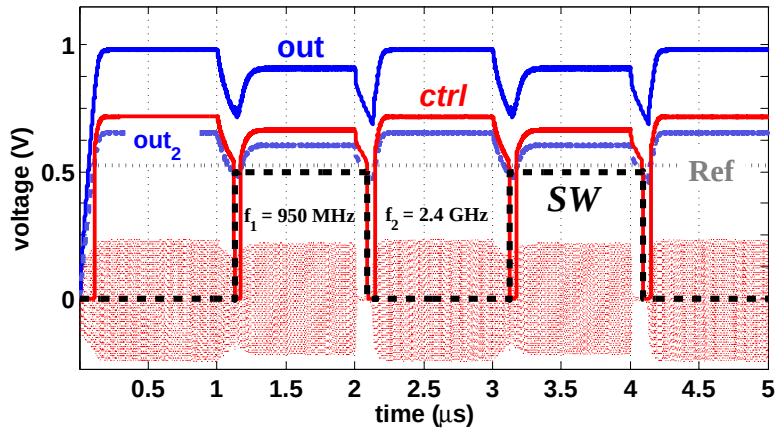


Figure 3.47: Transient response of the proposed matching scheme.

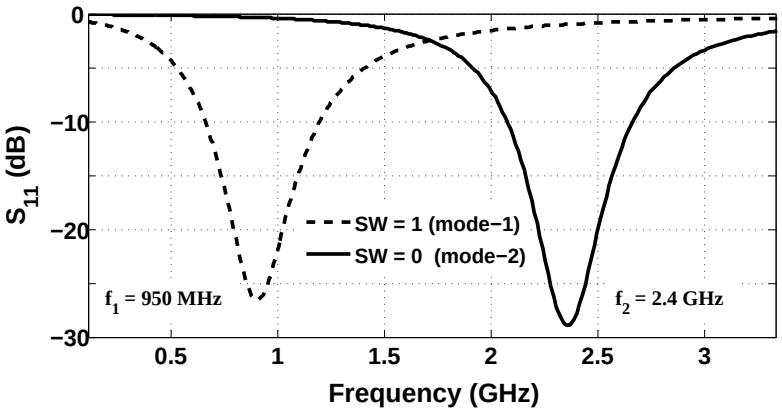


Figure 3.48: Frequency response of the proposed matching scheme.

Accounting for the power consumption of the comparator, band-gap reference generator and the flip-flop controller, the rectenna generates an output voltage of $\sim$1 V in mode-2 (f_{in} = 2.4 GHz) and achieves the PCE of 64% for an input amplitude of 40 mV. The output voltage and PCE in mode-1 (f_{in} = 950 MHz) are $\sim$0.9 V and 55%, respectively. The slight degradation in output voltage and PCE performance of the rectenna in mode-1 can be attributed to the larger portion of the input power being shunt to the ground due to the added input capacitance (through $M_{1,2}$). The auxiliary cell generates a bias voltage (V_{bias}) of $\sim$0.6 V. The simulated frequency response of the proposed matching scheme is shown in Figure 3.48.

3.7 Conclusion

In this chapter, three efficiency enhancement techniques applicable to UHF RFID rectifiers are presented. The proposed efficiency enhancement techniques improve the PCE of the rectifier when the input level is small and therefore, facilitate a longer communication distance and/or higher energy levels delivered to the tags circuitry.

The proposed switched rectifier archives a high PCE value for larger input levels (compared to the convectional rectifier) while the SC rectifier provides a high PCE for smaller input levels which corresponds to longer communication distances. The switched and SC rectifier are dependent on high-speed clock generators and rather bulky switched-capacitor network. Moreover, the SC rectifier requires an external voltage (power) source for the start-up and therefore, does not easily lend itself to passive implementation.

The AUX-boosted rectifier uses floating rectifier cells for the purpose of voltage-boost generation and is therefore, fully compatible with passive RFID requirements. However, a three-stage AUX-boosted rectifier requires six floating rectifier cells (two for each stage) and consequently twelve capacitors. Although as discussed in Section 3.3.1, the requirements for the auxiliary cells are relaxed, the imposed area overhead has to be taken has to be accounted for.

The QFG-boosted rectifier is the most attractive design among the proposed architectures in terms of area overhead and flexibility. The QFG structure allows direct access to the DC voltage level of the gate of switching transistors and can be used to dynamically adjust the PCE curve of the rectifier based on the application requirements.

Built upon the discussed efficiency enhancement techniques, a dual-band matching approach for the rectifier is presented. The proposed dual-band matching is based on dynamic modification of the input capacitance of the rectifier in response to variations of the input frequency. The proposed technique can be extended to a multi-band matching approach and/or to extend the bandwidth of the matching network for a single-band operation.

To study the performance of the proposed rectifiers in a practical application scenario, an ultra-low-power monitoring system for inductively-coupled

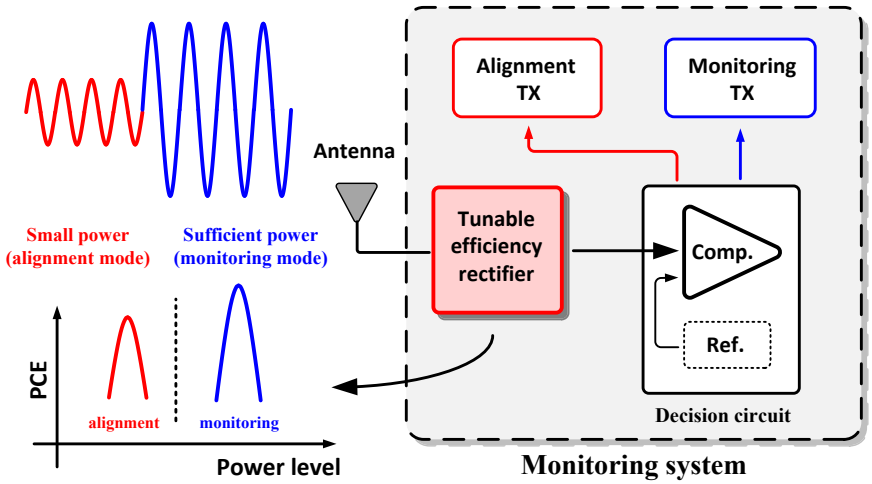


Figure 3.49: Schematic diagram of monitoring system.

biomedical implants is designed in [5, 8]. The monitoring system is equipped with an alignment mechanism. The alignment unit facilitates monitoring the received power by the tag's antenna in the proposed system. The received RF power by the antenna is rectified and the produced voltage is compared with an on-chip generated voltage. If the received power level is insufficient for proper operation of the main monitoring system, the tag transmits the appropriate signal to the reader, signifying the misalignment between the reader and the tag's antenna. Note that although in the alignment mode, the received power by the tag is insufficient to supply the monitoring system, the high efficiency rectifier provides enough energy for the the decision circuit and tag to transmit the misalignment signal. Upon receipt of the misalignment signal, the user can readjust the position of the external reader so as to deliver sufficient power to the system.

The entire system includes two transmitters, one low power transmitter for alignment mode and a more elaborate one for the monitoring mode. Also incorporated in the system is a decision circuit comprising of a comparator and a reference generator. The decision circuit activates each of the two transmitters based on the received power level.

Also crucial to this design is a rectifier which is capable of providing two optimal efficiency points, one for the alignment mode (low input power level) and one for the monitoring mode (sufficient input power level). The rectifier is optimized for the monitoring mode (i.e., high input power level). In the alignment mode when the tag receives small RF power and consequently small input voltage

is delivered to the rectifier input, floating voltage sources (in a fashion similar to the design presented in Section 3.4) are incorporated to boost the gate-drive voltage of the switches. During the monitoring mode, the decision circuit switches off the booster circuit (voltage sources) such that the rectifier operates at its optimal point. Figure 3.49 schematically shows the operation principles of the monitoring system.

The circuit blocks of the monitoring system are designed and simulated in a 0.13 μm CMOS technology. Details of the design are presented in [8].

To provide experimental results for a practical application scenario, an ultra-low-power integrated circuit is designed for a telemonitoring systems. The system comprises different building blocks including wireless power harvesting unit and a high efficiency rectifier, clock generator, capacitance-to-voltage converter and transmitter. Design techniques are developed to significantly reduce the power consumption of the system. The high efficiency rectifier supplies the entire monitoring circuitry. The monitoring system is capable of operating with an input level as low as $-$ 43.76 dBm. For a rectified voltage as low as 0.35 V, a sensitivity of 3.1 kHz/fF is achieved for the capacitance-to-voltage converter. This value is improved to 55.0 kHz/fF for a 1.0 V rectified voltage. Details of the design are presented in [8].

Chapter 4

Power Efficient Receive and Transmit Schemes

In this chapter, power efficient schemes for receive and transmit mode of wireless sensor nodes and RFID tags are discussed. In most of RFID applications, the tag needs to be wary of the incoming command from the reader. Therefore, a mechanism is required to guarantee the tag is constantly listening to the communication channel (even when no signal is being transmitted by the reader). the power consumed by the tag's receiver during such idle mode is practically wasted. Since the receiver contributes significantly to the overall power consumption of the tag, a method that reduces/eliminates such unnecessary power dissipation could be quite beneficial in an efficient implementation of tags. Wake-up radio concept as an asynchronous (event-based) scheme can significantly reduce the power consumption of the tags receiver during the idle mode and will be discussed in this chapter.

Typically, the power consumption of the transmitter unit is the biggest contribute to the overall power consumption of any wireless communication system. However, Passive RFID tags are generally incapable of accommodating a sophisticated transmitter due to their very tight power budget. Therefore, an alternative transmission method that reduces/eliminates the transmit mode power dissipation would be very desirable in the context of passive RFID tags. Backscattering method is an attractive approach for the transmission of signals

from passive RFID tags as it basically eliminates the need for a dedicated (active) transmitter. Backscattering scheme is discussed in this chapter in the context of telemonitoring systems for biomedical implants.

4.1 Proposed High-Sensitivity Fully Passive Wake-Up Radio

In power-limited consumer wireless devices such as biomedical implants, wireless sensor networks, wearable components, and Internet of things, energy saving is a critical design task. These devices are usually battery operated and have a radio transceiver that is typically their most power hungry block. Wake-up radio schemes can be used to achieve a reasonable balance among energy consumption, range, data receiving capabilities and response time.

4.1.1 Overview of Wake-up Radio Scheme

Wireless sensor networks (WSN) have been recognized as an enabling technology for a large variety of applications, including smart homes and cities, agriculture, transportation, health and fitness, entertainment, and structural health monitoring [90]. Strict energy constraints of battery-powered wireless sensor nodes necessitate energy-aware design at both software and hardware solutions. Reducing the RF transceiver power consumption of the WSN sensor nodes is of paramount importance, as the RF transceiver is one of the most power-hungry components of the WSN node [91].

Optimizing the power consumption of the wireless transceiver not only decreases the overall power consumption of the overall WSN system, but also provides opportunities to add more functionalities. In addition, since the battery size is typically an important portion of the overall node size, low-power circuits could enable smaller batteries and thus lead to further miniaturization required by many consumer applications such as wearable devices (smart watches and glasses), body area networks, and implantable devices [92].

To reduce the power consumption of the RF transceiver, several techniques have been proposed ([91]-[112]). All these techniques are trying to reduce or eliminate the power due to the idle listening of the transceiver. The idle state is

when the RF transceiver is monitoring the communication channel for an incoming message. Unfortunately, this monitoring can only happen if the radio is on and it is listening to the channel. The idle listening state consumes significant power [91]. Thus, significant efforts have been paid to alleviate this energy waste.

A common approach to reduce such idle-state energy is to use duty cycling. This technique consists of switching from listening mode to sleep mode to further minimize the transceiver power consumption [91, 93, 100]. However, despite the power reduction that this approach offers, it can limit the response time and agility of the nodes as the radios could be off (or in the sleep mode) for a relatively large portion of time. To exchange messages between two nodes, the receiver node must be awake when the sender initiates the communication. Thus, the receiver and the transmitter node radios need to be synchronized. Synchronization approaches can be classified into three main categories: synchronous, pseudo-asynchronous, or pure asynchronous communication schemes [94, 98, 101]. Duty cycling is in general a synchronous scheme, where the radio is woken up for a fixed or adaptive period of time to listen to any relevant incoming messages.

From a power consumption perspective, the asynchronous schemes are among the most efficient approaches, and an efficient realization of asynchronous communication is to use a wake-up radio receiver [113, 114]. Such a device is coupled with the main radio transceiver having the role of listening continuously to the transmission medium and waking up the main transceiver only when an incoming message is detected. Typically, the WUR consumes much less power than the main radio transceiver and thus it facilitates a significant power saving. An ultra-low-power realization of the WUR receiver can be achieved by reducing or eliminating the idle listening time [96].

There are a number of features that a WUR device has to support to improve its effectiveness. First, the power consumption of the WUR has to ideally be orders of magnitude lower than that of the main transceiver in the receiving mode. Other important features include high sensitivity, robustness to interferers, selectivity, and latency. Usually, sensitivity is the most sought after optimization goal with the ultimate aim to match the sensitivity of the main transceiver but at a much lower power. The sensitivity is directly related to the communication range: the higher the sensitivity (measured as the capability to sense the weakest signal in dBm), the

longer the range. However, improving the receiver sensitivity is typically translated to increased power consumption.

In this work, a fully passive low-cost wake-up receiver is presented that takes into account the abovementioned constraints and specifications. Specifically, the contributions of this work are as follows: The design and implementation of a wake-up radio which is fully passive. The WUR is capable to demodulate OOK messages and at the same time harvest energy to supply the rest of the wake up circuits. Furthermore, simulation and experimental validation of the proposed approach, in terms of power, sensitivity, and data rate are presented.

4.1.2 Related Work

Research activities on the use of WUR in wireless sensor networks to reduce power consumption have been prolific in recent years. WUR systems can be classified into three main categories: fully passive, semi-passive (or semi-active), and fully active circuits. The first group does not require an explicit power source as the circuit harvests energy from the environment (e.g., from the incident RF power). RF power harvesting circuits are typically realized using charge pump, Schottky diodes, and/or use CMOS technology. These circuits usually have a short range of communication. The communication range can be extended to a few tens of meters by using higher transmission power, or where applicable a larger antenna. Thus, they are more suitable for short-range applications and those that do not require any addressing mechanism. For example, they are used in biomedical implants, body area networks, near field communication and RFID. A major sub-block of a fully passive WUR is a passive rectifier with interrupt, e.g., [2, 95, 103–105]. Although the zero power consumption feature is attractive, in this work, we also focus on improving the range of communication.

Among the remaining two categories, namely, semi-active and fully active wake-up receivers, the semi-active approach is more commonly used. In this approach, only a minimal number of the receiver components are supplied by an explicit power source. Popular approaches for realisation of such circuits include using an envelope detector or ad-hoc ICs for the RF front-end and then using a comparator to generate an interrupt. Similar architectures for ultra-low-power

WURs for WSN devices are proposed to reduce the sensor node listening activities, and thus drastically decrease the overall network power consumption [106–109]. All these solutions use Schottky diodes for envelope detectors and a comparator. Also, these solutions use multi-stage rectifiers rather than one stage. For example, an elegant solution which consumes only 89 nW uses a CMOS custom rectifier and a comparator and achieves a sensitivity of $-$ 41 dBm [110].

Fully active solutions use active components both for the rectifier and the interrupt generator. For instance, a solution with a rectifier, wideband amplifier and the wake up signal recognition achieves a sensitivity of $-$ 47.2 dBm [110], however, similar to other fully active solutions, the power consumption is rather high (6 μW). As another example, an architecture which uses a low noise amplifier (LNA) in a fully-active solution achieves a sensitivity of $-$ 89 dBm [112]. The use of a LNA allows such a high sensitivity, however, at the cost of a high power consumption of few mW, which may offset the benefits of WURs.

A thorough survey of various wake-up schemes and their advantages over the wake-on (duty cycling) schemes is presented by Jelicic *et al.* [94]. It is shown that the WUR that does not support addressing [108], has an advantage over the other schemes due to its very low power consumption and low latency. However, an addressing mechanism is required to reduce the power consumption during network formation, and if the wake-up receiver can receive and process commands, the MAC data communication protocol can be optimized for low power consumption. There are two methods for implementing the addressing mechanism: a) custom circuit for addressing/address comparison [112] and b) using a generic microcontroller unit (MCU) [109]. The addressing methodology will have implications on the overall power budget and will influence the selectivity of the system. This emphasizes the importance of the capability of receiving data, which is considered in our proposed approach.

The system proposed in this work extends the state-of-the-art with respect to power consumption and data receiving capability. The design and implementation of a fully passive wake-up radio comprised of a CMOS rectifier and a comparator is presented which generates interrupt from a demodulated OOK signal which can be used for addressing.

4.1.3 Wake-Up Radio Concept

To communicate between two wireless nodes, the receiver node must be awake when the sender initiates the communication, a scheme which is referred as a rendezvous [113]. The receiver remaining awake even if it is not receiving any data is one of the main consumers of the power in a wireless radio communication system. This is why research efforts have been focused on reducing or eliminating the power consumption of idle listening via a number of novel hardware (e.g., WUR), software (e.g., MAC and routing algorithms) and duty cycle optimization approaches [97, 98].

There are three main classes of rendezvous schemes:

1. *Pure synchronous*: In this scheme, the node clocks are pre-synchronized such that the wake-up time of each node is known in advance. This scheme requires recurrent time synchronization that consumes considerable energy. Moreover, the nodes wake up even if there is no packet to transmit or receive, causing idle listening or overhearing.

2. *Pseudo-asynchronous (or cycled receiver)*: In this approach, source nodes wake up and emit a preamble signal that indicates the intention of the data transmission. The preamble time has to be set long enough to coincide with the wake-up schedule of the destination node (i.e., longer than its sleep time). In this scheme, time synchronization is not required, but nodes follow a duty cycle and consume considerable energy for preamble signalling.

3. *Pure asynchronous*: In this class, the sensor nodes are in deep sleep mode and can be woken up by their neighbours on demand with low-power wake-up receivers. Whenever a node intends to send a packet, it first wakes up the destination node with a wake-up message and then sends the packet. Therefore, wake-up receivers are a solution to the redundant energy consumption caused by rendezvous.

This work is focused on the pure asynchronous typology and its implementation by using a separate wake-up receiver to monitor the communication channel continuously, while the main radio is kept in the sleep mode during the times that it is not needed as schematically shown in Figure 4.1.

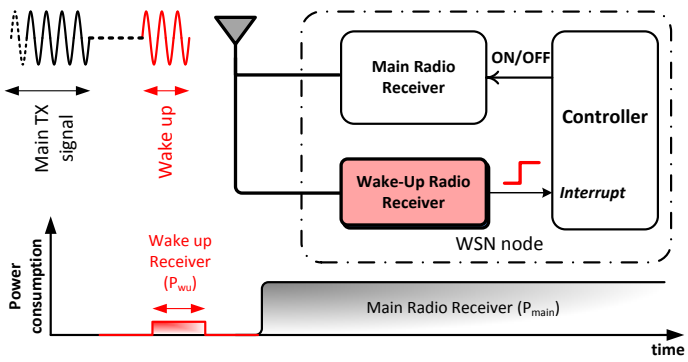


Figure 4.1: Generic block diagram of a wireless node with a separate wake up radio receiver [2].

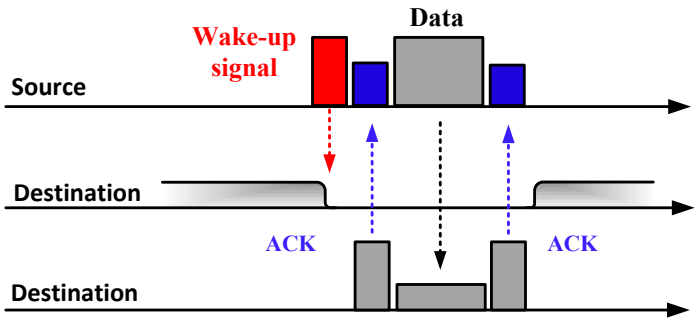


Figure 4.2: Asynchronous communication scheme using a wake up radio.

When a node wants to communicate, it sends a wake-up signal which is detected from the WUR to allow the central processing unit (CPU) to wake up the main radio to start the communication as shown in Figure 4.2.

The wake up message can contain, for example, the address of the destination node to wake up only the desired neighbour. This is an optional feature that depends on the design or the application requirements. The most important requirement of the wake-up radio is to have a low power consumption, usually in sub-μW or preferably few nano-watt range. Such low-power consumption allows the wake-up receiver to be continuously on, listening for the wake up signal while the main radio is switched off, achieving an overall power saving. Another important requirement of the WUR is its sensitivity which is typically measured in dBm. A more sensitive device is able to receive weaker signals, which means a longer transmission range can be supported. To cover most communication ranges

that are applicable in WSNs and RFID tags, a sensitivity of better than -20 dBm is desired. It is important to improve the sensitivity without increasing the power consumption of the receiver which is one of the main challenges in designing WURs. The WUR can use the same antenna, or use a different antenna. This depends on the frequency and the modulation used by the main radio transceiver. If the main transceiver is operating at the same frequency band as the WUR and it supports the WUR modulation format, then a single antenna can be used.

The design of the wake-up radio requires meticulous consideration of design issues in RF, analogue electronics, and digital and system design to carefully evaluate the following trade-offs:

- Wake-up range vs. energy consumption.
- Wake-up range vs. delay.
- Same-band vs. different-band wake-up radio.
- Addressing or without addressing.

As discussed in [95] which is one of the pioneering works on application of the wake-up radio concept in wireless sensor networks, the following design goals should be targeted for WURs:

- Low power consumption.
- High sensitivity.
- Resistance to interference.
- Fast wake-up.

The following subsections present design considerations of the proposed wake-up receiver which takes into account the above mentioned trade-offs and goals and a proof-of-concept implementation of the proposed wake-up receiver that confirms the performance of the proposed approach.

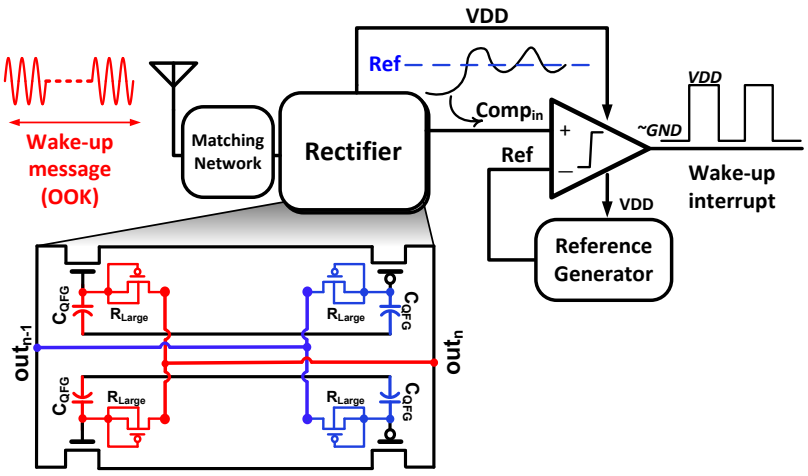


Figure 4.3: Block diagram of the proposed WUR front-end [2].

4.1.4 The Proposed Wake-Up Radio Architecture

As mentioned in Section 4.1.3, the WUR is expected to consume a negligible power compared to the main receiver, in particular, in the context of WSN nodes. The WUR is generally a very simple radio as it is primarily optimized for power efficiency rather than high data rate and spectral efficiency (which are expected from the main transceiver). As shown in Figure 4.3, a WUR front-end consists of an antenna (usually shared with the main transceiver), matching network, voltage multiplier (rectifier) and data slicer (comparator and the associated reference generator). Excluding the baseband processing circuitry and for a passive rectifier, the power consumption of the WUR front-end is limited to the power drawn from the main energy source (e.g., a battery) by the comparator and the reference generator.

Although owing to the relaxed performance requirements of the WUR, this power consumption is small, it should be accounted for in the overall power budget of the node as the WUR needs to be active all the time listening to the channel. Accordingly, a WUR scheme that does not load the node battery and extracts its energy from the wake-up signal itself is highly desired.

For this purpose, an RF to-DC converter (rectifier) is used to produce the envelope of the OOK signal (wake-up message) and at the same time, efficiently convert the RF carrier to a DC voltage to supply the comparator and the reference generator used in the WUR system. Besides ultra-low-power consumption, high

sensitivity (long communication range) is another desirable feature of a WUR. For electromagnetic coupling, the received power at the WUR antenna is a strong function of the communication distance (i.e., the distance between the transmitter and the receiver) and drops rapidly with the distance as expressed by Friis equation (i.e., Equation 1.2 provided in Section 1.3 and repeated here in the context of WUR):

$$P_{WUR} = EIRP_{TX} \cdot G_{ant} \cdot PCE_{rec} \cdot \left(\frac{\lambda}{4\pi d}\right)^2 \tag{4.1}$$

where P_{WUR} is the required received power for the proper operation of the WUR, $EIRP_{TX}$ is the isotropic power radiated by the transmitter, G_{ant} is the antenna gain, PCE_{rec} is the power conversion efficiency of the rectifier, λ is the wavelength of the transmitted RF signal, and d is the communication distance. Typically, these parameters are dictated by the application and geometry requirements, and thus to increase the operation distance for a fixed P_{WUR}, usually the only practical choice is to maximize PCE_{rec}.

For a fixed WUR antenna impedance (typically 50 Ω) and a reasonable communication distance (in the context of WSN), the induced voltage at the input of the rectifier (i.e., WUR antenna output) is normally too small to allow an efficient rectification. Therefore, in order to guarantee the proper operation of the rectifier and accordingly the entire WUR front-end, a mechanism is required to enhance the efficiency of the rectifier for small input levels. It should be noted that for a low-cost standard CMOS implementation which is greatly desired for wireless sensor nodes, the use of low turn-on voltage Schottky diodes to serve as the rectifier switches is not desired as they do not lend themselves to monolithic implementation. For the proof-of-concept experimental prototype in this work, a three stage differential-drive rectifier optimized for small input levels at 868 MHz input frequency is designed and implemented as shown in Figure 4.4. Note that a QFG-boosted version of this rectifier (refer to Section 3.4) is used for simulation purposes.

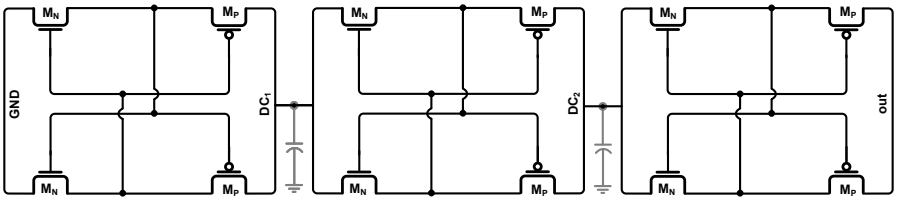


Figure 4.4: Schematic diagram of the three-stage differential rectifier.

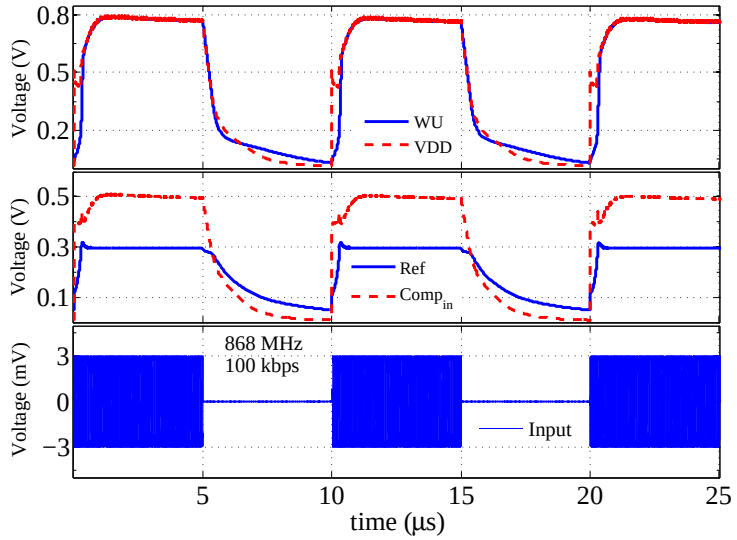


Figure 4.5: Transient simulation of wake-up radio front-end [2].

4.1.5 Simulation Results[1]

For simulations, a prototype WUR front-end is designed and simulated in 0.13 μm CMOS and operates at 868 MHz carrier frequency and 100 kbps data rate. A three-stage QFG biased differential rectifier receives -33 dBm (0.5 μW) from the antenna and delivers 0.25 μW DC power to drive the comparator and reference generator. As shown in Figure 4.5, for a 3 mV OOK signal, the rectifier generates $\sim$800 mV DC voltage. A fraction of this DC voltage, taken from the output of the second stage of the rectifier (namely Comp_{in} in Figure 4.3) is compared with the generated $\sim$300 mV reference. The comparator resolves within 5 μs and thus allows for a 100 kbps data rate.

[1] The material presented in this subsection is based on [2].

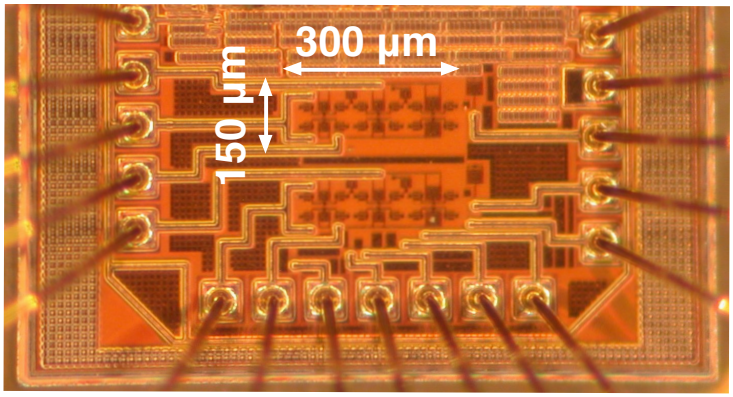


Figure 4.6: Micrograph of the three-stage rectifier.

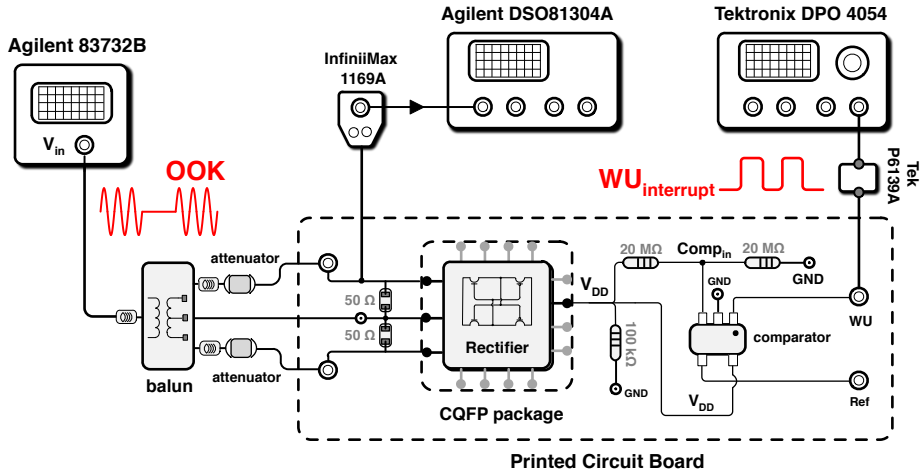


Figure 4.7: Block diagram of the measurement setup.

4.1.6 Experimental Results

For the proof-of-concept prototype, A three-stage differential-drive rectifier is designed and implemented in a 0.13 μm standard CMOS process. The entire rectifier occupies an area of 300 μm $\times$ 150 μm. The micrograph of the three-stage rectifier is shown in Figure 4.6. An external ultra-low-power comparator is used to detect the output of the rectifier [115]. The measurement setup is schematically shown in Figure 4.7.

A balun generates differential RF signals from a single-ended input and attenuators are used to match the output load of the balun. The rectifier drives a

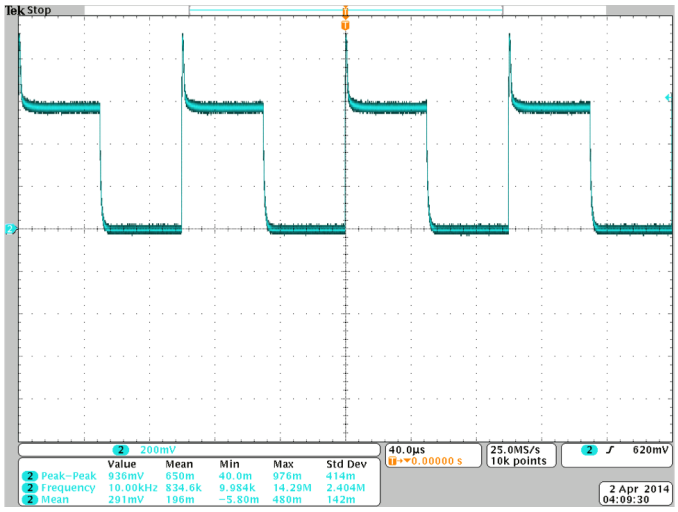


Figure 4.8: The rectifier output at 10kb/s data rate for a $-$ 21 dBm input power.

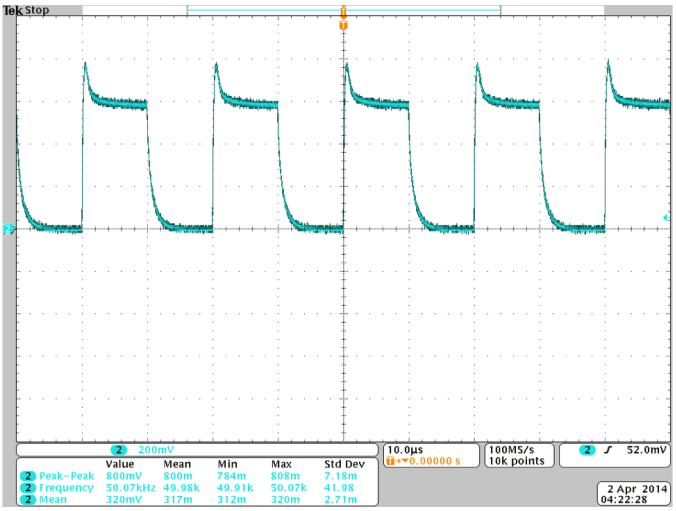
100 kΩ load that mimics the load of system. The input to the external comparator Comp_{in} (see Figure 4.3) is generated by a resistive divider. The reference voltage of the comparator is applied externally. Note that in a full on-chip design, this comparator input and the reference could be supplied by the output of an intermediate stage of the rectifier and a bandgap reference generator, respectively.

For a $-$ 21 dBm input power at 10 kb/s OOK data rate, Figure 4.8 shows the output of the rectifier for a 100 kΩ load. As shown in the figure, for a typically low data rate of 10 kb/s, the output of the rectifier resembles the envelope of the input OOK signal and therefore, could be directly applied to the succeeding base-band processing unit.

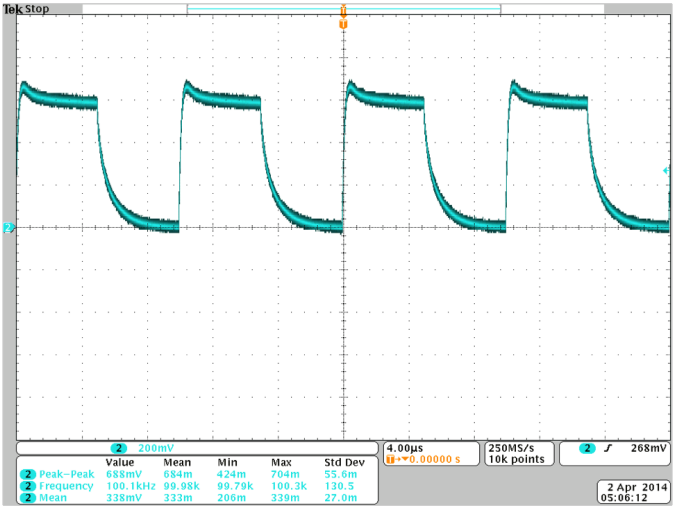
For a similar setup, the output of the rectifier is shown in Figure 4.9 for a 50 kb/s and 100 kb/s data rates. As shown in the figures, the output of the rectifier triggers at the appropriate rate to resemble the envelope of the detected data. Note that the output of the rectifier drives the 8 pF input capacitance of the test probe, which in turn affects the rising and falling times of the waveform.

Note that in this measurement setup, the input of the rectifier is not perfectly matched to the output of the RF signal generator. The input power is estimated by de-embedding the effect of reflection using the expression [78]:

$$\text{P}_{\text{in}} = \text{P}_{\text{sig}} \times |1 - \text{S}^2_{11,\text{diff}}| \tag{4.2}$$



(a)



(b)

Figure 4.9: The rectifier output at: (a) 50 kb/s and (b) 100 kb/s for a -21 dBm input power.

where, P_{sig} is the power delivered by the signal generator, P_{in} is the power received at the input of the rectifier and S_{11} is th reflection coefficient of the power delivery line.

Figure 4.10 shows the output of the entire WUR system ($WU_{interrupt}$ in Figure 4.7) for 10 kb/s, 50 kb/s and 100 kb/s OOK inputs. The input power is set to -20 dBm. As shown in the figure, the comparator output ($WU_{interrupt}$) is a good representation of the OOK signal envelope. The ultra-low-power comparator

Table 4.1: Performance summary of the proposed fully-passive WUR.

	frequency	data rate	power	sensitivity	Implementation
[116]	2.4 GHz	50 kbps	20 μW	-50 dBm	Simulation
[108]	433 MHz	5.5 kbps	270 nW	-51 dBm	Discrete
This work	868 MHz	100 kbps	0	-33 dBm	Simulation
This work	868 MHz	100 kbps	0	-21 dBm	Measurement

operates at a minimum supply voltage of 0.68 V. The average power consumption of the comparator at 0.68 V supply is measured to be 77 nW, 112 nW and 240 nW for 10 kb/s, 50 kb/s and 100 kb/s input rates, respectively.

For a load of 100 kΩ, the minimum input power for which the output of the rectifier is a valid detectable representation of the input is measured to be $-$ 26 dBm.

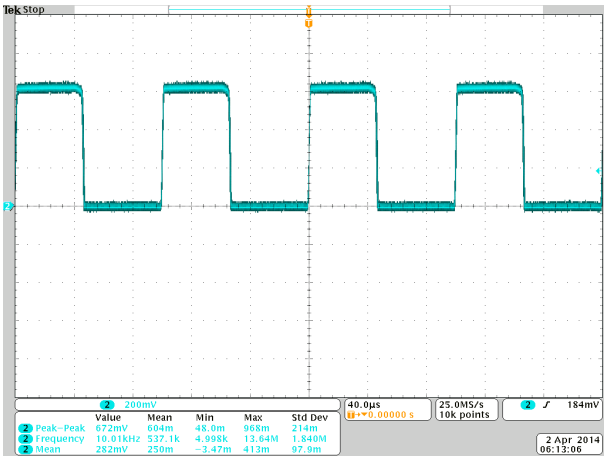
Figure 4.11 shows the rectifier output for $-$ 26 dBm input power. As shown in the figure, the output voltage of the rectifier is insufficient to drive the comparator (and potentially the succeeding baseband processing unit).

Table 4.1 provides a performance summary of the proposed WUR and comparison with the state-of-the-art designs in the similar range of operation frequency and data-rate.

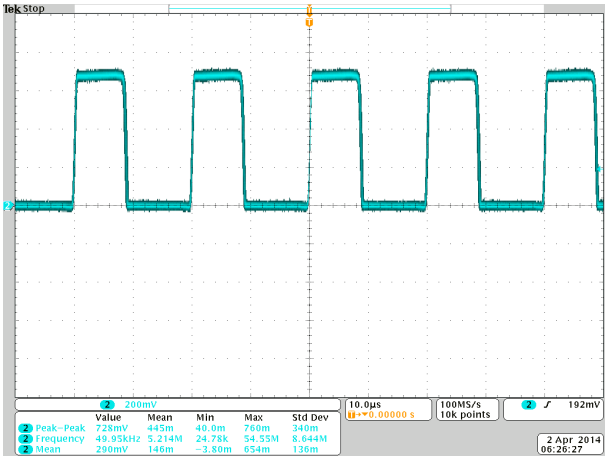
4.2 Feasibility Study of Backscattering For Telemonitoring[2]

Wake-up radio scheme as a power efficient approach in the receive mode was discussed in Section 4.1. In this section, backscattering method as a power efficient transmission scheme is studied. As discussed in Chapter 1, backscattering is commonly used for passive RFID tags at short communication distances. This scheme is specifically beneficial for telemonitoring systems in biomedical implants. In this work, the use of backscattering for telemonitoring of in-stent restenosis is investigated. Details of this study are provided in [8].

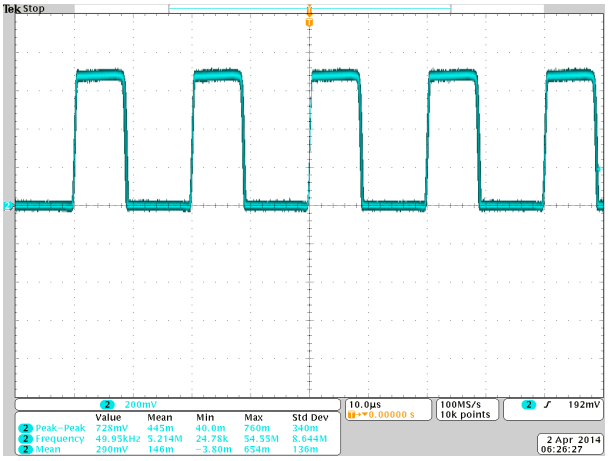
[2]The material presented in this section is based on [8].



(a)



(b)



(c)

Figure 4.10: Comparator output ($WUR_{interrupt}$) at (a) 10 kb/s, (b) 50 kb/s and (c) 100 kb/s.

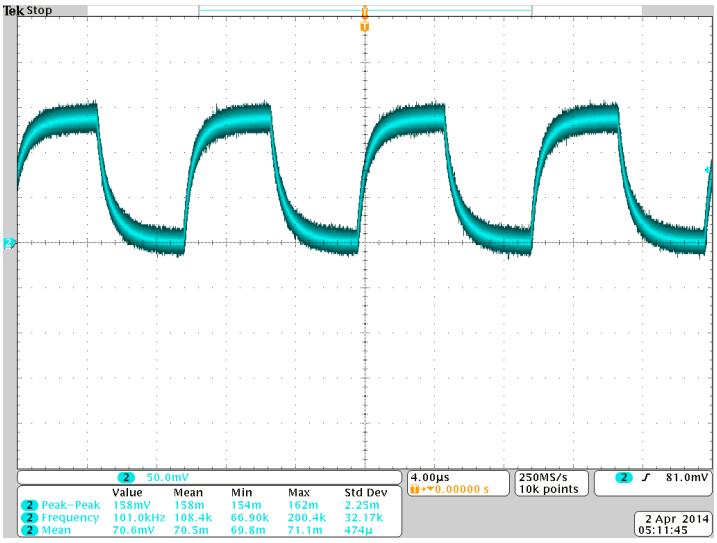


Figure 4.11: Rectifier output for an input power of − 26 dBm at 100 kb/s input data rate.

4.2.1 Overviwew of backscattering scheme for telemonitoring

Different techniques have been employed to wirelessly transmit power to biomedical implants. Inductive coupling (near field) [117–119], electromagnetic coupling (far field) [120, 121], and ultrasonic propagation [122] are among the most common means of wireless power delivery in the context of biomedical implants. The designs presented in [117–121] use active transmitters and those presented in [123–125] employ electromagnetic back-scattering approach and use a passive transmitter (relaxation oscillator, LC filter) in order to send the sensory data to the reader. The active approach requires significantly higher power which is not desirable in the context of wirelessly powered biomedical implants.

The focus of this work is passive backscattering telemonitoring scheme.

4.2.2 Telemonitoring of In-Stent Restenosis

Backscattering is a communication method in which the transmitted signal (incident power) is reflected back to the direction of the transmitter, thus alleviating the need for a dedicated transmitter [126, 127]. In the context of telemonitoring systems for biomedical implants (more specifically in-stent

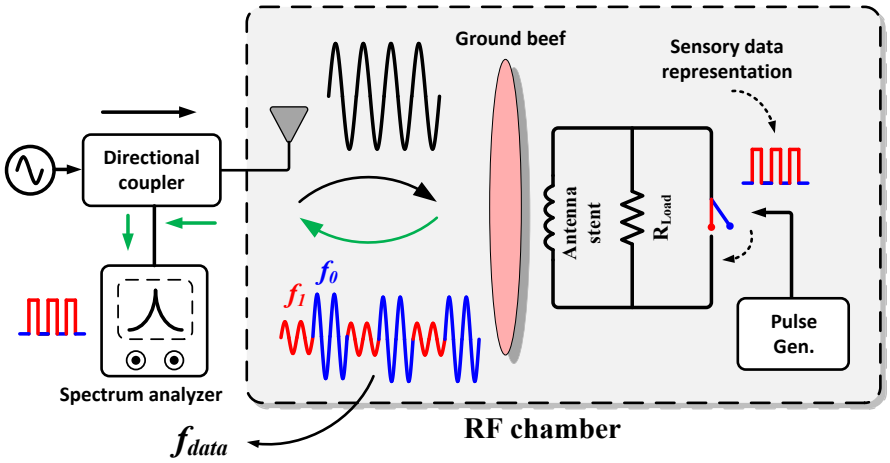


Figure 4.12: Schematic diagram of the test setup for backscattering feasibility study.

restenosis monitoring which is the focus of this work), the operation procedure is as follows: An external (and typically high power) reader transmits an RF carrier towards the implant's antenna. The transmitted radio waves penetrate the patient's body tissue and are harvested by the power harvesting unit of the implant to activate the tag IC. The implant's circuitry once activated, will process the captured sensory data (e.g., blood pressure captured through capacitive sensors). The processed data is then transmitted to the reader (interrogator) through backscattering method. The transmission of data through this method is achieved by modulating the impedance of the implants antenna. One way of modulating the impedance is by opening and closing the two terminals of the antenna by a switch which is controlled (turned on/off) by the data to be transmitted. The modulated impedance of the antenna is monitored and observed at the reader side, thus the data is detected. Backscattering method can be used with different modulation schemes such as amplitude shift keying, frequency shift keying and phase shift keying [126].

In this study, an antenna stent is used to serve as the implants antenna. A stent is a mesh tube device inserted in the blood passage to prevent flow constriction. In virtue of such structure, this device can be modified and used as an inductive coil and thus can serve as an antenna in the communication link [128].

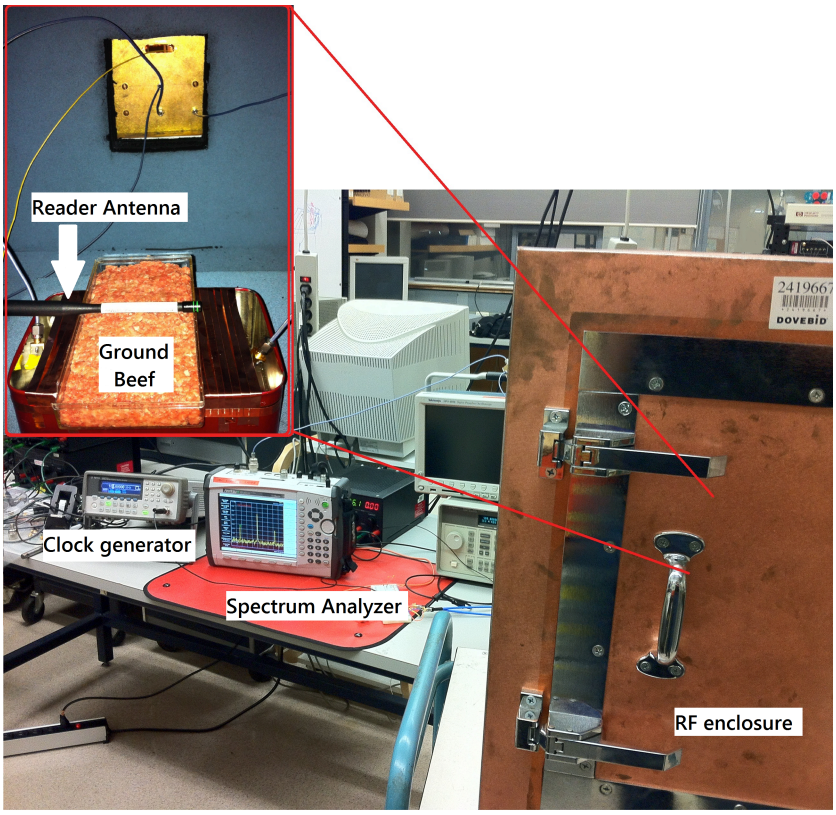


Figure 4.13: Backscattering-based measurement setup [8].

4.2.3 Experimental Results

To study the feasibility of backscattering approach for biomedical implants, a test setup is designed. The two terminals of the antenna (stent) are connected to a load resistance. A square-wave 100 kHz signal (to resemble the sensory data) drives an analog switch. The switch while closed, shorts the two terminals of the stent through bypassing the load resistance and when the switch is open, the two terminals of the stent are connected to the load. Therefore, the stent impedance is modulated with respect to the square-wave signal. The load resistance emulates the power (current) consumption of the implant in a practical scenario. RF carrier is transmitted to the antenna stent at 900 MHz. At the reader side, in order to detect the backscattered signal, a bidirectional coupler is used to isolate the received signal (backscattered by the antenna stent) and the transmitted signal (RF carrier). A spectrum analyzer is used to detect the backscattered signal in order to retrieve the data. The sensory data modulates the switching frequency in a *subcarrier modulation* fashion [9]. Note that antenna stent's impedance variation

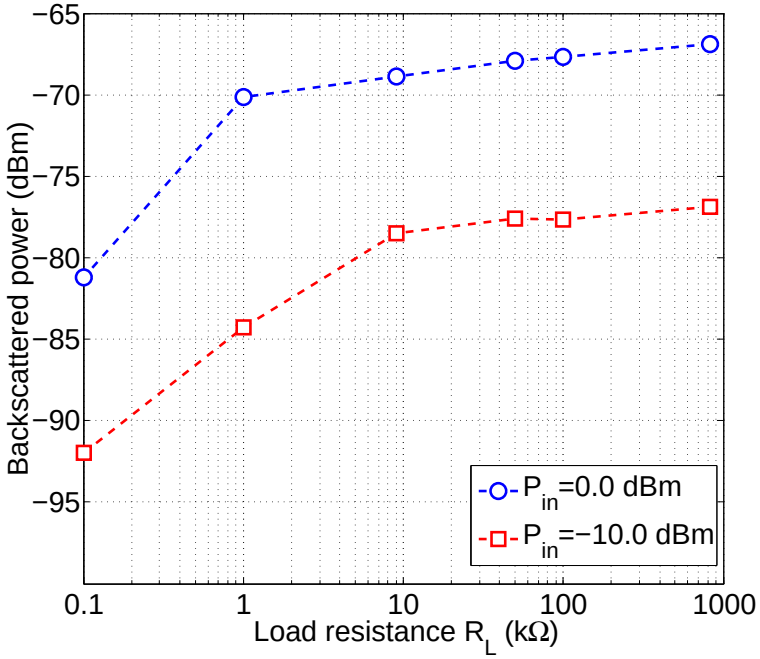


Figure 4.14: Measured backscattered power level versus different load values and input powers [8].

also modulates the amplitude of the backscattered signal, however, detection of such ASK signal requires a different receiver at the reader side (rather than an spectrum analyzer). Ground beef (applied in different thicknesses) is placed between the two antennas (reader and the implant) to mimic the real environment. The reader antenna, antenna stent and the analog switch are placed inside an RF shielded enclosure. Figure 4.12 ([8]) schematically shows the feasibility study setup while Figure 4.13 ([8]) shows the *in-vitro* experimental setup used for measurements.

The backscattered power level for different load values (R_{Load} in Figure 4.12) and for two transmitted powers of 0 dBm and $-$ 10 dBm are shown in Figure 4.13 [8]. Although the backscattered level is small, it is simply detectable by a typical reader. Also as demonstrated in Figure 4.13, a higher backscattered power level is received at the reader side, for larger load resistance values (smaller current consumption). This observation implies that a more power efficient implant circuitry leads to a more reliable backscattering communication. More details of this study are presented in [8].

4.3 Conclusion

In this chapter, a fully-passive wake-up radio capable of harvesting its entire required energy from the wake-up message is presented. The zero-power requirement of the proposed WUR can be exploited to prolong the lifetime of the energy source (battery) in wireless sensor nodes and active RFID tags. The proposed WUR is also useful in semi-passive and passive RFID tags by separating the data detection and power harvesting processes. Note that the settling requirements of the high-efficiency rectifier used for the WUR is different from that of the power harvesting unit. More specifically, the WUR rectifier performs as an OOK detector and its settling time has to comply with the designated data rate. However, the settling time of the rectifier used for power harvesting only needs to be compatible with power on/off cycles of the reader which is typically much slower than the data rate.

A high-efficiency rectifier for use in the WUR is designed and fabricated in a 0.13 μm CMOS technology. A discrete comparator and an external reference voltage are employed to complete the WUR architecture. The performance of the proposed WUR is verified through simulation and measurement results.

Also, the feasibility of backscattering technique in the context of biomedical implants is investigated. The impedance of an antenna stent is modulated by externally generated pulses (to emulate the sensory data) in an *in-vitro* measurement setup [8]. The measurement results verify the feasibility of backscattering technique to establish a communication between the implant's antenna (as the passive RFID tag or sensor node) and the reader, in biomedical applications.

Chapter 5

Power Efficient Clock Generator Circuit

As discussed in Chapter 1, the clock generator is an integral part most passive RFID tags and simple oscillators typically constitute the core of such clock generator circuits. Circuit-level design techniques to reduce the power consumption of the oscillators used in passive RFID tags is presented in this chapter.

5.1 Proposed Ultra-Low-Power Voltage-Controlled Ring Oscillator

The block diagram of a generic passive RFID tag (transponder) with an emphasis on the task of the clock generator (oscillator) is shown in Figure 5.1. The analog front-end is responsible for power harvesting and signal modulation/demodulation while the back-end processing unit controls data coding/decoding and memory/sensor access. As shown in the figure, a clock generator is an integral part of the processing unit. The EPCglobal™ Gen 2 mandates a minimum clock frequency of 1.92 MHz to guarantee a high-performance data transfer [129], [130]. To generate the required clock, a viable solution is to extract it from the incoming RF signal. However, such an approach requires a chain of dividers to convert the UHF carrier (860 MHz to 960 MHz) to the required baseband clock frequency [131]. The complexity and power overhead imposed by the dividers

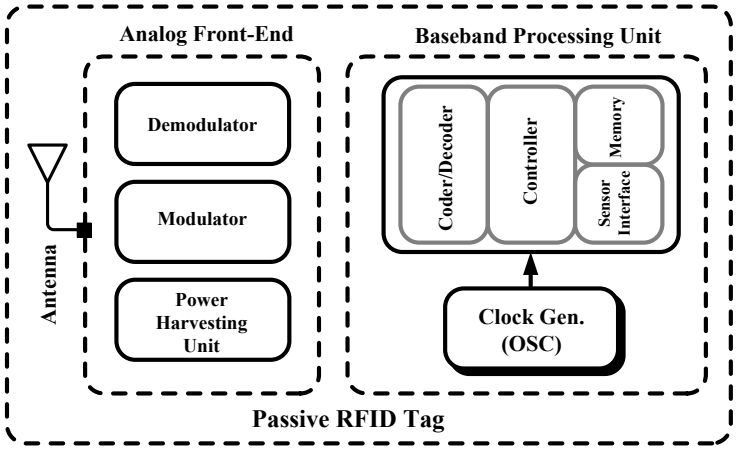


Figure 5.1: Block diagram of a generic passive RFID tag.

typically rules out this scheme in passive RFID tags, suggesting incorporation of a local (voltage-controlled) oscillator.

5.1.1 Overview of Low-Power Oscillators for Passive RFID tags

Passive LC oscillators and ring oscillator (RO)s are the two main categories of oscillators in CMOS technology. Unfortunately, the inductor as an essential component of LC oscillators does not simply lend itself to high-level of integration at UHF frequencies. LC oscillators also suffer from a limited frequency tuning range specifically in low-voltage applications where they have a narrow frequency tuning range [132]. In contrast, ring oscillators are not inherently dependent upon passive components (e.g., inductors) which is greatly desirable in the context of passive RFID tag design. Apart from silicon area considerations, low power consumption is also of paramount importance in passive tags considering their tight power budget. The local oscillator is a major contributor to the overall power consumption in passive tags. It is worth mentioning that passive UHF tags use backscattering method for the communication from the tag to the reader and theoretically do not allocate power for data transmission.

Extensive research has been conducted to address the power consumption of the ROs at a circuit-level perspective. Farzeen *et al.* [133], biases the delay cells

of a RO in the weak inversion region. The proposed oscillator achieves a power consumption of 24 nW for a 5.12 MHz oscillation frequency with 0.3 V power supply. In a work presented by Park *et al.* [134], a supply voltage of 0.3 V allows MOS transistors in the current-starved inverters to operate in subthreshold, near-threshold and above threshold regions. The proposed design consumes 95 nW for the entire RO-based temperature sensor while oscillating at 2 MHz to 8 MHz. Cilek *et al.* [131] controls the DC current of the current-starved inverters to minimize the power consumption. The proposed RO of [131] oscillates at 1.28 MHz and consumes 440 nW from a 0.9 V supply.

In this work, the gate-drive voltage of CMOS transistors in pseudo-differential (PD) delay cells are boosted through the use of QFG architecture [85]. The boosted gate-drive voltages facilitate oscillation with supply voltages as low as 90 mV which accordingly results in a low power consumption. The QFG technique practically imposes minimal area overhead and provides a secondary control mechanism over oscillation frequency.

5.1.2 Low-Power Ring Oscillator architecture

As mentioned in Section 5.1.1, low power consumption, small area, and tunability are major performance requirements of the local oscillator in the context of UHF passive RFID applications. Ring oscillators are a suitable candidate for such applications. The delay cells in a ring oscillator are implemented as either single-ended or differential inverting amplifiers [132]. While the single-ended ring-oscillator (SRO) requires an odd number of stages (minimum of three stages), its differential counterpart could be implemented with lower number of stages (minimum of two stages accommodating four current branches). The differential ring oscillator provides a better common-mode noise and supply rejection ratio and is capable of producing quadrature output signals. The power consumption of a ring oscillator is the summation of the static (P_S) and dynamic (P_D) power of the inverting amplifiers and is given by [135]:

$$\begin{aligned} P_{tot} &= P_S + P_D \\ &= I_{leak} \cdot V_{DD} + N \cdot f \cdot C_L \cdot V_{DD}^2 \end{aligned} \tag{5.1}$$

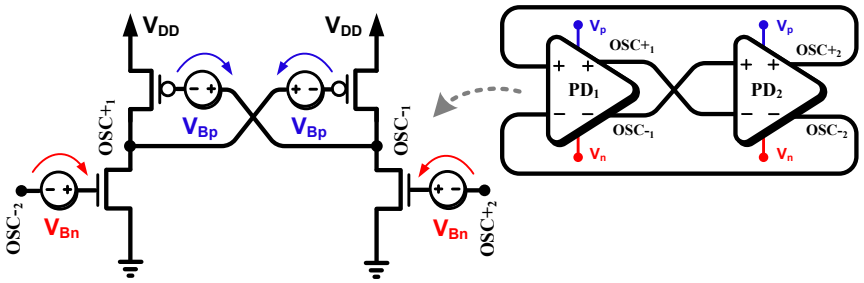


Figure 5.2: Schematic diagram of the proposed two-stage ring oscillator.

where I_{leak} is the leakage current of the inverting amplifier, V_{DD} is the supply voltage, N is the number of current branches, f is the frequency of oscillation and C_L is the capacitance of the output nodes. As suggested by Equation 5.1, for a given frequency of operation, the supply voltage, V_{DD}, and the number of stages, N, have to be minimized to reduce the power consumption.

In the proposed RO, a two-stage PD QFG architecture is employed. The PD architecture saves the voltage headroom for the tail transistor and allows oscillation with the minimum number of stages. To meet the *Barkhausen* criterion [136], each PD stage utilizes a local positive feedback in the form of two cross-coupled PMOS devices. The schematic diagram of the proposed QFG-biased PDRO is shown in Figure 5.2 where the gate-drive voltages of transistors are boosted through floating voltage sources. As shown in the figure, the floating voltage sources shift the AC input to the gates of transistors in a positive and negative direction for the PMOS and NMOS transistors, respectively. The boosted gate-drive voltages partially compensate the threshold voltage of transistors, facilitating oscillation with supply voltages smaller than the summation of the threshold voltages of the stacked transistors in the PD architecture. The floating voltage sources, $V_{Bp,n}$, can be efficiently implemented through the use of QFG architecture [85]. The QFG biasing scheme is shown in Figure 5.3a where the AC input (OSC) is coupled to the gate of the transistor through the capacitor C_{QFG} while the large resistor R_{large} weakly connects the gate to the desired DC bias voltages ($V_{n,p}$). As shown in Figure 5.3b, the effective value of the floating voltage sources are given by:

$$V_{Bn,p} = V_{n,p} - V_{DCin} \tag{5.2}$$

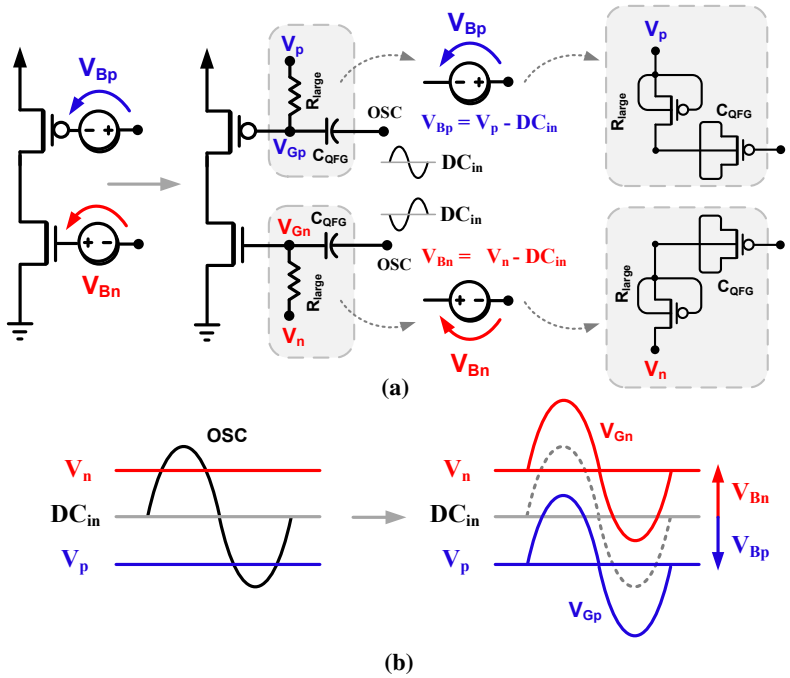


Figure 5.3: Implementation of the floating voltage sources through QFG architecture. (a) Schematic diagram of circuit-level implementation, (b) Schematic diagram of the boosted waveforms.

where V_{DCin} is the average voltage of the AC input, OSC, and is approximately equal to $V_{DD}/2$ for a rail-to-rail oscillator output. Boosting the gate-source voltages of the transistors as shown in Figure 5.3a virtually enhances the effective supply voltage by: $V_{Bn}+|V_{Bp}| = V_n - V_p$, which allows oscillation with smaller V_{DD}. Note that $V_p < V_{DCin}$ and accordingly, V_{Bp} is a negative voltage offset (see Figure 5.3a).

5.1.3 Design Considerations

As shown in Figure 5.3a, to save silicon area, the large resistor R_{large} can be implemented by the large leakage resistance of the reverse biased p-n junction of a PMOS in cut-off region [85]. The value of this resistor is not that critical as long as it is relatively large. The implementation of the coupling capacitor, C_{QFG}, requires further attention during the design process. The value of C_{QFG} affects the performance of the RO through two separate mechanisms as follows:

1. Coupling the AC signal, V_{OSC} to the gate terminals through C_{QFG} forms a

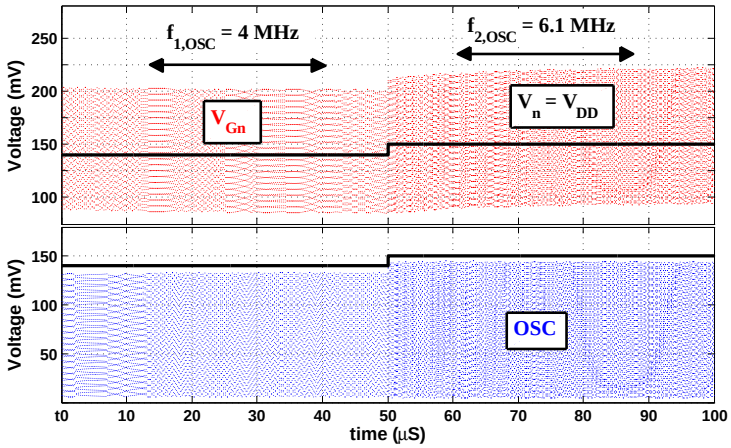


Figure 5.4: Transient settling behavior of the proposed QFG-biased VCRO.

capacitive divider at the gate of transistors and slightly attenuates the amplitude of the AC component. The QFG-coupled gate voltages $V_{Gn,p}$ are given by (see Figure 5.3a):

$$V_{Gn,p} = V_{OSC} \times \frac{C_{QFG}}{C_{QFG} + C_{Gn,p}} \tag{5.3}$$

where $C_{Gn,p}$ is the total parasitic capacitance seen at the gate of NMOS and PMOS transistors. Equation 5.3 suggests the use of a large coupling capacitor in order to fully exploit the available gate-drive voltage. However, aside from area considerations, an excessively large C_{QFG} increases the delay of the PD cells and accordingly reduces the oscillation frequency. Moreover, as shown in Equation 5.1, the large output capacitance C_L, increases the total power consumption of the oscillator. Therefore, for a fixed set of design parameters, there is an optimum range of C_{QFG} which results in a good performance in terms of oscillation frequency, silicon area, and power consumption.

2. The QFG architecture of Figure 5.3a forms a low-pass RC filter along the path from the bias node ($V_{n,p}$) to the gate of transistors. Thus, the DC value of the gate experiences a delay before fully settling to the desired value $V_{n,p}$. The settling behaviour is of particular importance if the RO is to be used as the VCO in a PLL. The time constant associated to this RC filter is given by:

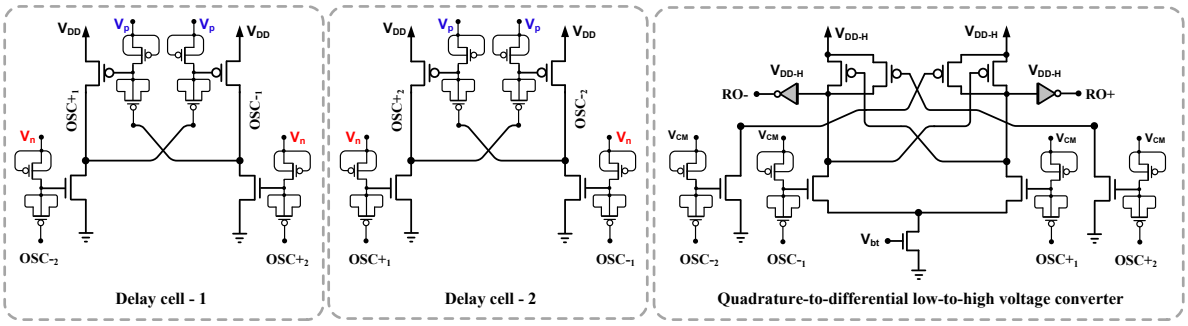


Figure 5.5: Schematic diagram of the proposed VCRO and voltage level converter.

$$\tau = R_{large} \times (C_{QFG} + C_{Gn,p}) \tag{5.4}$$

Equation 5.4 further highlights the significance of the C_{QFG} value. In the proposed QFG-biased RO, for a nominal frequency of 4 MHz, the associated time constant is 12 μs which yields to T_{settle} $\approx$50 μs. The 50 μs settling time corresponds to 200 cycles of the oscillator output at 4 MHz which satisfies the settling requirements of a VCO in PLL applications. As shown in Figure 5.3a, to save area, the coupling capacitors are implemented with MOSCAP devices.

To fully exploit the voltage levels already available in the circuit for the boosting purpose, V_n and V_p are connected to V_{DD} and ground, respectively, hence allowing a lower supply voltage value (see Figure 5.3a). Note that in view of Equation 5.2 and the discussion that followed, such a biasing scheme enhances the effective supply voltage by V_{DD} (i.e., $V_n - V_p = V_{DD} - 0$). Therefore, the supply voltage and accordingly V_n are used as the VCO control voltage while V_p is kept constant at zero. Figure 5.4 shows the transient waveform of $V_{G,n}$ in response to a step signal applied to the control voltage (V_{DD}=V_n). It is worth mentioning that both V_n and V_p could be used as a secondary frequency tuning knob. As discussed earlier, for a fixed V_{DD}, increasing V_n (V_p) virtually increases (decreases) the supply voltage and accordingly could be used to increase (decrease) the oscillation frequency.

The circuit-level diagram of the proposed VCRO is shown in Figure 5.5. As

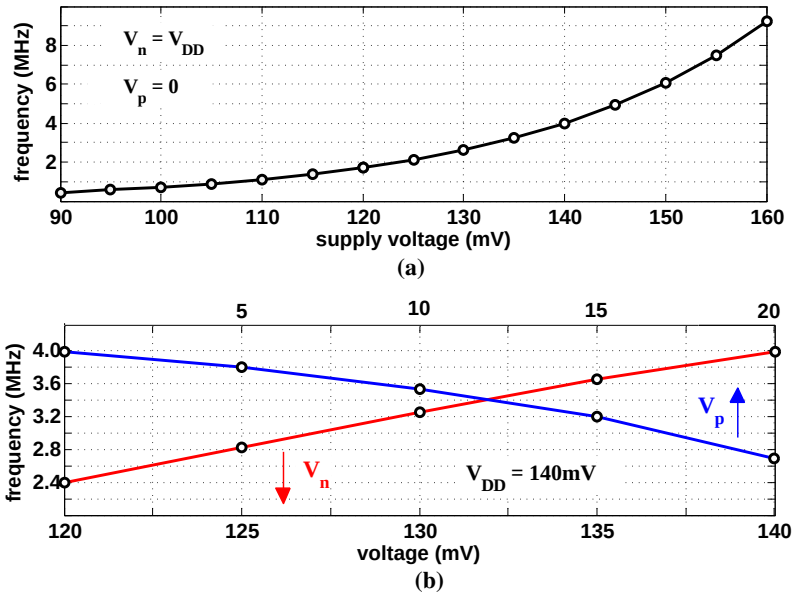


Figure 5.7: Oscillation frequency of the proposed VCRO. (a) As a function of V_{DD}, (b) As a function of V_n and V_p .

Table 5.1: Performance summary of the proposed low-power voltage-controlled ring-oscillator.

Reference	[131][a]	[133][b]	[137][a]	[138][a]	This work[c]
Technology	0.14 μm	90 nm	0.13 μm	0.13 μm	0.13 μm
Architecture	SRO	PDRO	Relaxation	Relaxation	PDRO
Frequency	1.28 MHz	5.12 MHz	5.65 MHz	2.52 MHz	4 MHz
Supply	900 mV	300 mV	600 mV	800 mV	140 mV
Power	440 nW	24 nW	720 nW	320 nW	3.6 nW

[a] Measurement results. [b] Simulation results.
[c] Post-layout simulation results.

shown in the figure, to interface the output of the VCRO with a succeeding circuitry that potentially uses a higher supply voltage, a quadrature-to-differential low-to-high voltage converter is proposed. The common-mode voltage of the input devices in the proposed converter is boosted through the use of QFG technique. The two output inverter buffers produce 50% duty-cycle fully differential outputs with a voltage swing of 0 to $V_{DD,H}$ from the low-voltage quadrature inputs. Note that, the capacitive loading effect of the converter slightly reduces the oscillation frequency and thus has to be accounted for in the design of the VCRO.

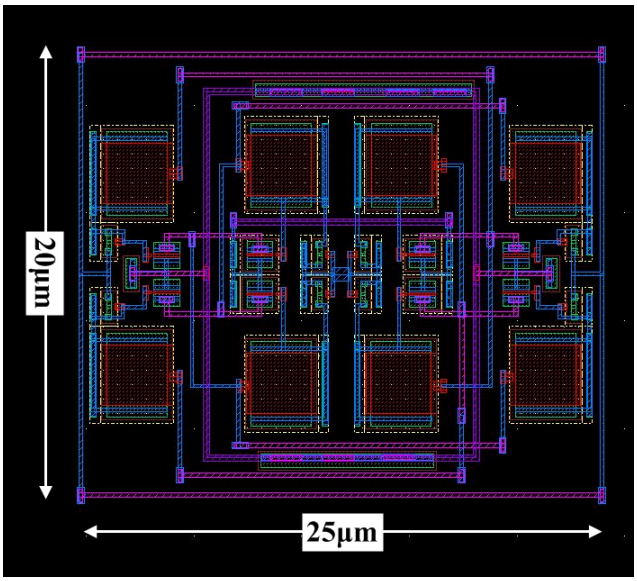


Figure 5.8: Layout view of the proposed VCRO.

5.1.4 Post-Layout Simulation Results

A proof-of-concept prototype of the proposed VCRO is designed and laid out in 0.13 μm CMOS technology. For a supply voltage in the range of 90 mV to 160 mV, the input and load transistors in the delay cells operate in weak to moderate inversion regions and are sized to minimize the power consumption. PMOS transistors in cut-off region are used to implement R_{Large} and MOSCAP devices are used for C_{QFG}. Figure 5.7a shows the oscillation frequency as a function of the supply voltage, while V_n is tied to V_{DD} (i.e., $V_n = V_{DD}$) and V_p is connected to ground (i.e., $V_p = 0$). As shown in the figure, an oscillation frequency (f_{OSC}) of 4 MHz is obtained for a 140 mV supply voltage. f_{OSC} spans a range of 450 kHz to 9.2 MHz for a V_{DD} variation of 90 mV to 160 mV. The power consumption of the VCRO for this range extends from 0.24 nW to 9.8 nW, with 3.6 nW for the nominal oscillation frequency of 4 MHz. Figure 5.7b shows the frequency as a function of V_n and V_p. For a fixed V_{DD} of 140mV, increasing V_n from 120mV to 140mV increases f_{OSC} from 2.4 MHz to 4 MHz while increasing V_p from 0 to 20 mV decreases f_{OSC} from 4 MHz to 2.7 MHz. For a V_{DDH}=0.6 V, the proposed low-to-high voltage converter consumes a power of 320 nW to generate a rail-to-rail differential clock (RO$\pm$) at 4 MHz frequency from the

quadrature inputs (0 mV-to-140 mV swing $OSC_{\pm 1,2}$) while V_{bt}=200 mV and V_{CM}=400 mV (see Figure 5.5).

The layout view of the proposed VCRO core is shown Figure 5.8. The proposed VCRO occupies an area of 500 μm^2 (25 μm$\times$20 μm) while only the first three metal layers (in a 0.13μm CMOS technology) are used for routing.

Table 5.1 provides a performance summary of the proposed VCRO and compares it with the state-of-the-art VCOs in the similar range of oscillation frequency.

5.2 Conclusion

An ultra-low-power VCRO is presented in this chapter to be used as the core of the clock generation circuitry in passive RFID tags. The proposed VCRO relies on QFG architecture to allow a low voltage operation and consequently, low power consumption. The VCRO uses MOSCAPs for the QFG structure to save layout area and is capable of accommodating two frequency control knobs through creating a separate access to the gates of the NMOS and PMOS transistors in the PD cells.

Chapter 6

Conclusion and Future Work

Passive RFID tags offer several key advantages over their active counterparts and conventional identification systems. The most significant advantages brought by such tags could be summarized as low cost, small form factor and maintenance-free operation. In virtue of these advantages, passive tags are widely used in numerous applications and the demand for such identification systems is expected to grow at a rapid pace in the near future.

The absence of a dedicated energy source for the passive tags calls for intelligent design techniques to enable the tag's circuitry to cope with the very tight power budget. Moreover, area efficiency is another crucial criteria to be met by the passive tags circuitry in order to guarantee a low cost implementation of the entire system.

The focus of this work is on the design of efficient data and power converter circuits for use in passive RFID applications. Different building blocks of a passive RFID tag are designed with an emphasis on area and power efficiency mainly at a circuit level perspective.

6.1 Low-Power and Area-Efficient SAR ADC

An ultra-low-power and area-efcient SAR ADC is presented in Section 2.2. The ADC achieves a low power performance through using two ultra-low-power unity gain buffers. The area is also significantly reduced by eliminating the need for the

conventional capacitive DAC array. The entire ADC only consumes 290 nW and achieves a FoM of 48 fJ/conversion step which makes it specifically attractive to serve as the core of the sensor interface in sensor-enabled passive RFID tags [6].

The proposed SAR ADC presented in Section 2.2 demonstrates a good performance in terms of power consumption and area. However, there are possibilities to enhance its performance by means of some supplementary amendments summarized as follows:

A *Buffers Slew Rate and Gain Enhancement*

Performance of an ADC is evaluated by means of its FoM as:

$$\mathrm{FoM} = \frac{\mathrm{P}}{2^{\mathrm{ENOB}} \cdot \mathrm{f_{sample}}} \tag{6.1}$$

where P is the power consumption, ENOB is the effective number of bits and $\mathrm{f_{sample}}$ is the sampling frequency. Therefore, for a given power consumption, to improve the FoM, ENOB (as a function of the gain of the buffers), and/or $\mathrm{f_{sample}}$, (as a function of the speed of the buffers) has to increase. Thus, a feasible option is employing a buffer/amplifier with a higher gain/speed and little extra power consumption.

B *Comparator Offset Cancelation*

To mitigate FoM degradation as a result of device mismatch in the buffers/comparator and capacitor mismatch in the DAC, offset/mismatch cancelation mechanisms are required. The effect of the extra power consumption imposed by offset/mismatch cancelation circuitries on the ADC FoM is overcompensated by the increased ENOB as suggested by Equation 6.1.

C *Rate-Resolution Scalability*

Due to the varying nature of the input signal, sampling rate and resolution scalability is highly desired in RFID-based sensor network applications. Scalability allows for further power conservation when the performance and speed demands are not high. This valuable feature can be achieved in the proposed scheme by means of clock/power-gating and asynchronous bit-decision timing [39].

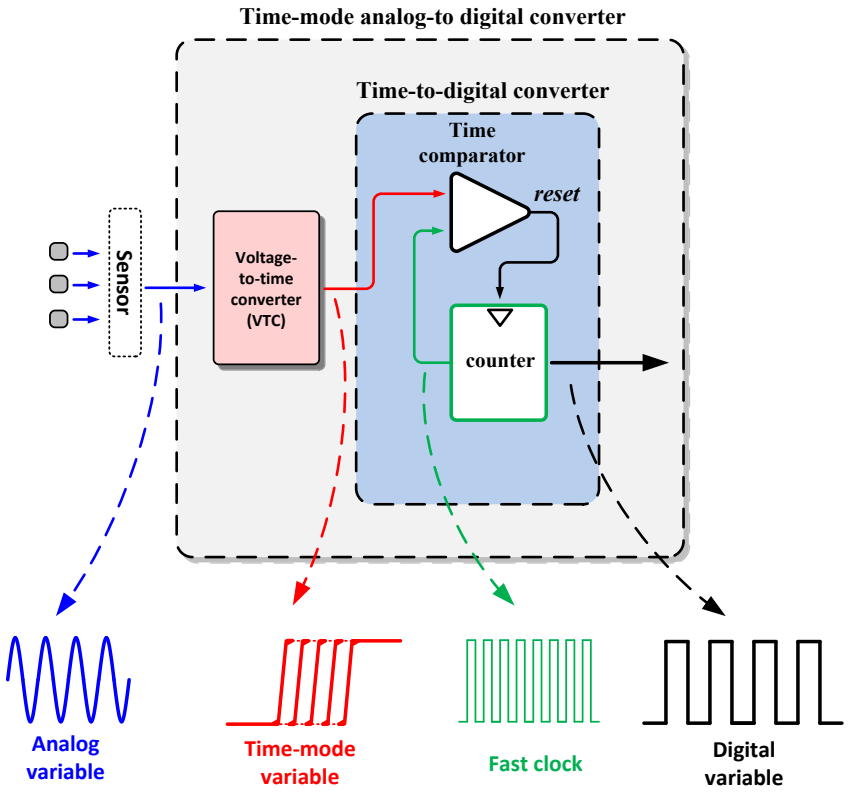


Figure 6.1: Schematic diagram of a time-mode ADC.

6.2 Wide Input Range voltage-to-Time Converter

A highly-linear wide input range VTC is presented in Section 2.4. VTC is a key building block in time-mode signal processing systems. Time-mode systems transfer the processing load from analog domain into time/digital domain. Therefore, such systems are very desirable in passive RFID tags due to their intrinsic low power consumption and ease of integration.

Wide input range and high linearity are among the most critical specifications of a VTC block. In the proposed VTC, high-linearity is achieved through re-ordering the charge and discharge cycles in conventional current-starved VTCs. also wide input range is obtained through the use of the proposed linear voltage-to-current converter.

The proposed VTC provides a good performance in terms of input range and linearity and is suitable to operate as the interface for the time-mode signal

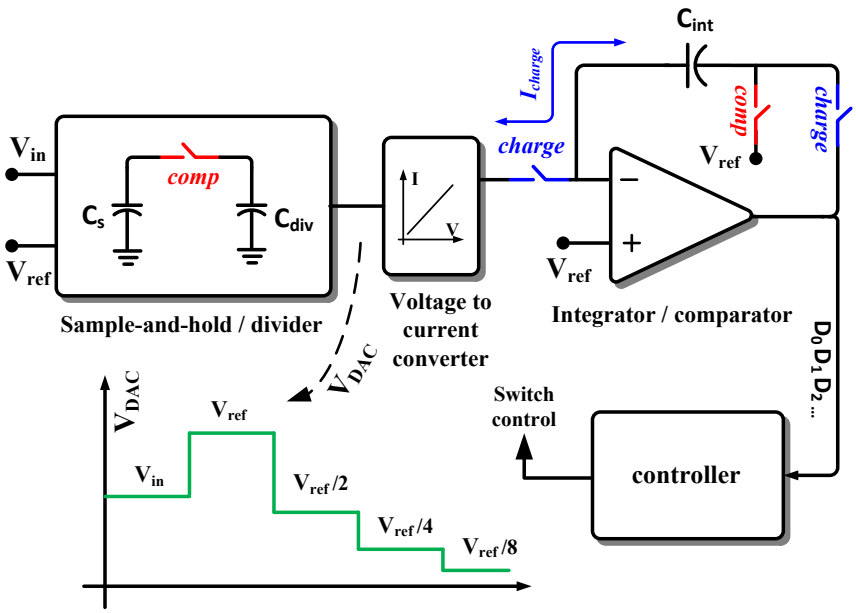


Figure 6.2: Schematic diagram of the current-based SAR ADC.

processing system. A time-mode analog-to-digital converter is TMSP system which is of particular interest in the context of passive RFID tags. As a future research track, the other building blocks of such an ADC namely a time comparator and a high-speed counter can be designed and assembled with the proposed VTC to develop a complete system [21, 49]. The diagram of the time-mode analog-to-digital converter is schematically shown in Figure 6.1

As another future work track, a current-based SAR ADC can be designed using the techniques developed in the design of the linear VTC Section 2.4. Such an ADC incorporates a sample-and-hold/divider, a linear voltage-to-current converter, an integrator/comparator and the control unit as shown in Figure 6.2. Initially the input voltage is sampled by the sample-and-hold block. The voltage-to-current converter (similar to the one proposed in Section 2.4) produces the appropriate current and charges the integration capacitor, C_{int}, during the charge phase. The voltage on C_s (i.e., V_{in}) is compared with the reference voltage, V_{ref}, and the MSB (i.e., D_0) is resolved. During the next charge cycle, the voltage-to-current converter driven by the sample-and-hold/divider (which is already charged with V_{ref} in the preceding comparison cycle) adds/subtracts V_{ref} to/from the voltage on C_s (i.e., V_{in} at this point) depending on the previous bit B_0. More specifically, If $B_0 = 0$,

V_{ref} is added to and if $B_0 = 1$, V_{ref} is subtracted from V_{Cint}. The resulted voltage is compared with V_{ref} and the next bit is decided. From this point on, the sample-and-hold/divider divides its voltage by two at each comparison cycle to have the appropriate DAC voltage ready for the next charge cycle. In the third charge cycle, $V_{ref}/2$ is added/subtarcted to/from V_{Cint} (depending on the value previous bit) and the resulted voltage is compared with V_{ref} to resolve the next bit. This procedure is repeated until all the bits are decided.

The amplifier operates as a unity-gain buffer during the integration phase (charge cycle) and therefore, stabilizes the inverting input voltage at a value close to V_{ref}. Such an approach comes with a valuable advantage: the drain voltage of the current mirror transistors ($M_{m1,2}$ in Figure 2.19) remains constant during the charge cycle which results in an accurate current copying. The feedback loop is opened during the comparison cycle and the amplifier performs as a comparator, comparing V_{Cint} with V_{ref}. Based on the previous bit value, the controller decides wether C_{int} is to be charged or discharged during each charge cycle and generates the appropriate switching signals.

The current-based SAR ADC eliminates the need for the bulky capacitive DAC and operates with only three capacitors (two for the sample-and-hold/divider and one for integration). To decrease the power consumption, the current levels (in the voltage-to-current converter) can be chosen arbitrarily small (i.e., as small as other design parameters such as the size of the integration capacitor permit).

6.3 Efficiency Enhancement Techniques for Rectifiers

Three efficiency enhancement techniques for CMOS differential rectifiers compatible with UHF passive RFID applications are presented in Section 3.2, Section 3.3 and Section 3.4. For small input levels, through proper boosting schemes, the gate-drive voltage of switches are biased at a level close to the optimal value, therefore, higher efficiencies are achieved for smaller input levels which in turn facilitate longer communication distance for RFID tags. PCE of UHF differential rectifiers are analyzed as a function of average forward-to-reverse current ratio in the switches. Based upon the analysis, boosting techniques are presented and studied in terms of power and area overhead and

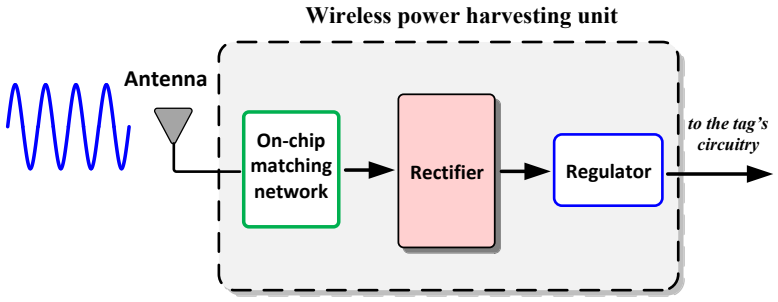


Figure 6.3: Schematic diagram of the wireless power harvesting unit.

design guidelines were provided. Post layout simulation results confirm the validity of the proposed techniques and high efficiencies were obtained at small input voltages.

For the proposed switched-rectifier of Section 3.2, two prototype three-stage CMOS RF-to-DC converters for UHF RFID tags are designed and laid out in 0.13 μm CMOS technology. Compared to conventional rectiers, both structures provide high power conversion efciency and low voltage operation capability. To enhance the differential rectier PCE, a new switching scheme is proposed that simultaneously reduces the effective turn-on voltage and leakage current of switch transistors. A simple clock generator is used to provide the appropriate clock signals required for the switching. The proposed scheme is then improved in terms of operation voltage range by applying an external voltage booster. Through the use of a floating voltage source capable of swapping its terminals, the gate of charge transfer switches are dynamically biased to alleviate the drawbacks associated with static biasing scheme. Note that in start-up phase, both structures rely on a power source for the purpose of clock and boost generation which can be supplied through an on-board battery in semi-passive tags. In passive RFID application, an auxiliary rectifier cell has to be incorporated in order to supply the required energy in start-up phase. The auxiliary rectifier can then be switched off when the output of the main rectifier reaches the desired value after which the main rectifier can continue its operation in a self-sufficient manner [7].

To remedy the requirement for an external power source during the start-up phase, the enhanced efficiency rectifier of Section 3.3 is presented. For this rectifier, A high PCE for small input voltages is achieved by boosting the gate

voltage of the switching transistors through a chain of auxiliary floating rectier cells. The proposed circuitry has a minimal power overhead and thus is suitable for passive UHF RFID applications. A prototype three-stage rectier is designed in a 0.13μm standard CMOS technology and post-layout simulation results show the capability of the proposed scheme in improving the efciency for small input voltage levels [4].

As a design approach to deliver a high efficiency over a wide range of inputs, a dynamic biasing scheme is proposed in Section 3.4. This extended high-PCE range is obtained by dynamically biasing of the gate of switches through a QFG architecture. The dynamic bias voltages are generated by a chain of voltage reference generators. The proposed scheme could also be used to improve the performance of the rectifier for very small input voltages, i.e., below the threshold voltage of transistors. Post-layout simulation results confirm the validity of the approach. Compared to conventional rectifiers, a proof-of-concept example has double the input range over which the PCE is more than 60% [3].

The proposed efficiency enhancement techniques provide a high PCE for small input levels and are capable of increasing the communication range. As a future research track, the proposed rectifiers can be assembled with practical antennas, on-chip matching networks and potentially a voltage regulator block to constitute a complete power harvesting unit. The diagram of such a power harvesting unit is schematically shown in Figure 6.3

6.4 Dual-Band Matching Scheme

A rectifier with a dual band matching circuit is a very attractive in the context of RFID tags. Such a rectifier facilitates energy harvesting at two distinct frequency bands and therefore opens up possibilities for numerous applications. In Section 3.6, through exploiting the techniques developed to enhance the efficiency of UHF rectifiers, a dual-band matching scheme is implemented to enable wireless power delivery with close to optimum PCE at two different frequencies. The separation between the two frequencies could be adjusted (within the range of the input capacitance variations) through proper design of the bias voltage circuit. The proposed matching technique facilitates on-chip matching and operates in a

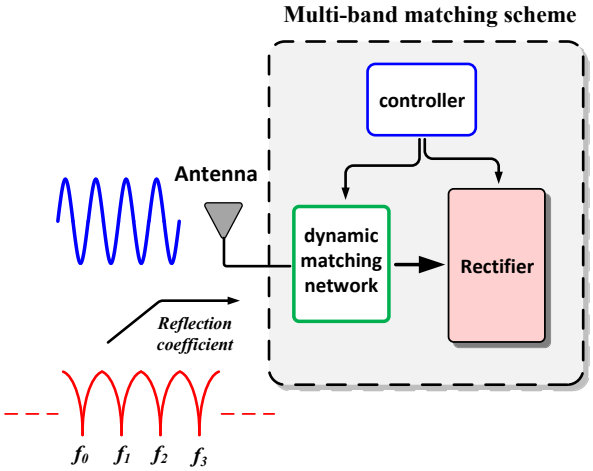


Figure 6.4: Schematic diagram of the multi-band matching scheme.

self-sufficient manner.

As a future work, a multi-band matching scheme can be designed to accommodate all or most of the RFID frequency bands. Since different ISM bands are positioned significantly far away in the frequency spectrum, such an scheme requires a sophisticated dynamic impedance controller. Along with dynamically controlling the input capacitance of the tag (rectifier), design techniques are required to also modulate the input inductance of the tag (matching network) to cover the wide dynamic range of input frequencies. The diagram of such a multi-band matching scheme is schematically shown in Figure 6.4

6.5 Fully Passive Wake-Up Radio

Wake-up radio scheme provides a significant power saving during the idle receive mode of tag's operation while the tag's receiver needs to constantly monitor the channel for a command signal from the reader. However, a successful realization of this method is greatly dependent on the power consumption of the wake-up radio. In Section 4.1, a fully passive wake-up radio for RFID tags and wireless sensor nodes is presented. Using a high-efficiency differential rectifier, the WUR front-end harvests its entire required energy from the wake-up signal without loading the main power source of the node. Detection for a $-$ 21 dBm input signal at 100 kb/s data rate is achieved at the output of the external ultra-low power comparator. The minimum input power for which the rectifier generates a

detectable DC output is measured to be $-$ 26 dBm. The WUR could be optimized for different carrier frequencies and data rates. Higher sensitivities could be achieved by further reducing the power consumption of the comparator and the reference generator through a fully integrated implementation and also by incorporating efficiency enhancement techniques for the rectifier [2].

As a future work, the proposed fully-passive wake-up radio can be improved in terms of sensitivity by means of enhancing the efficiency of the rectifier, using a detector (comparator and reference generator) with lower power consumption and incorporating a proper matching network. The implemented WUR can be tested in a field study under different signal transmission scenarios in a real environment.

6.6 Study of Backscattering for Telemonitoring

Backscattering is a power efficient scheme during the transmit mode of the tag as it alleviates the need for a power hungry dedicated transmitter. This scheme is widely used in passive RFID tags used in short range communication scenarios. To study the feasibility of backscattering for biomedical implants, a measurement setup to mimic the real environment is designed. The experimental results obtained form the measurements, confirm the feasibility of backscattering for telemonitoing in the context of biomedical implants. Details of this study are provided in [8].

As a future research, the backscattering scheme for biomedical implants can be tested in an *in-vivo* fashion. Also, transmission of real sensory data while using practical antenna and a more elaborate impedance modulator can be followed as a beneficial research track.

6.7 Low-Power Ring Oscillator

Clock generation circuitry is an integral part of most passive RFID tags. Like other building blocks of the tag, clock generator need to perform its task with a minimal power and area overhead. Oscillators form the core of such clock generator blocks. Among the different architectures of oscillator, ring-oscillators are the most appropriate candidates for passive RFID applications in virtue of their small area and low power consumption. In Section 5.1, An ultra-low-power VCRO for passive RFID tag applications is presented. Using QFG technique, the

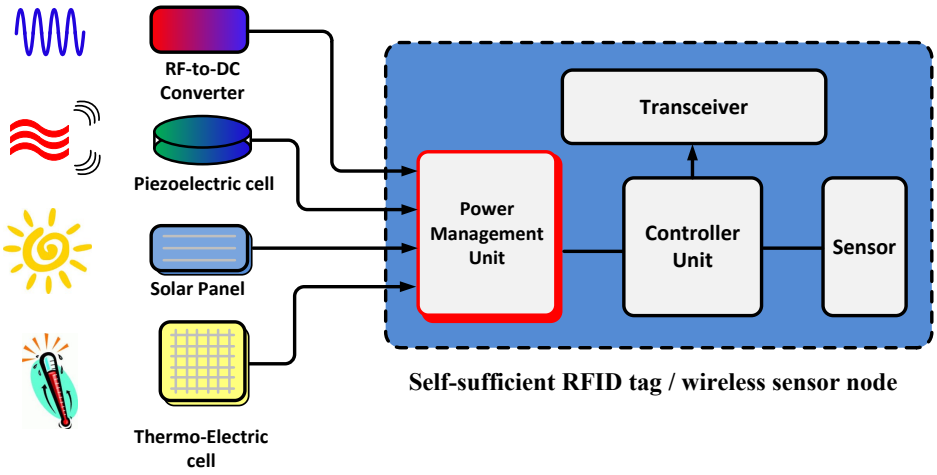


Figure 6.5: Schematic diagram of the self-sufficient RFID tag/senor node.

common-mode voltage of the devices in pseudo-differential delay cells are boosted, therefore, allowing oscillation with a low supply voltage. The QFG technique also offers a secondary frequency tuning knob. A quadrature-to-differential low-to-high voltage converter is presented to interface the low-swing output of the proposed VCRO with a higher voltage domain. Post-layout simulation results of the proposed VCRO confirm a nominal oscillation frequency of 4 MHz with a supply voltage as low as 140 mV while consuming 3.6 nW power. The VCRO core occupies an area of 500 μm^2.

As a future work, the proposed power reduction scheme for ring-oscillators can be implemented in a CMOS technology so that the effects of the technique on different performance metrics of the oscillator (e.g., phase noise) can be deliberately studied. The proposed oscillator can also be examined in a PLL system or a complete clock generator circuitry.

6.8 Future Target: Self-Sufficient RFID Tag

As discussed in details in this thesis, eliminating the battery as the sole non-permanent power source of passive RFID tags and wireless sensor nodes is an attractive approach. A battery-less tag (sensor node) supports a long operation life-time and facilitates further miniaturization of the node.

As a target system, a self-sufficient RFID tag (sensor node) is envisioned. The

tag harvests its required energy from all the available environmental sources including RF waves, temperature gradient, vibrations and solar radiation. For such a self-sufficient node, an efficient RF power converter is required to harvest the transmitted RF energy. The target system can benefit from proposed techniques in this thesis, such as power and area efficient data converters, efficient receive mode scheme (WUR) and efficient transmit mode schme (backscattering for short ranges).

Such a node requires an elaborate power management unit (PMU) to dynamically find the optimal source for specific application scenarios. The PMU (potentially) stores the excess energy for future use in the event of insufficient harvested power and/or power source failures. The study and proposition of new techniques to efficiently implement such a power management unit is a good topic for future research. The self-sufficient node is schematically depicted in Figure 6.5.

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