Design Techniques for Low-Power Low-Noise CMOS Capacitive-Sensor Readout Circuits

by

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Abstract

In recent years, the demand for low-cost, high performance, and miniature sized MEMS capacitive inertial sensors (accelerometer/gyroscope) has been steadily increasing. Use MEMS capacitive accelerometer as an example, for high precision applications, the resolution needs to be in the μg range at the frequency of interest. These high performance sensors are now been used in numerous applications that require more demanding specifications. For instance, they found their use in active suspension, adaptive brakes, alarm systems, tilt control, vibration, shock measurements, platform stabilization, inertial measurement units, inertial navigation/guidance, machine control, microgravity measurements, seismology, geophysical sensing, oil-field applications, earthquake detection, tactical missiles, robotics and minimally invasive surgery.

The precision in a micro-sensory system is limited by the CMOS electronic interfaces, due to the often higher electrical noise associated with the circuits. Additionally, with the growing popularity for portable devices such as cellular phones and tablets, power consumption also becomes an important factor. Therefore, the dissertation discusses and presents several circuit design techniques that improve important system parameters such as noise and power. Moreover, a design flow is provided at the end of the thesis to

demonstrate a systematic approach to design the sensor interface circuits.

Three major readout circuit blocks have been designed, built, and tested. The first interface uses a circuit technique such that the overall system is insensitive to parasitic capacitances from the sensing nodes. Moreover, a calibration scheme is used to remove DC offset caused by sensor capacitance mismatch. The second interface uses two circuit design techniques called correlated level shifting (CLS) and chopper stabilization (CS) to reduce the noise and the finite gain error from the operational amplifier (op amp), thereby improving both the noise and power performance of the system. The final interface utilizes a modified CLS technique such that it also serves as a noise and power improving mechanism. The first two readout circuits have been tested and measured experimentally, while the third readout circuit is verified via post-layout simulation.

Preface

I, Jack Shiah, am the principle contributor of all the chapters. Dr. Shahriar Mirabbasi, who is my direct research supervisor, has provided overall technical support and editing assistance on the manuscript. Dr. Edmond Cretu, Dr. Mrigank Sharma, and Dr. Elie Sarraf have provided technical support in regards to the MEMS sensor, as well as system integration (Chapter 3). The MEMS capacitive accelerometer was designed by both Dr. Mrigank Sharma and Dr. Elie Sarraf.

As mentioned below, some of the content of this thesis is written based on the following published or to-be-submitted works:

Conference Papers

1. J. Shiah, H. Rashtian, and S. Mirabbasi, "A low-noise high-sensitivity readout circuit for MEMS capacitive sensors", in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 3280–3283, May 2010 [1] → Chapter 3.

2. J. Shiah, H. Rashtian, and S. Mirabbasi, "A Low-Noise Parasitic-Insensitive CMOS Switched-Capacitor Interface Circuit for MEMS Capacitive Sensors", in *International NEWCAS Conference*, pp. 470–

473, June 2011 [2] → Chapter 3.

3. J. Shiah, and S. Mirabbasi, "A 5-V 555-μW 0.8-μm CMOS MEMS capacitive sensor interface using correlated level shifting", in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1504–1507, May 2013 [3] → Chapter 5.

Journal Papers

1. J. Shiah, and S. Mirabbasi, "A 5-V 290-μW Low-Noise Chopper-Stabilized Capacitive-Sensor Readout Circuit in 0.8-μm CMOS Using Correlated-Level-Shifting Technique", in *IEEE Transactions on Circuits and Systems II: Regular Paper*, vol. 61, no. 4, pp. 254–258, Feb. 2014 [4] → Chapter 4.

2. J. Shiah, M. Sharma, E. Sarraf, S. Mirabbasi, and E. Cretu, "A Parasitic-Insensitive Chopper Stabilized CMOS Readout Circuit with Sensor Mismatch Cancellation for Capacitive Micro-Accelerometers", to be submitted. → Chapter 3.

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Glossary

MEMS Microelectromechanical Systems

CS Chopper Stabilization

CDS Correlated Double Sampling

CLS Correlated Level Shifting

MCLS Modified Correlated Level Shifting

ADC Analog-to-Digital Converter

DAC Digital-to-Analog Converter

SC Switched-Capacitor

DoF Degree-of-Freedom

DSP Digital Signal Processing

CT Continuous Time

DT Discrete Time

ULP Ultra-Low-Power

AAF Anti-Aliasing Filter

PWM Pulse Width Modulation

AM Amplitude Modulation

FFT Fast Fourier Transform

Acknowledgements

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Moreover, I would wish to express my gratitude towards my supervisor, Dr. Shahriar Mirabbasi, for his guidance and patience during the course of this research. I am grateful for the interesting research topic and the chance to learn independently. I would also like to acknowledge Dr. Roberto Rosales for his help in regards to all the experimental equipment and for managing the test lab. The two people I mentioned in this paragraph both have great personalities and are two of the nicest human beings I know of.

I would like to show my sincere appreciation towards Dr. Edmond Cretu, Dr. Elie H. Sarraf, and Dr. Mrigank Sharma, for providing great amount of knowledge regarding MEMS micro-systems and numerous sensor elements. Without their aid, the experimental work would never have become a reality.

Moreover, thanks to all my colleagues and friends in the SoC group for their friendly support.

Last but not least, I want to thank my parents, Richard and Rose; my sister, Tammy; and my girlfriend, Joyce, for being so supportive no matter which stage of life I am at. Especially my mother, even during the darkest moments, she has been nothing but encouraging to me.

Dedication

To my parents.

Chapter 1

Introduction

Micro-electro-mechanical systems (MEMS) describe the technology of miniature devices that combine both electrical and mechanical components. More specifically, they generally consist of a microprocessor (electrical) and several functional blocks that interact with the mechanical surrounding such as micro-sensors [5]. These sensors are extremely small, having feature sizes in the micrometer scale. When the sensors are integrated within a broader system, combinations of different functionalities can be enabled, and amazing things happen. Systems built in MEMS technologies are generally smaller than a few millimetres.

Thanks to the technology advancement of silicon integrated circuit (IC), electronics can fortunately be realized on a tiny piece of silicon. As of the year 2014, transistor gate length is on the order of 10 nm [6], which is smaller than the Rhinovirus ($\sim$20 nm). With such prosperous IC industry, MEMS devices can also be built using IC fabrication technology. This opens up tremendous opportunities and possibilities since micro-machined silicon devices (mechanical) can be compatible with the surrounding electronics [7]. Many industries benefit from this fact because of the batch fabrication techniques. Sensors can be built in the micro scale with low cost and high

reliability. Ever since the end of 1980, miniature silicon-based inkjet printer head, pressure sensors, and accelerometers were already mass fabricated, which marks the beginning of a new "MEMS era" [8–11].

The readout/interface circuits (electrical), combining with the mechanical micro-sensors, form a complete MEMS device. In a complete MEMS device, the readout essentially translates the analog mechanical information, such as acceleration or angular speed, into an electrical signal, which is further processed by a computer. Such"complete system" allows MEMS technology to break into new application fields. The fact that the performance of the complete MEMS system is often largely dependent on the electrical readout, the development and design of such readout circuit has maintained as a hot research topic for more than two decades now. This thesis is also a research work based on the readout electronics.

Among all the different MEMS applications, the focus of this thesis is related to MEMS inertial sensor, which can be treated as a measurement unit that measures acceleration, velocity, and orientation of a moving object. The two main sensing components that are required in an inertial sensing application are accelerometer and gyroscope. They are used in a variety of applications including gaming, human activity monitoring, vehicular navigation, airplanes, drones, and earthquake detection [12–14].

Certain applications are more demanding than others in terms of sensitivity, resolution, signal to noise ratio (SNR) and dynamic range. Use accelerometer as an example, the need for a highly sensitive, high resolution/low-g (μg), and small sized MEMS accelerometer has been growing. These high performance sensors are now been used in numerous applications that re-

quire more demanding specifications. For instance, these accelerometers found their use in active suspension, adaptive brakes, alarm systems, tilt control, vibration, shock measurements, platform stabilization, inertial measurement units, inertial navigation/guidance, machine control, microgravity measurements, seismology, geophysical sensing, oil-field applications, earthquake detection, tactical missiles, robotics and minimally invasive surgery [15–17, 19–28, 41, 42, 49–55, 58, 65].

In the inertial navigation category, the author in [29] notes that high performance navigation grade (0.01 deg/hr and 25 μg) ring laser gyroscope (RLG) and inertial measurement unit (IMU) FOG IMUs are still relatively large and expensive. The same author states that MEMS system with performance of around 1 deg/hr and 100 μg would be available in the future.

In the field of robotic surgery, inertial sensors are used for detecting the position and orientation of the surgical tool. For example, the signal outputs can be integrated to determine or estimate the distance travelled by a surgical tool. The authors in [30] propose an active hand-held instrument to sense and compensate physiological tremor and other unwanted movements during a viteoretinal micro-surgery. The proposed system comprises six inertial sensors to compute and control the motion of the tip.

Additionally, seismic sensing for geophysical and oil explorations applications represents challenges in high sensitivity and low-g measurements. The MEMS technological breakthrough can definitely provide technical and economical benefits for seismic acquisition system users. This requires measurement of extremely small acceleration signal, on the order of $\sim ng/\sqrt{Hz}$ at very low frequencies (less than 100 Hz). There seems to be a grow-

ing trend in the industry to replace geophones with MEMS accelerometers, where large arrays of sensors tremendously increase the quality of seismic imaging. As a result, small size and weight of MEMS sensors can facilitate the deployment of very large seismic surveys [31]. An example of an inertial sensor used for such application is reported in [32]. They report the usage of 3C MEMS-based digital accelerometer (two horizontal and one vertical).

According to the market research done by IndustryARC [14], from the year 2013 to 2018, the global inertial sensor market has a 10.5% of compound annual growth rate (CAGR). This forecast is based on the fact that the key components inside the sensory systems will be cheaper and more compact due to technology advancement.

It is worth to mention that a CAGR of 10.5% can be considered healthy and steady. However, this rate predicted by IndustryARC seems to be quite conservative. From the market research conducted by MICROmanufacturing [33], inertial consumer combo sensors have a CAGR of 35%! The importance of the aforementioned research demonstrates a very strong trend in the inertial sensor market, which is the main motivation of this thesis. Note that the mechanical sensor of focus in the thesis is the accelerometer.

1.1 Objective

There are three major transduction mechanisms: piezoresistive, piezoelectric, and capacitive sensing [12]. Piezoresistive sensing detects the change of resistance of the piezoresistive material due to acceleration induced stress, and this resistance change can be easily detected by the dedicated electron-

ics. Piezoelectric sensing is based on a charge polarization of the piezoelectric material due to strain. Such charge polarization would produce a change in voltage. Lastly, capacitive sensing measures the change in capacitance due to the relative movement of a proof mass and the frame. Among them, capacitive sensing has been widely used due to its high sensitivity, good noise performance, low temperature coefficient, and good compatibility with CMOS technology for integrated sensor-based systems [34, 35]. An example of a capacitive accelerometer based MEMS chip is shown in Fig. 1.1 [90]. Here, the mechanical sensor is implemented in the same chip as the electrical readout. This way, the parasitic capacitance between the sensor and the readout can be minimized. This is especially beneficial if the device is intended for high-precision applications. Moreover, a single-chip solution would greatly reduce the size of the overall system, as well as the cost due to the elimination of wire bonding.

Many high-precision capacitive-sensing applications demand a high resolution sensor. The resolution of the system depends on the noise performance of the devices within it. As an example, the noise floor of an accelerometer determines the minimum detectable acceleration. Noise performance of a readout circuit has been the key research in the past [41, 42]. Moreover, when the sensors are used in portable devices, power consumption becomes another important factor. With such requirement on sensing accuracy and power, noise and other non-idealities must be minimized in the interface system to obtain satisfactory performance. In a complete MEMS system, there are two types of noise: mechanical (Brownian) and electrical. The mechanical noise is related to the sensor, whereas the electrical noise is associated

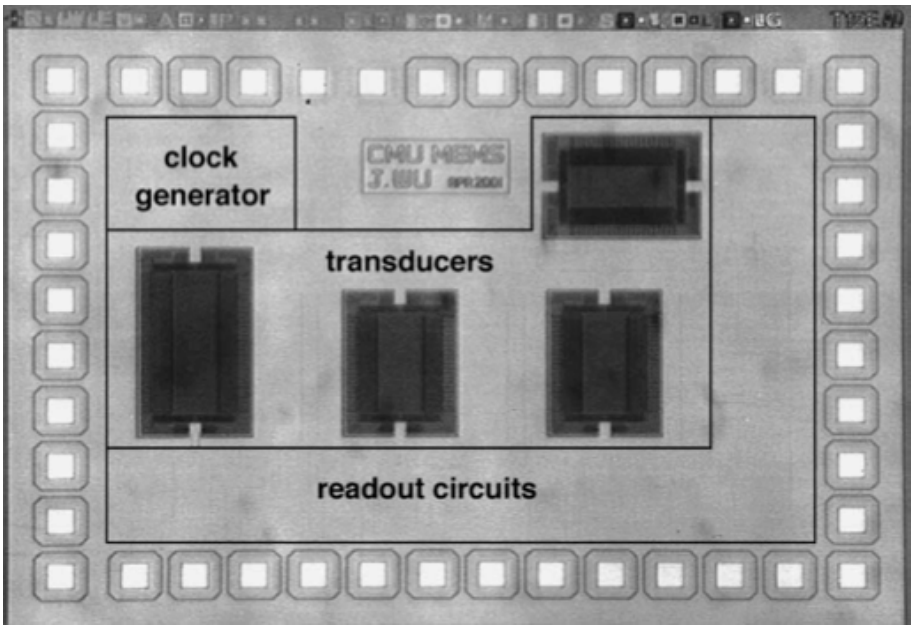

Figure 1.1: A microphotograph of an example of a single chip MEMS system, which realizes the complete analog interface for a capacitive MEMS accelerometer [90].

with the readout circuit. For a sensor with proof mass m and viscous damping coefficient b, its Brownian noise in the form of an equivalent acceleration noise can be expressed as [91]:

$$\overline{a_n^2} = \frac{4kTb}{9.8^2 m^2} \quad [g^2/Hz] \tag{1.1}$$

where k is the Boltzman constant (1.38×10^{23} J/K) and T is the absolute temperature. Depending on the size of the proof mass, the noise can vary. Typically, this noise is very small for high resolution applications, which is in the $\mu g/\sqrt{Hz}$ range. Due to the very low mechanical noise associated with the sensor, generally speaking, the electrical readout circuit puts the

limit on the resolution of the overall system. It is therefore very important that the noise floor of the electronic interface circuit is reduced to the level of the sensor mechanical noise. The major noise contribution in a CMOS integrated readout circuit is the flicker or $1/f$ noise of the input transistors at very low frequencies. This noise originates from "trapped" charges at the interface between the substrate and the oxide. These charges can be released by the energy state and result in the noise in the drain current. There are many other mechanisms that are believed to generate flicker noise [57]. Additionally, another electrical factor that affects the resolution of the system is the offset of the input transistors. In terms of offset, it is considered as a DC signal which originates from the imperfection of the fabrication technology. As devices are going through fabrication steps, the lithography cannot be absolutely symmetrical, thus generating mismatches in the transistors, which, in turn, produce DC offsets when circuits are built.

As far as power is concerned, the MEMS device should be operated in open-loop configuration. An example of an open-loop sensing accelerometer can be found in [90], and a closed-loop one can be found in [58]. A closed-loop system is able to increase the dynamic range, improve the linearity, and flatten the frequency response [59]. However, more components are required to implement a closed-loop system, which would consume a lot more power. Therefore, in order to achieve a low power device, operation in open-loop configuration may be more favourable. Chip area could be another specification that needs to be met. With all of the aforementioned important parameters of interest, the design of the electronic interface becomes a challenging and demanding task.

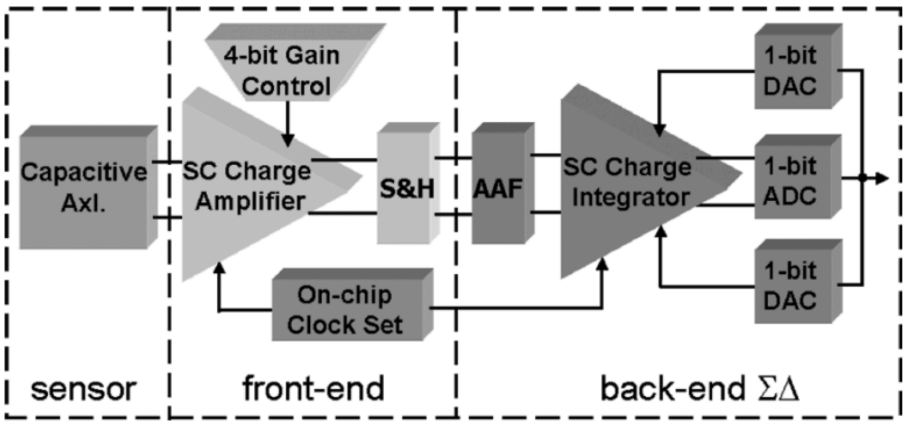

Figure 1.2: Block diagram of a14 bits open-loop ΣΔ CMOS SOI capacitive accelerometer [93].

An example block diagram of an open-loop MEMS capacitive sensor is shown in Fig. 1.2, where the capacitive sensor (on the far left) produces the input to the electrical system. The input is a capacitance variation generated from a force applied to the sensor. Then, the analog front-end, which converts the capacitance variation into a voltage signal. This signal is then filtered and digitized by an ADC in the back-end. Although all of the aforementioned circuit blocks are designed in this dissertation, the emphasis is on the capacitance-to-voltage converter, or the charge-transfer amplifier block. The ultimate scientific goal is to propose analog circuit design techniques to improve readout circuit performance in terms of noise and power, leading to a higher resolution, and lower power system.

1.2 Organization of the Thesis

This dissertation is organized into seven chapters. In the first chapter, the motivation behind the research and the main objective are introduced. Note that the objective is the discussion on several proposed low-power low-noise circuit design techniques for capacitive micro-sensors, in particular, inertial sensors such as an accelerometer (gyroscopes are not covered).

In Chapter 2, an overview of capacitive micro-accelerometer is first presented, including its theory of operation, modelling, and fabrication process. Then, well known circuit techniques that reduce low-frequency noise and offset are discussed. The name of the techniques are correlated double sampling (CDS) and chopper stabilization (CS). Finally, different types of sensing readout circuits that have been used in either industry or academia are described.

In Chapter 3, a chopper stabilized parasitic-insensitive interface with sensor mismatch cancellation for capacitive micro-accelerometers is presented. First, the design and the specifications of the mechanical sensing element (accelerometer) is discussed. Then, the proposed switched-capacitor (SC) readout circuit that interfaces with the sensor is described in detail. In this particular work, the electrical readout and the mechanical sensor are wire-bonded inside a single package forming a system-in-a-package (SiP). The experimental results are shown at the end of the chapter.

In terms of Chapter 4, a proposed capacitive readout circuit using correlated level shifting (CLS) technique in conjunction with CS is described. The CLS technique was originally presented in [98] and it will be briefly

overviewed in this chapter. The technique greatly boost op amp loop gain, thus achieving higher accuracy, which is beneficial for capacitive sensing readout circuits. Additionally, CS is applied in the circuit to reduce offset and $1/f$ noise. This integrated circuit is not interfaced with a MEMS sensor. Instead, a pair of on-chip variable capacitors are used to emulate the mechanical sensing element. Experimental results are reported at the end of the chapter.

In regards to Chapter 5, a modification to the CLS technique is proposed in which it reduces the offset and $1/f$ noise of the designed MEMS interface front-end, while preserving the benefits from the original CLS. The theory of operation of the technique is discussed in detail. Moreover, a $\Sigma\Delta$ analog-to-digital converter (ADC) is used in the back-end circuit block to digitize the analog signal from the front-end. At the end of this Chapter, the post layout simulation and measurement results are presented, followed by concluding remarks.

In Chapter 6, a general design flow describing readout circuit design process is presented, where MEMS accelerometer is used as an example. Moreover, the pros and cons of the reported readout circuits are discussed, such that the reader/designer is able to select suitable techniques for his/her own interface circuit design.

In Chapter 7, the major achievements of this work are summarized as concluding remarks. Additionally, some future directions for further investigations are provided.

Chapter 2

Background

As discussed in the previous chapter, capacitive MEMS sensors are widely used and can be found in many applications, such as high-precision inertial navigation. In this thesis, the ultimate scientific goal is to propose and demonstrate analog circuit techniques that are beneficial to the readout used in these high precision capacitive sensors. Therefore, in terms of the background of the thesis, the basic knowledge of a capacitive sensor will be first introduced in the form of a capacitive micro-accelerometer, where its theory of operation and electrical modelling will be discussed in detail. Secondly, some classic circuit techniques that would reduce the adverse effects when the capacitive sensor interfaces with the electronics will be presented. Finally, a literature survey that demonstrates several state-of-the-art complete inertial MEMS devices concludes this chapter.

2.1 Capacitive Micro-Accelerometer

The operation of a basic accelerometer can be explained with the aid of a simplified mechanical model illustrated in Fig. 2.1, where a proof mass m is connected to a rigid body via a spring having a spring constant of k_x. Also, the environment inside the frame provides damping D_x to reduce excessive

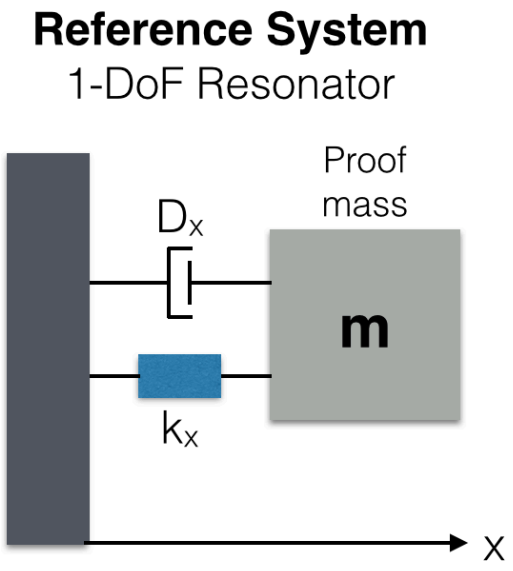

Figure 2.1: The simplified mechanical model of a single axis accelerometer (1-DoF resonator) having a proof mass m that is suspended by a spring k_x to the frame. The losses are modelled by a damper D_x. The variable x represents the position of the proof mass.

ringing. The mass can only move in the x-direction. Note that this example is essentially a one-degree-of-freedom (1-DoF) resonator, where a single-axis accelerometer is realized for the detection of translational (x-direction) acceleration.

When an external force (F_{ext}) is applied to the accelerometer in the positive x-direction, the mass would be displaced by a distance x. The spring would generate an elastic/restoring force (F_e) expressed as:

$$F_e = -k_x x \tag{2.1}$$

Moreover, in addition to the spring restoring force, there is a force that

depends on the velocity of the proof mass. Such force represents the energy lost in the resonator. The losses are caused by, for instance, material/anchor losses, mode conversion losses, and, especially, viscous losses, which is generally due to air damping [60]. The force exerted by the damper is:

$$F_d = -D_x \frac{\delta x}{\delta t} \tag{2.2}$$

Newton's second law of motion states that in an inertial frame of reference, the sum of all the forces acting on a mass is the mass times its acceleration:

$$\Sigma \overline{F} = m\overline{a} \tag{2.3}$$

Therefore, for the 1-DoF system shown in Fig. 2.1, the equation of motion for the proof mass is [60]:

$$ma_x + D_x \frac{\delta x}{\delta t} + k_x x = F_{ext} \tag{2.4}$$

where $a_x = \delta^2 x/\delta t^2$, and F_{ext} represents all the externally applied forces including the Brownian noise and electrostatic force.

Equation (2.4) demonstrates a relationship between the displacement x, and the acceleration a. In other words, an external force acting on the accelerometer induces a displacement on the proof mass, and this displacement can be detected to measure the amount of acceleration associated with the external force. For a capacitive accelerometer, the generated displacement under an outside force causes a change in capacitance (ΔC) which

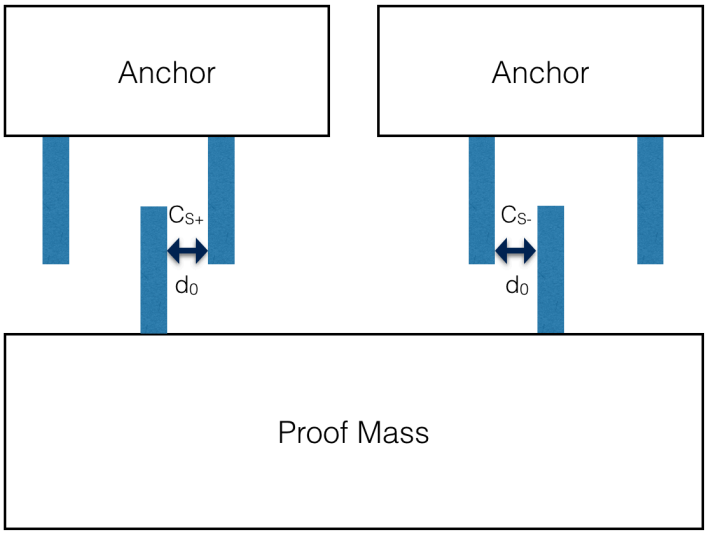

Figure 2.2: A simplified diagram of mechanical structure of a differential capacitive accelerometer (at rest). When a force is applied to the proof mass (right or left horizontally), the induced displacement causes the gap between the fingers d_0 to vary, thus generates changes in capacitances for C_{s+} and C_{s-}.

can be converted into an electrical signal such as voltage or current via a dedicated electronic readout circuit. The output of the interface circuit is then fed through digital signal processing (DSP) and the acceleration can be determined.

A simplified structure of a differential capacitive accelerometer is shown in Fig. 2.2, where a movable proof mass can only go either left or right depend on the direction of the external force (left/right). d_0 represents the nominal distance between the "shaded" fingers. The fingers act as two parallel plate capacitors (C_{s+} and C_{s-}) where the capacitances depend on the gap between the fingers:

$$C_{s+} = \frac{\epsilon_0 \epsilon_r A_{ol}}{d_0 - x} \tag{2.5}$$

$$C_{s-} = \frac{\epsilon_0 \epsilon_r A_{ol}}{d_0 + x} \tag{2.6}$$

where ϵ_0 is the vacuum permittivity, ϵ_r is the relative permittivity, and A_{ol} is the overlapping area between a pair of capacitive fingers.

When a force is applied to the capacitive sensor, since the proof mass is not fixed to any frame, it is free to move (only left/right in this example). Therefore, the fingers connected to the proof mass would move with the proof mass. The fingers attached to the anchors does not move because the anchors are fixed in space. This will induce a differential change in the distance between the fingers when the proof mass move in either directions. This change in the distance will generate changes in the differential capacitances according to (2.5) and (2.6).

If the displacement x is much smaller than the gap d_0:

$$C_{s+} = C_0 + \Delta C \tag{2.7}$$

$$C_{s-} = C_0 - \Delta C \tag{2.8}$$

where C_0 is the fixed sense capacitance and ΔC is the capacitance variation induced by acceleration:

$$C_0 = \frac{\epsilon_0 \epsilon_r A_{ol}}{d_0} \tag{2.9}$$

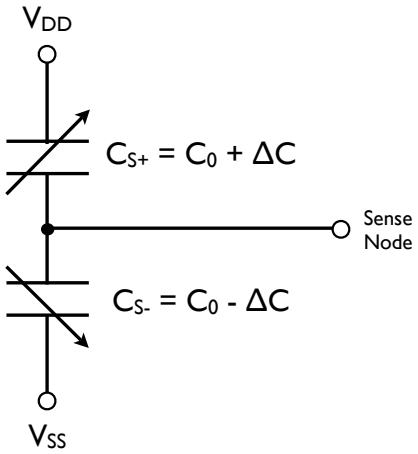

Figure 2.3: The modeling of the differential capacitive accelerometer in the electrical domain. As shown in the figure, the MEMS sensor can be simply viewed as two variable capacitors C_{s+} and C_{s-}.

$$\Delta C = \frac{\epsilon_0 \epsilon_r A_{ol} x}{d_0^2 - x^2} \tag{2.10}$$

Equation (2.9) and (2.10) demonstrate that the differential capacitive accelerometer can be simply modelled as two variable capacitors in the electrical domain as shown in Fig. 2.3.

2.2 Fabrication Process of Micro-Sensors

As mentioned in the Introduction, microstructures have adopted IC fabrication technologies and can be made in batches for mass production purposes. In other words, a large number of individual micro-devices can be realized simultaneously on a common substrate, usually on a silicon wafer. This can be illustrated in Fig. 2.4 [48]. The fabrication process involved in creating

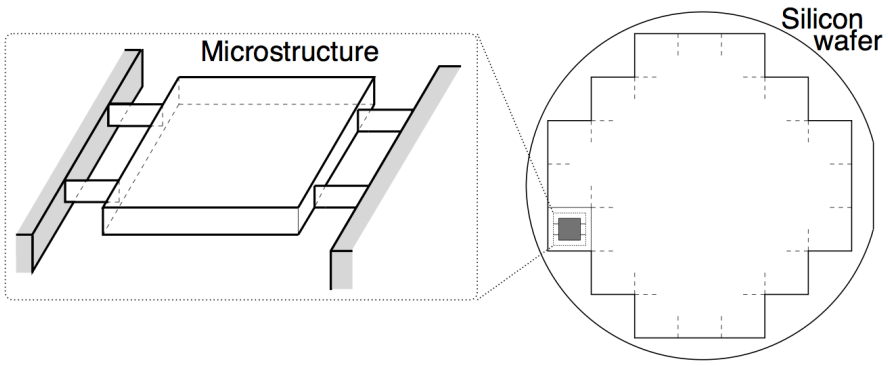

Figure 2.4: Micro devices on silicon wafer from fabrication process [48].

the microstructures include thin film deposition, photolithography, etching, and many more. After the fabrication is completed, the wafer is diced (divided) into separate micro devices. Each device is its own entity.

The two classical micro-fabrication techniques that have been used to implement MEMS capacitive sensors are surface micromachining [36–40, 42, 45] and bulk micromachining [43–47]. In surface micromachining, the mechanical microstructures are created by depositing and patterning thin films on the surface of a substrate, i.e., a silicon wafer. The resulting structure has a small mechanical proof mass, which limits the resolution of the microsensors. In contrast, bulk micromachined devices have much larger proof mass which leads to better resolution and higher sensitivity.

2.3 Classic Low-Frequency Noise/Offset Reduction Circuit Techniques

When a capacitive sensor such as the one explained in the previous section is interfaced with CMOS electronics, the noise/offset coming from the electrical side becomes an issue. If the electrical noise is higher than the mechanical noise at the frequency of interest, the overall sensor resolution would be limited by the former. Such problem is briefly discussed in the Introduction.

In CMOS circuits, when there is no noise/offset compensation applied, flicker noise is dominant in the low-frequency band. For many high precision MEMS sensing applications, the input signal varies slowly; therefore, low-frequency noise should be carefully dealt with. Throughout the history of CMOS circuit design, there are two classic circuit techniques that are intended to significantly reduce the flicker noise and offset: chopper stabilization (CS) and correlated double sampling (CDS) [96]. Although the theory of operation between the two are different, they achieve the same goal: reduction of low-frequency imperfections. In this chapter, both CS and CDS are introduced and discussed to give the reader an idea on how these techniques work and operate.

2.3.1 Chopper Stabilization Technique

The basic fundamental of CS can be best described graphically as shown in Fig. 2.5 [100]. A slow varying input signal V_{in} (signal of interest) is first modulated to higher frequency at f_{chop} via V_{chop} shown as V_A. The flicker noise should be insignificant compared with thermal noise at the modulating

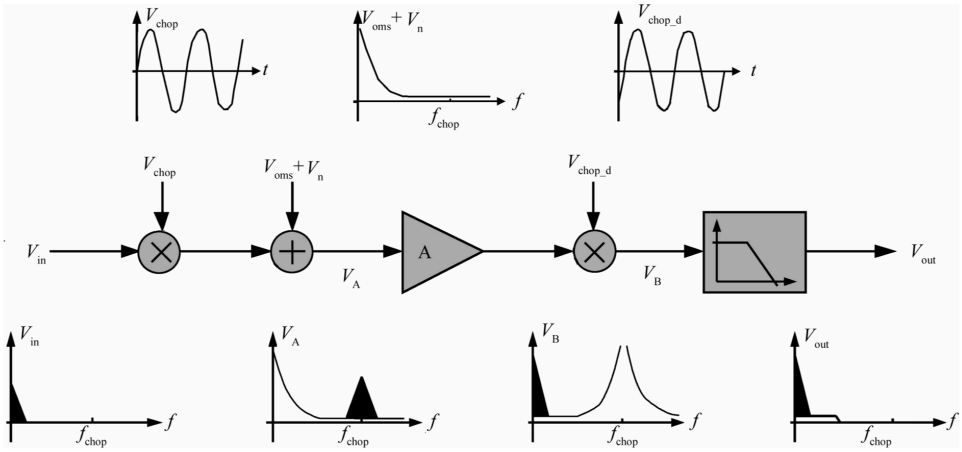

Figure 2.5: Frequency domain representation of a chopper stabilized amplifier.

(chopper) frequency (f_{chop}). The modulated signal with noise components are then amplified, and gone through the second modulation process via V_{chop_d}. The signal of interest is demodulated back to the baseband, while the flicker noise is modulated to higher frequency f_{chop}. A low pass filter (LPF) with a correct cutoff frequency at node V_B would filter out the flicker noise, leaving the signal at the baseband free of $1/f$ noise. Detailed noise analysis can be found in [96].

2.3.2 Correlated Double Sampling Technique

In terms of CDS, typically the circuit operates under two phase clocking where the op amp DC offset and low-frequency noise are sampled in one phase, and their effects are subtracted in the next phase by the instantaneous value of the contaminated signal. This operation can be best described by a simple example as shown in Fig. 2.6 [61]. In this example, the circuit

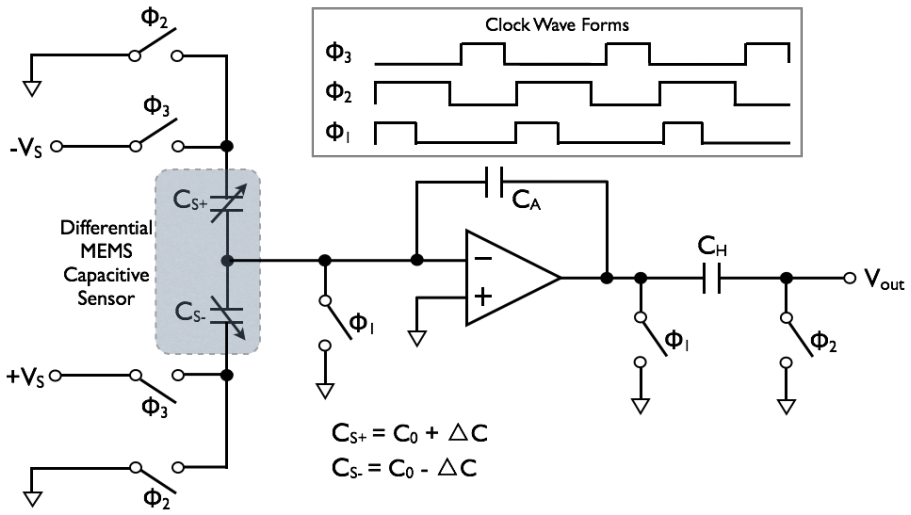

Figure 2.6: A MEMS capacitive readout example demonstrating correlated double sampling by using an error storage capacitor C_H.

is a capacitive sensor readout, where the sensor is modelled by a pair of differential variable capacitors. The reader can refer back to Fig. 2.3 for more details regarding such model.

In the ideal case, where circuit non-idealities do not exist, the output of the readout circuit (V_o) is:

$$V_o = \frac{2\Delta C}{C_A} V_s \tag{2.11}$$

where ΔC is the change in capacitance, C_A is the feedback capacitor, and V_s is the voltage source that charges the capacitive sensor.

Unfortunately, noise and offset always play a role when the circuit is implemented in the real world. Therefore, CDS is used to greatly reduce the aforementioned op amp imperfections. The key player in this circuit

is the error storage capacitor C_H. At the end of ϕ_1, the sampling switch located at the inverting input of the op amp is opened, thereby injecting charge and kT/C noise into the amplifier summing node. During the second half of ϕ_2, the aforementioned charge injection and kT/C noise, plus the input referred noise and offset of the op amp, are processed (amplified) and stored onto C_H. When ϕ_3 is high, voltage sources $\pm V_s$ are applied to the sensor capacitors, and the capacitance variation is translated into a voltage variation at the amplifier output. At the same time, the output contains both the signal of interest and the errors (noise and offset). These errors are subtracted by the previously stored imperfections on C_H, and results into a much better signal to noise ratio. Moreover, it is worth mentioning that the offset, charge injection, and kT/C noise are completely cancelled to the first order. Detailed noise analysis can be found in [96].

2.3.3 MEMS Capacitive Readout Circuits in the Literature

In this subsection, a number of innovative capacitive readout circuits in the literature will be discussed. To sense and process a sensor's physical information, the interface circuit can be implemented in either discrete-time (DT) or continuous-time (CT) fashion. Also, as mentioned in the previous chapter, depending on the requirements of the application, the sensor system can be either open-loop or closed-loop. If a low-cost and low-power system is desired in an application, open-loop style should be considered. On the other hand, if the end users are more interested in a large dynamic range and high linearity system, closed-loop sensor would be the obvious choice. For this thesis, power consumption is more of the focus instead of high linearity,

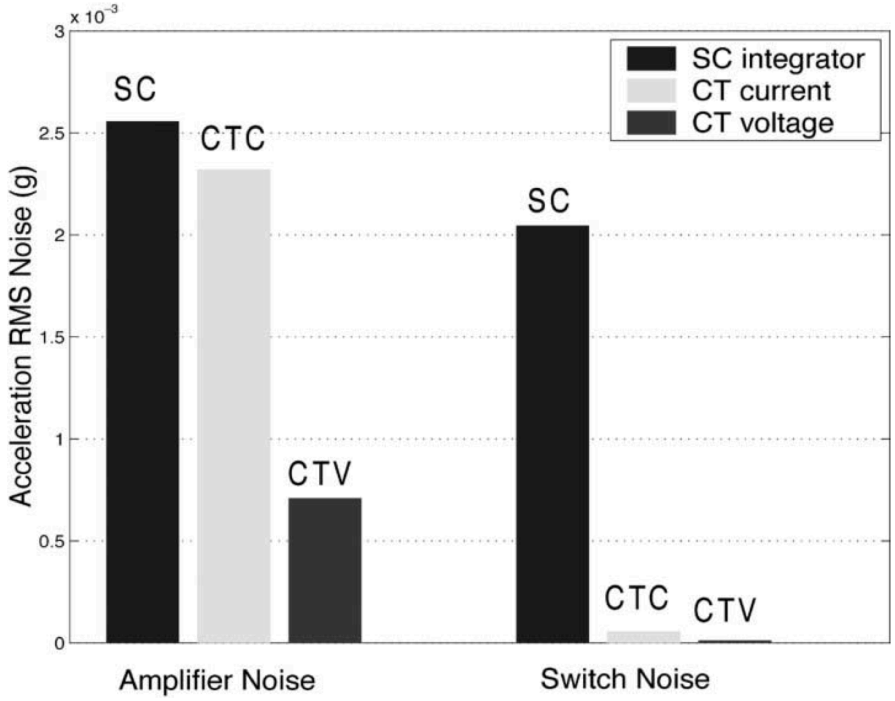

Figure 2.7: Electrical noise comparison between DT and CT based sensing circuits [90].

therefore, open-loop readouts will be the main discussion.

DT MEMS capacitive readout circuits essentially make use of switched-capacitor charge transfer amplifier scheme, which is very widely used in the literature [61–68]. This approach is very robust and can be conveniently implemented in CMOS technology. The primary issue with switched-capacitor interface circuit would be its high noise floor due to high kT/C noise at low capacitance, thermal noise of resistive MOS switches, and noise folding. Fig. 2.7 shows an interesting plot that compares the acceleration noise between DT and CT circuits [90]. Although DT circuits have the theoretical

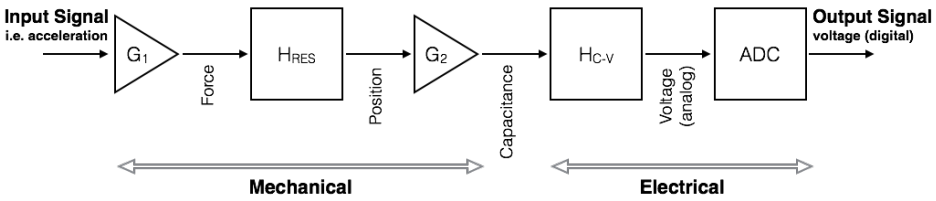

Figure 2.8: Block diagram of the capacitive open loop ULP readout front-end [68].

worse noise performance, the power consumption usually is less than its CT counterparts. This is because CT systems generally require more peripheral circuit blocks such as demodulator or low pass filter (LPF). Note that CT-based readout can be either continuous-time current (CTC) sensing [69] or continuous-time voltage (CTV) sensing [69–71, 90, 91, 100]. In this thesis, only CTV would be discussed.

Discrete-Time Based Interface

The first type of MEMS capacitive interface circuit that I would like to introduce is a DT, open-loop, ultra-low-power (ULP) readout. As mentioned previously, open-loop DT based circuits are more power efficient. ULP sensor interface circuits have been reported in [68, 72–74].

In [68], the overall structure of the capacitive readout circuit can be represented in a block diagram as shown in Fig. 2.8. This is a generic sensor interface chip, which means it can be applied to a broad range of different capacitive sensors. The externally applied input signal, i.e., an acceleration, is first converted into a force via a gain block G_1, which is essentially the mass of the sensor ($F = ma$). Simultaneously, the force

goes through the resonator (H_{RES}), in this case, the accelerometer, and generates a displacement between the "plates" that forms the capacitor. Note that the resonator is explained in Section 2.1. Such displacement creates a capacitance variation through G_2 (refer to Section 2.1). The change in capacitance is then translated into a change in analog voltage variation via a capacitance-to-voltage converter (H_{C-V}). Finally, the voltage variation is digitized via an analog-to-digital converter (ADC). In this case, it is an open-loop $\Sigma\Delta$ ADC.

Since DT circuits exhibit more noise, noise reduction circuit techniques should be used. In [68], both CS and CDS are used to improve the overall resolution of the readout front-end. CS is used to mainly deal with the mismatches between the two capacitance-to-voltage converters, whereas CDS is used to cancel the $1/f$ noise and amplifier offset. The detailed circuit schematics and analysis can be found in the paper. It is important to note that the focus of the ULP chip is obviously low-power design, at the expense of lower resolution, which is 9 bits.

Another similar design can be found in [93], which is a capacitive readout for a SOI accelerometer. Again, this is an open-loop design, where the authors decoupled the $\Sigma\Delta$ modulator from the sensor to achieve optimized performance regardless of the sensor capacitance [92]. The same block diagram in Fig. 2.8 can also be applied for this circuit, except that an anti-aliasing filter (AAF) is used in between the capacitance-to-voltage converter and the $\Sigma\Delta$ ADC. The actual block diagram of this particular system is shown in Fig. 1.2 in the Introduction. The capacitance-to-voltage converter is essentially the SC charge-transfer amplifier with programmable

gain control that determines the dynamic range of the system. The authors use CDS in the capacitance-to-voltage converter to reduce op amp offset and low-frequency noise. The signal out of the S/H block is fed to the ADC. Detailed circuit schematics and analysis can be found in the paper. Note that in this design, the authors focus on the resolution of the system rather than the power consumption. The capacitance resolution of the readout is 4 aF at 10 kHz and the system resolution is 14 bits.

A more recent open-loop SC based MEMS capacitive readout can be found in [102]. In this paper, only the capacitance-to-voltage converter is shown. The authors use a very interesting approach where lateral-BJT devices are used as input differential pair. It is due to the fact that BJT shows much better noise performance compared to CMOS technology. To further reduce the low-frequency noise and offset of the readout, CS technique is applied. The readout circuit shows very good noise performance (sub μg acceleration noise floor near DC).

The last DT interface circuit that will be discussed is an open-loop type readout that uses $\Sigma\Delta$ ADC topology. This type of readout circuit offers direct capacitance-to-digital conversion. Due to the popularity of digital signal processing (DSP), and the fact that the world has become digital everywhere, it is often convenient to have the natural signal (analog) to be quickly converted into digital forms.

There are many different types of ADC, where $\Sigma\Delta$ ADC is categorized as an oversampling converter. Oversampling means that the output data rate is deliberately set to be much higher than the signal bandwidth (BW). Generally speaking, the input BW of a MEMS capacitive sensor is quite low,

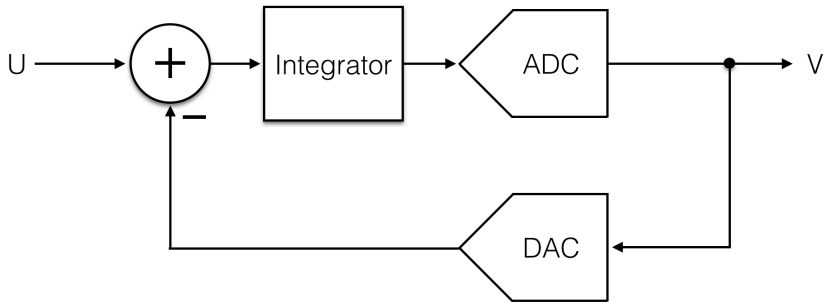

Figure 2.9: Block diagram of a first-order ΣΔ modulator.

which makes it even easier to implement the ADC.

The simplest form of a ΣΔ ADC (first-order) in block diagram is shown in Fig. 2.9 [75]. The converter consists of a negative feedback path with a DAC, a forward path with an integrator and an ADC. The ADC in the forward path can be a 1-bit quantizer (comparator).

The main advantage of using an oversampling converter is that it provides noise shaping and really suppresses the quantization noise. At the same time, it relaxes the specification requirements for the analog front end circuitries. For more detailed analysis on ΣΔ ADC, including its theory of operation and noise shaping discussion, please refer to [75].

The ΣΔ topology is especially well suited for the readout of capacitive sensors, as it directly translates the capacitance variation into a series of digital signal. This concept was originally proposed in [76], and the schematic of the readout is shown in Fig. 2.10. It can be seen that the first-order ΣΔ ADC has the capacitive sensor element as the sampling capacitors, together with an op amp with a feedback capacitor C_i, forms an integrator. The output of the integrator feeds into a comparator (1-bit ADC), and the final

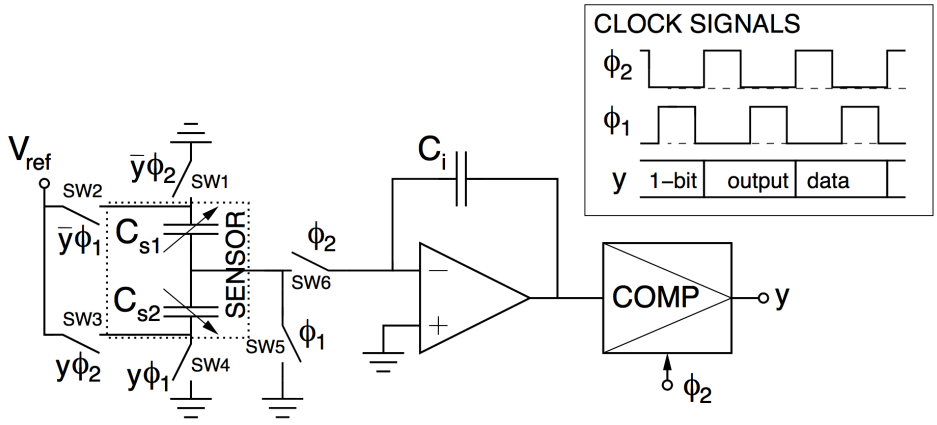

Figure 2.10: A first-order ΣΔ ADC for direct capacitance-to-digital conversion [48].

output is also used in the system feedback path (1-bit DAC). This circuit is essentially a first-order ΣΔ ADC, as described in Fig. 2.10. The output of the ΣΔ ADC is a pulse width modulated (PWM) signal, and once the output bit stream is filtered, the sensor information can be retrieved. Some of the more recent oversampled ΣΔ modulation-based sensor interfaces are discussed in [77–81]. Additionally, there are other interesting direct capacitance-to-digital converters such as capacitance-to-frequency converter [82], and capacitance-to-pulse-duration interfaces [83, 84].

Continuous-Time Based Interface

As mentioned earlier, a CT-based capacitive interface circuit exhibits better noise performance due to the absence of switch noise and noise folding as compared with its DT counterparts. A CT-based readout generally uses CS to reduce offset and $1/f$ noise. A classical CT interface can be found in [90].

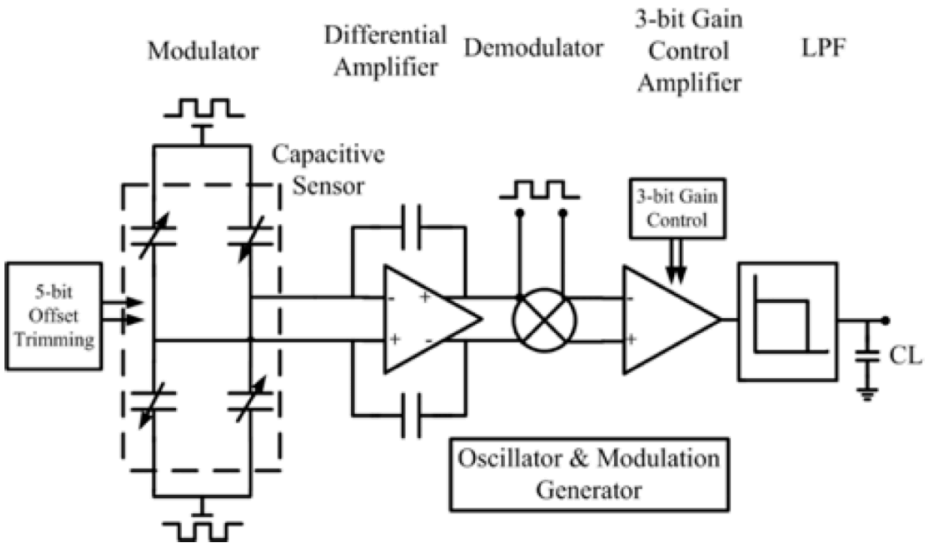

Figure 2.11: An example architecture of a CT-based capacitive readout circuit [91].

A more recent CT readout can be found in [91]. The typical architecture of a CT-based interface circuit consists of a modulator that modulates the input signal to higher frequency, an amplifier that produces voltage output that is proportional to input capacitance variation, a demodulator that brings the signal to the baseband, and a LPF that filters out high frequency noise. The overall sensing architecture demonstrated in [91] is shown in Fig. 2.11. The noise performance of these CT-based circuits are all very good (around 50 μg).

Chapter 3

A Parasitic-Insensitive Chopper-Stabilized CMOS Readout Circuit with Sensor Mismatch Cancellation for Capacitive Micro-Accelerometers

This chapter presents the theory, design and measurement results of a switched-capacitor (SC) CMOS readout circuit for a capacitive single-axis micro-accelerometer. The CMOS and micro-electromechanical-system-based (MEMS-based) devices are integrated in a single package forming a system-in-a-package (SiP). The interface front-end provides cancellation of DC offset caused by parasitic capacitances (e.g., due to bond-pads, interconnects between MEMS and electronic interface, capacitors themselves and sensor mis-

match). Additionally, the readout circuit utilizes chopper stabilization (CS) technique to reduce DC offset and low-frequency noise associated with the op amps [96]. The measured sensitivity of the accelerometer is 144 mV/g. The SiP achieves 3.9 $\mu g/\sqrt{Hz}$ acceleration noise floor and 0.05 aF$/\sqrt{Hz}$ capacitance noise floor at 500 Hz while consuming 4 mW from a single 5-V supply.

The major contribution of the designed MEMS interface circuit is its ability to virtually remove the adverse effects of parasitic capacitances and sensor mismatches. The basic concept of the technique was first introduced in [2] and [85]. In [85], the parasitic-insensitive technique was discussed and implemented on a CMOS integrator, whereas in [2], it was applied to a fully differential MEMS accelerometer. This chapter extends and provides simulation results and experimental verification of the proposed approach as well as more design insights in comparison to [2]. We also provide an overview of the fabricated SOI MUMPS micro-accelerometer and a more detailed analysis of the SC charge-transfer front-end.

In the literature, [86] also discusses a parasitic-insensitive readout circuit that interfaces with a MEMS gyroscope. The circuit architecture is similar to [2] in terms of switch placement. A minor difference between the two readout circuits is that the sampling capacitors in [86] are being reset initially. Moreover, the gyroscope in [86] is a single-ended device. Another parasitic cancellation technique can be found in [87], where the authors present a digital technique for capacitive sensors to calibrates non-idealities such as parasitics in the calibration phase and cancel the adverse effects in the measurement phase.

The chapter is broken down as follows: the micro-accelerometer is overviewed in Section 3.1, where both the physical structure and its electrical model are described. Section 3.2 discusses two non-idealities, i.e., parasitic capacitances and sensor capacitances mismatch that affect the DC level of output voltage signal. Section 3.3 describes the CS circuit implementation of the proposed charge-transfer amplifier, which is insensitive to parasitic capacitances and sensor capacitances mismatch. Experimental results are presented in Section 3.4, followed by a presentation of concluding remarks in Section 3.5.

3.1 Overview: Micro-Accelerometer

The designed MEMS accelerometer in this work is implemented in the SOI MUMPs technology (25 μm silicon thickness) [88]. The technology allows two device thicknesses: 25 μm and 10 μm. The substrate of the device is back etched to form a trench, thus eliminating the need for employing holes. This aspect of the technology is beneficial, as it adds to the proof mass required for highly sensitive acceleration measurements.

Design and modelling of the accelerometer is carried out in CoventorWare design environment. A proof mass is suspended using folded beams to reduce the mechanical nonlinearity and axial loading limitation of single fixed-guided beams. Four distinct sets of gap varying combs are used, which can be used for actuation and sensing. The minimum gap possible in SOIMUMPs technology is 2 μm, and the current design uses a gap of 3 μm. Simulated result of the exaggerated $0x$ mode (first resonant mode

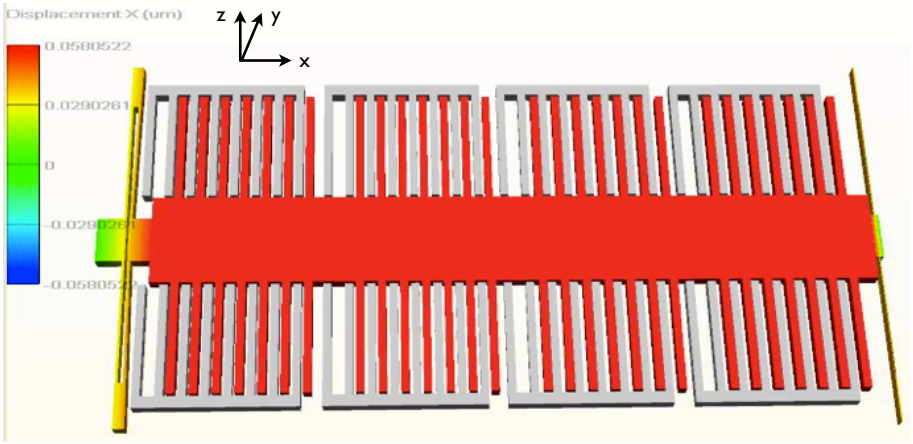

Figure 3.1: The simulated result of $0x$ mode of the micro-accelerometer in CoventorWare.

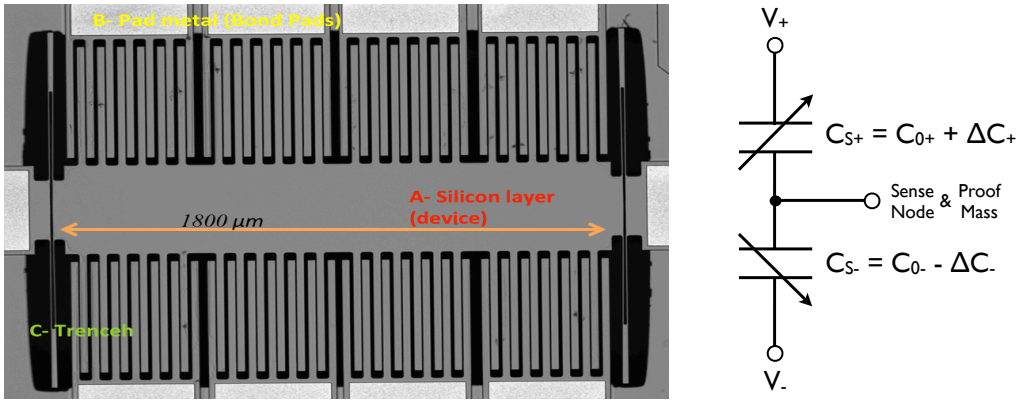

Figure 3.2: (a) A photograph of the fabricated capacitive micro-accelerometer under test; (b) Equivalent electrical model.

in x-y plane in the x direction) of the resonator is shown in Fig. 3.1. The image is exaggerated (fingers shifted to the right) to show that even with large displacements, there are no cross axis displacements.

A micrograph of the actual fabricated device (obtained from Polytec

MSA-500 microsystem analyzer) is shown in Fig. 3.2(a).The mechano-electrical interface can be modelled as a pair of differential capacitors C_{s-} and C_{s+} as shown in Fig. 3.2(b), where $C_{s-} = C_{0-} - \Delta C_{-}$ and $C_{s+} = C_{0+} + \Delta C_{+}$. Note that C_{0-} and C_{0+} are the fixed (nominal) capacitances when the accelerometer is at rest. Ideally, they should be equal, however, these fixed capacitances generally have a mismatch from practical fabrication procedures. The change in sensor capacitance ($\Delta C_{-,+}$) is generated differentially through the displacement x, which is caused by acceleration. For this gap varying type of sensor, we have:

$$C_{0-,+} = \frac{N\epsilon_0\epsilon_r A_{ol}}{d_{0-,+}} \tag{3.1}$$

$$C_{s-,+} = \frac{N\epsilon_0\epsilon_r A_{ol}}{d_{0-,+} \pm x} = C_{0-,+}\left(\frac{1}{1 \pm \frac{x}{d_{0-,+}}}\right) \tag{3.2}$$

where N is the total number of parallel capacitors realized through the fingers, ϵ_0 is the permittivity of vacuum, ϵ_r is the relative permittivity, A_{ol} is the overlapping area between each finger, and $d_{0+,-}$ is the nominal gap between each finger. Assuming $x \ll d_{0+,-}$ (which is a reasonable assumption, in particular for low-g acceleration), one can show that:

$$\Delta C_{-,+} = C_{0-,+}\left(\frac{\frac{x}{d_{0-,+}}}{1 \pm \frac{x}{d_{0-,+}}}\right) \tag{3.3}$$

To characterize the MEMS device optically, a Polytec MSA-500 microsystem analyzer is used. This state-of-the-art equipment combines laser Doppler vibrometry for out-of-plane displacements measurements and video

Table 3.1: Design Parameters of the Accelerometer

Proof mass dimensions	1.8mm x 0.4mm x 25μm
Proof mass	59.1 μ gram
Overlap area of each finger	540 μm^2
Capacitive gap	3 μm
Pull-in voltage	7.58 V
Sensitivity (differential)	13 fF/g
Resonant frequency	2.8 kHz
Brownian noise floor	0.6 $\mu g/\sqrt{Hz}$

stroboscopy for in-plane dynamics measurements. In the latter case, the equipment can detect device motions down to 2 nm resolution. From optical characterization, the important design parameters of the SOI MUMPS micro-accelerometer are listed in Table 3.1. Note that the pull-in voltage is the amount of voltage applied across the fingers such that the generated electrostatic force overcomes the spring force and as the result, would lead to fingers snapping together.

3.2 Overview of Parasitics and Mismatches

Fig. 3.3 shows a simple structure of a SC charge-transfer readout front-end with the presence of parasitic capacitances C_{p1}, C_{p2}, and C_{p3}, which represent the total parasitics at the corresponding nodes. Note that the MEMS capacitive sensor (mechanical part) is shown in the shaded area. Assuming the sensor is a micro-accelerometer, the function of the readout circuit is to detect the change in sensor capacitances due to an applied force

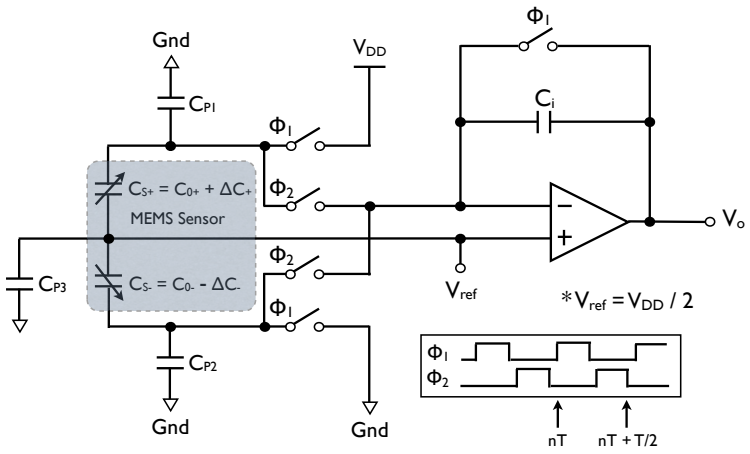

Figure 3.3: A simple SC charge-transfer MEMS capacitive readout circuit. The MEMS sensor is shown in the shaded area. The parasitic capacitances, i.e., C_{p1}, C_{p2}, and C_{p3}, are also shown in the figure.

(or acceleration), and translate such capacitance variation into an output voltage. The operation of the circuit shown in Fig. 3.3 is as follows: during ϕ_1, the sense capacitances C_{s+} and C_{s-} are charged to $(V_{DD} - V_{ref})$ and $-V_{ref}$, respectively, while the charge-transfering feedback capacitor C_i is discharged to zero. Simultaneously, the parasitic capacitor C_{p1} is charged to V_{DD}, while C_{p2} is discharged. Note that the parasitic capacitor C_{p3} (due to parasitic capacitances associated with the node connected to the proof mass of the sensor) is immaterial in the overall transfer function because it is always charged to the reference voltage V_{ref} (AC ground), i.e., $V_{DD}/2$.

When ϕ_2 goes high, the sum of the charges stored in the aforementioned capacitors are transferred to C_i and a new output is generated. Assuming the open-loop gain of the operational amplifier (op amp) is large, the output can be expressed as:

$$V_o = \frac{V_{DD}}{2}\left(1 + \frac{\Delta C_p - C_{MM} - \Delta C_T}{C_i}\right) \tag{3.4}$$

where ΔC_p is the difference between the two parasitics ($\Delta C_p = C_{p2} - C_{p1}$). Additionally, C_{MM} accounts for the sensor mismatch and is equal to the difference between the two nominal capacitances ($C_{MM} = C_{0+} - C_{0-}$). Finally, $\Delta C_T = \Delta C_+ + \Delta C_-$. As it can be seen from (3.4), the DC level of the resulting output is influenced by the parasitic ΔC_p and the sensor mismatch C_{MM}, which would affect the maximum output swing of the readout, leading to less dynamic range.

Generally speaking, the parasitic capacitances can be reduced effectively by minimizing the length of the interconnections, or by introducing individual shielding for the sensor leads. Moreover, in some approaches, such as [91], one can reduce the sensitivity to parasitic capacitances by increasing the gain of the op amps. Nevertheless, it is beneficial to design a circuit that removes or minimizes the adverse effects of the parasitic capacitances. Such a circuit is discussed in the following section.

3.3 Circuit Implementation

The overall building blocks of the CMOS MEMS SiP and its required signals are demonstrated in Fig. 3.4. The CS charge-transfer amplifier circuit is directly connected to the micro-accelerometer via bond wires. The charge-transfer amplifier circuit converts the sense capacitance variation (changing charge) to an amplified output voltage where the peak-to-peak voltage amplitude represents the displacement of the proof mass. This output signal

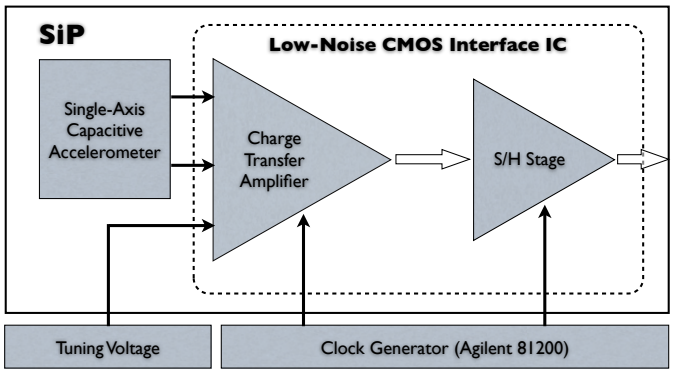

Figure 3.4: Overall system architecture of the implemented CMOS MEMS SiP.

enters a sampled and hold (S/H) stage which produces a smoother envelope detected signal. The externally applied tuning voltage is used to cancel the DC offset caused by sensor capacitance mismatch. The required clock signals are generated by an Agilent 81200 clock module. In the following subsections, each of the building blocks of the proposed CMOS interface IC is described in more detail.

3.3.1 Charge-Transfer Amplifier

To improve the sensitivity of the capacitive readout circuit, the parasitics and mismatches introduced in Section 3.2 should be carefully dealt with. The proposed parasitic insensitive circuit was originally presented in [2]. In this work, it is expanded, implemented, and measured. The interface circuit shown in single-ended configuration is illustrated in Fig. 3.5 to first explain the parasitic-insensitive technique. The overall differential readout circuit with CS will be shown after.

The purpose of the circuit in Fig. 3.5 is to eliminate the DC offset that the

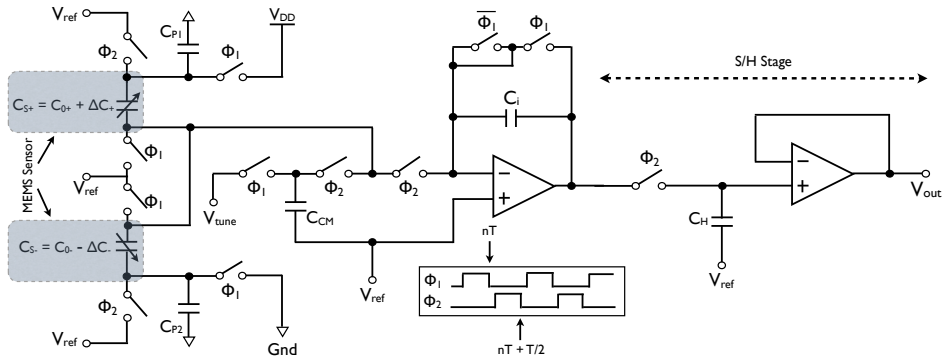

Figure 3.5: The schematic of the proposed capacitive readout circuit that consists of a parasitic-insensitive charge-transfer amplifier with sensor mismatch cancellation and a S/H stage.

parasitics and mismatches create in (3.4). During the ϕ_1 phase, similar to the circuit in Fig. 3.3, C_{s+} and C_{s-} are charged to $(V_{DD}/2)$ and $(-V_{DD}/2)$, respectively, while the integration capacitor C_i is discharged. The parasitic capacitances C_{p1} and C_{p2}, in this case, are connected to AC ground in both clock phases, therefore, they are always discharged. Therefore, these parasitic capacitances will not influence the transfer function. The capacitor C_{CM} is used to store the correct charges to cancel DC offset due to mismatch (common-mode adjustment) and has the following charge (Q_{CM}) in this clock phase:

$$Q_{CM} = \left(\frac{V_{DD}}{2} - V_{tune}\right) C_{CM} \tag{3.5}$$

Note that the amount of charge stored on C_{CM} can be adjusted by varying V_{tune}.

When ϕ_2 goes high, C_{s+} and C_{s-} are discharged because their terminals

are either connected to a DC source or virtual ground. The sum of the charges stored in ϕ_1 are transferred to C_i and a new output is formed:

$$V_{out} = \frac{V_{DD}}{2} + \frac{Q_{CM}}{C_i} + \frac{V_{DD}[C_{MM} + \Delta C_T]}{2C_i} \tag{3.6}$$

Note that the parasitic capacitances C_{p1} and C_{p2} play no role in the transfer function because they always remain discharged after settling.

If the following condition is fulfilled by adjusting V_{tune},

$$\frac{Q_{CM}}{C_i} + \frac{V_{DD}C_{MM}}{2C_i} = 0 \tag{3.7}$$

then the DC offset caused by sensor mismatch can be ideally eliminated, which would allow the circuit to operate at an optimal DC level. Also note that dummy switches are used in the charge-transfer amplifier to reduce the effects of charge injection [89]. It is important to mention that in this proof-of-concept prototype, the external adjustable signal V_{tune} is controlled manually. Such signal can certainly be varied automatically by other more sophisticated implementation, but it is out of the scope of this work.

To improve the noise performance of the system, chopper stabilization (CS) technique is also incorporated in the proposed parasitic-insensitive readout circuit to further reduce low-frequency imperfections associated with the op amp, i.e., offset and low-frequency noise. The exact differential structure of the overall readout circuit is shown in Fig. 3.6 with the key clock signals displayed in Fig. 3.7. Note that due to the use of CS technique, the sampling clock is divided into two phases: ϕ_{1a} and ϕ_{1b} as shown in Fig. 3.6. During consecutive ϕ_{1a} and ϕ_{1b} phases, the input capacitor structure

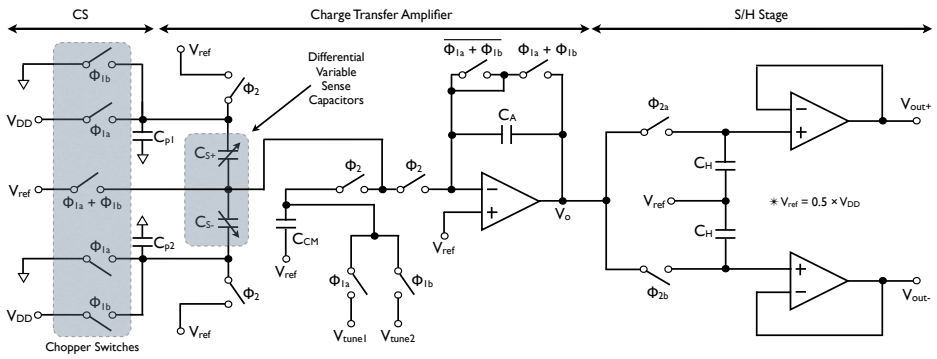

Figure 3.6: A CS parasitic-insensitive charge-transfer MEMS capacitive readout circuit with sensor mismatch cancellation. The S/H stage acts as a demodulator and produces a smoother signal at the output.

is alternately charged with opposite voltage polarity. During ϕ_{1a}, C_{S+} is charged to $V_{DD}/2$, and C_{S-} is charged to -$V_{DD}/2$. During the following ϕ_{1b}, C_{S+} is charged to -$V_{DD}/2$, and C_{S-} is charged to $V_{DD}/2$. Such operation generates an amplitude modulated (AM) signal at the output of the charge-transfer amplifier (during ϕ_2), where the peak-to-peak amplitude is proportional to the difference in the sensor capacitors [97]. Also, note that the op amp input offset and the flicker noise primarily affect the DC voltage level of the output, but not the amplitude of the AC signal. Therefore, the aforementioned low-frequency non-idealities can be removed after the output is demodulated differentially. It can be shown that the final output V_{out} (differential output after S/H) can be expressed as:

$$V_{out} = V_{out+} - V_{out-} = V_{DD}\left(\frac{C_{S+} - C_{S-}}{C_i}\right) \tag{3.8}$$

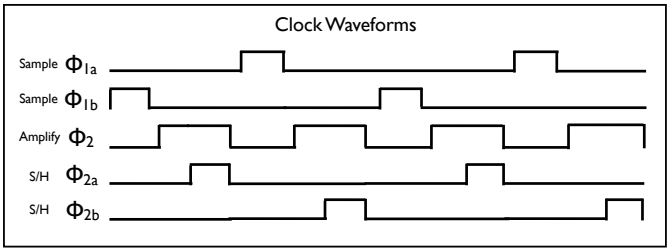

Figure 3.7: The clock waveforms for the CMOS readout as shown in Fig. 3.6.

3.3.2 S/H Stage

The output of the charge-transfer amplifier is fed to the S/H stage, which is implemented by two simple op amps with negative feedback configuration as shown in Fig. 3.6. The S/H stage is meant to smooth out the higher frequency modulated signal from the charge-transfer amplifier.

Note that to reduce the adverse effects of charge injection in the S/H circuit, transmission-gate switches are used at the non-inverting input of the op amps. Furthermore, special attention has been paid to sizing of the NMOS and PMOS of the switch such that their charge injection almost cancel each other, which in turn results in a low overall charge injection error.

Simulated transient response (differential S/H output) of the parasitic-insensitive readout circuit having different values for parasitics (C_{p1} and C_{p2}) is shown in Fig. 3.8. As it can be seen in the figure, the DC voltage level of the output is not affected and stays at 0 V.

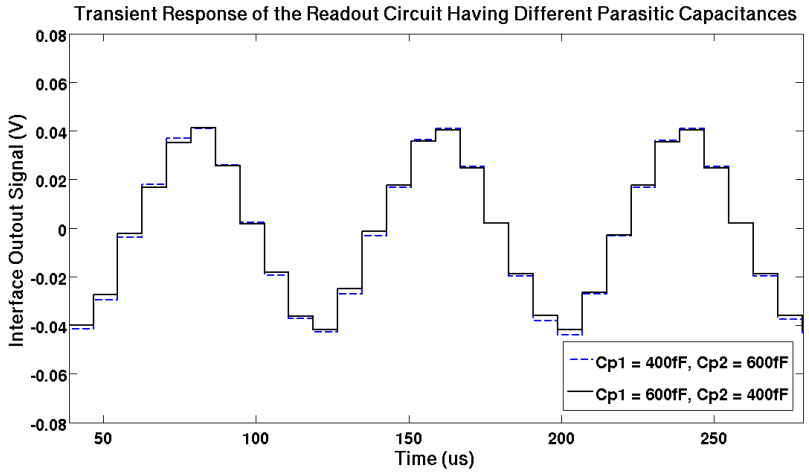

Figure 3.8: Simulation result showing that the DC voltage level at the output of the readout circuit is not affected by different values of parasitic capacitances.

3.3.3 Operational Amplifier

The op amps that are used in all of the building blocks of the sensor interface circuit utilize the folded-cascode topology as shown in Fig. 3.9. Each op amp has a gain of 72.15 dB, a phase margin of 60°, and a gain-bandwidth of 116.5 MHz at 500 fF load. Since the frequency of the variations in the sense capacitance are generally low for an accelerometer, minimization of the flicker noise is very important. The input-referred voltage flicker noise power spectral density (PSD) of the folded-cascode op amp is [89]:

$$\frac{\overline{v_{n,f}^2}}{\Delta f} = \frac{2}{C_{ox} f}\left[\frac{K_{Fp}}{(WL)_1} + \frac{K_{Fn}}{(WL)_3}\frac{g_{m3}^2}{g_{m1}^2} + \frac{K_{Fp}}{(WL)_9}\frac{g_{m9}^2}{g_{m1}^2}\right] \tag{3.9}$$

where g_{mi} is the transconductance of MOS transistor M_i, f is the frequency of operation of the circuit, W_i and L_i are the channel width and length of

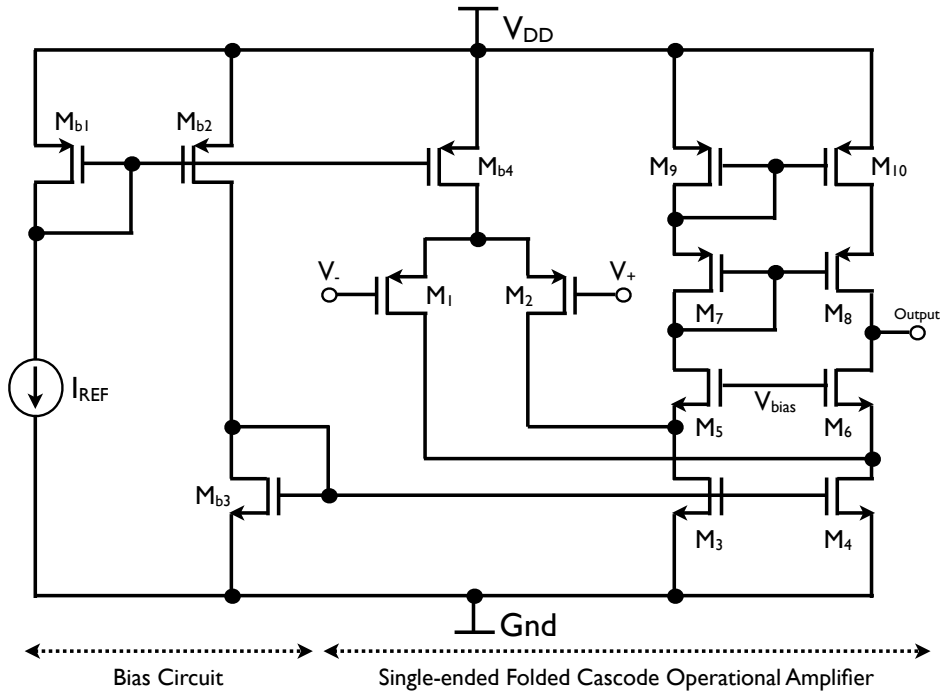

Figure 3.9: The schematic of the folded-cascode op amp designed to minimize both thermal and flicker noise.

transistor M_i, C_{ox} is the gate oxide capacitance per unit area, and K_{Fp} and K_{Fn} are the flicker noise coefficients of PMOS and NMOS transistors, respectively. In this design, PMOS input differential pair is chosen because of its lower flicker noise coefficient. The input pair is also made large to further reduce flicker noise.

Other than the flicker noise, the reduction of thermal noise is also taken into account. The input referred thermal noise power can be expressed as [89]:

$$\frac{\overline{v_{n,thermal}^2}}{\Delta f} \approx 2\left(4kT\frac{2}{3g_{m1}}\right)\left(1+\frac{g_{m3}}{g_{m1}}+\frac{g_{m9}}{g_{m1}}\right) \tag{3.10}$$

Table 3.2: Device Sizing of the Op Amp

Transistor	Width	Length
M_1	100 μm	0.8 μm
M_3	21.4 μm	0.8 μm
M_5	10.2 μm	1.6 μm
M_7	10.2 μm	5.2 μm
M_9	10.2 μm	5.2 μm
M_{b1}	100 μm	0.8 μm
M_{b2}	21.4 μm	0.8 μm
M_{b3}	10.2 μm	1.6 μm
M_{b4}	10.2 μm	5.2 μm

Since the input pair is made large, g_{m1} is large ($g_m \propto W$), thus reducing the thermal noise of the op amp. Another benefit of having large g_m for the input pair is that it increases the gain of the op amp. The trade-off of having a large input pair would be the reduction of the bandwidth due to the larger input capacitances. Fortunately, for this particular application where the input frequency is extremely low, the lower bandwidth is not a concern. The sizing of the transistors of the op amp is presented in Table 3.2. Note that the reference DC current I_{REF} is 12.5 μA.

3.3.4 Closed-Loop Noise and Offset Consideration

From the previous subsection, the total input-referred noise of the op amp is essentially:

$$\frac{\overline{v_{n,total}^2}}{\Delta f} = \frac{\overline{v_{n,f}^2}}{\Delta f} + \frac{\overline{v_{n,thermal}^2}}{\Delta f} \tag{3.11}$$

Since the sensing application operates at low frequency, flicker noise is the dominant noise, and thermal noise can be neglected for this analysis.

Based on the readout circuit shown in Fig. 3.6, the total noise at the output (V_{out+}), can be expressed as:

$$\overline{v_{out}^2} \approx \overline{v_{n,f}^2}\left(1+\frac{2C_0}{C_i}\right)^2 + \overline{v_{n,f}^2} \tag{3.12}$$

The total noise at the negative terminal (V_{out-}) has the same expression as (3.12). Since flicker noise mainly affects the DC level at the output, the flicker noise has minimal effect on the differential final output (V_{out+} - V_{out-}).

Furthermore, note that C_0 is the nominal capacitance when sensor is at rest. As it can be seen from (3.12), if the $2C_0$ is a small fraction of the feedback capacitor C_i, the output noise can be reduced. However, since the overall sensitivity (gain) of the readout circuit is inversely proportional to C_i, this feedback capacitance cannot be too large. Thus, for sizing the feedback capacitor C_i, there is a trade-off between noise and circuit sensitivity. Also, note that as discussed in Section 3.3.3, it is beneficial to keep the thermal noise contribution $\overline{v_{n,thermal}^2}$ low based on (3.10).

In terms of offset, the total offset that will appear at the positive terminal of the output (V_{out+}) can be expressed as:

$$V_{out,os} \approx V_{os}\left(1+\frac{2C_0}{C_i}\right) + V_{os} \tag{3.13}$$

where V_{os} is the input-referred offset of the op amp. The offset showing at the negative terminal of the output has the same expression as (3.13) and

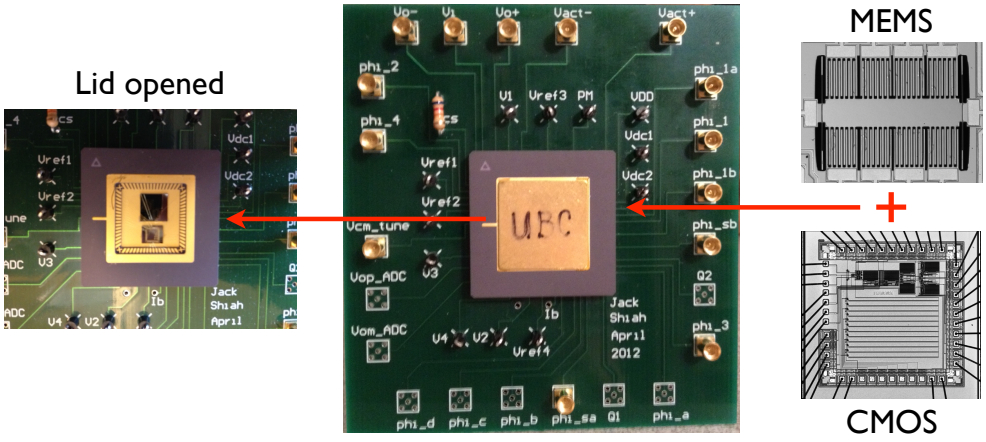

Figure 3.10: The S-i-P (CMOS and MEMS accelerometer integrated in a package) is mounted on a PCB for testing.

the differential final output will have no offset contribution (assuming the two S/H op amps are matched perfectly).

3.4 Experimental Results

3.4.1 Implementation

The CMOS readout and the MEMS accelerometer are fabricated in Dalsa's 0.8 μm CMOS process and SOI MUMPS, respectively. The two chips are put into a single package to minimize parasitics. An image of the system-in-a-package (SiP) mounted on a PCB is shown in Fig. 3.10. The circuit dissipates about 4 mW from a single 5-V supply.

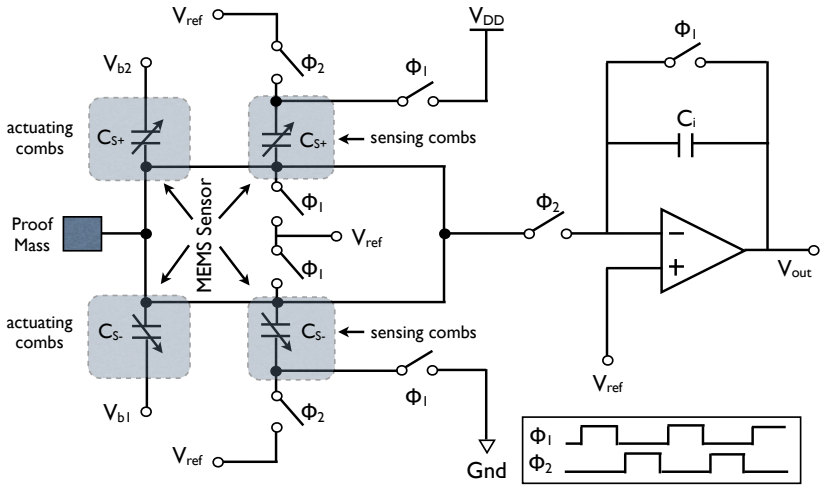

Figure 3.11: The test set up of CMOS MEMS S-i-P in simplified schematic form using electrostatic force testing.

3.4.2 Electrostatic Force Testing

In the absence of a shaker table, the external accelerations are mimicked using equivalent electrostatic forces, applied on a separate set of comb drives. The set up in simplified schematic form is illustrated in Fig. 3.11. The accelerometer dynamics can be modelled as:

$$m\frac{d^2x}{dt^2} + D_x\frac{dx}{dt} + kx = F_{el} \tag{3.14}$$

where x is the displacement, m is the mass of the proof mass, D_x is the damping coefficient, and k is the spring constant. F_{el} denotes the electrostatic force and can be expressed as:

$$F_{el} = \frac{\epsilon_0 A}{2(d_0 - x)}V_b^2 \tag{3.15}$$

where V_b is the actuation voltage across the plates. Note that only one parallel plate capacitor is being considered in (3.15), i.e., one finger of the multi-finger structure.

By applying AC voltages (V_{b1} and V_{b2}) to the differential actuating combs, the sensor is put into motion due to the corresponding electrostatic force, and the readout circuit outputs a voltage wave following the force (acceleration). If $V_{b2} = -V_{b1} = V_b = V_B \sin(wt)$, F_{el} can be linearized as follows (assuming x $\ll d_0$):

$$\begin{aligned} F_{el} &= F_{el2} - F_{el1} = \frac{\epsilon_0 A}{2d_0^2}[(V_{b2} - V_{ref})^2 - (V_{ref} - V_{b1})^2] \\ &= -\frac{\epsilon_0 A}{d_0^2} 2V_{ref} V_b \end{aligned} \tag{3.16}$$

Note that the frequency of F_{el} is identical to the frequency of V_b (i.e., w), therefore, the generated capacitance variation ΔC would also vary at w. This would be an issue if there is a signal feed through from the actuating voltages V_b to the output of the readout circuit. Such signal would have the same frequency of w, and therefore, the signal of interest ΔC (acceleration), cannot be differentiated from the feed-through signal.

The source of this feed-through can be explained as follows: when clock phase ϕ_2 is on, there is a path from V_{b1} and V_{b2} to the op amp. Therefore, the output of the first stage of the readout front-end, which is provided below, would have some components from V_{b2} and V_{b1}:

$$V_{out,partial}(s) = \frac{-V_{b2}(s)C_{S+}}{C_i} - \frac{V_{b1}(s)C_{S-}}{C_i} \tag{3.17}$$

If C_{S+} and C_{S-} are equal, $V_{out,partial}$ would be 0, and there would be no feed through. However, in practice, there will be mismatches in the fabricated device, which results in a portion of signal from V_b to feed through to the output of the charge-transfer amplifier. Since both the signal of interest and the coupled signal vary at the same frequency, it is not possible to separate them in the frequency domain. Note that this feed-through signal only exists when electrostatic force testing is utilized.

This problem can be solved if the AC actuating voltage V_b is applied to only one side of the actuating combs, while the other side is kept at a DC voltage (V_{ref}). The resulting force to displacement relationship would be:

$$m\frac{d^2x}{dt^2} + D_x\frac{dx}{dt} + \left(k - \frac{\epsilon_0 A}{d_0^3}V_b^2\right)x = F_{el} = \frac{\epsilon_0 A}{2d_0^2}V_b^2 \tag{3.18}$$

The electrostatic force can be further expanded to:

$$F_{el} = \frac{\epsilon_0 A}{2d_0^2}V_B^2\left(\frac{1 - cos(2wt)}{2}\right) \tag{3.19}$$

It can be seen from (3.19) that the force has a frequency of $2w$, which means the displacement and the eventual capacitance variation caused by it would also have a frequency of $2w$. Meanwhile, the signal that is coupled from the actuating voltage V_b is at the frequency of w; thus, the signal of interest can be separated from the feed-through signal (in the frequency domain).

The test set up is shown in Fig. 3.12. The sensitivity of the readout cir-

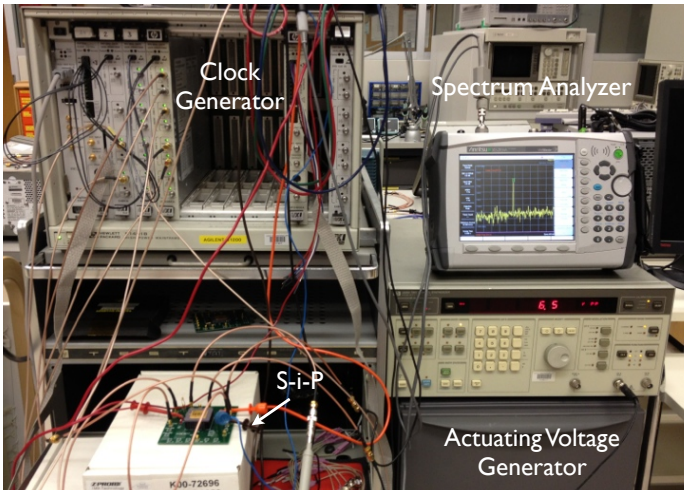

Figure 3.12: The actual test set up to obtain measurements for the S-i-P with each equipment identified.

cuit is measured using electrostatic forces. The amplitude of the actuating voltage is varied from 2.5 V to 6.5 V, producing the corresponding electrostatic force according to (3.19). It should be noted that, in order to measure the sensitivity, the actuating frequency is kept at 50 Hz (close to DC). Note that the applied actuating voltage needs to be under 7.58 V, which is the pull-in voltage of the accelerometer (Table 3.1). Since the actuating voltage is known, the electrostatic equivalent acceleration can be calculated as a_{el} = F_{el}/m. The measured acceleration to the output voltage relationship is plotted in Fig. 3.13. The probe connected to the output has a 10× attenuation, and thus the circuit exhibits a sensitivity of 144 mV/g. Moreover, the device is tilted vertically for the steady-state measurement of ±1g. At +1 g, the output voltage is at ∼2.65 V, whereas at -1 g, the output voltage is at ∼2.35 V.

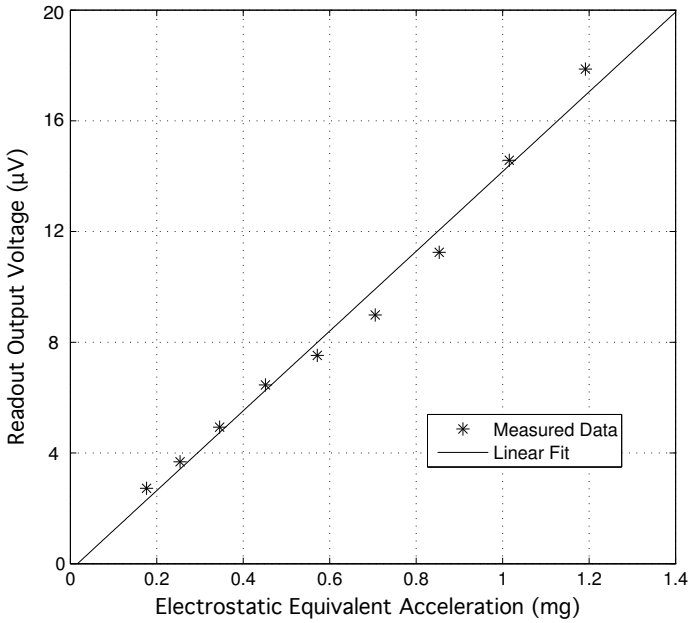

Figure 3.13: The relationship between electrostatic equivalent acceleration (a_{el}) in terms of g to the sensor output voltage. Note that the probe has a $10\times$ attenuation.

3.4.3 Signal of Interest and Noise Floor

The signal and noise measurements are conducted using a spectrum analyzer from Anritsu MS2034A. As previously mentioned, the signal of interest, namely, ΔC (or equivalently, acceleration), can be separated from the feed-through signal in the frequency domain. The test input acceleration is generated by an electrostatic force that is produced through an actuating AC voltage. The AC voltage has an amplitude of 6.5 V and is varying at 250 Hz. Therefore, the electrostatic equivalent acceleration would have an amplitude of 1.2 mg with a frequency of 500 Hz. Fig. 3.14 shows the output spectrum with the aforementioned input acceleration. It can be seen that

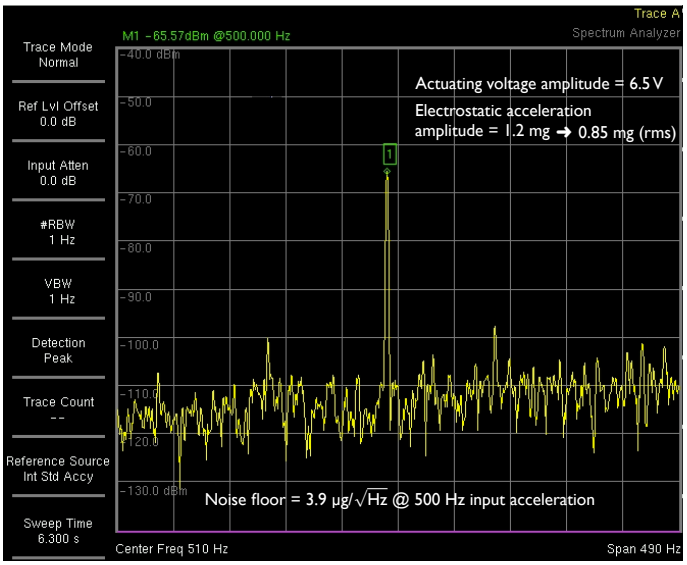

Figure 3.14: The spectra of the S-i-P output under sinusoidal input acceleration of 1.2 mg at 500 Hz (RBW = VBW = 1 Hz).

the output noise power spectral density is 50 dBm below the signal level at about -115 dBm, which corresponds to an acceleration noise floor of 3.9 $\mu g/\sqrt{Hz}$ and a capacitance noise floor of 0.05 aF$/\sqrt{Hz}$.

3.4.4 Electrostatic Spring Softening

The electrostatic spring-softening phenomenon was also observed. Equation (3.18) shows that the overall spring constant under the influence of electrostatic force is:

$$k_{overall} = k - \frac{\epsilon_0 A}{d_0^3} V_b^2 \tag{3.20}$$

Since the resonant frequency of the accelerometer is equal to $\sqrt{k_{overall}/m}$,

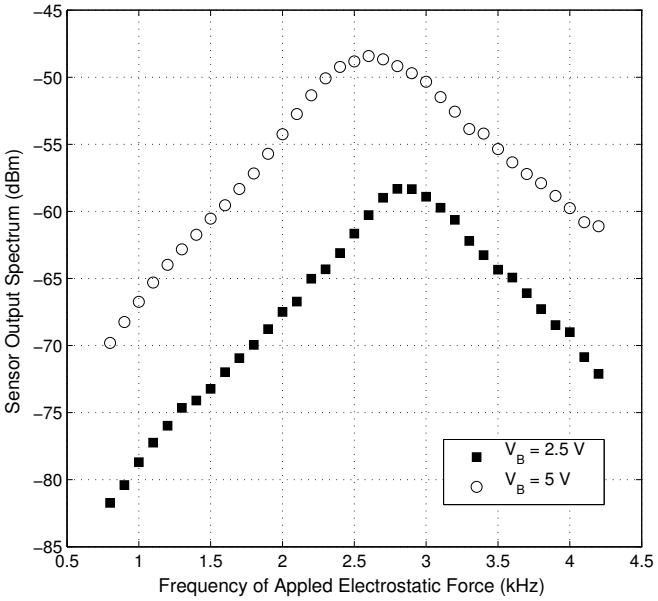

Figure 3.15: The effect of electrostatic spring softening is demonstrated here: when the actuating voltage increases from 2.5 V to 5 V, the resonant frequency of the accelerometer decreases.

if the amplitude of V_b (denoted as V_B) is increased, the resonant frequency should decrease. This effect is measured and shown in Fig. 3.15.

3.4.5 Device Performance Summary

The measured performance parameters are summarized in Table 3.3. The key parameters of interest are the acceleration noise floor and the power consumption as the noise floor sets the minimum acceleration that the system can sense, and the power optimization is always important, particularly for portable designs.

Note that the low acceleration noise floor of this work is a result of careful

Table 3.3: Performance Summary

Parameter	**This Work**
Sensitivity (mV/g)	144
Acceleration noise floor ($\mu g/\sqrt{Hz}$)	3.9
Capacitive noise floor (aF/$\sqrt{Hz}$)	0.05
Freq. where noise is measured (Hz)	500
Technology (μm)	0.8
Supply (V)	5
Power (mW)	4

design of both MEMS sensor and the sensor readout circuit. Special care has been paid to minimize the noise of the readout circuit and its input-referred capacitance noise floor (measured in aF/$\sqrt{Hz}$). Also, the sensor is designed to have a high capacitance to acceleration ratio (measured in capacitance per g). The input-referred capacitance noise floor of the design is 0.05 aF/$\sqrt{Hz}$. The high capacitance to acceleration ratio of 13 fF/g contributes to the low overall input-referred acceleration noise. The high capacitance to acceleration ratio of the sensor originates from the thick proof mass of the device. For instance, the proof mass of the sensor used in this work is 59.1 μgm, as opposed to the 0.932 μgm proof mass reported in [91]. The size of the proof mass is also an important factor in MEMS sensor design, as the capacitance to acceleration ratio increases with the device thickness, and furthermore, smaller gaps between the comb fingers increase the net capacitance. The accelerometer used here uses a device thickness of 25 μm, which is relatively large compared to that of the comparable designs. We have measured 4 different chips and chip to chip performance variation is within $\pm$2%.

3.5 Chapter 3 Conclusion

A switched-capacitor charge-transfer interface circuit with DC-offset cancellation for MEMS capacitive micro-accelerometers is presented. It is shown that the proposed circuit is insensitive to parasitic capacitances as well as sensor mismatches. Additionally, the readout circuit utilizes CS to further reduce op amp offset and low-frequency noise. The CMOS readout and the micro-accelerometer are integrated in a package for testing. The electrostatic force testing methodology is utilized. The measured acceleration and capacitance noise floor for the readout are 3.9 $\mu g/\sqrt{Hz}$ and 0.05 aF$/\sqrt{Hz}$ at input frequency of 500 Hz, respectively. The sampling clock runs at 10 kHz and the SiP consumes 4 mW.

Chapter 4

A Low-Noise Chopper-Stabilized Capacitive-Sensor Readout Circuit Using Correlated-Level-Shifting Technique

Various MEMS capacitive sensing interface circuits have been designed in both academia and industry in which two particular circuit design techniques have been widely used, namely, chopper stabilization (CS) and correlated double sampling (CDS) [96]. As discussed in Chapter 2.3, the main purpose of both techniques is to minimize low-frequency imperfections such as DC offset of the op amp and its flicker ($1/f$) noise. For CS, the low-frequency input signal is first modulated to a higher frequency where the effect of flicker

$(1/f)$ noise is negligible (as compared to the thermal noise). The signal is processed and is demodulated back to the baseband after amplification, and is then filtered to attenuate the out of band noise. In terms of CDS, typically the circuit uses two phase clocking where the op amp DC offset and low-frequency noise are sampled in one phase, and their effects are subtracted in the next phase.

In this chapter, a CMOS capacitive readout circuit for low-power MEMS inertial sensing applications is proposed to improve the overall accuracy and power consumption of the sensory system by incorporating a recently introduced switched-capacitor (SC) technique called correlated level shifting (CLS) in conjunction with CS. CLS is used to reduce errors from finite op amp gain while introducing negligible kT/C noise [98]. Given the same op amp performance, a circuit with CLS is able to achieve a higher accuracy and lower power consumption compared to those without CLS. Compared to CDS, which is commonly used in capacitive-sensor readouts, e.g., [93], an extra clock phase is required for CLS. However, for many sensor readout applications, where the speed that the circuit operates at is not very high (e.g., in kHz range), the extra clock phase would not cause a significant speed disadvantage. Moreover, it is demonstrated that CLS has significantly better noise performance than CDS at higher frequency. However, CDS does cancel very low-frequency noise and offset, whereas CLS does not [98]. Therefore, the CS technique is also incorporated to implement the capacitive-sensor front-end to not only reduce op amp errors due to its finite gain, but also cancel the aforementioned very low-frequency imperfections. Note that the concept of using CLS in conjunction with CS was first introduced in [99],

where it was applied to a $\Delta\Sigma$ analog-to-digital converter (ADC). In this work, these two techniques are combined for a sensor readout circuit, and moreover, the circuit structures used in [99] and this work are inherently different.

In order to verify the functionality of the readout circuit, in this work, the capacitive sensor is physically emulated by a pair of on-chip differential variable capacitors that are in the femto Farads range. The proposed front-end is designed in a 0.8 μm CMOS technology, and consumes 290 μW from a single 5V supply. The readout circuit achieves a capacitance noise floor of 0.018 aF/$\sqrt{Hz}$ at 400 Hz with a sensitivity of 50 mV/fF.

This chapter is organized as follows: an overview of CLS operation is described in Section 4.1, then the readout operation and non-idealities are discussed in Section 4.2, which shows the benefits of the proposed architecture. In Section 4.3, the readout circuit architecture and op amp structure are described in detail. Measurement results are presented in Section 4.4 and concluding remarks are provided in Section 4.5.

4.1 Overview of CLS Operation

CLS is a powerful SC technique that is intended to significantly reduce errors introduced by the finite op amp gain, thereby improving the overall accuracy of the circuit. The basic idea behind the error reduction phenomenon can be illustrated in Fig. 4.1 (a) and (b). Fig. 4.1 (a) shows an op amp used in an arbitrary feedback loop without CLS. The virtual ground error voltage (V_{error}) can be approximated to be $-V_o/A$, where V_o is the op amp output

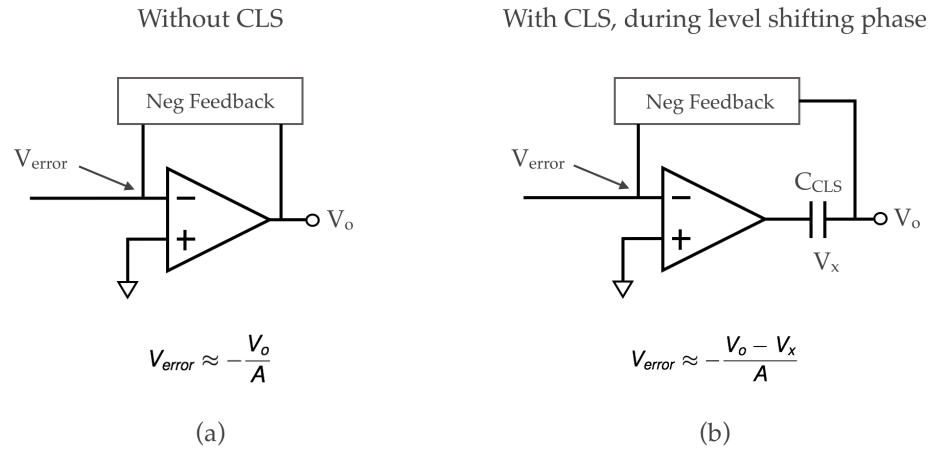

Figure 4.1: CLS virtual ground error voltage reduction analysis: (a) op amp circuit without CLS and (b) op amp circuit with CLS.

voltage shown in the Figure and A is the open-loop DC gain of the op amp. Traditionally, the error voltage V_{error} can be made smaller by making the op amp gain large, however, this would consume more power. Alternatively, the error can be reduced by making the voltage at the output of the op amp smaller. This is exactly what CLS does. As shown in Fig. 4.1 (b), with the CLS technique used (having a level shifting capacitor C_{CLS}), at the critical phase, the error voltage V_{error} is reduced because the output of the op amp is $V_o - V_x$. This indicates that the virtual ground error has become:

$$V_{error} \approx -\frac{V_o - V_x}{A} \tag{4.1}$$

Equation (4.1) demonstrates that the error voltage V_{error} can be significantly reduced by using CLS.

A more detailed and mathematical discussion on the operation of the

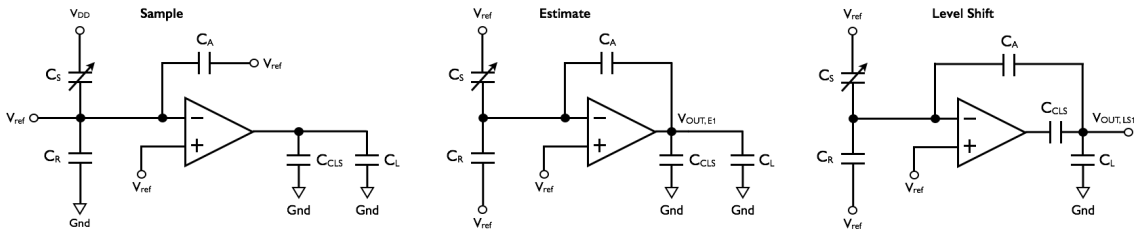

Figure 4.2: Operation of correlated level shifting (CLS). Three major clock phases are required for the circuit operation: sample, estimate, and level shift. Single-ended structure is shown for simplicity.

CLS technique is illustrated in Fig. 4.2, where a charge-transfer amplifier (capacitance-to-voltage converter) is used as an example. Note that single-ended circuit structure is used for the purpose of simplicity.

As it can be seen in the figure, CLS consists of three clock phases: sample, estimate, and level shift. C_S models the MEMS capacitive sensor (for the purpose of the discussion, this sensor can be treated as a varactor). This variable sensing capacitor can be written as: $C_S = C_0 + \Delta C$ where typically $\Delta C \ll C_0$. The input to this circuit is the capacitance variation ΔC. In Fig. 4.2, C_R is the reference capacitor and is equal to C_0. C_A is the feedback capacitor that dictates the sensitivity of the charge-transfer amplifier. C_{CLS} is the capacitor used in CLS to reduce the op amp finite gain error and its purpose is described in detail in [98]. The output at the end of the estimation phase is:

$$V_{OUT,E1} = \left[\frac{V_{DD}}{2} + \frac{V_{DD}}{2}\left(\frac{\Delta C}{C_A}\right)\right]\left(\frac{1}{1+\frac{1}{K}}\right) \tag{4.2}$$

where K is the op amp loop gain during this clock phase, and can be expressed as:

$$K = \frac{AC_A}{C_S + C_0 + C_A} \approx \frac{AC_A}{2C_0 + C_A} \tag{4.3}$$

where A is the DC gain of the op amp. Note that $V_{ref} = 0.5V_{DD}$.
The output of interest happens in the level shifting phase and is denoted as $V_{OUT,LS1}$, which can be expressed as:

$$V_{OUT,LS1} = \left[\frac{V_{DD}}{2} + \frac{V_{DD}}{2}\left(\frac{\Delta C}{C_A}\right)\right]\left(\frac{1}{1 + \frac{1}{K_{EQ}}}\right) \tag{4.4}$$

where the equivalent loop gain K_{EQ} is:

$$K_{EQ} = \left(\frac{2 + \lambda + K}{1 + \lambda}\right)K \approx \frac{K^2}{1 + \lambda} \tag{4.5}$$

where λ represents the effect of finite CLS capacitor C_{CLS}, and can be expressed as:

$$\lambda = \frac{1}{C_{CLS}}\left(\frac{2C_0C_A}{2C_0 + C_A} + C_L\right) \tag{4.6}$$

Assuming that there is no charge loss in C_{CLS}, i.e., by making C_{CLS} much larger compared to the load C_L, the equivalent loop gain can be simplified:

$$K_{EQ} = K(2 + K) \approx K^2 \tag{4.7}$$

Equations (4.5) to (4.7) essentially demonstrate that CLS greatly increases the effective loop gain of the circuit. Due to this property, designers can also achieve the same target specifications using less power. Moreover, it can be shown that CLS has a very good noise performance because im-

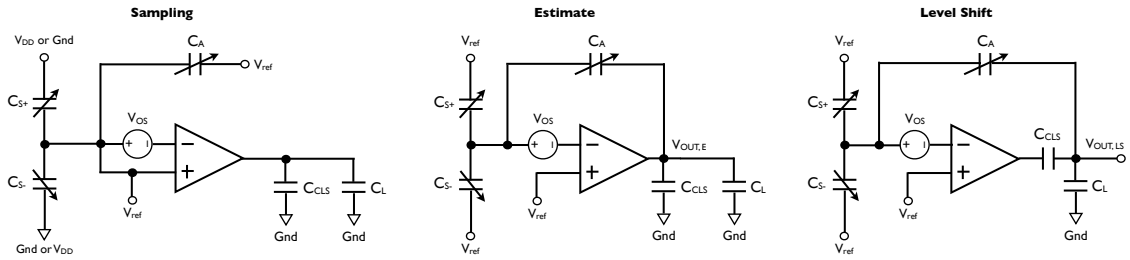

Figure 4.3: Operation of the proposed CS + CLS charge-transfer amplifier. Three major clock phases are required for the circuit operation: sample, estimate, and level shift. Note that the op amp offset model is included at the inverting input.

perfections such as thermal noise, charge injection, errors from finite swing, and incomplete settling that are sampled onto C_{CLS} during the estimation phase are reduced by the DC gain during the level shift phase. However, as previously mentioned, CLS does not cancel low-frequency noise and offset at the input of the op amp [98].

4.2 Readout Operation and Non-Idealities

The operating principle of the proposed CS plus CLS capacitive readout (charge-transfer amplifier) is shown in Fig. 4.3, where the circuit structure in each clock phase is displayed. The sampling clock waveforms are shown in Fig. 4.4, where three main clock phases are present: sample, estimate, and level shift (ignore $\phi_{LS,a}$ and $\phi_{LS,b}$ for now). It is important to note that due to the CS technique, the sampling clock is divided into two phases: ϕ_{Ca} and ϕ_{Cb}. During consecutive ϕ_{Ca} and ϕ_{Cb} sampling clock phases, the input capacitor structure is alternately charged with opposite voltage polarity. That

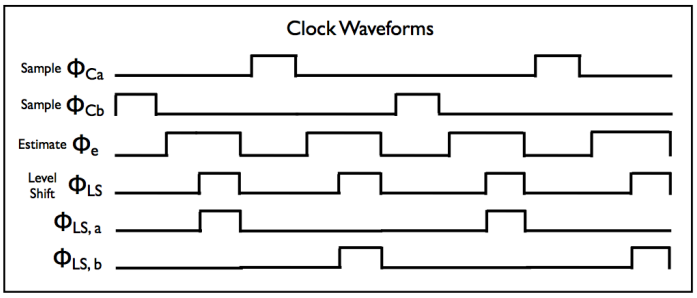

Figure 4.4: Clock waveforms governing the operation of the proposed CS + CLS charge-transfer amplifier.

is, during ϕ_{Ca}, C_{S+} is charged to $V_{DD} - V_{ref}$, and C_{S-} is charged to $-V_{ref}$. During the following ϕ_{Cb}, C_{S+} is charged to $-V_{ref}$, and C_{S-} is charged to $V_{DD} - V_{ref}$. Such operation enables the creation of an amplitude modulated (AM) signal at the output of the charge-transfer amplifier, where the peak-to-peak amplitude is proportional to the difference in the sensed (variable) capacitances. Note that the op amp input offset and the flicker noise mainly influence the DC voltage level of the output, but not the amplitude of the AC signal [97]. Therefore, the undesirable effects of such disturbances can be removed after the output is demodulated differentially. Also, note that, in this work, V_{ref} is equal to half of V_{DD}. The amplifier output at the end of the estimation phase, ϕ_e that follows ϕ_{Ca} (corresponding to the value of the capacitance during ϕ_{Ca}), is:

$$V_{OUT,E,\phi_{Ca}} = \left[\frac{V_{DD}}{2} + V_{os}\left(1 + \frac{2C_0}{C_A}\right) + \frac{V_{DD}}{2}\left(\frac{C_{S+} - C_{S-}}{C_A}\right)\right]\left(\frac{1}{1 + \frac{1}{K}}\right) \quad (4.8)$$

Similarly, the output signal at the end of the estimation phase, ϕ_e that follows ϕ_{Cb} (corresponding to the value of the capacitance during ϕ_{Cb}), is:

$$V_{OUT,E,\phi_{Cb}} = \left[\frac{V_{DD}}{2} + V_{os}\left(1 + \frac{2C_0}{C_A}\right) + \frac{V_{DD}}{2}\left(\frac{C_{S-} - C_{S+}}{C_A}\right)\right]\left(\frac{1}{1+\frac{1}{K}}\right) \quad (4.9)$$

where V_{os} is the offset of the op amp, C_A is the feedback capacitor, $C_{S+} = C_0 + \Delta C$ and $C_{S-} = C_0 - \Delta C$ (C_0 is the fixed nominal sensor capacitor). Additionally, K is the op amp loop gain during the estimation phase, and can be written as:

$$K = \frac{AC_A}{C_{S+} + C_{S-} + C_A} = \frac{AC_A}{2C_0 + C_A} \quad (4.10)$$

The output signals of interest for the proposed readout circuit are generated at the end of the level-shift phase:

$$V_{OUT,LS,\phi_{Ca}} = \left[\frac{V_{DD}}{2} + V_{os}\left(1 + \frac{2C_0}{C_A}\right) + \frac{V_{DD}}{2}\left(\frac{C_{S+} - C_{S-}}{C_A}\right)\right]\left(\frac{1}{1+\frac{1}{K_{EQ}}}\right) \quad (4.11)$$

$$V_{OUT,LS,\phi_{Cb}} = \left[\frac{V_{DD}}{2} + V_{os}\left(1 + \frac{2C_0}{C_A}\right) + \frac{V_{DD}}{2}\left(\frac{C_{S-} - C_{S+}}{C_A}\right)\right]\left(\frac{1}{1 + \frac{1}{K_{EQ}}}\right) \quad (4.12)$$

where the equivalent loop gain, K_{EQ}, is approximately K^2 as mentioned in (4.7). Note that this approximation is deduced from the fact that there is negligible charge loss from C_{CLS} since it is much larger than the load. As it can be seen, the equivalent loop gain is greatly improved, thus designers can reduce the gain specification of the op amp. Assuming the bandwidth requirement of the op amp remains the same, the amount of current needed to operate the circuit can also be reduced, leading to less power consumption.

Once the output of the charge-transfer amplifier is demodulated differentially, the final output (referred to ground) of the readout circuit can be expressed as:

$$V_{out} = V_{DD}\frac{2\Delta C}{C_A}\left(\frac{1}{1 + \frac{1}{K_{EQ}}}\right) \quad (4.13)$$

where any offset is canceled because V_{out} is essentially the difference between equations (4.11) and (4.12). It can be seen from (4.13) that the accuracy of the output is closely related to parameter $K_{EQ} \approx K^2$. Assuming A is fixed and finite, K_{EQ} can be maximized if C_A approaches infinity. However, the larger C_A is, the less sensitivity (Volts/Farads) the circuit can achieve. Therefore, the designer should take this trade-off into account. Moreover, the nominal sensor capacitor, C_0, is application dependent, as

different sensors have different nominal capacitances. Therefore, one can make the readout circuit more versatile by having the ability to vary C_A, which in turn, would allow the circuit to have different gain settings. This way, the interface circuit can be used for a wider range of capacitive sensors. In the proof-of-concept chip implemented in this work, C_A is realized as a bank of 3 capacitors and can be programmed to be 200, 400, or 600 fF.

In terms of noise, similar to the analysis presented in [98], we can derive that the CLS network adds the following amount of noise to the circuit:

$$V_n^2 \approx \frac{\left(1+\frac{2C_0}{C_A}\right)^2 V_{n,opamp}^2 + \frac{kT}{C_{CLS}}}{A^2} \tag{4.14}$$

where $V_{n,opamp}$ is the op amp noise that is sampled onto C_{CLS}, k is the Boltzmann constant, and T is the absolute temperature in Kelvins. Equation (4.14) shows the advantage of using CLS (as discussed in [98]): imperfections such as thermal noise, charge injection, errors from finite op amp gain, and incomplete settling that are sampled onto C_{CLS} during the estimation phase are reduced by the DC gain during the level-shift phase.

4.3 Readout Architecture and Op Amp Structure

The schematic of the overall CMOS readout circuit and the variable capacitive element (in the form of bank of capacitors) mimicking the sensor are shown in Fig. 4.5 and Fig. 4.6, respectively. The front-end circuit (Fig. 4.5) is composed of chopping switches, a CLS charge-transfer amplifier, sample and hold (S/H) buffers that act as a demodulator, and finally an externally

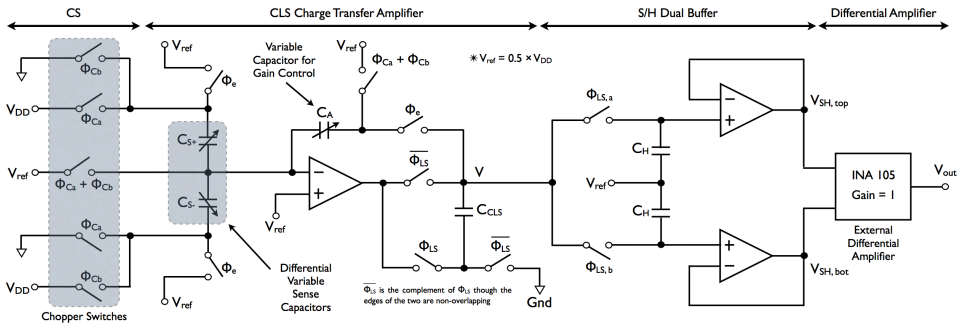

Figure 4.5: Schematic of the proposed capacitive readout circuit which consists of variable capacitors (to mimic the capacitive sensor), switches for chopper stabilization, CLS charge-transfer amplifier, S/H buffers and an externally connected unity gain differential amplifier (INA 105) for measurement purposes.

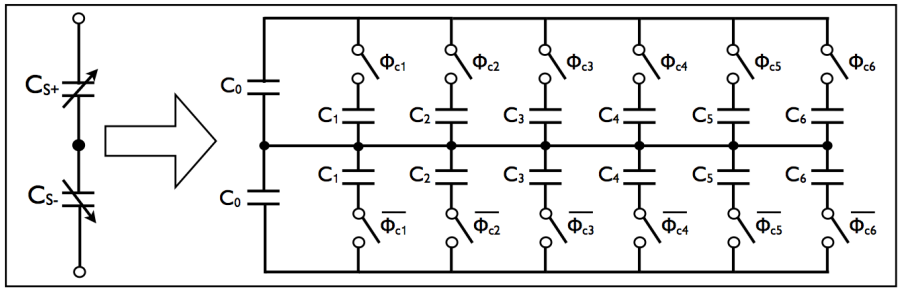

Figure 4.6: Digitally controlled bank of capacitors to mimic the MEMS capacitive sensor.

connected unity gain differential amplifier (INA 105) that is used to facilitate the measurement of the output noise and the output signal. In order to test the interface circuit, the MEMS capacitive sensor is emulated by a pair of on-chip differential variable capacitors C_{S+} and C_{S-}, where each C_{S+} and C_{S-} consists of a fixed nominal capacitor C_0 in parallel with 6 capacitors (C_1 to C_6) that can be selectively switched in via their control

switches (Fig. 4.6). Note that to test different ranges of capacitance variations, 3 different capacitor banks are used (only one is shown in Fig. 4.6). It is also important to note that C_1 to C_6 are equal in each set. Moreover, C_0 has a nominal value of 200 fF, while the value of C_1 for each set is 2 fF, 4 fF, and 8 fF, respectively. The change in capacitance is first converted to a charge and subsequently goes through the charge-transfer amplifier using CLS. The output of the charge-transfer amplifier is a voltage signal that is proportional to ΔC as explained in Section 4.2. Such output is fed to the S/H stage followed by an (off-chip) unity gain differential amplifier (INA 105) which converts the output differential signals of the S/H stage into a single-ended one. Note that, in practice, such differential amplifier is not necessary, since typically the output of the S/H stage is directly fed into an ADC having differential inputs.

The schematic of the op amp used in all of the building blocks is shown in Fig. 4.7. This op amp uses the folded-cascode topology and has a DC open-loop gain of 68.1 dB, a phase margin of 61.9°, and a gain-bandwidth of 2.5 MHz with an output compensation capacitor of 5 pF. It consumes 88 μW from a 5-V supply and has an output swing of 3.25 V. Additionally, the bias for the op amp is supplied externally.

The flicker noise associated with the op amp is given by [89]:

$$\overline{v_{n,flicker}^2} \approx \frac{K_f}{C_{ox}WL}\frac{1}{f} \tag{4.15}$$

where K_f is the flicker noise coefficient that is a process-dependent parameter, C_{ox} is the oxide capacitance per unit area, and f is the frequency. W

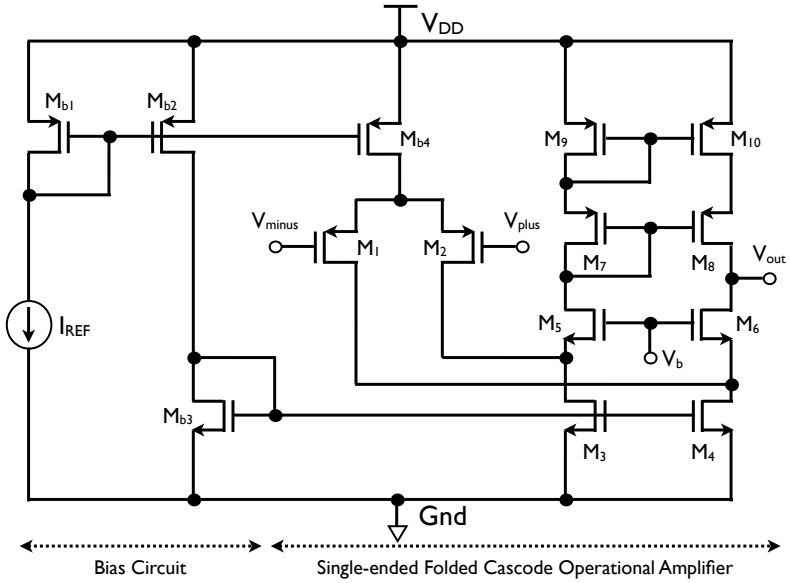

Figure 4.7: The schematic of the folded-cascode op amp that is implemented to minimize thermal and flicker noise.

and L denote the width and length of the input differential pair, respectively. For this design, a PMOS input pair is chosen because in the technology used in this work, the flicker noise coefficient of PMOS devices is lower than that of their NMOS counterparts. Additionally, to reduce the flicker noise, W is chosen to be relatively large (i.e., 100 μm). This large W will result in a large g_m (i.e., $\sim$78 μS) which as explained below will result in lower thermal noise.

The thermal noise ($\overline{v^2_{n,thermal}}$) of the folded-cascode amplifier can be expressed as [89]:

$$\frac{\overline{v^2_{n,thermal}}}{\Delta f} \approx 2\left(4kT\frac{2}{3g_{m1}}\right)\left(1+\frac{g_{m3}}{g_{m1}}+\frac{g_{m9}}{g_{m1}}\right) \tag{4.16}$$

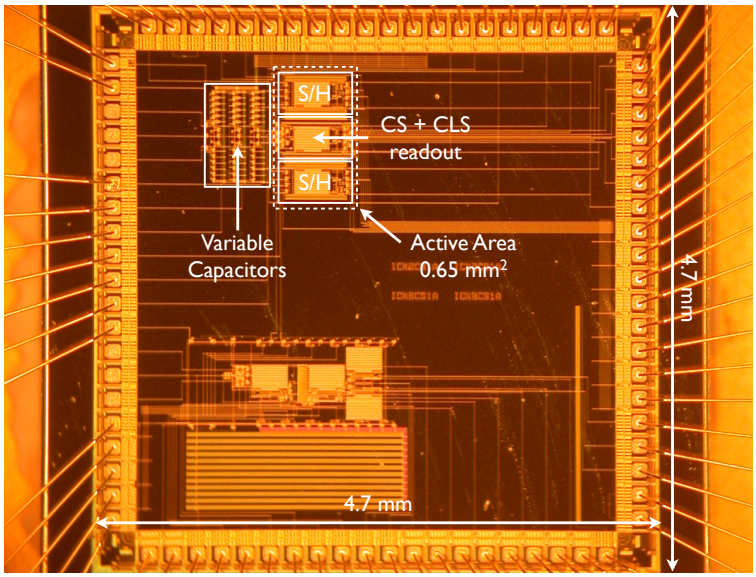

Figure 4.8: Micrograph of the test chip in 0.8 μm CMOS.

where g_m is the transconductance of the corresponding transistor. From (4.16), one can conclude that the thermal noise can be optimized if the transconductance of the input transistors (g_{m1}) are maximized, and the transconductance of the current mirror transistors (i.e., g_{m3} and g_{m9}) are minimized. In this work, g_{m1}, g_{m3}, and g_{m9} are ~78 μS, ~46 μS, and ~20 μS, respectively.

4.4 Measurement Results

The proposed capacitive readout circuit is fabricated in a 0.8 μm CMOS technology. The chip has an active area of 0.65 mm^2 and its micrograph is shown in Fig. 4.8. As explained earlier, to emulate the sensor differential capacitance, on-chip banks of capacitors are used in pairs. The test setup is

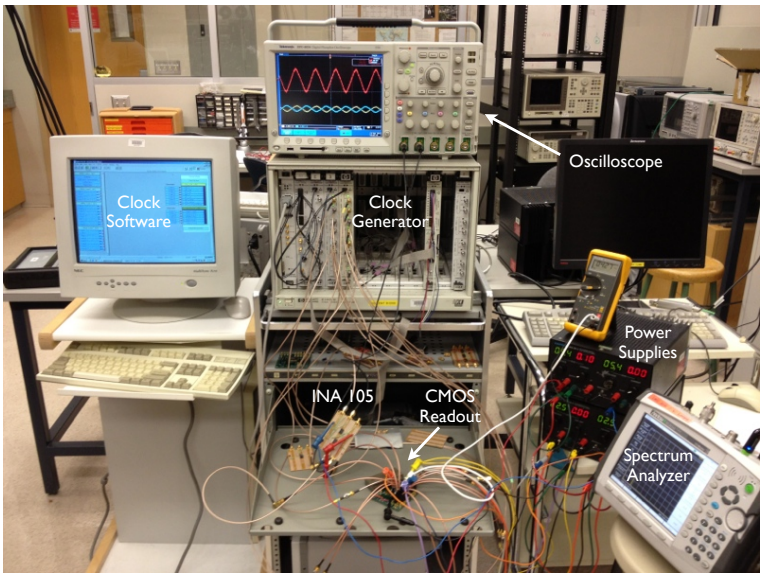

Figure 4.9: The test setup that is implemented to obtain important measurement results. Each equipment in the figure is identified in white text.

shown in Fig. 4.9 where each test equipment is also identified. The required clocks and capacitance control signals are generated by an Agilent 81200 data generator. The sampling clock runs at 100 kHz, and the capacitance control signals vary at roughly 400 Hz. The measured time domain response of the readout circuit at C_A = 200 fF with a differential capacitance variation of 24 fF (ΔC = 12 fF) running at ~400 Hz is shown in Fig. 4.10. Note that the green and blue signals are the outputs of the S/H buffers ($V_{SH,top}$ and $V_{SH,bot}$ in Fig. 4.5). The red signal is the difference between the two S/H outputs, and it has an amplitude of 0.6 V. The measured sensitivity (voltage variation in response to capacitance variation) of the prototype at different gain settings is plotted in Fig. 4.11. It can be seen that the circuit has a maximum gain of 50 mV/fF when C_A is equal to 200 fF. Fig. 4.12

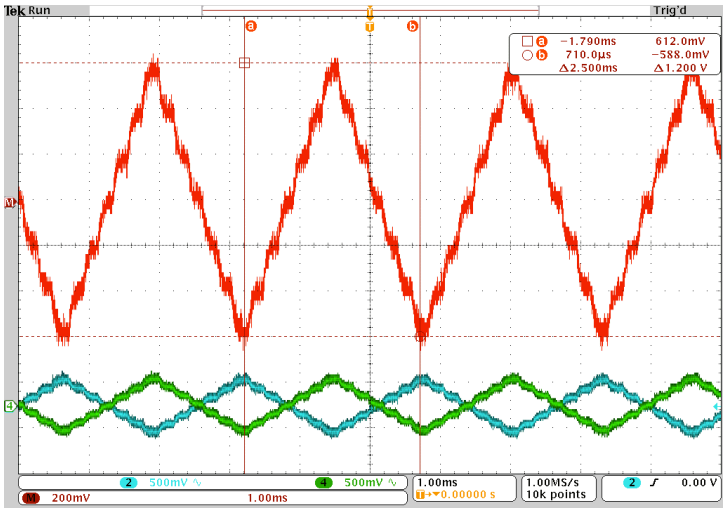

Figure 4.10: Differential output (in red) of the CMOS readout circuit with respect to a differential capacitance variation of 24 fF changing at approximately 400 Hz.

shows the output spectrum of the readout circuit when an input is applied at approximately 400 Hz. As it can be seen, the noise floor at the vicinity of 400 Hz is −111 dBm, which can be converted to 0.891 $\mu V/\sqrt{Hz}$. The capacitance noise floor can then be calculated using the maximum sensitivity of the interface circuit to be 0.018 aF$/\sqrt{Hz}$. The noise performance is expected to remain relatively the same if the readout circuit is implemented with a MEMS sensor in a single chip. A summary of the measured performance parameters in this design is shown in Table 4.1, where a comparison with other works [90, 91, 100–102] is also presented. It is important to note that, although the presented readout circuit compares favourably to other works in terms of its power consumption, a few of the latter designs include more on-chip circuitry such as clock generators and filters.

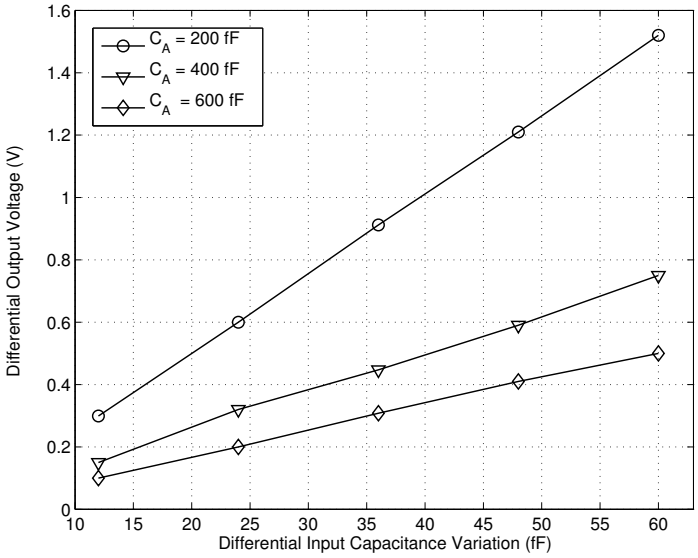

Figure 4.11: Measured sensitivity of the CMOS readout circuit at different gain settings. The measured output voltage indicates the AC amplitude.

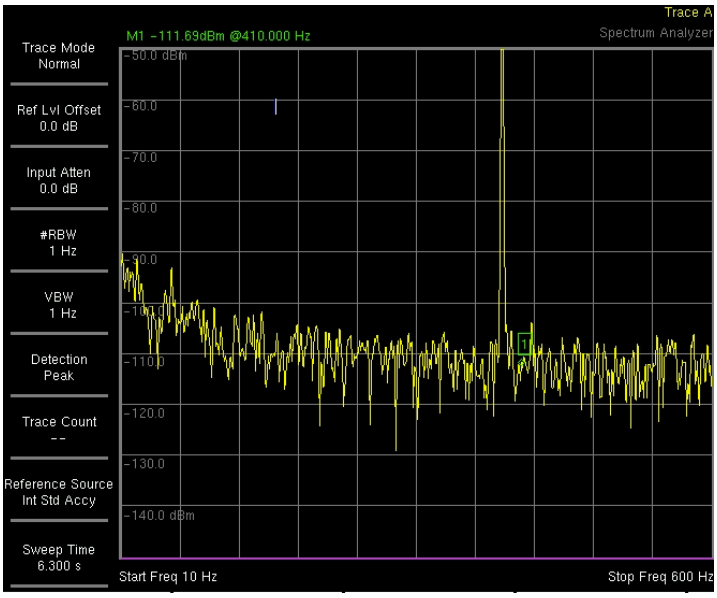

Figure 4.12: The spectrum of the output from 10 to 600 Hz when the input is applied at about 400 Hz. The capacitance noise floor is 0.018 aF/$\sqrt{Hz}$.

Table 4.1: Performance Summary and Comparison

Parameter	**This Work**	**[90]***	**[91]***	**[100]**	**[101]***	**[102]**
Capacitive noise floor (aF/$\sqrt{Hz}$)	0.018	0.02	0.016	0.2	0.19	0.42
Frequency where noise is measured (Hz)	400	400	400	N/A	average from 0 to 300	3
Clock (kHz)	100	1000	500	1000	6	600
Technology (μm)	0.8	0.5	0.35	0.35	0.35	0.6
Supply (V)	5	5	3.3	5	2.5 – 3.6	3
Power (mW)	0.29	30	2.57	5	1 – 1.44	3.75

*These designs include more on-chip circuitry such as clock generators and filters.

4.5 Chapter 4 Conclusion

A differential low-power low-noise CMOS readout circuit intended for MEMS capacitive sensors is presented. The circuit utilizes techniques such as correlated level shifting and chopper stabilization to reduce the adverse effects of op amp finite gain as well as DC offset and low-frequency noise. In this work, on-chip banks of capacitors are used to physically emulate the MEMS capacitive sensor. The capacitances are varied via control clock signals. The circuit achieves a maximum sensitivity of 50 mV/fF. The capacitance noise floor for the readout is 0.018 aF/$\sqrt{Hz}$ at 400 Hz. The sampling clock runs at 100 kHz and the overall interface consumes 290 μW.

Chapter 5

A 14-bit $\Sigma\Delta$ CMOS MEMS Capacitive Sensor Interface Using Modified Correlated Level Shifting

As discussed in the previous chapter, several MEMS capacitive sensing interface circuits have been proposed in the literature, where two particular circuit design techniques have been widely used. These are the chopper stabilization (CS) and the correlated-double-sampling (CDS) techniques [96]. Both techniques are used to reduce the offset and the low-frequency noise, e.g., $1/f$ noise of the op amp. Additionally, a relatively recent circuit technique, correlated level shifting (CLS), that aims to minimize the op amp finite gain error is also introduced in [98], and used in [4] as a sensor readout circuit. The heart of the previous chapter is essentially the combination of CLS and CS such that the readout circuit improves its accuracy, noise floor, and power performance. Note that the need to use CS is due to the fact that CLS does not cancel offset or very low frequency noise.

In this chapter, a SC sensor interface front-end circuit based on a variation of CLS is proposed to retain the features associated with the readout circuit in the previous chapter, without the need to use CS. In other words, the proposed interface front-end in this chapter uses a single modified correlated level shifting technique to not only minimize the op amp finite gain error, but also reduce low frequency imperfections associated with the op amp. This modified CLS technique therefore improves the noise and power performance of the circuit simultaneously.

To complete the sensor readout system, a back-end first-order 14-bit ΣΔ ADC is interfaced with the front-end circuit to provide a 1-bit pulse-width modulated (PWM) digital signal at the system output. As opposed to the previously reported sensor readout architectures, in which the MEMS sensor is directly connected to the integrator block of a ΣΔ modulator [18, 66], the presented system architecture has the front-end circuit block that converts the change in capacitance to voltage, followed by the back-end ADC that digitizes the amplified analog voltage signal from the front-end to a 1-bit output digital stream. The advantage of this architecture is the decoupling of the modulator from the sensor to achieve optimized performance independent of the sensor capacitance [93].

The content of this chapter describes a fully differential low-noise SC readout circuit that is intended for MEMS capacitive inertial sensors. The overall system architecture consists of two main sections: the front-end block and the back-end block. The front-end circuit consists of the sensor and the charge-transfer amplifier (capacitance-to-voltage converter) that uses a variation of correlated level shifting (CLS) technique to reduce the op amp

finite gain error as well as to minimize the effects of op amp offset and low-frequency noise. The output at the charge-transfer amplifier is smoothened out by a S/H stage. The back-end block consists of an anti-aliasing filter (AAF) followed by a 14-bit first-order $\Sigma\Delta$ ADC. The readout circuit is designed and laid out in a 0.8 μm CMOS process. For the purpose of simulations, the MEMS capacitive sensor is emulated by a pair of differential variable capacitors in Verilog-A. Post-layout simulation results demonstrate that the circuit achieves a capacitance noise floor of $\sim$0.25 aF/$\sqrt{Hz}$ at 500 Hz with a sensitivity of 12.42 mV/fF. The circuit consumes 1 mW from a single 5 V supply.

This chapter is organized as follows: the theory of operation of the proposed modified CLS is discussed in Section 5.1, where a simple single ended capacitive sensor readout circuit is used as an example. In Section 5.2, the overall sensor system architecture is first introduced and described, followed by detailed discussions on the front-end and back-end circuit blocks that make up the whole system. Post-layout simulation results are reported in Section 5.3 and the concluding remarks are provided in Section 5.4.

5.1 Modified CLS Theory of Operation

As discussed in the previous chapter (Chapter 4), in regards to the original CLS, while it possesses the loop gain boosting characteristic while introducing negligible noise, it has poor offset/very low-frequency noise performance. Please refer to Chapter 4 for detailed discussion on the operation of CLS.

Therefore, we propose to slightly modify the original CLS so that the

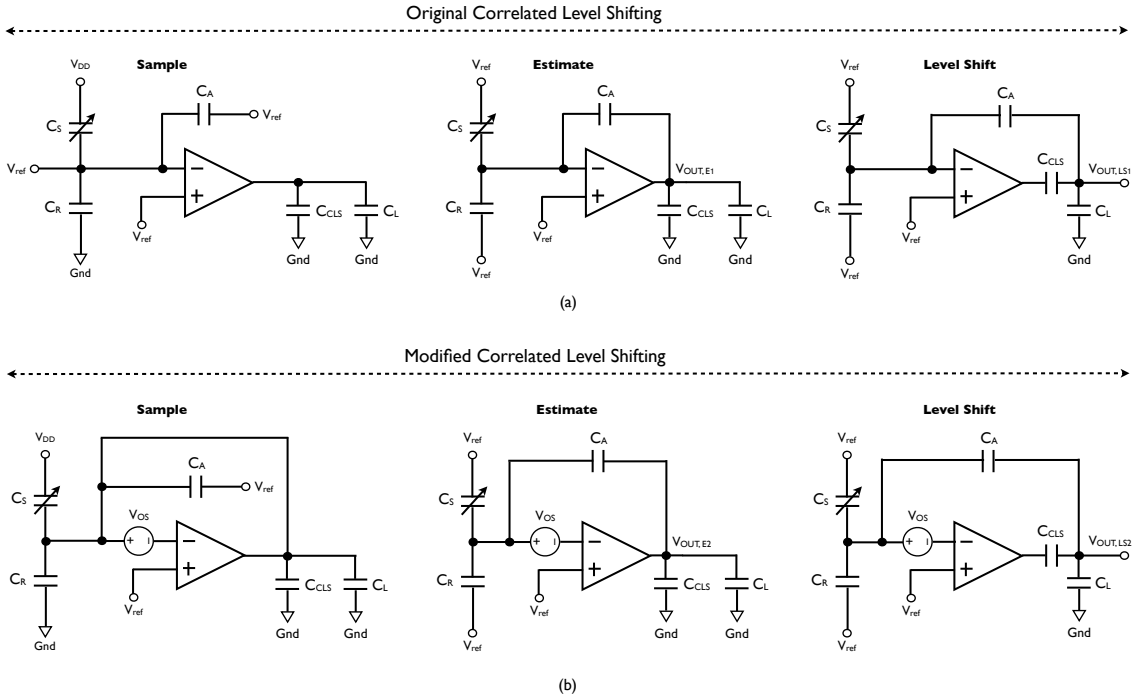

Figure 5.1: (a) Operation of correlated level shifting (CLS). (b) Operation of modified correlated level shifting (MCLS). Single-ended structure is shown for simplicity.

modified version is able to reduce offset and low-frequency noise while keeping the original advantages. Fig. 5.1 (a) and (b) shows both the original CLS and the modified CLS (MCLS) in capacitive sensor readout application. To briefly introduce both circuits in Fig. 5.1, C_S models the MEMS capacitive sensor (in this work, C_S is described using Verilog-A). This variable sensing capacitor can be written as: $C_S = C_0 + \Delta C$ where typically $\Delta C \ll C_0$. C_R is the reference capacitor and is equal to C_0. C_A is the feedback capacitor that dictates the sensitivity of the readout circuit. C_{CLS} is the capacitor used in CLS to reduce the op amp finite gain error and its purpose is described in

detail in Chapter 4.

The operating principle of the proposed MCLS is shown in Fig. 5.1 (b), where an input-referred voltage offset V_{os} of the op amp is included in the figure. Note that V_{os} can also represent very low-frequency noise as an approximation. The only difference between the two approaches (original CLS and modified CLS) is in the sampling phase. For the variant of CLS proposed in this work, instead of connecting the inverting input of the op amp to a DC source, a connection is made between the inverting node of the op amp to the output of the op amp, forming a negative feedback network. In this way, the offset of the op amp can be sampled onto C_A in the sampling phase, and subsequently its value can be subtracted from the signal in the next phases (CDS principle). The output at the end of the estimation phase can be written as:

$$V_{OUT,E2} \approx \left[\frac{V_{DD}}{2} + \frac{V_{os}}{K} + \frac{V_{DD}}{2}\left(\frac{\Delta C}{C_A}\right)\right]\left(\frac{1}{1+\frac{1}{K}}\right) \tag{5.1}$$

where K is the opamp loop gain during this clock phase, and can be expressed as:

$$K = \frac{AC_A}{C_S + C_0 + C_A} \approx \frac{AC_A}{2C_0 + C_A} \tag{5.2}$$

In equation (5.2), A is the DC gain of the op amp. Also note that $V_{ref} = 0.5V_{DD}$.

The output at the end of the level shift phase (output of interest) can be written as:

$$V_{OUT,LS2} \approx \left[\frac{V_{DD}}{2} + \frac{V_{os}}{K} + \frac{V_{DD}}{2}\left(\frac{\Delta C}{C_A}\right)\right]\left(\frac{1}{1+\frac{1}{K_{EQ}}}\right) \tag{5.3}$$

where the equivalent loop gain K_{EQ} can be approximated as:

$$K_{EQ} = K(2+K) \approx K^2 \tag{5.4}$$

where the assumption lies within the fact that there is no charge loss in C_{CLS}. This point has also been discussed thoroughly in Chapter 4 (Equation (4.5) to (4.7)).

As it can be seen from both (5.2) and (5.3), if the proposed modification is applied, the op amp offset is reduce by a factor of K, which can be maximized if C_A approaches infinity (assuming A is fixed). However, the sensitivity of the circuit (Volts/Farads) is inversely proportional to C_A, so if large sensitivity is a requirement in the system specification, then the designer should take this trade-off into account. On the other hand, the overall effective loop gain is still equal to K_{EQ}, which is approximately K^2. This shows that the MCLS still has the benefits from the original CLS.

5.2 CMOS Interface Circuit Architecture

The overall system architecture of the designed fully differential sensor interface circuit can be found in Fig. 5.2. As it can be seen in the figure, the sensor is directly connected to the front-end circuits, where a SC charge transfer amplifier is used to convert the changing charge of the capacitive MEMS sensor to an amplified voltage representing the physical signal of

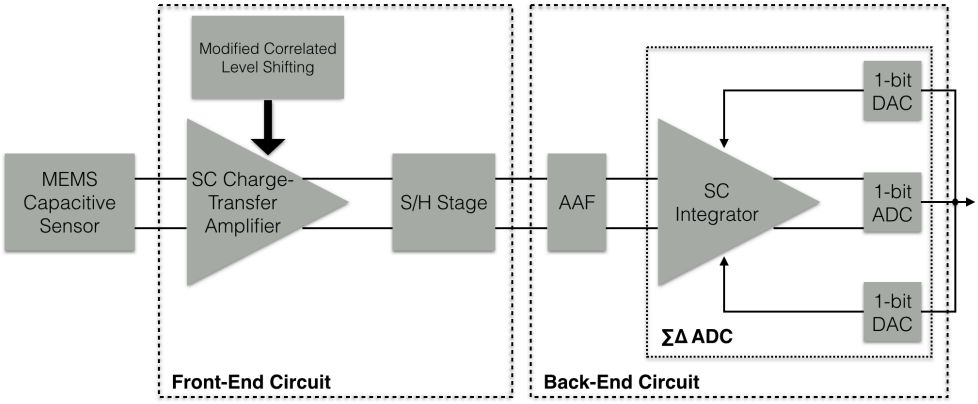

Figure 5.2: The overall sensing interface architecture with the physical sensor, front-end and back-end circuits. The front-end includes a modified correlated level shifting charge-transfer amplifier and a S/H stage while the back-end circuit includes an AAF plus a first-order ΣΔ ADC

interest. Note that the charge transfer amplifier uses the modified CLS as discussed in the previous section.

The voltage at the output of the charge transfer amplifier is sampled and subsequently enters the back-end circuit block. The first stage of the back-end circuitries is an anti-aliasing filter (AAF) that filters out high frequency components of the signal such that the signal is more band-limited and is free of aliasing. The second stage of the back-end circuits is a first order SC ΣΔ ADC that consists of an integrator, followed by a comparator (1-bit quantizer) and a 1-bit feedback DAC. As mentioned previously, this configuration decouples the ΣΔ modulator from the sensor capacitors such that the size of the sensor capacitances does not affect overall system performance. Moreover, the front-end can be clocked (sampled) at a much lower frequency compared with the back-end, as this is particularly useful when

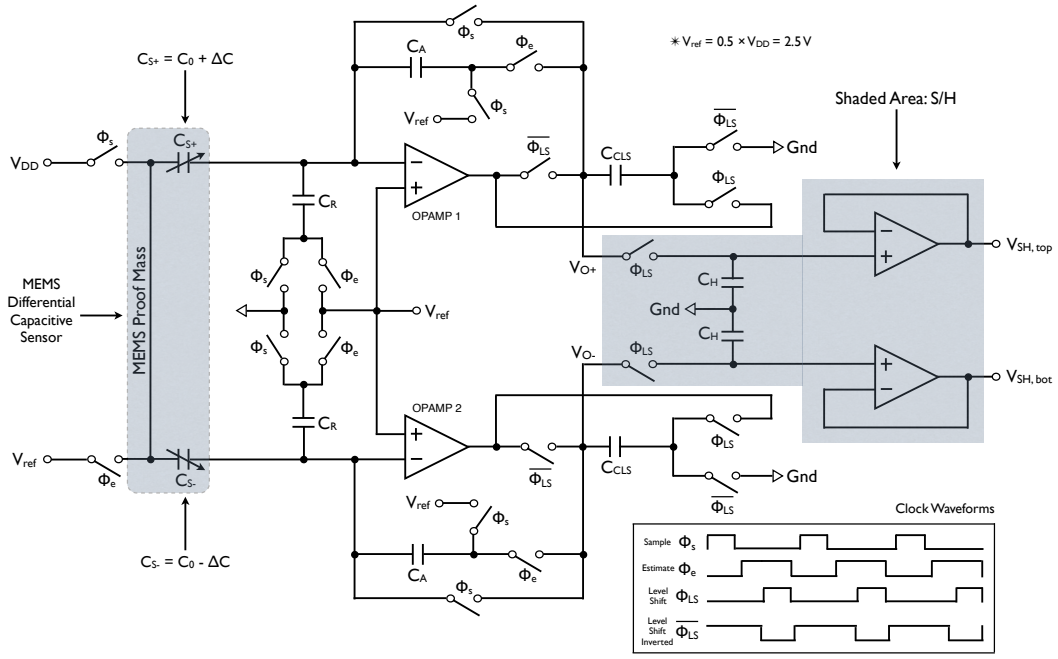

Figure 5.3: Schematic of the proposed capacitive readout front-end circuit which consists of variable capacitors (to mimic the MEMS sensor), modified CLS charge-transfer amplifier, and S/H dual buffers. The clock waveforms are also included in this figure.

the sensor capacitance is large (large time constant). The CMOS readout is implemented in fully differential fashion to reduce common mode interference (substrate and supply noise), and to increase the dynamic range. In the following subsections, each of the above mentioned blocks will be discussed in more detail.

5.2.1 Front-End Circuit Block

As it can be seen in Fig. 5.2, the front-end of the interface circuit consists of a SC charge-transfer amplifier followed by a S/H stage. The detailed

schematics of the front-end is shown in Fig. 5.3, where three major building blocks can be identified: a MEMS differential capacitive sensor, the proposed fully differential charge-transfer amplifier that uses modified CLS (MCLS), and a sample-and-hold (S/H) output stage. The MEMS capacitive sensor is essentially a three terminal device, where two of the terminals are connected to the inverting input of the op amps (OPAMP1 and OPAMP2), and the third is the proof mass. The variable capacitors C_{S+} and C_{S-} are differential and can be expressed as $C_{S+} = C_0 + \Delta C$ and $C_{S-} = C_0 - \Delta C$. It is important to note that this readout front-end theoretically can be interfaced with any types of capacitive differential sensor as long as the feedback capacitor C_A is programmable and can be matched with the nominal sensor capacitance.

The capacitance variations from the sensor are first converted into charges that are transferred onto the feedback capacitors C_A, and are amplified through the charge-transfer amplifier. The resulting output is in voltage. The operating principle of such charge-transfer amplifier is explained in Section 5.1 in the context of a single-ended circuit. The clocks shown in Fig. 5.3 essentially divide the system into three classical CLS phases: sample, estimate, and level shift. Note that the valid outputs V_{O+} and V_{O-} appear at the end of the level shift phase. The aforementioned outputs are fed to the S/H stage to obtain a smoother signal. The final differential output V_{OUT} is essentially:

$$V_{OUT} = V_{SH,top} - V_{SH,bot}$$
$$\approx \left[\frac{V_{os1} - V_{os2}}{K} + \frac{V_{DD}\Delta C}{C_A}\right]\left(\frac{1}{1+\frac{1}{K_{EQ}}}\right) \quad (5.5)$$

where V_{os1} and V_{os2} are the input referred offsets associated with OPAMP1 and OPAMP2, respectively. Interestingly, it can be seen that the final offset is significantly reduced by two phenomena. First, the final offset is proportional to the difference between the offset from OPAMP1 and OPAMP2. Assuming a good match between the two op amps, the offset can be very minimal. Furthermore, the offset difference is then reduced by a factor of K, which is derived in Section 5.1. Therefore, the offset and the very low frequency noise in this circuit can be decreased tremendously.

The op amps used in the circuit are all identical folded-cascode structures with a DC gain of 56.47 dB, a phase margin of 74.67°, an output voltage swing of 3.7 V, and a gain-bandwidth of 13.64 MHz at 1 pF load. The dual buffer consists of two op amps each configured as a unity gain buffer. The schematic of the op amps can be found in Fig. 4.7.

5.2.2 Back-End Circuit Block

Referring back to Fig. 5.2, it can be seen that the back-end of the interface circuit consists of an anti-aliasing filter (AAF) and a ΣΔ ADC. The output from the S/H stage is applied through the AAF such that the signal of interest is more band-limited, and more suitable for sampling. The detailed

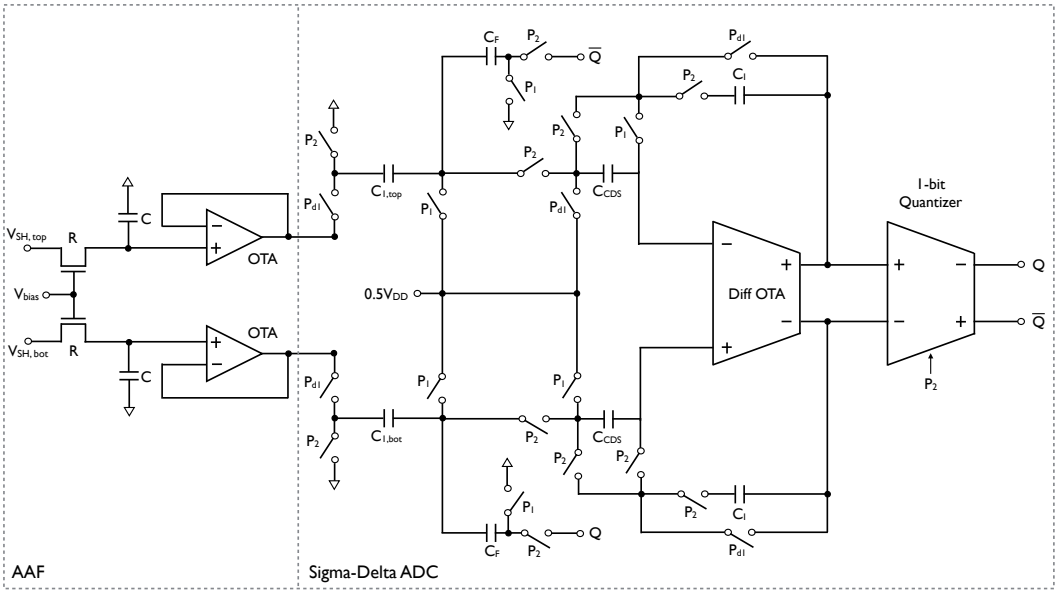

Figure 5.4: Schematic of the proposed capacitive readout back-end circuit which consists of an AAF and a SC ΣΔ ADC using CDS. The clocks used in the back-end are two non-overlapping clocks.

schematics of the back-end circuit block is shown in Fig. 5.4.

The AAF is a buffered RC low pass filter (LPF) where the R is made of a MOSFET operating in its linear region. The transistors in this case do not generate much flicker noise, but the thermal noise will be added to the input signal of the ΣΔ ADC. The thermal noise can be considered as a dithering mechanism which randomizes the quantization noise spectrum. Note that the 3-dB bandwidth of the filter is determined by the value of R and C, where the resistance is set by the size of the transistors.

The ΣΔ ADC is a first-order modulator, which consists of a fully differential SC integrator, a clocked 1-bit quantizer (comparator) and a SC negative feedback network (1-bit digital-to-analog converter). It is important to note

that, the ΣΔ ADC is an oversampling data converter that shapes the quantization noise out of the signal band, meaning the ADC could achieve very high resolution without the need of increasing analog components.

For a first-order ΣΔ ADC, the dynamic range (DR) can be expressed as [104]:

$$DR = 10log\left(\frac{9}{2\pi^2}\right) + 30log(OSR) \tag{5.6}$$

where OSR is the oversampling ratio of the converter, which is essentially the sampling clock frequency divided by 2X the input signal bandwidth. Equation (5.6) indicates that, the DR of the ADC increases by 9 dB every time the OSR doubles. This also translates into a 1.5 bits improvements from doubling the OSR. For this particular design, the OSR is roughly 1000, therefore, the DR should be expected to be ∼85 dB.

The circuit is clocked by two non-overlapping clocks P_1 and P_2. P_{d1} and P_{d2} are slightly delayed version of P_1 and P_2, and they are used to reduce the negative effects of charge injection. When clock phase P_1 is high (sampling phase), $C_{1,top}$ and $C_{1,bot}$ will be charged with the filtered output voltage of the front-end $V_{SH,top}$ and $V_{SH,bot}$, respectively. At the same time, the feedback capacitors C_F are charged to $0.5V_{DD}$. When P_2 switches to high (integration phase), the difference between the input signal (output of the AAF) and the 1-bit digital-to-analog converter (DAC) will be integrated through the SC integrator, and the digital output bit stream will show up at the output of the 1-bit quantizer. Moreover, the correlated double sampling (CDS) capacitors at the input of the op amp will store the offset and flicker

noise in the sampling phase. These offset and noise will then be canceled out during the integration phase. Also note that the ΣΔ ADC is separated from the actual sensor, therefore, it is not required to have C_1, C_F, or C_I programmable as the operation of the ADC does not depend on the sensor capacitance.

The internal structure of the 1-bit quantizer is basically an uncompensated op amp and a D flip-flop (DFF). The DFF is a falling edge trigger device, meaning that the comparator digital output will be latched at the falling edge of P_2. The sampling clock runs at 1 MHz. The noise shaping capability of a ΣΔ ADC will push the quantization noise out of the signal band.

5.3 Post-Layout Simulation Results

The readout circuit including the aforementioned front-end and back-end circuitries is designed and laid out in a 0.8 μm CMOS process. The circuit layout is shown in Fig. 5.5, where the active area is enclosed in a white dotted box and has a dimension of 2×0.25 mm^2. To simulate the interface, a pair of voltage-controlled differential capacitors C_{S+} and C_{S-} are implemented in Verilog-A to emulate the MEMS capacitive sensor. In terms of the front-end circuitry, Fig. 5.6 shows the simulated transient response of the readout front-end with respect to a sinusoidal ΔC with an amplitude of 50 fF and a frequency of 500 Hz (100 fF if considered differentially). Note that the sampling clock frequency is set at 100 kHz.

The output of the S/H stage has a differential amplitude of 1.242 V,

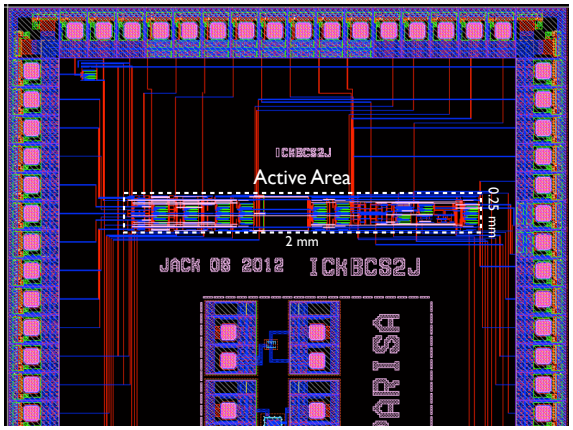

Figure 5.5: Layout of the proposed interface circuit in 0.8 μm CMOS. Note that the active area is enclosed in a white dotted box.

which corresponds to a differential sensitivity of 12.42 mV/fF. Moreover, an offset voltage source is intentionally placed at the input of an op amp (charge-transfer amplifier) during the simulation, and it can be seen that the DC level of the output is unaffected by the offset and is still at V_{ref} of 2.5 V. In Fig. 5.7, a comparison between the original CLS and the proposed modified CLS in terms of low-frequency noise behaviour is demonstrated via noise simulation. It can be seen that the proposed approach outperforms conventional CLS at very low frequencies (6 dB improvement at 1 Hz). For the proposed circuit, the equivalent output noise at 500 Hz is 3.05 $\mu V/\sqrt{Hz}$, which indicates an input-referred capacitance noise floor of approximately 0.25 aF/$\sqrt{Hz}$. Based on this simulation result, it can be seen that the noise floor of this readout circuit is higher compared with the previous designs. This can be attributed to the fact that more op amps and capacitors are used in this readout. The op amp is a major noise source, and capacitors

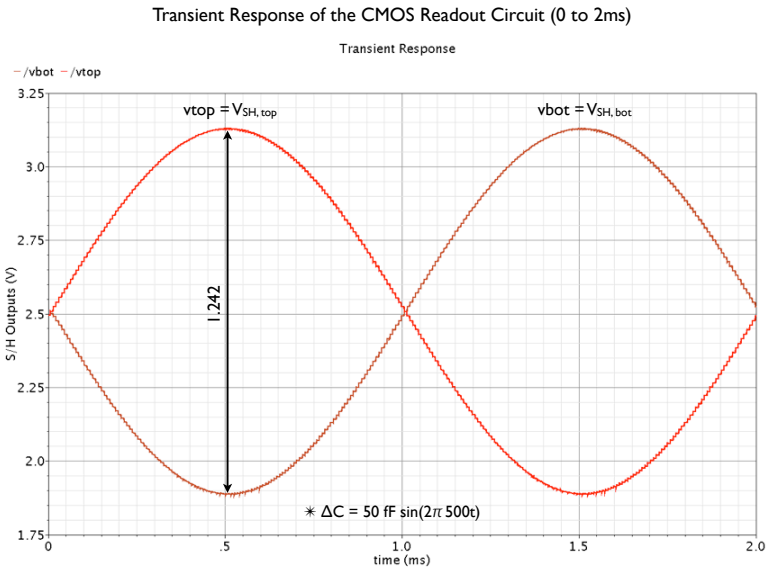

Figure 5.6: Transient response of the CMOS readout circuit front-end when an input capacitance variation of 50 fF (100 fF differential) is applied at 500 Hz.

in series with resistors will generate kT/C noise. For this particular readout, the purpose is to show that CLS can be modified such that offset and very low-frequency noise can be reduced. If the designer can implement a fully differential amplifier as opposed to two differential input single ended output op amp, the noise can be reduced significantly. Moreover, by using larger capacitors, i.e., larger C_R, kT/C noise can also be reduced. Therefore, this design would be more useful for sensors that have higher nominal capacitances. Finally, the front-end circuit consumes 555 μW from a single 5V supply.

In regards to the back-end circuit block, the output of the $\Sigma\Delta$ ADC is a pulse-width modulated (PWM) signal. The bitstream represents the input

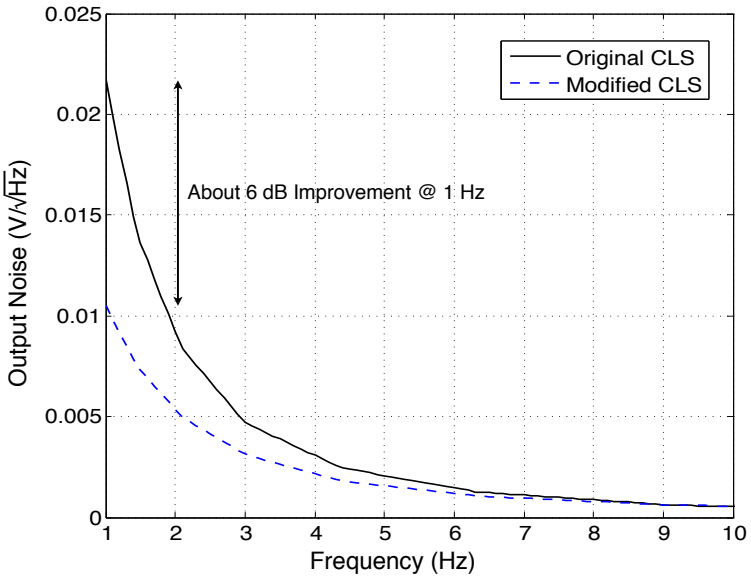

Figure 5.7: Simulated low-frequency noise response of the two approaches (CLS and proposed modified CLS).

analog signal. This analog signal is essentially the output of the S/H circuits from the front-end circuit block. In this case, it is a sinusoidal voltage signal tracking the sinusoidal capacitance variation coming from the sensor.

To first verify the functionality of the $\Sigma\Delta$ ADC, a first-order low-pass RC filter with 3-dB bandwidth of 4 kHz is used at the output to average down the bitstream. Since the input signal is running at 500 Hz, the filtered output should be a 500 Hz signal as well. Fig. 5.8 shows the low-pass filtered output signal (LP_out), the ADC output bitstream (Qb), and the input voltage signal (cap2) that generates the sinusoidal ΔC. As it can be seen, the filtered bitstream absolutely represents the analog input signal with a slight delay.

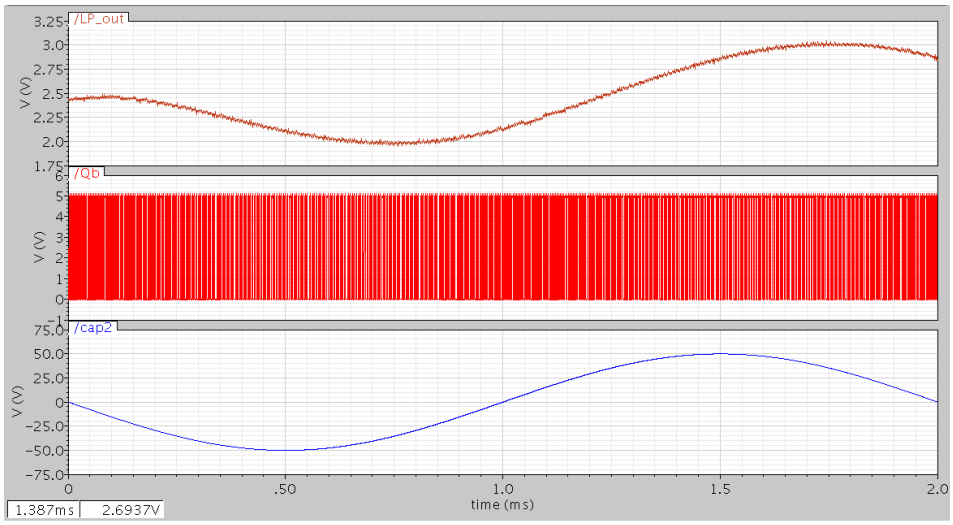

Figure 5.8: Transient response of the CMOS readout back-end when an input capacitance variation of 50 fF (100 fF differential) is applied at 500 Hz. The red bitstream is the output of the ΣΔ ADC that is getting filtered. The brown signal represents the low-pass filtered output, which tracks the input signal in blue.

The resolution is determined by examining the output spectrum of the ΣΔ ADC. The PWM bitstream data at the output is collected and Fast Fourier Transform (FFT) is applied to the data in Matlab to obtain the spectral content of the digital signal. Fig. 5.9 illustrates the power spectrum of the ADC output, where the noise shaping capability of the ΣΔ ADC is clearly shown. It can be seen that the CMOS interface circuit achieves a DR of roughly 85 dB, which is equivalent to a resolution of 14 bits. Lastly, the power consumption from the back-end is about 450 μW. Therefore, the total power consumption of the CMOS readout circuit is 1 mW.

A performance summary of the design is provided in Table 5.1. For the purpose of comparison, the measured performance of recent related works

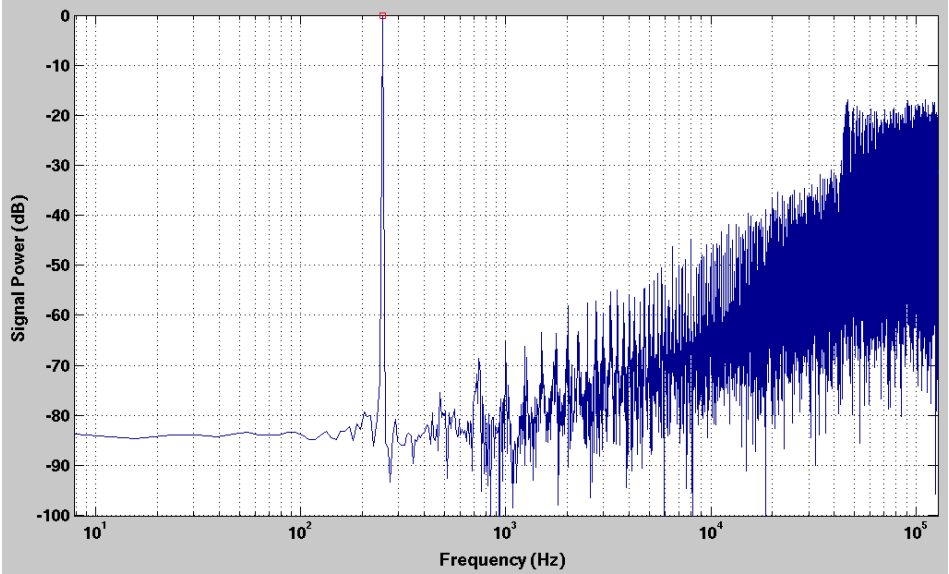

Figure 5.9: The spectral content of the PWM output. The input signal is a sinusoidal capacitance variation with a frequency of 500 Hz. The $\Sigma\Delta$ ADC processes the input and shapes the quantization noise out of the signal band. The DR is ∼85 dB, which translates to 14 bits of resolution.

[90, 91, 93, 101] is also included in the table. Note that [90] and [91] use continuous-time-based (CT-based) circuits, [101] uses pseudo-CT-based circuit, and [93] uses discrete-time-based (DT-based) circuit. Generally speaking, CT-based circuits exhibit better noise performance at the cost of consuming more power. Table 5.1 shows that the power and noise performance of the proposed readout circuit compares favourably with the state-of-the-art designs.

Table 5.1: Performance Summary and Comparison

Parameter	**This Work***	**[90]****	**[91]****	**[101]****	**[93]****
Noise Floor (aF/$\sqrt{Hz}$)	0.25	0.02	0.016	0.19	4
Frequency where noise is measured (Hz)	500	400	400	average from 0 to 300	10k
Clock (kHz)	125	1000	500	6	1000
Technology (μm)	0.8	0.5	0.35	0.35	0.25
Supply (V)	5	5	3.3	2.5 – 3.6	2.5
Power (mW)	1***	30	2.57	1 – 1.44	6***

*Post-layout simulation results **Measured results ***Including a SC $\Sigma\Delta$ modulator

5.4 Measurement Results

The CMOS readout circuit including both the front-end (charge-transfer amplifier and S/H) and back-end (AAF and $\Sigma\Delta$ ADC) circuits is fabricated in CMOS 0.8 μm technology. The overall size of the interface circuit chip is 25 mm^2, however, the active area is only 0.5 mm^2 as discussed in the previous section. The sensor interface chip is wire-bonded to the MEMS accelerometer in a single package. This accelerometer is described in Section 3.1 and the overall size of the sensor chip is 30.25 mm^2. A micrograph showing the whole system inside the package is illustrated in Fig. 5.10, where the CMOS readout is on the right, and the MEMS sensor is on the left.

The device package is mounted at the centre of a designed PCB for testing purposes. The dedicated PCB is shown in Fig. 5.11. The DC biasing circuitries surround the packaged device, while the connectors sit at the perimeter of the board. After powering up the chip and providing the necessary biases, I notice that the DC voltage level at the output of the front-end is roughly 0 V, which is substantially less than the expected value of 2.5 V (V_{REF}). This phenomenon has not changed after careful board debugging. There are no short circuits on the PCB and the biasing are all correct. We have 3 packages for testing and they all show the same results. I believe this problem could be caused by either of the following:

1. Mismatch between the nominal sensor capacitance C_0 and the reference capacitor C_R of the charge-transfer amplifier: referring back to Fig. 5.1(b), assuming all ideal components, if C_R is not equal to the nominal capacitor C_0, the output of the charge-transfer amplifier

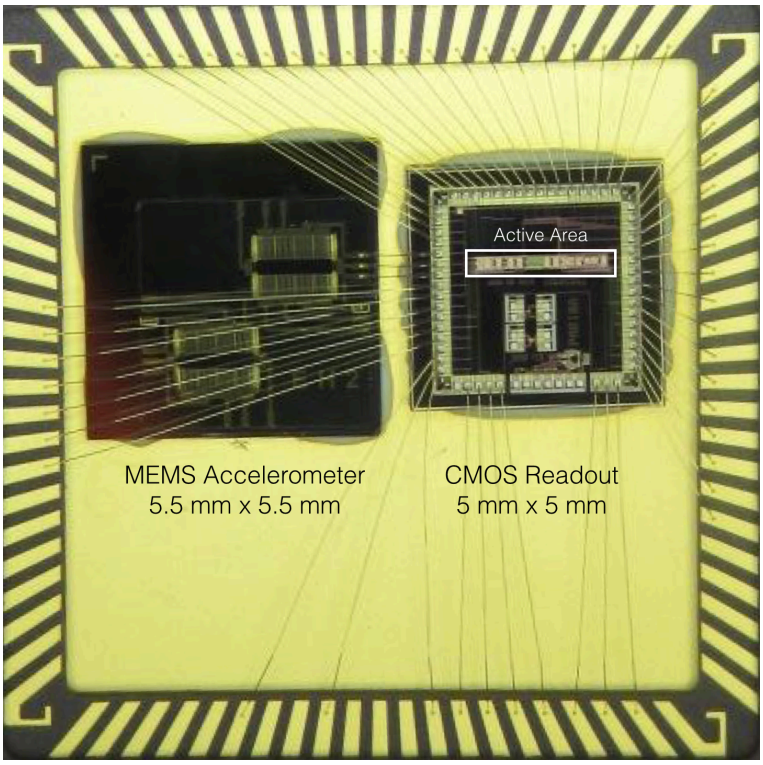

Figure 5.10: Micrograph of the overall sensing device: CMOS readout circuit is on the right where as the MEMS accelerometer is on the left. The sensor and the electronics are wire-bonded together in a single package.

during the level shift phase can be expressed as:

$$V_{OUT,LS2} = \frac{V_{DD}}{2} + \frac{V_{DD}(C_0 - C_R)}{2C_A} + \frac{V_{DD}}{2}\left(\frac{\Delta C}{C_A}\right) \tag{5.7}$$

This indicates that the common-mode voltage at the output of the charge-transfer amplifier can potentially drop to near zero value if:

$$\frac{C_R - C_0}{C_A} \geq 1 \tag{5.8}$$

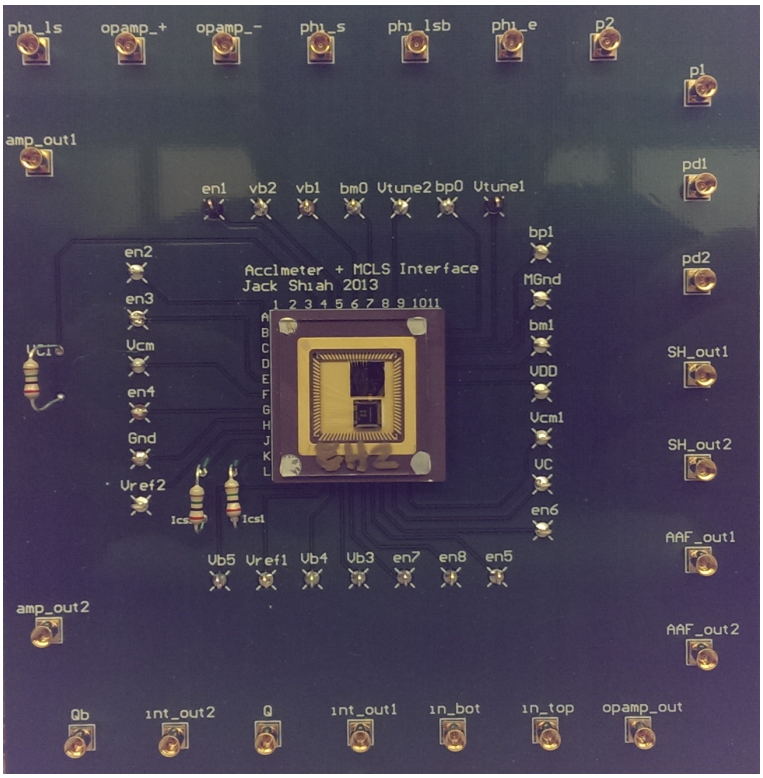

Figure 5.11: Dedicated PCB to test the accelerometer sensing system which is placed at the centre of the board.

For this design, C_R is designed to be equal to the nominal capacitance (C_0) value, which was provided by the MEMS designers. It is likely that C_R turned out to be larger than C_0 from all the parasitics near it, which caused this saturation phenomenon. Although I had trimming capability for C_R, the resolution is quite limited, as I did not design for a wider range of reference capacitances.

2. Chips are broken during the wire-bonding process: I believe this is another likely root because the packaging service provider had to cut

off the back of the readout circuit chip partially in order for the devices to fit inside the package.

3. Device is damaged from electrostatic discharge (ESD): I did implement ESD protection pads for the readout circuit, therefore, this may be less likely than other potential causes.

4. The op amp is broken: I believe this is unlikely because the current flowing through the op amp is correct from probing.

To summarize, I believe the reasoning behind the malfunctioning chip could be the mismatch between sensor capacitance (C_0) and reference capacitance (C_R), and the damage caused during the CMOS MEMS integration. Therefore, the performance of the sensing system is purely based on post-layout simulations.

5.5 Chapter 5 Conclusion

A low-noise interface circuit for MEMS capacitive sensory systems using modified CLS technique is presented. It is shown that the proposed circuit decreases the adverse effects of the op amp offset and low-frequency noise while maintaining the major benefit of the CLS, that is, reducing the effects of op amp finite gain. The design is laid out in 0.8 μm CMOS. Post-layout simulation results show that the interface system has a sensitivity of 12.42 mV/fF while consuming 555 μW from a single 5 V supply. Moreover, the readout circuit can resolve input capacitance variations as low as 0.25 aF/$\sqrt{Hz}$ at 500 Hz.

Chapter 6

Overall Design Flow and Discussion on Reported Readouts

So far in this thesis, three major circuit design techniques for MEMS capacitive sensor interface are proposed and analyzed in detail. In Chapter 3, the parasitic-insensitive chopper stabilized readout circuit is described. In Chapter 4, the chopper stabilized correlated level shifting readout circuit is presented. And finally in Chapter 5, the $\Sigma\Delta$ modified correlated level shifting readout is discussed. The primary objective of utilizing the above mentioned techniques is to achieve a high resolution high performance MEMS device. In particular, the system should have very good noise and power metrics and can be used in applications where high performance is required.

It is however very important to put the circuit design techniques aside and form a clear design flow. In other words, when a problem is given, the designer should follow a design flow and choose the correct circuit technique to implement the MEMS sensing device such that the system performance specifications are met efficiently.

In this chapter, the objective is to discuss the overall design flow from system level down to circuit level. In Section 6.1, a design flow chart is first given, followed by detailed explanations for each step. In Section 6.2, a general discussion on each of the reported readout circuit is provided, such that the reader will be able to select suitable circuit techniques for his/her own design.

6.1 Design Flow Chart and Detailed Explanation

Figure 6.1 shows a readout circuit design flow chart, where on the mechanical side, MEMS accelerometer is used as an example.

As discussed in the Introduction, for performance demanding applications, high resolution MEMS devices are required. Take MEMS accelerometer as an example, the resolution needs to be in the μg range for inertial sensing. This system level resolution should be the first specification to be examined, and the MEMS designer will implement a certain mechanical structural engineering procedure to ensure such resolution mechanically. With a sufficiently large proof mass, μg can be the mechanical Brownian noise floor. Therefore, with a good MEMS mechanical design, theoretically, the sensor is able to detect such small acceleration.

Once the resolution in g is determined (step 1), based on the mechanical design of the MEMS sensor, the relationship between acceleration and capacitance variation can be derived from the mechanical sensor. By knowing the minimum detectable acceleration, i.e., μg, the capacitance noise floor can be calculated using mechanical sensitivity in F/g (step 2). Note that this

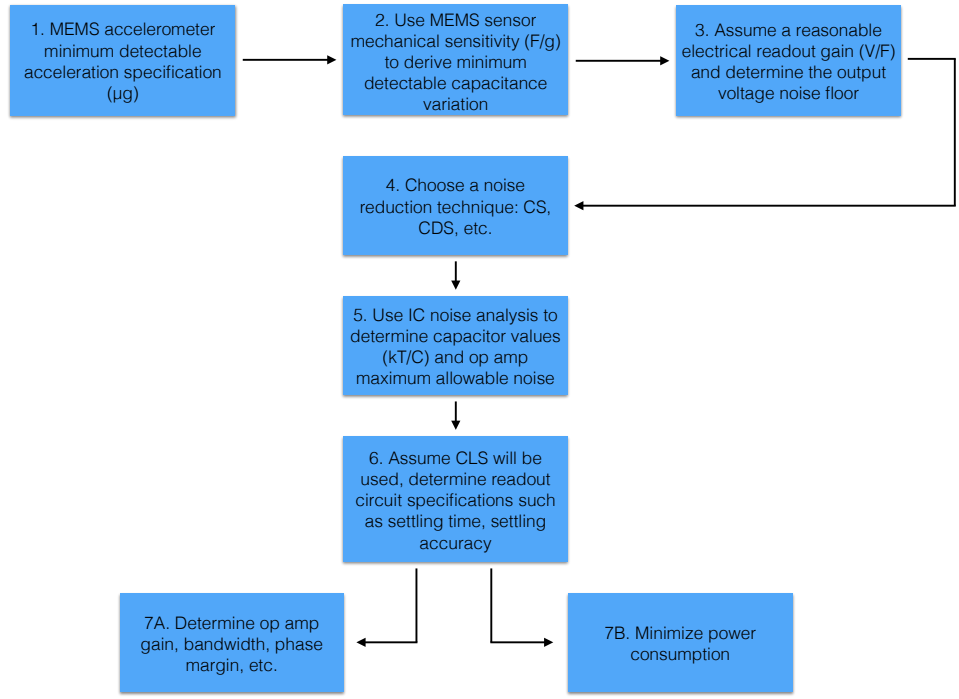

Figure 6.1: A general readout circuit design flow chart.

topic is also discussed in Section 2.1. Such minimum capacitance variation basically determins the type of readout circuit to be designed.

The resulting readout circuit needs to resolve the aforementioned small capacitance variation. In other words, the output voltage noise of the readout has to be minimized to meet such requirement. With reasonable assumption on the readout gain (V/F), the output noise voltage can be determined (step 3).

In step 4, the designer should choose a noise reduction technique. For instance, CS can be used to lower offset and flicker noise. However, extra

clocking is required to implement CS, which would increase the overall power consumption. If CDS is used, although additional clocking is not needed, the extra capacitor used to store errors would introduce extra kT/C noise. Therefore, these interesting trade-offs between noise and power should be considered by the designer.

In terms of step 5, circuit noise should be analyzed to determine capacitor values as well as op amp noise specification. The capacitor value mainly dictates the thermal noise level (kT/C). In regards to op amp, although both thermal and flicker noise exist, CS/CDS can reduce the latter. It is important to note that, it is not possible to keep increasing the capacitor value because large capacitors consume area. Furthermore, the feedback capacitor in the charge-transfer amplifier determines the capacitance-to-voltage gain. Large feedback capacitor will deteriorate the gain of the circuit, which can be undesirable (related to step 3).

From Chapter 4 and 5, it can be seen that CLS is a very useful technique in terms of readout circuit designing. Therefore, CLS should be assumed in the design process because it increases the loop gain of the readout circuit (step 6). With that in mind, designer can derive the op amp specifications based on settling time and accuracy. The op amp open loop gain is not required to be too large due to the loop gain boosting property of CLS, so power consumption can be reduced. The settling time can be used to determine the op amp frequency response (step 7A and 7B). By knowing all the specifications, the designer can implement all the circuit blocks down to the transistor level.

6.2 General Discussion on Reported Readouts

Based on the discussion from Section 6.1, there are many design considerations from step 4 and onwards. For high resolution readout circuits, it is important to utilize a noise reduction technique. In regards to the reported designs, CS is used in Chapter 3 and Chapter 4, whereas the readout in Chapter 5 uses an offset compensation technique similar to CDS. The designs presented from Chapter 3 to 5 are in chronological order. The parasitic-insensitive readout circuit uses CS and very large op amp input differential pair to reduce noise. The issue with this is that the device will be large, and there is no power minimization technique applied. Therefore, although good noise performance can be achieved, there are many aspects of the design that can be improved. Chapter 3 will be removed from further discussion.

Starting from Chapter 4, CLS has been used to improve settling accuracy and power consumption. By utilizing CS in conjunction with CLS, very good noise and power performance is achieved (0.018 aF/$\sqrt{Hz}$ and 0.29 mW). It is however important to note that the power consumption reported in Chapter 4 only includes the readout circuit, but not any other required peripheral circuitries such as clocks, filters, or ADCs.

In terms of Chapter 5, a modified CLS technique is used to implement the readout circuit. The designed interface circuit generates more noise compared to Chapter 4. However, it should be noted that the circuit implemented in Chapter 5 is a fast prototyping experiment, where many design aspects can be improved theoretically. For example, there are more op amps

used in Chapter 5 compared to Chapter 4. The designer can implement a fully differential op amp as opposed to two differential-to-single-ended op amps. By using a single fully differential op amp, the noise performance can be improved. Moreover, the modified CLS technique does not require extra clocking scheme, which is needed by CS. Therefore, the circuit in Chapter 5 should consume less power than the one in Chapter 4 when the whole system is considered.

In conclusion, if one hopes to design a readout circuit that has very good noise performance, the CS + CLS readout introduced in Chapter 4 can be considered. On the other hand, if the MEMS device requires very good power consumption while having reasonable noise floor, the modified CLS circuit described in Chapter 5 can be utilized. The development of CMOS interface circuits in all the chapters aligns with the ultimate scientific goal: proposing analog circuit design techniques to effectively reduce noise and power consumption for MEMS electronic readout. The key is to find good balance between noise and power by utilizing different approaches, in order to develop the right circuits based on the given specifications.

Chapter 7

Conclusion and Future Work

7.1 Research Contributions

The general theme of this thesis is the design and implementation of CMOS electronics interfacing MEMS capacitive sensors. More importantly, the research is mainly focused on analog circuit design techniques that improve the power and noise performance of the overall system. The sensor used in this work is a capacitive SOI MUMPS micro-accelerometer, and several readout circuits are proposed, designed, fabricated, and characterized. The front-end typically consists of a sensor, a charge-transfer amplifier (capacitance-to-voltage converter), S/H circuits, and filters. The output from the front-end would be a purely analog signal, where it is necessary to digitize the signal using an ADC for further digital signal processing. A summary of the overall work done in the research have been published in both conference proceedings [1–3] and journals [4]. Additionally, there is another journal manuscript that will soon be submitted.

- In Chapter 3, a CMOS readout circuit is designed and fabricated to interface with a MEMS capacitive accelerometer. On the mechanical side, the micro-sensor is implemented in SOI MUMPs technology in

which a large proof mass is utilized so that the sensor has high sensitivity and good noise performance. Special circuit techniques have been added to the readout electronic so that it is parasitic insensitive. Additionally, the circuit utilizes chopper stabilization (CS) technique to reduce the offset and low-frequency noise coming from MOS transistors. In this work, the CMOS interface and the MEMS sensor are wire-bonded in a single package forming a system-in-a-package. Measurement results show that the sensing system exhibits good noise performance.

- In Chapter 4, a switched-capacitor circuit technique called correlated level shifting (CLS) is used in conjunction with CS for the design of the readout circuit front-end. CLS was first proposed in [98] and it significantly improves the overall loop gain of the op amp. This would increase the accuracy of the output and loosen the gain specification of the op amp, which would reduce the power consumption of the system. The one drawback associated with CLS is that it does not cancel DC offset and very low-frequency noise of the op amp. By adding CS into the scene, the low-frequency imperfections (DC offset and $1/f$ noise) associated with the op amp would be reduced. In this work, a pair of on-chip variable capacitors are used to emulate the mechanical sensing element. Experimental results show very good power and noise performance from the circuit.

- Extending the novelty of CLS, a modification to the technique is proposed such that the modified version not only improves the loop gain

of the op amp, but also reduces its DC offset and low-frequency noise. Note that no other circuit techniques are required to reduce the noise. Everything related to this circuit technique is presented in Chapter 5, where principle of operation, circuit analysis, and post-layout simulations are presented. The modified CLS preserves the benefits of the original one, and simulation results show that the modified version has ∼6 dB noise improvement at low-frequency.

- Chapter 6 provides a detailed design flow for the designers to follow and implement the CMOS readout circuit efficiently and systematically. Moreover, discussion and comparison on the aforementioned three circuit design approaches is presented. Each design technique has its own merit and can be used depending on the application.

7.2 Future Work

Future directions for expanding the current research include:

- As discussed in the Introduction and Background chapters, one of the design focus is power consumption, leading to the selection of open-loop readout. However, it is possible to incorporate the readout circuit in a closed-loop system too. One of the possible future work would be to use the low-power low-noise charge-transfer amplifier inside a closed-loop sensing system for superior linearity and dynamic range.

- The proposed readout circuits should be connected with an ADC chip so the sensor's output can be digitized and processed. So far the

measurement results are purely analog. It would be interesting to use a $\Sigma\Delta$ ADC to digitize the analog signal.

- To achieve the most optimal performance, The MEMS capacitive sensor and the electronics should be implemented on the same wafer, making the chip monolithic and much smaller in size. This will greatly reduce the parasitic effect from the mechanical sensor to the readout circuit. Moreover, this can avoid wire bonds that could potentially act as an antenna and receive unwanted noise. Wire-bonding the MEMS sensor and readout circuit is done in Chapter 3, but ideally, as mentioned previously, fabricating both devices on the same wafer would achieve better results.

- A shaker table is very important for characterizing and measuring the sensory system as it is able to provide sinusoidal acceleration to the devices. For future work, one may use a shaker table to test the MEMS sensor with readout circuit.

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