

ON THE DESIGN OF TYPE-I INTEGER-N PHASE-LOCKED LOOPS

by

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Abstract

The phase-locked loop (PLL) is an essential building block of modern communication and computing systems. In a wireless communication system, a PLL is almost always used as the local oscillator (LO) that synthesizes the required frequency for data transmission and reception. In wireline and optical communication systems, PLL-based clock and data recovery (CDR) circuits are often employed for the extraction of the clock signal from the incoming data signal, and aligning the recovered clock edge with the incoming data for optimal bit-error rate (BER) performance. Furthermore, in microprocessor and field-programmable gate array (FPGA) systems, PLLs are typically used for clock generation.

Although phase-locking is a very mature research topic, its continuous application in modern integrated circuits (ICs) and systems requires continuous improvement in its performance, power consumption, and manufacturing costs. Analog Type-II PLLs are among the most widely used category of PLLs in CMOS (complementary-metal-oxide-semiconductor) ICs, mainly due to their robustness, superior performance and their well-established theory. However, analog Type-II PLLs require a large area in loop-filter (LF) and employ noisy and difficult-to-design charge-pumps (CPs). All-digital PLLs are also widely used, but they suffer from the strict jitter requirements on time-to-digital converters (TDCs).

We propose a Type-I PLL that uses a small LF area, does not require bias-generation circuits or CP, and consumes low power. A pulse-width-modulated (PWM) voltage output from the phase-frequency detector (PFD) is fed to a simple RC single-pole LF. Two major limitations of conventional Type-I topologies – limited lock-range and large reference spur – are overcome by increasing the PFD gain with a combination of a voltage booster and a digital level shifter, and a sample-and-hold (S/H) envelope detector, respectively. Furthermore, a saturated-PFD (SPFD) is proposed to reduce cycle slipping and to further improve the lock-range and lock-time. A proof-of-concept prototype 2.2-to-2.8 GHz PLL occupies a core area of 0.12 mm^2 in $0.13\text{-}\mu\text{m}$ CMOS and achieves $490 \text{ fs}_{\text{rms}}$ random jitter, -103.4 dBc/Hz in-band phase-noise, -65 dBc reference spur, $2.5 \text{ }\mu\text{s}$ worst-case lock-time while consuming 6.8 mW from a 1.2 V supply.

Preface

This thesis is an original intellectual product of the author A. Sharkia. Some of the material of Chapters 3, 5 and 6 are based on a conference paper that has been accepted at the 2015 IEEE Custom Integrated Circuits Conference (CICC) in San Jose, and will be published in the conference proceedings (A. Sharkia, S. Aniruddhan, S. Shekhar, and S. Mirabbasi, “A high-performance, yet simple to design, digital-friendly Type-I PLL,” in *Custom Integrated Circuits Conference, 2015. CICC '15. IEEE*, San Jose, CA, Sep. 2015).

All of the work presented henceforth was conducted in the System-on-Chip (SoC) Laboratory at the University of British Columbia, Point Grey campus.

Table of Contents

Abstract.....	ii
Preface.....	iii
Table of Contents	iv
List of Tables	vii
List of Figures.....	viii
List of Abbreviations	x
Acknowledgements	xii
Dedication	xiii
Chapter 1: Introduction	1
1.1 Motivation	1
1.2 Objective	2
1.3 Outline.....	2
Chapter 2: Integer-N PLL Fundamentals	3
2.1 Linear Phase-Domain Model	3
2.2 PLL Type and Order	4
2.3 Type-I PLL Transfer Functions.....	5
2.4 PLL Performance Metrics	6
2.4.1 Phase-Noise.....	6
2.4.1.1 Reference and Divider Phase-Noise Contributions	9
2.4.1.2 PFD/CP and LF Phase-Noise Contributions	10
2.4.1.3 VCO Phase-Noise Contribution	12
2.4.2 Reference-Spurs	13
2.4.3 Type-I PLL Lock-Range.....	15

2.4.4	Lock-Time.....	15
2.4.5	Stability of PLLs.....	16
2.4.6	Area and Power Consumption	17
2.5	Basic PLL Circuits	17
2.5.1	3-State Phase-Frequency Detector (PFD).....	17
2.5.2	Charge-Pumps (CP)	19
2.5.2.1	CP in Type-II PLLs	19
2.5.2.2	CP in Type-I PLLs.....	20
Chapter 3: Proposed PLL Architecture		22
3.1	Limitations of Prior-Art Type-II and Type-I PLLs.....	22
3.2	Boosted-Gain Type-I PLL.....	23
3.3	Voltage Booster for Higher Loop-Gain and Lock-Range.....	24
3.4	Saturated-PFD for Improving Lock-Time and Lock-Range.....	25
3.4.1	Dynamic, True-Single-Phase-Clocked (TSPC), D-Flip-Flop (DFF).....	29
3.5	Synchronous Envelope Detector for Spur-Reduction.....	30
3.6	Resistor Degenerated VCO	32
Chapter 4: Layout and Printed Circuit Board Design		34
4.1	PLL Layout	34
4.1.1	VCO Layout.....	34
4.2	Packaging.....	36
4.3	PCB Design and Measurements Setup.....	36
4.3.1	First PCB Design	36
4.3.2	Second PCB Design.....	37
Chapter 5: Simulation and Measurement Results.....		39
5.1	Simulated PLL Bandwidth.....	40

5.2	Phase-Noise	41
5.2.1	Simulated Phase-Noise	41
5.2.2	Measured Phase-Noise	42
5.2.3	Phase-Noise Measurements / Simulations Comparison	45
5.3	Spectrum Measurements	46
5.4	Lock-Time Measurements.....	48
5.5	Power Consumption	49
5.6	Performance Summary and Comparison.....	49
Chapter 6: Conclusion and Future Work.....		51
Bibliography		53

List of Tables

Table 2.1 A reference for the symbols shown in the above phase-domain model	8
Table 3.1 PLL architecture comparison.....	23
Table 5.1 Performance summary and comparison.....	50

List of Figures

Figure 1.1 Basic half-duplex RF transceiver block diagram	1
Figure 2.1 Basic PLL block diagram	3
Figure 2.2 Linear model of PFD/CP	4
Figure 2.3 Phase-noise explained	7
Figure 2.4 Phase-domain model of PLL with noise sources	8
Figure 2.5 Reference phase-noise before and after being low-pass filtered by a PLL	10
Figure 2.6 Output referred PFD/CP/LF phase-noise before and after being low-pass filtered by a PLL.....	11
Figure 2.7 VCO phase-noise before and after being high-pass filtered by a PLL.....	13
Figure 2.8 Reference-spurs	14
Figure 2.9 Conventional 3-state PFD schematic.....	18
Figure 2.10 Conventional 3-state PFD state-machine	18
Figure 2.11 Conventional 3-state PFD waveforms.....	19
Figure 2.12 Basic CP for Type-II PLLs.....	20
Figure 2.13 Integrate-and-reset CP for Type-I PLLs.....	21
Figure 3.1 Block diagram of the proposed Type-I PLL.....	24
Figure 3.2 Digital level-shifter schematic.....	24
Figure 3.3 Proposed voltage booster.....	25
Figure 3.4 Saturated vs. Conventional PFD Transfer Functions	26
Figure 3.5 Type-I PLL loop-dynamics with a conventional PFD vs. SPFD: response of the VCO control voltage (simulated) to a step in the reference frequency.....	26
Figure 3.6 Schematic of the proposed 5-state SPFD	27
Figure 3.7 Proposed SPFD state-machine	28

Figure 3.8 TSPC flip-flop schematic	29
Figure 3.9 LF with the S/H as a synchronous envelope detector.....	31
Figure 3.10 Pulse generator schematic	31
Figure 3.11 Resistor-degenerated LC-VCO with a 3-bit capacitor bank.....	32
Figure 3.12 Simulated VCO tuning curves for different capacitor bank values.....	33
Figure 4.1 Layout of the boosted-gain Type-I PLL.....	35
Figure 4.2 First PCB design.....	36
Figure 4.3 Second PCB design	38
Figure 5.1 Die micrograph.....	39
Figure 5.2 Simulated closed-loop PLL Bode plot (top: amplitude; bottom: phase).....	40
Figure 5.3 Simulated PLL phase-noise breakdown (output referred).....	41
Figure 5.4 Measured divided-by-2 PLL output phase-noise	42
Figure 5.5 Measured divided-by-2 PLL output jitter.....	43
Figure 5.6 Measured divided-by-2 free running VCO phase-noise.....	44
Figure 5.7 Measured free-running VCO phase-noise vs. locked PLL phase-noise (traces are scaled by +6 dB to compensate for the frequency division by 2).....	45
Figure 5.8 Measured vs. Simulated PLL phase-noise.....	46
Figure 5.9 Measured Divided-by-2 output spectrum (100 MHz span).....	47
Figure 5.10 Measured divided-by-2 output spectrum (1 to 4 GHz)	47
Figure 5.11 Measured frequency step response	48
Figure 5.12 Power consumption breakdown (based on simulations)	49

List of Abbreviations

PLL	Phase-Locked Loop
LO	Local Oscillator
CDR	Clock and Data Recovery
BER	Bit-Error Rate
IC	Integrated Circuit
CMOS	Complementary-Metal-Oxide-Semiconductor
LF	Loop-Filter
CP	Charge-Pump
TDC	Time-to-Digital Converter
PWM	Pulse-Width-Modulated
PFD	Phase-Frequency Detector
S/H	Sample-and-Hold
SPFD	Saturated Phase-Frequency Detector
SoC	System-on-Chip
CAD	Computer-Aided Design
RJ	Random Jitter
DJ	Deterministic Jitter
RMS	Root Mean Square
RF	Radio-Frequency
TX	Transmitter

RX	Receiver
ADE	Analog Design Environment
AMS	Analog / Mixed Signal
PCB	Printed Circuit Board
LTI	Linear Time-Invariant
DC	Direct Current
AC	Alternating Current
XO	Crystal Oscillator
TCXO	Temperature-Compensated Crystal Oscillator
OCXO	Oven-Controlled Crystal Oscillator
PVT	Process, Voltage and Temperature
VCO	Voltage-Controlled Oscillator
LDO	Low-Dropout Regulator
SSA	Signal Source Analyzer
PN	Phase-Noise
I/O	Input/Output

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To my Family and Friends

Chapter 1: Introduction

1.1 Motivation

Phase-Locked Loops (PLLs) are essential building blocks of many communication systems. They can be found in wireless, wireline and optical transceivers. In wireless communication systems, a PLL is often used as a frequency synthesizer, which serves the role of the local oscillator (LO). Figure 1.1 shows a block diagram of a basic half-duplex radio-frequency (RF) transceiver. Figure 1.1 shows how the LO signal is fed into an up-conversion mixer on the transmitter (TX) side, and into a down-conversion mixer on the receiver (RX) side.

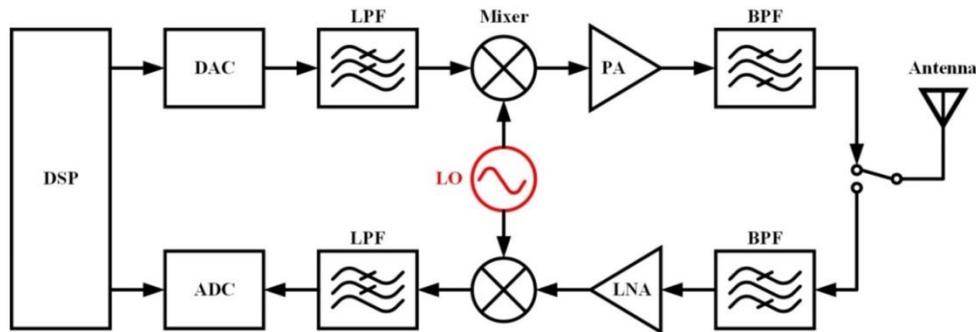


Figure 1.1 Basic half-duplex RF transceiver block diagram

Both wireline and optical communication systems utilize PLLs within different system blocks to provide various functionalities. On the TX side, a PLL is typically used as frequency synthesizer which sets the clocking frequency, thus setting the output data rate. Furthermore, in many high speed, high performance, wireline / optical data links, the data is sent from the TX to the RX without the clock. In such systems, clock and data recovery (CDR) circuits on the RX side are used to extract the clock signal from the incoming data signal and align the clock edge for achieving optimal bit-error-rate (BER). Most common implementations of CDRs are PLL-based.

Another common application of PLLs is in digital and microprocessor circuits. PLLs in digital circuits are typically used as frequency synthesizers that take on the responsibility of setting the clocking frequency of the circuit. By changing the divider / pre-scaler values of the PLL, the clocking frequency of the digital circuit can be varied to adapt for different

computation loads. Such dynamic frequency adaptation allows the system to choose the best clocking frequency for the best computation / power tradeoff.

1.2 Objective

The objective of this work is to design a digital-friendly, small area, low power, and high performance CMOS monolithic (fully integrated) PLL. Due to the inherently large area and design-complexity of the commonly used Type-II PLLs, we propose the boosted-gain Type-I PLL as valid alternative for mitigating some of these limitations, since Type-I PLLs typically occupy smaller loop-filter (LF) area, and are simpler to design due to the simpler charge-pump (CP) implementation. Conventional Type-I PLLs suffer from their own limitations of limited lock range and larger reference spur. This work addresses those issues.

Furthermore, to mitigate the cycle-slipping problem of conventional 3-state phase-frequency-defectors (PFDs), we propose a new circuit implementation for the saturated-PFD (SPFD), and utilize it within the proposed boosted-gain Type-I PLL system.

As a proof-of-concept, the proposed boosted-gain type-I PLL is designed and fabricated in IBM 0.13- μm CMOS process using Cadence Virtuoso Analog Design Environment (ADE), an industry standard for analog/mixed-signal (AMS) CMOS design. Post silicon measurements are performed to confirm the effectiveness of the proposed architecture and techniques in achieving the desired performance.

1.3 Outline

This thesis is organized as follows: Chapter 2 presents basic PLL theory and background that are needed for understanding the proposed architecture. Chapter 3 first presents the limitations of prior-art Type-II and Type-I PLLs, and then describes how the proposed PLL can overcome these limitations. Chapter 4 briefly touches on the layout of the proposed PLL and the design of the printed-circuit boards (PCBs) that were used to test the PLL chip after fabrication. Chapter 5 presents the measurement results of the proof-of-concept chip that was fabricated, and compares it with some of the simulation data. Lastly, Chapter 6 concludes this thesis and presents some ideas for future work.

Chapter 2: Integer-N PLL Fundamentals

One of the most common PLL architectures is the charge-pump (CP) based, analog, integer-N PLL. This classic PLL architecture is most commonly used for frequency synthesis when a high quality, low phase-noise and low reference spur signal is needed. An integer-N PLL is by definition any PLL with an integer frequency division ratio, N , between its output frequency, f_o , and its reference frequency, f_r (equation (2.1)). A PLL is “locked”, when a constant phase (or frequency) relation is preserved between its output signal and its reference signal. Equation (2.1) is true only when the PLL is locked.

$$N = \frac{f_o}{f_r} \quad (2.1)$$

2.1 Linear Phase-Domain Model

Despite it being inherently non-linear (different frequencies at the input and the output), a PLL can be represented by a simple linearized phase-domain model [1]. Figure 2.1 shows the block diagram of a classic phase-frequency-detector/charge-pump (PFD/CP) based, integer-N, PLL with the transfer functions of the various system blocks indicated.

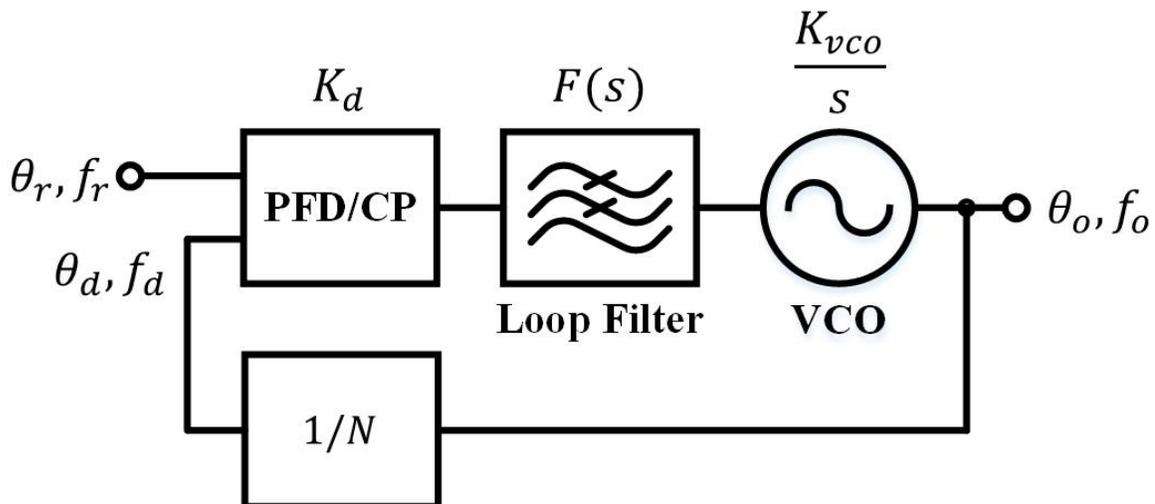


Figure 2.1 Basic PLL block diagram

Figure 2.2 shows the linear phase-domain model of the PFD/CP [2]. When the two input signals of the PFD are of different frequencies, the PFD works as a frequency detector, providing an output that is linearly proportional to the difference in frequency between its two input signals. However, when the two input signals of the PFD have very close (or equal) frequencies, the PFD works as a phase-detector, providing an output that is proportional to the phase difference between its two inputs. The gain block (K_d) that is shown in Figure 2.2 is representing the combined gain of the PFD and the CP, which is why we will be referring to this block as the PFD/CP.

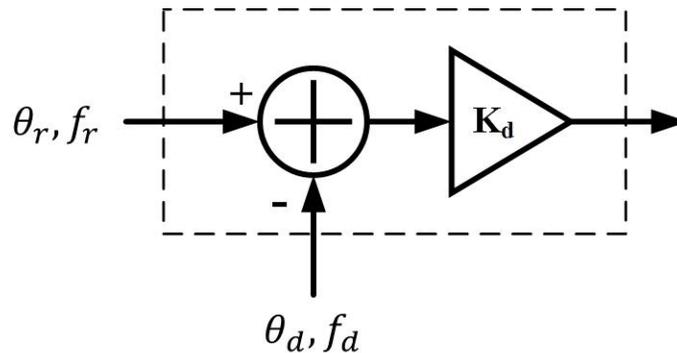


Figure 2.2 Linear model of PFD/CP

Based on the linear phase-domain model, PLLs can be treated as standard linear time-invariant (LTI) systems. Using the linearized model is an established technique which offers many benefits; most important of which, is allowing the designer to use many powerful mathematical and analytical tools from the field of control theory. Tools such as the Laplace transform, Bode plots, pole-zero diagrams, stability analysis, etc. are often used to give the designer a greater insight and understanding of the PLL performance, without the need for time-consuming circuit simulation tools [1].

2.2 PLL Type and Order

PLLs are often categorized based on their “type” and their “order”. The type of a PLL corresponds to the number of integrators in the forward path [1]. Integrators in the forward path show up as poles at the zero frequency (DC) in the Laplace domain representation. The minimum number of integrators in the forward path of a PLL is one, which is the voltage-controlled oscillator (VCO) (equation (2.2)). Type-I PLLs have only one integrator in the

forward path, the VCO, whereas type-II PLLs have the additional integrating action of the PFD/CP. Type-III PLLs and higher can also be found in literature [3], but they are far less common due to their higher complexity and loop stability issues. According to [4], many of the published works on monolithic PLL implementations indicate that the PFD/CP based Type-II architecture is the most common.

$$H_{VCO}(s) = \frac{K_{vco}}{s} \quad (2.2)$$

The order of a PLL corresponds to the total number of poles in the forward path of the system, which is why the order of a PLL can never be less than its type [1]. As an example, a Type-I PLL with a single pole LF is considered a 2nd order PLL, because it has two poles: one caused by the VCO and the other by the LF. On the other hand, a Type-II PLL with a single pole LF is considered a 3rd order system.

2.3 Type-I PLL Transfer Functions

This section presents various transfer functions that related to Type-I PLLs. The analysis done here can be used to analyze Type-II, Type-III and higher types of PLLs by simply modifying the PFD/CP transfer function from K_d , for Type-I, to K_d/s , for Type-II, K_d/s^2 , and more generally to K_d/s^{n-1} ; where n is the PLL type.

Since a linear time-invariant system is assumed, a Type-I PLL can be represented by the following transfer function (equation (2.3)):

$$H(s) = \frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{K_d K_{vco} F(s)}{s}}{1 + \frac{K_d K_{vco} F(s)}{Ns}} \quad (2.3)$$

Assuming $G(s)$ represents the forward path gain divided by N , we get Equation (2.4):

$$G(s) = \frac{K_d K_{vco} F(s)}{Ns} \quad (2.4)$$

Combining Equations (2.3) and (2.4), a simplified PLL transfer function can be obtained, and is shown in Equation (2.5):

$$H(s) = \frac{NG(s)}{1 + G(s)} \quad (2.5)$$

Equation (2.6) represents the error transfer function of the PLL, which is defined as the ratio between the phase error at the input of the PLL (the difference between the reference phase θ_r and the feedback phase θ_d) and the reference phase θ_r [1].

$$E(s) = \frac{\theta_e(s)}{\theta_r(s)} = \frac{\theta_r(s) - \frac{\theta_o(s)}{N}}{\theta_r(s)} = 1 - \frac{H(s)}{N} = \frac{1}{1 + G(s)} \quad (2.6)$$

Looking at Equation (2.6), we can see that the forward gain transfer function, $G(s)$, appears in the denominator of the error transfer function $E(s)$. This is a clear indication that the higher the gain of the PLL, the smaller the error. This important observation is one of the reasons for proposing the boosted-gain PLL architecture.

2.4 PLL Performance Metrics

PLLs can be characterized based on the phase-noise of their output signal, the relative power of the reference spur, the lock-range, lock-time, power and area consumption. Depending on the application, emphasis on the various performance metrics will vary. For example, a PLL in a high performance RF transceiver must have superior phase-noise and spur performance, whereas a PLL used for clocking a digital processor may have a much more relaxed phase-noise and spur performance requirements.

2.4.1 Phase-Noise

PLL phase-noise is the random and undesired variation in the phase/frequency of the PLL output signal, and is measured in units of “dBc/Hz” (Figure 2.3). The term “phase-noise” is often used in the RF domain, and the term “random-jitter” (RJ) is often used in the wireline/optical communications domains. Both the phase-noise and the RJ are describing the same physical phenomena but using different mathematical representations. To calculate the RJ from a given phase-noise plot, we simply integrate the phase-noise within a given bandwidth. RJ is measured in units of root-mean-square (RMS) seconds. Since most of the

theoretical PLL analysis will be presented is based on the linearized phase-domain model, this thesis will be referring to the phase-noise more often than the RJ.

Off-the-shelf discrete high quality oscillators such as crystal oscillators (XOs) and temperature-compensated crystal oscillators (TCXO) offer superior phase-noise and spur performance that are practically impossible to match using CMOS oscillators; mainly due to the limited quality factors that can be achieved in CMOS, in addition to process, voltage and supply (PVT) dependence. On the other hand, off-the-shelf discrete oscillators (especially XOs) are typically expensive, and are available in specific fixed frequency values that usually do not exceed few hundreds of megahertz.

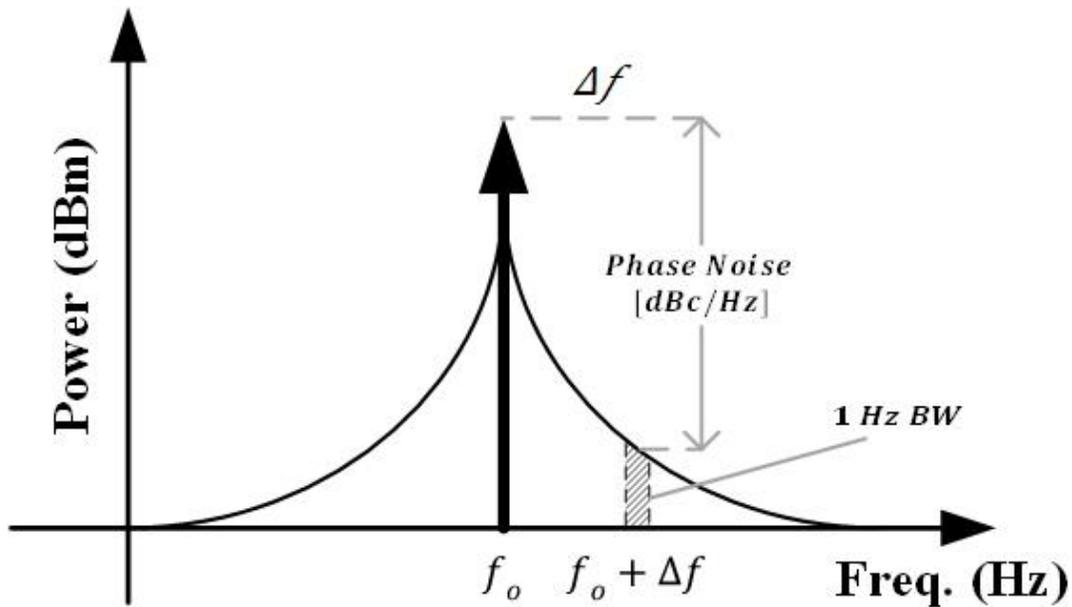


Figure 2.3 Phase-noise explained

PLLs can be used to overcome the shortcomings of CMOS oscillators and limitations of discrete oscillators. A PLL works as a frequency / phase stabilizer that forces the VCO's output frequency / phase to have a fixed and known relationship with an input reference signal. If the reference signal is stable and relatively PVT independent, the VCO's output will experience a significantly stronger rejection to PVT variations, and thus a signal with stable and precise frequency is generated.

Furthermore, a PLL acts as a high pass filter with regards to the VCO's phase-noise, since it attenuates the VCO's in-band (low frequency, below the PLL bandwidth) phase-

noise. This is a very important and useful feature of PLLs, because CMOS VCOs tend to experience very high phase-noise at the low offset frequencies (close to the carrier), mainly due to the frequency up-conversion of the VCO transistors' flicker noise and any flicker noise on the control line.

The phase-noise of a PLL output signal is caused by a combination of all the random noise sources in the system. Typically the following noise sources are considered when analyzing / designing a PLL: the noise of the reference signal, PFD/CP noise, LF noise, VCO noise, and divider noise. Figure 2.4 shows the phase domain model of the PLL with the different noise sources. In this model all the system blocks are divided into an ideal noiseless functional block and an added noise signal. Table 2.1 is a reference to the symbols shown in Figure 2.4.

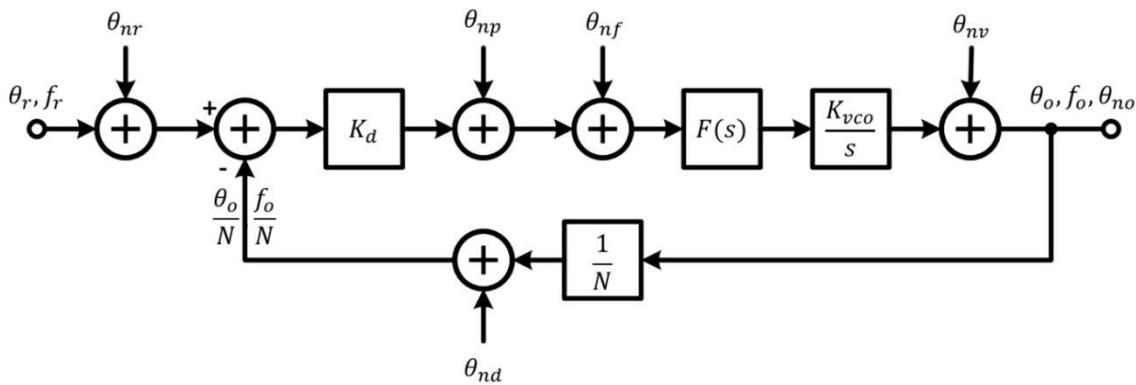


Figure 2.4 Phase-domain model of PLL with noise sources

Symbol	Meaning		Symbol	Meaning
θ_r	Reference Phase		N	Divider Ratio
f_r	Reference Frequency		θ_{nr}	Reference Noise
θ_o	Output Phase		θ_{pr}	PFD/CP Noise
f_o	Output Frequency		θ_{nf}	Input-referred LF Noise
K_d	PFD/CP Gain		θ_{nv}	VCO Noise
$F(s)$	LF Transfer Function		θ_{nd}	Divider Noise
K_{vco}	VCO Gain		θ_{no}	Output Noise

Table 2.1 A reference for the symbols shown in the above phase-domain model

2.4.1.1 Reference and Divider Phase-Noise Contributions

Because an LTI system is assumed, analyzing the contributions of each of the noise sources to the output PLL phase-noise is relatively straight forward. Since both the phase-noise of the reference signal and the divider output are referred to the input of the PLL, the same transfer function ($T_{nr,nd}(s)$, shown in Equation (2.7)) can be used to describe them. Here, $\theta_{no,r}$ and $\theta_{no,d}$ are referring to the output-referred (PLL output) reference phase-noise and divider phase-noise, respectively.

$$T_{nr,nd}(s) = \frac{\theta_{no,r}(s)}{\theta_{nr}(s)} = \frac{\theta_{no,d}(s)}{\theta_{nd}(s)} = H(s) = \frac{NG(s)}{1 + G(s)} \quad (2.7)$$

In the following analysis will have assume a single-pole (at ω_{LF}), low-pass, RC filter for the sake of drawing useful conclusions with regards to the input referred phase-noise transfer function. Assuming Equation (2.8) is representing the selected single pole RC LF:

$$F(s) = \frac{1}{1 + RCs} = \frac{1}{1 + \frac{s}{\omega_{LF}}} \quad (2.8)$$

The resulting reference and divider phase-noise transfer function is shown in Equation (2.9):

$$\begin{aligned} T_{nr,nd}(s) = H(s) &= \frac{\frac{K_d K_{vco}}{s \left(1 + \frac{s}{\omega_{LF}}\right)}}{1 + \frac{K_d K_{vco}}{Ns \left(1 + \frac{s}{\omega_{LF}}\right)}} = \frac{NK_d K_{vco}}{Ns \left(1 + \frac{s}{\omega_{LF}}\right) + K_d K_{vco}} \\ &= \frac{N}{\frac{Ns \left(1 + \frac{s}{\omega_{LF}}\right)}{K_d K_{vco}} + 1} = \frac{N}{s^2 \left(\frac{N}{\omega_{LF} K_d K_{vco}}\right) + s \left(\frac{N}{K_d K_{vco}}\right) + 1} \end{aligned} \quad (2.9)$$

Equation (2.9) indicates that the phasenoise transfer function from the input of the PLL to its output is that of a two pole low pass filter with a pass-band (in-band) gain of N . This means that the lower offset frequency (below PLL bandwidth) components of the reference and divider phase-noise will be amplified by a factor of N ($20 \log_{10}(N)$ in the dB scale), and that the higher offset frequency components will be attenuated.

Figure 2.5 shows reference phase-noise plots before and after being low-pass filtered by a second-order Type-I PLL. Note that the amplitudes of both phase-noise plots are

normalized to the output frequency of the PLL, in order to help visualize the low-pass filtering action that Equation (2.9) implies.

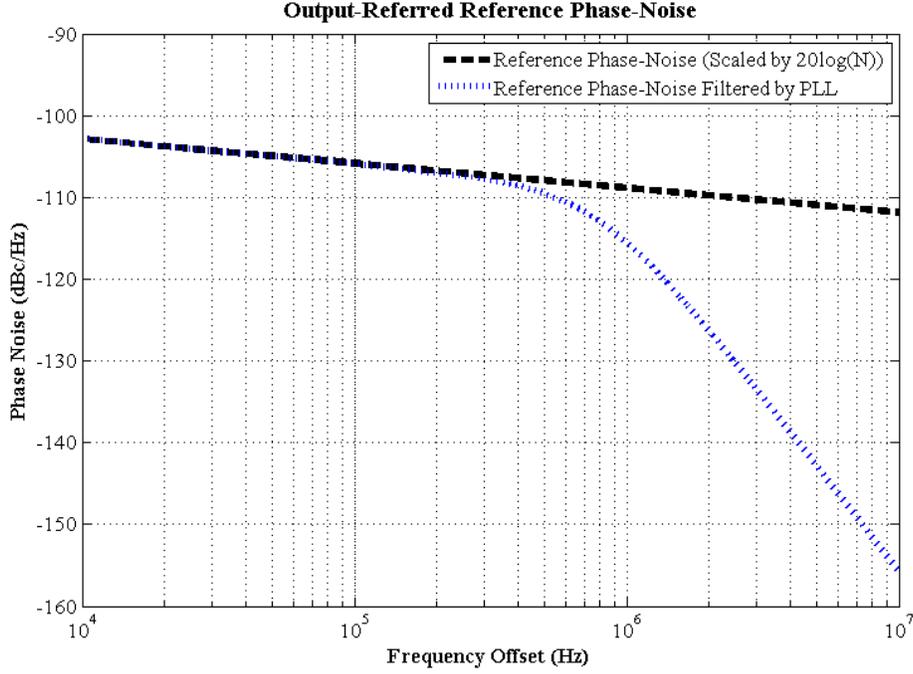


Figure 2.5 Reference phase-noise before and after being low-pass filtered by a PLL

2.4.1.2 PFD/CP and LF Phase-Noise Contributions

The transfer function of the PFD/CP and LF noise ($T_{np,nf}(s)$) is shown in Equation (2.10). Here, $\theta_{no,p}$ and $\theta_{no,f}$ are representing the output-referred (PLL output) PFD/CP noise and the LF noise, respectively.

$$T_{np,nf}(s) = \frac{\theta_{no,p}(s)}{\theta_{np}(s)} = \frac{\theta_{no,f}(s)}{\theta_{nf}(s)} = \frac{\frac{K_{vco}F(s)}{s}}{1 + \frac{K_d K_{vco} F(s)}{Ns}} = \frac{NG(s)}{K_d(1 + G(s))} \quad (2.10)$$

Assuming Equation (2.8) is representing the LF, we obtain Equation (2.11):

$$\begin{aligned}
 T_{np,nf}(s) &= \frac{NG(s)}{K_d(1+G(s))} = \frac{H(s)}{K_d} \\
 &= \frac{\frac{N}{K_d}}{s^2 \left(\frac{N}{\omega_{LF} K_d K_{vco}} \right) + s \left(\frac{N}{K_d K_{vco}} \right) + 1}
 \end{aligned} \tag{2.11}$$

Equation (2.11) indicates that, the transfer function of the output-referred PFD/CP and input-referred LF phase-noise is also behaving like a two-pole low-pass filter, just like the reference and divider phase-noise transfer function. However, the main difference is that the in-band phase-noise which is caused by the PFD/CP and the LF gets amplified by a factor of N/K_d ($20 \log_{10}(N/K_d)$ in the dB scale), rather than by a factor of N . This indicates that higher PFD/CP gain is desirable for attenuating the PFD/CP and LF generated phase-noise; which is another reason for the proposal of the boosted-gain PLL.

Figure 2.6 shows the combined PFD/CP/LF phase-noise before and after being low-pass filtered by a second-order, Type-I PLL. Note that the amplitudes of both phase-noise plots are normalized to the output frequency of the PLL, in order to help visualize the low-pass filtering action that Equation (2.11) implies.

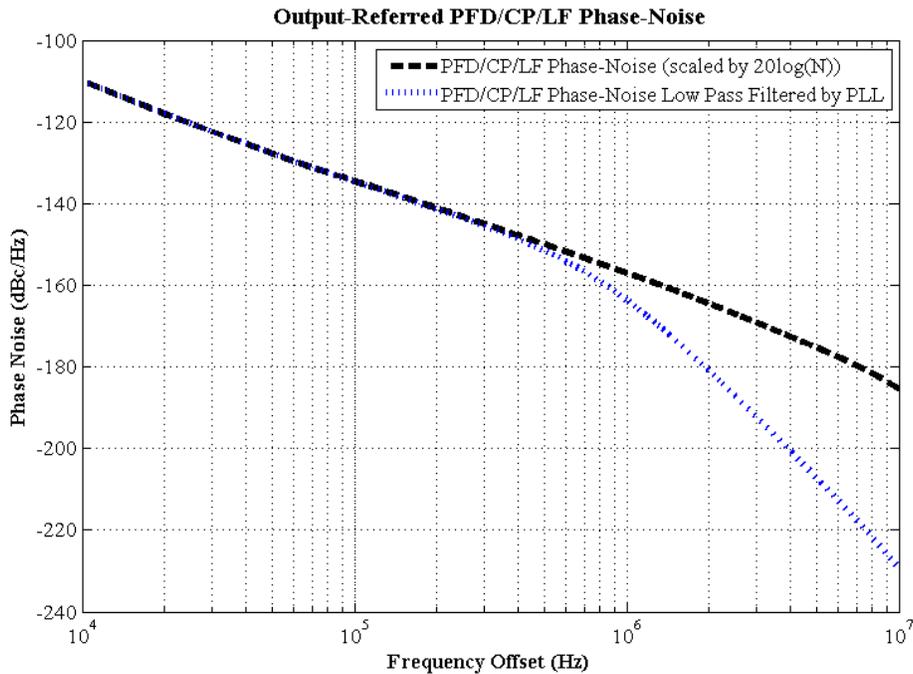


Figure 2.6 Output referred PFD/CP/LF phase-noise before and after being low-pass filtered by a PLL

2.4.1.3 VCO Phase-Noise Contribution

The transfer function of the VCO phase-noise ($T_{nv}(s)$) is shown in Equation (2.12). Here, $\theta_{no,v}$ is representing the output-referred VCO phase-noise.

$$T_{nv}(s) = \frac{\theta_{no,v}(s)}{\theta_{nv}(s)} = \frac{1}{1 + \frac{K_d K_{vco} F(s)}{Ns}} = \frac{1}{1 + G(s)} \quad (2.12)$$

A quick look at Equation (2.12) tells us that the higher the forward gain of the PLL, the more attenuation of VCO phase-noise is achieved. However, to get an even deeper insight, we will again assume the LF to be the single-pole low-pass RC filter described by Equation (2.8), which leads to Equation (2.13):

$$\begin{aligned} T_{nv}(s) &= \frac{1}{1 + \frac{K_d K_{vco} F(s)}{Ns}} = \frac{Ns}{Ns + \frac{K_d K_{vco}}{1 + \frac{s}{\omega_{LF}}}} = \frac{Ns \left(1 + \frac{s}{\omega_{LF}}\right)}{Ns \left(1 + \frac{s}{\omega_{LF}}\right) + K_d K_{vco}} \quad (2.13) \\ &= \frac{\frac{Ns}{K_d K_{vco}} \left(1 + \frac{s}{\omega_{LF}}\right)}{\frac{Ns}{K_d K_{vco}} \left(1 + \frac{s}{\omega_{LF}}\right) + 1} \end{aligned}$$

Equation (2.13) clearly shows that the VCO phase-noise gets high-pass filtered, which means that the only the in-band phase-noise of the VCO is attenuated, and the out-of-band phase-noise of the VCO passes with a unity gain.

To help visualize the high-pass filtering action that Equation (2.13) implies, Figure 2.7 shows how the low offset frequency components of the VCO phase noise get attenuated when the VCO is inserted in a second-order, Type-I PLL system.

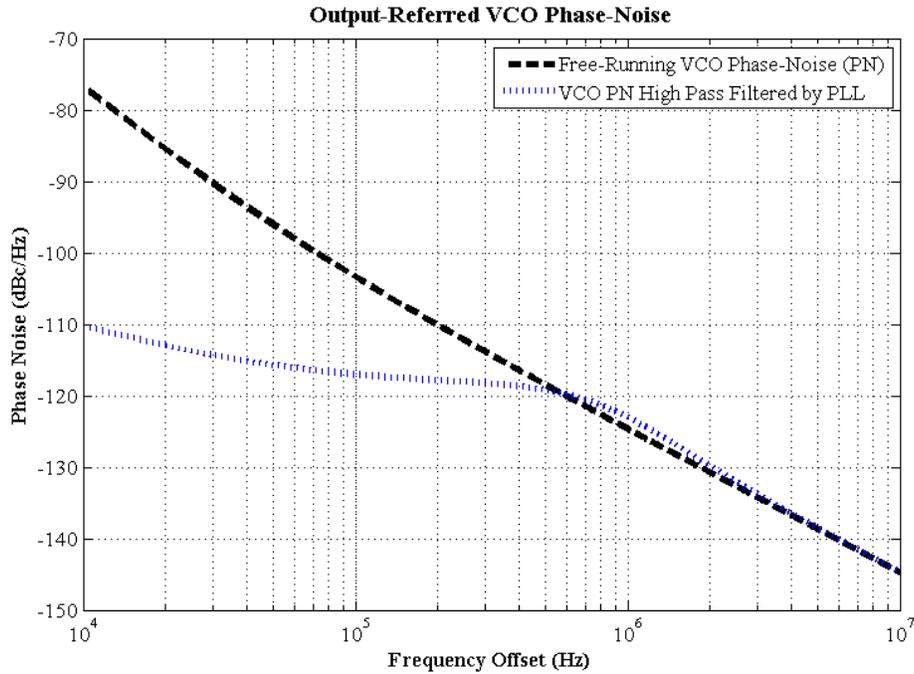


Figure 2.7 VCO phase-noise before and after being high-pass filtered by a PLL

The PLL must be designed carefully such that the total output phase-noise is minimized. If the output phase-noise is dominated by the VCO, then a wide bandwidth is desirable so that we maximize the attenuation of the VCO phase-noise. On the other hand, if the output phase-noise is dominated by any of the other sources (reference, divider, PFD/CP, or LF), then a narrow bandwidth is more desirable in order to maximize the attenuation of the in-band phase-noise cause by the sources mentioned above.

2.4.2 Reference-Spurs

Just like phase-noise, spurs also lead to undesired variations in the PLL output frequency; however, unlike the random variations caused by the phase-noise, spurs lead to deterministic variations with specific amplitudes and frequencies (Figure 2.8). In the wireline/optical communications domains, the term “deterministic-jitter” (DJ) is often used to describe the same physical phenomena that spurs describe, but in a different representation. While DJ is measured in peak-to-peak (pk-pk) seconds, spurs are measured in “dBc”, which refers to decibels with respect to the carrier.

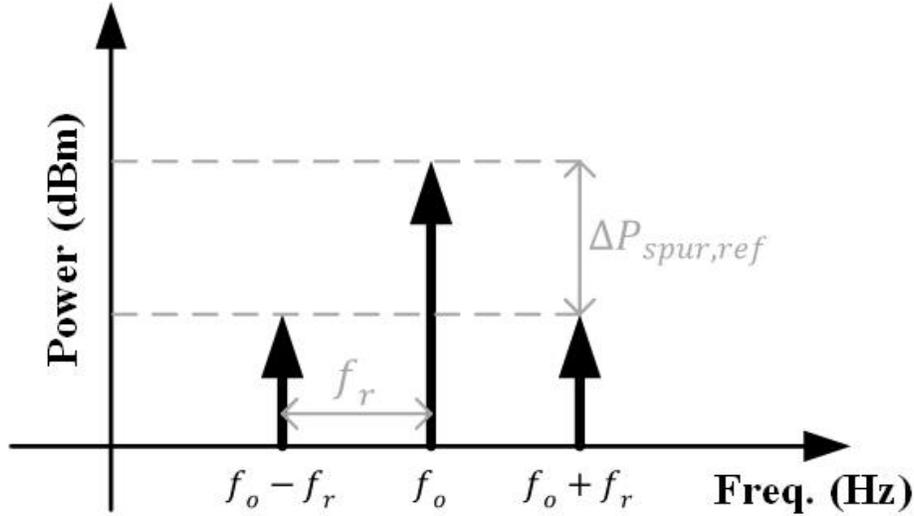


Figure 2.8 Reference-spurs

One of the main reasons for causing the spurs (especially the reference-spurs) at the output of a PLL is the voltage ripple on the VCO control line. The VCO can be thought of as a mixer, since the spectrum of the ripple on the VCO control line gets up-converted, and shows up as spurs around the VCO center frequency [5]. Equation (2.14) describes the amplitude of the spurs that show up on the VCO output, and are caused by a ripple on the control line [5]. $\Delta P_{spur,ref}$ is the amplitude of the spur in dBc, K_{vco} is the gain of the VCO in (MHz/V), A_r and f_r describe the amplitude and frequency, respectively, of a given tone on the VCO control line.

$$\Delta P_{spur,ref} = 20 \log_{10} \left(\frac{K_{vco} A_r}{2f_r} \right) \quad (2.14)$$

In an ideal Type-II PLL, the VCO control contains a pure DC signal, due to the integrating action of the PFD/CP, which leads to the PLL locking a zero phase-offset between its reference and feedback signals. However, realistic implementations of Type-II PLLs often suffer from CP current mismatch and LF capacitor leakage, which lead to very small ripples (with the reference frequency) on VCO control line [5]. This secondary effect leads to a very small reference spur in the realistic implementation of Type-II PLLs.

By contrast, even an ideal Type-I PLL will always have some ripples (with the reference frequency) on the VCO control line, because of the non-integrating action of the

Type-I PFD/CP, which leads to the PLL locking with a static phase offset, between its reference and feedback signals. Locking with a static phase offset leads to systematic ripples on the VCO control line, which lead to a systematic reference-spur at the PLL output [6].

In summary, compared to a Type-II PLL, a Type-I PLL suffers from a poor reference-spur performance due to the systematic ripples on its VCO control caused by the non-integrating action of its PFD/CP. The reference-spur can be attenuated by designing an LF that attenuates the ripples on the VCO control line.

2.4.3 Type-I PLL Lock-Range

Equation (2.14) describes the input-referred lock-range of a generic Type-I PLL [4]. If we assume a single-pole low-pass response for the LF, and then rearrange and solve Equation (2.15), we obtain Equation (2.16), which describes the lock-range of a Type-I PLL with a single-pole ($1/\tau$) low-pass LF [4].

$$\Delta\omega_L = \frac{2\pi K_{vco}K_d}{N} * |F(\Delta\omega_L)| \quad (2.15)$$

$$\Delta\omega_L = \sqrt{\frac{\sqrt{1 + \left(\frac{4\pi\tau K_{vco}K_d}{N}\right)^2} - 1}{2\tau^2}} \quad (2.16)$$

Equation (2.16) indicates that the lock-range of a Type-I PLL is directly related to its forward gain ($K_{vco}K_d$). This is another reason that makes boosting the forward gain of the PLL desirable.

2.4.4 Lock-Time

As we discussed earlier, a PLL is locked when it provides an output signal whose phase/frequency has a constant relation with the PLL input (reference) signal. Furthermore, the lock-time of a PLL system is the time it takes for a PLL to acquire lock (become locked) after a phase/frequency step is applied to the input of its PFD. A phase/frequency step can

easily be applied by either changing the reference phase/frequency in a very short time, while the PLL is running, or by changing the value of the feedback divider, also while it is running.

As we would expect from a negative-feedback control system, the settling time of the system (which is equivalent to lock-time in PLLs) is inversely related to the bandwidth of the system. This means that a higher bandwidth PLL is generally faster in acquiring lock than a lower bandwidth PLL. Fast-locking PLLs are very desirable because they allow their host system to quickly reconfigure the output phase/frequency of the PLL without causing a long delay in the system.

2.4.5 Stability of PLLs

Just like any other negative-feedback control system, the Bode criterion of stability can be used to evaluate the stability of a PLL system [1]. The Bode criterion of stability states that a PLL is stable if its open-loop phase lag at the gain crossover frequency (the unity gain frequency, frequency at which the open-loop gain is 0 dB) is less than 180° . This criterion is valid if there is only one crossover frequency and the open loop gain is stable (no poles in the right-half plane), which is the case for most PLLs [1]. A PLL must have a phase margin of at least 45° to be considered stable, however phase margins of 60° or more are preferable [1].

When comparing the stability of Type-II vs. Type-I PLLs, we find that Type-II PLLs are inherently unstable, due to the two integrators (PFD/CP, VCO) in the forward path, which lead to a -180° phase shift in the open-loop phase plot. To stabilize Type-II PLLs, a stabilizing zero is typically added to the LF (to add $+90^\circ$ phase shift), in addition to a large LF capacitor to limit the open-loop gain. By contrast, Type-I PLLs have only one integrator in the forward path (VCO), which makes their open-loop phase plot start at -90° . This means that stabilizing Type-I PLLs is an inherently simple task that does not require the addition of a stabilizing zero, or a large capacitor in the LF. The smaller LF capacitor in Type-I PLLs typically leads to a smaller LF area, which is a very desirable feature.

2.4.6 Area and Power Consumption

The area and power consumption of any modern CMOS circuit have a huge impact on the feasibility of integrating the circuit within a larger IC or a system-on-chip (SoC). The area of a CMOS circuit directly impacts the cost of its manufacturing, and expensive ICs are more difficult to integrate in low-to-medium-cost consumer electronics. Furthermore, the power consumption of a battery-powered IC directly affects the depletion time of the battery. Devices with short battery lives are generally less attractive for today's consumer electronics market. As stated in the previous Section, the area of a Type-II PLL is large owing to the large LF capacitor needed for stability. On the other hand, the area of a Type-I PLL can be significantly smaller since it is more stable and does not require a large LF capacitor.

2.5 Basic PLL Circuits

2.5.1 3-State Phase-Frequency Detector (PFD)

Because of its simple digital-friendly implementation, robustness, and the fact that it serves the roles of two circuits (phase-detector and frequency-detector), the conventional 3-state PFD shown in Figure 2.9 [2], is the most commonly used type of PFD, especially in PLLs that are used as frequency synthesizers. The 3-state PFD can be realized using various circuit implementations [2], however the functionality in most cases is the same, and it can be described by the state-machine shown in Figure 2.10, and the waveform diagram in shown in Figure 2.11.

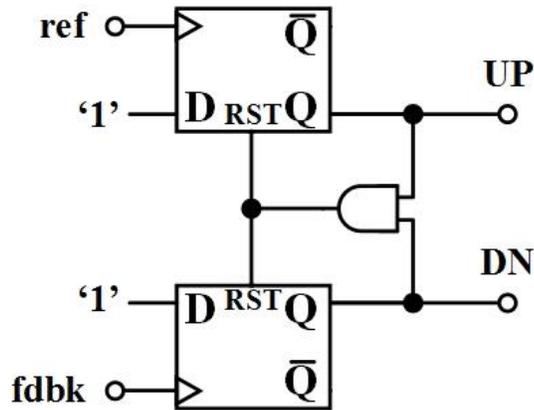


Figure 2.9 Conventional 3-state PFD schematic

The task of the 3-state PFD is to provide Up (UP) and Down (DN) signals that allow the PLL to increase or decrease its output frequency based on the phase difference of between the reference and feedback signals. As the state-machine (Figure 2.10) shows, in its default state (standby), both outputs of the PFD are at logic low (UP = '0', DN = '0'). If a reference rising edge arrives before the feedback rising edge, the state of the PFD will change to UP = '1' and DN = '0', indicating that the VCO must increase its frequency to catch up with the reference signal. The PFD will remain in the previous state until a feedback rising edge arrives, in which case the output of the PFD will reset to the default state (UP = '0', DN = '0'), providing an output that is linearly proportional to the phase difference between the two input signals. This behavior can be seen in Figure 2.11.

In contrast, if the feedback rising edge arrives before the reference rising edge, the state of the PFD will change from the default to UP = '0' and DN = '1', indicating that the VCO must slow down, and it will stay in that state until a reference rising edge arrives, in which case it will reset to the default state. This behavior leads to an output that is proportional to the phase difference between the two input signals.

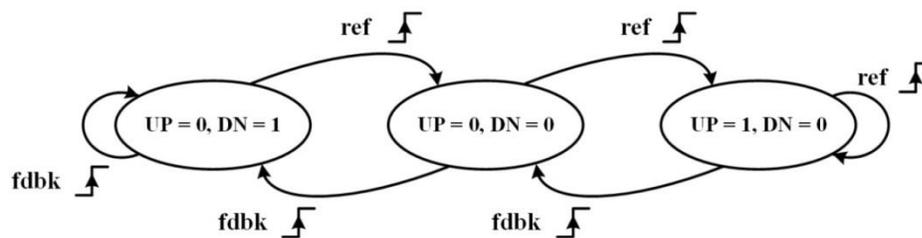


Figure 2.10 Conventional 3-state PFD state-machine

Figure 2.11 shows how the duration of the UP is proportional to the delay between the two input signals. The delay of the UP signal, and the narrow DN pulses are non-idealities that are caused by the delay of the flip-flops and the AND gate.

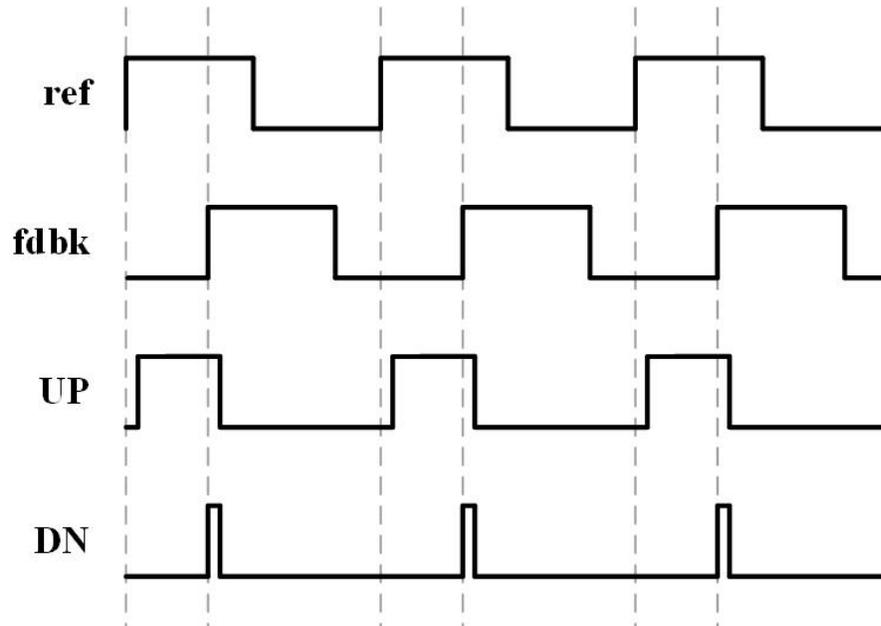


Figure 2.11 Conventional 3-state PFD waveforms

2.5.2 Charge-Pumps (CP)

The charge-pump (CP) is an analog circuit block that takes the PFD output, and converts it to an analog current signal. The following sub-sections describe CPs for Type-II and Type-I PLLs.

2.5.2.1 CP in Type-II PLLs

The CP in a Type-II PLL takes the digital UP and DN ($\overline{\text{DN}}$) pulses from the PFD, and outputs an analog signal that is proportional to the integral of their difference. Figure 2.12 shows a schematic of the basic CP which is typically used in Type-II PLLs [2].

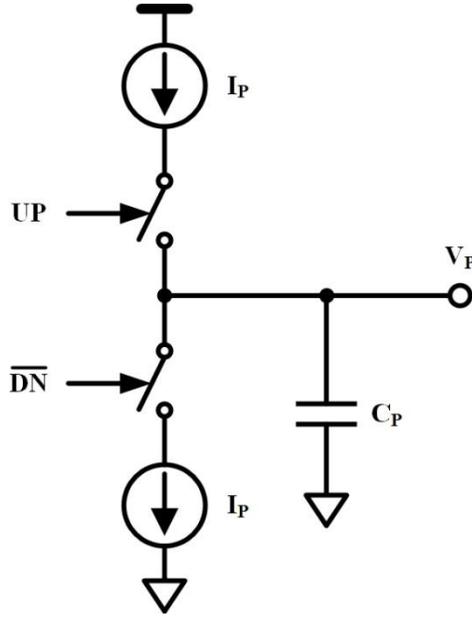


Figure 2.12 Basic CP for Type-II PLLs

Equation (2.17) shows the transfer function from the input of the 3-state PFD to the output of the CP shown in Figure 2.12. The $1/s$ term in Equation (2.17) indicates that the PFD/CP combination in a Type-II PLL acts as an integrator. Furthermore, the gain of the PFD/CP is proportional the charge pump current (I_P), and inversely proportional to the integrating capacitor C_P .

$$\frac{V_P}{\Delta\theta}(s) = \frac{1}{s} * \frac{I_P}{2\pi C_P} \quad (2.17)$$

Although the schematic shown in Figure 2.12 looks very simple, the actual work that goes into designing a CP for Type-II PLLs is very challenging, and requires dealing with many issues, such as designing low-noise, high-output-impedance current sources, matching the values of the UP/DN currents, designing their biasing circuitry, designing and matching of the current switches that must be designed to minimize charge-sharing and clock-feedthrough [7].

2.5.2.2 CP in Type-I PLLs

Unlike in a Type-II PLL, the PFD/CP in a Type-I PLL does not act as an integrator. This simple difference in the desired behavior can lead to significantly simpler PFD/CP

implementations in Type-I PLLs. Figure 2.13 shows one approach for implementing a Type-I PLL CP [8]. Unlike Type-II PLLs, we did not find a dominant approach for implementing the CP in Type-I PLLs. This is mainly due to the relatively limited number of recent publications dealing with Type-I PLLs.

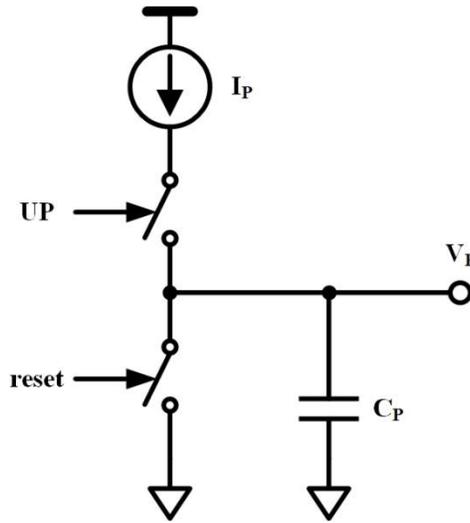


Figure 2.13 Integrate-and-reset CP for Type-I PLLs

The CP shown in Figure 2.13 only uses the UP signal from the PFD (Figure 2.9), and it works by outputting an analog voltage that is proportional to the width (time) of the UP pulse. In a sense, the CP in Type-I PLLs works as a simple time-to-voltage converter. Note that the CP shown in Figure 2.13 is intended for use with a discrete time LF, which means that its output is sampled and then reset at the end of each integration cycle.

Equation (2.18) approximates the transfer function of the CP shown in Figure 2.13. Note how the PFD/CP in a Type-I PLL behaves as a proportional gain block, rather than an integrator.

$$\frac{V_P}{\Delta\theta}(s) = \frac{I_P}{2\pi C_P} \quad (2.18)$$

Although the CP shown in Figure 2.13 is easier to design than the CP shown in Figure 2.12, it still has its own limitations, such as the need for a biasing circuit, and the limited voltage headroom due to the current source which limits the range of the VCO control voltage, and thus limiting the overall PLL lock-range.

Chapter 3: Proposed PLL Architecture

3.1 Limitations of Prior-Art Type-II and Type-I PLLs

Designing high performance CMOS PLLs has been almost an art in itself. Type-II CP-based analog PLLs, the overwhelming popular choice, require several considerations and tradeoffs between loop-bandwidth, stability, area, phase-noise, reference-spur, lock-time, and power-consumption. Loop-stability requires stabilizing zero in LF, necessitating careful design and simulation, and a significant expense of area-consuming capacitors. Phase-noise considerations put severe restrictions on CP design and power-consumption. The design methodology has only become more difficult with CMOS scaling. Scaling of CMOS devices has resulted in reduced output impedance of short-channel transistors, as well as reduction in supply voltage in order to prevent damaging the oxide due to its reduced thickness. This has led to degraded performance of current source circuits in short-channel transistors. At low supply voltages, analog circuit blocks such as operational amplifiers and CPs are particularly difficult to design. Use of thin oxide also exacerbates the current leakage through them, which results in increased reference spur at the PLL output. Clearly, the analog-intensive methodology and CP-based Type-II PLL takes significant design-time, and consumes substantial die area. All-digital PLLs do not need LF capacitors or CPs, are scaling-friendly, but have strict jitter requirements on TDCs. They also consume more power than the analog PLLs in lower-cost, older CMOS processes.

Type-I PLLs do not require an integrator in the LF, with the VCO constituting the sole integrator in the loop, unlike Type-II PLLs. This makes Type-I PLLs easier to design for stability, requiring a low-area capacitor in the LF as no zero-stabilizing resistors are needed [7]. However, the limited performance of Type-I PLLs has restricted its usage. Lack of integration in the LF limits loop gain, constraining the locking range, while lock-acquisition with a static phase offset results in significant reference spur due to the persistent ripple on the VCO control line [7]. To overcome these limitations, prior efforts have used auxiliary loops [9, 10], or auxiliary LF paths with a quasi-Type-II/I implementation [6]. However, these implementations still require CPs and other analog components, have significant design complexity, and the performance in terms of phase-noise, reference spur and power

consumption must still be improved. In this work, we propose a Type-I PLL that overcomes the limitations of Type-I PLLs, while achieving performance comparable to Type-II PLLs in noise and spur. The proposed PLL architecture is scaling-friendly due to lack of any voltage/current bias circuits, CPs and amplifiers, achieves low power and low LF area.

Table 3.1 summarizes the advantages and disadvantages of the Type-II, Type-I [6] and the proposed boosted-gain Type-I PLL architectures.

	Conventional Type-II	Conventional Type-I	Proposed
Lock-Range	Good	Poor	Good
Reference-Spur	Good	Poor	Good
Stability	Poor	Good	Good
Area	Poor	Good	Good

Table 3.1 PLL architecture comparison

3.2 Boosted-Gain Type-I PLL

Figure 3.1 shows the block diagram of the proposed Type-I PLL where the conventional CP current output has been replaced by a PWM voltage output from the PFD. The voltage output is fed to an LF consisting of a single pole RC filter. Such a simple LF is made possible due to the inherent stability of Type-I PLLs because of the lower number of poles in the forward path [9]. This enables the use of a relatively small filter capacitor by eliminating the need for adding a zero in the loop filter for stabilization as in Type-II PLLs. This topology makes the design of the proposed PLL significantly simpler as well as more portable to different CMOS processes. In the following sections, further enhancements to the Type-I PLL are discussed.

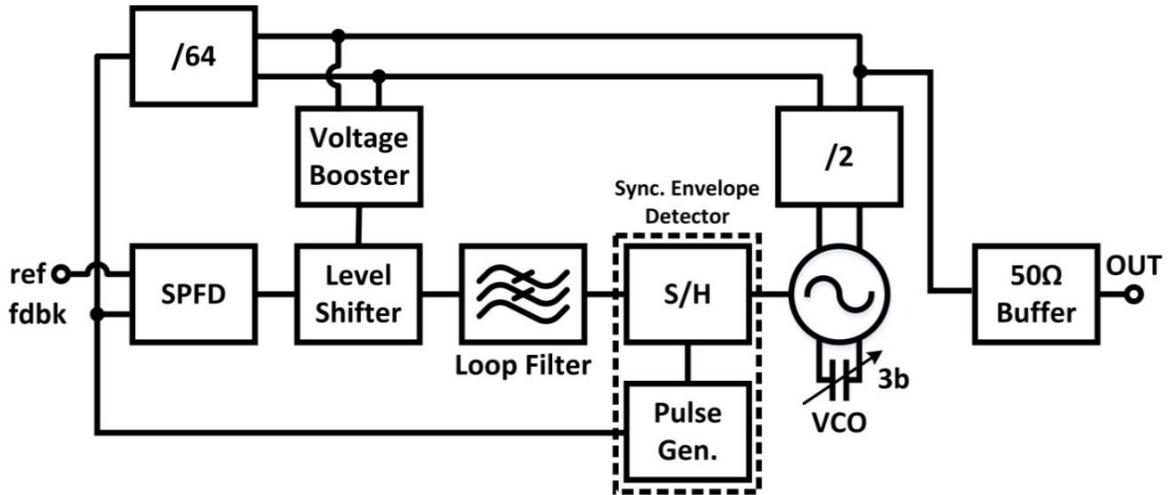


Figure 3.1 Block diagram of the proposed Type-I PLL

3.3 Voltage Booster for Higher Loop-Gain and Lock-Range

A standard digital level shifter (shown in Figure 3.2) [11] translates the output of the SPFD from the nominal supply voltage (1.2 V) to a higher voltage level ($V_{\text{Boosted}} \approx 2.2$ V). Boosting the SPFD output signal leads to a proportional boost in the forward gain of the system, this in turn improves the lock-range of the overall PLL (as indicated by Equation (2.16)). The idea of boosting the forward gain of Type-I PLLs has been explored in [6], where a linear amplifier introduces a zero to boost the forward gain of the PLL, leading to a Type-II-like operation.

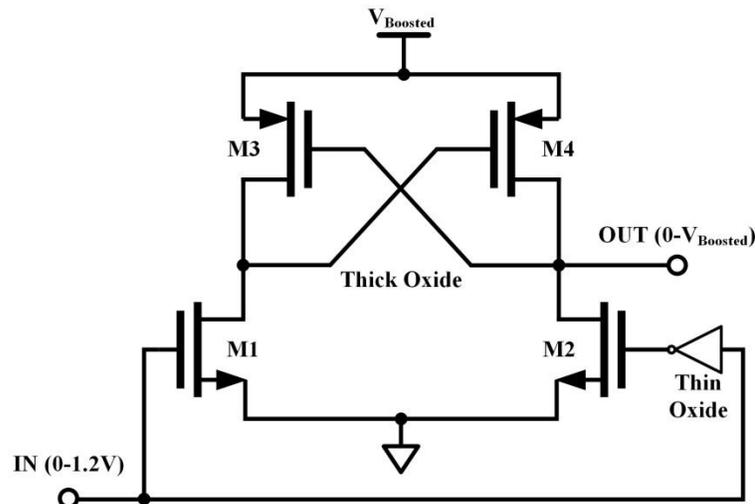


Figure 3.2 Digital level-shifter schematic

In contrast to [6], the proposed solution here does not raise loop stability concerns, or require analog amplifiers, current sources and biasing circuits. The high voltage (2.2 V) is generated using a small-area voltage booster (shown in Figure 3.3) from a 1.2 V supply. Initially proposed by [12] as a CMOS rectifier, and modified herein as a voltage booster, this structure is simple to design, efficient, and does not require any biasing circuitry. Furthermore, it can be clocked over a wide range of frequencies. In this work, it is clocked using the divided-by-2 VCO output frequency (~ 1.23 GHz). Clocking with a high frequency ensures that any spurs introduced by the switching are significantly attenuated by the low-pass response of the PLL. Moreover, the required capacitances (C_{AC} , C_F , shown in Figure 3.3) are also scaled down. For improved reliability, the voltage booster and the level shifter are designed using thick oxide MOS transistors (I/O devices). It should be noted that almost all advanced CMOS processes offer such thick oxide devices for I/Os.

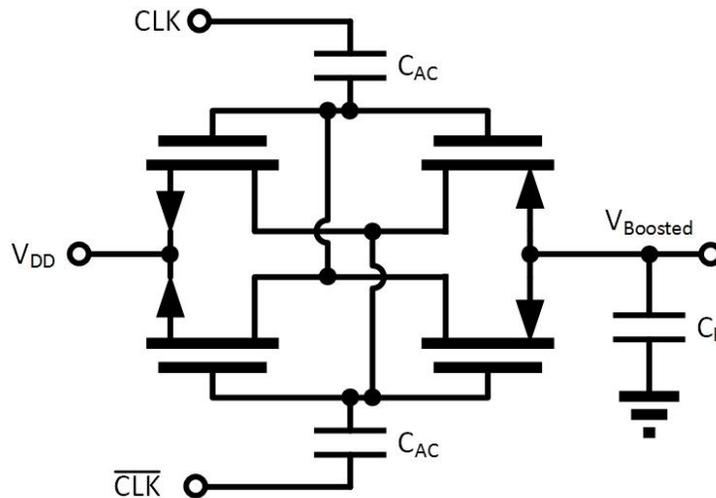


Figure 3.3 Proposed voltage booster

3.4 Saturated-PFD for Improving Lock-Time and Lock-Range

An ideal PFD must generate a linear output proportional to the phase difference of its two input signals, regardless of their relative phase difference. However, conventional 3-state PFDs [7, 6] suffer from cycle-slipping, attributed to the reset of the PFD output signal when the input phase difference is around $2\pi n$, where $n = \pm 1, 2, 3, \dots$, as shown in Figure 3.4. Eliminating cycle-slipping results in a faster, more predictable transient behavior, and an

increased acquisition speed [13, 14]. Figure 3.5, shows the step responses of two identical representative Type-I PLL systems, with the only difference being that a conventional 3-state PFD is used in one of them, and the proposed 5-state SPFD used in the other. Figure 3.5 was generated by feeding the same reference frequency to both PLLs, and as we can see, the PLL with the conventional 3-state PFD is not even able to lock since the provided frequency is outside of its lock-range. On the other hand, the PLL with the SPFD locks quickly, which indicates a lock-range extension that can be attributed to the use of the proposed SPFD.

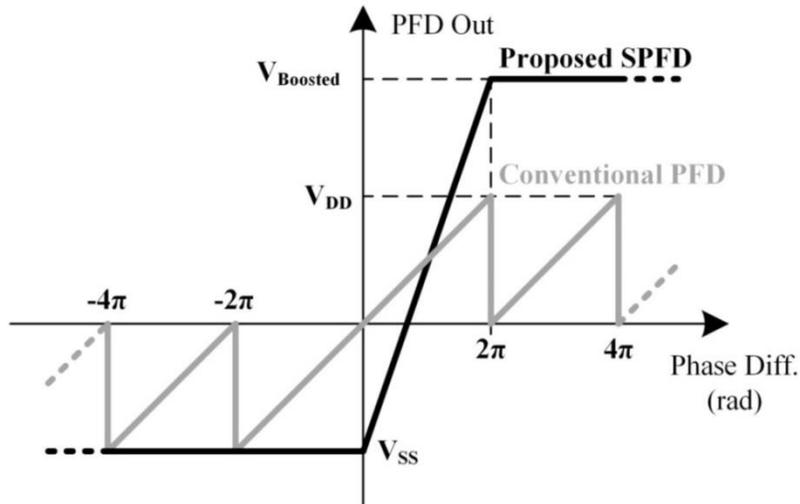


Figure 3.4 Saturated vs. Conventional PFD Transfer Functions

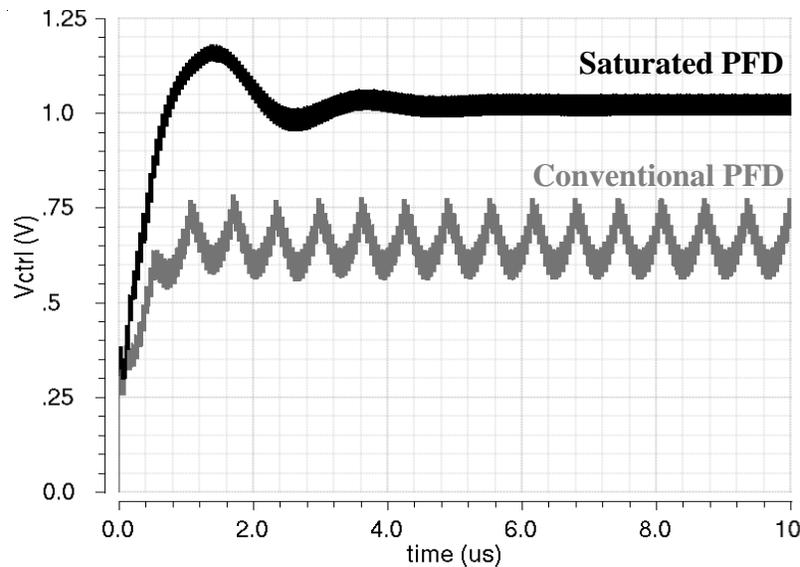


Figure 3.5 Type-I PLL loop-dynamics with a conventional PFD vs. SPFD: response of the VCO control voltage (simulated) to a step in the reference frequency.

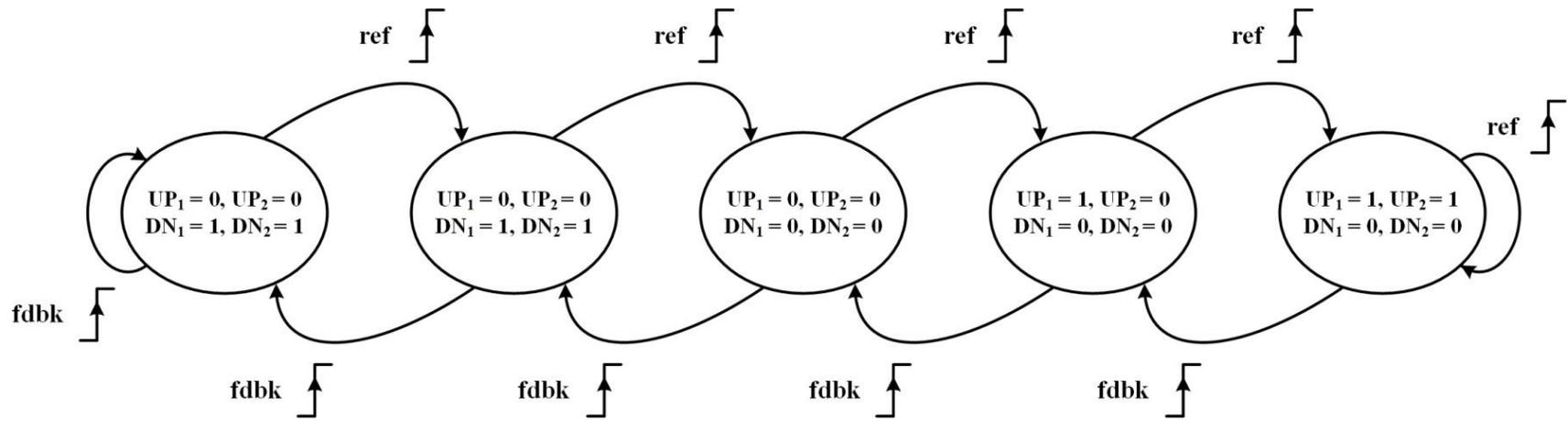


Figure 3.7 Proposed SPFD state-machine

3.4.1 Dynamic, True-Single-Phase-Clocked (TSPC), D-Flip-Flop (DFF)

Dynamic, true-single-phase-clocked (TSPC) D-Flip-Flops (DFFs) offer great advantages in terms of speed, area [15, 16] and power. Figure 3.8 shows the schematic of the TSPC DFF that has been used in the proposed SPFD, divider (/64), and pulse generator. Just as the name suggests, TSPC DFF only needs a single phase of the clock for latching the input data, as compared to the two-phase clocking that standard static DFF implementations need. The main advantages of single phase clocking is that it obviates the need for non-overlapping clock phases, eases routing, in addition to power savings in the clock distribution network. It has also been shown that TSPC based PFDs can lead to significant reduction (up 6 dB) in the PLL phase-noise when compared to static DFF based PFDs [17].

Many variations of the TSPC DFF have been presented in the literature. The TSPC DFF shown in Figure 3.8 is based on a design that was first introduced in [15].

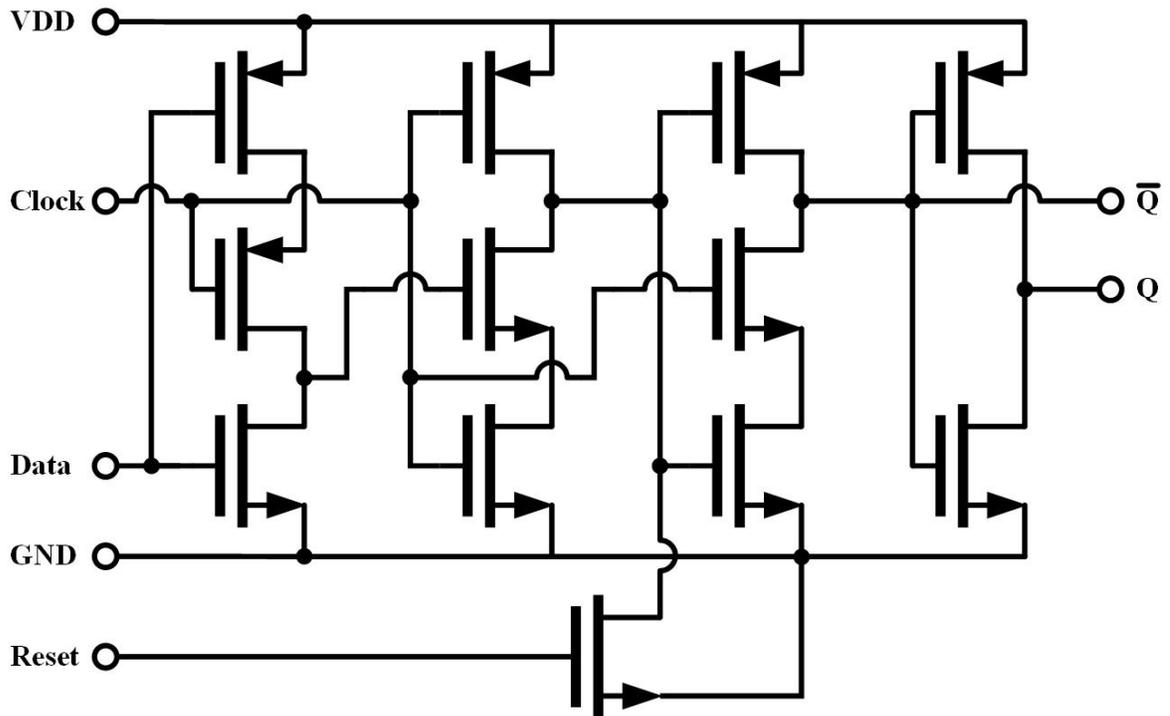


Figure 3.8 TSPC flip-flop schematic

The main disadvantage of using TSPC DFFs is that they need to be refreshed in order to keep the stored value intact. This problem translates into a limit on the minimum clocking

frequency of the TSPC DFF, which typically ranges from few hundreds of kilohertz to few megahertz, depending on the technology and the design. This problem can lead to reduced yields in large scale digital IC manufacturing, which is why the static DFF typically is preferred. The minimum frequency problem does not prevent us from using TSPC DFFs in the proposed PLL, since whenever the PLL is powered and the reference is provided, all the TSPC DFFs in the system will be continuously clocked with frequencies that never go below 15 MHz.

3.5 Synchronous Envelope Detector for Spur-Reduction

Figure 3.9 shows the proposed LF and the S/H circuit. The loop filter consists of a simple single pole RC filter (R1, C1). In a Type-I PLL, the loop locks with a static phase offset, in a region where the loop gain is more linear, but this creates a periodic disturbance on the VCO control line. This reference spur is suppressed by adding an S/H circuit. Prior implementations of S/H circuits in CP-based Type-I PLLs [7, 9, 10] have required different sample, hold and reset signals, and have incorporated the S/H circuit as an additional pole. In our proposed voltage-mode implementation, the S/H circuit is effectively working as a synchronous envelope detector, or a passive down-converting mixer. Since the sample capacitor, C2, is significantly smaller than the loop filter capacitor, C1, the S/H circuit does not have a significant impact on the transfer function of the system.

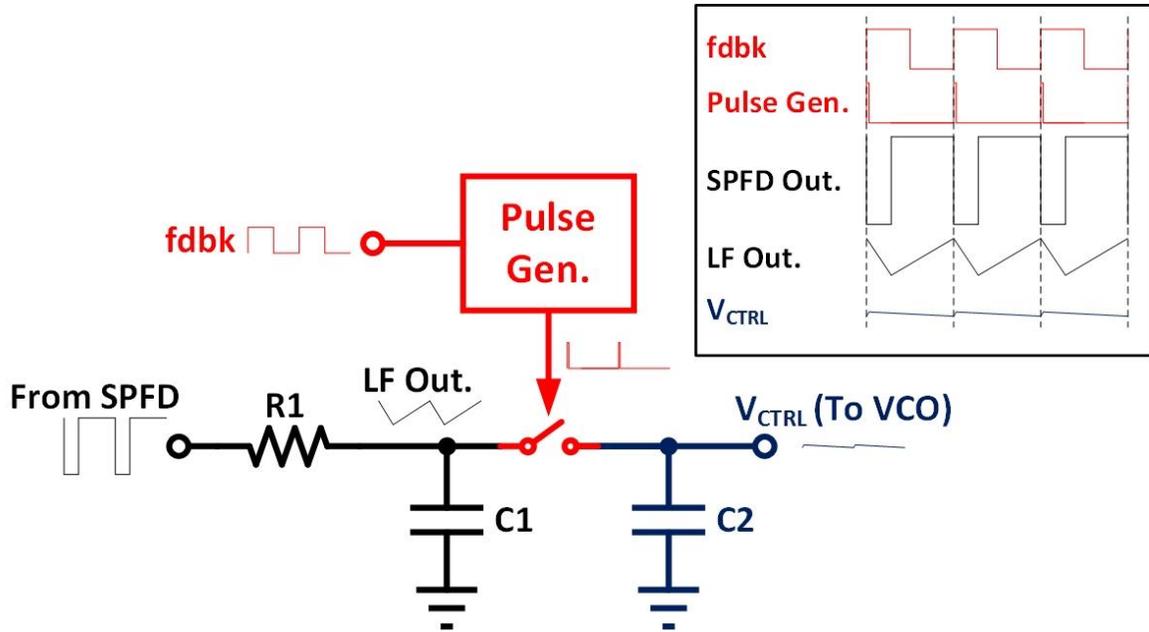


Figure 3.9 LF with the S/H as a synchronous envelope detector

The proposed circuit implementation of the pulse generator circuit, which is shown in Figure 3.10, is based on a simple TSPC DFF and a short, inverter chain based, delay line. The width of the pulse generated by the proposed circuit is proportional to the combined delays of the reset action of the DFF, in addition to the propagation delay caused by the delay line. This circuit was designed to generate pulse widths of approximately 1.2 ns; however the exact pulse width depends on the specific PVT conditions. Although undesirable, the simulated variations in the pulse width are too small to have any noticeable impact on the performance of the PLL.

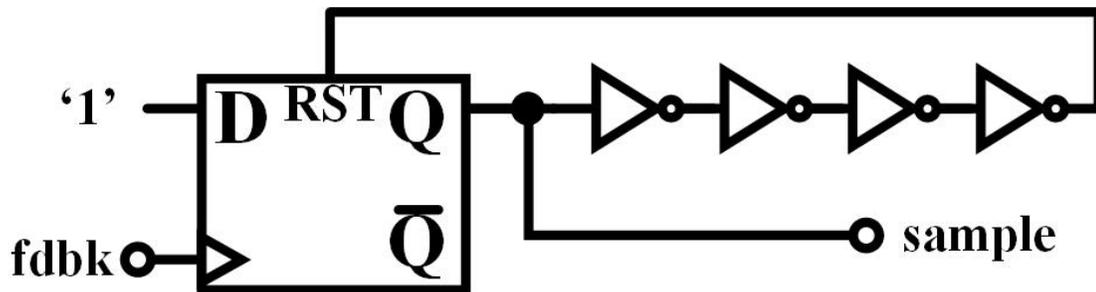


Figure 3.10 Pulse generator schematic

3.6 Resistor Degenerated VCO

The VCO used in this design (shown in Figure 3.11) is a complementary cross-coupled LC-VCO with a 3-bit capacitor bank, and source-damping resistors similar to [18]. The source damping resistors help reduce the VCO output phase noise by preventing the flicker ($1/f$) noise of the VCO transistors from being up-converted to phase-noise [18]. According to [18], up to 6 dB of phase-noise improvement can be observed after adding the source-degeneration resistors, however based on our simulations a maximum improvement of 2.1 dB was observed. The values of R1 and R2 are $40\ \Omega$ and $25\ \Omega$, respectively, and were chosen based on simulations to minimize the VCO phase-noise.

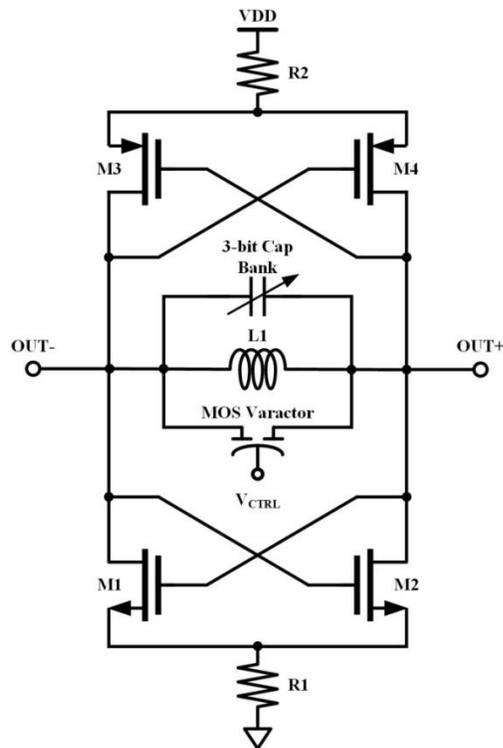


Figure 3.11 Resistor-degenerated LC-VCO with a 3-bit capacitor bank

The 3-bit capacitor bank was added to increase the tuning range of the VCO, without increasing the VCO gain (K_{vco}), since higher VCO gain leads to higher reference-spur, as Equation (2.14) suggests. Figure 3.12 shows the simulated tuning curves of the proposed VCO, and was generated by sweeping the capacitor bank value from b000 to b111, and for each capacitor bank value, the VCO control line voltage (V_{CTRL}) was swept from 0 V to 1.2 V.

The simulated VCO gain is approximately 190 MHz/V at the center of the tuning curves Figure 3.12, which is the nominal operating point, and it is reduced near the edges of the tuning curves. Furthermore, the simulated tuning range is approximately from 2.2-to-2.8 GHz. The tuning range can easily be increased by increasing the number of bits in the capacitor bank, however since this is just a proof of concept, we decided to limit the capacitor bank to 3-bits.

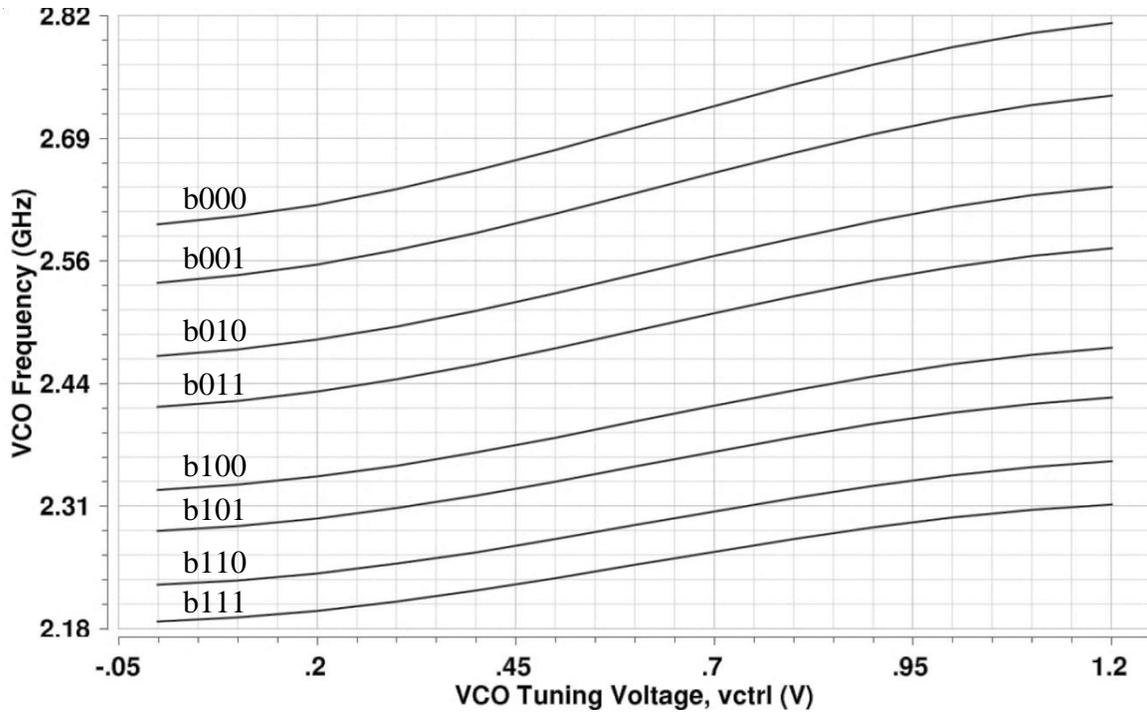


Figure 3.12 Simulated VCO tuning curves for different capacitor bank values

Chapter 4: Layout and Printed Circuit Board Design

4.1 PLL Layout

Figure 4.1 shows the layout of the proposed boosted-gain Type-I PLL. The layout was done in Cadence Virtuoso Layout Suite using full custom layout techniques. 13 pads are used in total; each of which is connected to electro-static-discharge (ESD) protection diodes. Attention was given to noise and cross-talk minimization, which is why the chip was powered through multiple supplies: one for the VCO (analog), one for the rest of the PLL (mostly digital), and a third supply that was used to power the 50 Ω output driver, which is needed for performing lab measurements. Furthermore, most of the unoccupied areas of the die were filled with power supply decoupling capacitors.

4.1.1 VCO Layout

VCO layout can have a huge impact on the quality of its performance, which is why special attention was given to the VCO. The following steps were taken to maximize the quality of the VCO performance:

- A large, top-metal, symmetric inductor was used due to its high quality factor.
- Large distance was kept between the inductor and any wires, capacitors and fillings, especially on top metal layers to prevent quality factor degradation.
- Metal-Insulator-Metal (MIM) capacitors were used in the capacitor bank of the VCO due to their linearity and high quality factors.
- The varactor was divided into interleaving fingers, and was laid-out symmetrically to minimize the effects of the systematic process variations.
- The inductor and capacitors of the VCO were connected using thick top-metal wires to prevent quality factor degradation.
- The VCO transistors were laid-out symmetrically and guard rings were added to minimize noise and cross-talk coupling through substrate.
- Supply decoupling capacitors were used in the empty areas of the die to filter the supply noise and ripple.

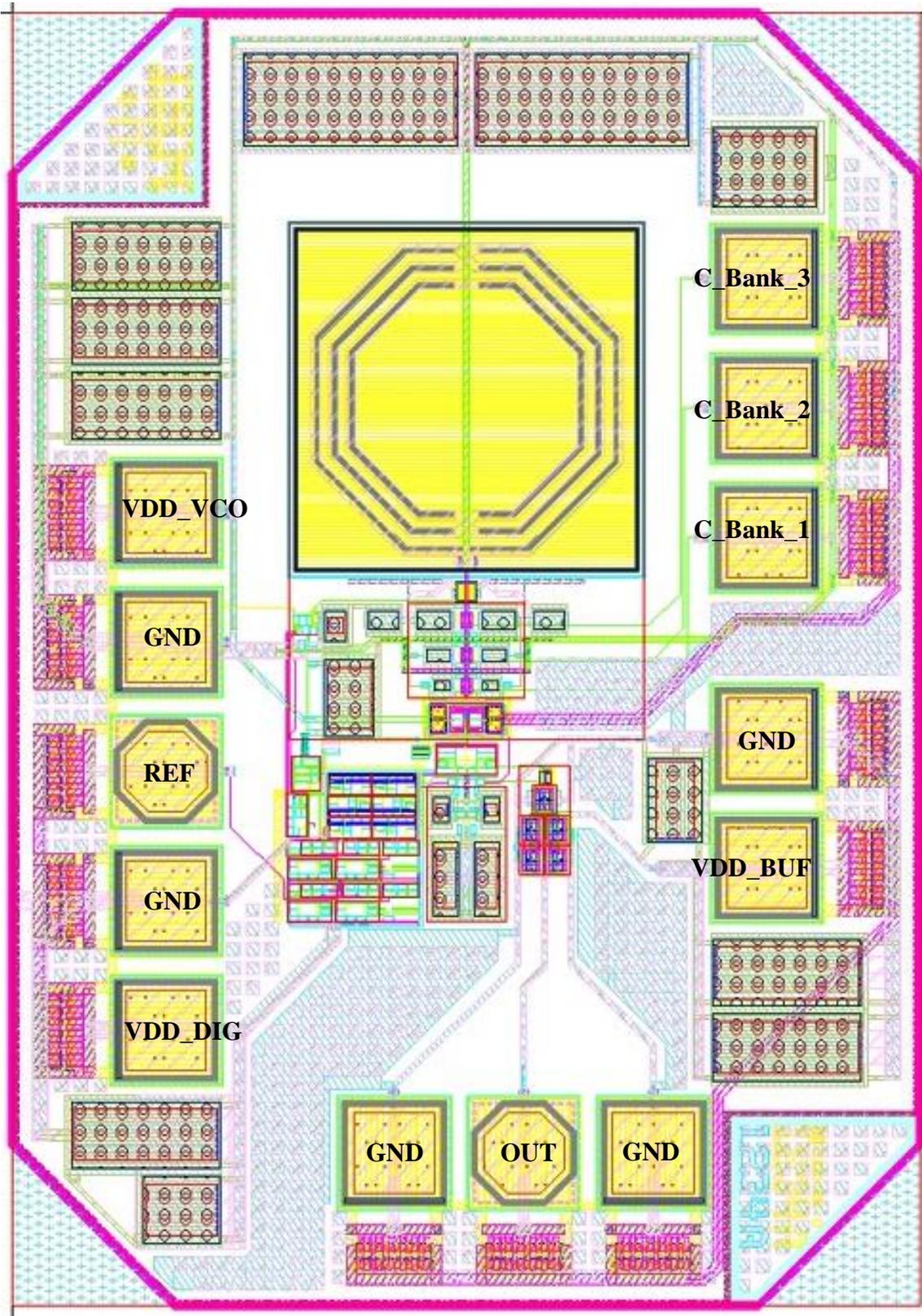


Figure 4.1 Layout of the boosted-gain Type-I PLL

4.2 Packaging

A handful of the fabricated chips (5 out of 40) were packaged in a 24-pin ceramic-flat-package (CFP-24) by MOSIS. Packaging helps in protecting the chip from accidental damage, in addition to simplifying the measurement procedure, since all the measurements can be performed with the packaged chip soldered directly onto a custom made test board instead of using an RF probe station.

4.3 PCB Design and Measurements Setup

4.3.1 First PCB Design

Figure 4.2 shows the first PCB that was designed and fabricated for characterizing the proof-of-concept PLL chip. This circuit was manufactured on a standard 2-layer PCB, with 35 μm copper thickness on each side. The board dimensions are 30 \times 50 mm. The bottom layer (not shown) is mostly a ground plane, and the top layer (shown in Figure 4.2) contains all of the components, and most of the routing.

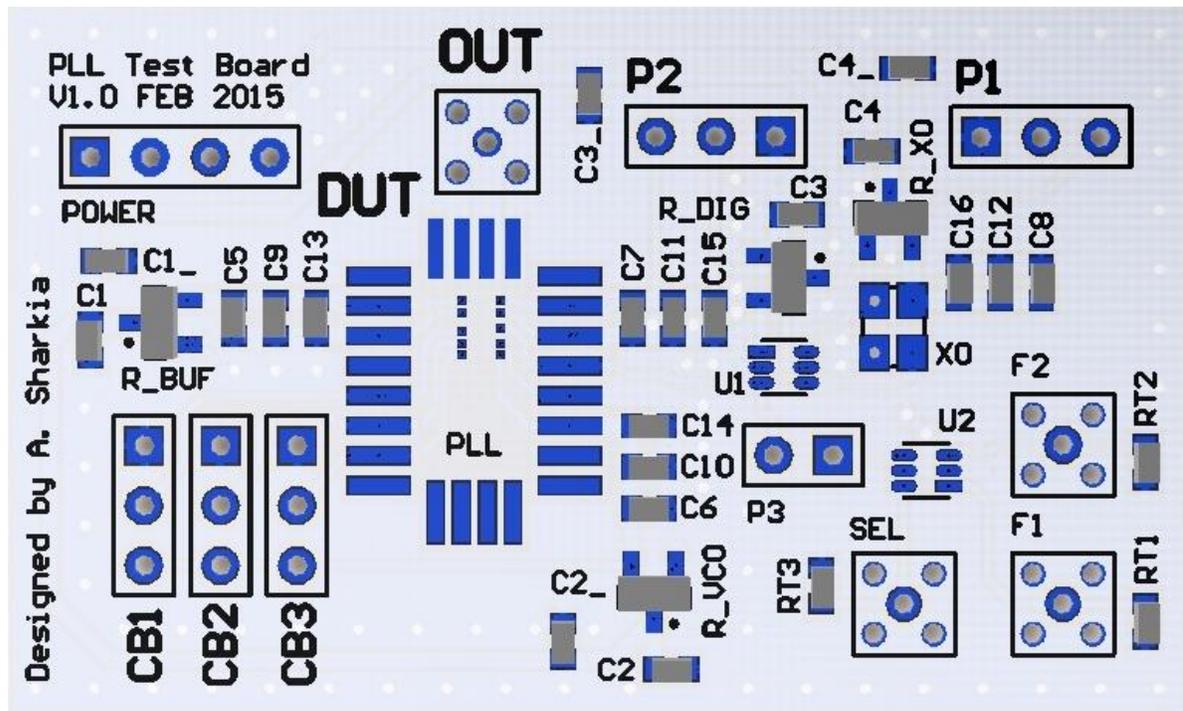


Figure 4.2 First PCB design

This PCB was designed and used for performing the following measurements:

- Phase-noise
- Spectrum (including spurs)
- Lock-time (frequency step response)
- Jitter
- Power consumption

However the initial in-band phase-noise measurements were significantly worse than the expected values (from simulations). This led us to discovering that the linear low-dropout regulators (LDOs) that were used to power the PLL were the cause of the unexpectedly high phase-noise. This meant that a second PCB had to be designed for the purposes of phase-noise and jitter measurements, as described in Section 4.3.2.

This PCB contains a digital 2-to-1 multiplexer (mux) whose output is connected the input (reference node) of the PLL. The 2-to-1 mux was included to enable us to accurately measure the frequency step response of the PLL. The step response measurement was performed by quickly switching (using the mux) between two reference signals with different frequencies (provided by external signal generators), and monitoring the output of the PLL using an Agilent E5052A Signal Source Analyzer (SSA).

The power consumption of the PLL was measured by first bypassing the LDOs, powering the PLL from an external power supply, and measuring the current consumption of circuit. The power consumption measurement was done while the PLL is locked to the XO reference, which has a frequency of 19.2 MHz.

4.3.2 Second PCB Design

A second PCB, shown in Figure 4.3, was designed to enable the accurate measurement of the phase-noise, jitter and spectrum of the PLL without the being affected by the power supply noise. To achieve this goal, the second PCB replaces the standard LDOs from the first PCB with the ADM7154, which is an ultralow noise, high power-supply-rejection-ratio (PSRR) linear regulator that is designed specifically for RF and PLL applications [19].

In addition to the ultralow noise regulators, the second PCB includes many high quality power supply bypass capacitors that are placed very close to the pads of the package. The values of these bypass capacitors range from 1 nF to 100 μ F, in order to guarantee supply noise filtering on both ends of the spectrum.

The second circuit was manufactured on a standard 2-layer PCB, with 35 μ m copper thickness on each side. The board dimensions are 52 \times 85 mm. The bottom layer (not shown) is mostly a ground plane, and the top layer (shown in Figure 4.3) contains all of the components, and most of the routing.

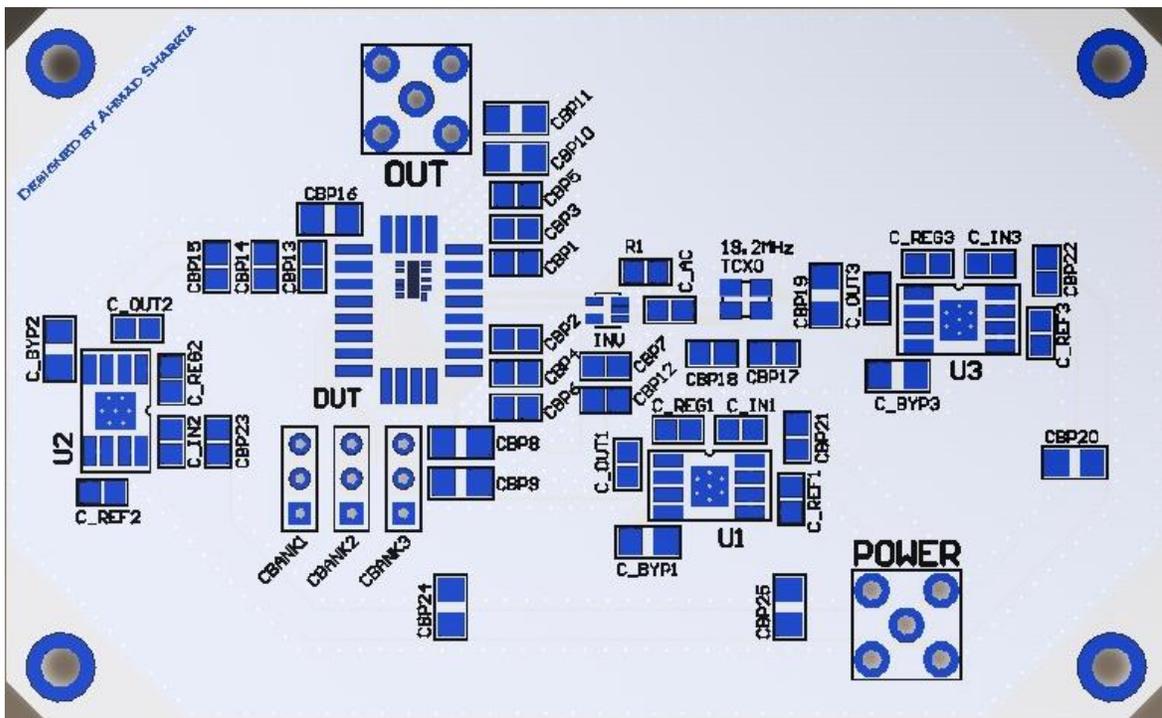


Figure 4.3 Second PCB design

Chapter 5: Simulation and Measurement Results

The proposed boosted-gain Type-I PLL is implemented on a $0.7 \times 1 \text{ mm}^2$ die on IBM's $0.13\text{-}\mu\text{m}$ 8-metal RF CMOS process (CMRF8SF). Figure 5.1 shows the die micrograph with the different circuit blocks clearly labeled. The test die is housed in a 24-pin ceramic flat package (CFP-24), and is characterized using a 19.2 MHz reference frequency, while being powered from three 1.2 V regulators (for VCO, PLL, and 50Ω buffer).

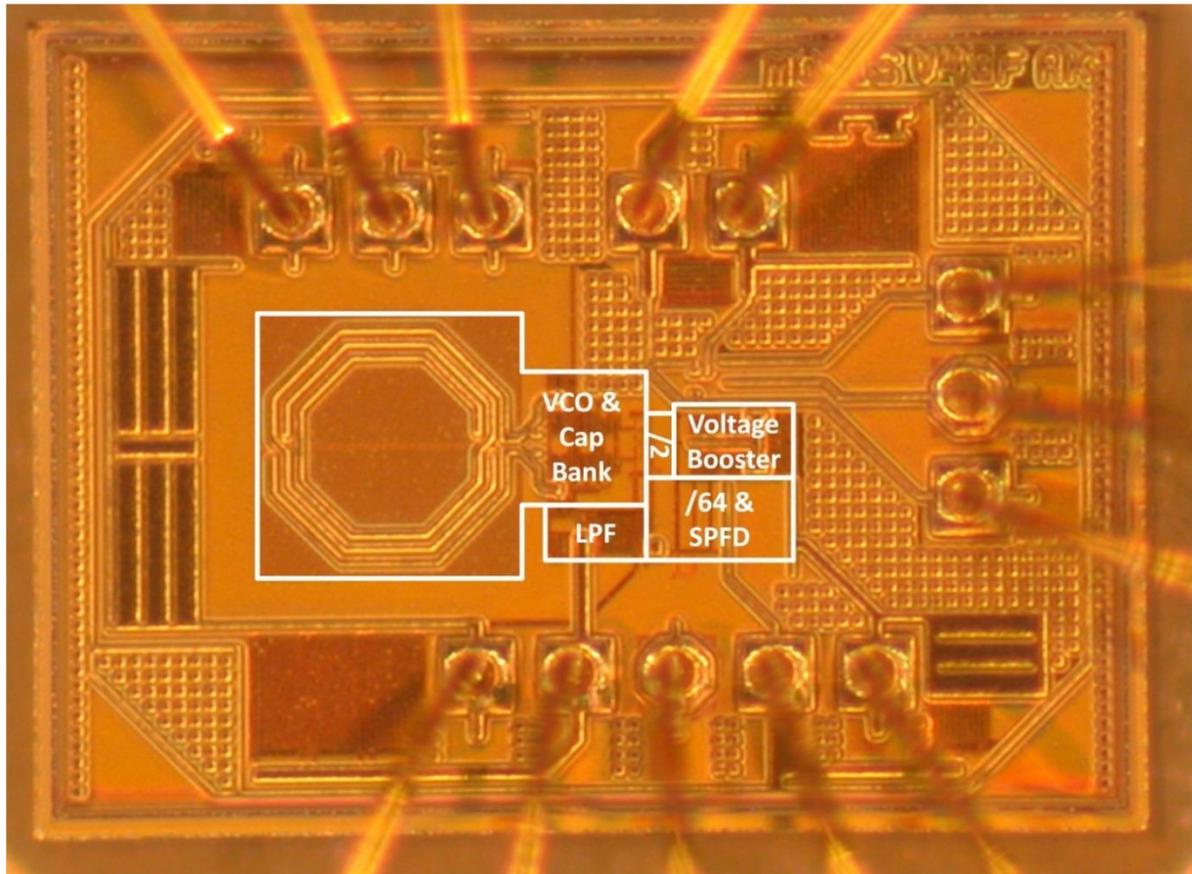


Figure 5.1 Die micrograph

Total core area of the PLL is 0.12 mm^2 , out of which the LF and S/H synchronous envelope detector occupy an area of 0.005 mm^2 , while the voltage booster consumes an area of 0.006 mm^2 . All measurements are conducted with the divided-by-2 output of the VCO (Figure 3.1). Therefore, the phase-noise and spur measurements need to be scaled by +6 dB to compensate for this frequency division.

5.1 Simulated PLL Bandwidth

Figure 5.2 shows the closed-loop Bode plot resulting from the mathematical analysis and simulation of the proposed PLL. It can be seen that the low-frequency (DC) gain of the PLL is 42.1 dB, which corresponds to a frequency gain of 128, since $20 \log_{10}(128) = 42.1 \text{ dB}$. The -3 dB bandwidth of the PLL is around 660 kHz. This bandwidth was chosen such that the overall PLL phase-noise is minimized. Furthermore, the simulated phase-margin of the PLL is 71° , which indicates that the proposed PLL is highly stable, since phase-margin values of 55° and above are typically desired for a stable system.

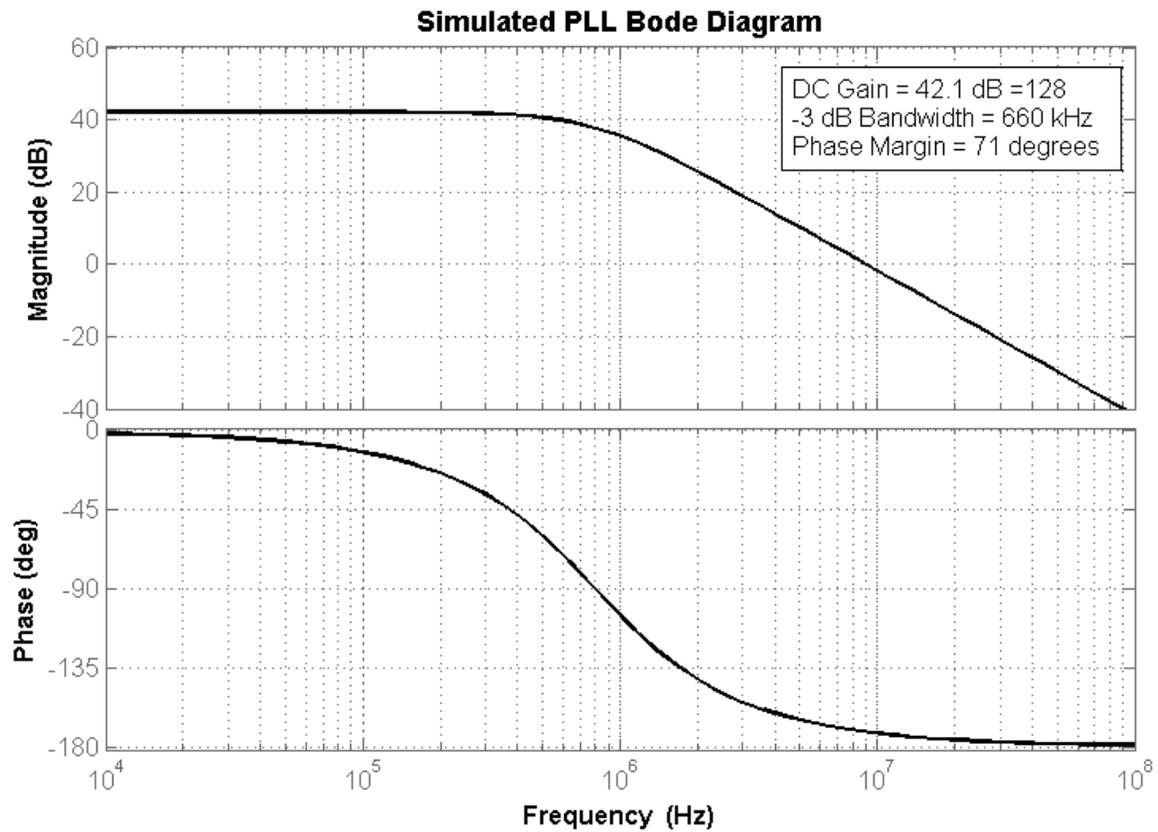


Figure 5.2 Simulated closed-loop PLL Bode plot (top: amplitude; bottom: phase)

5.2 Phase-Noise

5.2.1 Simulated Phase-Noise

Figure 5.3 shows the simulated output-referred phase-noises of the various circuit blocks (PFD/CP, divider and VCO), the output-referred phase-noise of the reference signal (from TCXO datasheet), and the overall phase-noise of the PLL, which is obtained by combining the contributions of all the noise sources. At the center frequency of ~ 2.4 GHz, the simulated in-band phase-noise at a 100 kHz offset is -105 dBc/Hz. Figure 5.3 clearly indicates that the in-band phase-noise of the PLL is dominated by the phase-noise of the TCXO. This means that a higher quality reference oscillator, such as an Oven-Controller Crystal-Oscillator (OCXO), is expected to lead to up to 11 dB improvement in the-band phase-noise of the PLL output.

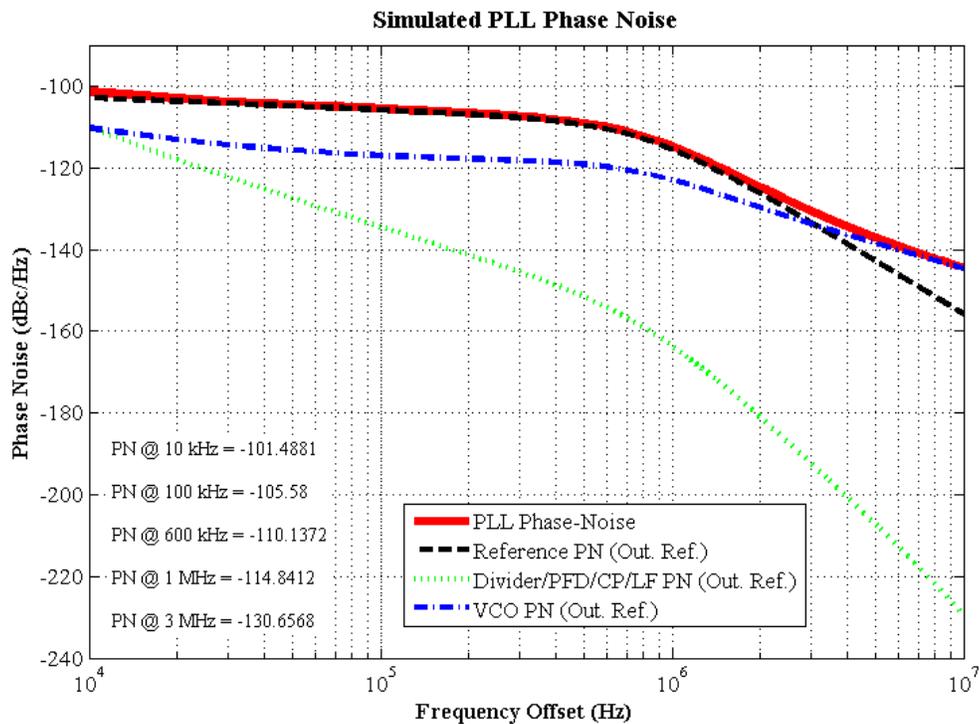


Figure 5.3 Simulated PLL phase-noise breakdown (output referred)

5.2.2 Measured Phase-Noise

All phase-noise measurements were performed using an Agilent E5052A SSA. Figure 5.4 shows the measured phase-noise plot of the divided-by-2 output of the PLL. At the center frequency of 1.23 GHz, the measured in-band phase-noise at a 100 kHz offset is -109.4 dBc/Hz, which corresponds to -103.4 dBc/Hz for PLL output frequency of 2.46 GHz. Lack of charge-pumps and large resistors in the LF results in the in-band phase-noise being dominated by reference phase-noise.

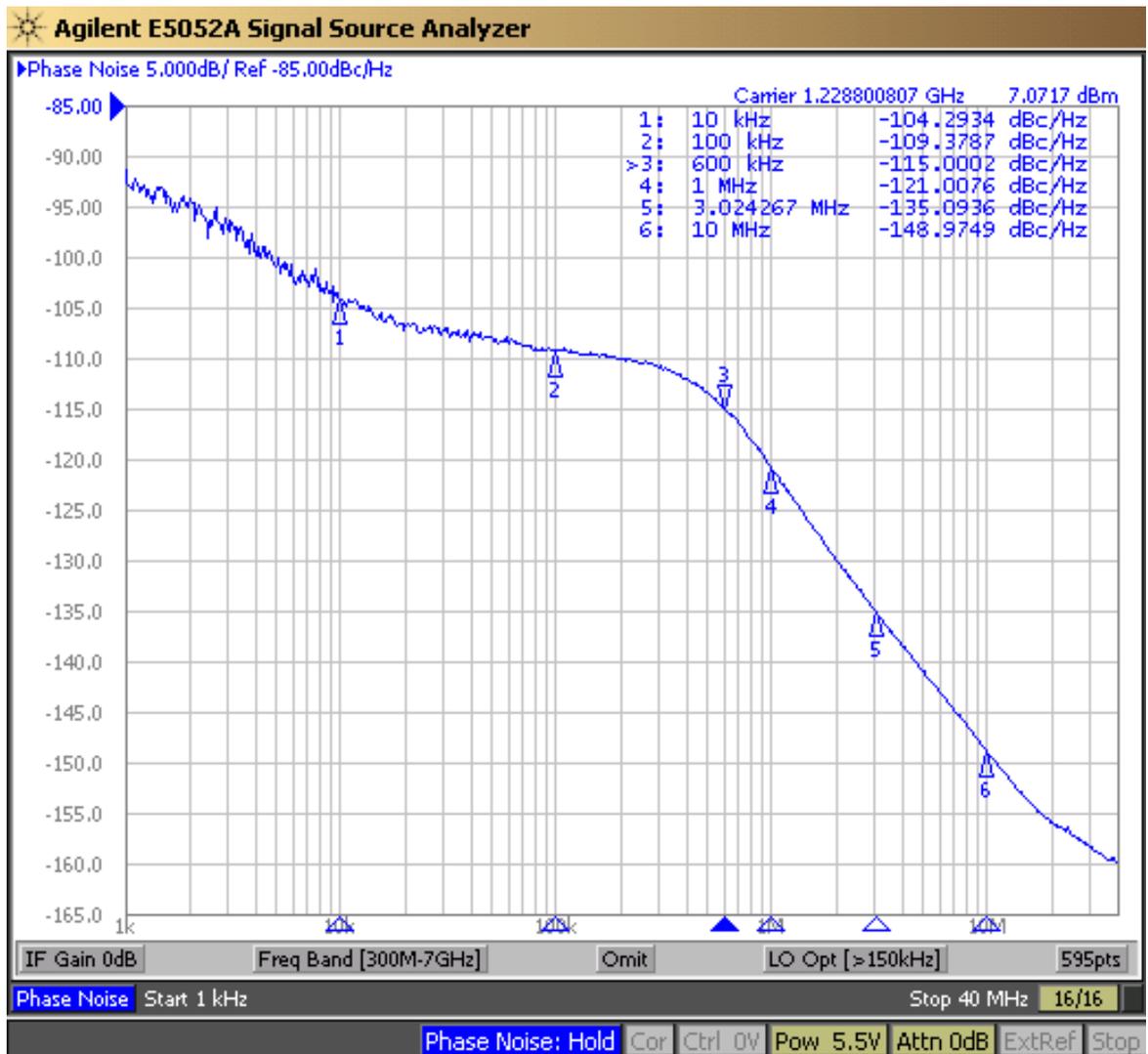


Figure 5.4 Measured divided-by-2 PLL output phase-noise

Figure 5.5 shows the divided-by-2 PLL output jitter, which was measured using an Agilent Infinium DSO81304A Oscilloscope. The measured RJ and DJ are 490 fs_{rms} and

9.04 ps, respectively, at a divided output frequency of 1.23 GHz. The measured DJ value is higher than expected. More measurements will be performed to verify this result. The jitter at the undivided output should ideally be the same or better.

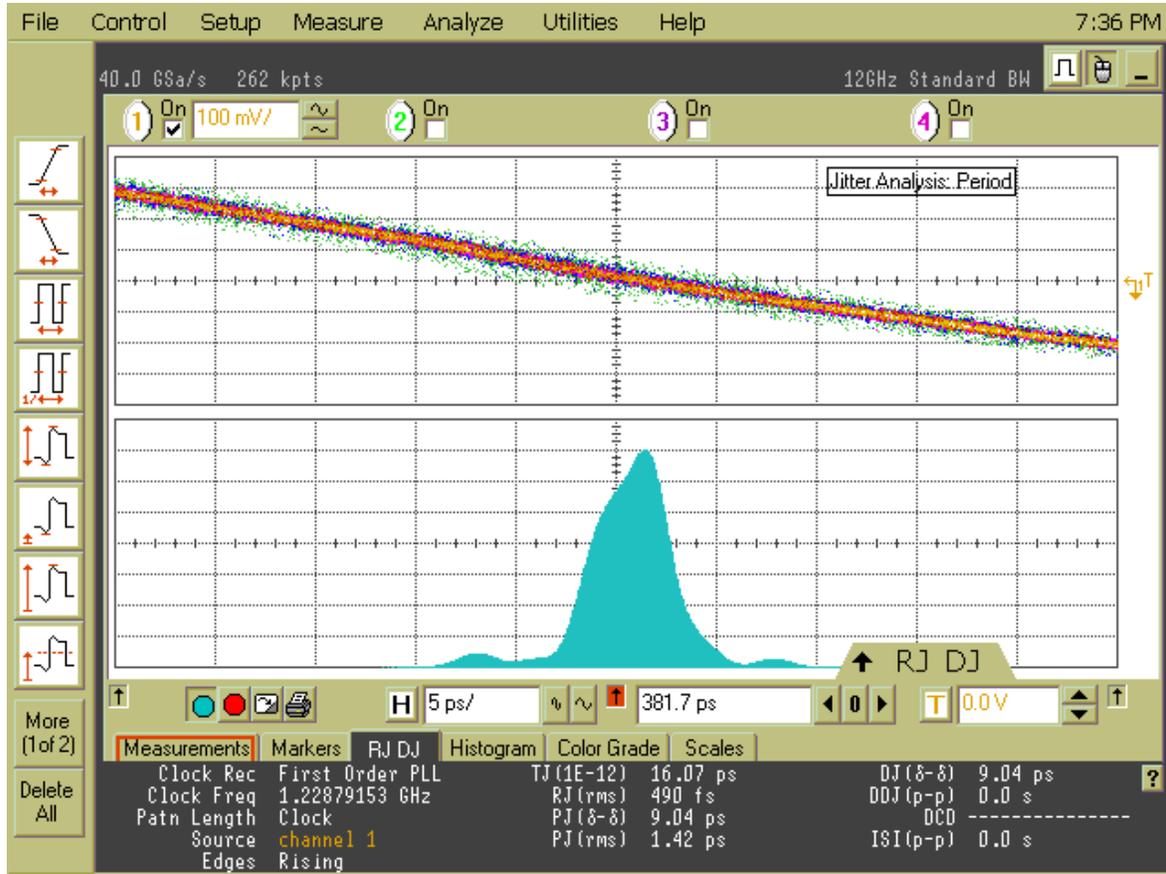


Figure 5.5 Measured divided-by-2 PLL output jitter

Figure 5.6 shows the measured phase-noise of the free running VCO. This measurement was performed by turning on the PLL without providing any reference signal, which would force the voltage at the VCO control line to be at its minimum (0 V). It is not possible to measure the VCO phase-noise at the exact desired frequency of 1.23 GHz since there is no access to the VCO control line. However by tuning the programmable capacitor bank we were able to PLL the phase-noise at a frequency (1.17 GHz) that is relatively close to the desired. Figure 5.6 shows that the free-running VCO phase-noise, measured at the divided output, at a 100 kHz offset is -103.4 dBc/Hz. This indicates that the undivided VCO phase-noise at the 100 kHz offset is -97.4 dBc/Hz.

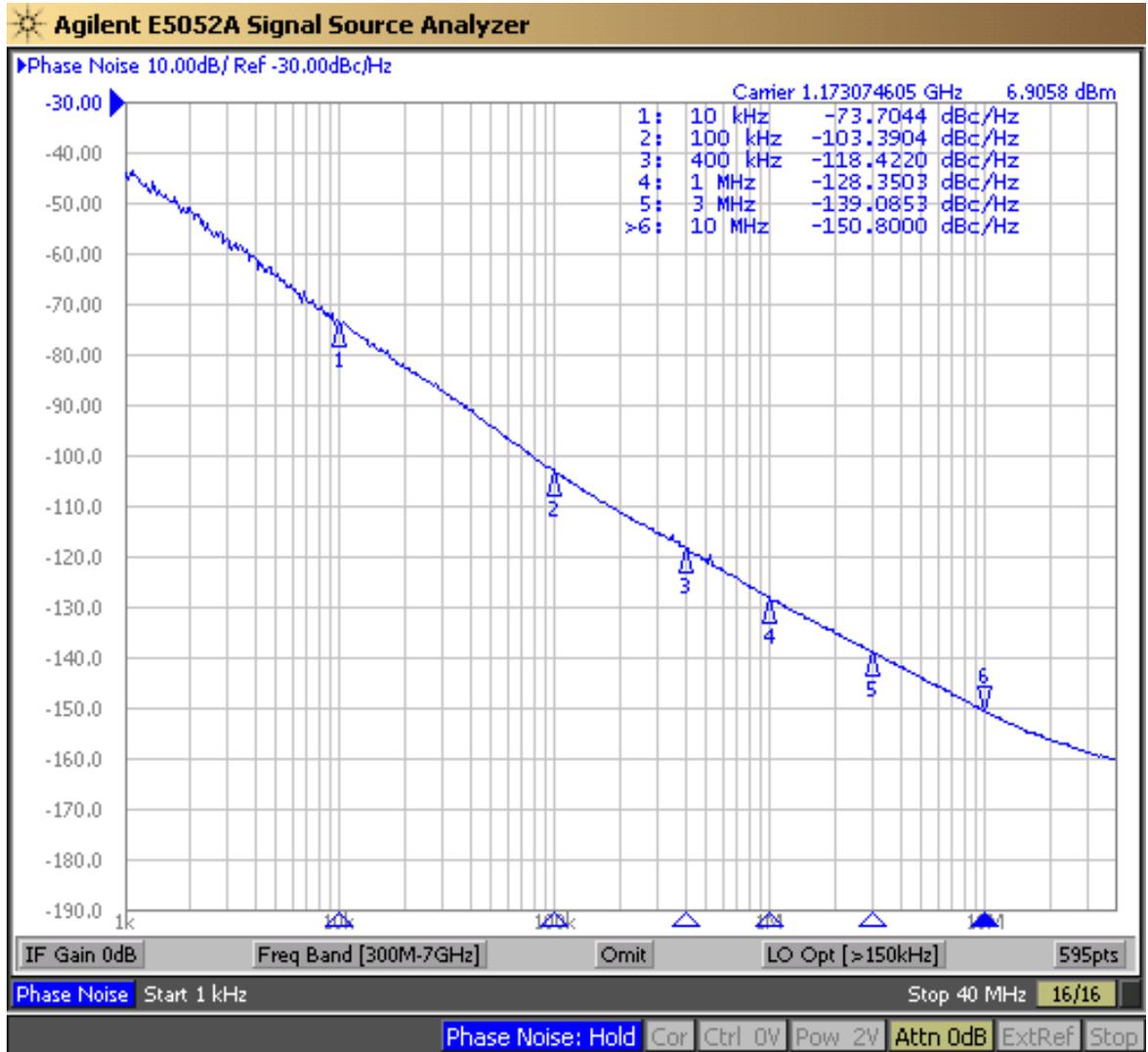


Figure 5.6 Measured divided-by-2 free running VCO phase-noise

Figure 5.7 combines the data that was shown in the previous two figures. Looking at Figure 5.7 we can clearly see the effectiveness of the PLL in attenuating the in-band VCO phase-noise.

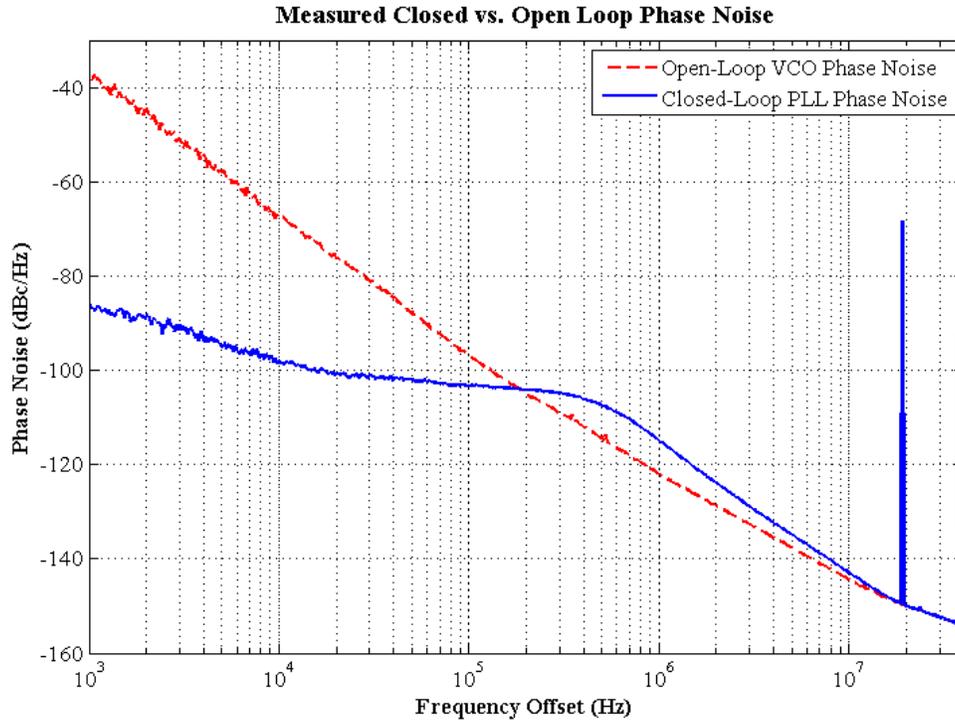


Figure 5.7 Measured free-running VCO phase-noise vs. locked PLL phase-noise (traces are scaled by +6 dB to compensate for the frequency division by 2)

5.2.3 Phase-Noise Measurements / Simulations Comparison

Figure 5.8 shows the simulated and the measured PLL phase-noise. The main differences that can be observed are the slightly smaller measured bandwidth, and the slightly higher in-band phase-noise. The measured PLL bandwidth is between 500 kHz to 600 kHz, compared about 660 kHz according to simulations. Furthermore, the measured in-band phase-noise at 100 kHz is -103.4 dBc/Hz, compared to -105.6 dBc/Hz, which indicates a very small difference of 2.2 dB.

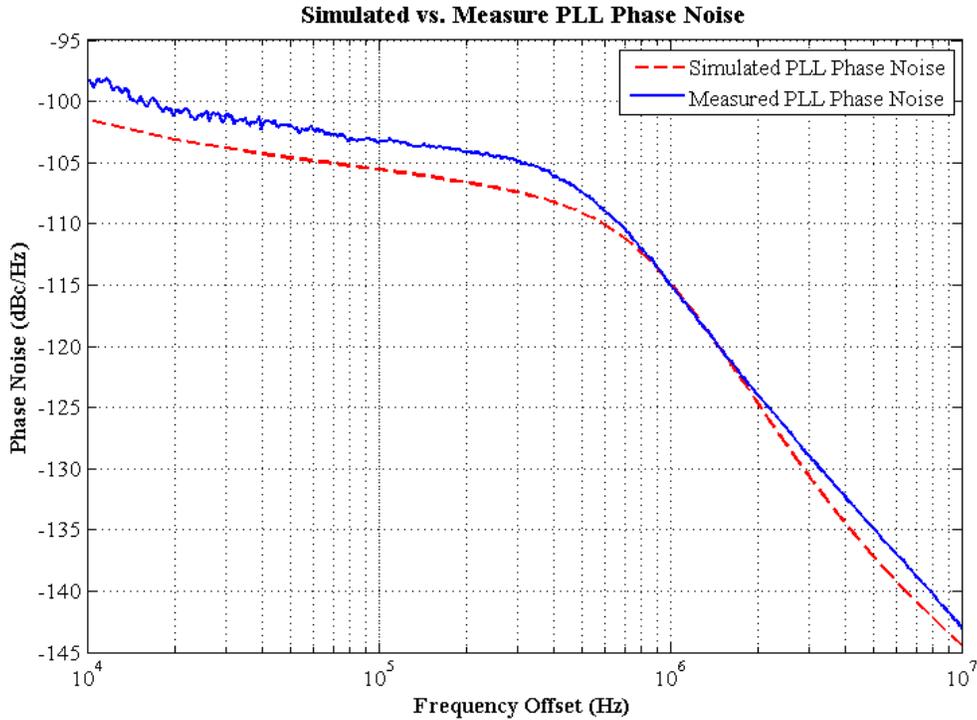


Figure 5.8 Measured vs. Simulated PLL phase-noise

5.3 Spectrum Measurements

Figure 5.9 shows the output spectrum of the PLL. The first harmonic of the reference spur is measured to be around -71 dBc, which in turn, implies that the undivided output reference spur is around -65 dBc. This low measured reference spur indicates the effectiveness of the S/H synchronous envelope detector circuit.

Figure 5.10 shows the measured spectrum of the divided-by-2 PLL output from 1 to 4 GHz. The large number of spurs has been correlated with simulations, and is caused by our design oversight of measuring the PLL output in a single-ended manner, rather than differentially. As per simulations, the real differential output of the VCO is much cleaner than the single-ended spectrum shown in Figure 5.10. This problem could have been avoided if a proper differential-to-single-ended buffer was used, however the short design time did not allow us to design this circuit. Unfortunately we are currently unable to generate precise PLL output bandwidth plots from simulation because of FFT (Fast-Fourier Transform) problems. We are currently looking into solving this problem.

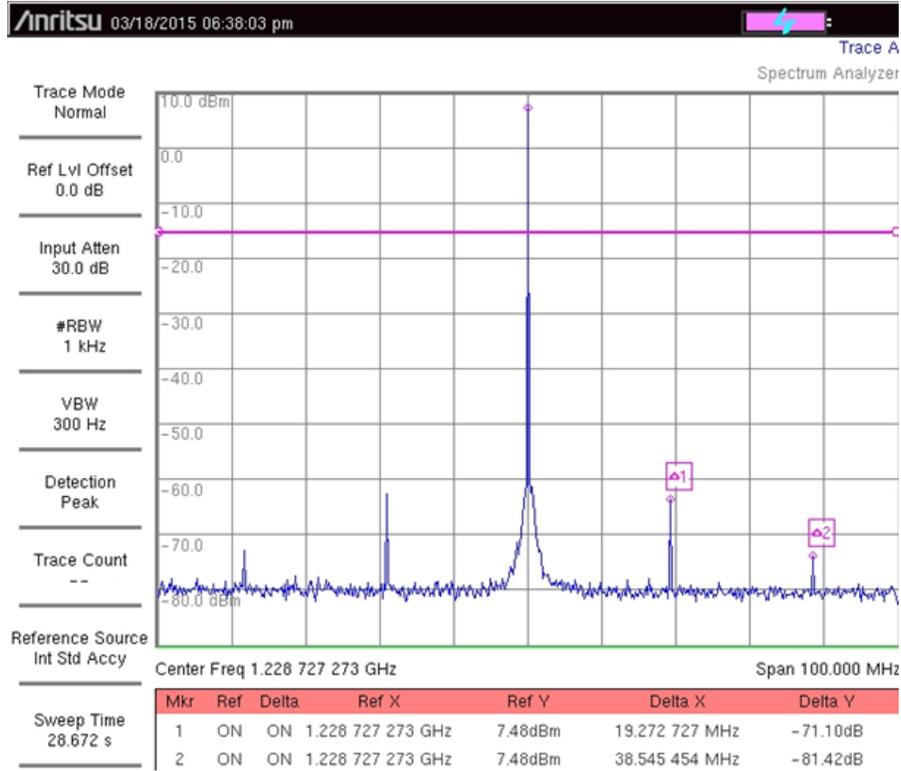


Figure 5.9 Measured Divided-by-2 output spectrum (100 MHz span)

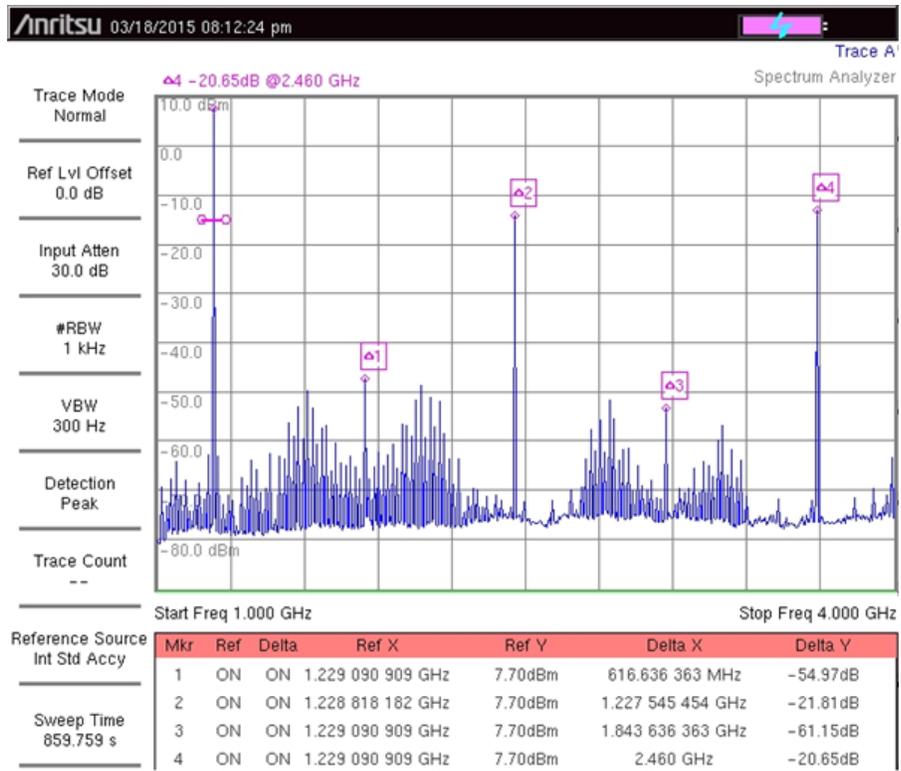


Figure 5.10 Measured divided-by-2 output spectrum (1 to 4 GHz)

5.4 Lock-Time Measurements

The frequency step response of the PLL is shown in Figure 5.11, generated by switching the reference frequency between 18.3 and 19.6 MHz (provided by external signal generators) using an off-chip multiplexer at a rate of 50 kHz (also provided by an external signal generator). Based on several other similar measurements, the output frequency settles in less than 2.5 μs for the worst case. The figure also confirms the effectiveness of the SPFD, since despite the large frequency step, no cycle slipping is observed.

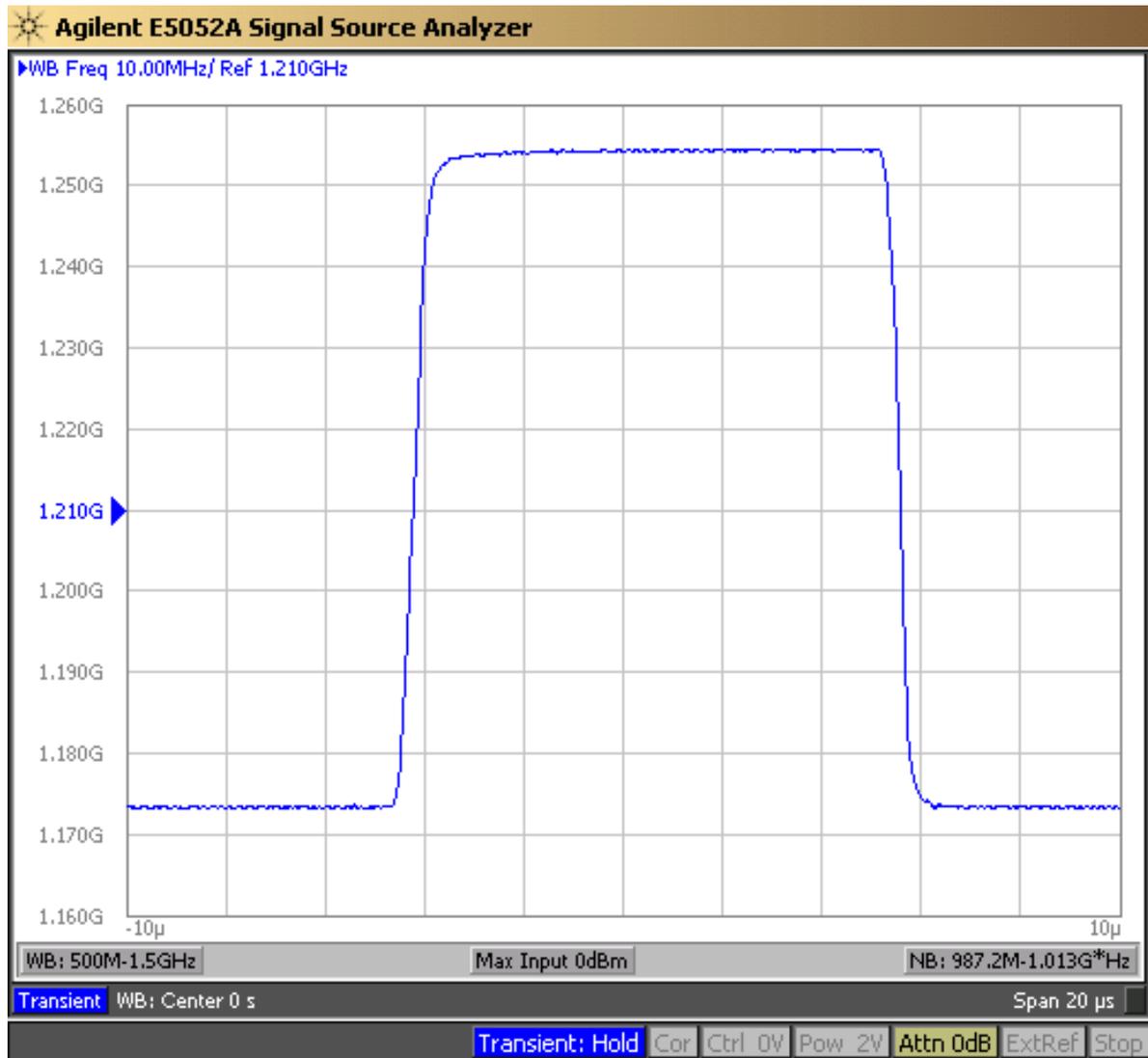


Figure 5.11 Measured frequency step response

5.5 Power Consumption

Figure 5.12 shows the power consumption breakdown of the proposed PLL based on simulations. The total simulated PLL power consumption is about 6.4 mW, compared to 6.8 mW of measured power consumption. The power breakdown is based on simulations rather than measurements because we do not have access to the power supply lines of the various PLL sub-blocks. The power breakdown shows that the VCO and the fast differential divider are consuming 83.5% of the overall system power.

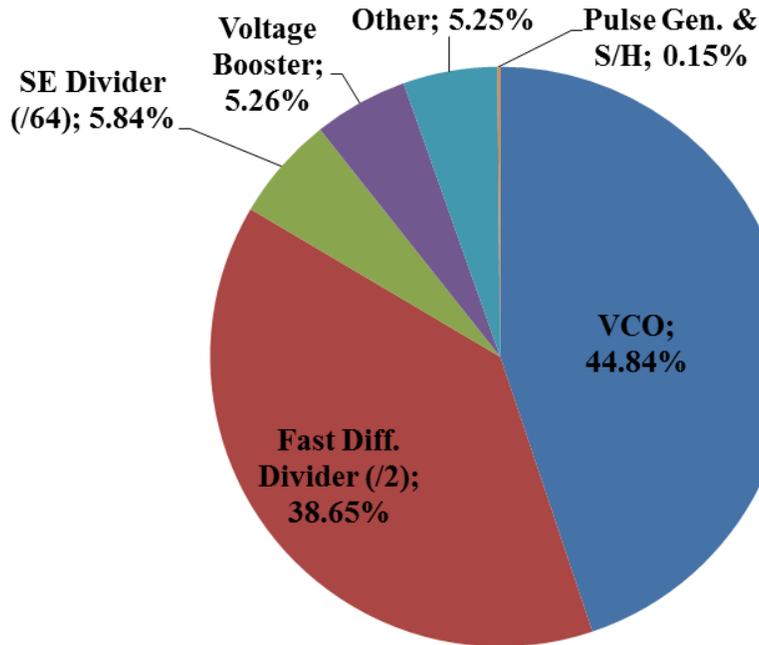


Figure 5.12 Power consumption breakdown (based on simulations)

5.6 Performance Summary and Comparison

Table 5.1 summarizes the measured performance of the proposed PLL and compares it with state-of-the-art Type-I and Type-II CP-based integer-N PLLs. We can see that the proposed PLL surpasses most of the compared works in area, power consumption and lock-time. Furthermore, the reference-spur and phase-noise performances are comparable to most of the other works.

	This Work	Sun 2012 [6]	Rao 2009 [20]	Gu 2006 [21]	Catli 2013 [22]	Chiu 2009 [23]	Bruss 2008 [24]	Wu 2007 [25]
CMOS Process (nm)	130	130	65	130	28	180	90	130
Supply Voltage (V)	1.2	1.2	1.0 / 1.8	1	1	1.8	1.2	1.5
Power (mW)	6.8	19.5	29	25	15.5	17.1	9.7	48
Tuning Range (GHz)	2.2 to 2.8	2.74 to 5.37	2.3 to 4.65	5.7 to 6.8	8 to 12.2	4.9 to 5.3	3.8 to 5.15	4.1 to 4.21
Reference Frequency (MHz)	19.2	21	156.25	62.5	156.25	4.7	1	16
Loop Bandwidth (kHz)	~700	~500	1,500 – 10,000	1,875	1,300 – 6,500	20	80	200
In-Band Phase-Noise (dBc/Hz)*	-103.4 @ 100 kHz	-92.4 @ 100 kHz	-115.7 @ 100 kHz	-102.7 @ 100 kHz	-116 @ 100 kHz	-97.3 @ 100 kHz	-86.4 @ 100 kHz	-79 @ 100 kHz
Out-of-Band Phase-Noise (dBc/Hz)*	-129 @ 3 MHz	-122.8 @ 3 MHz	-	-137.4 @ 3 MHz	-119 @ 10 MHz	-124 @ 1 MHz	-132 @ 3 MHz	-124 @ 3 MHz
Random Jitter (fs_{rms})	490 @ 1.23 GHz	-	460 @ 5 GHz	500	198	-	-	-
Reference Spur (dBc)*†	-65	-60.7	-39	-104.7	-49.3	-89.6	-102	-
Lock Time (μs)**	<2.5	-	32 to 58	-	-	10	60	50
Area (mm²)	0.12	1.5	0.35	0.43	0.093	1.61	0.23	1.5

* Output normalized to 2.4 GHz

† Reference normalized to 19.2 MHz

Table 5.1 Performance summary and comparison

Chapter 6: Conclusion and Future Work

While traditional analog Type-II PLLs and all-digital PLLs have their own merits in terms of performance, this work demonstrates a simple-to-design, digital-friendly Type-I PLL. This PLL attains excellent performance in die area, power consumption, loop stability, lock-time, lock-range and phase-noise, with a low reference spur. Several techniques have been leveraged to improve the performance of the Type-I PLL without introducing significant design complexity or analog-intensive blocks such as opamps, amplifiers, bias-generation circuits, charge-pumps, auxiliary loops, auxiliary paths and zero-stabilization in LF. These techniques include voltage-mode Type-I operation, increasing forward path gain using a simple voltage booster and a level shifter, a S/H circuit that serves as a synchronous envelope detector, and saturated PFD for fast loop acquisition and enhanced lock-range.

The proof-of-concept PLL was designed and fabricated in a 0.13- μm CMOS process. The PLL occupied a small die area of 0.12 mm². Post-silicon performance measurements such as phase-noise, bandwidth, lock-range and power consumption show good agreement with the performance predicted by circuit level simulations and theoretical analysis.

Both phase-noise measurements and simulations indicate that the in-band phase noise values reported in this thesis are dominated by the phase-noise of the reference oscillator. This means that a significant improvement of up to 11 dB may be achieved if a higher quality reference oscillator with lower phase-noise is used. This motivates the next step of this research to measure the true in-band phase-noise of the PLL by using a reference oscillator with at least 15 dB lower phase-noise. In addition, since the power consumption of the PLL was dominated by the VCO and the divider, exploring ideas that reduce the VCO and divider power, or even eliminate the need for a divider would be very interesting.

Lastly, we are interested in investigating the feasibility of implementing a Type-I sub-sampling PLL. A Type-II sub-sampling PLL architecture was recently presented in [26], and it showed superior phase-noise performance compared to the PFD/CP-based Type-II PLL. The performance published in [26] is not included in the comparison table because the sub-sampling PLL is not in the same category as PFD/CP-based PLLs.

In summary, this research showed that despite the inherent limitations of Type-I PLLs, proper design techniques and innovations can result in performances that are very comparable with state-of-the-art Type-II PLLs without the need for the large area and design complexity that Type-II typically require.

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