IMPLEMENTING DIGITAL CONTROL TO IMPROVE CONTROL BANDWIDTH AND DISTURBANCE REJECTION ON A LLC RESONANT DC-DC POWER CONVERTER

by

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Abstract

In this thesis, the implementation of an adaptive digital control scheme and the development process to implement it for an existing analog controlled LLC resonant converter is presented. The goal is to improve the dynamic performance (aka control bandwidth) and the disturbance rejection ability of the closed loop system using digital control. A brief analysis of the experimented on LLC resonant converter and simulations of its control-to-output frequency response characteristics under different operating conditions are initially performed in order to show its non-linear behavior. Then the design process and requirements for both the digital and analog components to make the existing LLC converter compatible with a digital signal microcontroller is presented in detail. The digital signal microcontroller (DSC), ADC, DPWM, sampling period, interrupt service routine (ISR), and the 2P2Z digital compensator implementation will be overviewed. Analog components such as the voltage/current sensors, the VCO, and other analog interfacing components will also be presented. After that, the complete design process to achieve optimized digital compensators for several different operating points is presented. This design process introduces the method of using either the uncompensated loop-gain frequency response data collected empirically from the physical converter or from a PSIM simulation and then using MATLAB's System Identification software toolbox to generate an estimated mathematical model based on frequency response data. A digital compensator is then designed based on the estimated mathematical model. A comparison between the PSIM simulation and the empirical data of the LLC converter's plant frequency response for several different operating conditions is also presented. A digital adaptive compensator algorithm is implemented so that the most optimized compensator design for a given converter operating range is selected. The algorithm uses the output voltage and current to determine the operating point of the converter, which then access a software look-up-table (LUT) for the optimized compensator. A complete prototype is built to experimentally validate the digital design process and the performance results of a classical single compensator design is compared with the adaptive compensator design in order to show the benefits of the adaptive compensator control scheme.

Preface

The experiments presented in this thesis were performed on a commercially available power converter provided by Delta-Q Technologies. Furthermore, some of the analog components presented in this thesis were part of the original LLC converter design such as the VCO and gain inverter op-amp circuit. Some components were also modified from their original design to better fit the digital design needs such as the sensors. All the prototyping work done was at Delta-Q technologies laboratories. My contributions include implementing digital control on the pre-existing LLC resonant power converter (model: IC650), which involved collecting data necessary to model the converter, using MATLAB to produce estimated models, and programming the digital signal microcontroller to implement the adaptive control algorithm.

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List of Symbols

a_n	n_{th} numerator coefficient of 2P2Z transfer function
b_n	n_{th} denominator coefficient of 2P2Z transfer function
C_r	Resonant Tank Capacitor
C_s	Series Resonant Tank Capacitor
C_{sr}	Series Resonant Tank Capacitor for the Series Resonant Parallel Converter
C_{pr}	Parallel Resonant Tank Capacitor for the Series Resonant Parallel Converter
f_c	Cross-over Frequency
f_o	Resonant Frequency
f_{sw}	Switching Frequency
G_o	Controller Gain
g_m	Gain Margin
L_m	Magnetizing Inductor
L_r	Resonant Inductor
n	Transformer Ratio
Q	Quality Factor
T_s	Sampling Period
V_c	Control Voltage
V_{sq}	Square Wave Voltage
θ_m	Phase Margin

List of Abbreviations

2P2Z	Two Pole Two Zero
AC	Alternating Current
ADC	Analog-to-Digital Converter
CLA	Control Law Accelerator
CPU	Central Processing Unit
DC	Direct Current
DPWM	Digital Pulse-Width Modulation
DSC	Digital Signal Controller
DSP	Digital Signal Processing
FLC	Fuzzy Logic Control
FRA	Frequency Response Analyzer
GUI	Graphic User Interface
HRPWM	High Resolution Pulse Width Modulator
IIR	Infinite Impulse Response
ISR	Interrupt Service Routine
LPF	Low-pass Filter
LSB	Least Significant Bit
MAC	Multiply and Accumulate
MEP	Micro Edge Positioner
MSPS	Million Samples per Second
OCP	Overcurrent Protection
OE	Output-Error
OVP	Overvoltage Protection
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PRC	Parallel Resonant Converter
PWM	Pulse-Width Modulation
RC	Resistor Capacitor
SISO	Single Input Single Output
SMPS	Switch Mode Power Supply

SOC   Start of Conversion

SPRC   Series Parallel Resonant Converter

SRC   Series Resonant Converter

VCO   Voltage Controlled Oscillator

ZVS   Zero Voltage Switching

List of Units and Prefixes

A	Amperes
dB	Decibels
Hz	Hertz
s	Seconds
V	Volt
W	Watt
Ω	Ohm
°	Degree
p	Pico (10^{-12})
n	Nano (10^{-9})
μ	Micro (10^{-6})
m	Mili (10^{-3})
k	Kilo (10^{3})
M	Mega (10^{6})

Acknowledgements

Dedication

Dedicated to my parents.

1   Introduction

1.1   Overview

Switch-mode power supplies (SMPS) drive many of today's industrial applications because of their superior performance, efficiency, size, and cost [1], [2], [3]. The increased demand to provide tightly regulated voltage and current to the load has sparked interest in more advanced control algorithms for SMPS. Many applications demand strict regulation of output voltage or current while maintaining good dynamic performance during transients, which means voltage or current deviation should be small and settle to the reference value quickly [1], [4]. This requires a well-designed closed loop controller to give the system a high feedback loop bandwidth. However, achieving a high feedback loop bandwidth with analog components is challenging because converter characteristics change with varying operating conditions such as load, input voltage, and component variations [5]. This thesis presents the design process and implementation of digital control on a DC-DC LLC resonant converter in order to improve overall dynamic performance and disturbance rejection. In addition, although not the main focus of this thesis, it is still important to describe the LLC converter characteristics which will be presented in Chapter 2.

1.2   Digital Control

Digital control of power converters offers many advantages over their analog counterparts. Digital control is more flexible, reliable, provides better integration, cost-effective, and less susceptible to noise [6], [7]. The following is a more detailed list of the advantages associated with digital control over analog control for power converter applications [1]:

- The ability to implement sophisticated algorithms for increasing efficiency and dynamic performance of power converters.
- The flexibility of reconfiguring control parameters without the need for changes in hardware.
- Less susceptible to controller component variation and noise sensitivity.
- Integration of multiple functionalities on one microcontroller helps reduce cost.

Because of these benefits, digital control is becoming more popular in high frequency DC-DC converters. The transition from analog control to widespread digital control has been slow

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because operating at high frequencies requires high performance processors, analog-to-digital converters (ADCs), and digital pulse-width modulators (DPWMs), all of which comes at a price. However, recent technological advances are making low cost high performance digital signal controllers (DSC) possible (a DSC is a microcontroller specially designed to provide fast signal processing abilities) [8]. There are also challenges to keep in mind when implementing digital control. Limited resolution of the ADC and DPWM leads to quantization errors, high frequency operations can result in low resolution DPWM that may lead to limit cycle oscillations, and a slow processor clock speed limits the control bandwidth of the system [8], [9].
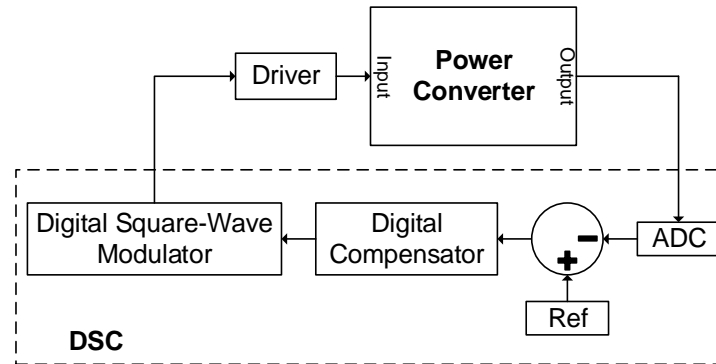
Figure 1.1 - Simplified block diagram of power converter with digital signal controller

Figure 1.1 shows a simplified block diagram of a power converter being controlled by a DSC and some inner components of the DSC. The power converter output signal is fed into the ADC, which digitizes the signal. The digital signal is subtracted from the reference signal and the error is fed into the digital compensator for computation. The calculated value of the digital compensator is normalized and is fed into the digital square wave modulator, which can vary duty cycle or frequency.

In [6], the author presents a method for digital voltage mode control on a nonresonant-coupled parallel resonant converter. It was found that the nonresonant-coupled parallel resonant converter's control-to-out frequency response shape did not change much under different operating conditions. It was found that only the magnitude (or gain) of the frequency response changed. As a result, a gain-scheduled digital controller was proposed which adaptively varies the gain of the digital compensator in order to compensate for the changing frequency response of the converter under different operating conditions. The author used Saber simulation software to simulate the gain at the 10kHz point over the entire converter operating range and constructed a look-up-table of 32x32 gain value points for the different operating points. It was shown that

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the gain-scheduled digital control method increased bandwidth performance by four times over a classical analog control approach while not compromising stability margins. The digital implementation however did result in higher sub-harmonic noise in the converter's output compared with the analog implementation. The author claims such noise can be improved upon with a higher resolution digital PWM output. There is however, an issue with this control technique for LLC resonant converters. The non-resonant parallel converter can only operate above resonant frequency in order to achieve zero-voltage switching (ZVS). As a result, its frequency response characteristics do not have the double pole effect experience by LLC converters operating close to or below resonant frequency. That is to say, the LLC frequency response shape varies much more under different operating conditions. Therefore, simply changing the gain may not enough to ensure best performance.

In [10], the author presents a digital control scheme for charging a capacitor using a high voltage output LCC resonant converter. The control scheme uses current control mode (for constant current charging) and voltage control mode (for constant voltage charging). A large signal state-space model of 18 operating points throughout the charging cycle was developed using a generalized averaging modeling method with MATLAB. The author implemented a gain-scheduled PI controller for each operating point where the output current was used as the gain-scheduling variable for determining the correct gain value. It was found that the transition from current control mode to voltage control mode during the charging cycle produces a large step change because the difference between the output voltage and reference voltage was large. As a result, the control loop will introduced to a large step change, which would introduce a large voltage overshoot. The author's solution to this issue is to add an adaptive first order low-pass voltage reference filter in order to ensure no overshoot during the transition. The adaptive filter adapts the voltage level of the current to voltage mode transition and adapts the filter corner frequency to the rate of the voltage rise measured for a given load with a constant current. A disadvantage in adding this extra filter is the sacrifice in rise time (or bandwidth) of the control system.

In [11], the authors implements and compares a digital PID and fuzzy logic controller (FLC) on a half-bridge DC/DC LLC resonant converter. The inputs to the FLC are the *error*, the *difference of error*, and the *sum of error* and they are divided into nine triangular membership functions with a total of 81 rules. Each rule consists of a weighting factor and the degree of

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change of switching frequency. The authors' simulation and experimental results indicated that the fuzzy logic controller was able to achieve faster dynamic response in comparison with the PID controller. A load variation experiment showed that the output voltage responded to a step change in load in about 15ms for the PID controller whereas the fuzzy logic controller responded to the same step change in about 5ms.

In [12], the author presents an adaptive digital PID control scheme in order to improve the dynamic performance of power converters. The main idea is to have a slower but more stable PID controller for steady-state operations and a faster PID controller during the transients. The Kp and Ki constants in the PID controller are increased during the transient in order to achieve a higher temporary bandwidth which corresponds to improved dynamic performance. The adaptive controller observes the error caused by the difference between the output voltage and reference voltage. Once the error is outside a pre-defined threshold, the Ki and Kp values are increased abruptly to a large value in order to increase the bandwidth and speed of the closed loop system. The controller then monitors when the error signal starts to reach steady state and then gradually reduce the Ki and Kp values to their original steady-state values. The author built a proof of concept experimental prototype of the digital adaptive control scheme on a single-phase DC-DC buck converter. Experimental results showed a 26% reduction in voltage overshoot and a >50% reduction in settling time for a particular case of a step load change compared to a conventional PID.

1.3 Motivation and Objective

Advantages such as higher efficiency, greater power density, lower component stress, and higher switching frequency make DC-DC resonant converters topologies more attractive over their traditional PWM counterparts [6], [13]. However, the main disadvantage of resonant converters is that they require complex control because of their sensitivity to operating conditions and parameter tolerances. Because of the complex control nature of resonant converters, they stand the most to benefit from digital control [5].

In traditional analog design, a controller is designed for a particular power operating point. The controller is designed with a reduced bandwidth so that stable operation under varying conditions and parameters can be maintained. Such design often greatly limits the dynamic performance and disturbance rejection of the system. Attempting to increase the gain and

bandwidth of the system further may cause instability during both steady state and dynamic operations [1].

The main objective of this thesis is to improve the dynamic performance and the AC line ripple rejection ability on a commercially available analog controlled DC-DC LLC resonant converter by implementing digital control. In order to design a compensator, a mathematical model of the power converter is needed. Because of the non-linear nature of resonant converters, it is difficult to model them with traditional mathematical modelling methods and those methods are either over simplified (such as the using the first harmonic approximation), not very accurate, or overly complex and difficult to use. As a result, this thesis also presents an approach to accurately model a resonant power converter while simplifying and speeding up the modelling process, which would avoid the inaccurate/complex traditional mathematical modelling methods. As will be discussed later, this approach involves empirically gathering the frequency response data from the physical converter. With the frequency response data, a mathematical transfer function is estimated using a software tool and then the compensator is designed.

1.4 Outline

This thesis is organized into seven chapters. In Chapter 1, the importance and advantages of digital control is introduced and the motivation to implement digital control on a resonant converter is established. Some previous digital control work done on power converters are also presented along with a summary of their advantages and disadvantages.

Chapter 2 provides a brief literature review of some basic resonant converter topologies. The LLC resonant converter experimented on in this thesis is presented in more detail along with its specifications. In addition, a simulation of the LLC converter's control-to-output frequency response for several different operating conditions is shown to emphasize its dynamic differences.

In Chapter 3, a detailed overview of the design infrastructure and analysis of the components used to implement digital control on the LLC resonant converter is presented. Digital design considerations such as the digital signal microcontroller (DSC), analog-to-digital converter (ADC), digital PWM (DPWM), sampling rate, and more are covered. In addition, the analog components needed to integrate the DSC with the LLC converter are presented.

In Chapter 4, the complete design process to achieve optimized digital compensators for varying operating points of the LLC converter is presented. The process involves introducing an approach of modelling the LLC resonant converter by gathering its uncompensated loop-gain frequency response data for various operating points and then using MATLAB to estimate mathematical models based on gathered data. With the estimated models, optimized digital compensators are designed. A comparison between the simulated PSIM control-to-output frequency response and the physically measured data is also presented and analyzed. An overview of the hardware and software tools used in the digital compensator design process will also be shown. Finally, a summary of the performance result of a single compensation design vs an adaptive compensation design is shown. (The performance is evaluated by the system's stability margins, bandwidth, and 120Hz disturbance rejection ability.)

Chapter 5 provides an overview of the digital control software architecture. Details on the adaptive compensation algorithm, which includes the responsibilities of the background loop and interrupts service routine task are covered.

Chapter 6 presents the experimental results to validate the work done in this thesis. First, an overview of the experimental prototype lab bench setup is shown. The modifications performed on the closed loop digital controlled system done to obtain the experimental loop-gain frequency response is measurements are presented. Next, the experimental data and performance results of the digitally compensated loop gain will be presented. Finally, comparisons between the experimental data and simulation will be shown.

Chapter 7 summarizes the work done in this thesis and provides further discussion insight regarding the overall work. Future work and possible improvements are also discussed.

2 Literature Review

This chapter provides a review of the fundamental operation and characteristics of some common resonant converter topologies as well as highlighting their limitations. More emphasis will be placed on the LLC resonant converter topology and the specification for the LLC converter experimented on in this thesis is presented. Furthermore, the LLC converter's control-to-output (plant) frequency response for several different operating conditions is shown.

2.1 Resonant Converters

A resonant converter contains a resonant tank that consists of L-C type networks. The resonant tank is driven by a periodic (voltage or current) square wave which results in the voltage and current of the resonant tank varying sinusoidally [14]. Frequency modulation is used to control the resonant type converter. Varying the switching frequency changes the impedance of the resonant tank, which results in the regulation of the voltages and currents [15]. There are three main well-known topologies for resonant converters: the series resonant converter SRC, the parallel resonant converter PRC, and the series-parallel resonant converter SPRC. The following is a brief overview of these topologies along with their advantages and disadvantages.

The series resonant converter (SRC) shown in Figure 2.1 [16] has a resonant tank consisting of an inductor Lr and a capacitor Cr in series.
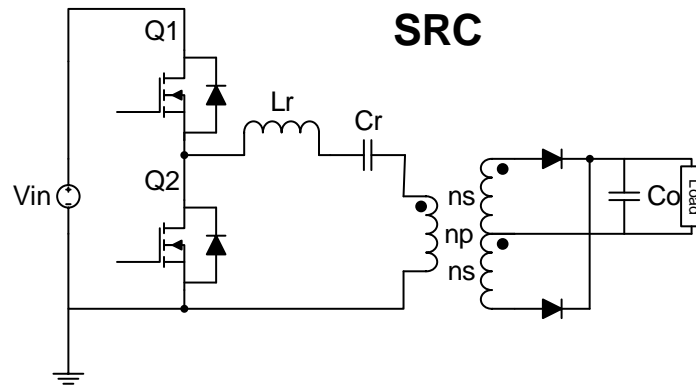
Figure 2.1 - Series Resonant Converter (SRC)

As discussed in [16], the SRC acts like a voltage divider by having its resonant tank in series with the load. By changing the impedance of the resonant tank, the voltage divider equation will change therefore changing the gain of the converter. Because the load is in series with the resonant tank, the circulating energy in the tank is small which means less conduction losses. The DC gain of the SRC is always lower than one. A gain of one is achieved at resonant

frequency where the impedance of the series resonant tank is small and all the input voltage drops on the load. The SRC is non-ideal for practical DC-DC converter applications because it requires a high range of switching frequencies for light load regulation. It also has high circulating energy that results in conduction losses and the switches experience high turn off current.
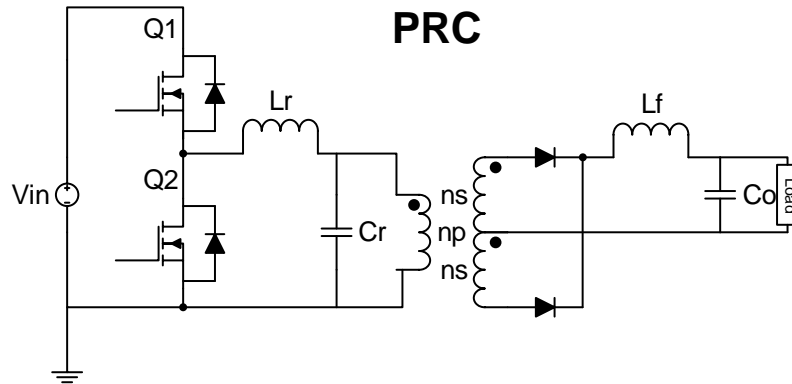
Figure 2.2 - Parallel Resonant Converter (PRC)

The parallel resonant converter (PRC) is shown in Figure 2.2 [16]. It is essentially a series resonant converter expect for the fact the load is in parallel with the resonant capacitor. The converter's operating region is much smaller compared to the SRC and can have a DC gain greater than one. The main problem of the PRC is its high circulating current even at no load conditions because the load is in parallel with the resonant capacitor. Therefore, the PRC experiences even higher conduction losses. The PRC also suffers from high turn off current just like the SRC [16].
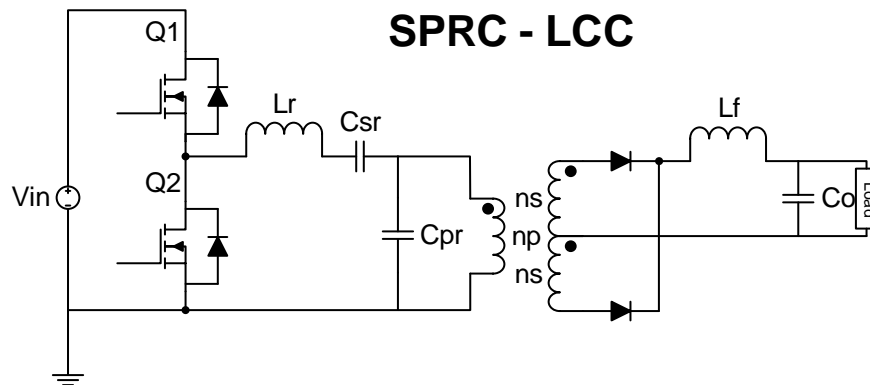
Figure 2.3 - Series Parallel Resonant Converter (SPRC) LCC

A LCC type series parallel resonant converter SPRC shown in Figure 2.3 [16] can been viewed as a combination of the SRC and the PRC. The resonant tank consists of three resonant components: Lr, Csr, and Cpr. The LCC combines the good characteristics of the SRC and the

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PRC by having less circulating current and smaller sensitivity to load change. However, it still suffers with wide input ranges, which leads to high conduction and switching losses under high input voltages [16].

2.2 LLC Resonant Converter

In this section, the LLC converter is presented in more detail and its advantages over the series resonant converter (SRC), parallel resonant converter (PRC), and the LCC series parallel resonant converter (SPRC) is presented.
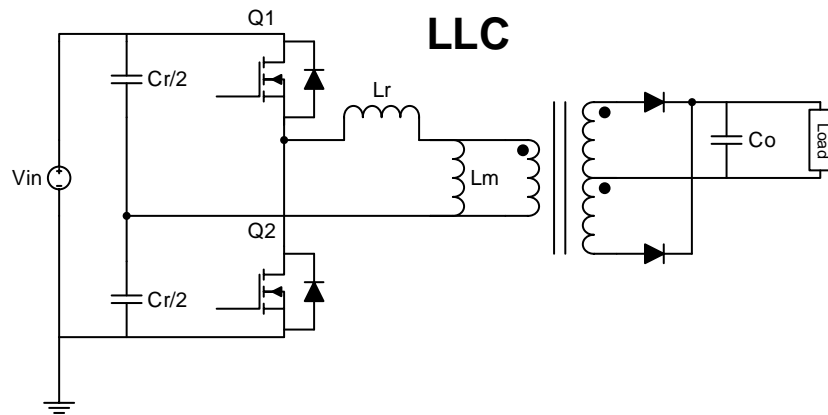
Figure 2.4 - LLC Resonant Converter

The LLC resonant converter shown in Figure 2.4 [17] is essentially the dual of the LCC resonant converter. Its resonant tank is composed of two inductors (Lr and Lm) and one capacitor (Cr). The major advantage of the LLC resonant converter is it allows for zero-voltage switching (ZVS) operation for a variety of loads. It can also operate with a narrow switching frequency range [17]. Another advantage of LLC compared to the LCC topology is the two inductors Lr and Lm of the LLC can be combined into one physical component therefore saving cost whereas the LCC converter requires two large high cost capacitors [18].

The LLC resonant converter can be broken down into four sections: the bridge inverter, the LLC resonant tank, the high frequency transformer, and the rectifier [19].
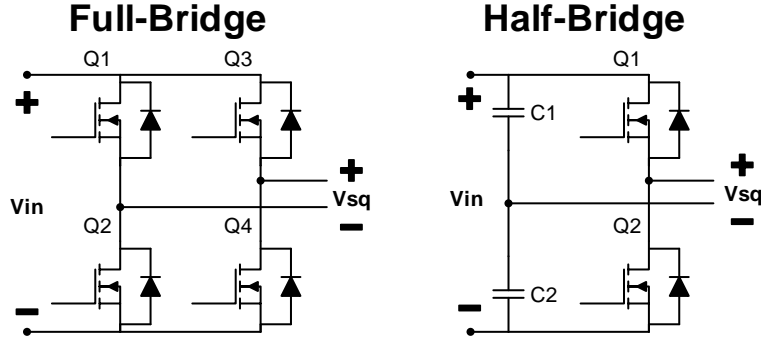
Figure 2.5 - Full-Bridge & Half-Bridge switching circuits

A full-bridge and half-bridge inverter is shown in Figure 2.5 (the half-bridge inverter is used for this thesis). It is the first stage of the LLC converter, which converts a DC input voltage into a square wave of switching frequency (f_{sw}). The duty cycle of the square wave is typically 50% with a small dead time to help with zero voltage switching (ZVS). The mathematical equation of the square wave V_{sq} generated by the half-bridge inverter is shown in Equation 2-1 [15] where d represents the duty cycle.

$$V_{sq} \approx \frac{4}{\pi} \frac{V_{in}}{2} \sin(\pi \frac{d}{2}) \sin(\omega t) \qquad \text{Equation 2-1}$$

Ultimately, the main advantage of a half bridge is its reduced cost (because of fewer switches) with the sacrifice of increased power loss because of the increased RMS current going through the switches (which causes increased losses) [19]. The half-bridge is usually used for lower power levels (<1000W) where the power loss is deemed acceptable compared to the decrease in cost [16].
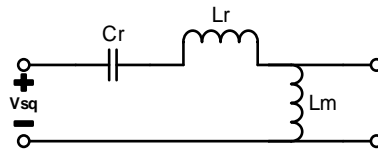
Figure 2.6 - LLC Resonant Tank

The square wave generated by the half-bridge inverter is fed into the resonant tank as shown in Figure 2.6. The LLC tank consists of a series resonant inductor Lr, a series resonant capacitor Cr, and a parallel resonant inductor Lm. It is shown in [20] that the impedance of the resonant tank can be varied by changing the frequency of the square wave fed into it.

The high frequency transformer shown in Figure 2.4 is used to decrease/increase the secondary side voltage and provide galvanic isolation to the input for safety. Using integrated

magnetic technology for the transformer allows the Lr and Lm inductors to be a part of the same magnetic structure, which is useful in terms of increasing the converter's power density [18], [21].

Full-Bridge Rectifier　　　　　**Full-Wave Rectifier**
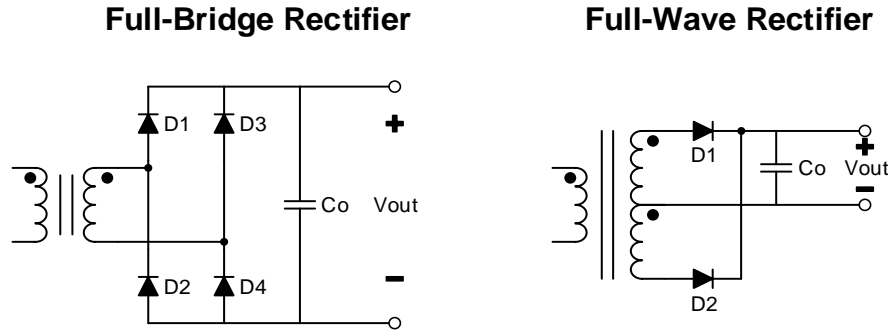
Figure 2.7 - Full-Bridge (left) and Half-Bridge (right) rectifier

The last stage of the LLC resonant converter is the bridge rectifier with a capacitor output filter Co as shown in Figure 2.7 [19]. Figure 2.7 shows both a full-bridge and a full-wave rectifier. The function of this section is to transform the scaled AC voltage output from the transformer to a DC output.

Full-Wave compared to Full-Bridge Rectifier						
Diode Voltage Rating	# of Diodes	Diode Conduction Losses	# of Secondary Windings	R_{sec} per winding	I_{RMS} per winding	Transformer Secondary loss
×2	÷2	÷2	×2	×2	$\times\sqrt{0.5}$	×2

Table 2.1 - Full-Wave rectifier compared to Full-Bridge rectifier

As summarized in Table 2.1 [19], the diodes of the full-wave rectifier experience twice the voltage compared to the full-bridge rectifier. However, the full-wave rectifier only has two diodes while the full-bridge rectifier has four diodes resulting in the full-wave rectifier having half the total diode conduction losses. The full-wave has two secondary windings therefore the resistance is doubled for the same winding area. Each winding in the full-wave rectifier caries a RMS current that is $\sqrt{0.5}$ times the RMS current of the full-bridge rectifier. In all, the total secondary winding copper losses of the full-wave rectifier is two times more compared to the full bridge rectifier. The full-bridge rectifier's advantage of experiencing only half the amount of voltage when compared with the full-wave rectifier makes it a good candidate for high output voltage applications. The full-wave rectifier is best used for low output voltages and high

currents applications because of its lower conduction losses (the full-wave rectifier is used in this thesis).
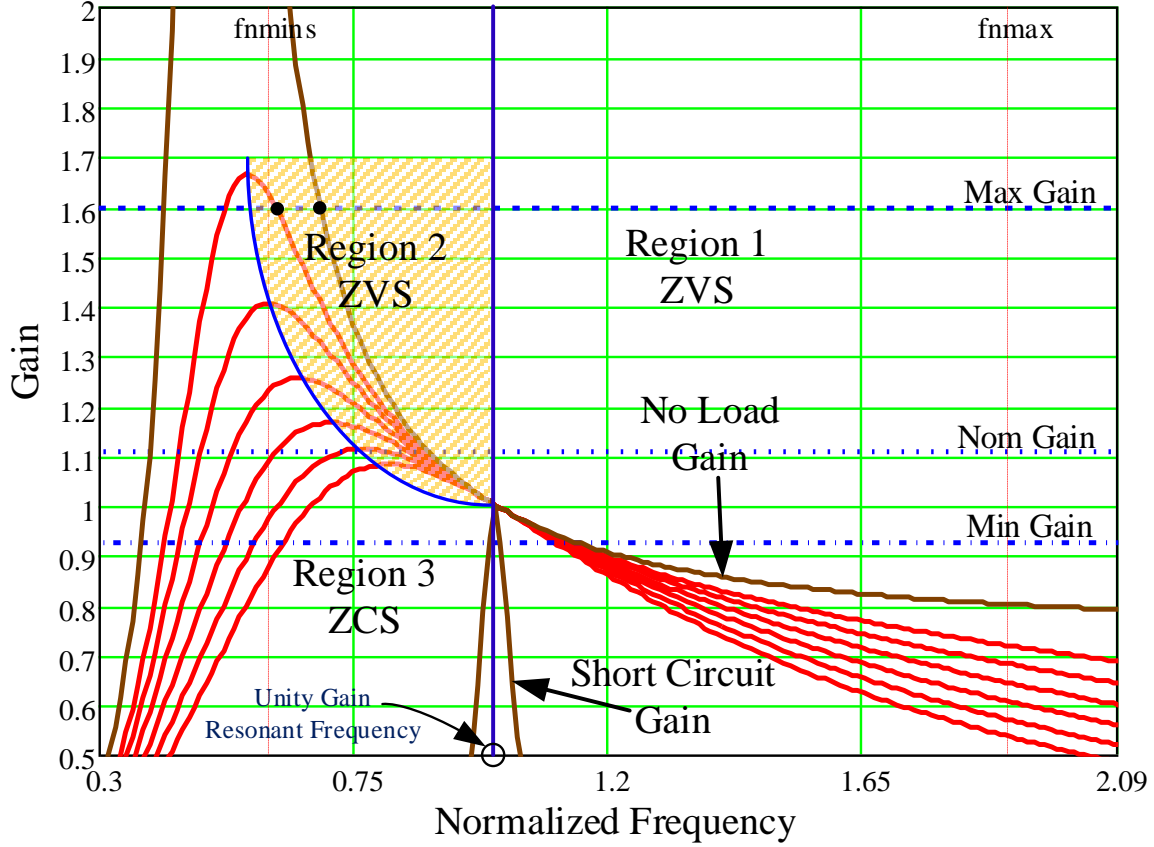
Figure 2.8 - Typical LLC Converter DC gain characteristic

Figure 2.8 [22] shows the normalized gain vs frequency characteristic of a LLC converter. As can be seen from Figure 2.8, the characteristics are split into three regions (the boundaries shown by the solid blue lines): Region 1, Region 2, and Region 3. It is desirable to operate the converter under ZVS conditions therefore the converter is operated in Region 1 and Region 2. Region 1 and 2 are located on the negative gradient of the DC gain curve and Region 3 is located on the positive gradient [23]. The resonant frequency f_o of the circuit is dependent on the series resonant inductor Lr and series resonant capacitor Cr that can be seen in Equation 2-2 [20].

$$f_o = \frac{1}{2\pi\sqrt{(L_r C_r)}}$$

Equation 2-2

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The magnetizing inductor Lm introduces a second resonant frequency when there is not load and it is given by Equation 2-3 [13], [20].

$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}$$

Equation 2-3

The LLC converter can operate in three modes depending on the input voltage and load conditions. The three modes of operations are [12], [20], [18]:

- At resonant frequency operation, $f_{sw}=f_o$.
- Above resonant frequency operation, $f_{sw}>f_o$.
- Below resonant frequency operation, $f_{sw}<f_o$.

2.3 LLC Converter Design Specifications
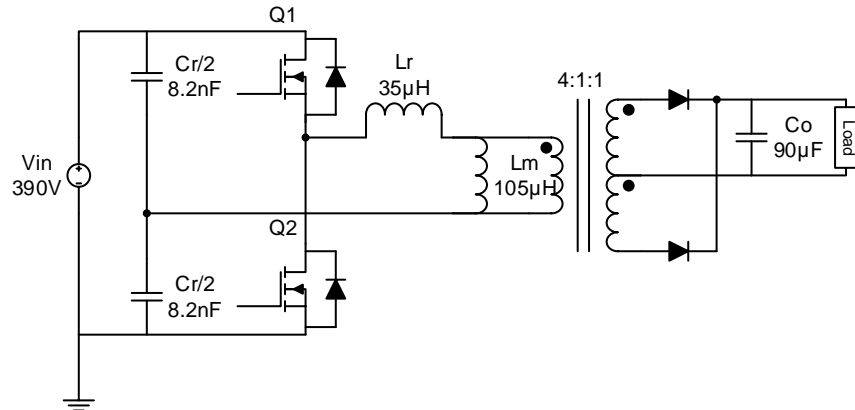
Figure 2.9 - LLC resonant converter basic design and component values

Figure 2.9 illustrates a simplified schematic of the LLC resonant converter design and its component values used for this research. The converter is designed for an optimal 48V output and maximum 650W output power. The switches Q1 and Q2 are driven using complementary 50% duty cycle square waves and the square wave's frequency is varied to control the converter. The specifications and component values of the converter are summarized in Table 2.2. These values represent the commercially available converter's design used in this thesis.

LLC Converter Specifications		
Parameter	**Symbol**	**Value**
Resonant Inductor	Lr	35 [µH]
Resonant Capacitor	Cr	2×8.2 [nF]
Magnetizing Inductor	Lm	105 [µH]
Transformer Ratio	n	4:1:1
Output Capacitor	Co	6×1.5 [nF]
Resonant Frequency	fr	210 [kHz]
2nd Resonant Frequency	fp	105 [kHz]
Switching Frequency Range	fsw	150 – 450 [kHz]
Input Voltage	Vin	370 – 410 (390 nominal) [V]
Output Voltage	Vo	36 – 72 (48 nominal) [V]
Max Load Current	Io$_{max}$	13 [A]
Max Output Power	Pout$_{max}$	650 [W]

Table 2.2 - LLC Converter Specifications and component values

2.4   LLC Plant Frequency Response
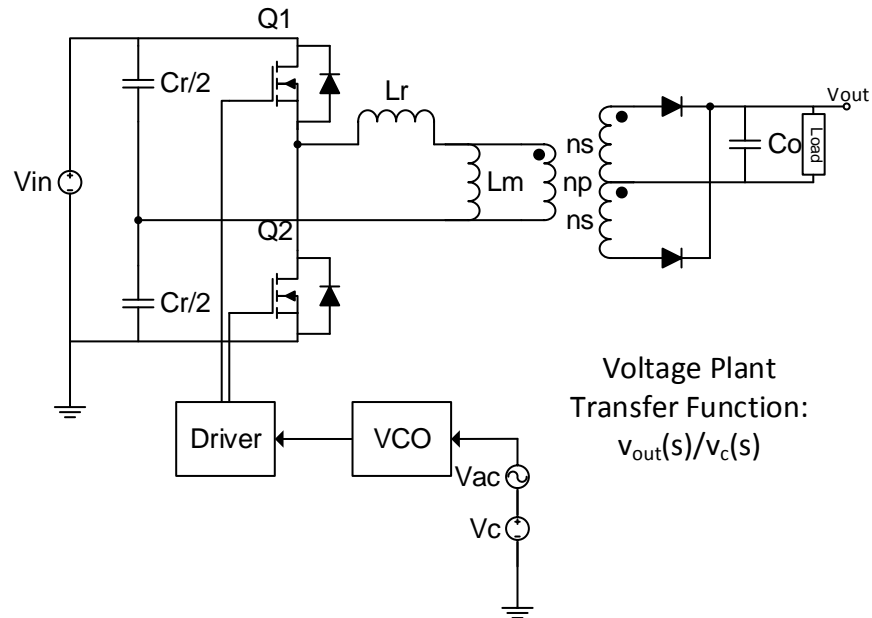
Figure 2.10 - LLC circuit setup for the plant control-to-output frequency response measurement

It is important to highlight how the LLC converter's plant dynamic characteristics change with the operating points. In this context, the operating points are effected by variations in the output voltage, output current, and load [21]. Figure 2.10 [16] illustrates how the control-to-output frequency response (or plant) was measured. The control voltage Vc is a DC voltage which sets the operating point for a given load. Then a perturbing small signal sinusoid voltage Vac of varying frequencies is added. The combined voltage of Vc and Vac is then fed into the voltage-controlled oscillator (VCO) which drives the switching frequency of LLC converter. The

control-to-output frequency response of the voltage plant is given by Equation 2-4. The current plant is given by Equation 2-5.

$$Voltage\ Plant\ Transfer\ Function = \frac{\widehat{v_{out}}}{\widehat{v_c}}$$
Equation 2-4

$$Current\ Plant\ Transfer\ Function = \frac{\widehat{\iota_{out}}}{\widehat{v_c}}$$
Equation 2-5

Figure 2.11 (Voltage Plant with Load=3.5 Ω), Figure 2.12 (Voltage Plant with Load=7 Ω), Figure 2.13 (Current Plant with Load=3.5 Ω), and Figure 2.14 (Current Plant with Load=7 Ω) help illustrate the plant variations under varying operating conditions and are simulated in PSIM. Two loads (3.5Ω and 7Ω) are considered over a range of output voltages and currents. It is noticed that the plant appears somewhat like a second order system where operations at, near, or below resonance appear to have a high Q factor. Operations above resonance results in the system poles splitting from a complex pole pair into two real poles [24]. It is also noticed that the overall shape of the magnitude and phase are very similar below 10kHz for the various operating points. The main difference is the magnitude (that can vary as high as 30dB) and the varying Q factor, which makes control design difficult.
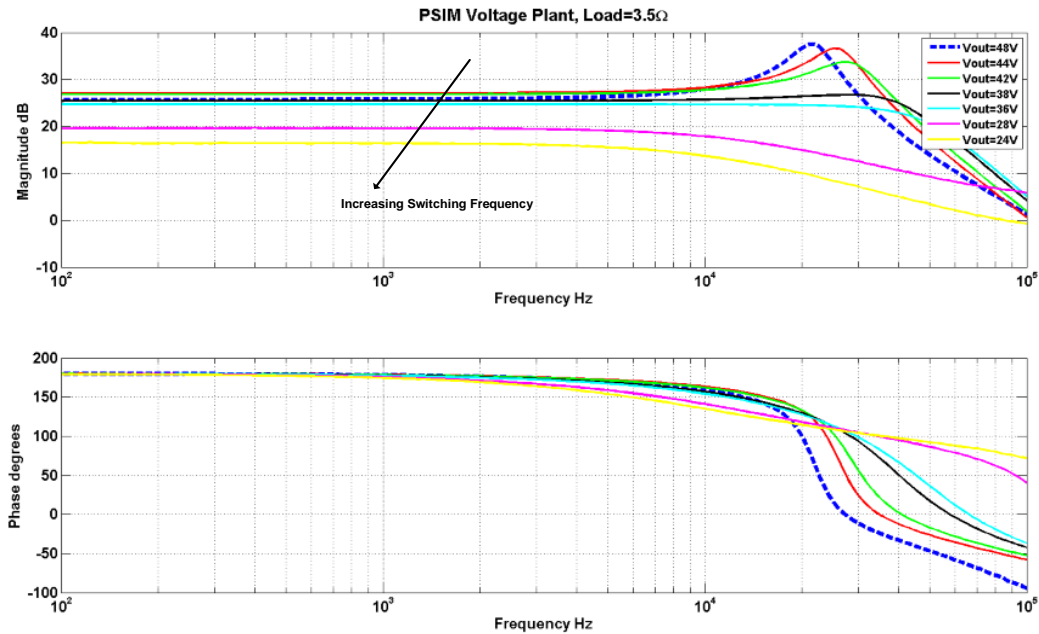
Figure 2.11 - LLC Voltage Plant frequency response with Load=3.5Ω (PSIM Simulation)
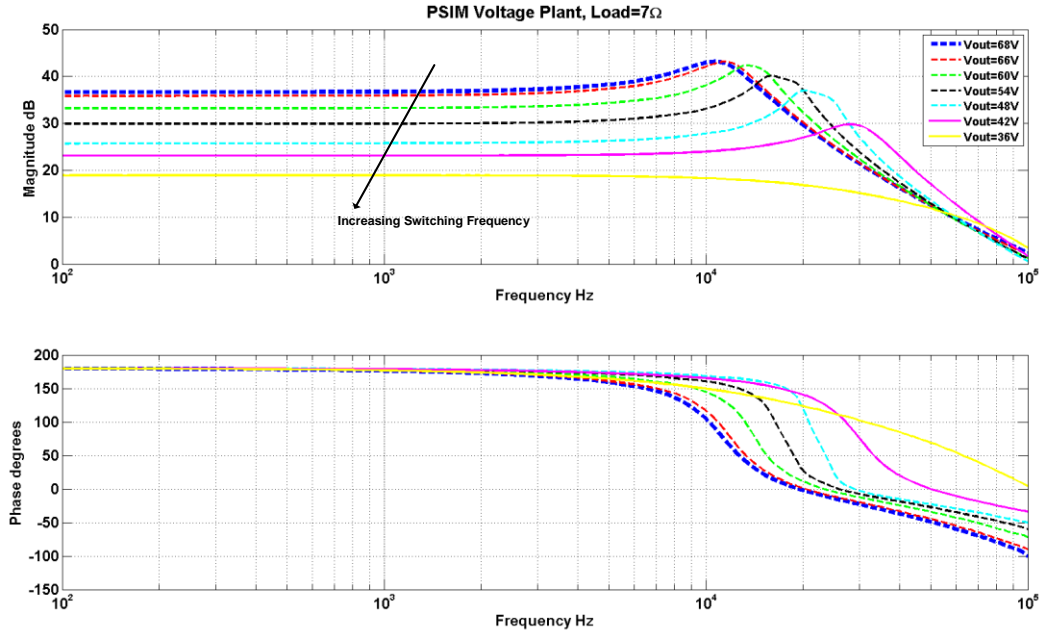
Figure 2.12 - LLC Voltage Plant frequency response with Load=7Ω (PSIM Simulation)

Table 2.3 summarizes the switching frequencies corresponding to the different output voltages for the plant frequency response in Figure 2.11-Figure 2.12. The lowest switching frequency is 155kHz and the highest is 380kHz.

Operating Point		Switching Frequency (fc)
Vout	**Load**	
48V	3.5Ω	208kHz
44V	3.5Ω	227kHz
42V	3.5Ω	236kHz
38V	3.5Ω	256kHz
36V	3.5Ω	265kHz
28V	3.5Ω	329kHz
24V	3.5Ω	380kHz
68V	7Ω	155kHz
66V	7Ω	158kHz
60V	7Ω	169kHz
54V	7Ω	182kHz
48V	7Ω	209kHz
42V	7Ω	245kHz
36V	7Ω	298kHz

Table 2.3 - Voltage Plant switching frequency for various operating points
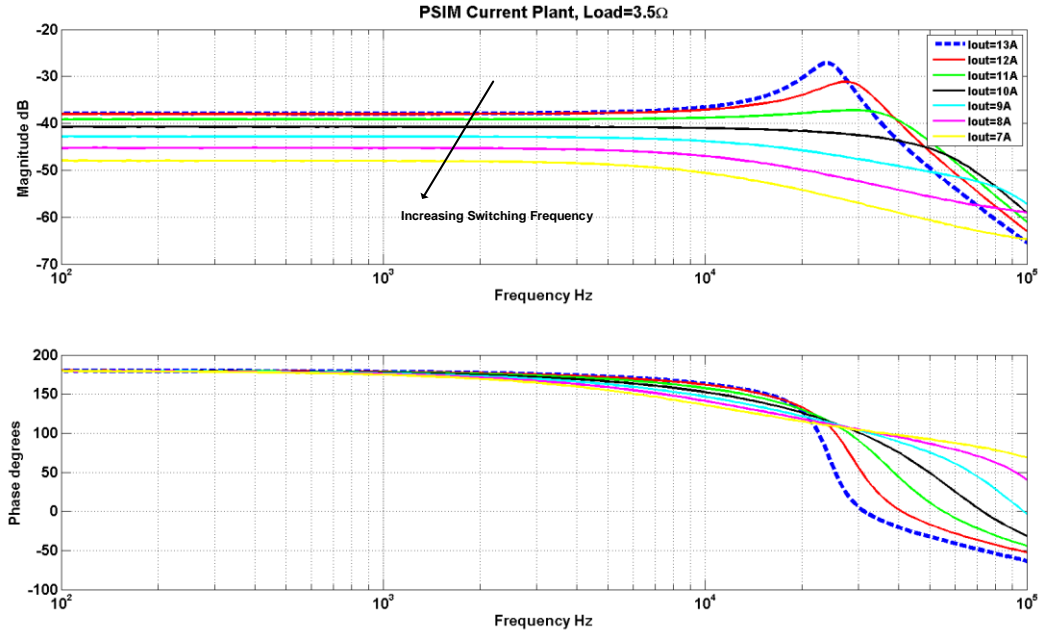
Figure 2.13 - LLC Current Plant frequency response with Load=3.5Ω (PSIM Simulation)
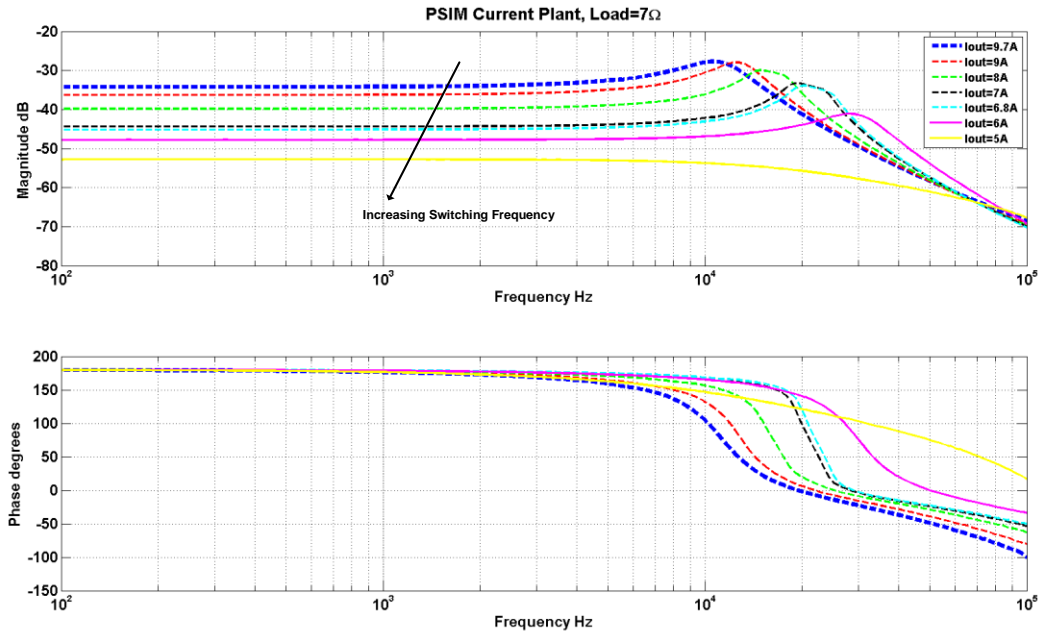
Figure 2.14 - LLC Current Plant frequency response with Load=7Ω (PSIM Simulation)

Table 2.4 summarizes the switching frequencies corresponding to the different output currents for the plant frequency response in Figure 2.13-Figure 2.14. The lowest switching frequency is 155kHz and the highest is 372kHz.

Operating Point		Switching Frequency (fc)
Iout	Load	
13A	3.5Ω	220kHz
12A	3.5Ω	236kHz
10A	3.5Ω	253kHz
9A	3.5Ω	272kHz
8A	3.5Ω	297kHz
7A	3.5Ω	329kHz
6A	3.5Ω	372kHz
9.7A	7Ω	155kHz
9A	7Ω	163kHz
8A	7Ω	179kHz
7A	7Ω	204kHz
6.8A	7Ω	209kHz
6A	7Ω	245kHz
5A	7Ω	310kHz

Table 2.4 - Current Plant switching frequency for various operating points

3 Digital Design Infrastructure Components and Considerations

The purpose of this chapter is to provide an overview of the components required to realize digital control on an existing analog controlled LLC converter. The objective is to implement a digitally controlled prototype with minimal modifications to the existing converter. The practical requirements components such as the sensing circuitry, the digital controller, and other digital design aspects will also be explored. For a designer, this is a useful way to determine the benefits of digital control without having to re-design a converter system for digital control.

3.1 Digital Design Infrastructure Overview

In this section, an overview of the digital design infrastructure and its components are given. A general explanation of each component, why they are needed, and how they interact with one another is given. In addition, some brief comments on certain design decisions are noted.
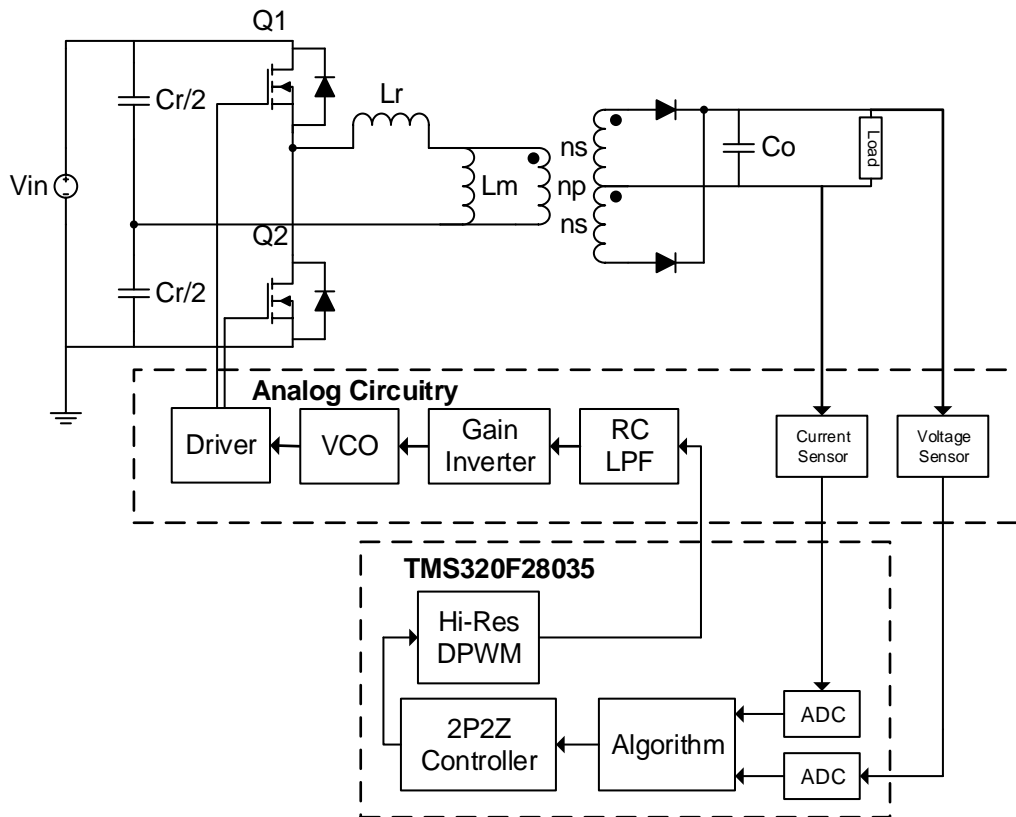
Figure 3.1 – High-level block diagram of the digital control infrastructure for the LLC converter

Figure 3.1 illustrates a high-level overview of the digital control infrastructure for the LLC converter. The system can operate in either current control mode or voltage control mode. The output current and voltage from the converter are fed into analog sensors, which are designed to scale the values to be compatible with the digital signal controller's (DSC) ADC. The Texas Instrument C2000 Piccolo TMS320F28035 is selected as the DSC. The DSC then performs all the necessary control logic (which is explained in more detail in Chapter 5) and outputs a digital PWM (DPWM) square wave. The PWM signal is fed into a RC low pass filter (LPF) in order to be smoothed out into a DC like voltage. The DC voltage is then fed into a gain inverter circuit, which functions to scale the voltage to a compatible range for the VCO input. It also inverts the DC signal (which is to say as the input to the gain inverter increases, the output will decrease and vice versa). This behaviour is implemented in order to compensate for the natural $180°$ phase offset of the LLC converter plant which is shown in Figure 2.11-Figure 2.14. The output of the gain inverter is then fed into the voltage-controlled oscillator (VCO) which then drives the switches. Note that since the VCO is designed to take an input DC voltage, the PWM signal from the DSC had to be low pass filtered hence the need for the RC LPF.

The reason why the DSC was not chosen to drive the LLC switches directly with frequency modulation was that it was decided safest to keep the already built in integrated circuit (IC) VCO chip to drive the switches. The built in VCO contains already integrated over voltage and current protection along with some other safety mechanisms, which was well test, and proven to work. Therefore, keeping the VCO allows for safer prototyping new control designs and performing tests. However, in order to implement digital control on the LLC converter while keeping the VCO, extra circuitry had to be introduced which were the third order RC low-pass filter and gain inverter circuit. As will be discussed later, adding these extra components introduces non-idealities and reduces the maximum potential system bandwidth. However, because the goal of this thesis is to provide a proof-of-concept on the benefits of a digital control vs analog control and to provide a simpler more accurate method of modelling a resonant converter, the disadvantages introduced by adding these extra components does not hinder accomplishing the goals.

3.2   Digital Components & Consideration

The following sections provide an overview and detail of some of the key features of the Texas Instruments C2000 Piccolo DSC that are needed to implement digital control on the LLC converter. A general summary of the DSC features is taken from the Texas Instruments TMS320F2803x datasheet [25] and shown in Appendix A: TI C2000 Piccolo TMSF28035 Specifications. The main features to take note of are: it has a fixed point 60MHz CPU, it is capable of fast interrupt and response processing, it has a programmable control law accelerator (CLA) (which is a separate floating point math processing unit), an on chip analog to digital converter (ADC), and a digital high resolution pulse width modulation (HRPWM) unit.

3.2.1   Analog-to-Digital Converter (ADC)

The analog output voltage and current signals are fed into their corresponding sensors which are then converted to digital signals with the help of the built in ADC module. To convert the continuous time signal to discrete time, the ADC samples the waveform at some sampling frequency usually in the kHz for power converters. Higher sampling rates produce better accuracy, but at the cost of increased CPU utilization [26], [27]. The sampled value is captured and then held until the next sampled value. Figure 3.2 [15] illustrates this process.
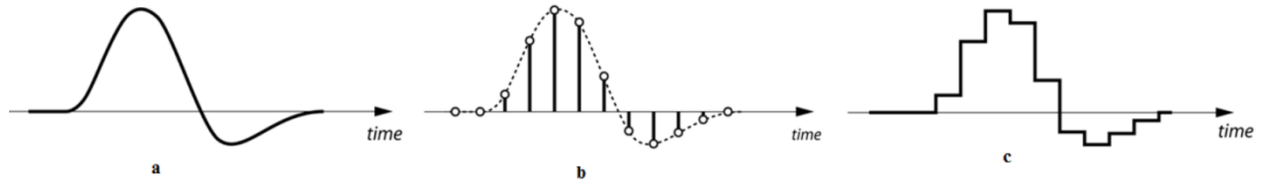
Figure 3.2 - Continuous to discrete signal conversion

The TMS320F28035 ADC module has a 12bit resolution and can take a maximum input voltage of $V_{max} = 3.3V$ [28]. The resolution indicates the number of discrete values it can produce over a range of analog values. For a resolution of 12bits we have 2^{12} (4096) discrete values that can be used to map an analog signal. The resolution for the ADC can be calculated using Equation 3-1 [28], where $V_{max} = 3.3V$, $V_{min} = 0V$, and n represents the number of bits.

$$Res = \frac{V_{max} - V_{min}}{2^n - 1}$$

Equation 3-1

Plugging in these values will give us the resolutions of the ADC:

$$Resolution = \frac{3.3 - 0}{4096 - 1} \approx 805\mu V \qquad\qquad \text{Equation 3-2}$$

The resolutions determine the magnitude of the quantization error. However thanks to the high resolution 12bit ADC, the quantization error is not a huge factor for this application.

3.2.2 High Resolution PWM (HRPWM)

The TMS320F28035 digital PWM (DPWM) module can generate a variable duty cycle square wave signal of magnitude 3.3V. As shown in [29], the precision of the PWM signal is dependent on the system clock speed, which is 60MHz for the TMS320F28035. A 60MHz clock speed provides a period of 16.67ns (1/60MHz) which is the minimum time step possible. Although a 16.67ns time step may seem very small, there will be resolution issues when operating at high PWM frequencies.

A high PWM duty cycle resolution is desirable not only for higher accuracy but also for stability. Digitally controlled switch-mode converters operating in closed loop have the possibility of building up limit cycles. The term limit cycle is used to describe the presence of oscillations occurring in the regulated output under steady-state operation that are the results of quantization errors in the control loop [30]. For a DPWM, limit cycles appear when the least significant bit (LSB) of the DPWM resolution is changing the output by a value that is larger than the resolution of the ADC [30], [31]. In other words, limit cycles occur when the DPWM bit resolutions is lower than the ADC bit resolution.
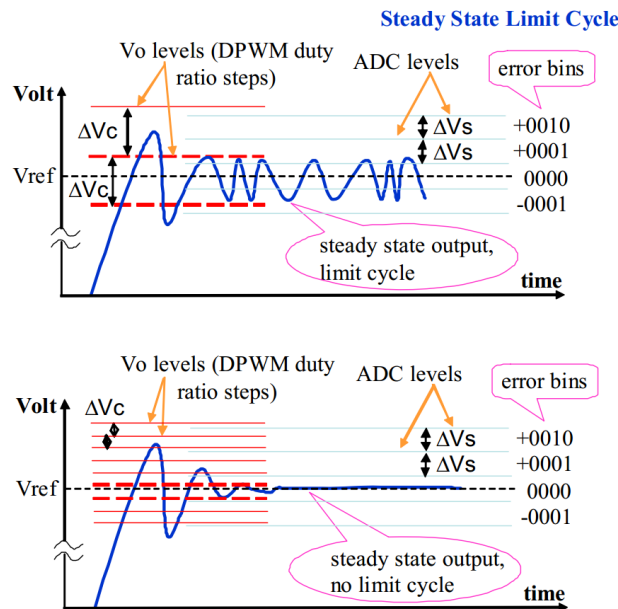
Figure 3.3 - Limit cycle effect

Figure 3.3 [32] show an example of the limit cycle effect. The top plot shows the delta ADC levels (ΔVs) to be smaller than the delta DPWM duty ratio steps (ΔVc) or in other words, the ADC resolution is higher than the DPWM resolution. Because of the lower DPWM resolution, the output voltage (Vo) has difficulty matching the reference signal therefore, it oscillates between the DPWM step values. The bottom plot in Figure 3.3 shows the delta ADC levels (ΔVs) to be larger than the delta DPWM duty ration steps (ΔVc) or in other words, the ADC resolution is lower than the DPWM resolution. In this case, because of the higher DPWM resolution, the output voltage is able to match the reference signal resulting in no limit cycle oscillation occurring.

The limit cycle issue is traditionally overcome by either reducing the ADC resolution, which results in lower output regulation accuracy, or by increasing the DPWM duty cycle resolution, which can be accomplished by decreasing the PWM frequency, dithering, or by hardware acceleration [30], [33]. In this thesis, the high ADC resolution will be kept at 12bits and the TMS320F28035 high resolution PWM (HRPWM) feature will be used in order increase the DPWM resolution while maintaining a high PWM frequency. A high PWM frequency is desirable because of the RC filter, which is explained more in Section 3.3.1.

PWM resolution (%) = $F_{PWM}/F_{SYSCLKOUT}$ x 100%

PWM resolution (bits) = $Log_2 (T_{PWM}/T_{SYSCLKOUT})$
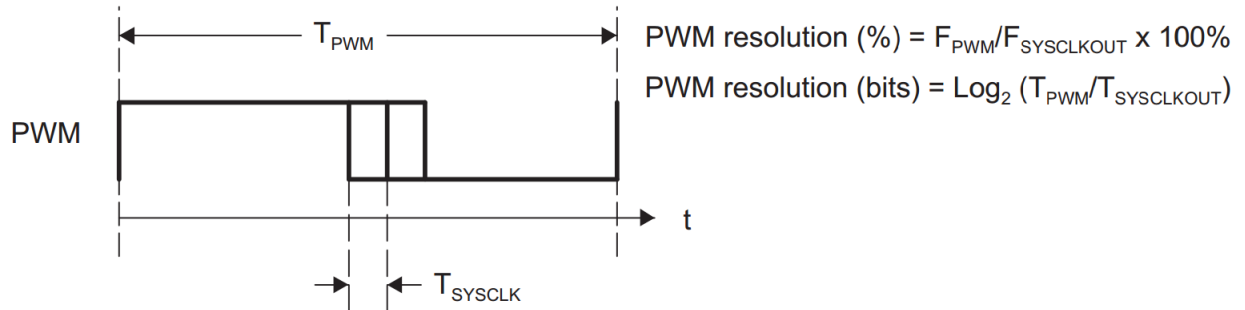
Figure 3.4 - Conventional generated PWM resolution calculation

Figure 3.4 [29] shows the resolution calculations for a conventionally generated PWM signal. Using the equations in Figure 3.4, it calculated that if the PWM frequency was set to 500kHz and system clock is 60MHz, the PWM resolution would be approximately 7bits which is less than the 12bit ADC resolution. This is not ideal because the lower PWM resolution will introduce the limit cycle effect. In order to achieve a 12bit resolution or higher for the PWM resolution, the PWM frequency has to be lower than 15kHz which is not high enough for the RC

filter (further explanation in Section 3.3.1). Fortunately, the TMS320F28035 DSC has a high-resolution PWM (HRPWM) module, which can extend the time resolution capabilities of the conventionally derived PWM.
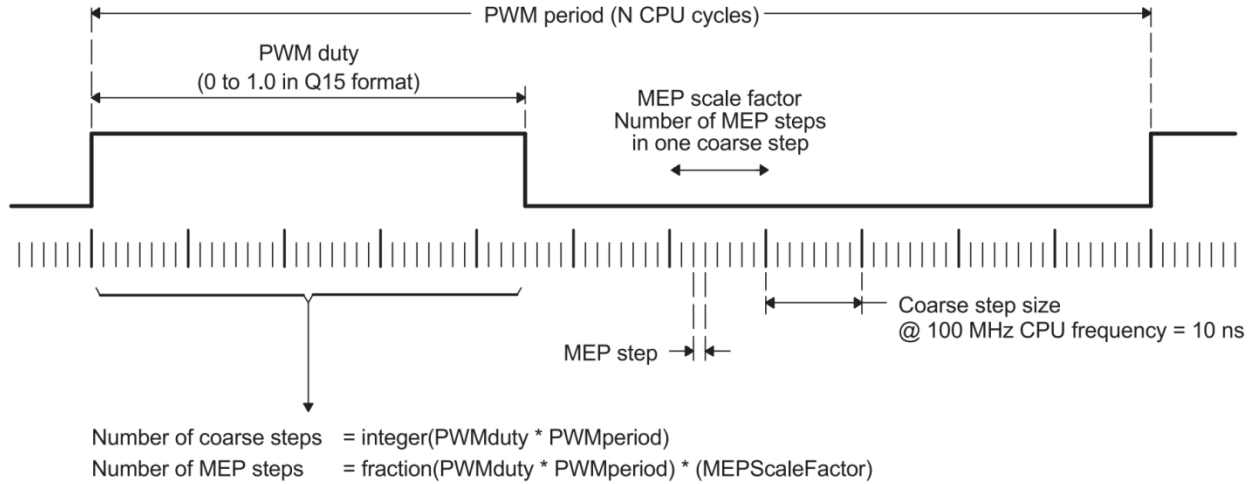
Figure 3.5 - Micro edge positioner (MEP) concept

The HRPWM is based on a micro edge positioner (MEP) technology that positions several edges in between one conventional system clock time step. This decreases the time step to potentially 150ps instead of the conventional 16.67ns time step for a 60MHz system clock [29]. Figure 3.5 [29] demonstrates the MEP concept.

Table 3.1 summarized the resolution comparison between the conventionally generated PWM and the HRPWM. The percentage resolution and bit resolution for varying PWM frequencies using a 60MHz system clock is compared. It is noted that in order to keep the bit resolution above the 12bit ADC resolution, the HRPWM frequency should not pass 1MHz. This is a substantial improvement over the conventional PWM resolution, which only allows 15kHz for a 12bit resolution.

Resolution for PWM and HRPWM @60MHz System Clock				
PWM Frequency (kHz)	**Conventional PWM Resolution**		**HRPWM Resolution**	
	Bits	**%**	**Bits**	**%**
20	11.6	0.0	18.1	0.000
50	10.2	0.1	16.8	0.001
100	9.2	0.2	05.8	0.002
150	8.6	0.3	15.2	0.003
200	8.2	0.3	14.8	0.004
250	7.9	0.4	14.4	0.005
500	6.9	0.8	13.4	0.009
1000	5.9	1.7	12.4	0.018
1500	5.3	2.5	11.9	0.027
2000	4.9	3.3	11.4	0.036

Table 3.1 - Conventional PWM resolution vs HRPWM resolution

3.2.3 Digital 2P2Z Compensator

A two pole two zero (2P2Z) infinite impulse response (IIR) filter structure is used for the voltage and current compensator. The discrete transfer function of the 2P2Z compensator is shown in Equation 3-3 [34] where z^{-n} represents a unit delay of n sample time steps.

$$\frac{U[z]}{E[z]} = \frac{b_2 z^{-2} + b_1 z^{-1} + b_0}{1 - a_1 z^{-1} - a_2 z^{-2}}$$

Equation 3-3

Equation 3-3 can also be represented in difference equation form as shown in Equation 3-4 [34] where $u[n]$ represents the present controller output, $u[n-1]$ represents the controller output from the previous cycle, $u[n-2]$ represents the output from two cycles previously. The same is concept applies to $e[n]$ which represents the controller input.

$$u[n] = a_1 u[n-1] + a_2 u[n-2] + b_0 e[n]$$
$$+ b_1 e[n-1] + b_2 e[n-2]$$

Equation 3-4

Figure 3.6 shows the 2P2Z controller graphically. A saturation limit is used so that the output is bound to a specific range [35].
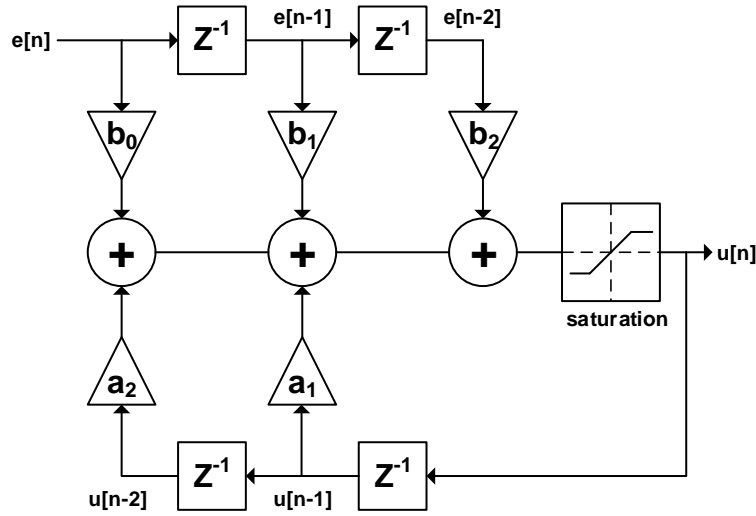
Figure 3.6 – Graphical representation of a 2P2Z IIR Filter with a saturation limit

The advantage of this type of IIR filter structure is that it can be expanded to a more complex 3P3Z filter by simply adding extra z^{-3} and b_3 and a_3 terms. However, this will require more memory and higher computation times [36].

3.2.4 Sampling Rate

One main disadvantage with digital control is its limited bandwidth when compared to analog control [37]. Choosing the sampling rate (or sampling frequency) is very important when implementing digital control. A high sampling rate allows for a high closed loop bandwidth and better high frequency signal representation [38]. Choosing a sampling rate is application specific. For power converters, it is desirable to have the sampling rate to be as fast as possible especially for high dynamic performance applications [39]. The sampling rate is limited by the CPU clock speed, complexity of the control code, and hardware capabilities. In order to achieve real-time control for a closed loop system, the control code should be finished processing before the next sample period. Increasing the sampling rate would decrease the period before the next sample therefore providing less time for the control code to complete. Figure 3.7 [32] illustrates this concept.

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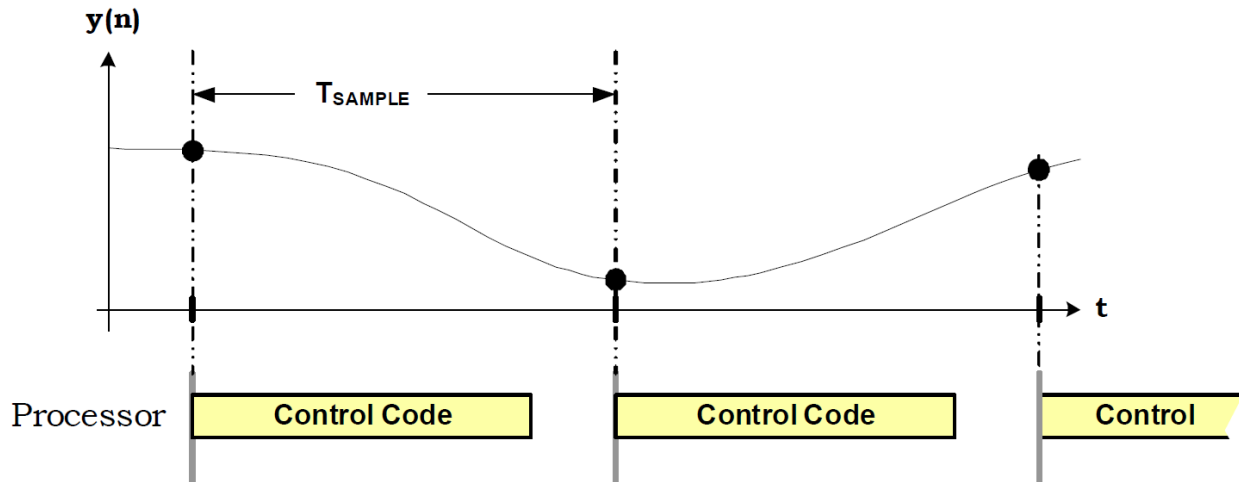
Figure 3.7 - Processor bandwidth vs control code

Table 3.2 shows several sample frequencies with their corresponding sampling period and the number of clock cycles for a processor clock speed of 60MHz (1 cycle = 16.67ns). The number of clock cycles corresponds to the amount of software code instructions that can be executed. The number of cycles is calculated by dividing the sampling frequency's sampling period by the 60MHz period or by dividing the 60MHz by the sampling frequency. As can be seen, the number of instructions is extremely limited at high sampling rates. A sampling rate of 1MHz or over would overload the processor for a single closed 2P2Z control loop as will be shown later.

Sampling Frequency (kHz)	Sampling Period (ns)	# of cycles for 60MHz CPU: (Sampling Period)/(16.67ns)
100	10000	600
250	4000	240
400	2500	150
500	2000	120
750	1333	80
1000	1000	60
1500	667	40
2000	500	30

Table 3.2 - Sampling frequency, sampling period, # of cycles for 60MHz CPU

The major advantage of a digital signal microcontroller compared to a traditional microcontroller is its superior hardware architecture which allows it to perform complex signal processing type math in a single clock cycle [8], [40]. An example is the multiply and accumulate (MAC) instruction which only takes one cycle to compute for a DSC whereas it would take multiple clock cycles for a traditional microcontroller. I chose a sampling frequency

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of 400kHz which gives me sufficient sampling accuracy and bandwidth while leaving enough overhead processing power for other control functions. At 400kHz sampling rate, the CPU can execute 150 cycles of instructions per sample period.

ADC Sequential Sampling Timings:
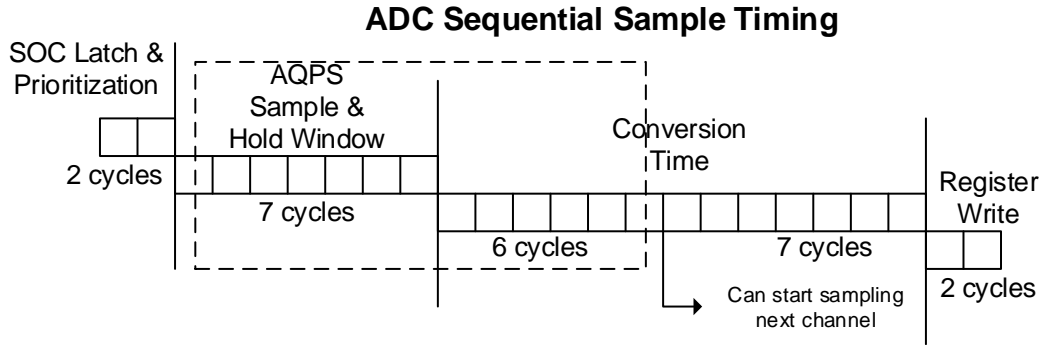
Figure 3.8 - ADC sequential sample timing

Figure 3.8 [41] shows the typical timing for a TMS320F28035 ADC conversion process. According to [28] it takes an initial 2 cycles for the Start of Conversion (SOC) to initialize but it only needs to be done once. The minimal sample and hold time is 7 cycles. Some circuits require longer times to transfer the charge into the sampling capacitor of an ADC so the sample window length can be extended. The conversion time takes 13 cycles but the sampling of another channel can start after the first 6 cycles of the conversion time. Lastly, it takes 2 cycles to write the data into a register. The ADC is capable of sampling at a maximum continuous rate of 4.6MSPS (million samples per second). This is calculated by 60MHz/13cycles. Table 3.3 provides a summary of sampling timings for an ADC conversion process of different sample window values. Each cycles take 16.67ns.

Clock Speed	Sample Window (cycles)	Sample Window (ns)	Conversion Time of 13 cycles (ns)	Register Write of 2 cycles (ns)	Total time to process analog signal (ns)	% of Processor load @400kHz sampling rate
60MHz	7	116.67ns	216.67ns	33.33ns	366.67ns	14.67%
60MHz	26	433.67ns	216.67ns	33.33ns	683.34ns	27.33%

Table 3.3 - Summary of sample timings for different sample window values

As can be seen, increasing the sample window time from 7 cycles to 26 cycles increased the CPU load from 14.67% to 27.33%, which is quite significant. The SOC initialization 2 cycles

is not included in the *Total time to process analog signal* time and the *% processor load* column calculations because it is only a one time initialization process. The *total time to process analog signal* is equal to the sum of the *sample window time*, *conversion time*, and *register write* time. The *% of processor load @400kHz sampling rate* column is calculated by dividing the total *time to process analog signal* column by 150*16.67 (150 is the number of cycles for a 400kHz sampling frequency running under a 60MHz processor clock).

Digital 2P2Z Compensator Timing:

As discuss previously, the digital compensator used is a 2P2Z discrete IIR filter. Texas Instruments provides pre-written software codes to calculate the 2P2Z equation shown in Equation 3-4. The code is written in assembly language in order to be as efficient as possible and takes 34 cycles to execute [34]. Table 3.4 shows the percentage utilization of the CPU for an interrupt service routine (ISR) running the control loop I implemented.

Control Loop Tasks	# of Cycles
Context save, restore, ISR management, etc.	27
ADCDRV_4ch	14
CNTL_2P2Z	34
PWMDRV_1chHiRes	10
Total ISR Loop Cycles	85
# cycles for 400KHz sampling with 60MHz CPU	150
% CPU Utilization for a @60MHz CPU	$85/150 \approx 57\%$

Table 3.4 – Percentage CPU utilization for the interrupt service routine implemented

As can be seen from Table 3.4, the combine CPU utilization for my ISR control loop is around 58%, which still allows more room to increase the sampling frequency. However, I chose to keep the sampling rate at 400kHz because it was sufficient. In addition, there is a slower background loop, which is in charge of the adaptive compensator selection therefore the extra CPU overhead

is needed for that. The extra CPU utilization overhead can also allow future more complex control loops to be implemented.

3.2.5 Interrupt Selection

The TMS320F28035 DSC has a total of 12 CPU interrupt groups with 8 interrupts per group equalling 96 possible interrupts. Appendix A shows a table [25] taken from the TMS320F2803x datasheet, which shows all the 96 possible interrupts. Some interrupts are not used and reserved for future devices. The interrupt activates the interrupt service routine (ISR) which samples from the ADC, calculates the 2P2Z compensation, and outputs the HRPWM. All this must be done before the next ISR is called as illustrated back in Figure 3.7. I chose the ePWM1 (INT3.1) to activate the ISR. The ePWM1 is set to 400kHz (the sampling frequency) and the ISR is set to activate on the falling edge of ePWM1.

3.3 Analog Components: Sensors & Filters & VCO

3.3.1 RC Low-pass Filter

As explained previously in Section 3.1, the input of the VCO (voltage-controlled oscillator) requires a DC voltage in order to modulate the switching frequency. As a result, the PWM waveform outputted by the DSC needs to be converted into a DC signal so that it can be compatible with the VCO input. An analog low pass filter (LPF) is used to filter the high frequency components of a PWM signal leaving only its low frequency component as illustrated in Figure 3.9 [42].
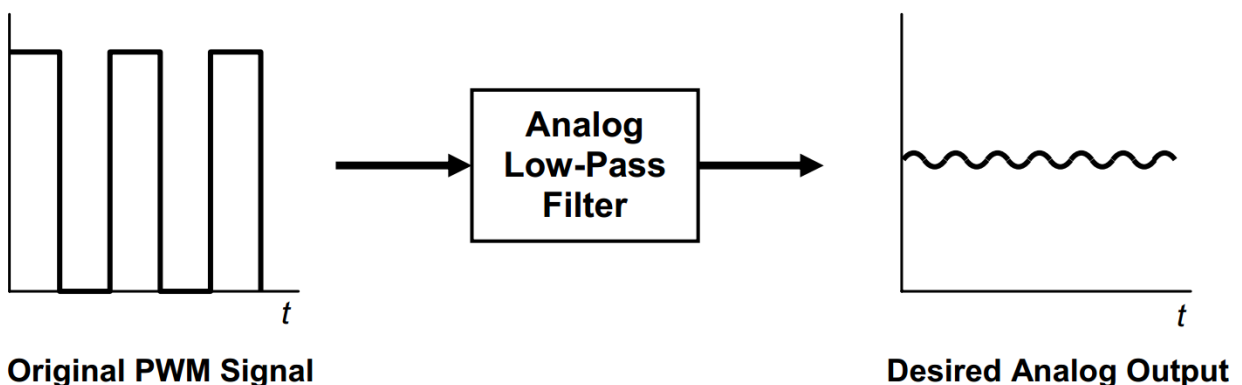
Figure 3.9 - PWM signal low pass filtered to a desired analog signal

The PWM signal outputted by the DSC is a variable duty cycle square wave with a 3.3V amplitude. This signal can decomposed into a DC component and square wave component as shown in Figure 3.10 [42].

Original PWM signal   **D.C. Component**   **Zero average square wave**
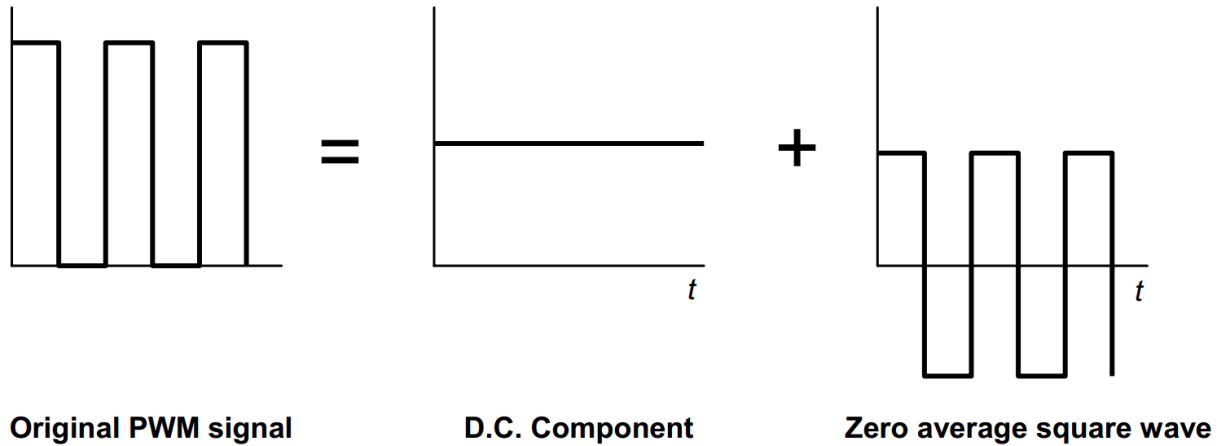
Figure 3.10 - Decomposition of PWM signal

The DC component is directly proportional to the PWM duty cycle. For example, a duty cycle of 50% will give a DC component of 1.65V (0.5*3.3V).

This approach of converting a digital PWM waveform to an analog DC signal can introduce performance issues, which limit its uses to low resolution and low bandwidth applications. The performance directly relates to the ability of the low-pass filter to remove the high frequency components of the PWM signal. If the filter has a low cut-off frequency, the overall system's bandwidth will suffer. However, increasing the cut-off frequency (which can also lead to slow stop-band roll-off) can reduce the DC signal resolution. One way to alleviate both these issues is to increase the PWM frequency. However, increasing the PWM frequency on a DSC results in decreased resolutions as discussed previously [42], [43]. However, thanks to the HRPWM capability of the TMS320F28035 DSC, these performance limitations can be overcome.

The low-pass filter used in this experiment is a 3rd order RC low-pass filter shown in Figure 3.11.
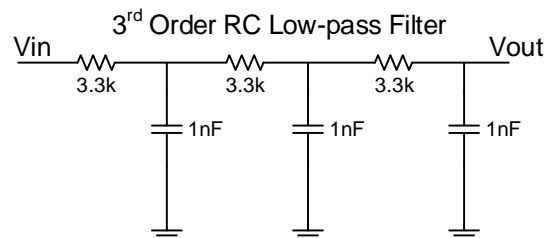
Figure 3.11 - RC 3rd order low-pass filter

Figure 3.12 shows the simulated PSIM frequency response (blue) and the physically measured frequency response (red) of the third order RC low-pass filter. The physical frequency response measurement was done by using a frequency response measuring equipment called the Venable Frequency Response Analyzer (FRA).
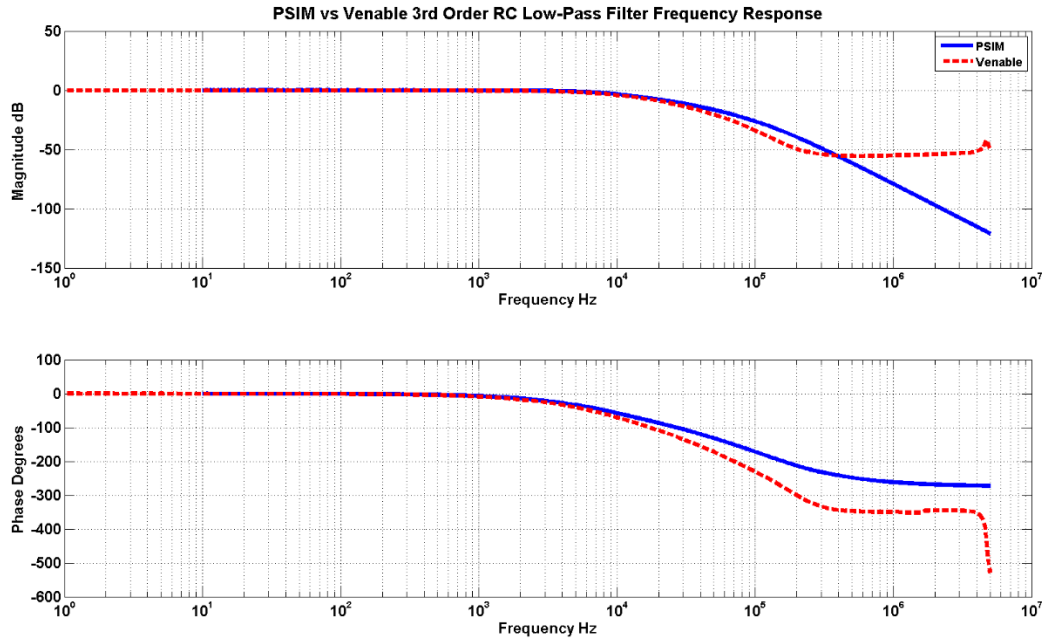
Figure 3.12 - Frequency response of RC 3ʳᵈ order low-pass filter (PSIM vs Venable)

It is observed that the physical frequency response measurement using the Venable starts to deviate from the PSIM simulation around 20kHz and its magnitude levels off after 200kHz. One possible reason is the effect of parasitic capacitance increasing the gain at higher frequencies, which the PSIM simulation does not account for.

It is desirable to reduce the high frequency ripple when filtering the PWM signal as was shown in Figure 3.9 therefore the PWM frequency should operate where the gain of the RC filter is low. According to the PSIM simulation, the RC filter has a continual roll-off slope of around -60dB per decade. However the Venable data shows the practical minimum achievable gain is around -50dB at 200kHz or greater. As a result, I chose to operate the PWM frequency at 200kHz. I did not choose to increase the PWM frequency to even higher frequencies (even though the HRPWM module can achieve a frequency of 1MHz while maintaining over a 12bit resolution) because higher frequencies may introduce more noise into the system. Operating the PWM at 200kHz and combined with the HRPWM feature provides a PWM resolution of 14.8

bits. It is important to note that the RC LPF introduces a non-desirable effect to the frequency response of the system such as phase lag and reduced gain after the cut-off frequency. However, this thesis will mainly focus on performance improvements using digital control below the RC LPF's cut-off frequency therefore making the negative RC LPF effects less significant.

3.3.2 Gain Inverting Op-amp Circuit
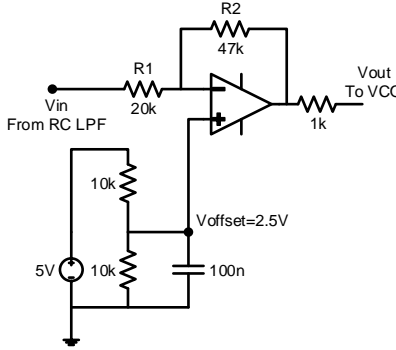
Figure 3.13 - Gain Inverting Op-amp (Gain Inverter)

The purpose of the gain inverting op-amp circuit shown in Figure 3.13 is to modify its input voltage range to be more compatible with the VCO input specifications and to compensate for the $180°$ phase shift in the LLC plant. (What is meant by the compensating for the $180°$ phase shift is that the circuit will inverse its output voltage value from the input: i.e.: as the input voltage increases, the output voltage decreases and vice versa.) This circuit act as an intermediate bridge placed between the RC low-pass filter and the VCO. I will just refer to it as the "*gain inverter*". The RC LPF outputs a voltage range of 0V to 3.3V while the VCO operates with an input voltage range of 1.3V to 6V. The gain inverter maps the voltage range of the RC LPF to the input voltage range of the VCO and it can be mathematically characterized by Equation 3-5 to Equation 3-7.

$$V_{out} = \left(1 + \frac{R2}{R1}\right) V_{offset} - \frac{R2}{R1} V_{in} \qquad \text{Equation 3-5}$$

$$V_{out} = 8.375 - 2.35 V_{in} \qquad \text{Equation 3-6}$$

$$V_{in} = 3.564 - 0.426 V_{out} \qquad \text{Equation 3-7}$$

3.3.3 Voltage Controlled Oscillator (VCO)

The voltage controlled oscillator (VCO) used in this thesis is the *ON Semiconductor NCP1395*. It is a high performance resonant mode controller that can output frequencies between

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50kHz to 1MHz. For this thesis, the LLC design requires an operating frequency range between 150kHz to 450kHz therefore the range of the VCO was set to that range. Figure 3.14 was taken from the NCP1395 datasheet showing the input voltage range vs output frequency range.
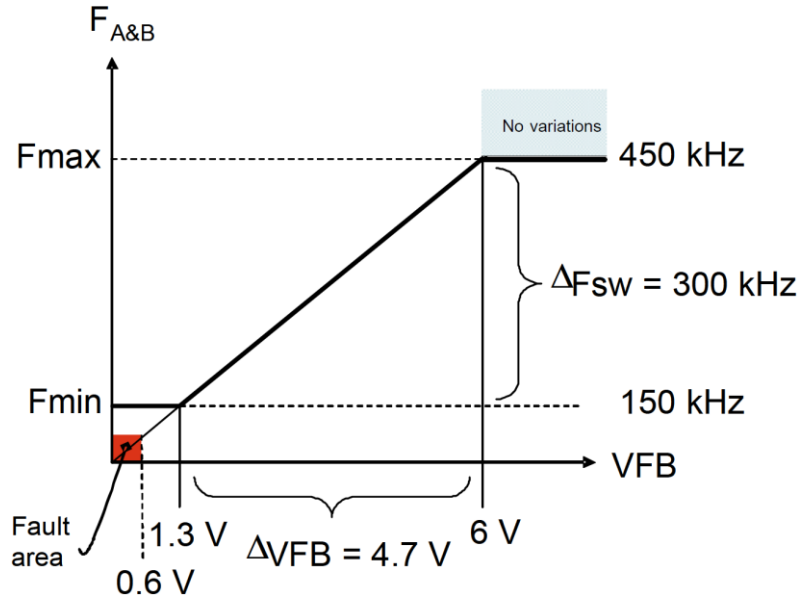
Figure 3.14 - NCP1395 VCO operating frequency range

The NCP1395 VCO is capable of an adjustable soft-start sequence, an adjustable dead time, over temperature protection, and can immediately shutdown for over voltage protection (OVP) or over current protection (OCP). It was because of these built in and already proven tested hardware features that it was decided to drive the LLC converter using the VCO instead of directly driving the LLC switches with the DSC's DPWM. Because of this decision, the RC LPF had to be added since the VCO cannot accept a PWM signal as input.

3.3.4 Voltage Sensor
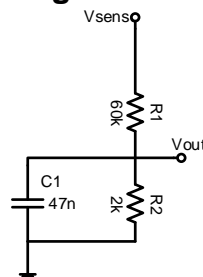
Figure 3.15 - Voltage Sensor for the Load

The output voltage range of the LLC load exceeds the 0V to 3.3V range of the ADC therefore it must be scaled down. The voltage sensor is just a simple voltage divider with a capacitive filter shown in Figure 3.15. Equation 3-8 gives its DC gain.

$$V_{out} = \frac{R_2}{R_2 + R_1} V_{in} = \frac{2k}{2k + 60k} V_{in}$$

Equation 3-8

$$= 0.03226 V_{in}$$

The LLC output voltage is designed for an operating voltage range of 36-72V. In order to design for overvoltage protection and to prevent saturation or damage to the ADC, a 100V margin was considered. This means that an output voltage of 100V would translate to 3.3V output from the sensor. Figure 3.16 shows a PSIM simulation frequency response of the voltage sensor. The cut-off frequency f_{cutoff} is calculated in Equation 3-9.

$$f_{cutoff} = \frac{1}{2\pi C_1 R_2}$$

$$= \frac{1}{2\pi (47 \times 10^{-9})(2000)}$$

Equation 3-9

$$\approx 1.7 kHz$$
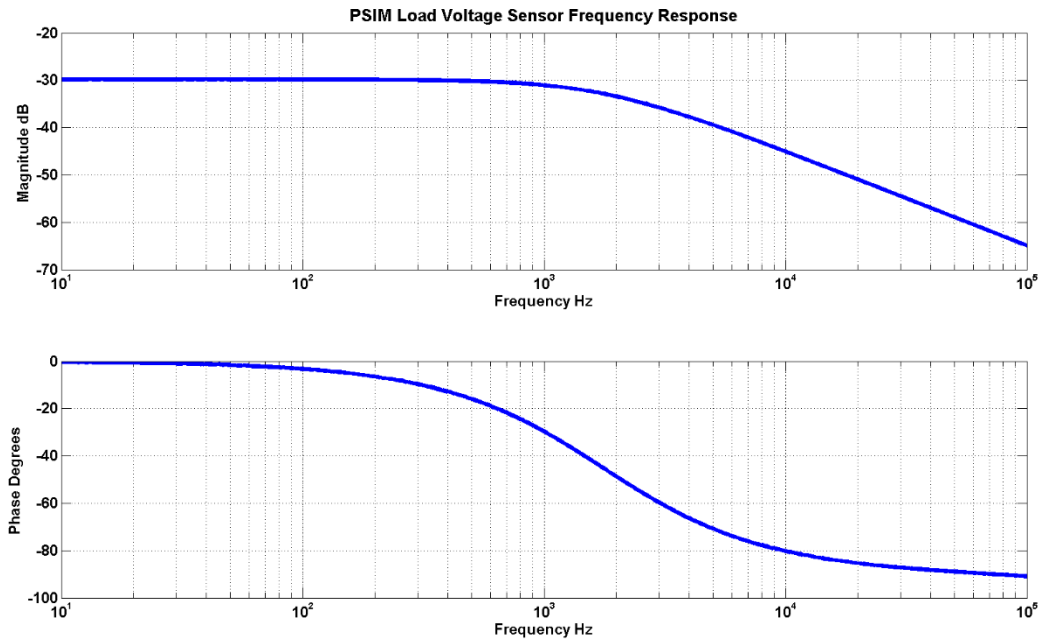
Figure 3.16 - Voltage Sensor Frequency Response (PSIM)

The low sensor bandwidth was chosen in order to help reject noise but with the disadvantage of limiting the bandwidth. The closed loop voltage control does not need to be extremely fast compared to the current control therefore having a low cut-off frequency of 1.7kHz was decided to be acceptable.

3.3.5 Current Sensor
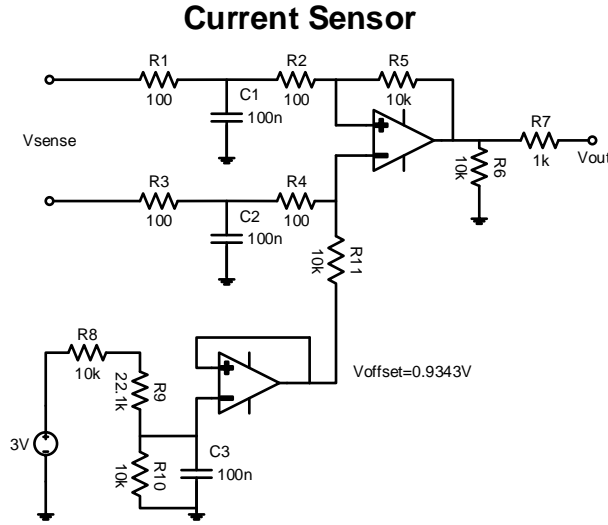
Figure 3.17 - Current Sensor for the Load

The load current is sensed by measuring the voltage drop across an accurate low resistance series resistor of 2mΩ. Using Ohm's law, the voltage drop can be converted to the output current. The LLC output load current is designed to operate at an optimal 13A. Current ripple, overcurrent conditions, and ADC protection must be also considered when designing the sensor therefore a safety margin of approximately 23A is used. Figure 3.17 shows the current sensor and is mathematically described in Equation 3-10 to Equation 3-12 where $V_{offset} = 0.9343V$. The capacitors C1 and C2 help filter noise. With a load of 13A, the output sensor voltage V_{out} is 2.23V, which is below the ADC 3.3V max input.

$$V_{out} = \frac{R5}{R5 + (R2 + R1)} V_{sense} + V_{offset} \qquad \text{Equation 3-10}$$

$$V_{out} = \frac{10000}{10000 + (100 + 100)} (0.002 \\ \times I_{load}) + 0.9343 \qquad \text{Equation 3-11}$$

$$V_{out} = 50(0.002 \times I_{load}) + 0.9343 \qquad \text{Equation 3-12}$$

Figure 3.18 shows the PSIM simulation of the current sensor's frequency response and Equation 3-13 gives the cut-off frequency f_{cutoff}.
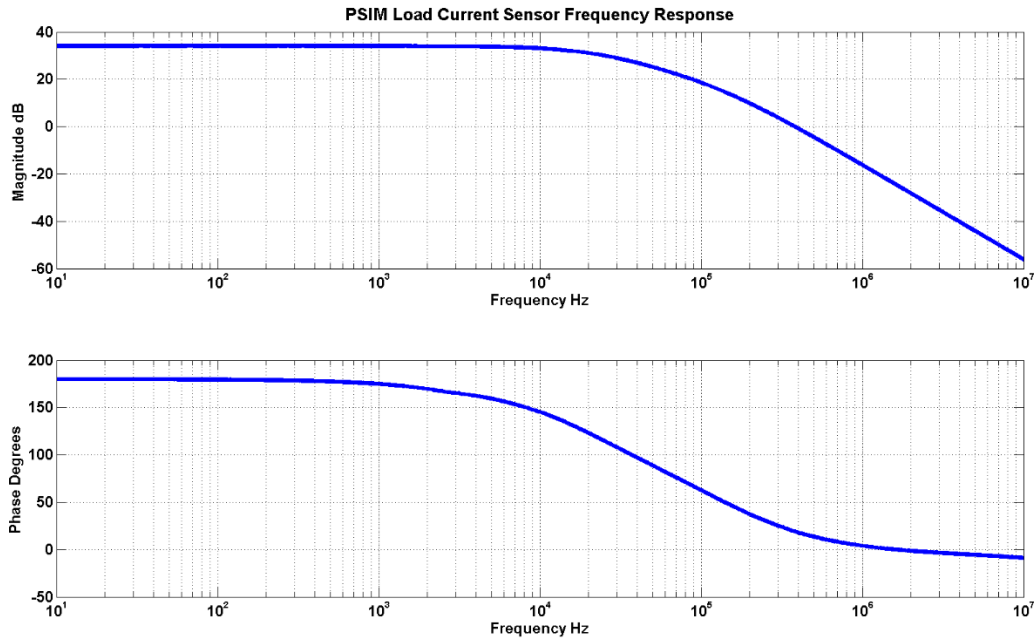
Figure 3.18 - Current Sensor Frequency Response (PSIM Simulation)

$$f_{cutoff} = \frac{1}{2\pi C_1 R_2}$$

$$= \frac{1}{2\pi(100 \times 10^{-9})(100)} \qquad \text{Equation 3-13}$$

$$\approx 16kHz$$

The current sensor has a cut-off frequency of around 16kHz which is much higher than the voltage sensor's 1.7kHz. The current sensor was given a much higher bandwidth because it is desirable to have a higher bandwidth for current control.

4   Digital Controller Design Implementation Process

4.1   Overview

Chapter 4 will discuss the full process used to design the digital compensator (or controller) for various operating points. To design the compensator, the control-to-output transfer function of the converter (or plant) model is needed. The definition the plant can be found in Section 2.4.

For PWM converters, standard averaging methods can be used to derive the mathematical transfer function model with good accuracy [16]. However, unlike PWM converters, the control-to-output transfer function of frequency controlled resonant converters cannot be obtained by averaging methods due to different ways of energy processing [44]. There are several methods for modeling resonant converters but most of them are too simplified and idealized while others are too complex and difficult to use [45]. Because of these difficulties, a different approach is presented in this thesis to model a resonant converter. The purpose of this thesis is to improve the performance of an already existing analog controlled LLC converter by implementing digital control. This means there is a physically built LLC converter available. Instead of attempting to use overly complex or simplified mathematical resonant converter modelling methods, the frequency response data of the physical converter is simply measured using a Venable frequency response analyzer (FRA) or simulated using PSIM. (The Venable FRA is a hardware which is capable of measuring the frequency response of a circuit.) The frequency response data acquired from Venable is imported into the MATLAB workspace environment. Then using MATLAB's System Identification Toolbox, a mathematical model based on the physically measured frequency response data is estimated. Once the mathematical model is estimated, MATLAB's SISO Toolbox is used to design the compensators in the continuous-time domain and then is converted into its discrete-time equivalent using the bilinear transformation method. This approach provides a more accurate (because it accounts for all the non-idealities in the system) and simpler way to design the compensator for the LLC resonant converter while avoiding the complex mathematical modelling techniques.

The obvious disadvantage of using the physical frequency response data to model the converter is the need for an already built physical converter. However, the frequency response data can also be obtained with simulation software such as PSIM. In Section 4.2, a PSIM model

of the LLC converter is made (shown in Appendix B: PSIM Simulation Schematics) and its frequency response data is simulated. The accuracy of the simulation depends on the accuracy of the PSIM model. Adding parasitic effects and other non-ideal effects can help accuracy but greatly increases an already lengthy simulation time. Therefore, those effects were not included in this thesis. Furthermore, adding more details to the simulation model does not guarantee better accuracy. However, as will be shown in Section 4.2.3, the basic PSIM simulation model provides a fairly accurate comparison to the physically measured Venable frequency responses for some operating conditions. However, the simulation accuracy seems to become much worse as the switching frequency increases.

Figure 4.1 shows a general high-level overview of the digital controller design process.
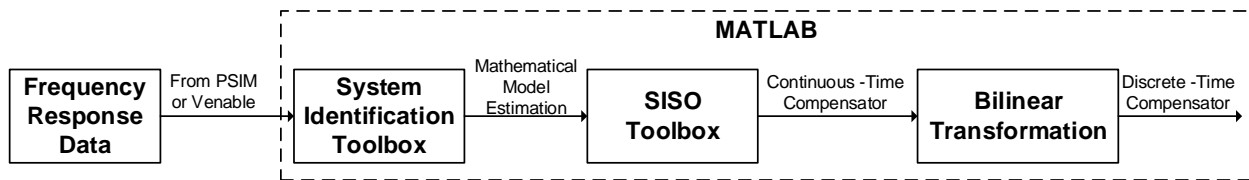
Figure 4.1 - High Level Overview of Digital Controller Design Process

4.2 Frequency Response Data

As explained in Section 4.1, the mathematical model can be estimated from either the Venable frequency response data or the PSIM simulated data. The frequency response data collected from Venable or PSIM contains the uncompensated loop gain which is what will be used to design the compensators in this thesis. The loop gain is defined in general as the product of the gains around the forward and feedback paths of the loop [20]. Figure 4.2 shows the components in the uncompensated loop-gain frequency response measurement. The uncompensated loop gain components include the RC low-pass filter, the gain inverter circuitry, the VCO, the LLC converter, and the voltage or current sensor. For voltage mode control, the uncompensated loop gain includes the voltage sensor in the loop measurements and for current mode control, the uncompensated loop gain includes the current sensor in the loop measurements.
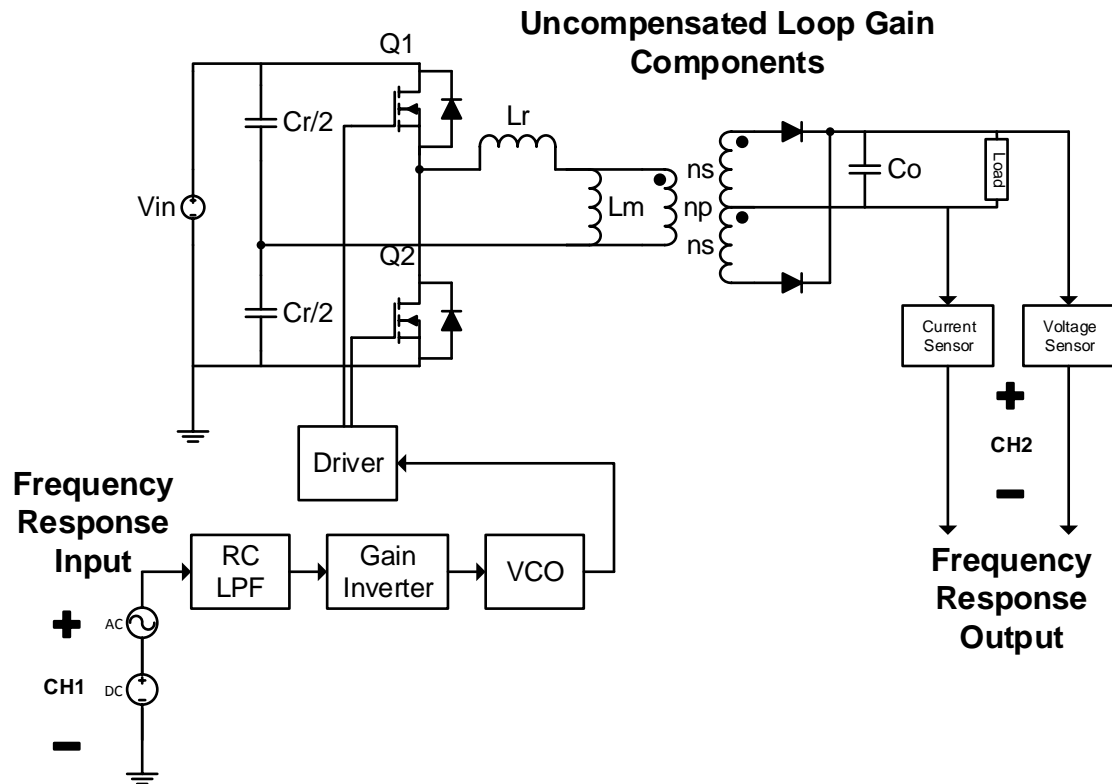
Figure 4.2 - Uncompensated loop gain frequency response components

4.2.1 Venable Frequency Response Analyzer

The Venable Frequency Response Analyzer hardware used is the *Venable 6305*, which can sweep up to 5MHz. Figure 4.3 shows the Venable software program's control menu settings used to sweep the frequency response of the LLC converter.
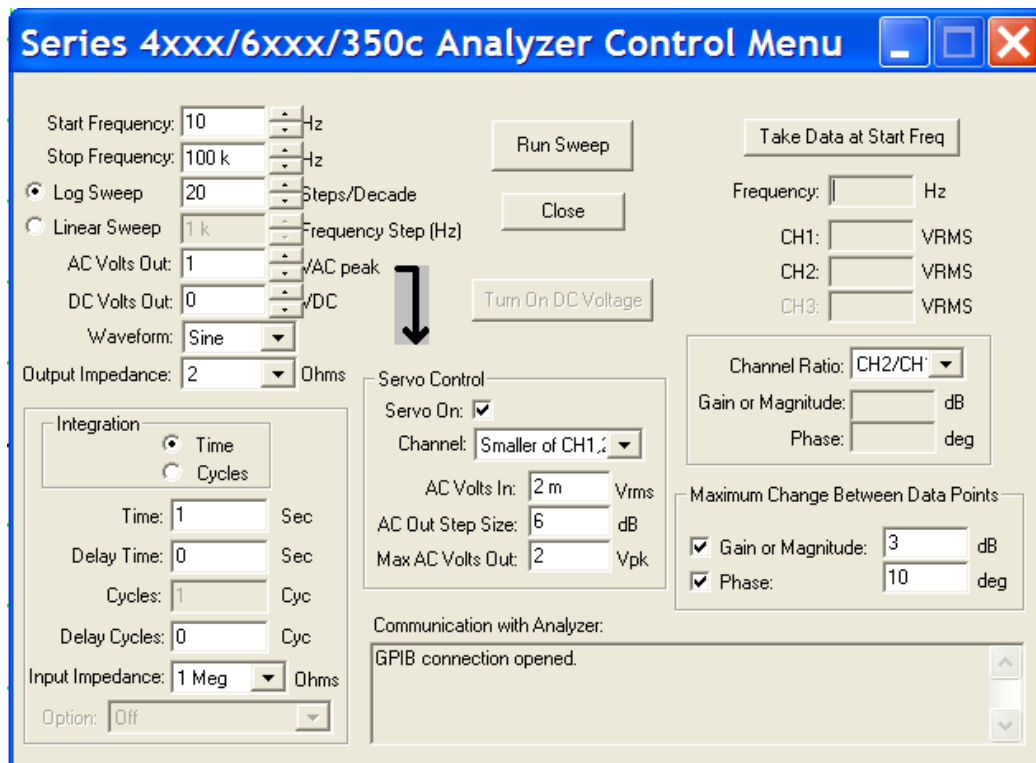
Figure 4.3 – Venable Software Program Frequency Response Analyzer Control Menu Settings

The frequency sweep range is set to 10Hz-100kHz with 20 data points per decade. If the maximum change between data points is more than 3dB for the magnitude or 10 degrees for the phase, extra data points will be automatically added. This way any major changes to the frequency response will be captured. The *DC Volt* output (which controls the steady-state switching frequency) sets the value for a chosen operating point. Enabling the *Servo Control* automatically adjusts the small signal *AC Volt Out* magnitude to maintain a set minimum of 2mV$_{rms}$ in either Channel 1 or 2. This is done because at higher frequencies, the gain of the converter drops which results in Channel 2 signal decreasing lower than the noise floor of the system. As a result, the *AC Volt Out* magnitude will automatically increase in order to maintain the signal of interest to be at least 2mV$_{rms}$ so that the signals can stay above the noise floor. The frequency response is calculated by dividing CH2 (output) by CH1 (input).

The following Figure 4.4-Figure 4.7 shows the Venable data results of the uncompensated voltage and current loop-gain frequency response for a resistive load. Two resistive loads were tested: 3.5Ω and 7Ω. The output voltage was varied for Figure 4.4 and Figure 4.5. The output current was varied for Figure 4.6 and Figure 4.7.

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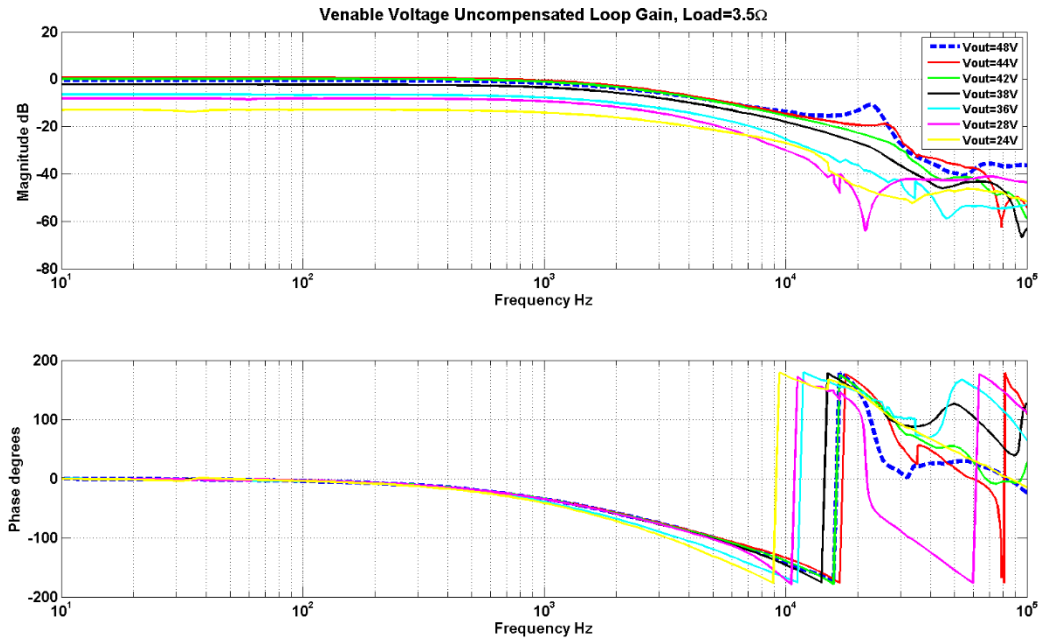
Figure 4.4 - Venable uncompensated voltage loop gain with load=3.5Ω (physical measurement data)
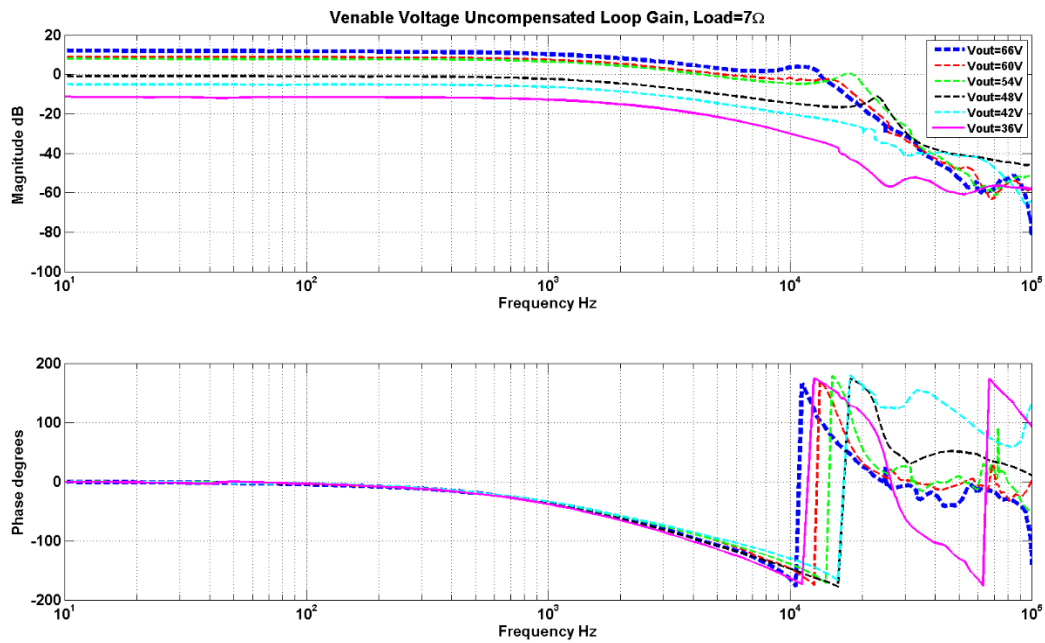
Figure 4.5 - Venable uncompensated voltage loop gain with load=7Ω (physical measurement data)

42
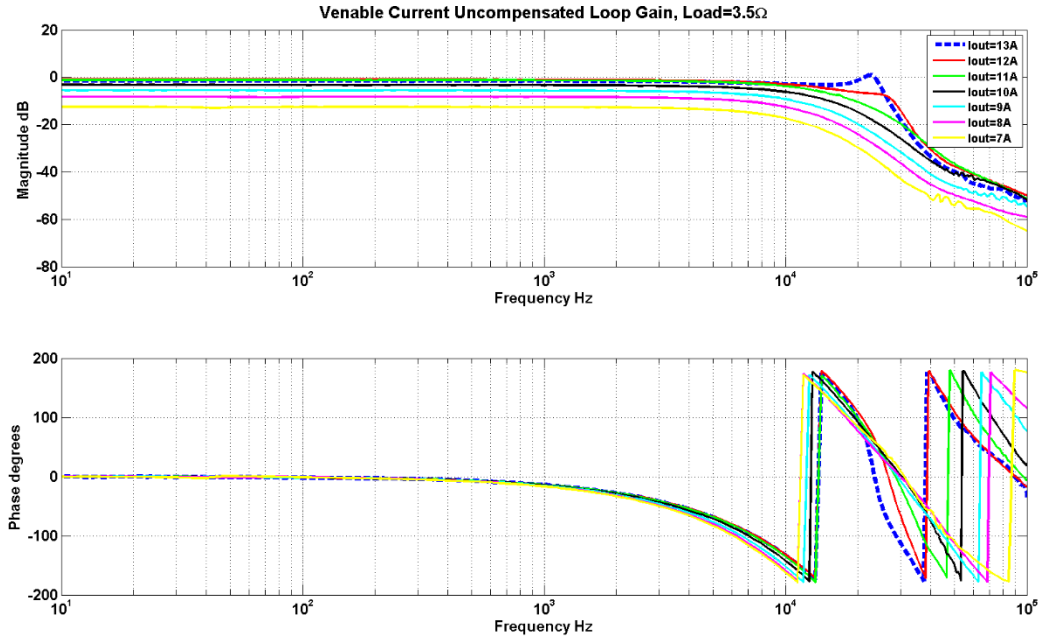
Figure 4.6 - Venable uncompensated current loop gain with load=3.5Ω (physical measurement data)
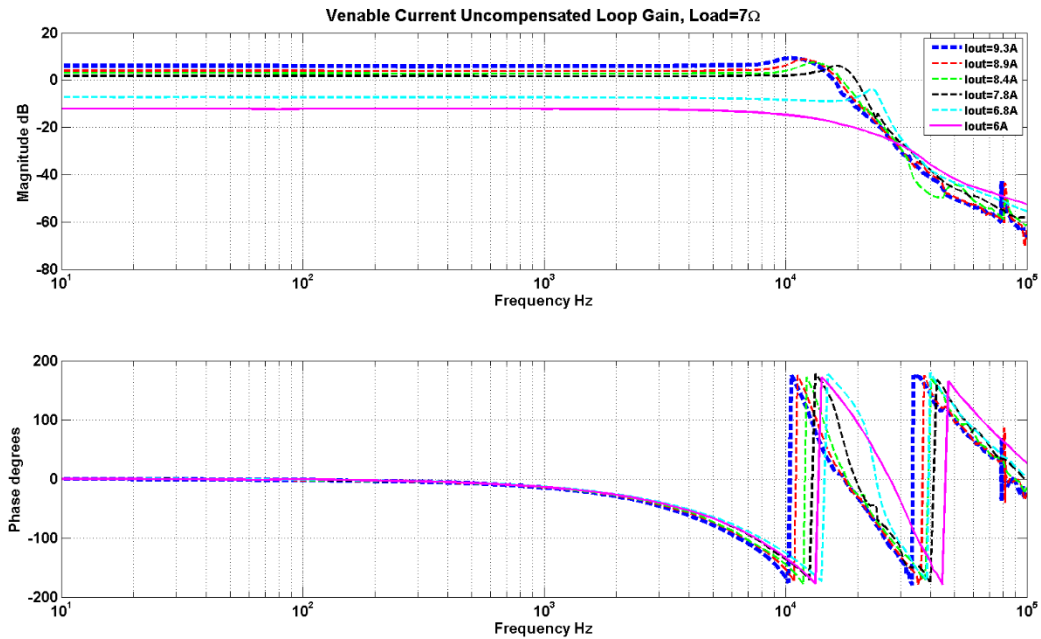
Figure 4.7 - Venable uncompensated current loop gain with load=7Ω (physical measurement data)

Note that when the phase reaches -180°, instead of continuing down, it jumps up to +180°, which is just how the relative angle is defined. The frequency response results become more distorted after 10kHz which coincides with the phase reaching close to -180°. When controlling the converter, I am only interested in frequencies below 10kHz. Some of the frequency response

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results are heavily distorted particularly for the low output voltage and current operating points. One of the possible reason for these distortions is the limitations of the Venable hardware. It is also noted that the frequency response magnitude varies up to 25dB for the various operating ranges.

4.2.2 PSIM

PSIM has a function call the "*AC Sweep*" [46] that can empirically calculate the frequency response of a circuit of control loop. The circuit can be in its original switch mode form and no average model is required. Figure 4.8 shows the *AC Sweep* settings I used to find the frequency response.
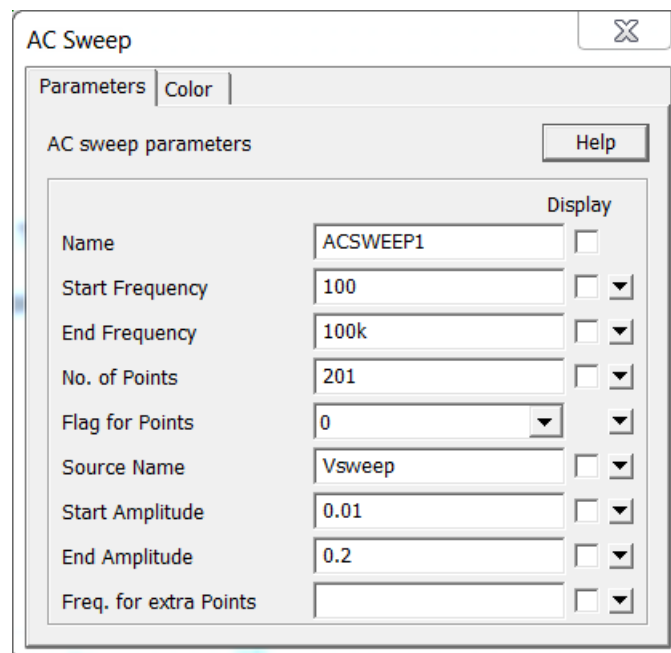
Figure 4.8 - PSIM AC Sweep setting

The frequency sweep ranges from 100Hz-100kHz with 201 data points spread out evenly. The starting AC perturbation amplitude is 10mV and ends at 200mV. I did not choose to set the *Start Frequency* lower (like 10Hz) because the simulation time would have taken exponentially longer. Also starting at sweep at 100Hz is sufficient because the frequency response shape does not change between 10Hz to 100Hz as can be seen in the Venable frequency response figures in Section 4.2.1.

Figure 4.9-Figure 4.12 shows the simulated PSIM data results of the uncompensated voltage and current loop-gain frequency response for a resistive load. Two resistive loads were tested: 3.5Ω and 7Ω. Varying voltages and currents were set to both the resistive loads.
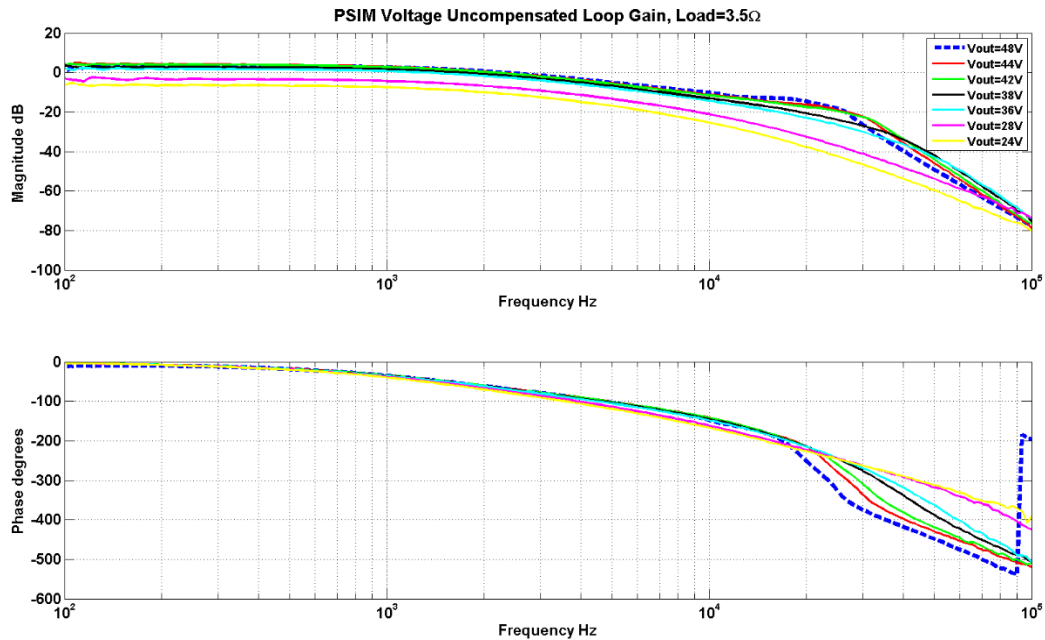
Figure 4.9 - PSIM uncompensated voltage loop gain with load=3.5Ω
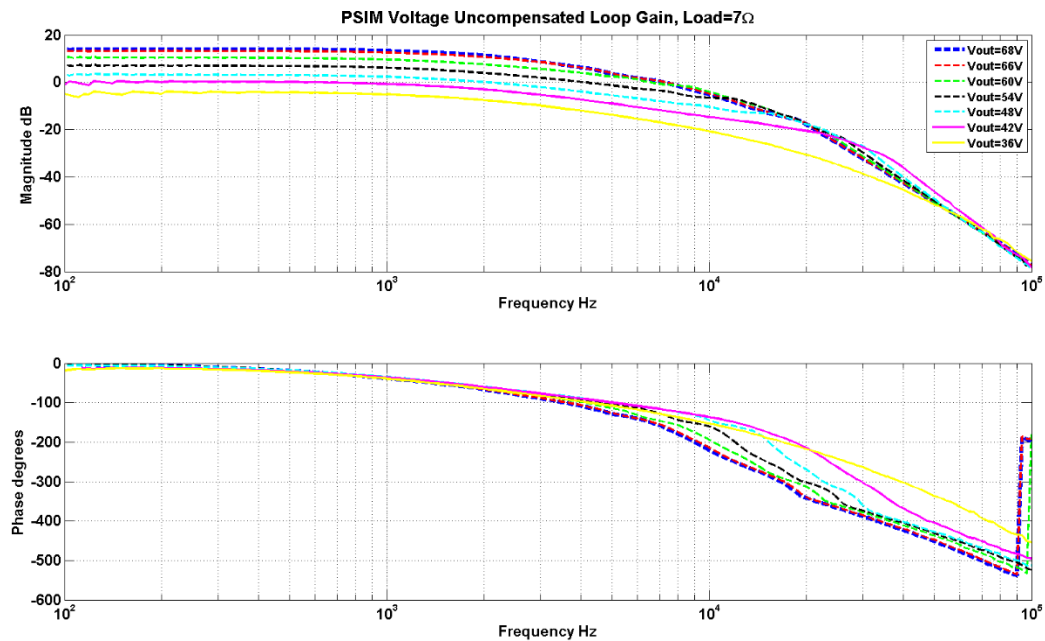
Figure 4.10 - PSIM uncompensated voltage loop gain with load=7Ω
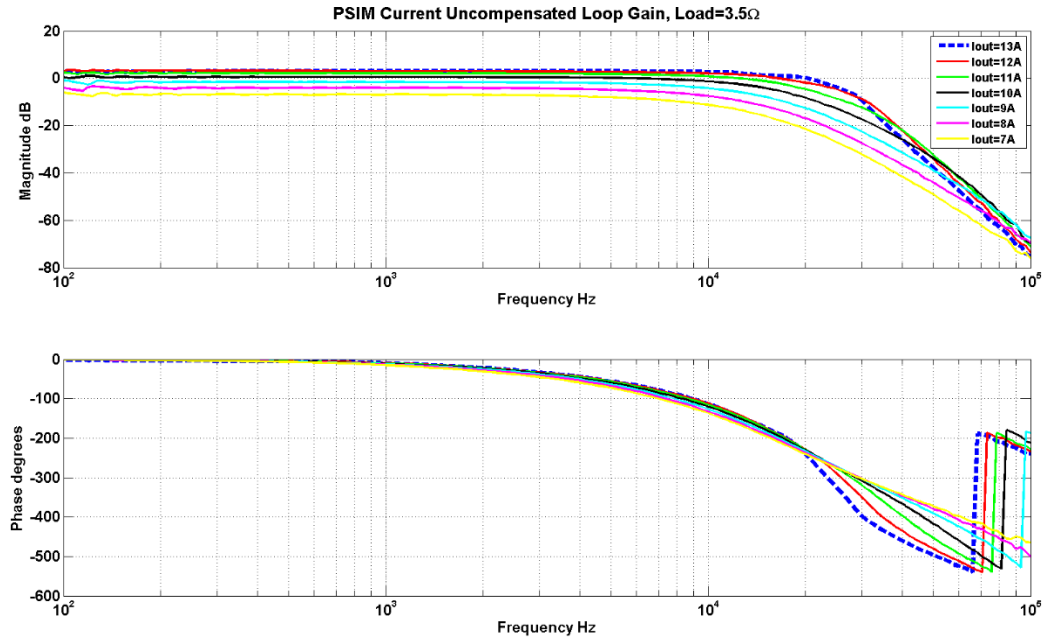
Figure 4.11 - PSIM uncompensated current loop gain with load=3.5Ω
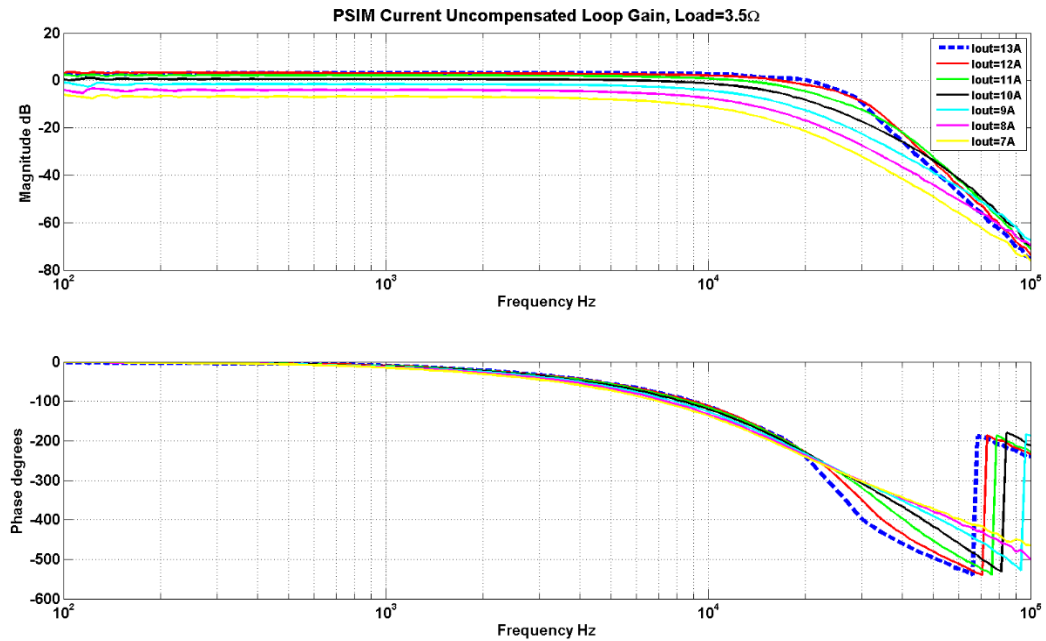
Figure 4.12 - PSIM uncompensated current loop gain with load=7Ω

The frequency response from the PSIM simulations are much smoother compared to the Venable frequency response because of ideal characteristics of the simulation components. The frequency response at different operating conditions also varies as much as 25dB.

4.2.3 PSIM vs Venable Frequency Response Data

In this section, a comparison between the Venable frequency response data and simulated PSIM frequency response data is presented. The comparison is made in order to see how accurate the PSIM model is when compared with to the Venable data and to explore the possibility of using the PSIM data to design the compensator instead of using the Venable data. As mentioned previously, the obvious advantage of using PSIM is that it does not need a physical converter to be built in order to obtain the frequency response.

Figure 4.13-Figure 4.16 shows the frequency response data of the voltage plant compared between the PSIM simulation data and Venable experimental data for several different output voltages and loads. Figure 2.10 shows how the frequency response of the voltage plant was measured. As can be seen, the general shapes of the frequency response are similar but there is a magnitude (or gain) difference between the simulation and experimental data. The magnitude varies from almost no difference in the Vout=66V and Load=7Ω operating condition (in Figure 4.15) to as much as 8dB gain difference in the Vout=36V and Load=7 Ω operating condition (in Figure 4.16). It is also noticed that the Venable frequency response magnitude is always lower than the PSIM frequency response data and the difference in magnitude between the two becomes larger as the output voltage (Vout) becomes smaller (decreasing output voltage corresponds to increasing the switching frequency fsw).
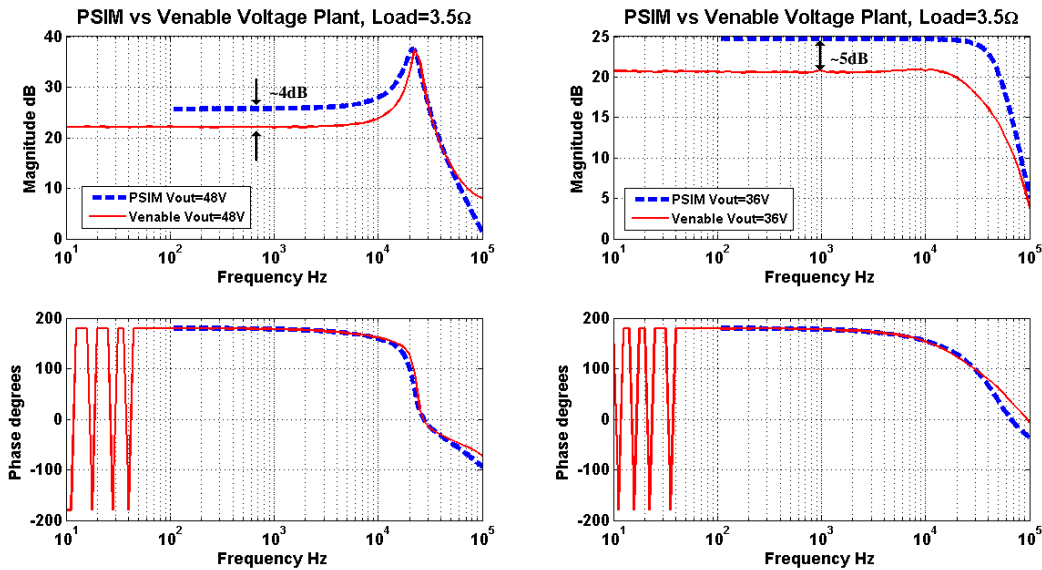
Figure 4.13 - Voltage Plant, Vout=48V & 36V, Load=3.5Ω (PSIM vs Venable)
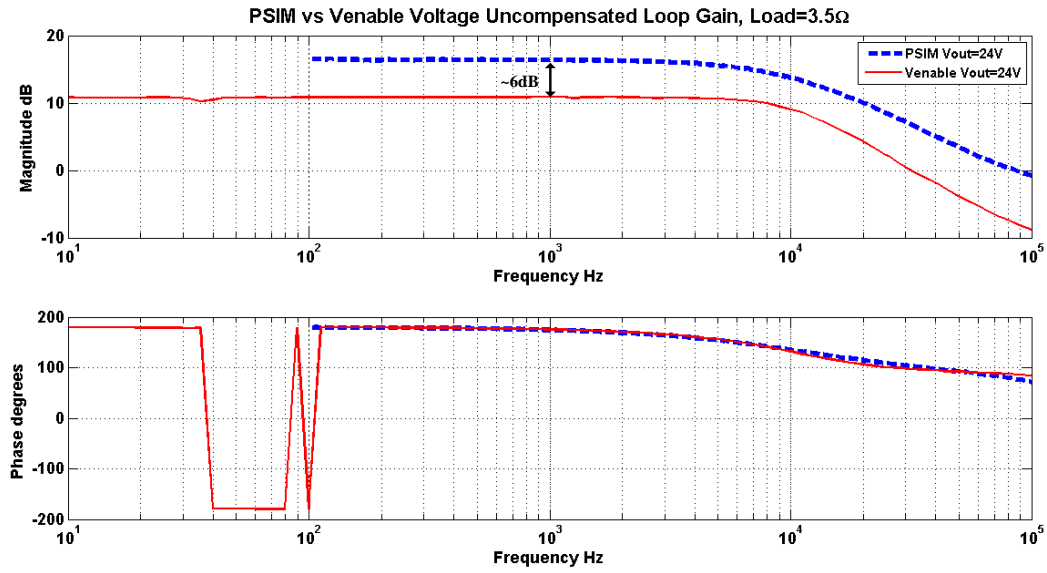
Figure 4.14 - Voltage Plant, Vout=24V, Load=3.5Ω (PSIM vs Venable)
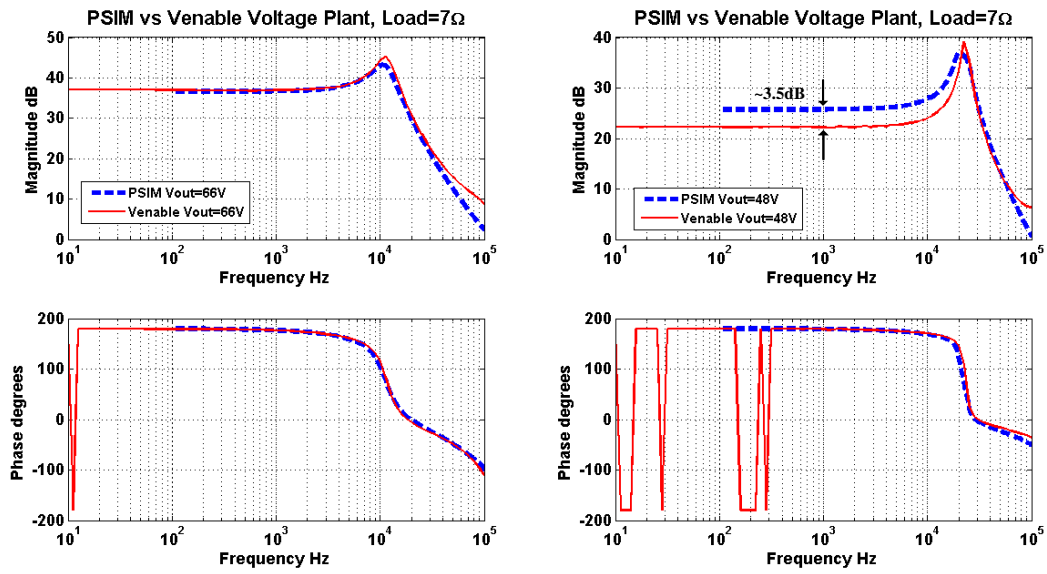
Figure 4.15 - Voltage Plant, Vout=66V & 48V, Load=7Ω (PSIM vs Venable)
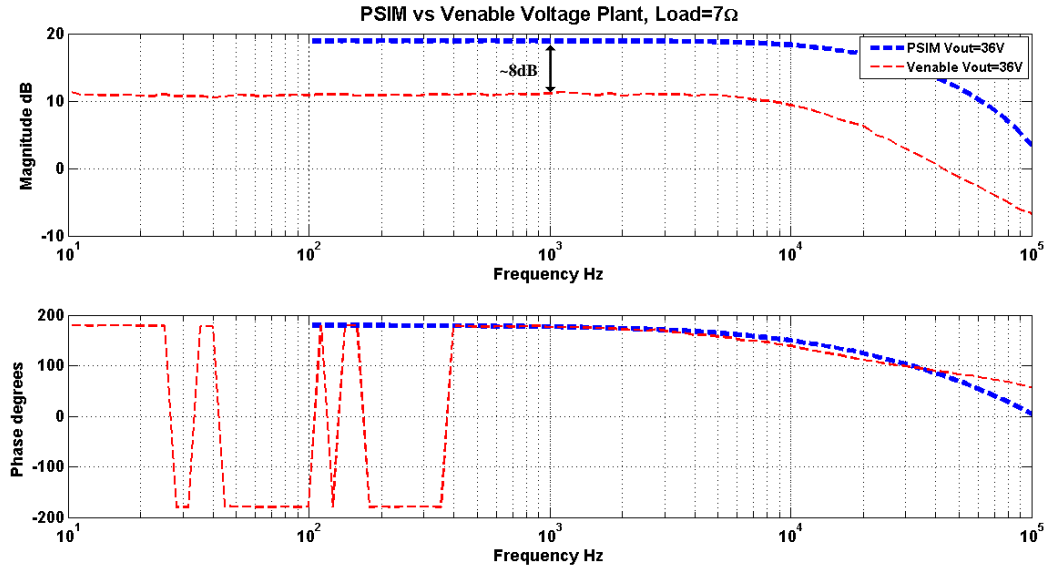
Figure 4.16 - Voltage Plant, Vout=36V, Load=7Ω (PSIM vs Venable)

Figure 4.17-Figure 4.19 compares the uncompensated voltage loop-gain frequency response of the PSIM simulations with the corresponding physical Venable data for several operating conditions. Figure 4.20 and Figure 4.21 shows the uncompensated current loop gain for the loads of 3.5Ω and 7Ω. The uncompensated loop gain includes the RC filter, Gain Inverter, VCO, the LLC converter plant, and the voltage/current sensor as was shown in Figure 4.2.
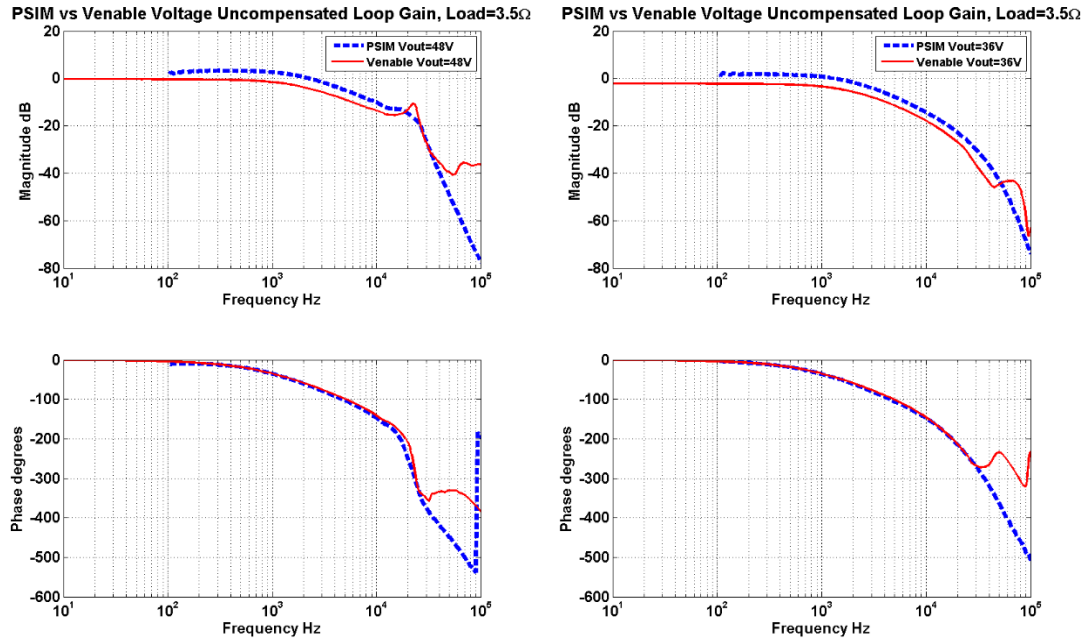
Figure 4.17 - Uncompensated voltage loop gain, Vout=48V & 36V, Load=3.5Ω (PSIM vs Venable)
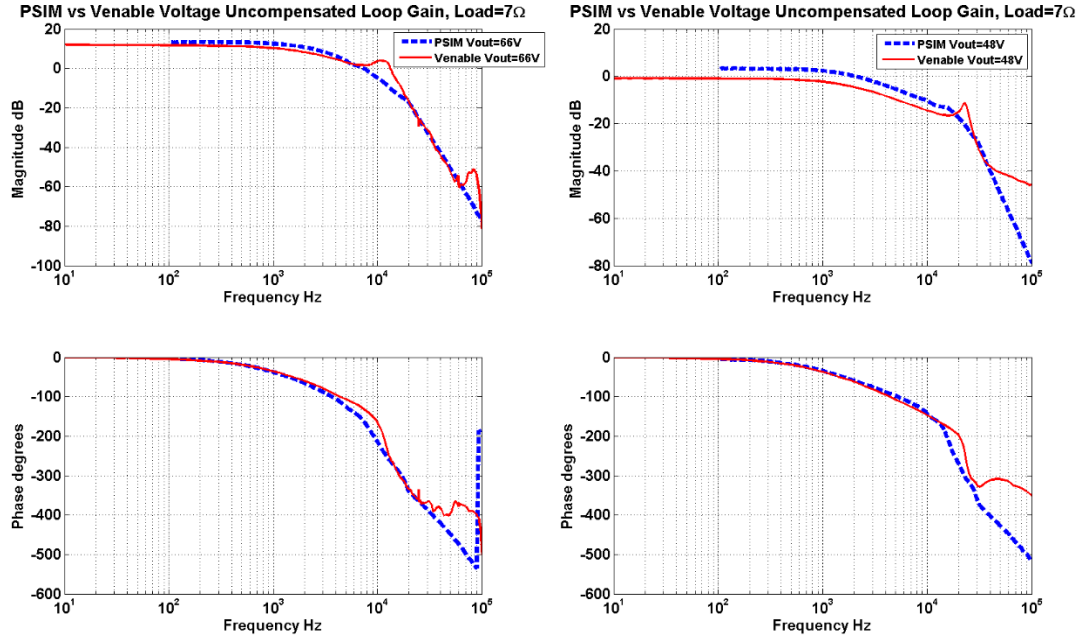
Figure 4.18 - Uncompensated voltage loop gain, Vout=66V & 48V, Load=7Ω (PSIM vs Venable)
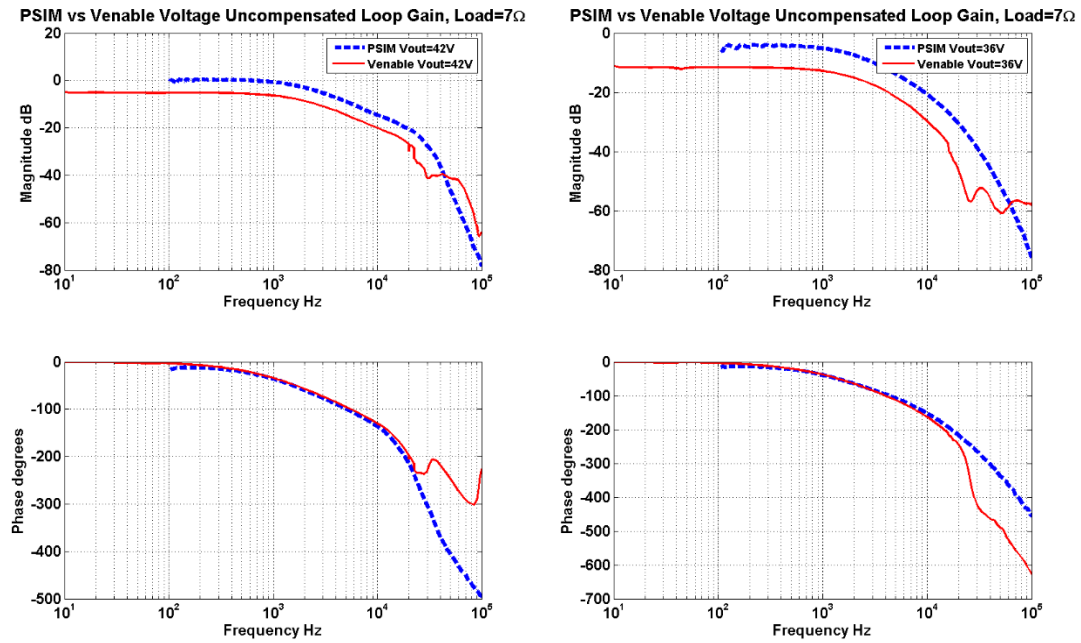
Figure 4.19 - Uncompensated voltage loop gain, Vout=42V & 36V, Load=7Ω (PSIM vs Venable)
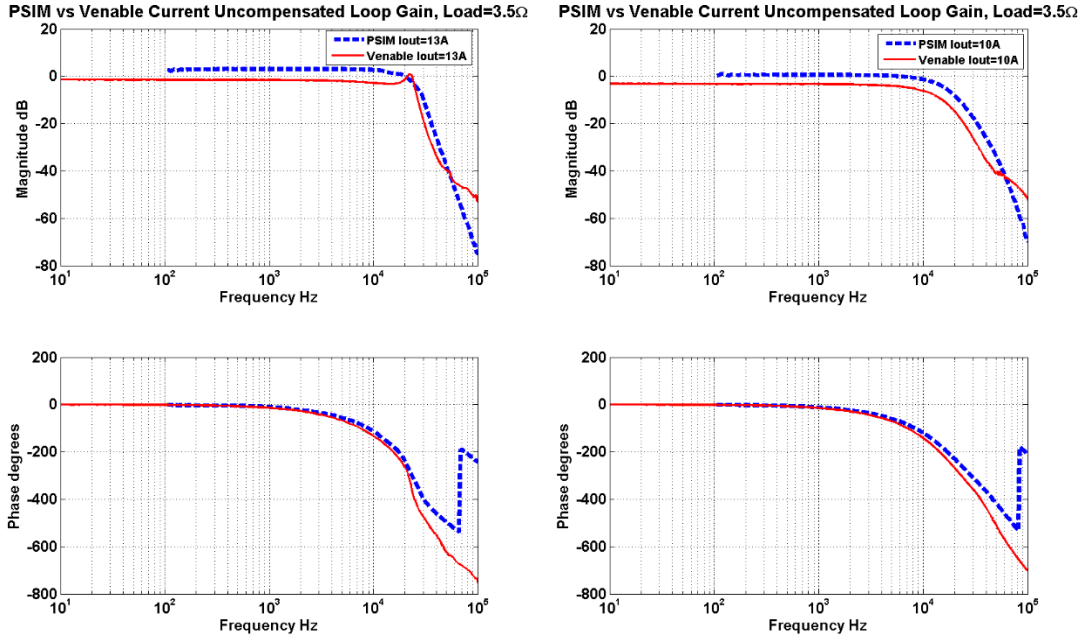
Figure 4.20 - Uncompensated current loop gain, Iout=13A & 10A, Load=3.5Ω (PSIM vs Venable)
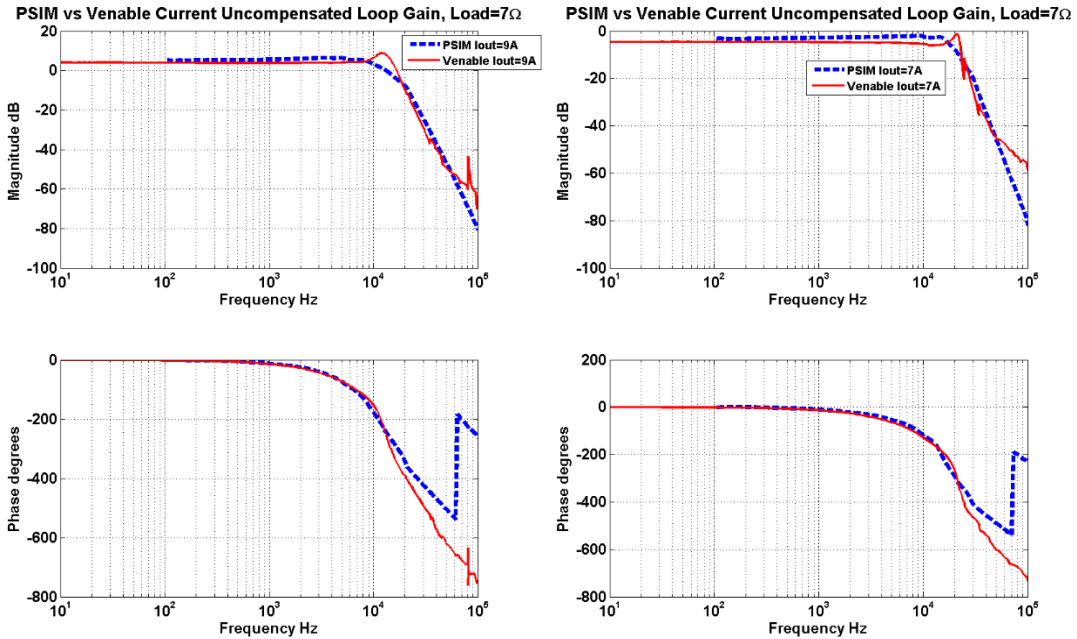
Figure 4.21 - Uncompensated current loop gain, Iout=9A & 7A, Load=7Ω (PSIM vs Venable)

The PSIM simulation results produced fairly accurate results under 10kHz when compared to the Venable results. The shapes of the frequency response curves are very similar. However, just like the plant frequency response comparison (Figure 4.13-Figure 4.16), the difference in magnitude (or gain) becomes more significant as the output voltage (Vout) decreases (which

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corresponds to increasing switching frequency). As the output voltage (Vout) is set lower, the magnitude difference between PSIM and Venable increases. The cause may be that at higher frequencies, the non-idealities of the resonant tank components (the inductor and capacitor) become more profound, which results in reduced gains. PSIM does not show this reduced gain because the components in the circuit model are very basic and idealized (the PSIM models are shown in Appendix B: PSIM Simulation Schematics).

4.3 MATLAB System Identification Process

The frequency response data collected in Section 4.2 is saved as a *.dat* file and imported to MATLAB's workspace environment to be used by the System Identification Toolbox. This software tool is an application for constructing mathematical models of dynamic systems from measured input-output data. It allows the user to create and use models of dynamics systems not easily modeled from first principles or specifications. Time-domain and frequency-domain input-output data can be used to identify continuous-time and discrete-time transfer functions, process models, and state-space models [47].

The Venable frequency response data will be used instead of the PSIM data because it represents the most accurate model. The frequency response data collected from Venable contains an array of magnitude in dB and its corresponding phase in degrees. Each index in the array needs to be first converted into complex vectors or magnitude/phase vectors as a function of frequency. Equation 4-1 [47] shows how the conversion is done. The Venable magnitude data (in dB) needs to be converted into normal amplitude (Amp) units before the complex conversion in Equation 4-1 can be used. This can be done by using the using the MATLAB function: db2mag.

$$Complex = \ Amp \times e^{\frac{(phase^{\circ})\pi i}{180^{\circ}}}$$
<div align="right">Equation 4-1</div>

After the conversion, the new complex vector can then be stored into an *IDFRD* object. The *IDFRD* object encapsulates the frequency response data and allows the user to specify properties such as the complex response data, frequency vector, sampling interval (set sampling interval to zero for continuous time), and other more complex properties (disturbance spectra, uncertainty measures, etc). The IDFRD object is imported into the System Identification Toolbox

for transfer function estimation. Figure 4.22 shows the graphical user interface (GUI) for the system identification toolbox main workspace (left) and the importing window (right).
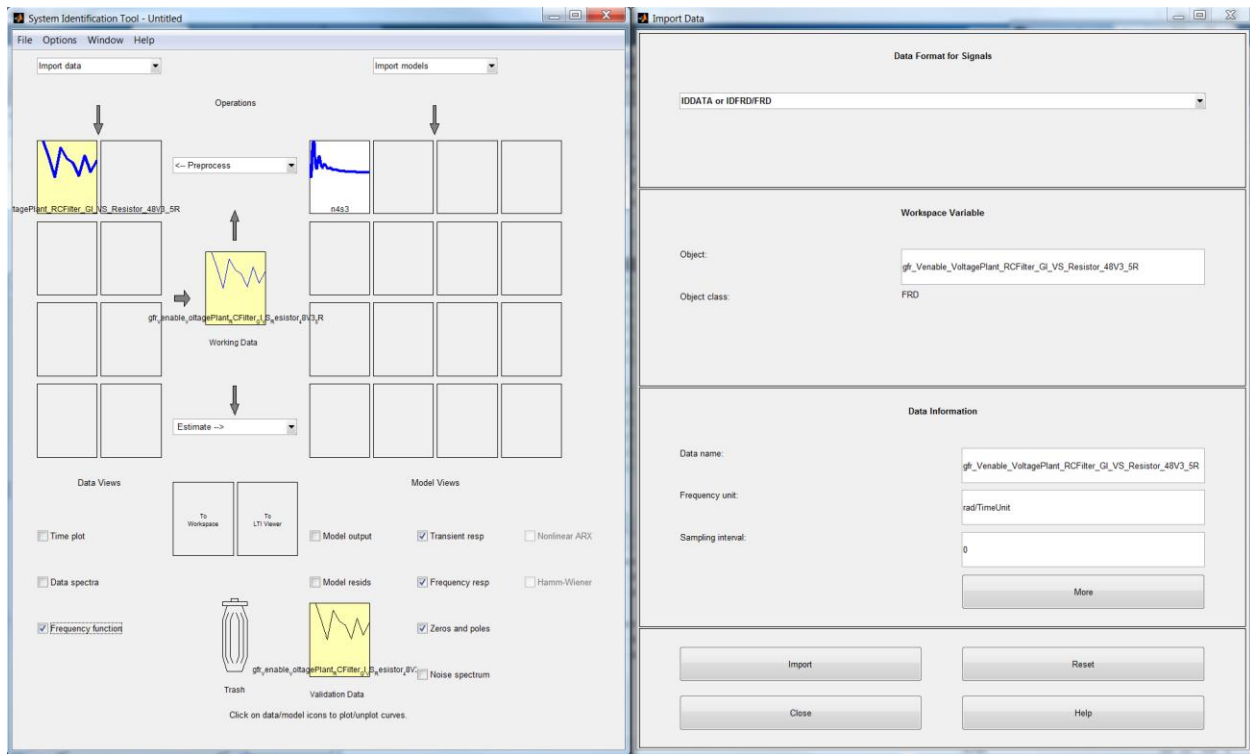
Figure 4.22 - System identification toolbox main workspace (left) & data importing window (right)

Multiple *IDFRD* models can be imported and stored into the workspace and each model can be estimated with different estimation techniques. The quality of the estimation techniques can be evaluated by comparing the estimated step-response, frequency-response, and pole-zero plots with each other. Each estimation technique correlates to a model structure such as state-space model structure, polynomial model structure, output-error model structure, etc. The state-space model is a good overall model since only the number of states needs to be specified in order to estimate a model. The output-error (OE) model is also a good choice because of their simplicity. From previous analysis in Section 2.4, it was noted that the voltage/current plant behaved like a second order system therefore a simple polynomial second order model structure might be sufficient. However, because the frequency response data being estimated contains the uncompensated loop gain (which includes a RC low-pass filter, VCO, and sensors); I found the simple second order polynomial model structure did not provide sufficient accuracy. As a result, I found the best model structure to use was the state-space structure.

Once the model structure has been decided, the model order number needs to be determined. In general, the aim should be not to use a model order higher than necessary [48]. This can be determined by analyzing the improvement in percentage fit as a function of model order. Figure 4.23 shows the model estimation GUI (left) and the model order selection window (right). The model estimation GUI was selected to a state-space structure with order number 1-10 to be evaluated in the order selection window. The domain was set to continuous time since the uncompensated loop gain data collected came from analog components. In the order election window, it can be seen by increasing the model order number (x-axis) the log of sigma values (y-axis) becomes less. It is desirable to have a lower log of sigma value, which represents a more accurate model. However, it is undesirable to use a very high order number. If the order is higher than necessary, then the extra parameters are used to model the measurement noise. Therefore, the extra poles and zeroes are estimated with a lower level of accuracy. Ultimately, I found an order number of 3 to 5 provided me with the best accuracy.
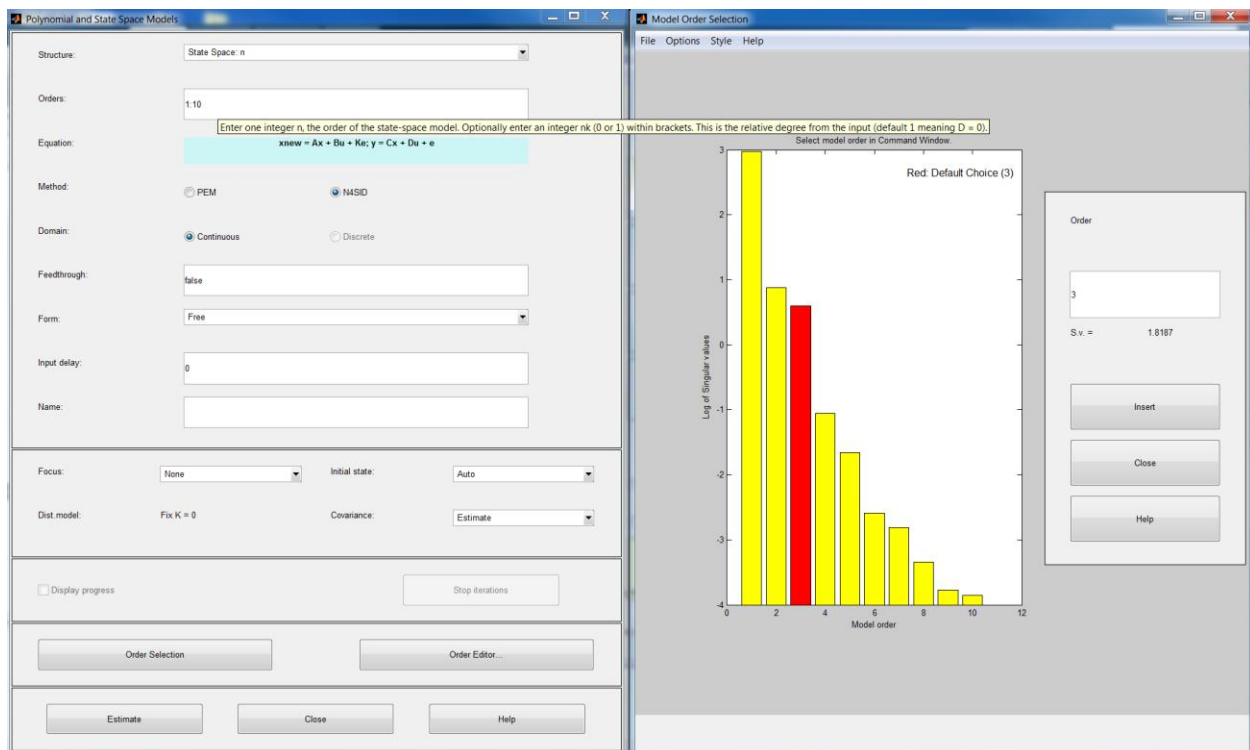
Figure 4.23 - System identification toolbox model estimation structure GUI (right) & model order selection (left)

Figure 4.24-Figure 4.27 shows several uncompensated loop-gain frequency response comparison plots along with their percentage fit between the estimated model (light grey line) and the actual Venable data (blue line) for different operating points. Results show the accuracy

of the state-space estimation model is very good. The percentage fit ranges from 92% to 99%. More importantly, the estimation model matches almost exactly with the Venable data at frequency below 20kHz which is well above the control bandwidth I am trying to achieve. These results show the validity of using the system identification estimation method to model the converter.

**Venable Frequency Response Data vs System Identification Estimation
Uncompensated VOLTAGE Loop Gain with Load=3.5Ω**
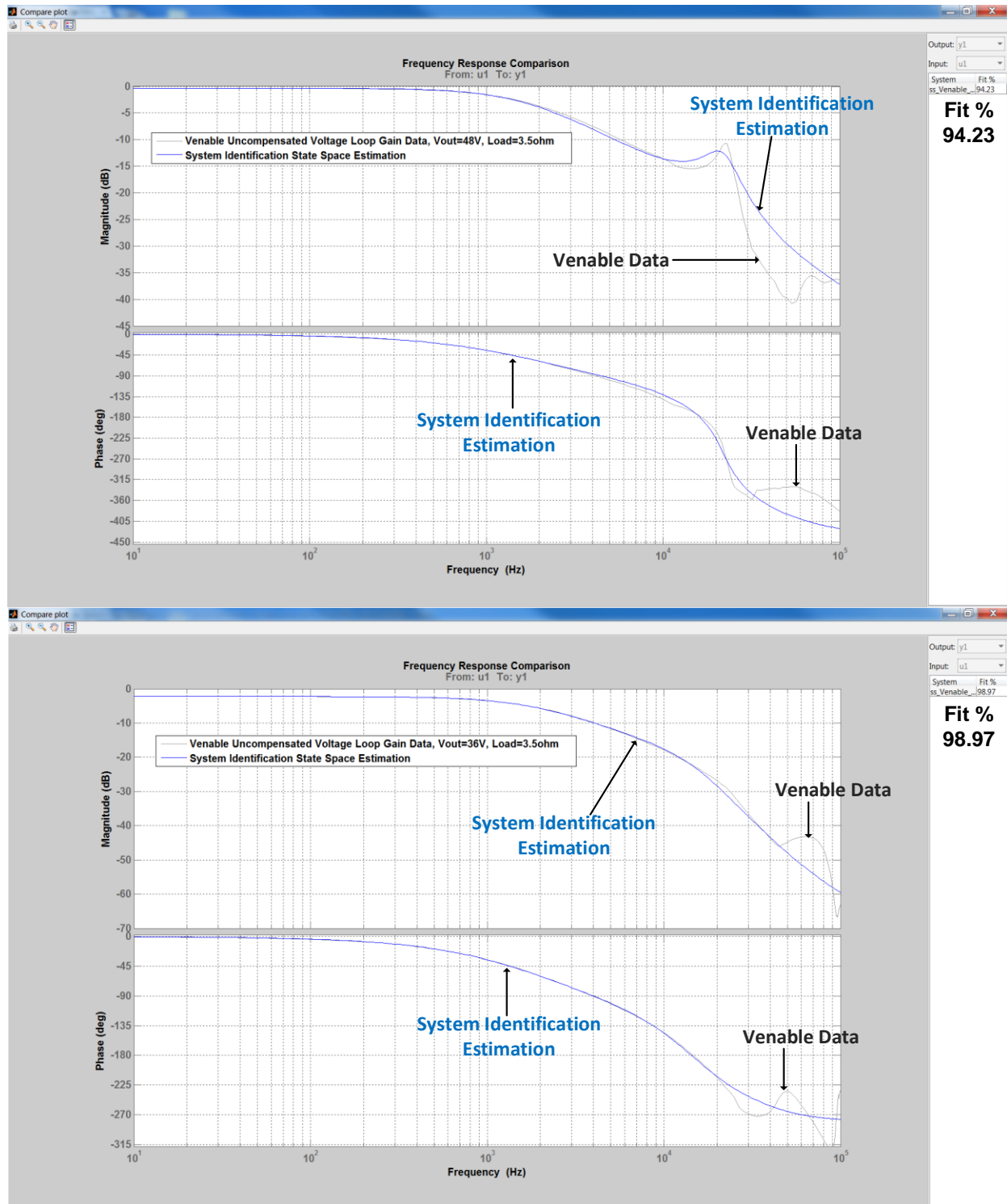
Figure 4.24 - Uncompensated voltage loop gain, Venable data vs State-space estimation, Load=3.5Ω

**Venable Frequency Response Data vs System Identification Estimation
Uncompensated VOLTAGE Loop Gain with Load=7Ω**
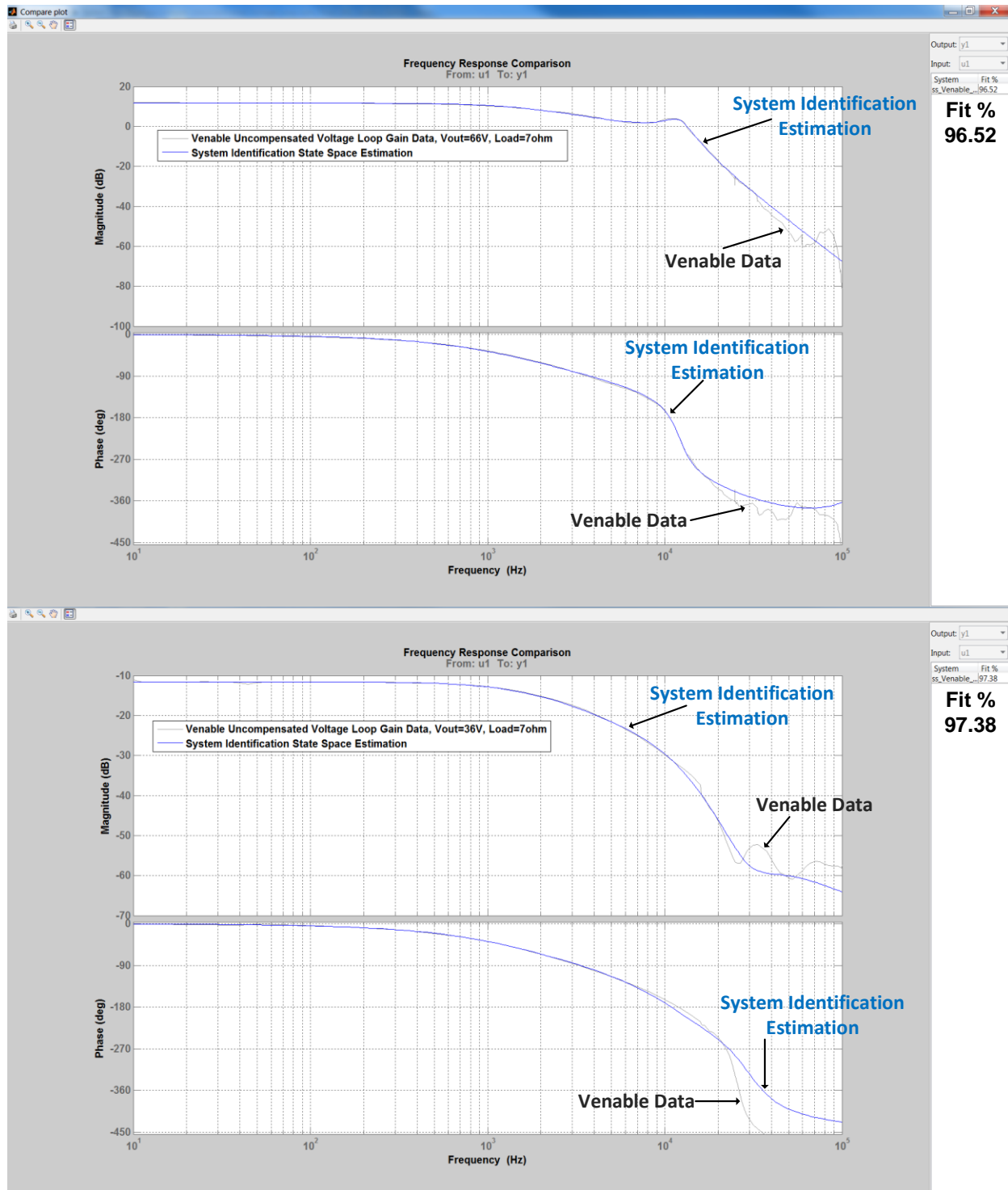
Figure 4.25 - Uncompensated voltage loop gain, Venable data vs State-space estimation, Load=7Ω

**Venable Frequency Response Data vs System Identification Estimation
Uncompensated CURRENT Loop Gain with Load=3.5Ω**
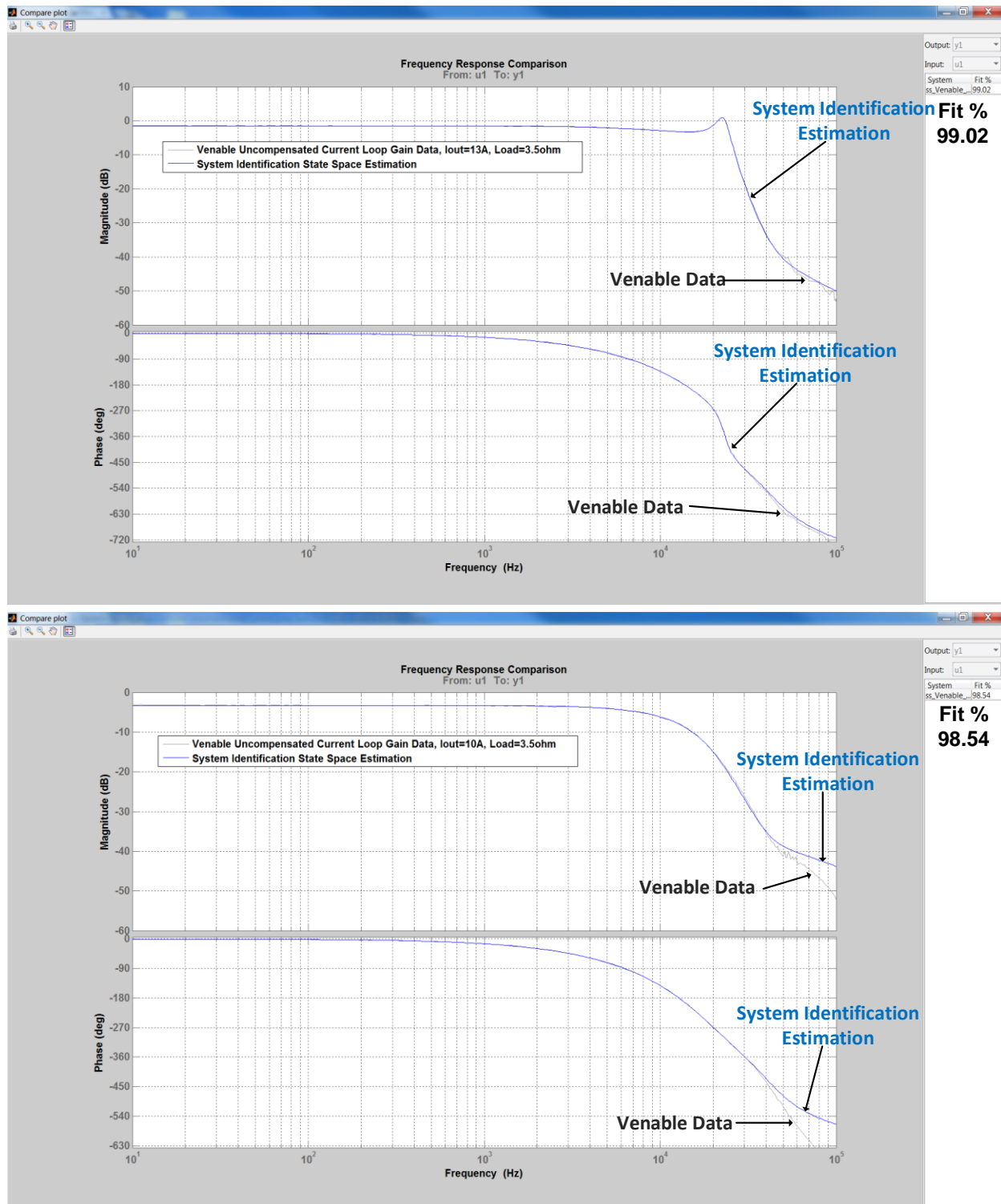
Figure 4.26 - Uncompensated current loop gain, Venable data vs State-space estimation, Load=3.5Ω

Venable Frequency Response Data vs System Identification Estimation
Uncompensated CURRENT Loop Gain with Load=7Ω
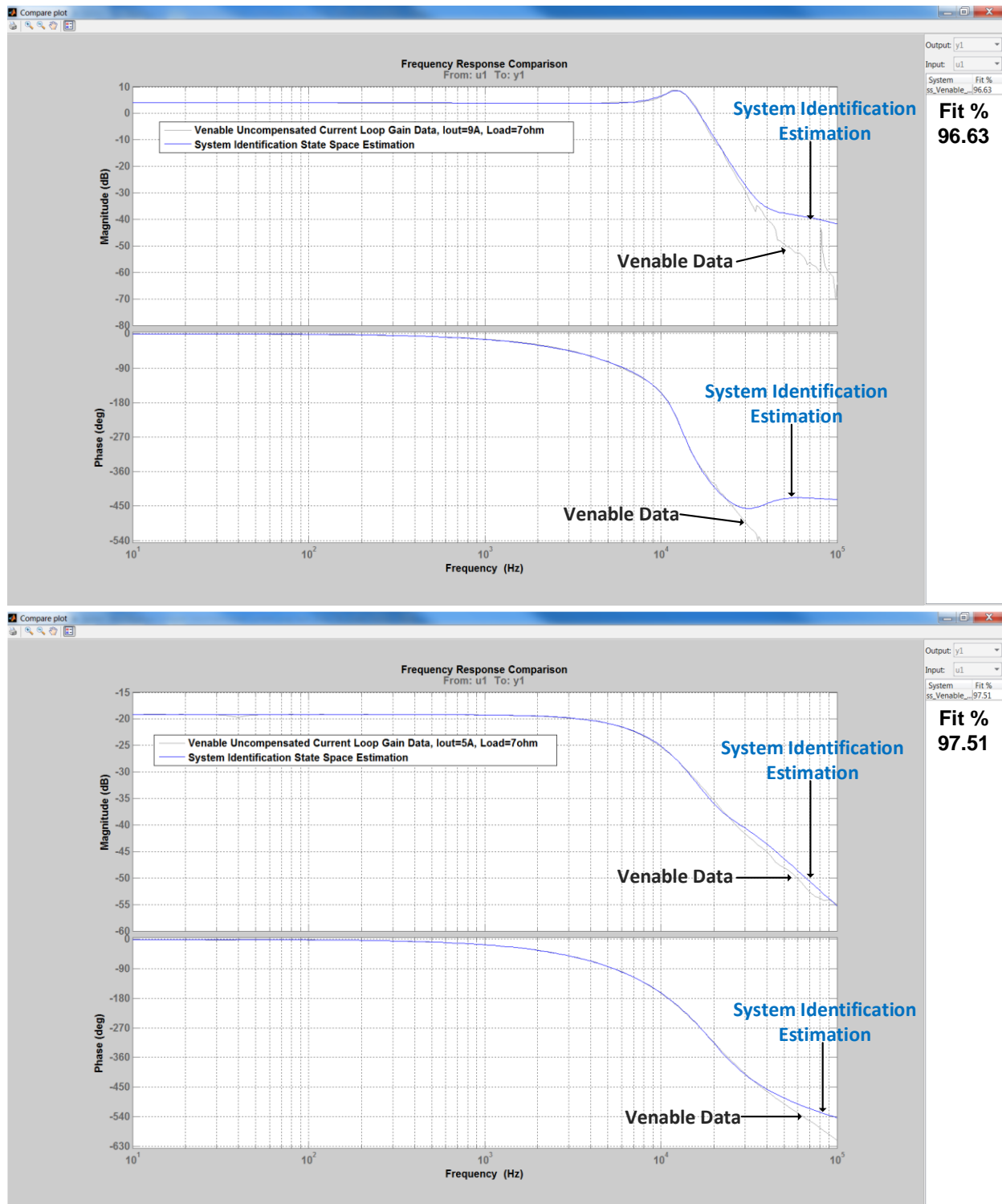
Figure 4.27 - Uncompensated current loop gain, Venable data vs State-space estimation, Load=7Ω

4.4 Compensator Design & Performance Results

4.4.1 MATLAB SISO Toolbox
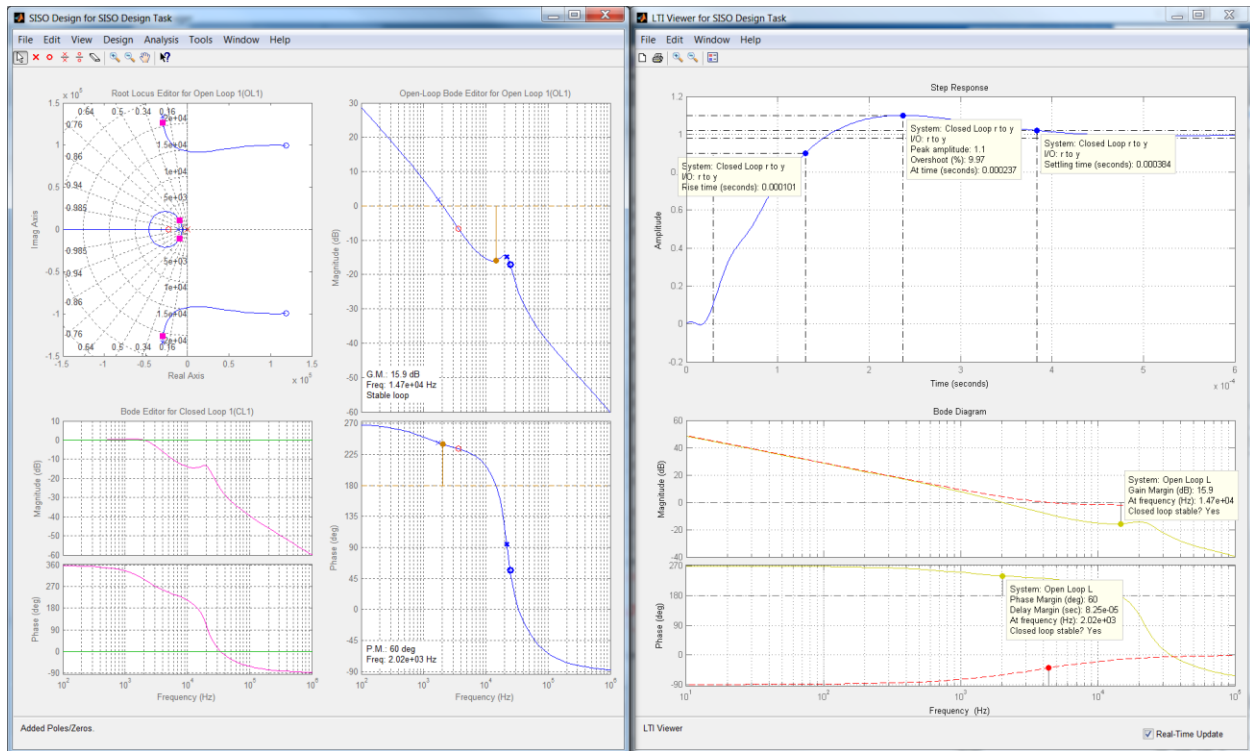
Figure 4.28 - MATLAB SISO Tool Design GUI

The System Identification estimation model is imported into MATLAB's SISO Design Toolbox for compensator design. The SISO Design Tool is a graphical user interface (GUI) used to design compensators [49]. It has a graphical tuning window which allow the user to display and manipulate the bode, root locus, and Nichols plot. Poles and zeroes can be added and manipulated dynamically to the system in order to see its effects. Figure 4.28 shows the SISO tool used to design a compensator for a specific operating point. The window on the left in Figure 4.28 is where the gain, poles, and zeroes of the compensator can be added/manipulated and its effects can be seen in the nyquist, loop gain, and closed loop response plots. The window on the right in Figure 4.28 shows additional analysis such as step response, impulse response, bode, nyquist, and pole/zero to further expand analysis. In this case I choose to focus on the step response, the bode plot of compensated loop gain and compensator. The right window can also show the performance results of the compensated system such the rise time, overshoot, settling time, phase margin, and gain margin.

4.4.2 Compensator Design

At a high level, there are three main fundamental goals for compensation: stability, reference tracking, and disturbance rejection. The LLC converter by itself is open loop stable but the open loop reference tracking and disturbance rejection ability is poor [20], [24], [50]. It is well known that adding a feedback loop can cause an otherwise stable system to become unstable [20]. In closed loop form, it becomes difficult to stabilize when trying to improve reference tracking and disturbance rejection. Therefore, the compensation goal is to improve the reference tracking ability and its disturbance rejection ability while maintaining the LLC converter's inherent stability. The ability of how well a system can perform reference tracking and disturbance rejection is related to the system bandwidth [24], [51]. However, the bandwidth is not the only measurement to consider for disturbance rejection. Another disturbance rejection requirement is the 120Hz noise from the rectified AC line. A large magnitude for the compensated loop-gain at 120Hz means better AC line disturbance rejection. I chose to aim for around 20dB or greater at 120Hz which would provide rejection by a factor of 10 (20log(10)=20dB). The stability margins I chose to maintain and their definitions are shown in Table 4.1.

Symbol	Value	Description
φ_m	$\geq 60°$	**Phase Margin**: The amount of phase change necessary to make the system unstable when the gain is exactly equal to 0dB.
g_m	$\geq 10dB$	**Gain Margin**: The amount of gain change necessary to make the system unstable when the phase is equal to -180° or 0°.

Table 4.1 - Compensation stability objectives

The following describes how a compensator was designed for the LLC resonant converter operating at a particular point. The procedure was similarly done for all the other operating points. When designing the compensator, the first added is an integrator in order to eliminate the DC error. After that, the gain is adjusted and then poles/zeroes are added in order to achieve the best bandwidth and disturbance rejection while satisfying the stability objectives listed in Table

4.1. Compensators were based on the PI and PID controller structure. The transfer functions of the PI and PID controller are shown in Equation 4-2 and Equation 4-3 respectively where G_0 is the DC gain.

$$PI = G_0 \left(\frac{\left(1 + \frac{s}{\omega_z}\right)}{s} \right)$$

Equation 4-2

$$PID = G_0 \left(\frac{1}{s} \frac{(1 + \frac{s}{\omega_{z1}})(1 + \frac{s}{\omega_{z2}})}{(1 + \frac{s}{\omega_p})} \right)$$

Equation 4-3

Both controller types are sufficient to achieve the stability objectives with PI working better for some operating conditions while PID doing a better job for other operating conditions. Figure 4.29 shows the bode plot of the uncompensated loop gain, the PID compensator, and the PID compensated loop gain for a LLC converter in voltage control mode operating at Vout=48V and Load=3.5Ω. As shown in Figure 4.29, a maximum crossover frequency (fc) of fc=3.7kHz is achieved while maintaining a minimum gain margin of 10dB and phase margin of 60°. Note that the crossover frequency is also related to the closed loop bandwidth of the system therefore the higher the fc, the higher the closed loop bandwidth. The magnitude at 120Hz is 28.7dB, which should reject disturbances at that frequency by a factor of 27.
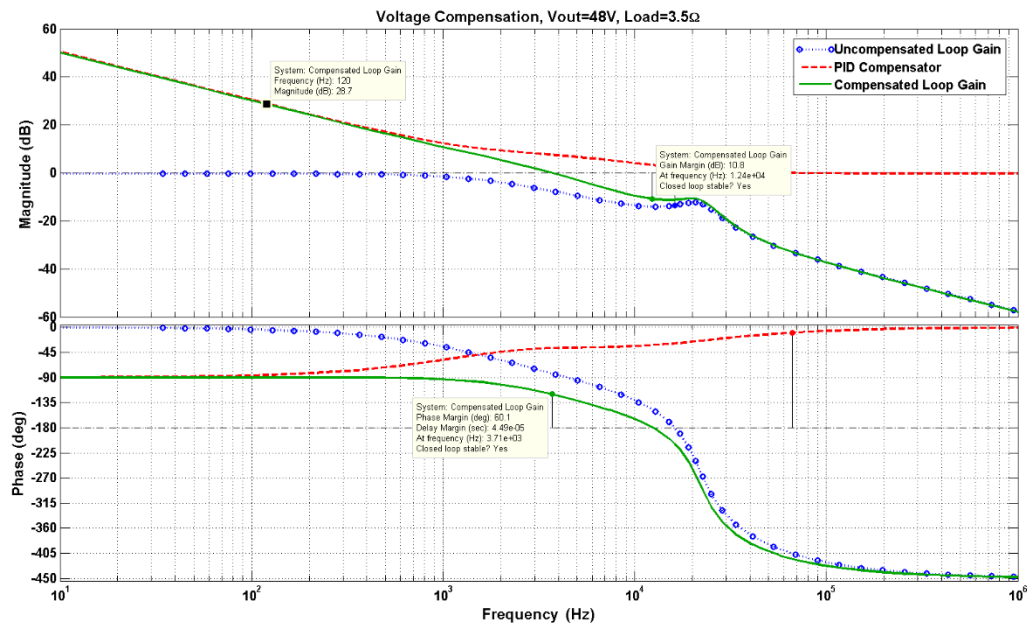
Figure 4.29 - Frequency response of: uncompensated loop gain, compensator, compensated loop gain

Figure 4.30 shows the bode plot of the compensated loop gain T(s), the sensitivity function 1/(1+ T(s)), and the complementary sensitivity function (T(s)/(1+ T(s))). The sensitivity function represents the closed loop system's ability to reject disturbances and the complementary sensitivity function represents the closed loop system's reference tracking ability. The design requirement for the maximum peak of sensitivity (M_s) is $M_s < 2$(6dB).
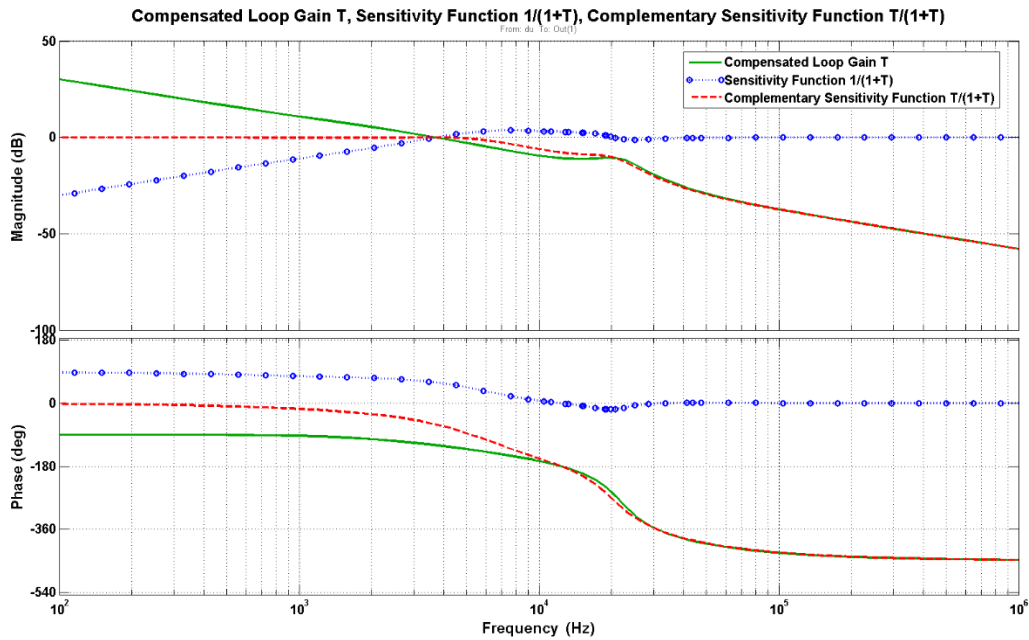
Figure 4.30 - Frequency response of: compensated loop gain, sensitivity function, complementary sensitivity function

Figure 4.31 shows the closed loop reference step response. The rise time is 4.59e-05s, the overshoot is 5.07%, the settling time is 0.256ms, and the final value is one meaning no steady state error. The percentage overshoot can be easily reduced by increasing the compensated loop gain's phase margin. However doing so would reduce the crossover frequency (or bandwidth) which translates to a longer settling time. For this project, it was decided that the system's bandwidth is more important as long as the overshoot percentage is below 10%.
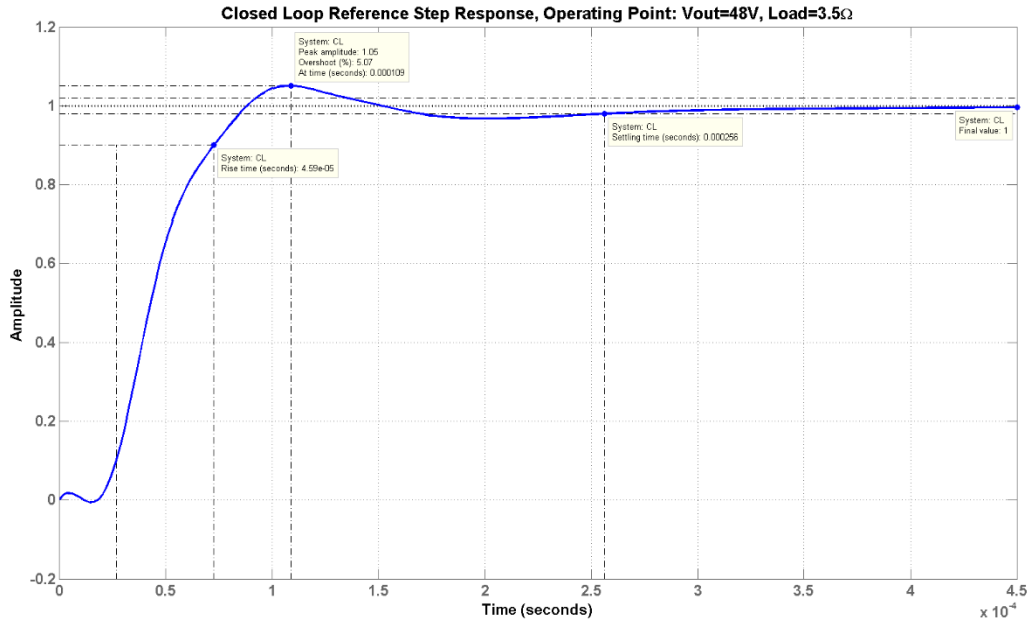
Figure 4.31 - Closed-loop reference step response

The PID compensator equation used for the above plots is shown in Equation 4-4.

$$PID\ Compensator$$

$$= 21144 \frac{(1 + 9.6 \times 10^{-5}s)(1 + 0.00012s)}{s(1 + 2.5 \times 10^{-5}s)}$$

Equation 4-4

$$\approx 21144 \frac{(1 + \frac{1}{2\pi(16579)}s)(1 + \frac{1}{2\pi(1326)}s)}{s(1 + \frac{1}{2\pi(6366)}s)}$$

As mentioned before, the $\frac{1}{s}$ term is to eliminate the DC error. The two zeroes located at 1326Hz and 16579Hz help reduce the negative phase shift. Adding a pole at 6366Hz helps maintain the gain margin while maximizing the bandwidth.

Discrete-time Compensator:

The compensator designed using the SISO toolbox is in continuous-time domain and needs to be converted to discrete-time format in order to be used in a digital device. The Tustin or bilinear transformation shown in Equation 4-5 [52] is the method used to transform the continuous-time controller to its discrete-time

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$$s = \frac{2}{T_s}\frac{z-1}{z+1}$$

Equation 4-5

where s represents the continuous-time complex number and z represents the discrete-time. The DSC has a sampling rate of 400kHz therefore the sampling period T_s is equal to 1/400kHz. The bilinear transformation yields the best frequency-domain match between the continuous-time and discretized systems and often yields a better match in the frequency domain than the zero-order-hold (ZOH) method [53], [54]. Equation 4-6 shows the discrete-time transformation of the continuous-time PID transfer function from Equation 4-4.

$$PID(z) = \frac{1.06z^2 - 1.853z + 0.7987}{z^2 - 1.905z + 0.9048}$$

Equation 4-6

In digital signal processing (DSP), it is desirable to write the discrete transfer function as a rational expression of z^{-1} and to order the numerator and denominator terms in ascending power of z^{-1} as shown in Equation 4-7 [52], [55]. This is because it is easier to program such equation in software.

$$PID(z^{-1}) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

Equation 4-7

Converting Equation 4-8 into the DSP form result in the following:

$$PID(z^{-1})$$

$$= \frac{1.06 - 1.853z^{-1} + 0.7989z^{-2}}{1 - 1.905z^{-1} + 0.9048z^{-2}}$$

Equation 4-8

Figure 4.32 compares the continuous time controller with its discrete time equivalent.
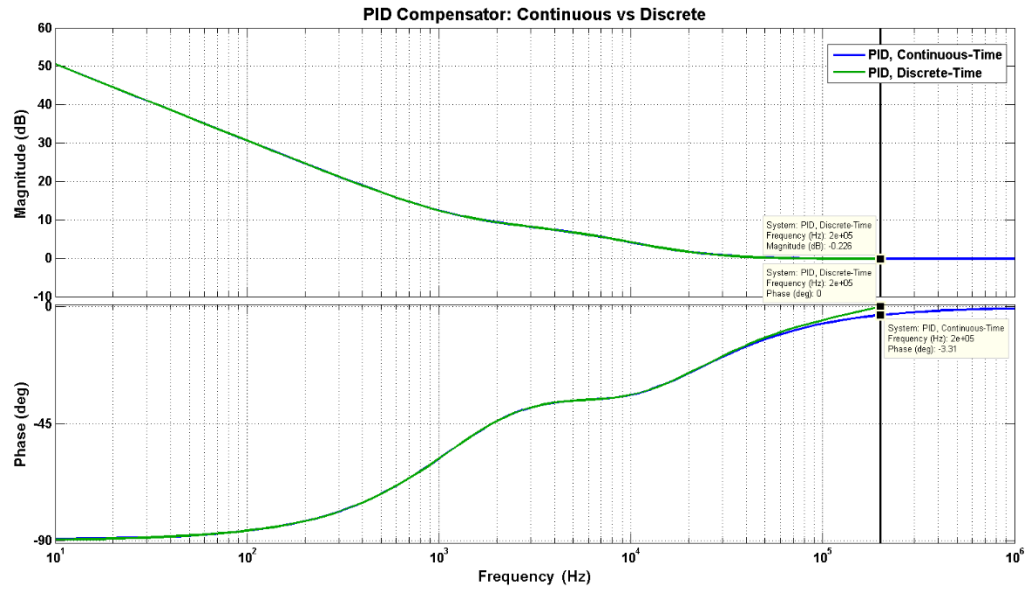
Figure 4.32 - Continuous vs discrete compensator

The maximum unique frequency is limited by the sampling theorem. Notice that the response of the discrete time compensator exhibits increasing phase lag as it approaches the Nyquist frequency (400kHz/2=200kHz). This is due to sample-to-output delay and the effects of reconstruction [55]. The phase lag will increase considerably at frequencies higher than Nyquist frequency. Because I am controlling the closed loop system at frequencies much lower than the Nyquist frequency, the phase lag effect is not a major concern.

4.4.3 Compensator and Performance Results

Table 4.2 shows the optimized compensator designs for several different operating modes/conditions. The table shows the compensator designs for voltage control mode and current control mode. The continuous-time and its discrete-time equivalent of the compensators are also presented.

Optimized Compensator Designs				
Control Mode	**Operating Mode**		**Transfer Function**	
	V or I	**Load**	**Continuous**	**Discrete**
Voltage	48V	3.5Ω	$17244\dfrac{(1 + 4.3 \times 10^{-5}s)}{s}$	$\dfrac{0.7415 - 0.6984z^{-1}}{1 - z^{-1}}$
	42V	3.5Ω	$26292\dfrac{(1 + 5.6 \times 10^{-5}s)}{s}$	$\dfrac{1.472 - 1.407z^{-1}}{1 - z^{-1}}$
	36V	3.5Ω	$34382\dfrac{(1 + 6.0 \times 10^{-5}s)}{s}$	$\dfrac{2.063 - 1.977z^{-1}}{1 - z^{-1}}$
	66V	*7Ω*	$2860.5\dfrac{(1 + 3.8 \times 10^{-5}s)}{s}$	$\dfrac{0.1087 - 0.1015z^{-1}}{1 - z^{-1}}$
	60V	7Ω	$4822\dfrac{(1 + 3.8 \times 10^{-5}s)}{s}$	$\dfrac{0.1832 - 0.1712z^{-1}}{1 - z^{-1}}$
	54V	7Ω	$4302\dfrac{(1 + 3.1 \times 10^{-5}s)}{s}$	$\dfrac{0.1334 - 0.1226z^{-1}}{1 - z^{-1}}$
	48V	7Ω	$12379\dfrac{(1 + 4.1 \times 10^{-5}s)}{s}$	$\dfrac{0.5075 - 0.4766z^{-1}}{1 - z^{-1}}$
	42V	7Ω	$33124\dfrac{(1 + 4.2 \times 10^{-5}s)}{s}$	$\dfrac{1.391 - 1.308z^{-1}}{1 - z^{-1}}$
	36V	7Ω	$84688\dfrac{(1 + 7.7 \times 10^{-5}s)}{s}$	$\dfrac{6.521 - 6.309z^{-1}}{1 - z^{-1}}$
Current	13A	3.5Ω	$16189\dfrac{(1 + 1.7 \times 10^{-8}s)}{s}$	$\dfrac{0.0002752 + 0.0402z^{-1}}{1 - z^{-1}}$
	12A	3.5Ω	$17244\dfrac{1}{s}$	$\dfrac{0.03935z^{-1}}{1 - z^{-1}}$
	11A	3.5Ω	$27429\dfrac{(1 + 1.5 \times 10^{-5}s)}{s}$	$\dfrac{0.4114 - 0.3429z^{-1}}{1 - z^{-1}}$
	10A	3.5Ω	$31078\dfrac{(1 + 1.6 \times 10^{-5}s)}{s}$	$\dfrac{0.4972 - 0.4196z^{-1}}{1 - z^{-1}}$
	9A	*7Ω*	$7101\dfrac{1}{s}$	$\dfrac{0.01775z^{-1}}{1 - z^{-1}}$
	8A	7Ω	$11196\dfrac{1}{s}$	$\dfrac{0.02799z^{-1}}{1 - z^{-1}}$
	7A	7Ω	$24032\dfrac{1}{s}$	$\dfrac{0.06008z^{-1}}{1 - z^{-1}}$
	6A	7Ω	$93776\dfrac{(1 + 1.5 \times 10^{-5}s)}{s}$	$\dfrac{1.407 - 1.172z^{-1}}{1 - z^{-1}}$
	5A	7Ω	$172630\dfrac{(1 + 1.9 \times 10^{-8}s)}{s}$	$\dfrac{0.00328 + 0.4283z^{-1}}{1 - z^{-1}}$

Table 4.2 - Optimized adaptive compensator designs using MATLAB SISO for continuous time and converted into discrete-time using bilinear transformation with a sampling period of $T_s=1/400kHz$

Single Compensation:

In order to show the advantages of using an optimized adaptive compensator for each operating point, a single digital compensator design was used to compensate for all operating conditions, which is how a traditional/classical analog system would be implemented. The single compensator designed aims to achieve a minimum of 60º phase margin and 10dB gain margin

under all operating conditions. To achieve the stability margins for all the operating conditions, the compensator was designed for the worst-case uncompensated loop gain, which corresponds to the uncompensated loop gain with the highest gain. Table 4.2 highlights the worst case operating condition in red (one for voltage control mode and one for current control mode). The worst case operating condition for voltage mode control is Vout=66V and Load=7Ω and the worst case operating condition for current mode control is Iout=9A and Load=7Ω. Their corresponding optimized compensators were used for the single compensator design. By using the compensator design for the worst-case operating condition, it ensures the rest of the operating conditions meet the minimum stability criteria.

Figure 4.33 (voltage control mode) and Figure 4.34 (current control mode) shows the compensated loop gains of several different operating conditions being compensated by the single compensation method. Take note of the large overall loop gain variation, which translates to a large variation in loop-gain crossover frequency of approximately 10:1 ratio. This results in an inconsistence in control-to-output frequency response characteristic and transient behavior between different operating conditions.
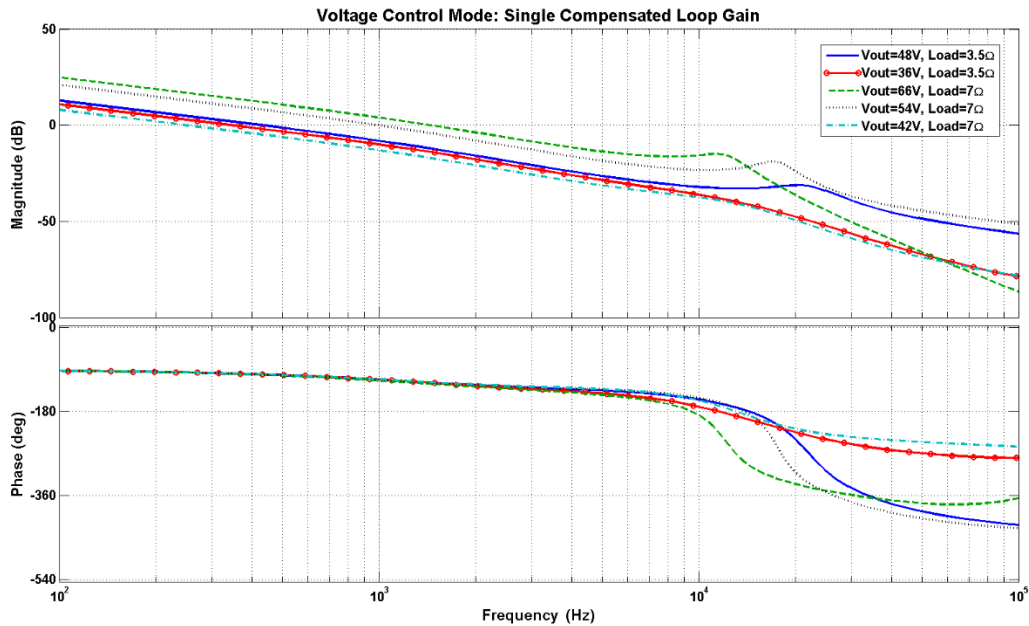
Figure 4.33 - Single compensation control voltage loop gain (Simulated)
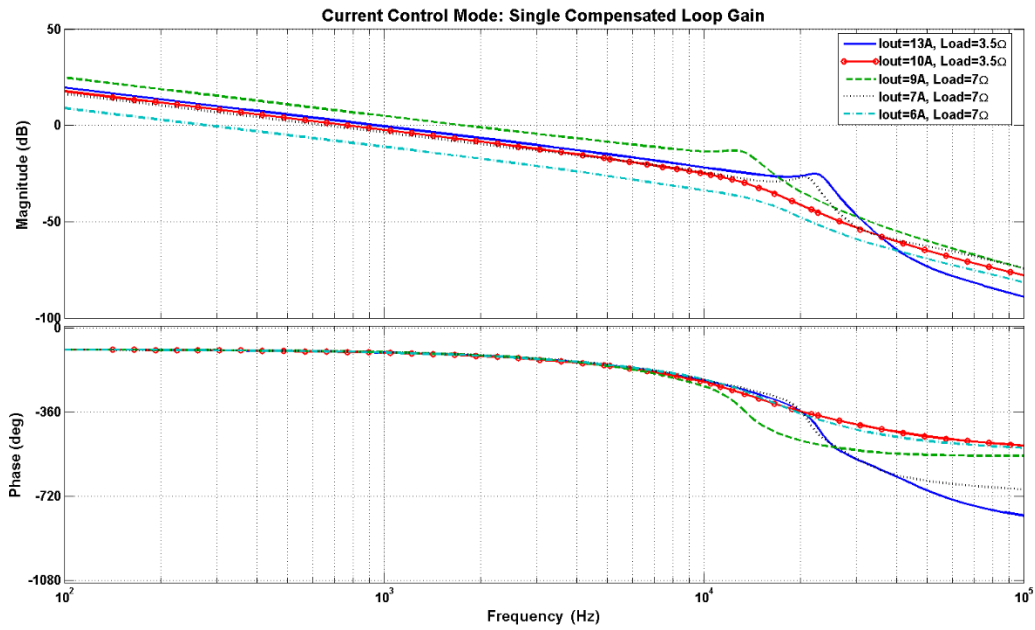
Figure 4.34 - Single compensation control current loop gain (Simulated)

Figure 4.35 and Figure 4.36 shows the corresponding step response and their settling times for various operating conditions and are summarized in Table 4.3.
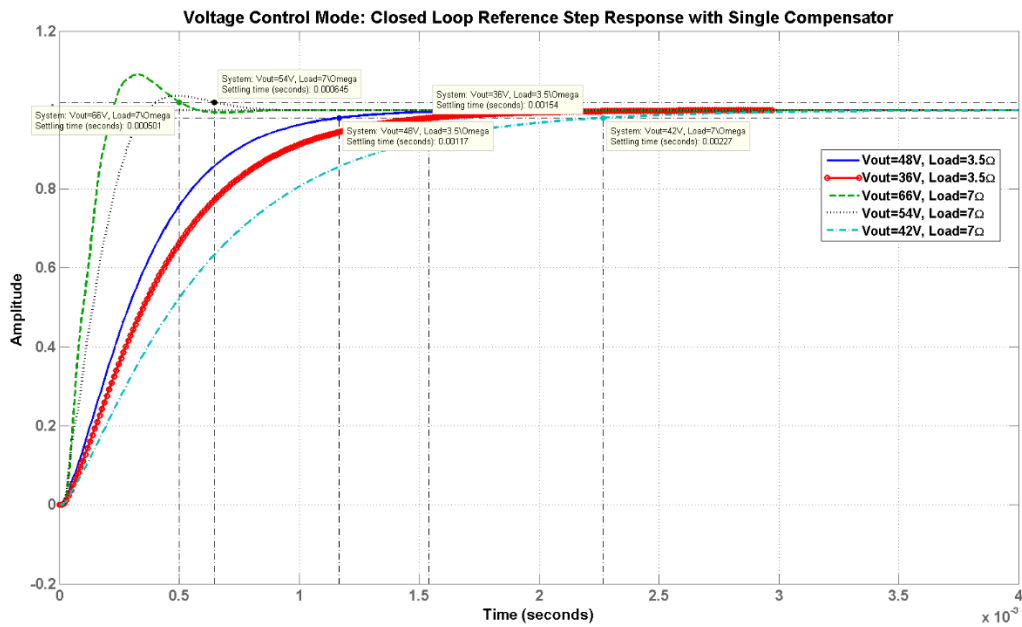
Figure 4.35 - Closed loop (Voltage Mode Control) reference step response with single compensator (Simulated)
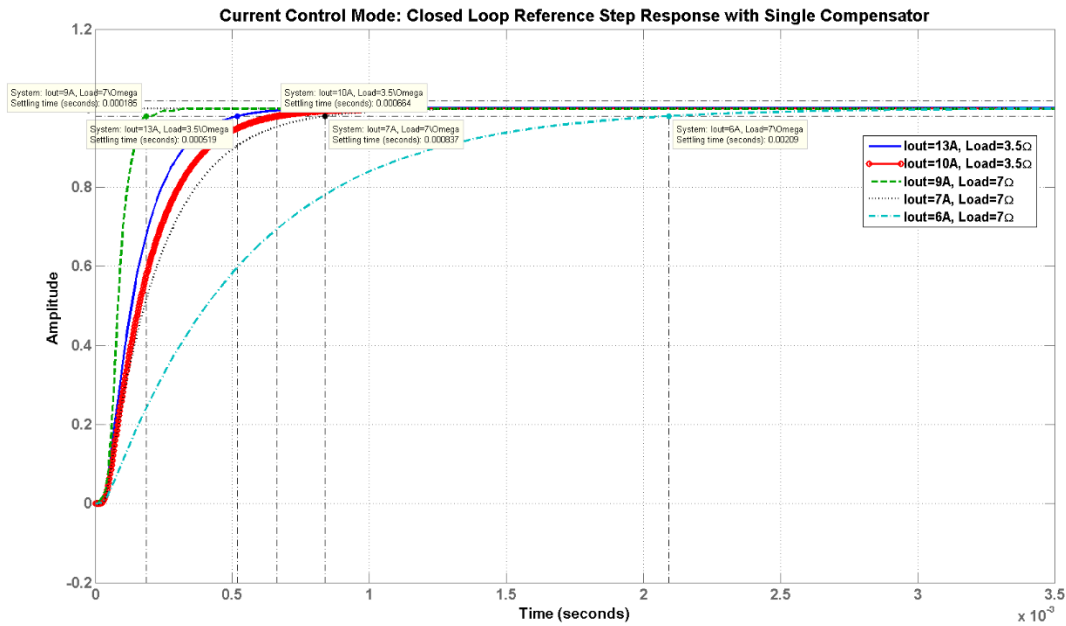
Figure 4.36 - Closed loop (Current Mode Control) reference step response with single compensator (Simulated)

Adaptive Compensation:

Figure 4.37 (voltage control mode) and Figure 4.38 (current control mode) shows the compensated loop gains of several different operating conditions being adaptively compensated. The overall loop gain variation is much less when compared to the single compensator case. Furthermore, the overall loop-gain crossover frequency is much higher.
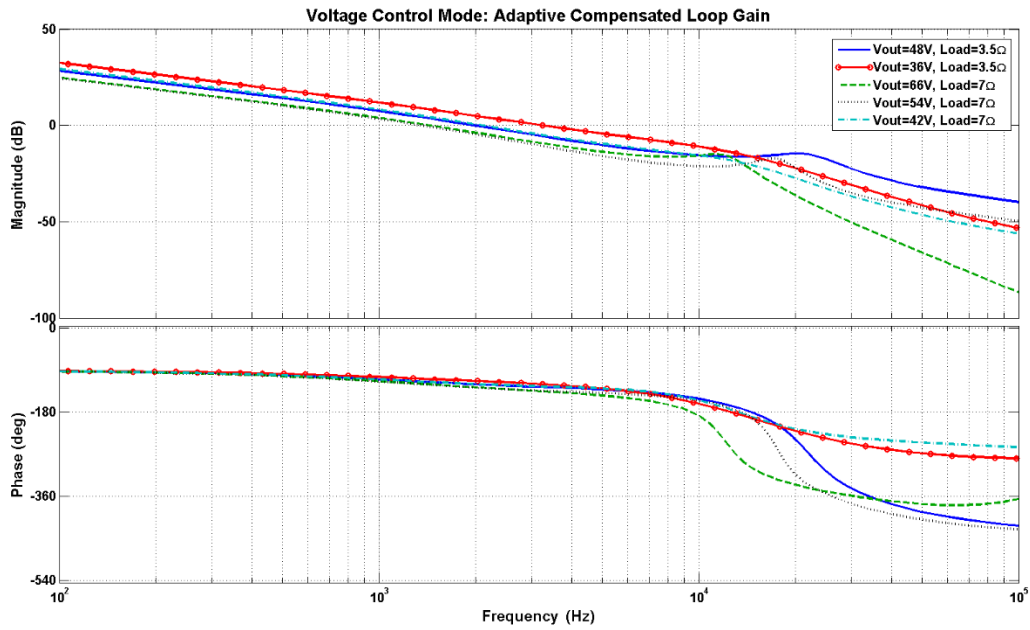
Figure 4.37 - Adaptive compensation control voltage loop gain (Simulated)
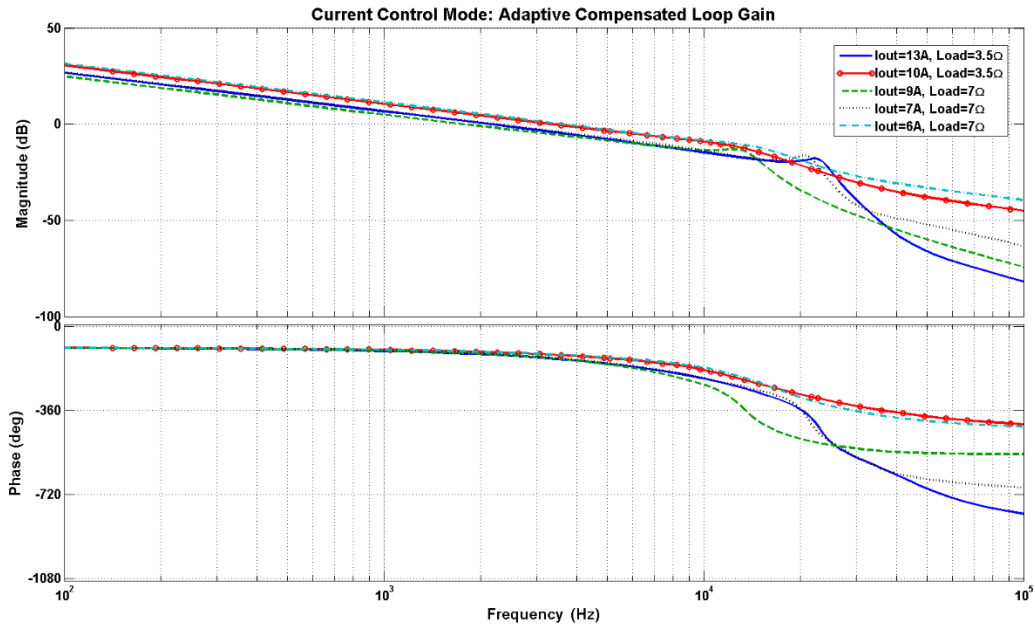
Figure 4.38 - Adaptive compensation control current loop gain (Simulated)

Figure 4.39 and Figure 4.40 shows the corresponding step response and their settling times for various operating conditions, which are also summarized in Table 4.3. The settling times are shorter by around a factor of 10, which corresponds to the adaptively compensated loop gain plots in Figure 4.37 and Figure 4.38.
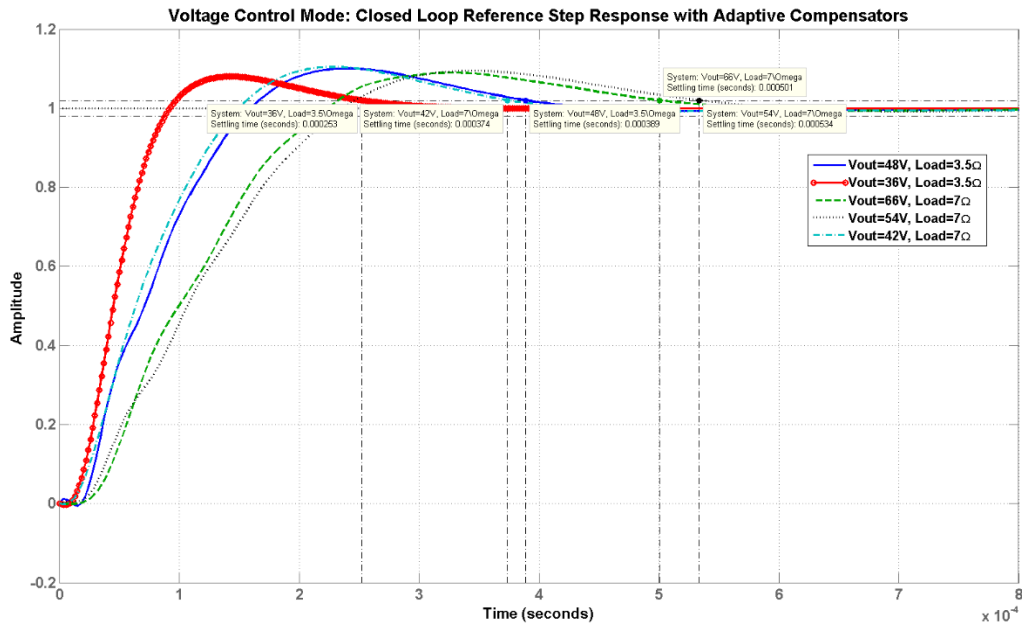
Figure 4.39 - Closed loop (Voltage Mode Control) reference step response with adaptive compensator (Simulated)
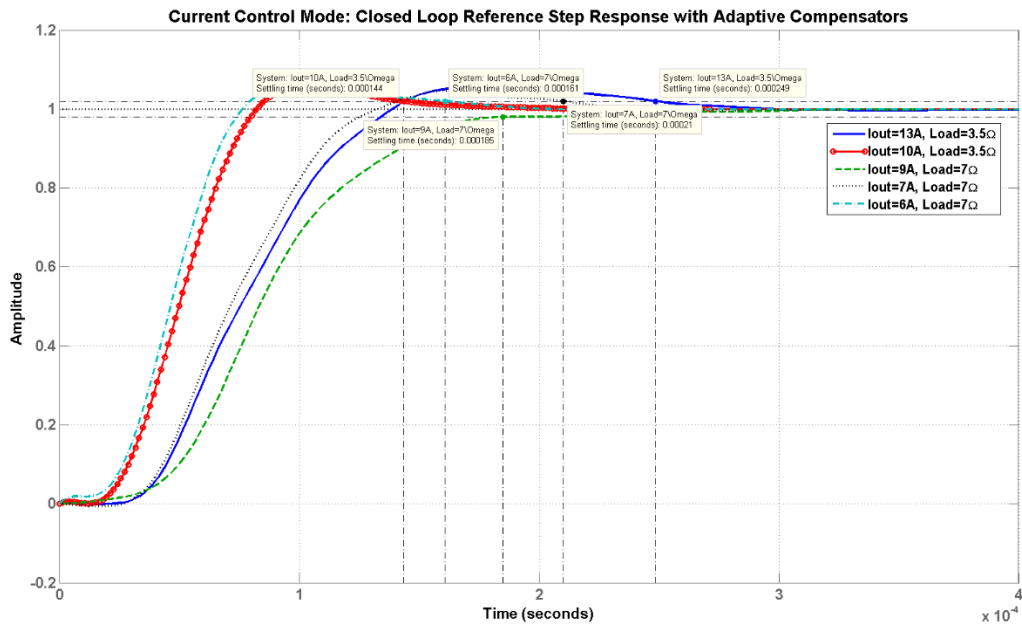
Figure 4.40 - Closed loop (Current Mode Control) reference step response with adaptive compensator (Simulated)

Performance Results:

 Note that the following results are simulated in MATLAB but the compensators were designed based on the estimated uncompensated loop gain data taken from the physical converter using Venable. Table 4.3 shows a comparison of the settling times between the single

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compensator design and the adaptive compensator design. As can be seen, the adaptive compensator design provides faster settling times. Note that two settling times between single compensator and adaptive compensation are the same for the operating points Vout=66V, Load=7Ω (in voltage mode control) and Iout=9A, Load=7Ω (in current mode control). This is because the single compensator design was based on the optimized compensator designs for the worst-case operating points which are Vout=66V, Load=7Ω (in voltage mode control) and Iout=9A, Load=7Ω (in current mode control) as was shown in Table 4.2. Therefore, the single compensator case and the adaptive compensation case uses the same compensator design for the Vout=66V, Load=7Ω and Iout=9A, Load=7Ω operating conditions hence results in having the same settling times.

Step Response Settling Times for Single Compensator vs Adaptive Compensator Design (MATLAB)				
Control Mode	Operating Point		Settling Time (µs)	
	V or I	Load	Single Compensation	Adaptive Compensation
Voltage	48V	3.5Ω	1170	389
	36V	3.5Ω	1540	253
	66V	7Ω	501	501
	54V	7Ω	645	534
	42V	7Ω	2270	374
Current	13A	3.5Ω	519	249
	10A	3.5Ω	664	144
	9A	7Ω	185	185
	7A	7Ω	837	210
	6A	7Ω	2090	161

Table 4.3 - Step Response Settling Times for Single Compensator vs Adaptive Compensator Design (Simulated)

Table 4.4 and Table 4.5 presents the compensated loop-gain performance results for the single compensation and adaptive compensation control respectively. The performance is evaluated by the stability margins, the gain at 120Hz, and the loop gain cross over frequency (fc). As discussed previously the gain at 120Hz is important for rejecting the AC line frequency disturbance and fc relates to the systems bandwidth.

Single Compensator Performance Results (MATLAB)						
Control Mode	**Operating Point**		**Stability Margins**		**Gain @ 120Hz**	**Loop Gain Cross-Over Freq (fc)**
	V or I	**Load**	**Phase**	**Gain**		
Voltage	48V	3.5Ω	79.9º	32.8dB	11.2dB	0.428kHz
	42V	3.5Ω	79.6º	36.5dB	11.7dB	0.452kHz
	36V	3.5Ω	81.8º	38.1dB	9.27dB	0.345kHz
	66V	7Ω	60º	15.9dB	23.2dB	1.44kHz
	60V	7Ω	67.2º	21.1dB	20.2dB	1.09kHz
	54V	7Ω	68.5º	21.9dB	19.3dB	0.989kHz
	48V	7Ω	79.8º	35.2dB	10.5dB	0.399kHz
	42V	7Ω	84.1º	40.7dB	6.34dB	0.248kHz
	36V	7Ω	86.8º	45.2dB	-0.07dB	0.119kHz
Current	13A	3.5Ω	76.6º	17.7dB	18dB	0.949kHz
	12A	3.5Ω	76.8º	17.1dB	18.4dB	1kHz
	11A	3.5Ω	76.2º	19.5dB	18.2dB	0.975kHz
	10A	3.5Ω	78.5º	19.8dB	16.2dB	0.772kHz
	9A	7Ω	66.6º	10.2dB	23.3dB	1.77kHz
	8A	7Ω	73.4º	13.6dB	21.1dB	1.37kHz
	7A	7Ω	81.7º	20.4dB	14.8dB	0.657kHz
	6A	7Ω	86º	29.7dB	7.38dB	0.281kHz
	5A	7Ω	87.9º	35.2dB	0.242dB	0.124kHz

Table 4.4 - Single compensator performance results (MATLAB Simulated)

Adaptive Compensation Performance Results (MATLAB)						
Control Mode	Operating Point		Stability Margins		Gain @ 120Hz	Loop Gain Cross-Over Freq (fc)
	V or I	Load	Phase	Gain		
Voltage	48V	3.5Ω	60°	16.2dB	26.8dB	1.99kHz
	42V	3.5Ω	60°	14.8dB	31dB	3.15kHz
	36V	3.5Ω	60°	14dB	30.9dB	3.24kHz
	66V	7Ω	60°	15.9dB	23.2dB	1.44kHz
	60V	7Ω	60°	16.5dB	24.8dB	1.66kHz
	54V	7Ω	60°	20.3dB	22.9dB	1.35kHz
	48V	7Ω	60°	22dB	23.3dB	1.46kHz
	42V	7Ω	60°	18.9dB	27.6dB	2.11kHz
	36V	7Ω	60°	12.6dB	29.4dB	3.09kHz
Current	13A	3.5Ω	60°	10.6dB	25.1dB	2.14kHz
	12A	3.5Ω	60.6°	10.2dB	25.3dB	2.21kHz
	11A	3.5Ω	60°	9.44dB	30dB	3.61kHz
	10A	3.5Ω	62.7°	9.89dB	27.9dB	2.95kHz
	9A	7Ω	66.6°	10.2dB	23.3dB	1.77kHz
	8A	7Ω	63.5°	9.69dB	25.1dB	2.18kHz
	7A	7Ω	61.5°	9.82dB	25dB	2.24kHz
	6A	7Ω	60°	8.7dB	29.8dB	3.61kHz
	5A	7Ω	60°	9.82dB	28dB	2.9kHz

Table 4.5 - Adaptive compensation performance results (MATLAB Simulated)

In the single compensator case, all the phase and gain margins for the operating points are above the stability criteria in Table 4.1. This results most of the operating conditions having no overshoot in the step response as was seen in Figure 4.35 and Figure 4.36. However, in most cases, the gain at 120Hz (which ranged from -0.07dB to 23.3dB) and the crossover frequency suffered significantly. The single compensation technique has difficulty maintaining a 20dB gain at 120Hz. The crossover frequency is also reduced significantly to as low as 119Hz. This translates too much slower settling times.

In the adaptive compensation case, the compensators are optimized for each individual operating point therefore resulting in the best bandwidth and 120Hz disturbance rejection. As can be seen in Table 4.5, the gains at 120Hz for each operating mode are all above 20dB. The crossover frequency ranges from 1.44kHz to 3.61kHz which is significantly better than the 119Hz to 1.77kHz single compensator case.

5 Adaptive Digital Control Software Architecture

The Texas Instruments (TI) Code Composer Studio software was used create the digital control algorithm. Code Composer Studio is an integrated development environment (IDE) that supports TI's microcontroller and their embedded processor portfolios. The IDE comprises of a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features [56]. The programming language I used to write the software code is mainly C and a small amount of assembly.
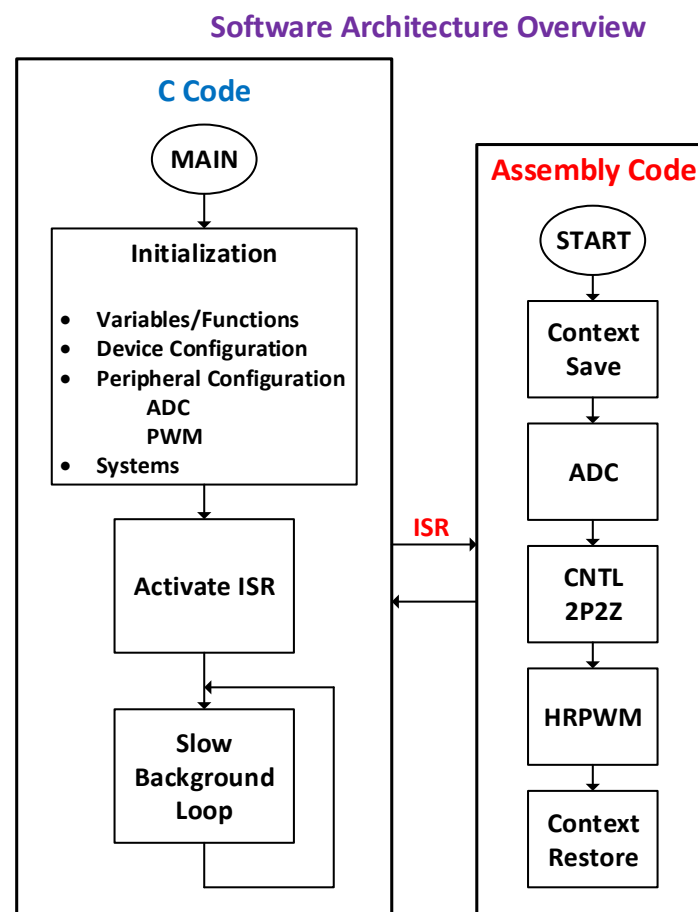
Figure 5.1 – Adaptive control software architecture overview

The general software execution procedure is illustrated in Figure 5.1. The main code is written in C and is responsible for the initialization procedure, the ISR activation, and the slow background loop (left side of Figure 5.1). As can be seen, the main code's first task is to start the initialization procedure, which is to create the necessary variables, configure the device/system, and configure the device peripherals. Configuring the device/system involves selecting the

correct clock speed of the CPU, configuring the input and output pins, enable/disable the watchdog timer, setting up and enabling the interrupt vectors, memory allocations, and much more. The main things to configure for the ADC involves setting channel number, the start of conversion (SOC) trigger, and sample window size. Configuring the PWM involves setting the target PWM module pin, the period, the mode, etc. Setting up and configuring these components correctly are crucial to ensure correct functionality of the DSC. After the initialization procedure, the interrupt service routine (ISR) is activated. The ISR is in charge of the converter's control loop and executes at 400kHz. It is executed in assembly language in order to ensure efficient and fast code execution. Finally, after the ISR is activated, the slow background loop is initialized. The slow background loop is in charge of running the adaptive compensator algorithm, which selects the most optimized compensator design to be use for a given operating point.

Background Loop:
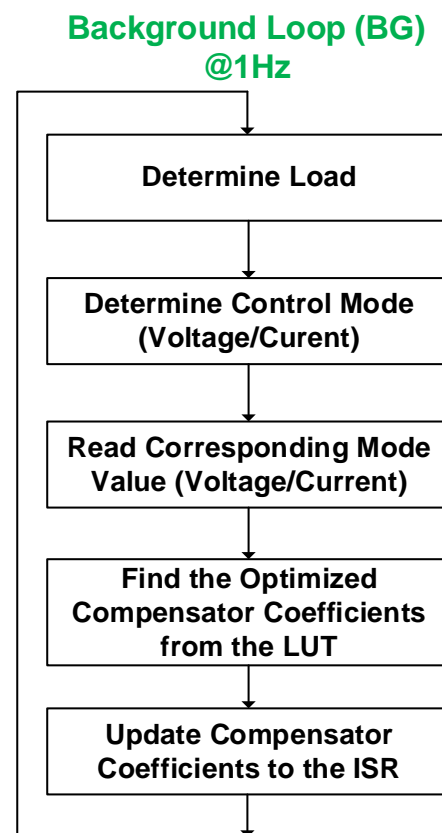
Figure 5.2 - Background loop (BG) in charge of selecting optimal compensator for a range of operating points

Figure 5.2 shows the general execution routine for the background loop. The background loop's main purpose is to update the ISR with the compensator optimally designed for a specific

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operating range. The background loop is set to loop at a slower 1Hz (may also be set to longer such as 10Hz if the plant changes very slowly) because the converter's parameters vary slowly. It also contains a look-up-table (LUT) of all the designed compensator coefficients $(b_2, b_1, b_0, a_2, a_1)$ in Table 4.2. The background loop first determines the value of the load by reading the voltage and current measurements from the ADC. The voltage and current measurements read from the ADC registers are normalized values so they need to be converted back to their original output values before the load can be determined. Once the load is calculated, the user specified control mode (voltage control mode or current control mode) is determined. If the designer set the converter to voltage mode control, the output voltage value will be used as the input to the look-up-table (LUT) and vice versa for current control mode. Based on the voltage or current value, the LUT can output and update the best-optimized compensator for a particular operating range.

Interrupt Service Routine (ISR):
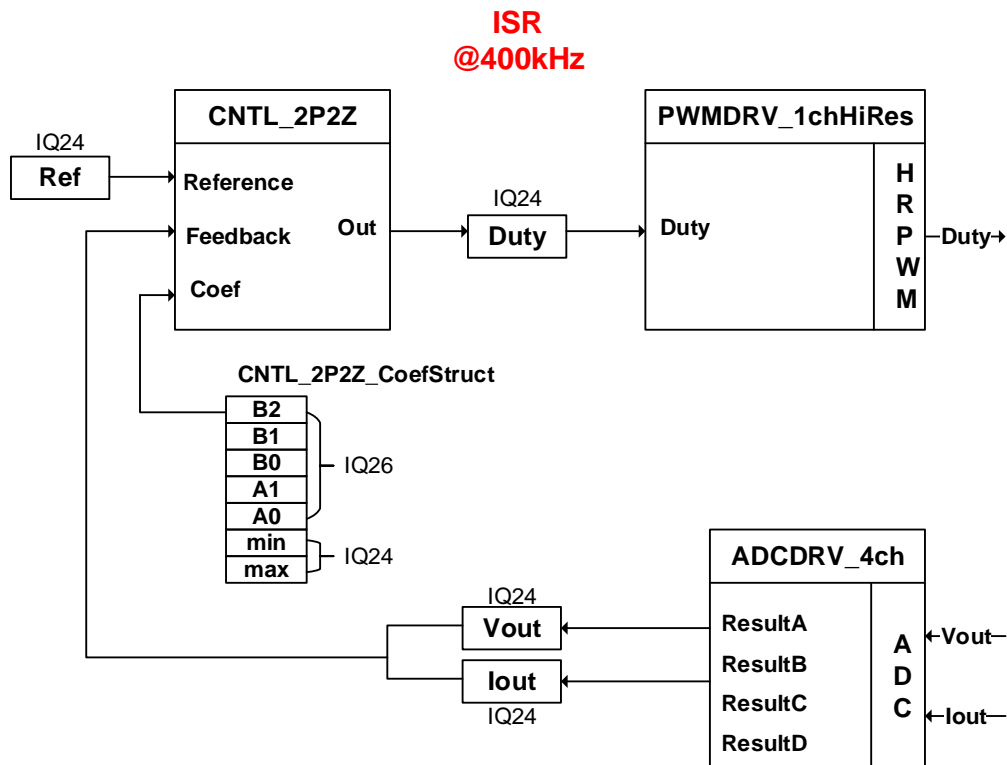
Figure 5.3 - Interrupt service routine (ISR) control loop

The interrupt service routine (ISR) executes the control loop code at a rate of 400kHz as illustrated in Figure 5.3. Texas Instruments provides the designer with a library of pre-written software function (or macro-blocks) call the Digital Power Library (DPLib). The library is

designed to enable flexible and efficient coding of digital power supply applications. The *ADCDRV_4ch* (ADC driver), *CNTL_2P2Z* (2nd order digital controller), and *PWMDRV_1chHiRes* (PWM driver) in Figure 5.3 are three macros-blocks provided by the Digital Power Library. The "Vout", "Iout", "Ref", and "Duty" correspond to software variables (which were initialized in the main code) which form the connection points, or "nodes" between the macro-blocks by the method of C pointer assignment in software. The advantage is that designs may be easily re-configured with different software configurations. The macro-blocks require initialization and the variable nodes must be connected properly before being ran in the ISR [34]. The initialization and setting up the connections were done in the main code's initialization procedure as was shown in Figure 5.1. Because digital power applications require a high control loop rate, the real-time portion of the code (normally contained within an ISR) must execute in as few cycles as possible. Therefore, the DPLib macro software blocks are written in assembly (more information regarding Texas Instruments Digital Power Library can be found in [34], [57]). The *ADCDRV_4ch* macro-block is in charge of reading the Vout and Iout results from the ADC result registers and converting them into a certain number format (IQ24) then normalizing the output to 0-1.0. The *CNTL_2P2Z* macro-block implements a second order 2-pole 2-zero IIR filter with a programmable output saturation. The "CNTL_2P2Z_CoefStruct" stores the controller's coefficients (B2,B1,B0,A2,A1) which values are updated from the background loop's look-up-table at a rate of 1Hz. The *PWMDRV_1chHiRes* is in charge of driving the high-resolution duty on the PWM output pin.

6 Experimental Validation & Results

6.1 Prototype Setup and Design

The prototyping lab bench illustrated in Figure 6.1 shows the components I used to help implement digital control on the LLC converter and gather the experimental data used to validate the digital compensator design process.
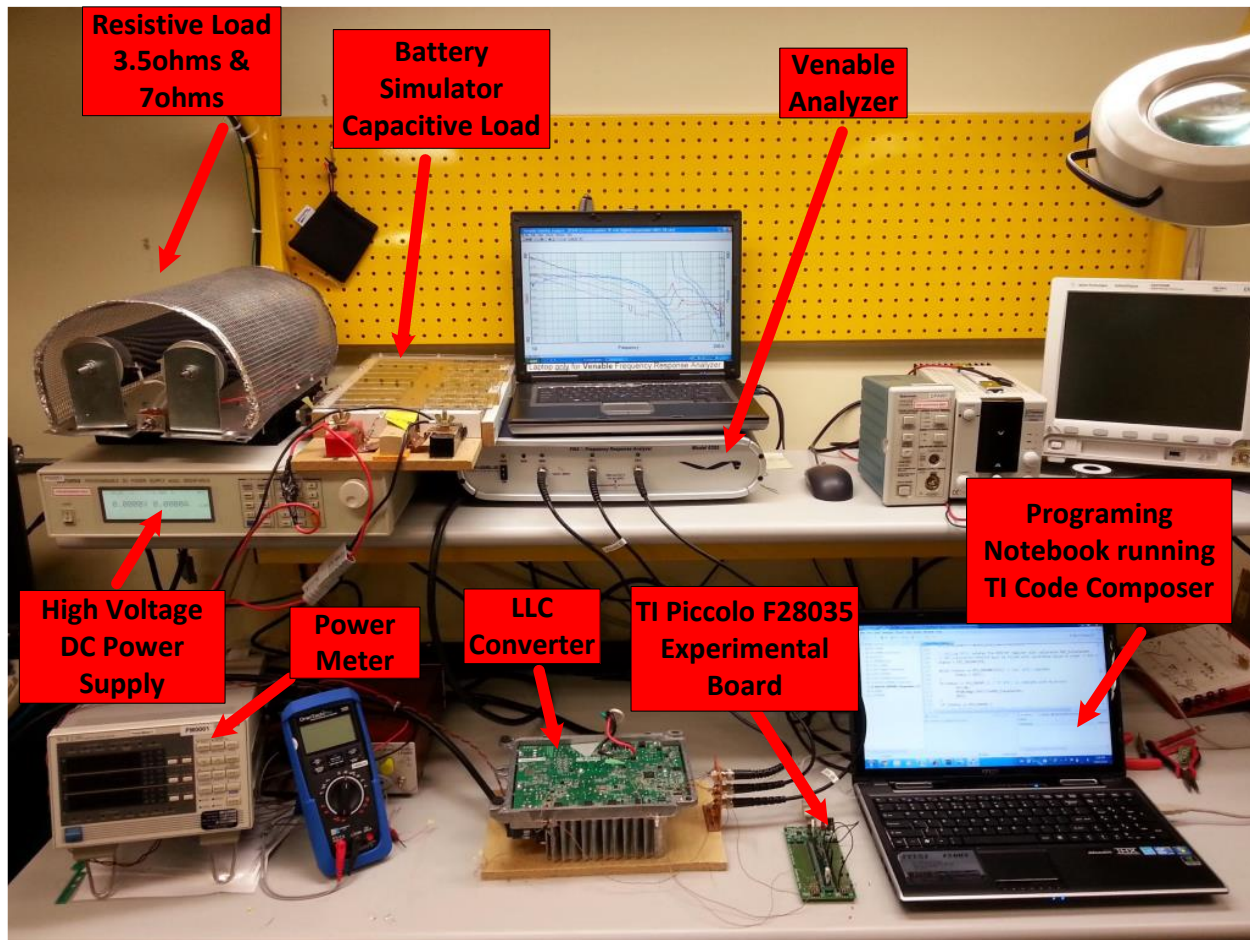
Figure 6.1 - Experimental prototype lab bench setup for digital control of LLC converter

In order to measure the digitally compensated loop-gain frequency response of the closed loop system, the LLC converter PCB had to be modified. Figure 6.2 shows an overview of how the modification for the closed loop system was implemented.
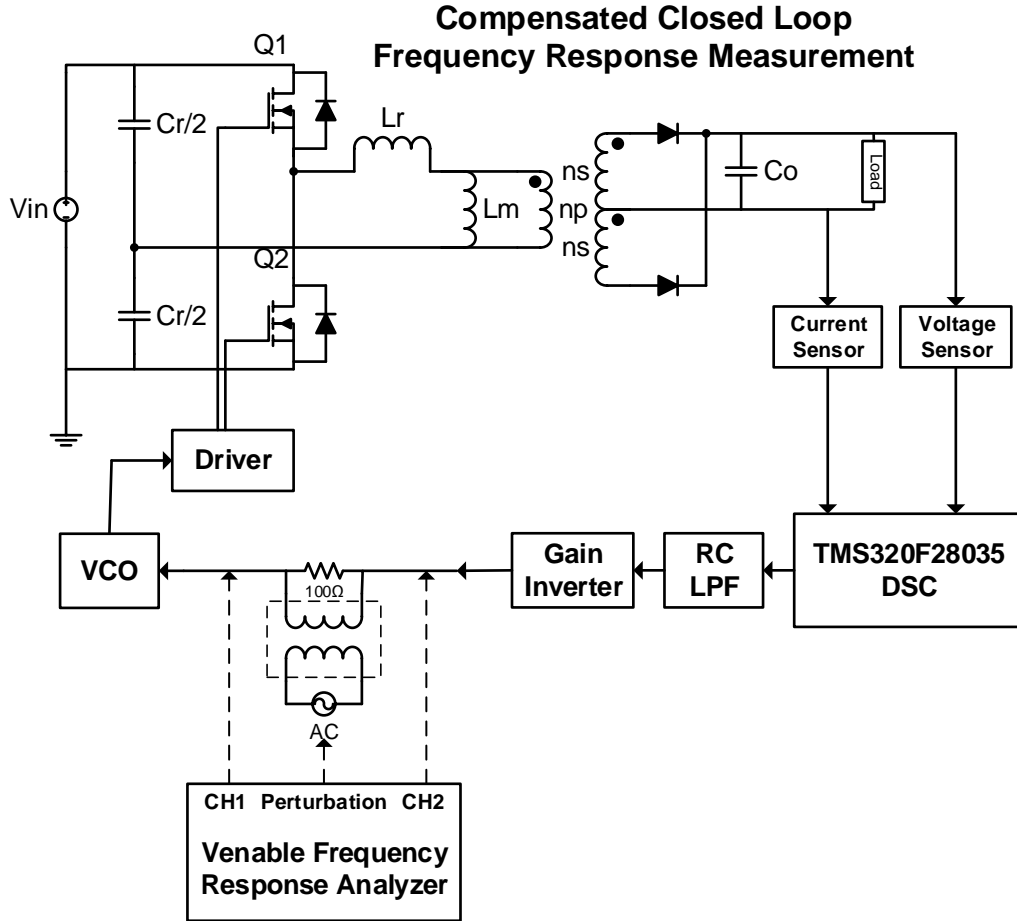
Figure 6.2 - Experimental closed loop frequency response loop gain measurement setup overview using Venable

A 100Ω resistor is added in the loop so that a perturbation AC signal can be injected along a path in the closed loop system. The injection place chosen is between the gain inverter and the VCO. Channel 1 (CH1) and Channel 2 (CH2) probes the waveforms and determines the compensated loop gain frequency response of the whole system.

6.2 Experimental Data & Performance Results

In this section, the digitally controlled experimental loop gain data collected from the prototype system (shown in Figure 6.2) is presented in Figure 6.3-Figure 6.6. The experimental loop gain data is gathered for the single compensator case and adaptive compensation case under the various operating conditions. The digital control software algorithm described in Chapter 5 is running while the loop gain data is gathered for the adaptive compensation case. Figure 6.3-Figure 6.4 shows the digitally compensated loop gains for the single compensator and adaptive compensator case in voltage control mode respectively. Figure 6.5-Figure 6.6 shows the digitally

compensated loop gains for the single compensator and adaptive compensator case in current control mode respectively.
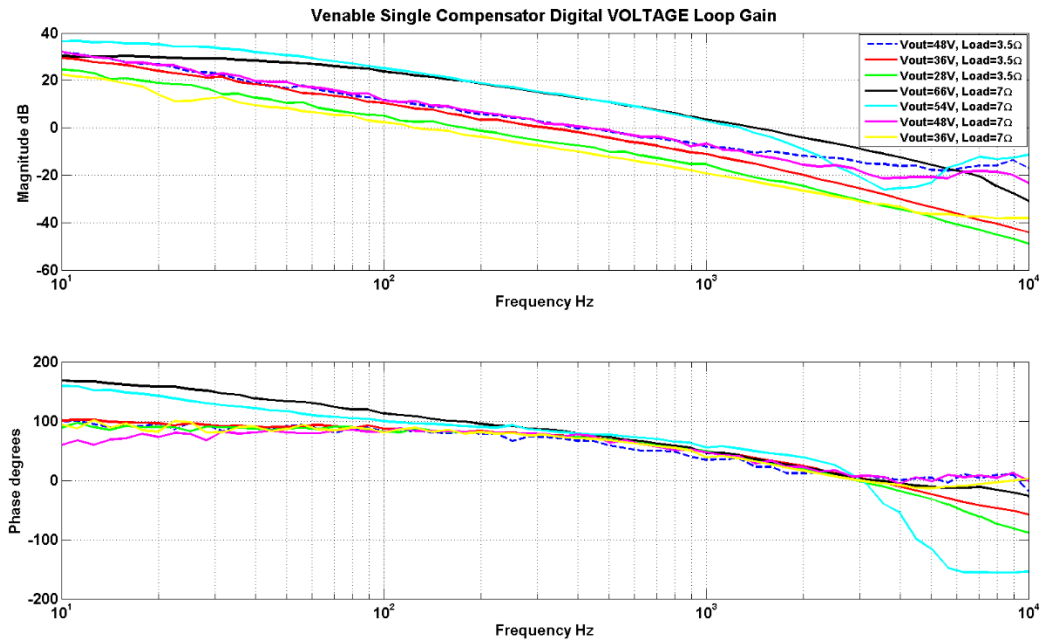
Figure 6.3 - Single compensation digital voltage loop gain (Experimental Data)
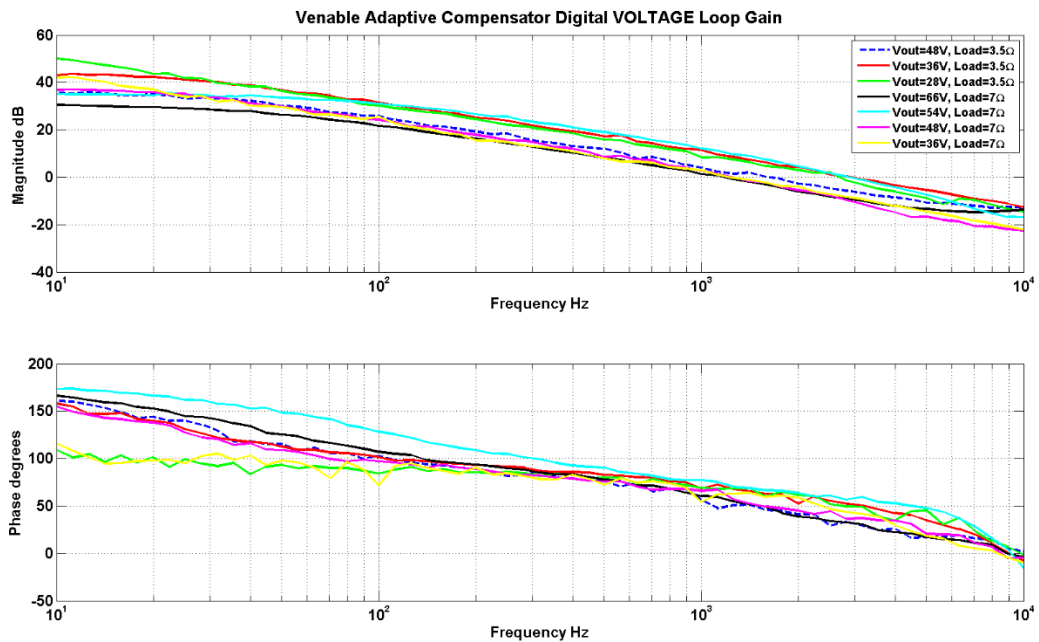
Figure 6.4 - Adaptive compensation digital voltage loop gain (Experimental Data)
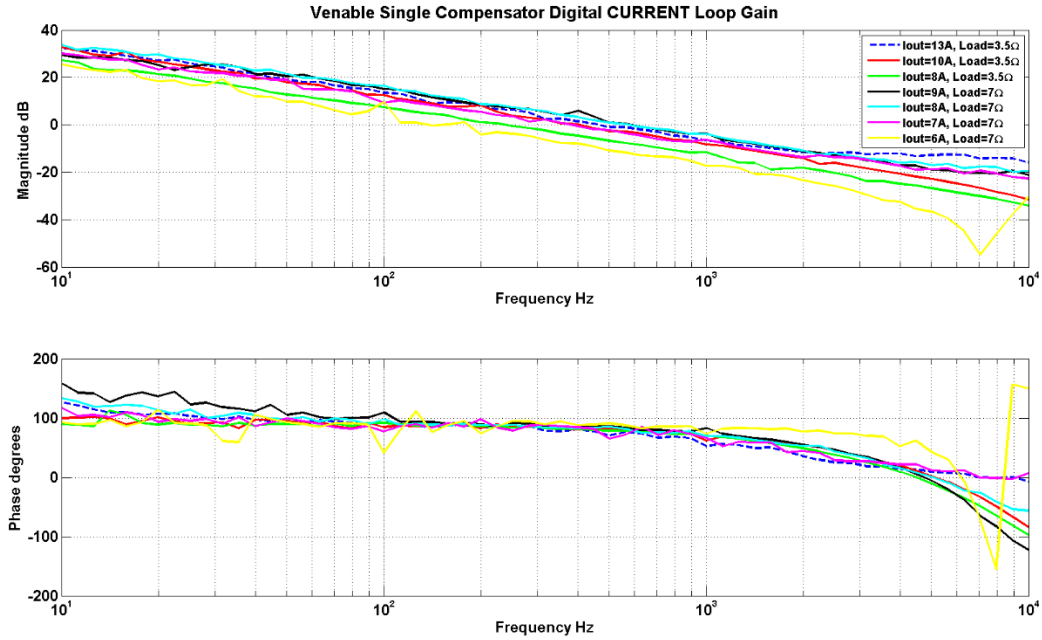
Figure 6.5 - Single compensation digital current loop gain (Experimental Data)
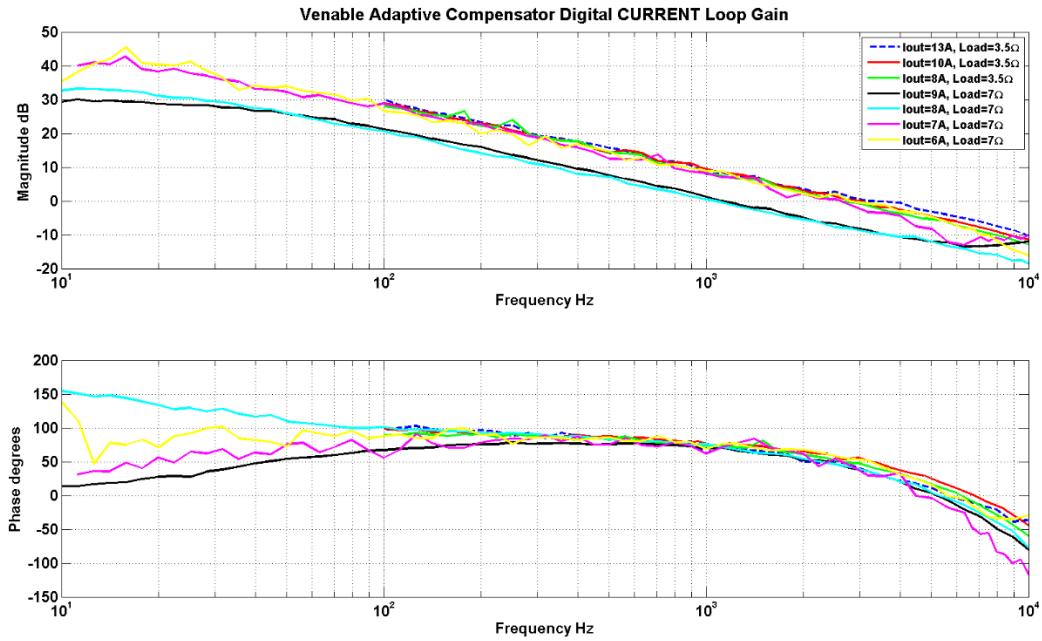
Figure 6.6 - Adaptive compensation digital current loop gain (Experimental Data)

In the single compensator case, it can be seen that although the stability margins are well above the minimum criteria, the loop gain crossover frequency fc (which also corresponds to the control bandwidth) and the 120Hz disturbance rejection ability suffers greatly. Table 6.1 shows a summary of the experimental performance results for the single compensator design. These

experimental performance results are similar to the MATLAB simulated single compensator performance results back in Table 4.4. As can be seen, the worst performance voltage control mode operating point is Vout=36V, Load=7Ω and it achieves a crossover frequency fc=120Hz with a gain of 2dB at 120Hz. The worst performance current control mode operating point is Iout=6A, Load=7Ω and it achieves a crossover frequency of 210Hz and gain of 6dB at 120Hz. These performance results are very poor and can be much improved with the adaptive control method.

Experimental Digital Single Compensator Design Performance Results						
Control Mode	Operating Point		Stability Margins		Gain @ 120Hz	Loop Gain fc
	V or I	Load	Phase	Gain		
Voltage	48V	3.5Ω	78°	22dB	11dB	400Hz
	36V	3.5Ω	80°	26dB	7dB	300Hz
	28V	3.5Ω	88°	28dB	5dB	190Hz
	66V	7Ω	50°	13dB	22dB	1.05kHz
	54V	7Ω	62°	21dB	23dB	1.01kHz
	48V	7Ω	75°	19dB	17dB	400Hz
	36V	7Ω	90°	30dB	2dB	120Hz
Current	13A	3.5Ω	85°	10dB	12dB	450Hz
	10A	3.5Ω	90°	21dB	10dB	400Hz
	8A	3.5Ω	90°	23dB	8dB	220Hz
	9A	7Ω	70°	18dB	18dB	600Hz
	8A	7Ω	85°	15dB	19dB	650Hz
	7A	7Ω	88°	20dB	11dB	500Hz
	6A	7Ω	85°	30dB	6dB	210Hz

Table 6.1 – Single digital compensator experimental performance results

Table 6.2 summarizes the experimental performance results (from Figure 6.4 and Figure 6.6) of the digital adaptive compensated loop gains. The performance results show that the gain and phase margin requirements (phase margin = 60º, gain margin = 10dB) are not quite met for some operating conditions but they do come close. One possible reason is the unforeseen additional lag caused by the DSC, which would negatively affect the phase margin. Redesigning the compensators to have a slightly lower loop gain crossover frequency (fc) can help increase the phase and gain margins or design the compensated system intially with higher gain/phase requirements in mind so that the decrease in margins in the physical results are already accounted for. When compared to the results in Table 6.1, the gain at 120Hz and the loop crossover frequency are all significantly better than the single compensator design case. The

adaptive compensator design increases the control bandwidth up to 3-5 times higher and the gains at 120Hz are all around 20dB or more for all the varying operating conditions.

Experimental Digital Control Adaptive Compensated Experimental Performance Results						
Control Mode	Operating Point		Stability Margins		Gain @ 120Hz	Loop Gain fc
	V or I	Load	Phase	Gain		
Voltage	48V	3.5Ω	53°	11dB	25dB	1.7kHz
	36V	3.5Ω	54°	11dB	30dB	3kHz
	28V	3.5Ω	52°	15dB	28dB	2.7kHz
	66V	7Ω	60°	14dB	21dB	1.2kHz
	54V	7Ω	57°	20dB	22dB	1.3kHz
	48V	7Ω	60°	21dB	20dB	1.3kHz
	36V	7Ω	65°	18dB	21dB	1.2kHz
Current	13A	3.5Ω	53°	9dB	28dB	3kHz
	10A	3.5Ω	56°	10dB	27dB	2.9kHz
	8A	3.5Ω	55°	12dB	28dB	2.8kHz
	9A	7Ω	52°	8dB	26dB	2.2kHz
	7A	7Ω	58°	10dB	27dB	2.2kHz
	6A	7Ω	55°	8dB	24dB	2.5kHz

Table 6.2 - Adaptive digital control compensation experimental performance results

Note that the distortions in the experimental frequency response data may be the cause the noise interference because I was getting slightly different results at different times. The limitations of the Venable FRA hardware may also be part of the reason for the distortions.

Venable Digital Loop Gain Experimental Data vs MATLAB Loop Gain Simulation:

Figure 6.7-Figure 6.16 shows a comparison between the Venable adaptively compensated digital loop gain experimental data and its corresponding MATLAB simulated compensated loop gain for several different operating conditions. The comparisons shows both voltage mode control and current mode control loop gains which are adaptively compensated.
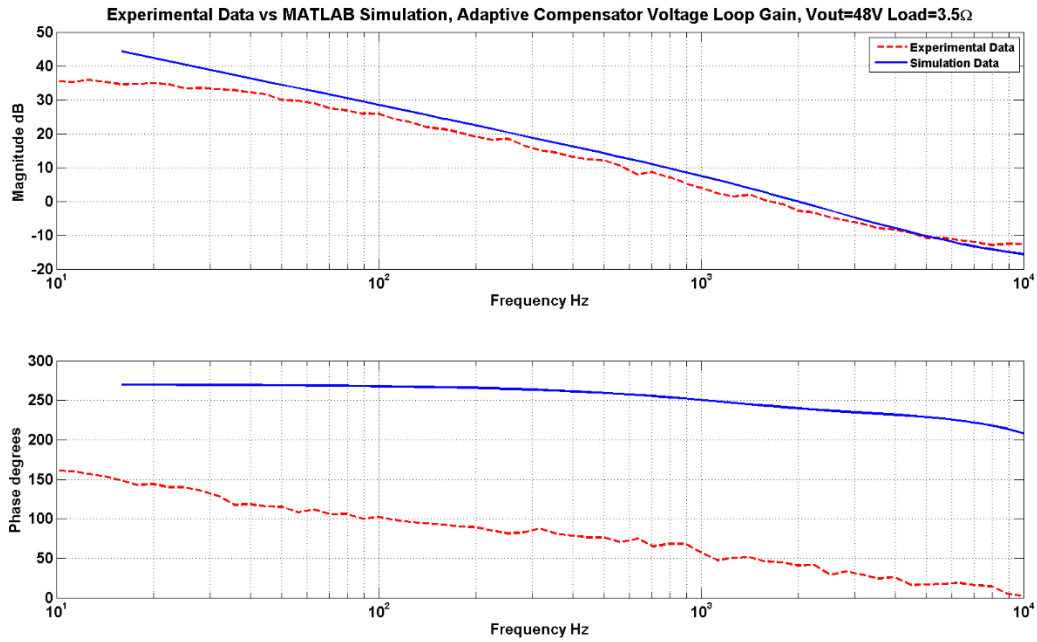
Figure 6.7 – Venable experimental data vs MATLAB simulation, Adaptive Compensation, Voltage Loop Gain, Vout=48V Load=3.5Ω
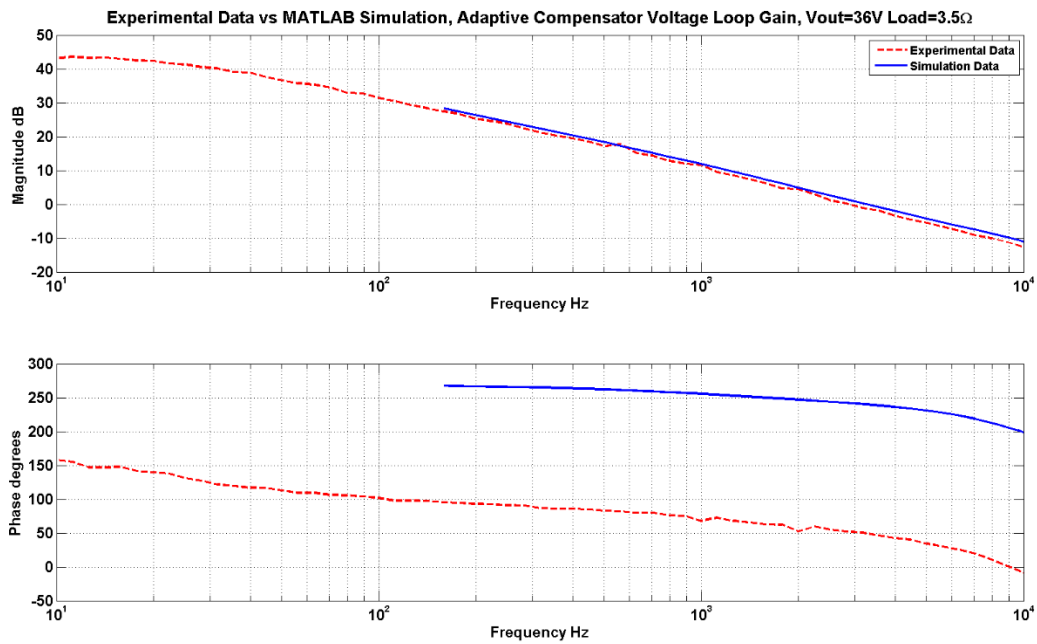
Figure 6.8 - Venable experimental data vs MATLAB simulation, Adaptive Compensation, Voltage Loop Gain, Vout=36V Load=3.5Ω
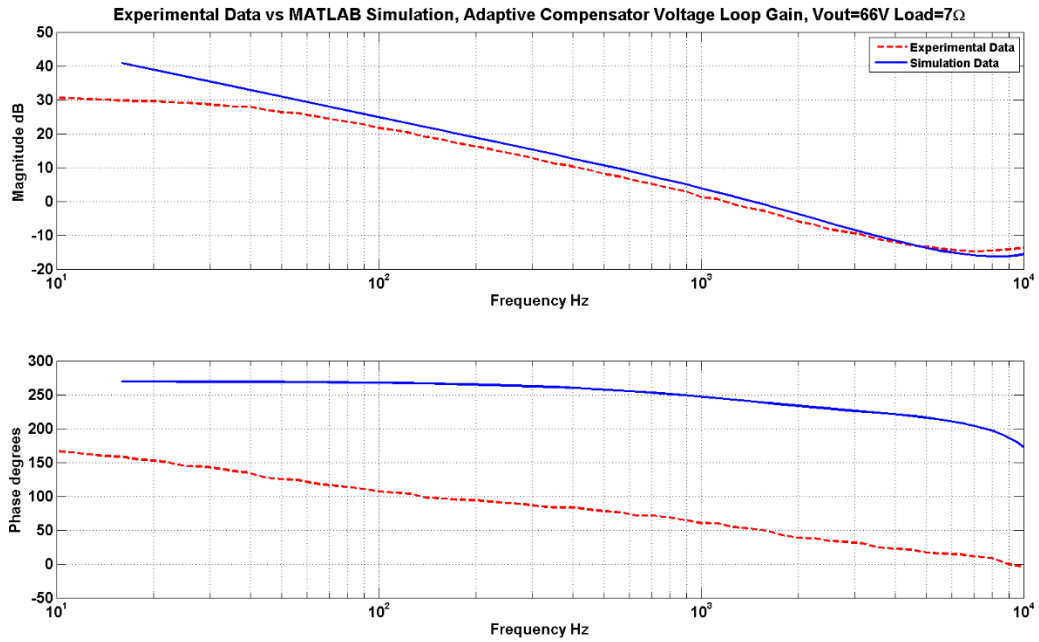
Figure 6.9 - Venable experimental data vs MATLAB simulation, Adaptive Compensation, Voltage Loop Gain, Vout=66V Load=7Ω
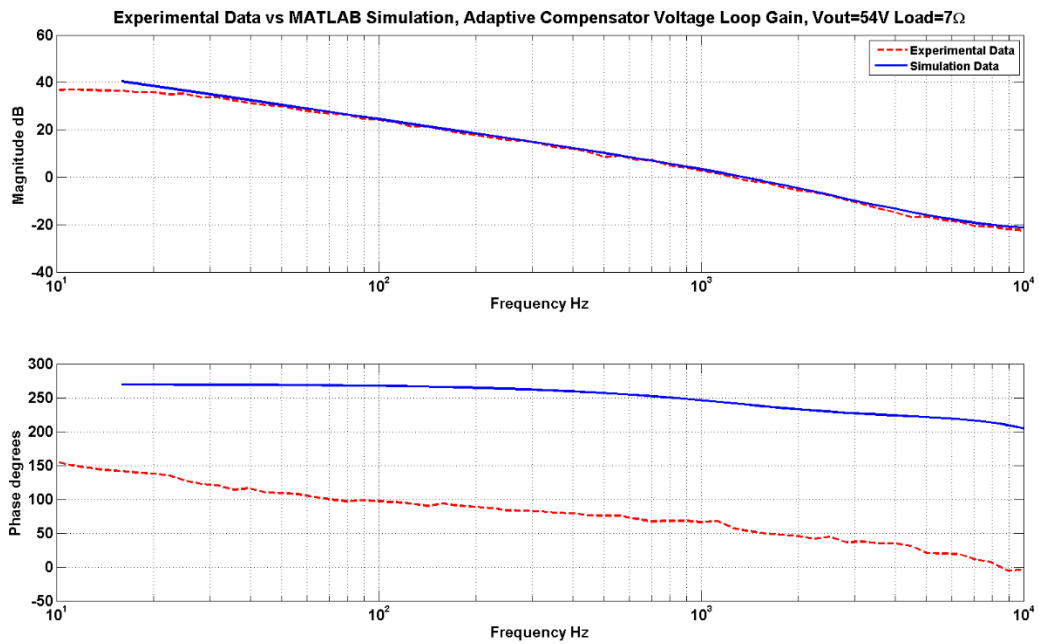
Figure 6.10 -Venable experimental data vs MATLAB simulation, Adaptive Compensation, Voltage Loop Gain, Vout=54V Load=7Ω

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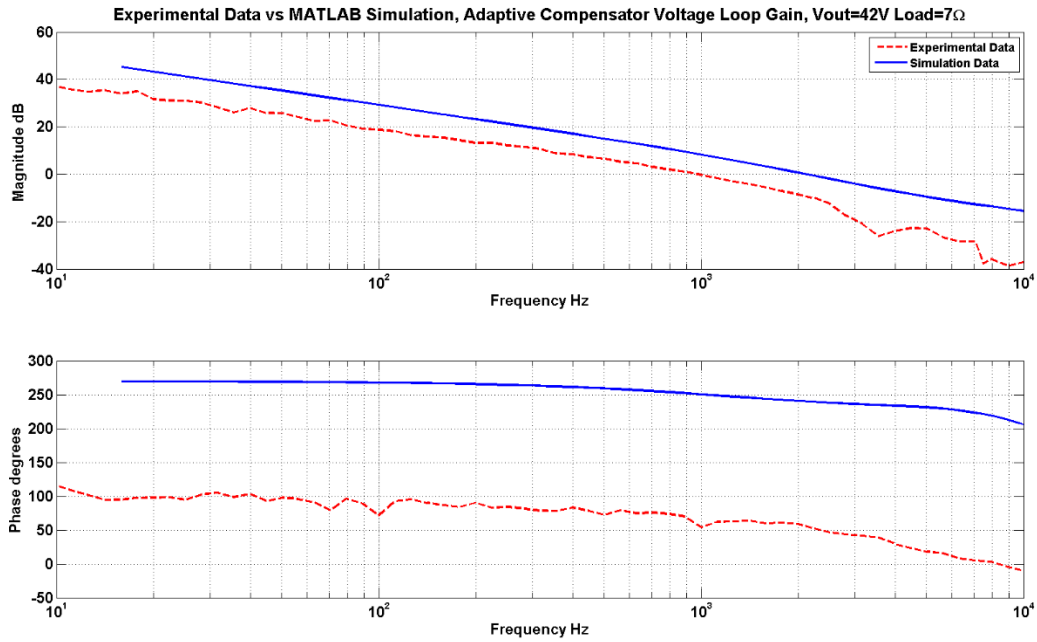
Figure 6.11 - Venable experimental data vs MATLAB simulation, Adaptive Compensation, Voltage Loop Gain, Vout=42V Load=7Ω
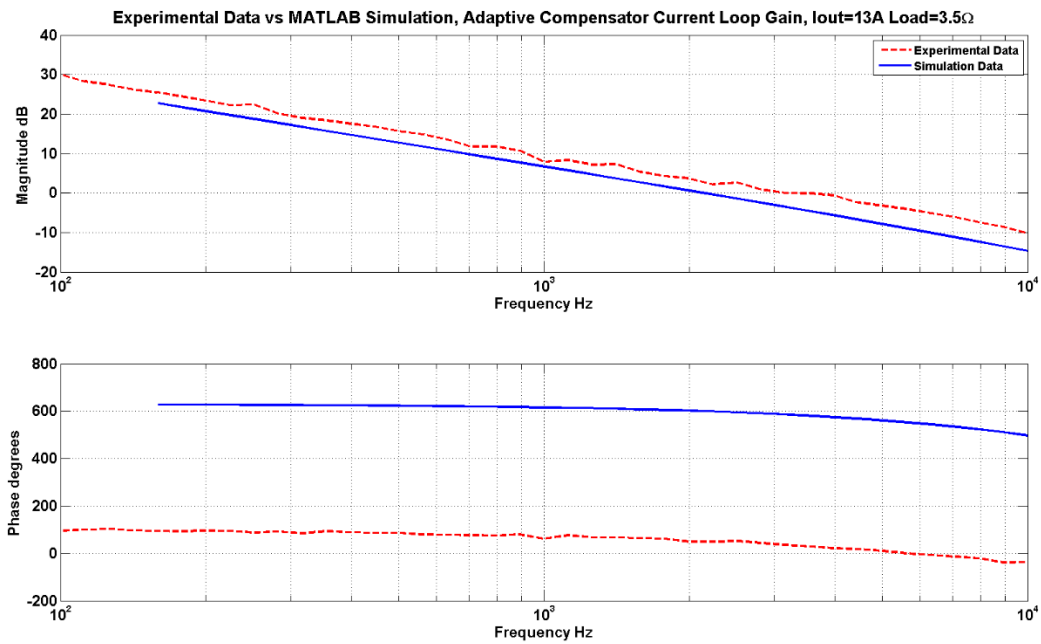
Figure 6.12 - Venable experimental data vs MATLAB simulation, Adaptive Compensation, Current Loop Gain, Iout=13A Load=3.5Ω
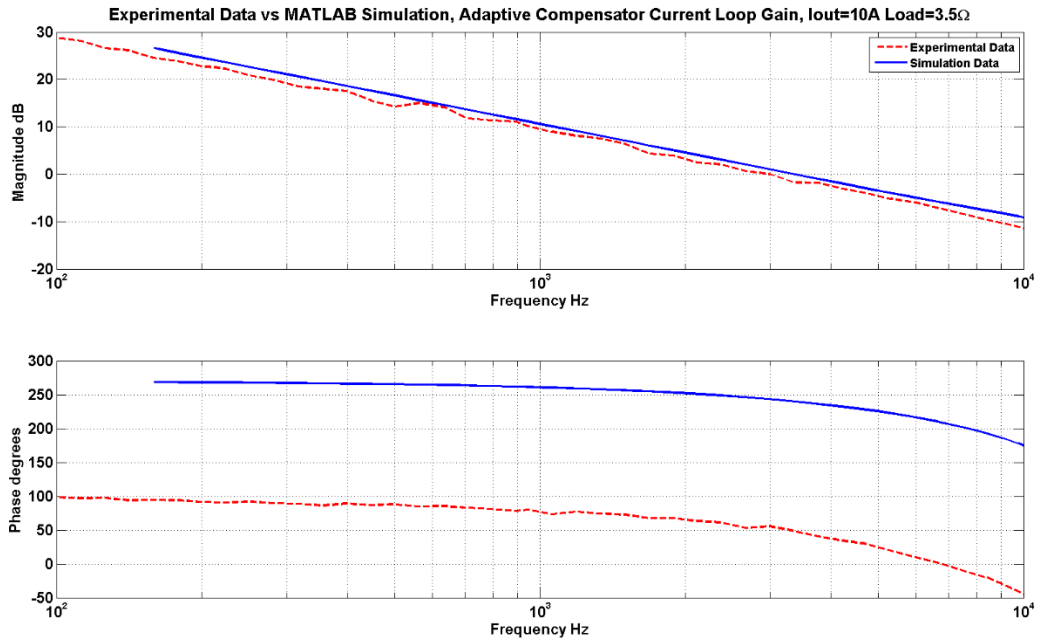
Figure 6.13 - Venable experimental data vs MATLAB simulation, Adaptive Compensation, Current Loop Gain, Iout=10A Load=3.5Ω
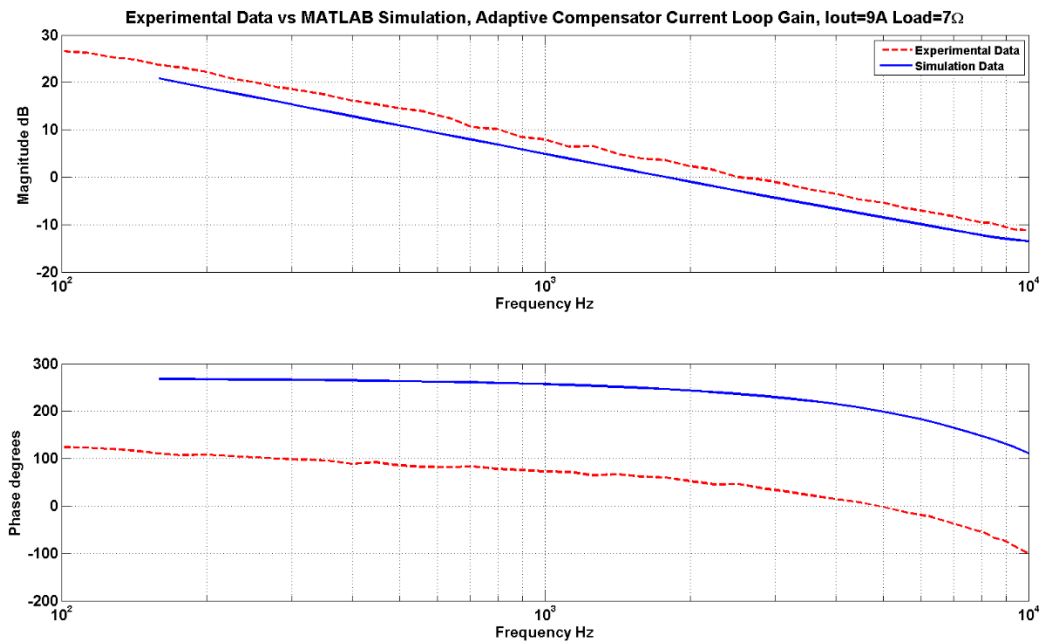
Figure 6.14 - Venable experimental data vs MATLAB simulation, Adaptive Compensation, Current Loop Gain, Iout=9A Load=7Ω
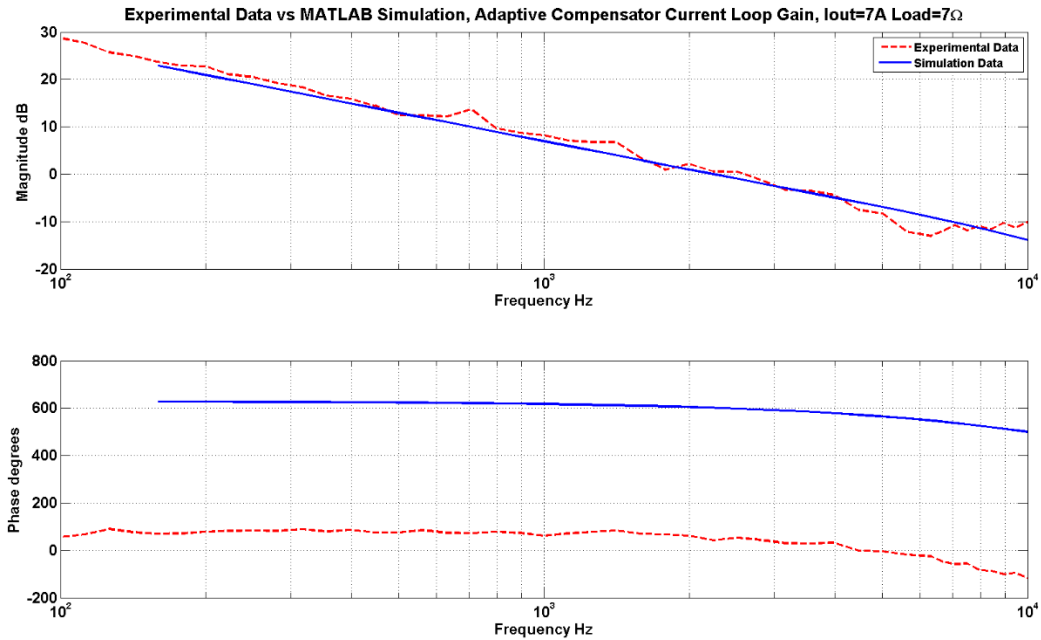
Figure 6.15 - Venable experimental data vs MATLAB simulation, Adaptive Compensation, Current Loop Gain, Iout=7A Load=7Ω
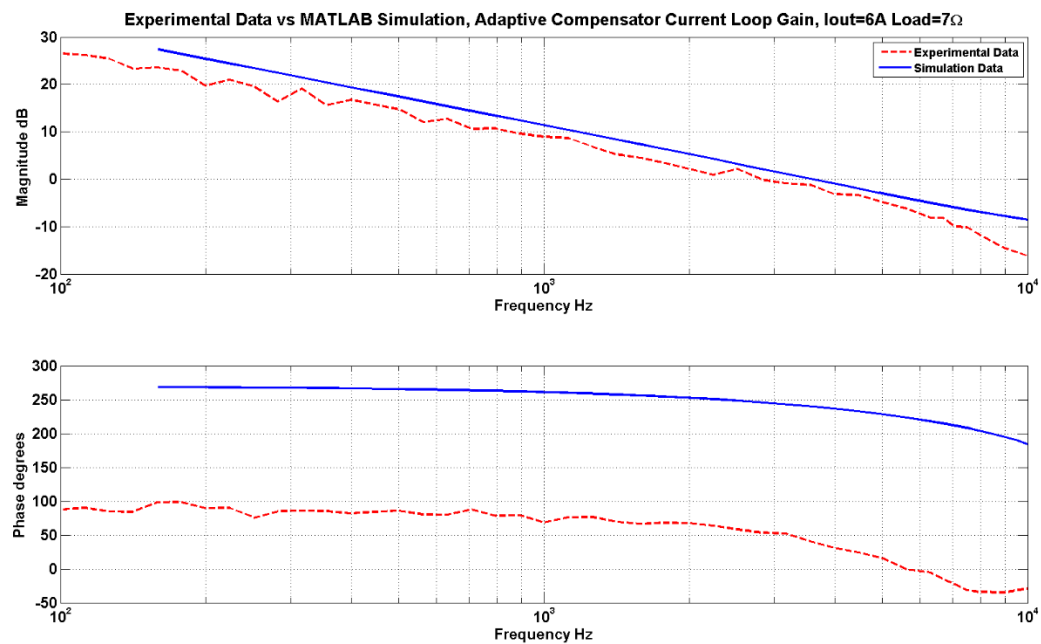
Figure 6.16 - Venable experimental data vs MATLAB simulation, Adaptive Compensation, Current Loop Gain, Iout=6A Load=7Ω

As can be seen from the comparison figures, the experimental data and the simulation overall matches well with a few outliers. Figure 6.11 shows the biggest magnitude discrepancy between the experimental data and simulation whereas all the other comparisons only have

minor magnitude discrepancies and are some are almost a perfect match. These comparison results shows the validity of using the empirical frequency response data and digital compensator design approach proposed in Chapter 4.

Note that the experimental phase plots are shifted approximately 180º when compared to the simulated phase plots. The 180º shift is the result of how the loop gain was experimentally measured. Recall that the 100Ω injection resistor is placed between the VCO and gain inverter circuit as shown in Figure 6.2. Because the CH2 measurement probe takes its measurement right after the gain inverter circuit while the CH1 probe measures the AC injection just before the VCO, the injected signal gets inverted by the gain inverter hence the 180º phase shift. For the simulated results, recall the loop gain measurements were taken before the gain inverter circuit as shown was in Figure 4.2.

One thing to note is that some of the 2P2Z compensators used in the experimental compensated loop gain data had to be modified from their original designs in Section 4.4.3. This is because some of the compensator designs when implemented with the TMS320F28035 DSC for the experimental prototype produced distorted and inconsistent results. I believe the reason may be that even though the compensator design was based on the physical uncompensated loop gain data and the discrete compensator bilinear transformation accounted for the 400kHz sampling rate, it was still not enough to accurately account for the full DSC effects (such as the ADC, DPWM, and switching noise). As a result, some of the compensators were modified to have a reduced crossover frequency in order to increase the stability margins. This will make some of the experimental performance results not match the simulated performance results in Section 4.4.3 exactly but the discrepancies should be minimal.

7 Conclusions and Future Work

7.1 Conclusions

The growing demand and necessity for tight regulation of the output voltage/current of power converters is critical for many various applications. As time passes, the regulation requirements for power converters become stricter which traditional (or classical) analog control techniques have trouble keeping up. In this thesis, a digital control technique was implemented on an existing analog controlled DC-DC LLC resonant converter in order to improve its dynamic performance and disturbance rejection. The main contribution of this thesis includes the design considerations of modifying an analog controlled LLC converter to support digital control, the digital controller design process, and the adaptive digital control algorithm technique. A secondary contribution is the introduction of an approach to model the LLC resonant using empirical data instead of using traditional mathematical techniques.

7.1.1 Considerations of Implementing Digital Design on an Existing Analog Controlled Converter

Chapter 3 provides an overview of the digital control considerations and the necessary components needed to implement digital control on an existing LLC resonant converter. The chapter describes the ADC, high resolution PWM, digital 2P2Z compensator, sampling rate, and the amount of system resources available/needed in order to execute these functions in time before the next sample rate. It was decided to implement the control loop at 400kHz which provides more than enough control bandwidth while leaving enough computation headroom for future features. Chapter 3 also provides a detailed overview of the analog components that are needed to successfully integrate digital control. The RC low-pass filter, the Gain Inverting Op-amp circuit, the VCO, and the voltage/current sensors were presented in detail. It was explained that it would be safer to keep the already built in analog VCO component to drive the LLC switches instead of driving the switches directly with the DSC because the VCO contained already implemented safety features which would make prototyping safer. Keeping the VCO resulted in the need to add the RC filter and Gain-Inverting Op-amp circuitry, which has negative effects on the overall system bandwidth. However, thanks to the high-resolutions PWM feature of the DSC, the RC filter was designed to have its cut-off frequency around 10kHz which is

much higher than the control bandwidth improvement aimed for in this thesis therefore the negative effect introduced by the extra component is considered not as significant.

7.1.2 Effectiveness of the Empirical Data Modelling Approach

Chapter 4 provides a detailed overview on process to achieve an optimized digital compensator design based on the empirical uncompensated loop-gain frequency response data collected from the physical converter. The digital controller design process involves first acquiring the uncompensated loop-gain frequency response data either from the physical converter using the Venable FRA hardware or from a PSIM simulation for several operating conditions. It was decided to use the Venable frequency response data because it provided a more accurate model of the converter. Then the frequency response data is used to estimate a mathematical state-space model with MATLAB's System Identification Toolbox. Finally, with the estimated model, an optimal continuous-time compensator was designed using MATLAB's SISO Toolbox and the compensator is then converted into its discrete-time equivalent using the bilinear method. In all, the approach of using the empirical data to model the LLC converter proved to be an effective and accurate way of designing compensators for the converter. When comparing the experimental frequency response performance results in Section 6.2 with the simulated performance results in Section 4.4.3, they match well. This modelling approach can also be applied to other resonant converters particularly to converters that are difficult to model using traditional mathematical methods.

7.1.3 Performance Improvements with Adaptive Compensation Design vs Single Compensation Design

Section 4.4.3 show a performance comparison between controlling the LLC converter using a traditional single compensator design method vs an adaptive compensation method, which provides an optimal compensator for a given operating range. The results in Section 4.4.3 are experimentally validated in Section 6.2. It was summarized that the single compensator design method was able to achieve excellent stability (gain and phase) margins through all operating conditions but with the sacrifice of significantly reduced bandwidth and very poor 120Hz noise rejection ability. In the adaptive compensation design method, the stability margins were not as high as the single compensation design but still achieve around the specified minimum values (phase margin > 60º, gain margin >10dB). However, the control bandwidth improved by a factor of 3-5 times and the compensated loop gain magnitude at 120Hz achieved

greater than around 20dB for all operating points. In all, the adaptive compensation method provided superior dynamic and noise rejection results while maintaining adequate stability for all operating conditions when compared to the single compensation design method.

7.1.4 Venable vs PSIM Frequency Response Data Accuracy

The overall frequency response shape from the PSIM simulation data matches well when compared to the Venable data for the varying operating points as was shown in Figure 4.13 to Figure 4.21. However, the magnitude of the frequency response between PSIM and Venable can vary up to 8dB. In particular, it was noticed that as the output voltage or current was set lower (which corresponds to increasing the switching frequency), the more the PSIM data deviated away from the Venable data. It was also noticed that the Venable magnitude is always lower than its corresponding PSIM simulation. The difference in magnitude may be caused by the ideal characteristics of the PSIM simulation components and the overall simplified converter model. At higher frequencies, the non-idealities of the resonant tank components (the inductor and capacitor) become more profound, which may result in reduced gains. Adding non-ideal factors such as parasitic effects increases complexity of the model, which also significantly increase an already long simulation time and may not even guarantee better accuracy. As a result, I decided the PSIM model was not accurate enough to design the compensator and therefore the Venable frequency response data was used instead. However, if the physical converter is not available or built, PSIM may be used to provide a viable rough estimate of the converter. The digital signal microcontroller's flexibility to adjust the control may be used to compensate for any discrepancies between the simulation and physical results.

7.1.5 Obtaining the Frequency Response Data More Quickly and Efficiently

Obtaining the frequency response data using the Venable method can be quite tedious because each measurement has to be manually setup for each operating point. In addition, increasing the data points to measure for the frequency response also increases the time to complete the measurement. This issue is compounded if the designer needs data for a large amount of operating points. An automated test bench can help speed up the data collection time significantly because it would not require someone to monitor and adjust the system constantly. For the PSIM frequency response simulation, each simulation can take up to 2-8 hours depending on the chosen starting frequency and the level of complexity of the circuit model. The

simulation time goes up exponentially for a lower starting frequency and increased circuit complexity. It was noticed that a single PSIM simulation takes up 25% of a computer's CPU utilization. Therefore, running four simulations at the same time will take up 100% of the CPU utilization while not slowing down any of the individual simulation times. It would also be helpful to somehow automate this process.

7.2   Future Work

1) Use the control law accelerator (CLA) module in the DSC to compute the 2P2Z compensator calculations. This will reduce the load of the main processor allowing for benefits such as faster sampling rates, more complex control algorithms, and additional software features.

2) Investigate the stability of the system when increasing the software background loop update rate (which is in charge of selecting the optimal compensator).

3) Find possible relationships between the 2P2Z coefficients with changing operating points. This may allow an algorithm to change the coefficients of the compensator to move with the changing operating points. The benefit is the elimination of the need to collect a large amount of frequency response data and store large amounts of compensator coefficients in the microcontroller memory.

4) Implement time domain step change experimental tests to compare with the simulated ones in this thesis.

5) Directly drive the LLC converter with DPWM frequency modulation therefore eliminating the need for the analog VCO. This will allow for better control bandwidth because of the elimination of the RC filter.

6) Create a more accurate PSIM model of the LLC resonant converter including parasitic effects. Evaluate how well creating a more complex PSIM model can help accuracy and determine if the expected much increased simulation time is worth it.

7) Model the converter and its digital components using direct digital design technique.

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Appendices

Appendix A: TI C2000 Piccolo TMSF28035 Specifications

- **High-Efficiency 32-Bit CPU (TMS320C28x™)**
  - **60 MHz (16.67-ns Cycle Time)**
  - **16 x 16 and 32 x 32 MAC Operations**
  - **16 x 16 Dual MAC**
  - **Harvard Bus Architecture**
  - **Atomic Operations**
  - **Fast Interrupt Response and Processing**
  - **Unified Memory Programming Model**
  - **Code-Efficient (in C/C++ and Assembly)**
- **Programmable Control Law Accelerator (CLA)**
  - **32-Bit Floating-Point Math Accelerator**
  - **Executes Code Independently of the Main CPU**
- **Endianness: Little Endian**
- **JTAG Boundary Scan Support** [1]
- **Low Cost for Both Device and System:**
  - **Single 3.3-V Supply**
  - **No Power Sequencing Requirement**
  - **Integrated Power-on Reset and Brown-out Reset**
  - **Low Power**
  - **No Analog Support Pins**
- **Clocking:**
  - **Two Internal Zero-pin Oscillators**
  - **On-Chip Crystal Oscillator/External Clock Input**
  - **Dynamic PLL Ratio Changes Supported**
  - **Watchdog Timer Module**
  - **Missing Clock Detection Circuitry**
- **Up to 45 Individually Programmable, Multiplexed GPIO Pins With Input Filtering**

- **Peripheral Interrupt Expansion (PIE) Block That Supports All Peripheral Interrupts**
- **Three 32-Bit CPU Timers**
- **Independent 16-Bit Timer in Each ePWM Module**
- **On-Chip Memory**
  - **Flash, SARAM, OTP, Boot ROM Available**
- **Code-Security Module**
- **128-Bit Security Key/Lock**
  - **Protects Secure Memory Blocks**
  - **Prevents Firmware Reverse Engineering**
- **Serial Port Peripherals**
  - **One SCI (UART) Module**
  - **Two SPI Modules**
  - **One Inter-Integrated-Circuit (I^2C) Bus**
  - **One Local Interconnect Network (LIN) Bus**
  - **One Enhanced Controller Area Network (eCAN) Bus**
- **Enhanced Control Peripherals**
  - **Enhanced Pulse Width Modulator (ePWM)**
  - **High-Resolution PWM (HRPWM) Module**
  - **Enhanced Capture (eCAP) Module**
  - **High-Resolution Input Capture (HRCAP) Module**
  - **Enhanced Quadrature Encoder Pulse (eQEP) Module**
  - **Analog-to-Digital Converter (ADC)**
  - **On-Chip Temperature Sensor**
  - **Comparator**
- **Advanced Emulation Features**
  - **Analysis and Breakpoint Functions**
  - **Real-Time Debug via Hardware**
- **2803x Packages**
  - **56-Pin RSH Very Small Quad Flatpack (No Lead) (VQFN)**
  - **64-Pin PAG Thin Quad Flatpack (TQFP)**
  - **80-Pin PN Low-Profile Quad Flatpack (LQFP)**

*Appendix A.1 - TI C2000 Piccolo TMSF2803x General Specifications*

	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1.y	WAKEINT (LPM/WD) 0xD4E	TINT0 (TIMER 0) 0xD4C	ADCINT9 (ADC) 0xD4A	XINT2 Ext. int. 2 0xD48	XINT1 Ext. int. 1 0xD46	Reserved – 0xD44	ADCINT2 (ADC) 0xD42	ADCINT1 (ADC) 0xD40
INT2.y	Reserved – 0xD5E	EPWM7_TZINT (ePWM7) 0xD5C	EPWM6_TZINT (ePWM6) 0xD5A	EPWM5_TZINT (ePWM5) 0xD58	EPWM4_TZINT (ePWM4) 0xD56	EPWM3_TZINT (ePWM3) 0xD54	EPWM2_TZINT (ePWM2) 0xD52	EPWM1_TZINT (ePWM1) 0xD50
INT3.y	Reserved – 0xD6E	EPWM7_INT (ePWM7) 0xD6C	EPWM6_INT (ePWM6) 0xD6A	EPWM5_INT (ePWM5) 0xD68	EPWM4_INT (ePWM4) 0xD66	EPWM3_INT (ePWM3) 0xD64	EPWM2_INT (ePWM2) 0xD62	EPWM1_INT (ePWM1) 0xD60
INT4.y	HRCAP2_INT (HRCAP2) 0xD7E	HRCAP1_INT (HRCAP1) 0xD7C	Reserved – 0xD7A	Reserved – 0xD78	Reserved – 0xD76	Reserved – 0xD74	Reserved – 0xD72	ECAP1_INT (eCAP1) 0xD70
INT5.y	Reserved – 0xD8E	Reserved – 0xD8C	Reserved – 0xD8A	Reserved – 0xD88	Reserved – 0xD86	Reserved – 0xD84	Reserved – 0xD82	EQEP1_INT (eQEP1) 0xD80
INT6.y	Reserved – 0xD9E	Reserved – 0xD9C	Reserved – 0xD9A	Reserved – 0xD98	SPITXINTB (SPI-B) 0xD96	SPIRXINTB (SPI-B) 0xD94	SPITXINTA (SPI-A) 0xD92	SPIRXINTA (SPI-A) 0xD90
INT7.y	Reserved – 0xDAE	Reserved – 0xDAC	Reserved – 0xDAA	Reserved – 0xDA8	Reserved – 0xDA6	Reserved – 0xDA4	Reserved – 0xDA2	Reserved – 0xDA0
INT8.y	Reserved – 0xDBE	Reserved – 0xDBC	Reserved – 0xDBA	Reserved – 0xDB8	Reserved – 0xDB6	Reserved – 0xDB4	I2CINT2A (I2C-A) 0xDB2	I2CINT1A (I2C-A) 0xDB0
INT9.y	Reserved – 0xDCE	Reserved – 0xDCC	ECAN1_INTA (CAN-A) 0xDCA	ECAN0_INTA (CAN-A) 0xDC8	LIN1_INTA (LIN-A) 0xDC6	LIN0_INTA (LIN-A) 0xDC4	SCITXINTA (SCI-A) 0xDC2	SCIRXINTA (SCI-A) 0xDC0
INT10.y	ADCINT8 (ADC) 0xDDE	ADCINT7 (ADC) 0xDDC	ADCINT6 (ADC) 0xDDA	ADCINT5 (ADC) 0xDD8	ADCINT4 (ADC) 0xDD6	ADCINT3 (ADC) 0xDD4	ADCINT2 (ADC) 0xDD2	ADCINT1 (ADC) 0xDD0
INT11.y	CLA1_INT8 (CLA) 0xDEE	CLA1_INT7 (CLA) 0xDEC	CLA1_INT6 (CLA) 0xDEA	CLA1_INT5 (CLA) 0xDE8	CLA1_INT4 (CLA) 0xDE6	CLA1_INT3 (CLA) 0xDE4	CLA1_INT2 (CLA) 0xDE2	CLA1_INT1 (CLA) 0xDE0
INT12.y	LUF (CLA) 0xDFE	LVF (CLA) 0xDFC	Reserved – 0xDFA	Reserved – 0xDF8	Reserved – 0xDF6	Reserved – 0xDF4	Reserved – 0xDF2	XINT3 Ext. Int. 3 0xDF0

Appendix A.2 - TI C2000 Piccolo TMSF2803x Interrupt Vector Table

Appendix B: PSIM Simulation Schematics
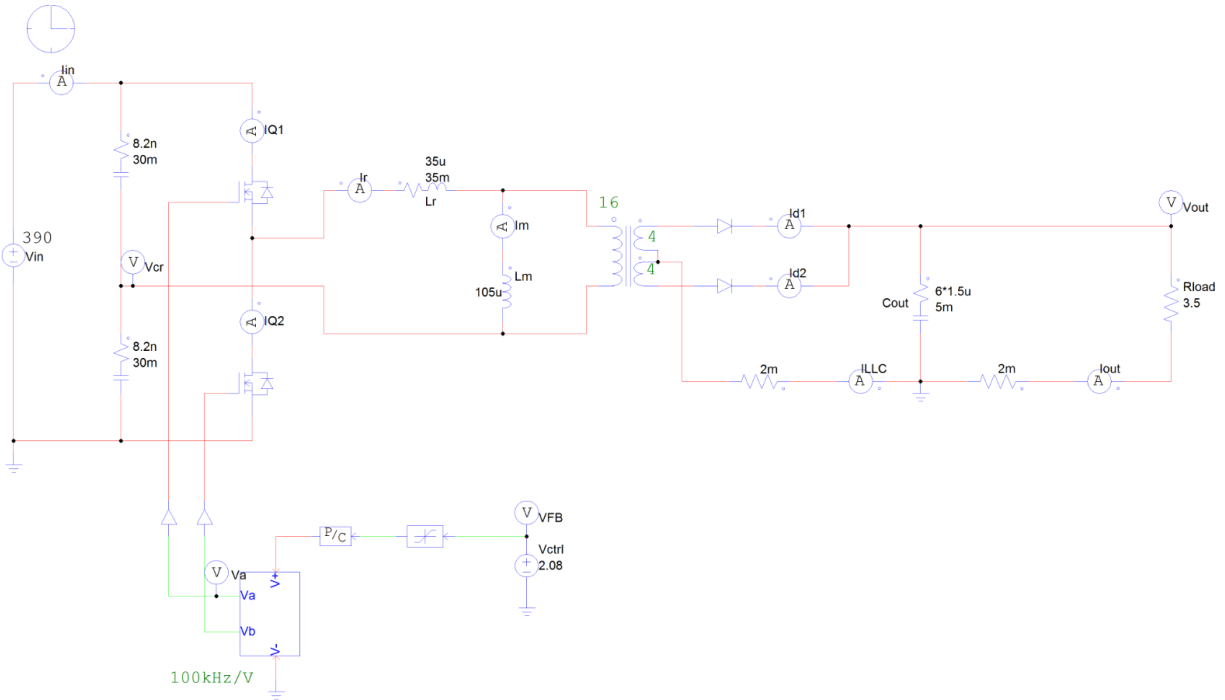
Appendix B.1 - PSIM model of LLC converter
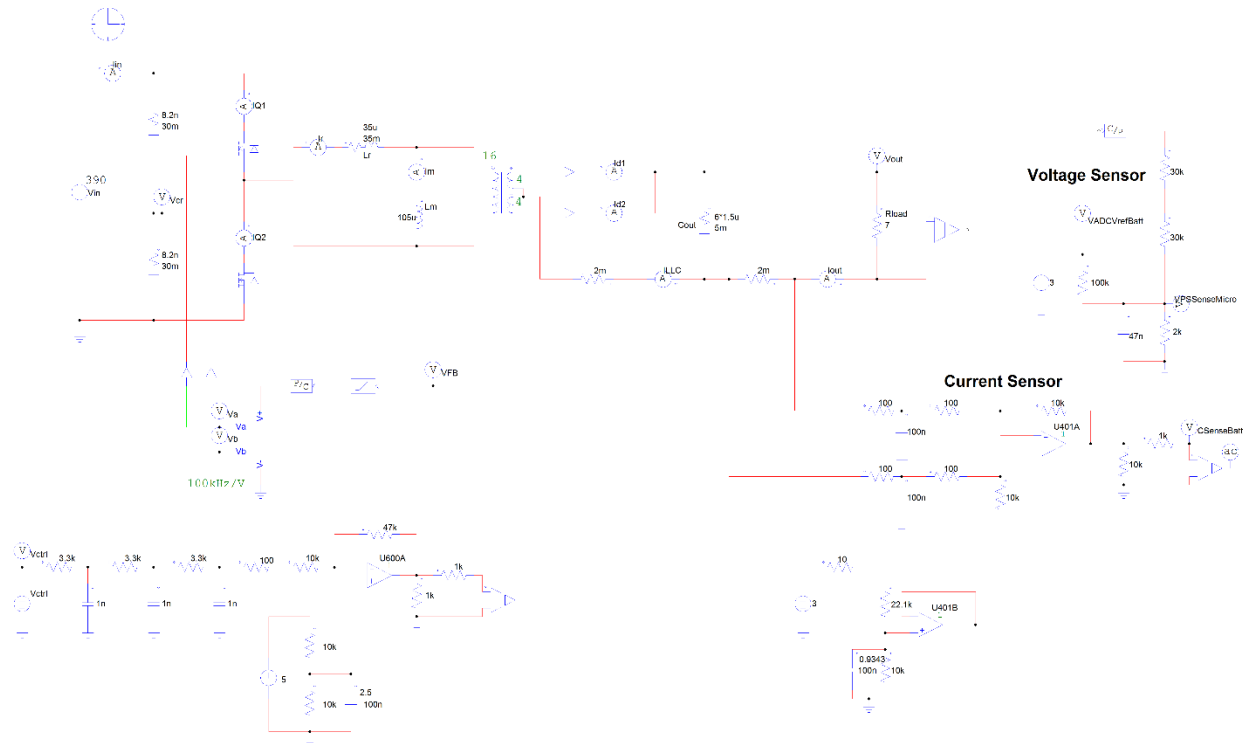
Appendix B.2 - PSIM model of Loop Gain Components including: RC Filter, Gain Inverter, VCO, LLC converter, Voltage/Current Sensors