A SERIES RESONANT CONVERTER FOR VOLTAGE EQUALIZATION OF SERIES CONNECTED SUPERCAPACITOR, ULTRACAPACITOR OR LITHIUM BATTERY CELLS

by

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Abstract

Supercapacitors are energy storage devices with great potential in many industrial applications. Although they are not as energy dense as batteries, they have much higher power density. This unique feature enables them to be used to provide bursts of energy in electric vehicle applications. They can be connected in parallel with batteries to source and sink dynamic energy which increases the lifetime of the expensive lithium batteries.

Typically, the maximum voltage of a single supercapacitor unit is low, e.g. 2.5 V. In many applications, manufacturers need much higher voltages, e.g. 400 V, so it is necessary to connect supercapacitors in series. A series connection of supercapacitor cells can result in voltage imbalance between cells, since individual supercapacitors have different tolerances. Voltage imbalance can lead to damage of the individual supercapacitors and even the failure of the total energy storage system. Cell voltage equalization is a strategy to maintain the reliability of the supercapacitor pack.

A single series inductor-capacitor (LC) resonant tank is proposed in this thesis for the voltage equalization of series connected energy storage elements. The circuit can be used for lithium battery cells, or supercapacitors, but the focus of the work targets supercapacitors. The circuit includes two levels of source connected MOSFET switches for the connection between resonant tank converter and each supercapacitor cell. A controller arranges supercapacitor voltages in descending order and makes a decision based on whether switches associated with the corresponding supercapacitors should be operated. If the voltage difference is higher than the pre-determined allowable value, the microcontroller sends pulse width modulation signals to gate drivers which control the on-off time of the MOSFET switches.

Simulation results are presented using PSIM and demonstrate that voltage differences among supercapacitors can be removed fast. Experimental results show that the prototype of the proposed circuit can reduce a voltage deviation of 527 mV down to 10 mV in 15 minutes. The circuit is small in size, achieves a relatively short voltage equalization time and has minimal loss, therefore largely alleviating the problems inherent to existing voltage equalization converters.

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List of Symbols

C	Capacitor
C_{1*} *to* C_{3*}	Reference capacitors
C_r	Resonant capacitor
C_{rated}	Rated capacitance of supercapacitor
D	Duty cycle
D_{cw}	Freewheeling diode when inductor current flows in clockwise direction
D_{ccw}	Freewheeling diode when inductor current flows in counter-clockwise direction
D_{1a} *to* D_{1d}	Full bridge rectifier diodes
D_{in}	Diodes on the positive levels of switches
D_{ip}	Diodes on the levels of P-channel switches
D_{s1}	Zigzag diode
ES	Energy storage device
f_r	Resonant frequency
f_s	Switching frequency
I_{ch}	Major charging current source
I_{dis}	Discharging current of a single supercapacitor
I_{rec}	Current received by the rest of supercapacitors
I_{rms}	Root mean square value of resonant current
I_{peak}	Peak value of resonant current
i_{Lm}	Magnetizing inductor current
i_r	Resonant current
i_{pack}	Current flowing through supercapacitor pack
i_{pk}	Peak current
L	Inductor

L_m	Magnetizing inductor
L_r	Resonant inductor
N	Total number of supercapacitors connected in a string
n	Sequence number of supercapacitors
R_{b1} to R_{b2}	Balancing resistors
R_{ds}	Drain-to-source resistance
R_{p1} to R_{p2}	Leakage resistors
R_{total}	Total resistance in the equivalent circuit
SC_1 to SC_n	Supercapacitors
S_{in}	Switches on the negative levels of supercapacitors
S_{ip}	Switches on the positive levels of supercapacitors
T	Switching period
t_0	Time instant when energy transportation starts
t_1	Time instant when resonant inductor current reaches its peak value
V_{cr}	Resonant capacitor voltage
V_{gs}	Gate to source voltage
V_i	Initial voltage of supercapacitor
V_p	Peak voltage of supercapacitor
V_{pack}	Voltage of entire supercapacitor pack
V_{rated}	Rated voltage of supercapacitor
V_{rms}	Root mean square value of resonant tank voltage
V_{sc}	Supercapacitor voltage
ω	Angular frequency
Z	Circuit impedance

$\lvert Z \rvert$	Magnitude of circuit impedance
$\lvert Z(f) \rvert$	Magnitude of circuit impedance with respect to switching frequency

List of Abbreviations

A	Amperes
AC	Alternating Current
ADC	Analog to Digital Converter
DC	Direct Current
EMI	Electrical Magnetic Interference
ESR	Equivalent Series Resistance
F	Farads
FFT	Fast Fourier Transform
H	Henry
Hz	Hertz
k	Kilo (10^3)
M	Mega (10^6)
m	Milli (10^{-3})
MIPS	Microprocessor without Interlocked Pipeline Stages
MOSFET	Metal Oxide Silicon Field Effect Transistor
PWM	Pulse Width Modulation
RMS	Root Mean Square
s	Seconds
V	Volts
W	Watts
μ	Micro (10^{-6})
Ω	Ohms

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All my achievements until now are the contribution of my effort and infinite support from my academic colleagues.

Dedication

To my parents who have supported me throughout my years of education financially and spiritually. To my cousins who have encouraged to study for the master degree.

Chapter 1: Introduction

1.1 Overview of Supercapacitor Characteristics

With the world's economic development, the total amount of existing non-renewable energy resources has decreased gradually. At the same time, the requirement for developing new energy resources has increased sharply. During the past several decades, a wide variety of energy resources have been explored. These energy resources mainly range from solar, wind, and tidal energy to biofuel energy. However, due to the increasing demand of energy and high costs of new energy development, non-renewable energy such as oil and natural gas still plays a vital role in society. Electrical energy is one of the most widely consumed forms of energy in modern era. However, the low efficiency of electrical energy conversion presents challenges for the integration of renewables. In order to maintain sustainable energy development, it is critical to improve electrical energy utilization efficiency.

Power electronics is the primary area for enhancing electrical energy utilization efficiency and the field has experienced rapid advancement over the past several decades. It has recently become prevalent in power conversion systems including AC/DC rectification systems, DC/DC conversion systems and DC/AC inversion systems. Power electronics also makes a significant contribution to electric transportation systems since electric vehicle technology has seen tremendous growth in the past decade.

In electric vehicles, fuel cells, batteries and capacitors usually act as energy storage devices to replace gasoline engines used in gas-powered vehicles. This continued adoption could reduce the greenhouse gas emitted from vehicles and reduce fossil fuel energy consumption. Batteries are relatively energy dense (typically 100- 200 Wh/kg) [1], but their limited power density has directed the research to focus on battery/capacitor hybrid systems. Supercapacitors,

or ultracapacitors, hereafter referred to as supercapacitors are a new type of capacitor, with very high capacitance in the hundreds to thousands of Farads. Conventional capacitors are typically limited to tens of farads. Supercapacitors have low equivalent series resistance (ESR), high level of stability, wide temperature operating range and virtually infinite life cycles and this enables them to be substitutes for conventional batteries.

Although supercapacitors have lower energy density (which is usually defined as the amount of energy kept in reserve per unit mass), they have much higher power density [2] (which is defined as the ratio of power to weight) than batteries. The power density for a typical supercapacitor cell can reach 2 kW/kg, while the energy density is 10 Wh/kg [3]. Due to their fast charge and discharge speed, they can easily satisfy electric vehicle demands for instantaneous power sourcing or sinking. Compared with batteries, which are rather difficult to manage because of their unstable internal chemical reactions [4], supercapacitors are much safer since they use static electricity for energy storage. Furthermore, unlike batteries which leak harmful chemicals into the environment when they are disposed of, supercapacitors are environmentally friendly [5]. In comparison with conventional batteries, the advantages of supercapacitors are summarized as follows:

1. High power density (ten times higher than that of typical batteries);

2. Environmentally friendly and safe;

3. Fast charge and discharge rate (supercapacitors can be recharged in less than thirty seconds);

4. Infinite charging and discharging cycles with little charge and discharge degradation;

5. Long calendar lifetime (typically 10 to 20 years);

6. Low internal resistance (higher current flow through with high efficiency).

The disadvantages of supercapacitor in industrial applications include:

1. Low energy density;

2. High self-discharge rate;

3. Spark hazard when short-circuited;

4. Low maximum voltage per unit cell due to manufacturing limitations; (therefore requires series connection of supercapacitors to obtain high voltage).

1.2 Supercapacitor Applications in Electric Vehicles

Supercapacitors are optimal devices for absorbing and delivering sudden power surges. The diagram for an example supercapacitor application in an electric vehicle is illustrated in Figure 1.1.

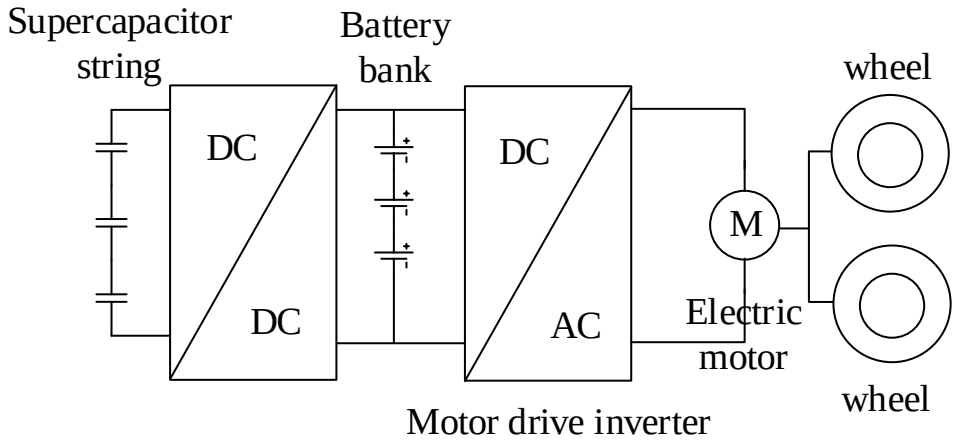

Figure 1.1 Battery and supercapacitor application in electric vehicle

In a typical electric vehicle application, supercapacitors can be used in conjunction with batteries as temporary energy storage devices. On the theoretical level, it is possible to use

supercapacitors as the sole energy source to power electric vehicles. However, their low energy density usually prevents them from exclusive use, so battery-supercapacitor hybrid systems can be used. While most existing EVs on the market, including the Tesla Model S, Nissan Lead and Ford Focus EV exclusively use batteries, issues with battery heating during acceleration/ deceleration dynamics, battery pack lifetime reduction have become a major concern. To solve this, supercapacitors can be added in parallel connection with batteries to meet the requirements of peak power absorption [6]. The basic idea behind this transportation application is that when starting an electric vehicle, supercapacitors can reduce battery cycling [7]. Since the lifetime of batteries can be longer when they undergo small amount of discharge with low frequency, these supercapacitors could extend the lifetime of expensive batteries during braking [8]. Supercapacitors can also be used for energy regeneration. In a typical electric vehicle application, batteries cannot utilize the large charge current during braking, while supercapacitors can capture the braking energy and store the energy temporarily. They then redistribute the stored energy for vehicle start and acceleration [9]. In addition, if the batteries fail to work normally under harsh weather conditions, supercapacitors can provide energy since they have wide operating temperature range, typically -40 ºC to 85 ºC [10].

1.3 The Necessity of Voltage Equalization for a Supercapacitor String

Generally, individual supercapacitor cell voltages are quite low [11] (2.5 to 2.7 volts, typically). This is due to the fact that they are built with high capacitance (the maximum capacitance could reach up to 5000 Farads). For modern industrial applications, it is critical for energy devices to generate high voltages to minimize system currents for a given power level. As a result, series and parallel configurations of supercapacitors are necessary to obtain

a high voltage [12], e.g. 200V. The voltage characteristics of supercapacitors depend on many factors, including equivalent series resistances (ESR), self-discharge rates and capacitance tolerance [13]. Due to their tolerance, not all the supercapacitors connected in series have the same capacitance (supercapacitor tolerance is typically up to +/-20%). Since supercapacitors are configured in series, the current flowing through the string is identical for all cells. Supercapacitors redistribute the charge between them in order to ensure that there is equal amount of current flowing through them. This directly contributes to the imbalance of individual supercapacitor voltages in a string during a single charging and discharging cycle. As the charging and discharging process continues, the voltage difference among the supercapacitors is further enlarged. This can become a severe problem because overcharging contributes directly to supercapacitor cell overheating which can result in capacitor damage, including gas generation and electrolyte decomposition. Therefore, the life span of supercapacitors will be reduced [14], or more severely, instantaneous failure. On the other hand, supercapacitors with lower voltages cannot reach their full potential energy storage capacity during the same charging process [15]. If we assume three supercapacitors have individual capacitances of $1.2C_{rated}$, C_{rated} and $0.8\ C_{rated}$, then because of the constant charging current, the voltage distributed across each supercapacitor is $0.83V_{rated}$, V_{rated} and $1.25\ V_{rated,}$ as illustrated in Figure 1.2. If the rated voltage for each supercapacitor is 2.5V, then the highest voltage/lowest capacitance cell will achieve a voltage of 3V, which is beyond the surge voltage level of a typical supercapacitor. Since the energy stored in the vehicle is dependent on both the high voltage supercapacitor cells and the low voltage supercapacitor cell, it is imperative to take some measures to minimize voltage difference among supercapacitors. These measures include the use of voltage detection and equalization circuits.

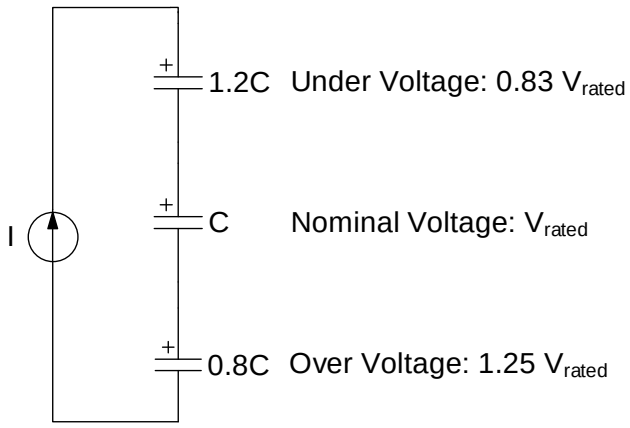

Figure 1.2 Voltage imbalance situation of supercapacitor

1.4 Contribution of the Thesis

The major contributions of this thesis include the following:

(1) A novel series LC resonant tank converter for voltage equalization of series connected supercapacitors;

(2) An explanation of the advantages of using resonance to achieve maximum current in the proposed equalization circuit;

(3) An explanation of the application of Fourier series analysis to the equivalent circuit model for the proposed equalization circuit;

(4) Experimental results demonstrating the effectiveness of the proposed circuit.

1.5 Thesis Outline

The thesis is organized into 5 chapters.

Chapter 1 provides a brief introduction of supercapacitors, current and future supercapacitor applications in the electric vehicle industry and the necessity of voltage equalization for supercapacitors.

Chapter 2 reviews the existing passive and active voltage equalization topologies for supercapacitors.

Chapter 3 presents the proposed single series LC resonant tank converter topology, its modes of operation, mathematical analysis for the equivalent circuit and simulation results.

Chapter 4 presents the experimental setup of the proposed topology, the components used in the printed circuit board prototype, and the results generated during tests.

Chapter 5 provides a summary of the work completed and results and includes additional topics for potential future work.

Chapter 2: Review of Existing Topologies for Energy Storage Device Cell Voltage Equalization

2.1 Overview

In this chapter, a review of existing voltage balancing circuits is presented. A brief review of different active voltage equalization methods is carried out along with their respective advantages and disadvantages. The review outlines the limitations of the existing work in order to establish the motivation for the proposed circuit topology.

2.2 Categorization of Voltage Equalization Methods

There have been several voltage equalization techniques proposed in the last twenty years. Generally, these voltage equalization methods can be categorized into two groups, passive voltage equalization methods and active voltage equalization methods [16].

Passive voltage equalization methods, such as the resistor shunting method, use energy-consuming devices such as resistors to remove excess energy from the higher-voltage supercapacitors. The extra energy flows through resistors and is dissipated as heat [17]，as illustrated in Figure 2.1.

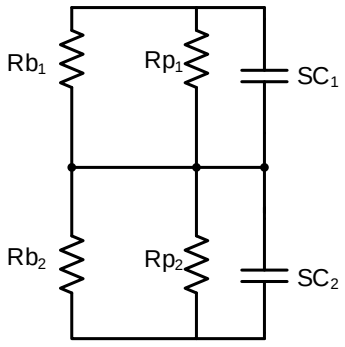

Figure 2.1 Passive voltage equalization topology using shunting resistors [17]

Balancing resistors R_{b1} and R_{b2} are matched and are configured in parallel with the supercapaitors which have very high internal parallel leakage resistors R_{p1} and $R_{p2,}$ which model their leakage current. Therefore, by connecting an additional resistor to each supercapacitor, the equivalent resistance across the supercapacitors reduces significantly and the equivalent resistance for each supercapacitor is nearly equal. However, in order to effectively balance a wide cell, the balancing resistors should be less than two percent of the highest leakage resistance. For example, assume two supercapacitors are charged by a 5 V voltage supply. Their rated voltages are 2.5 V and their leakage resistances are R_{p1}=1 MΩ and R_{p2}=0.5 MΩ, respectively. Therefore, the corresponding actual voltages across each supercapacitor are 3.3 V and 1.7 V. The voltage mismatch is 1.6 V. If we add a 200 kΩ balancing resistor, which is twenty percent of the maximum parallel leakage resistance value, then the apparent equivalent resistance will be 167 kΩ for SC_1 and 142 kΩ for SC_2. Correspondingly, the voltages for the two supercapacitors will be 4.61 V and 0.39 V. In this case, the resulting voltage difference is even higher than the case without voltage equalization. The resulting voltage for the higher voltage supercapacitor likely would lead to supercapacitor degradation. If we connect a 20 kΩ balancing resistor, which is two percent of the maximum parallel leakage resistance value, the apparent equivalent resistance will be 19.6 kΩ for SC_1 and 19.2 kΩ for SC_2. Correspondingly, the voltages for the two supercapacitors will be 2.52 V and 2.48 V. These voltage levels within 20 mV of the nominated value, i.e. 2.5 V and the voltage difference of the two supercapacitors is reduced to 40 mV. Generally, the lower the value of the balancing resistors, the smaller the voltage difference that can be achieved. This process terminates when all the supercapacitors configured in the string obtain their voltages.

Despite the fact that this topology has a simple structure and control strategy, small relative package size and low relative cost, the efficiency of the topology is low since a considerable amount of energy is converted into heat. In addition, the excessive heat generated by the resistors in the circuit could increase the temperature in the supercapacitor circuit, and therefore reduce the lifetime of the supercapacitors, or lead to difficulties with heat management.

On the other hand, active voltage equalization methods remove excess charge from high-voltage supercapacitors and transport the charge to the supercapacitors with lower voltages. These techniques employ energy storage elements such as inductors and capacitors to store energy temporarily. In terms of efficiency, the active voltage equalization methods are superior to passive voltage equalization methods because they can fully recover the energy in the original unbalanced supercapacitor cells.

Recently, due to the limitations of passive voltage balancing, researchers have begun to investigate active voltage equalization topologies [18] [19] [20] [21]. Some of these topologies use switched capacitors [22] [23] [24] [25], or buck-boost converters [26] [27] to regulate the voltages of individual supercapacitors and the others utilize transformers [28] [29] [30] to dynamically achieve voltage balancing. Work in these areas is discussed in the following sub-sections.

2.3 Single Inductor Topology

The single inductor voltage equalization topology proposed in [31] is illustrated in Figure 2.2. In this circuit, unidirectional switches are connected to the upper and lower side of the supercapacitors to maintain the direction of the inductor current. Bidirectional switches are

connected to the top and bottom of the entire supercapacitor string. The main current source, I_{ch}, aids the charge transfer during the charging process.

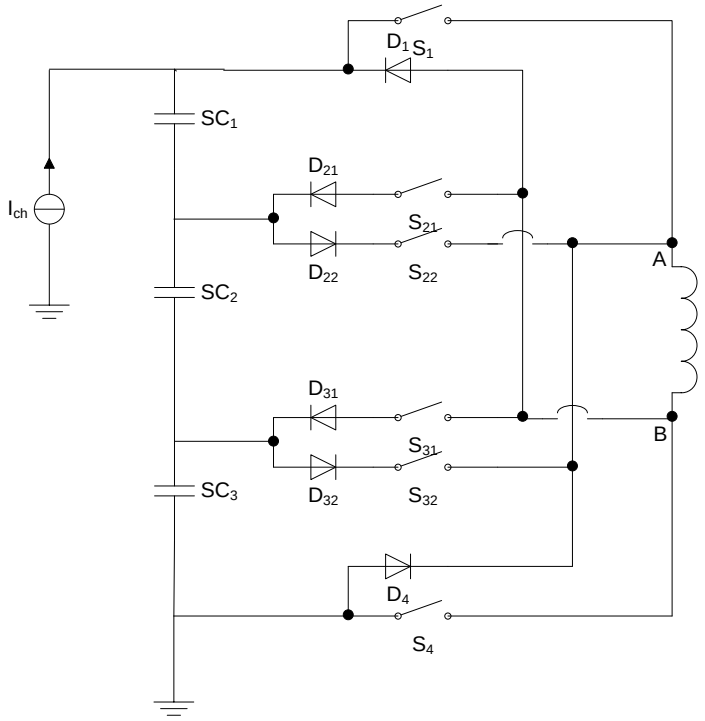

Figure 2.2 Single inductor topology [31]

The circuit operation is described as follows. As illustrated in Figure 2.3, assuming $V_{SC1} > V_{SC2}$. During the first half period of a single switching cycle, switch S_1 and S_{21} are turned on such that the voltage across supercapacitor SC_1 is applied to inductor L. Therefore, the current in the inductor increases linearly. During the second half period of the switching cycle, since the current in the inductor must maintain its direction, switch S_1 is turned off while S_{32} is turned on to redistribute the energy stored in the inductor to SC_2.

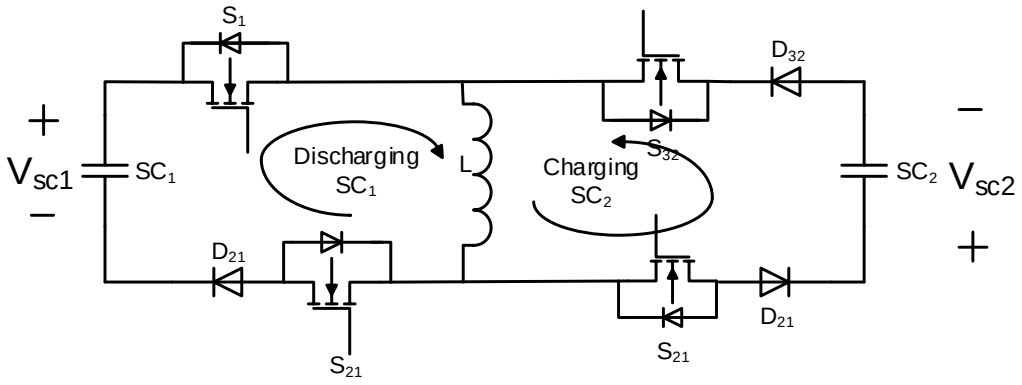

Figure 2.3 Equivalent circuit for single inductor topology when Vsc1>Vsc2

If there are more supercapacitors that need to be discharged in the supercapacitor string, the switches associated with each supercapacitor should be turned on in sequence to prevent overcharging of the low voltage supercapacitors. In this case, the discharging current can be much larger than the charging current.

In the most extreme case, for n supercapacitors, where there is only one weakly charged (i.e. low voltage) supercapacitor and the rest are all overcharged, the average current from the overcharged supercapacitors would be (n-1) I_{ch}, which transfers the charge to the supercapacitor with less voltage. Therefore, the inductor must be designed to ensure the weakly charged supercapacitor can absorb all the charge delivered.

The major advantage of this topology is that it employs only one inductor as the immediate energy storage device. However, the control strategy for the switches is complex.

2.4 Bi-directional Cûk Converter Topology

The bi-directional Cûk Converter topology proposed in [32] is illustrated in Figure 2.4. The equivalent circuit for two supercapacitors assuming $V_{SC1} > V_{SC2}$ is illustrated in Figure 2.5.

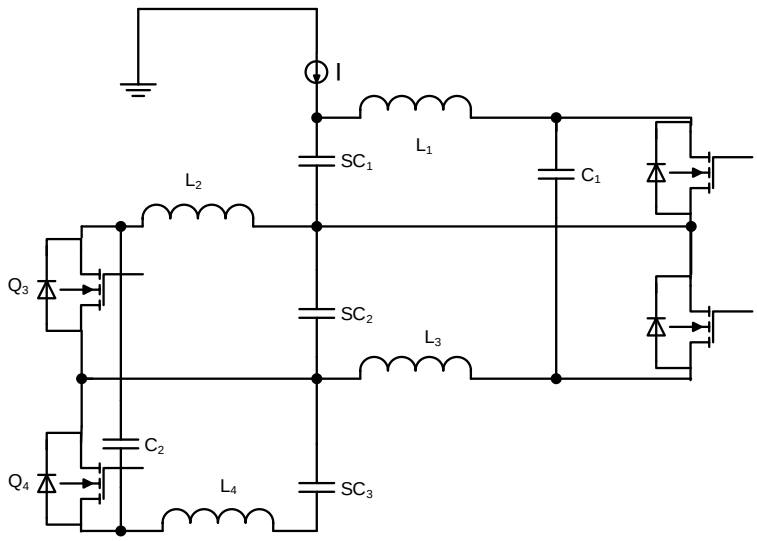

Figure 2.4 Bi-directional Cûk converter topology [32]

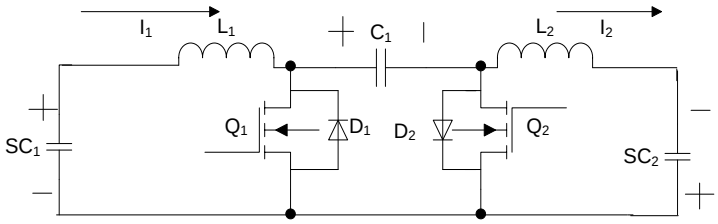

Figure 2.5 Equivalent circuit when $v_{sc1}>v_{sc2}$ in the bidirectional Cûk converter

Assume the voltage of supercapacitor SC_1 is higher than that of SC_2. There are three modes of circuit operation involved for this topology.

During mode 1 in time interval 0 - D_1T, where T is the switching period and D_1 is the duty ratio for the time duration when only Q_1 is turned on. Switch Q_1 is turned on to allow SC_1 to store energy into the inductor L_1. Simultaneously, capacitor C_1 discharges through Q_1 to SC_2, as shown in Figure 2.6. This mode ends when the voltage in C_1 reaches zero. The capacitor voltage across C_1 in this mode can be expressed as:

$$v_{c1} = \frac{i_1(1-D)T - i_2 t}{C_1} \tag{2-1}$$

where i_1 and i_2 are the currents flowing through SC_1 and SC_2 respectively and D is the duty ratio for the time duration when both Q_1 and D_2 are turned on.

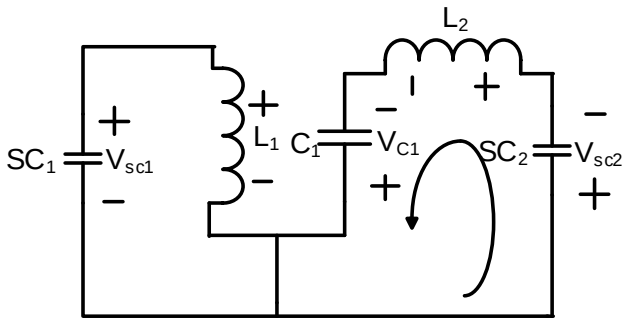

Figure 2.6 Operation mode 1 of the bi-directional Cûk converter

During mode 2 between time interval D_1T and DT, Switch Q_1 remains on, while body diode D_2 is forced to turn on. Then inductor L_2 distributes its stored energy to supercapacitor SC_2 through D_2, as shown in Figure 2.7. The capacitor voltage across C_1 in this mode remains zero.

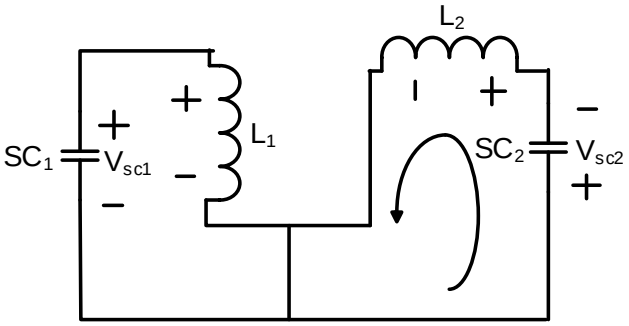

Figure 2.7 Operation mode 2 of bi-directional Cûk converter

During mode 3 between time interval DT and T, Q_1 is turned off, while D_2 remains on. Capacitor C_1 is charged by SC_1, while the voltage of SC_2 is controlled by the current in inductor L_2, as shown in Figure 2.8.

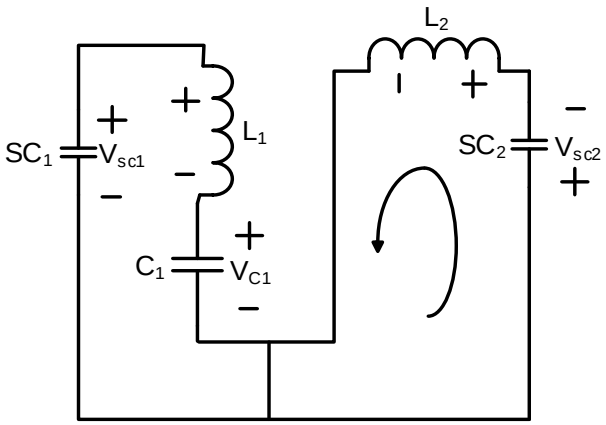

Figure 2.8 Operation mode 3 of bi-directional Cûk converter

The capacitor voltage in this mode can be written as (2-2):

$$v_{c1} = \frac{i_1(t - DT)}{C_1} \tag{2-2}$$

The capacitor C_1 is charged to the same initial voltage as at time zero, therefore by capacitor charge balance,

$$I_1(1 - D)T = I_2 D_1 T \tag{2-3}$$

which means:

$$D_1 = \frac{(1 - D)I_1}{I_2} \tag{2-4}$$

By integration of the capacitor voltage in mode 1, the average capacitor voltage and average diode voltage can be expressed by (2-5) and (2-6), respectively.

$$V_{c1} = \frac{T}{2C_1} I_1(1 - D)(1 - D + D_1) \tag{2-5}$$

$$V_{D2} = \frac{I_1(1 - D)D_1 T}{2C_1} \tag{2-6}$$

Since the average supercapacitor voltages are $V_{SC1}=V_{C1}-V_{D2}$ and $V_{SC2}=V_{D2}$, the ratio between V_{SC1} and V_{SC2} can be expressed as:

$$\frac{V_{sc2}}{V_{sc1}} = \frac{D_1}{1-D} \tag{2-7}$$

Substituting (2-4) into (2-6), the duty ratio D_1 is given by:

$$D_1 = \sqrt{\frac{2C_1V_{sc2}}{I_2T}} \tag{2-8}$$

Although this circuit has a relatively short voltage equalization time, the control pattern of the switches is complicated.

2.5 Single Switch Voltage Multiplier Topology

The single switch voltage multiplier topology proposed in [33] is illustrated in Figure 2.9. In this circuit configuration, SC_1 to SC_3 are supercapacitors and C_{1*} to C_{3*} are reference capacitors whose voltages are also balanced during the equalization process. The inductor L_1 in the circuit plays the role of a current source and the inductor L_2 is placed to prevent a short circuit through diode D_{s1}. The diodes in the zigzag pattern transport the energy upward from the bottom of the circuit.

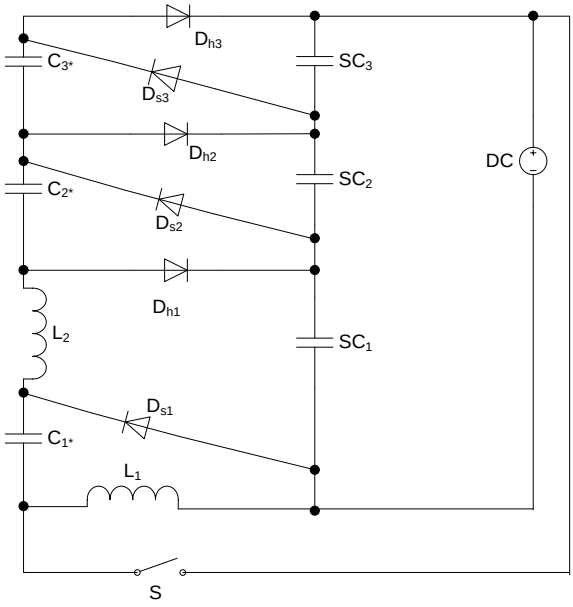

Figure 2.9 Single switch voltage multiplier topology [33]

When the switch S turns on, there is current flowing through the switch from the DC voltage source. The reference capacitors on the left-hand side are charged by the DC voltage source. There is a branch of balancing current flowing through the supercapacitors on the right-hand side to balance the voltages of the supercapacitors and the rest of current continues to flow upward to balance the voltage of the upper supercapacitors, as shown in Figure 2.10.

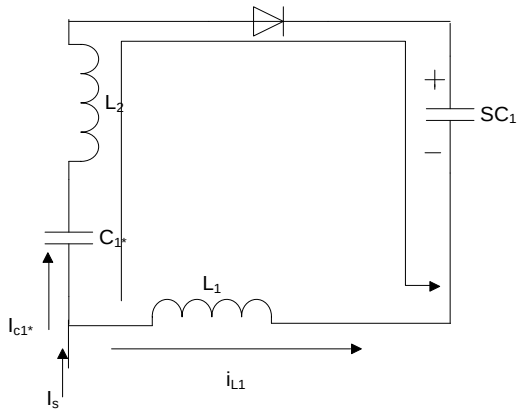

Figure 2.10 Current flow during the on-state of the switch

When the switch turns off, the inductor distributes its stored energy to reference capacitor C_{1*} through the diode D_{s1}, as shown in Figure 2.11.

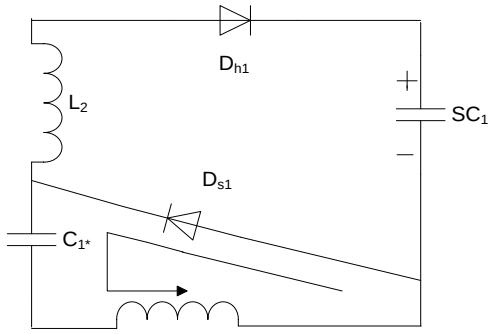

Figure 2.11 Current flow during the off-state of the switch

The voltages of the supercapacitors are applied across the reference capacitors through the diagonal diodes. With the flowing energy, all the voltages of reference capacitors can also be balanced.

Although only one switch is used in the circuit and there is no necessity for voltage detection circuits since the energy transports from the bottom unit to the top unit automatically, this circuit suffers from the problem of a relatively long voltage equalization time. In addition, the switches and diodes suffer from high voltage and current stress.

2.6 Buck-boost Shunting Converter Topology

The buck-boost shunting converter topology proposed in [34] is illustrated in Figure 2.12. In this circuit configuration, the supercapacitor string is charged by a constant current source I, which assists the process of charge transportation. Each supercapacitor in the string is connected in parallel with a buck-boost converter unit which plays the role of voltage equalization. C_r is a capacitor for temporary energy storage and it is connected with an additional buck-boost converter to retransfer its stored energy back to the current source. The

voltages of supercapacitors are measured by voltage detectors and then the measured voltages are compared with the average voltage of all supercapacitors. As long as the difference between the measured voltage and the average voltage exceeds a predetermined value, the corresponding buck-boost converter will be activated by the controller.

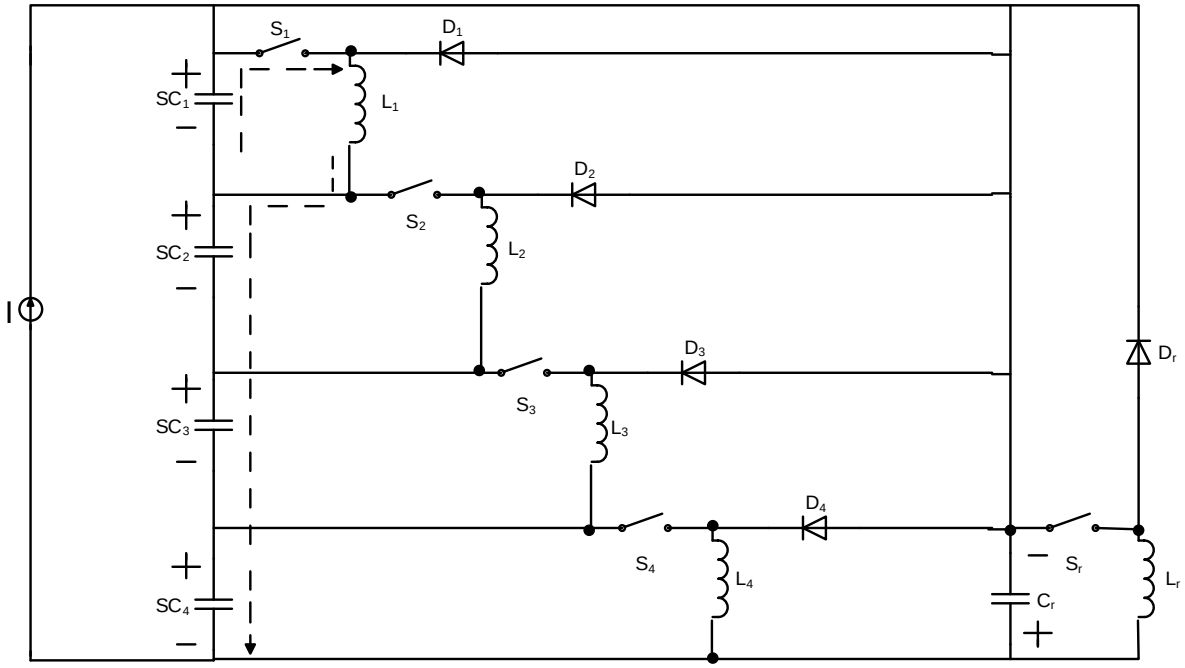

Figure 2.12 Buck-boost shunting converter [34]

As an example, assuming supercapacitor SC_1 has higher voltage than the others. Switch S_1 is turned on to balance the voltage of SC_1. The buck-boost converter shunting SC_1 draws energy from SC_1 and stores the energy in inductor L_1. The current through the inductor increases linearly and reaches its peak current value when switch S_1 is turned off. Then during the off-state of S_1, the inductor releases its stored energy downstream to the other supercapacitors. Therefore, current flows out of the inductor and through SC_2, SC_3, SC_4 and C_r.

When there are more supercapacitors that have higher than rated voltages, then the lower supercapacitor equalization circuits draw currents that are higher than the current provided by the constant current source. The current consists of the part of constant current source and the part dispensed from upper supercapacitors. Thus, the duty ratio of the lower supercapacitor units is larger than that of the upper units, and is given by:

$$D = \frac{Li}{vT} \tag{2-9}$$

However, the upper units have a higher decreasing rate of inductor current ($\frac{di}{dt} = \frac{v}{L}$) than the lower units because they sustain higher reverse voltages when their corresponding switches turn off.

The discharging current of a single supercapacitor can be expressed as:

$$I_{dis} = \frac{1}{T}\int_0^{DT} \frac{Vt}{L} dt = \frac{1}{2}\frac{VD^2T}{L} \tag{2-10}$$

And the current received by the remaining supercapacitors is given:

$$I_{rec} = \frac{1}{T}(\frac{1}{2}\frac{Vsc\ DT}{L}\frac{Vsc\ DT}{(N-n+1)V}) \tag{2-11}$$

where V_{sc} stands for the individual voltage of a single supercapacitor, N is the total number of supercapacitors connected in a string and n is the sequence number of the supercapacitors.

As an example of when there are more supercapacitors sustaining over-voltages, assume that SC_1 and SC_2 supercapacitor equalization units are activated. From the analysis above, the duty cycle of the circuit SC_1 is less than that of the SC_2 unit and therefore, switch S_1 enters its off state before switch S_2. There are three modes of operation for the converter unit. These are described in the following paragraphs.

In mode 1, switches S_1 and S_2 are turned on. As a result, the currents flowing into the inductors L_1 and L_2 increase linearly.

In mode 2, switch S_1 is turned off while switch S_2 remains on. Consequently, the current flowing into inductor L_1 decreases gradually while the current flowing into inductor L_2 continues to increase. Either the current in the inductor L_1 declines to zero before the instant when switch S_2 is turned off or the inductor current becomes zero after the switching of S_2.

In mode 3, the stored energy in inductor L_2 is transferred to capacitor C_r which accumulates the transported energy from the equalization units. When the stored energy exceeds the predetermined energy storage capacity value of capacitor C_r, capacitor C_r distributes its energy back to the supercapacitor string.

The main advantage of this topology is its relatively low component count and cost. However, the switches suffer from high voltage stress and the control strategy for the switches is complex.

2.7 Selective Flyback Converter Topology

The selective flyback converter topology proposed in [35] is illustrated in Figure 2.13. The input of the flyback transformer used in this topology is connected to each supercapacitor which is controlled by its own switch. The output of the converter is the total voltage of the supercapacitor string. Therefore, the entire topology is a pack-to-cell topology.

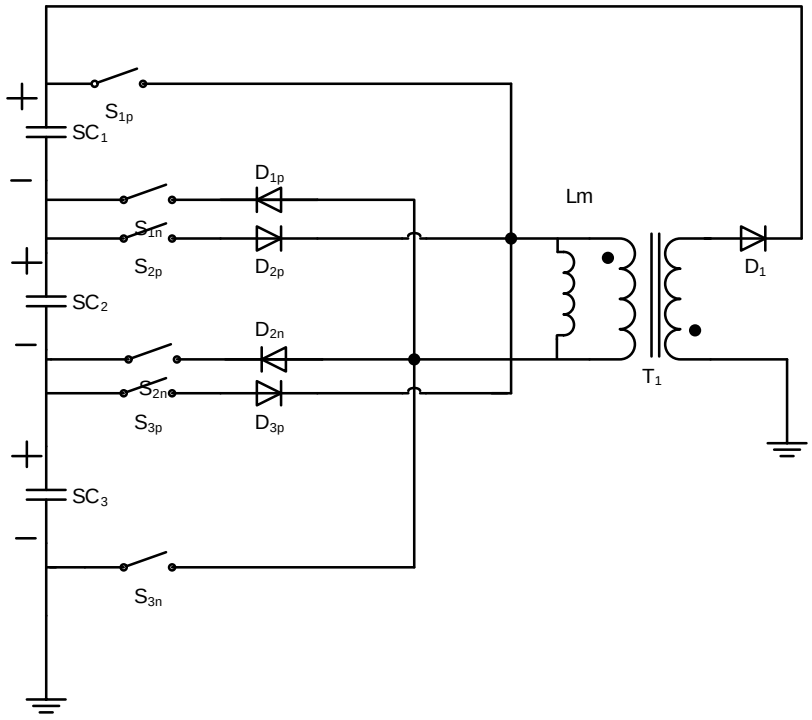

Figure 2.13 Selective flyback converter topology [35]

In this circuit configuration, each supercapacitor has a pair of switches and diodes connected to both the upper side and lower side of the transformer. The diode $D_{(i+1)p}$ connected in series with $S_{(i+1)p}$ is used to prevent the ongoing charging supercapacitor from being shorted when it is in the voltage balancing process. If $D_{(i+1)p}$ is removed, then S_{ip}, D_{ip} and the body diode of $S_{(i+1)p}$ would form a short circuit to the supercapacitor. The same principle can be applied for the connection of $D_{(i+1)n}$. However, the top and bottom supercapacitors do not have adjacent supercapacitors connected on the upper side and lower side respectively. Consequently, diodes connected in series with these switches are not required.

The circuit has two modes of operation which are described in the following paragraphs.

In mode 1, the voltage detector associated with each supecapacitor finds the higher voltage supecapacitor and the corresponding switches S_{ip} and S_{in} are turned on. The supecapacitor voltage is applied to the transformer primary winding and the magnetizing inductor current in the transformer increases linearly until it reaches the preset peak current value, as given by:

$$i_{Lm}(t) = \frac{V_{sc}(t - t_0)}{L_m} \tag{2-12}$$

In mode 2, switch S_{ip} remains turned on and switch S_{in} is turned off. The magnetizing inductor current is reflected to the secondary side of transformer and the diode D_1 is forced to turn on. The reflected energy is transported back to the supercapacitor string. This mode ends when the reflected current becomes zero. The reflected current is given by:

$$i_{pack}(t) = \frac{1}{n}[i_{pk} - \frac{V_{pack}}{nL_m}(t - t_1)] \tag{2-13}$$

After mode 2, all the switches wait until another switching signal is generated.

The main advantage of this topology is its fast speed to achieve voltage equalization. There is no necessity for external power sources due to the fact that the energy reflected from the primary side of the transformer can be delivered back to the supercapacitor string. It can also achieve voltage balancing with high efficiency due to the minimization of power flow paths. Nevertheless, the disadvantage is that the voltage stress and current stress for the switches and diodes are high. Apart from that, the magnetic losses in the circuit are high, which results in low efficiency of the circuit.

2.8 Half-bridge Multi-winding Output DC-DC Converter Topology

The half-bridge multi-winding output DC-DC converter topology proposed in [36] is illustrated in Figure 2.14.

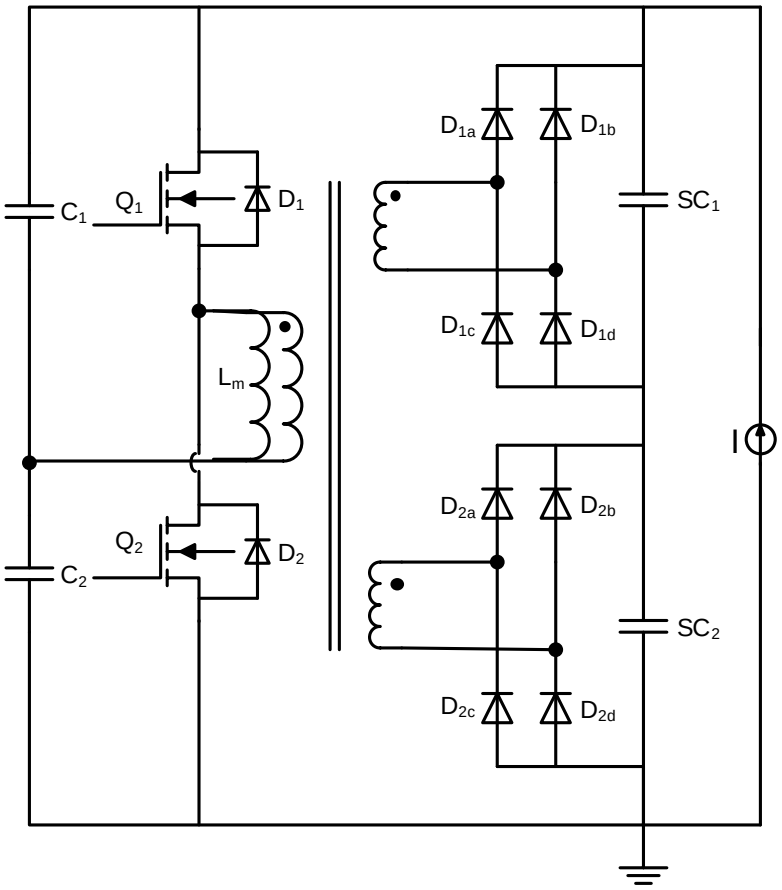

Figure 2.14 Half-bridge multi-winding output DC-DC converter topology [36]

The topology consists of a multi-winding transformer and multiple diode bridge rectifiers. The multi-winding transformer has identical turns on the secondary windings to ensure the same ratio from the primary side to secondary side. The supercapacitor voltages are controlled by their own diode bridge rectifiers. The equalization current in the circuit flows through the lowest voltage supercapacitor in the string. This is because when the rectifier diodes in the bridge rectifiers for the lowest voltage supercapacitor conduct, the voltage of the lowest

voltage supercapacitor is applied across all secondary windings. For the other secondary windings, their voltages are less than their corresponding supercapacitor voltages, resulting in the blockage of rectifier diodes. When the lowest voltage supercapacitor reaches the voltage level of the second lowest supercapacitor, the rectifier diodes associated with these two supercapacitors are turned on to allow equalization current to flow through these two supercapacitors. The analogy can be extended for many supercapacitors in the string. There are four operation modes involved in the circuit. The circuit operation is explained in the following paragraphs.

In mode 1, illustrated in Figure 2.18, switch Q_1 is turned on and there is an inductor current flowing through Q_1 into the dot of the primary winding and thus a positive voltage is applied to the primary winding of the multi-winding transformer. For a single unit such as SC_1, diodes D_{1a} and D_{1d} in the diode rectifier are forced to turn on to allow the secondary reflected current to flow into supercapacitor SC_1. The magnetizing inductor current on the primary winding increases gradually and supercapacitor SC_1 is charged.

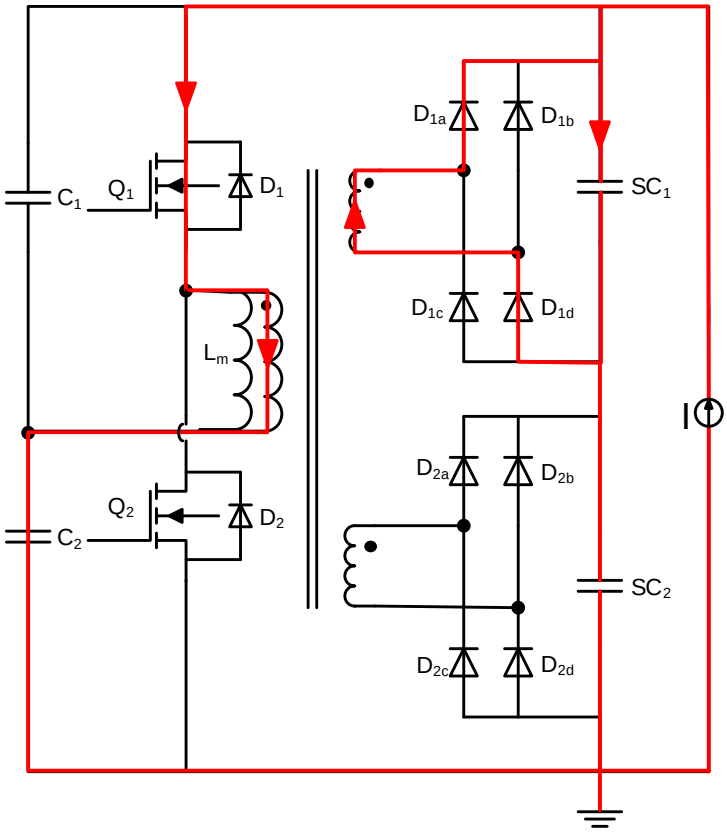

Figure 2.15 Operational process of half bridge multi-winding transformer topology. Mode 1: circuit operation when Q_1 is on.

In mode 2, illustrated in Figure 2.18, switch Q_1 is turned off. However, diodes D_{1a} and D_{1d} in the diode rectifier continue to conduct, which results in the commutation of the magnetizing inductor current. Since the magnetizing inductor current cannot change direction instantaneously, it freewheels through the body diode of switch Q_2. The current reflected from the primary side still charges the corresponding supercapacitor SC_1. At the end of this energy exchange process, the magnetizing inductor current returns to zero.

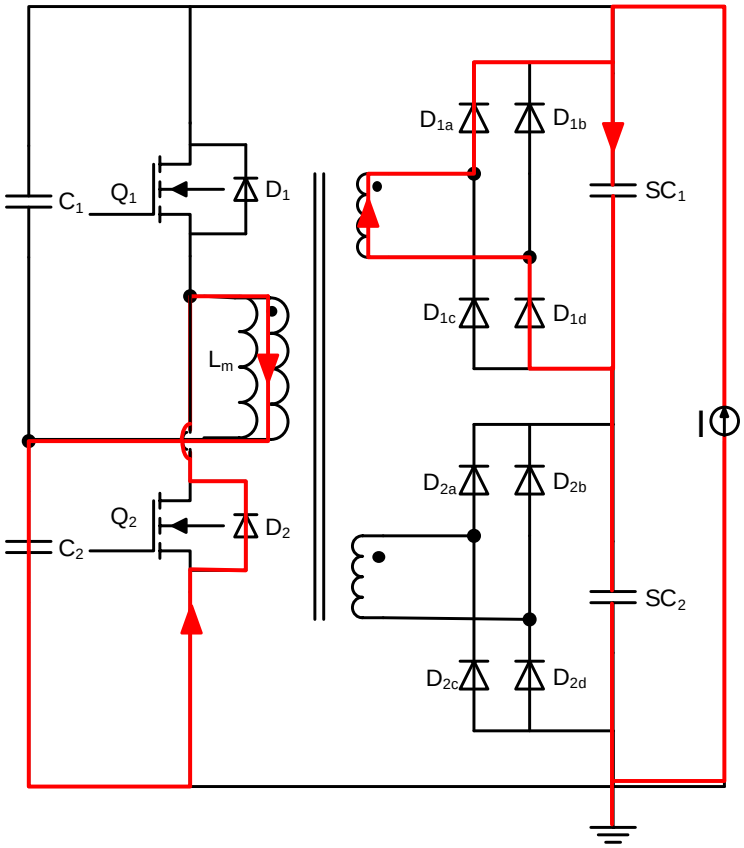

Figure 2.16 Operational process of half bridge multi-winding transformer topology. Mode 2: circuit operation when D_2 is on.

In mode 3, illustrated in Figure 2.17, switch Q_2 starts to conduct. Since the magnetizing inductor current becomes zero, Q_2 conducts. The magnetizing inductor current flowing through Q_2 comes out of the dot of the primary winding and thus a negative voltage is applied to the primary winding of multi-winding transformer. Therefore, diodes D_{1b} and D_{1c} are forced to conduct to allow the current reflected from the primary side to provide charge to the corresponding supercapacitor SC_1. At the end of this energy exchange process, the magnetizing inductor current reaches its negative peak value.

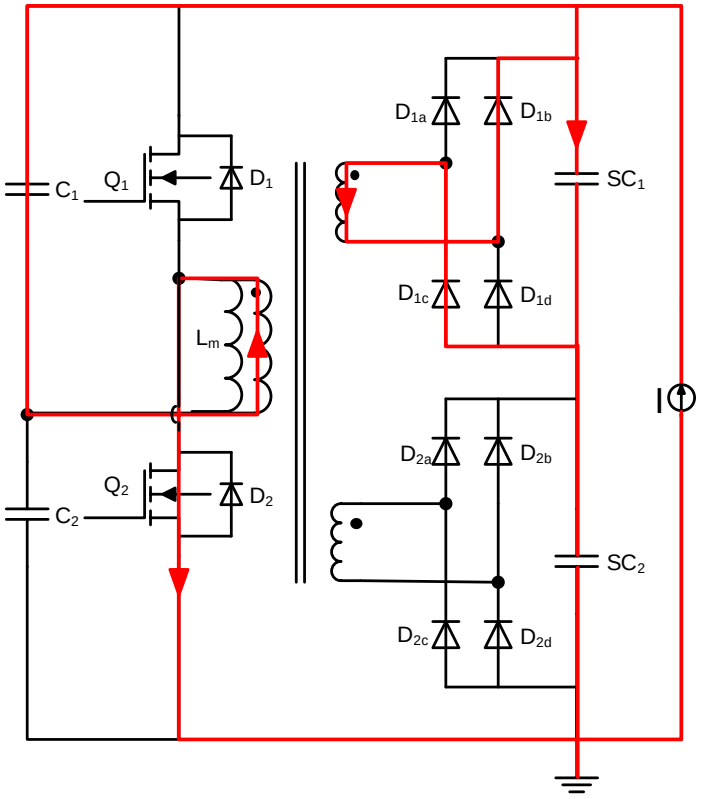

Figure 2.17 Operational process of half bridge multi-winding transformer topology. Mode 3: circuit operation when Q_2 is on.

In mode 4, illustrated in Figure 2.18 , switch Q_2 turns off. However, diodes D_{1b} and D_{1c} in the diode rectifier continue to conduct. The magnetizing inductor current freewheels through the body diode of switch Q_1. The current reflected from the primary side charges the corresponding supercapacitor. At the end of this energy exchange process, the magnetizing inductor current returns to zero to allow zero voltage switching for switch Q_1 in the next switching cycle.

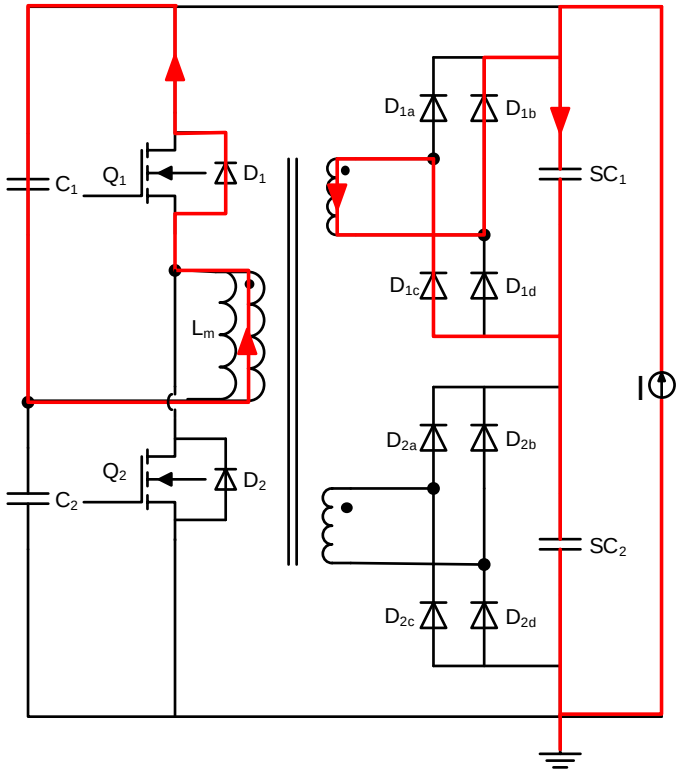

Figure 2.18 Operational process of half bridge multi-winding transformer topology. Mode 4: circuit operation when D_1 is on.

The major advantage of this topology is that there is a relatively low number of switches. Furthermore, it can achieve voltage equalization in a relatively short time without the need for voltage detection circuits. However, the multi-winding transformer needs to be customized specifically in order to satisfy different configurations of series connected supercapacitors. Lastly, the circuit is extremely large when one hundred or more supercapacitors are connected in series.

2.9 Summary

In this chapter, a comprehensive review of recent supercapacitor voltage balancing circuit topologies was presented. These topologies are used to provide a solution for the voltage imbalance of supercapacitors in the applications of electric vehicles applications. Although the

shunting resistor approach has a relatively simple structure and low cost and has been commonly used in vehicles already, it is unappealing since the equalization circuit dissipates excess energy in the circuit. In addition, very high thermal energy generated by the resistors reduces the lifetime of the supercapacitors. Therefore, several inductor and capacitor based circuits were presented, including single inductor converters, a bi-directional Cûk converter, a single switch voltage multiplier, a buck-boost shunting converter and several transformer based topologies, including the selective flyback transformer and half-bridge multi-winding DC-DC converters. These converters have the advantages of relatively fast voltage equalization speed and high efficiency. However, the relative costs and sizes of circuit package prohibit them from application in electric vehicles.

Chapter 3: Proposed Series Resonant LC Voltage Balancing Converter

3.1 Overview

This chapter provides an outline of the proposed topology for the voltage equalization of supercapacitors. The chapter is arranged as follows. In Section 3.2, the major design constraints for developing new voltage equalization methods are explored. In Section 3.3, motivations for designing the new prototype are explained. In Section 3.4, the design of the new topology is presented along with a circuit analysis. In Section 3.5, an analysis of the circuit operation is presented. In Section 3.6, the voltage and current stress for different levels of switches are analyzed and evaluated. The conclusions are presented in Section 3.7.

3.2 Design Constraints

Before designing a new voltage equalization converter, there are factors and constraints that need to be taken into account in order to achieve optimal performance and desired characteristics which include small package size, low cost, low weight, no need for customizing transformers for an arbitrary number of cells, a high degree of extendibility,and a fast voltage equalization speed. Correspondingly, the demerits consist of large package size, high cost and weight, complicated customized transformers for anarbitrary number of cells, lack of extendibility, and long voltage equalization time. Although some of the existing topologies reviewed in Chapter 2, have some of the above mentioned desired characteristics, each has drawbacks as well.

3.3 Motivation for Topology Design

The size of the voltage equalization converter circuit package is a critical issue in electric vehicle applications. Generally, transformer-based converters have a larger size than non-

isolated converters. Capacitor-based converters typically have smaller package sizes, but the voltage equalization process is sluggish, i.e. typically 5 hours [37]. In order to design a voltage equalizer with relatively smaller size and faster voltage balancing speed, inductive elements can be added to capacitor-based converters. Since sizes of reactive components can decrease by increasing the switching frequency, the optimal strategy to reduce the size of the entire package for voltage balancing circuits is to increase the switching frequency of the circuit. However, when switches are operating at high frequencies, switching losses become significant. This results in lower energy efficiency of the circuit, and therefore less energy is recovered from high voltage cells to transfer to low voltage cells. In order to lower switching losses in the circuit, resonant circuits can be used.

Resonant converters have been used in various applications such as switch mode power supplies and power factor correction circuits. A resonant converter includes a resonant tank which consists of inductors and capacitors. The benefits of resonant converter include its high efficiency, reduced volume of inductive elements and reduced electro-magnetic interference (EMI) effects. A resonant circuit can be operated in three frequency ranges, at the resonant frequency, above the resonant frequency or below the resonant frequency.

Nearly lossless, soft switching is a key benefit of resonant converters. Zero voltage switching and zero current switching are two types of soft switching. To achieve zero current switching, the switching frequency must be below the resonant frequency, where the capacitive impedance dominates the circuit. When the circuit is operating at a switching frequency above the resonant frequency, the inductor current lags the resonant tank voltage of the circuit. Therefore, the lagging current can discharge the switch parasitic capacitances down to zero volts before the switch is turned on, allowing for the current to flow with zero voltage and

hence achieve zero voltage switching. This means that the sinusoidal waveform of the inductor current lags the fundamental portion of the square waveform of the voltage. Hence, there is almost no switching loss generated during the turn on of MOSFET switches.

3.4 The Proposed Voltage Equalizer Circuit

The proposed series LC resonant voltage equalizer is illustrated in Figure 3.1. This voltage equalizer consists of a series LC resonant converter which is connected to each supercapacitor in the string (SC_1, SC_2… SC_n) by a group of four switches. MOSFET switches are used in the proposed topology because of their capability of high frequency operation and easy usage.

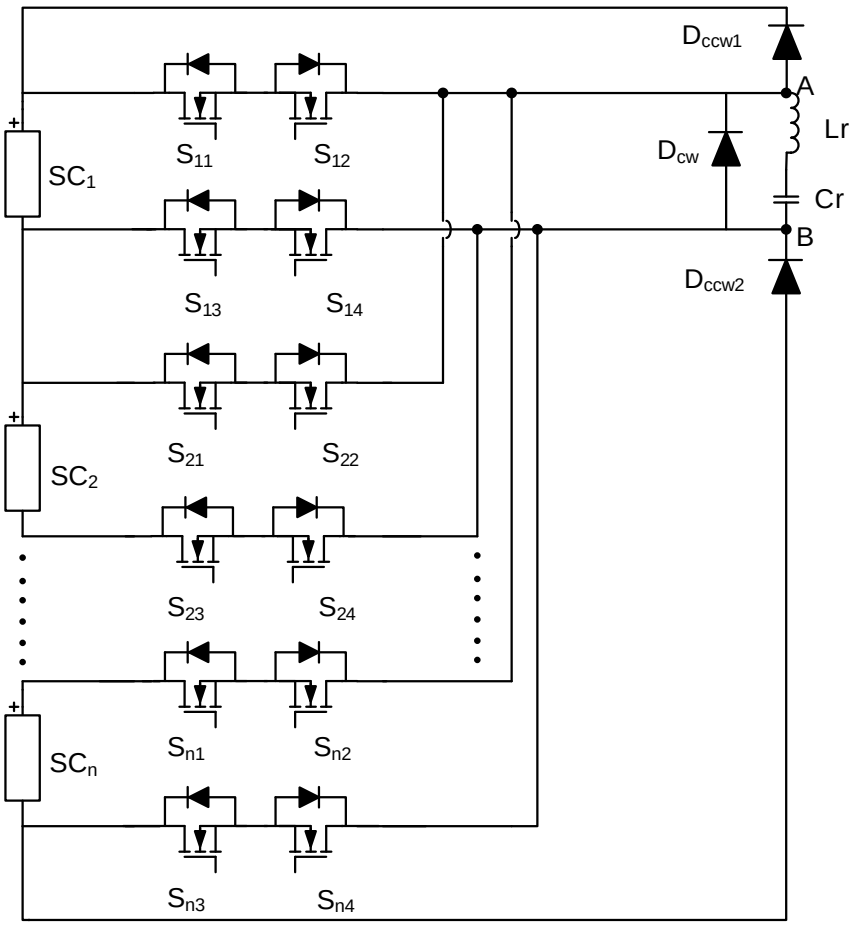

Figure 3.1 Proposed supercapacitor voltage equalization converter

During the voltage balancing process, the group of four switches corresponding to each supercapcitor cell can provide bidirectional energy paths which effectively reduce the voltage equalization time. The two series connected switches in each circuit level are source connected. This is because all the switches at different circuit levels should be triggered on and off by different isolated gate drivers. If all the switches are connected in the manner that the drain of one switch is connected to the source of another switch, the total number of isolated gate drivers will increase significantly. The common source connection of switches renders the usage of only one isolated gate driver on each circuit level. The gate signal from a single gate driver can be applied to the gate of two switches simultaneously, triggering them on and off, thereby providing an energy flow path. The anti-series switches are used to prevent body diode conduction since low voltage MOSFETs cannot block a negative voltage due to the MOSFET intrinsic body diode. Lastly, three diodes D_{cw}, D_{ccw1}, $D_{ccw2,}$ are configured in series and parallel with the LC resonant tank in order to provide a continuous flowing path for the resonant inductor current.

In the existing solutions, excessive capacitor energy is successively transported up the string of series supercapacitors from one to the next, which increases balancing time and leads to the potential for over-voltage on an intermediate cell. However, in the proposed circuit, energy can be transported directly from the source supercapacitor to the target supercapacitor through the single resonant converter. This is because in most practical cases, not all supercapacitors connected in the string have departed voltages from the desired voltage level. Some supercapacitors might have approximately the same voltage as the rated voltage when they are charged and hence, there is no necessity to equalize their voltages. Therefore, only the cells with out of tolerance voltages should have their voltages equalized.

The proposed circuit structure enables supercapacitor voltage equalization selectively by accurate voltage detection. The single LC resonant tank performs the similar function as the transformer in the designs presented in Chapter 2 by providing energy transfer paths among the supercapacitors connected in isolation. In contrast to transformer based schemes, the single resonant tank reduces the converter cost sharply and enables a potentially smaller package. In the case where hundreds of supercapacitors are series connected, the scheme can be conveniently modified by adding additional sets of switches in parallel with existing levels of switches instead of adding extra windings of transformers as in the transformer based topologies.

In order to further minimize the voltage equalization time, the switching frequency is set to be close to the resonant frequency, where the impedance of the converter reaches its lowest value and therefore higher current can be achieved in the energy flow path in each switching cycle. This results in more energy transported in each switching cycle and therefore a shorter voltage balancing time can be expected.

When the higher voltage supercapacitor and the lower voltage supercapacitor are selected in the string by a voltage detection circuit, the switches associated with the higher voltage supercapacitor are triggered on resulting in charge flowing from this supercapacitor to the series LC resonant tank. The resonant tank stores the energy transported from the high voltage supercapacitor temporarily and releases the energy to the lower voltage supercapacitor to increase its voltage in the second phase of the switching cycle.

3.5 Voltage Equalization Operation

Since in the general case, the proposed voltage equalizer only balances the two supercapacitors with the greatest voltage difference, the proposed voltage equalization circuit operation is presented for two cells. The following analysis is conducted assuming that supercapacitors SC_1 and SC_n have voltage values where V_{SC1} is greater than V_{SCn}.

The circuit operation for the proposed converter can be divided into four modes, described in the following paragraphs. The waveforms for all four modes are provided in Figure 3.2.

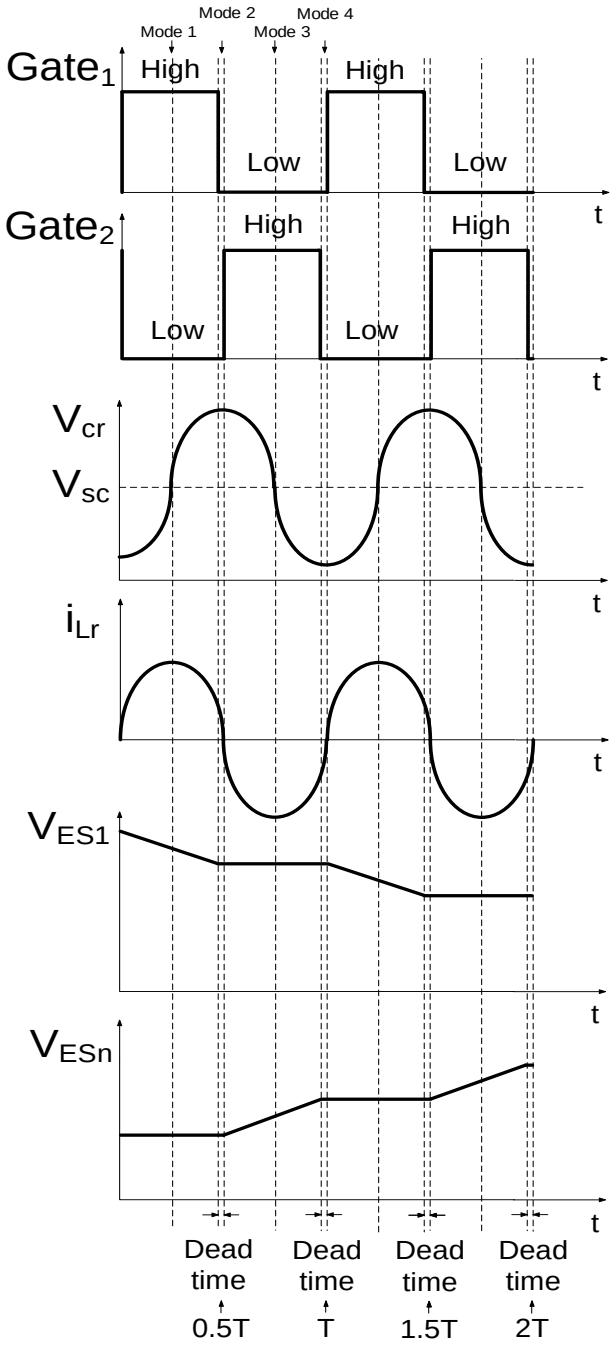

Figure 3.2 Analytical waveforms of resonant capacitor voltage, resonant inductor current and supercapacitor voltages in four modes.

Figure 3.3 illustrates the equivalent circuit during mode 1.

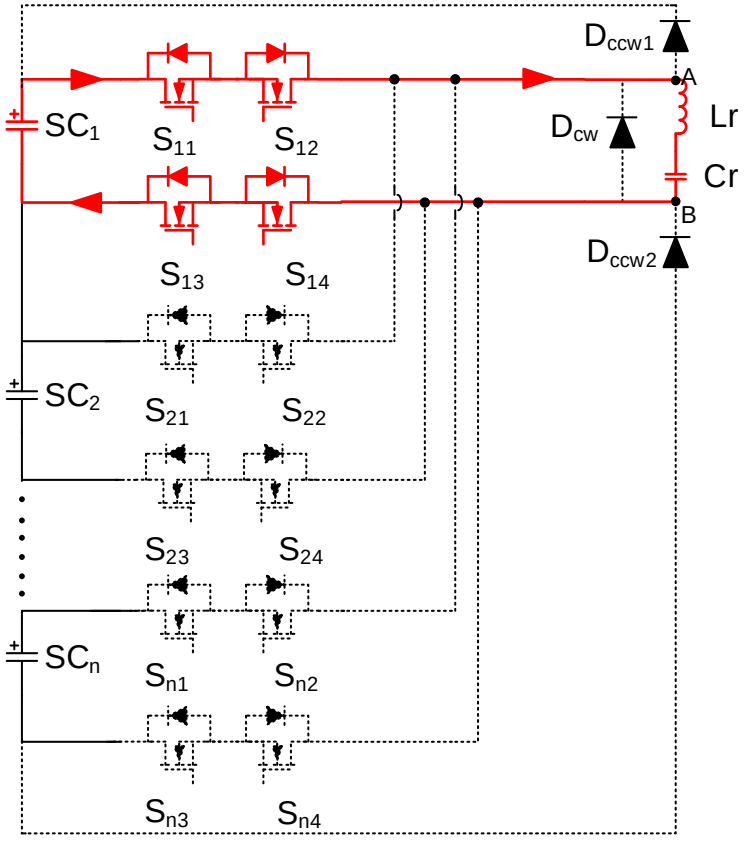

Figure 3.3 Current flowing paths of the proposed converter. Mode 1: Energy transportation from high voltage supercapacitor to LC resonant equalization converter.

During the first half switching cycle, since the voltage of SC_1 is higher than that of SC_n, all four switches associated with SC_1 are turned on.Therefore, SC_1 is connected to the LC resonant tank directly. The charging current flows through the resonant inductor and capacitor, resulting in an increase of the resonant inductor current and resonant capacitor voltage. When the resonant capacitor voltage reaches the same voltage level as the supercapacitor SC_1, the voltage across the resonant inductor becomes zero, and the current flowing through the inductor reaches its positive peak value. After this critical point, supercapacitor SC_1 continues to charge the resonant capacitor and the SC_1 voltage is less than the resonant capacitor voltage. Therefore, the voltage across the resonant inductor is now negative. This negative voltage

contributes to a gradual decrease of the inductor current. At the moment when all the switches connected to supercapacitor SC_1 are turned off, mode 2 begins.

The equivalent circuit during mode 2 is illustrated in Figure 3.4.

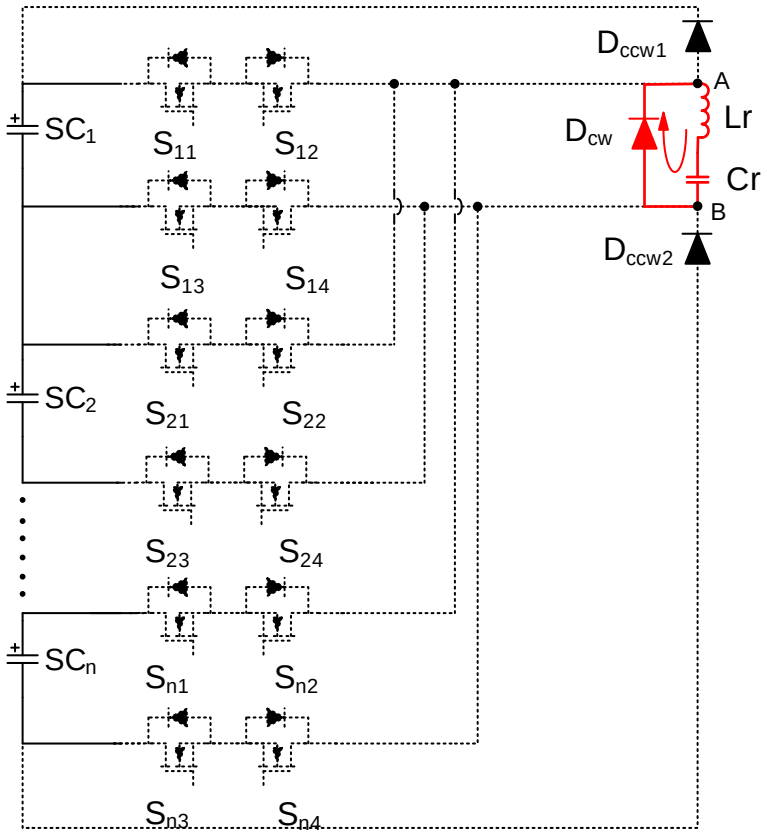

Figure 3.4 Current flowing paths of the proposed converter. Mode 2: Energy flowing paths when resonant inductor releases its stored energy.

In mode 2, since the inductor current cannot change its direction immediately, diode D_{cw} is forced to be on in order to provide a path for the resonant inductor current. When the inductor current returns to zero, the resonant capacitor voltage reaches its positive peak value. The resonant capacitor holds this voltage until the beginning of the next half of the switching cycle, as illustrated in **Error! Reference source not found.**.

The equivalent circuit during mode 3 is illustrated in Figure 3.5.

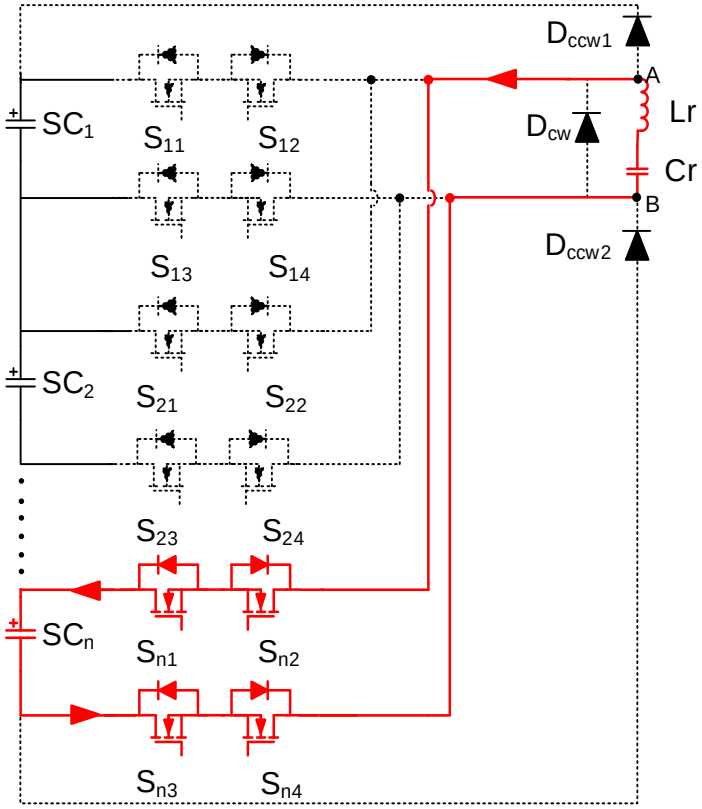

Figure 3.5 Current flowing paths of the proposed converter. Mode 3: Energy transportation from equalization converter to low voltage supercapacitor.

This mode begins when the switches associated with supercapacitor SC_n conduct. During the second half of switching cycle, the energy transport direction is reversed. The resonant capacitor releases all its reserve energy to supercapacitor SC_n. The resonant inductor current flows in the opposite direction, gradually bringing its voltage back to zero. When the resonant capacitor voltage reaches the same level as supercapacitor SC_n, the resonant inductor current reaches its negative peak. Then the resonant capacitor voltage further decreases, resulting in a low current flowing in the circuit. When the switches associated with supercapacitors SC_n are turned off, mode 4 begins.

The equivalent circuit during mode 4 is illustrated in Figure 3.6.

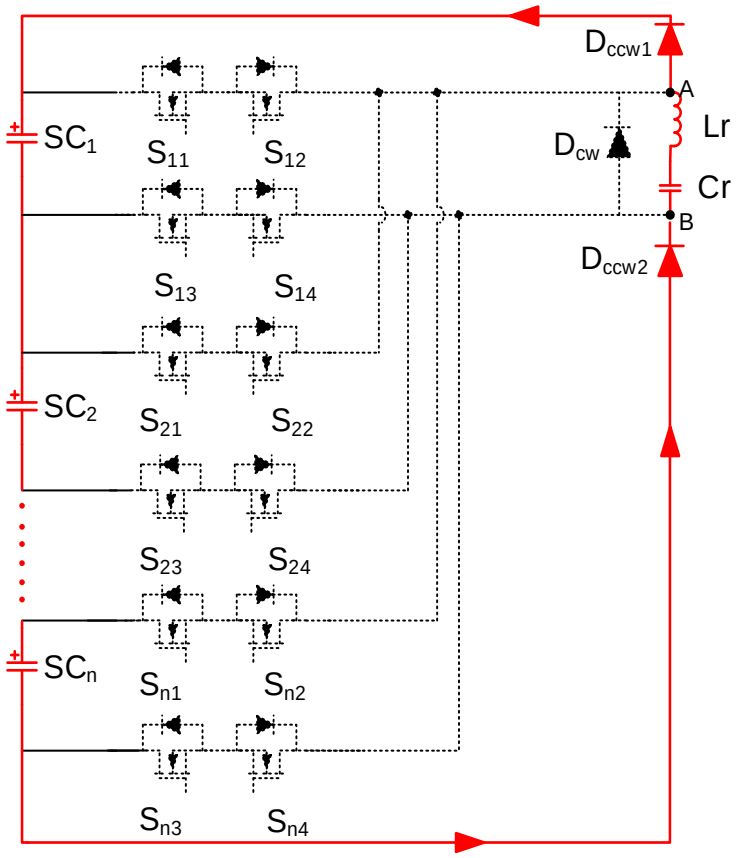

Figure 3.6 Current flowing paths of the proposed converter. Mode 4: Energy flowing paths when resonant inductor releases its stored energy in the opposite direction.

The resonant inductor current still cannot change its direction and therefore it forces the conduction of diodes D_{ccw1} and D_{ccw2}. The resonant inductor current flows through diode D_{ccw1}, the supercapacitor string and diode D_{ccw2} back to resonant capacitor. The analysis of the circuit operation for mode 3 and 4 is similar to the analysis in the first half of the switching cycle, i.e. modes 1 and 2. This energy transport process continues in successive switching cycles until the voltage difference of the two supercapacitors reaches a pre-selected target value.

3.6 Mathematical Analysis of the Proposed Circuit

During a switching cycle, the supercapacitor voltages are changing. However, the voltage variations are small and can be assumed to be constant during one switching cycle. The following analysis assumes that the resistance in the circuit can be neglected.

During the first half of the switching duty cycle, the LC resonant tank is connected to SC_1 in order to receive charge. The voltage across the resonant inductor is the voltage difference between supercapacitor SC_1 and capacitor C_r.

The resonant inductor voltage is given by:

$$L_r \frac{di_r}{dt} = V_{SC1} - V_{Cr} \tag{3-1}$$

The resonant inductor current is given by:

$$i_r = C_r \frac{dV_{Cr}}{dt} \tag{3-2}$$

Combining (3-1) and (3-2), a second order LC differential equation is given by:

$$L_r C_r \frac{d^2 V_{cr}}{dt^2} + V_{Cr} = V_{SC1} \tag{3-3}$$

The general solution for the differential equation is:

$$V_{cr} = A_1 \cos \omega t + A_2 \sin \omega t + V_{sc1} \tag{3-4}$$

The initial condition for the resonant capacitor voltage at the instant t_0 is, $V_{Cr}(t_0) = V_i$, and the initial condition for the resonant inductor current is, $i_r(t_0) = 0$.

Therefore, the terms A_1 and A_2 are given by:

$$A_1 = (V_i - V_{sc1}) \cos \omega t_0 \tag{3-5}$$

$$A_2 = (V_i - V_{sc1}) \sin \omega t_0 \tag{3-6}$$

Substituting these two constants into equation(3-4), the resonant capacitor voltage can be expressed as:

$$V_{Cr} = (V_i - V_{SC1})\, cos\omega t cos\omega t_0 + (V_i - V_{SC1}) sin\omega t sin\omega t_0 + V_{SC1}$$

$$= (V_i - V_{SC1})\, cos\omega(t - t_0) + V_{SC1} \quad (3\text{-}7)$$

The resonant current is given by :

$$i_r = (V_i - V_{SC1})\, C_r \omega sin\omega(t - t_0) \quad (3\text{-}8)$$

In the beginning of the second half of the switching cycle, switches S_{11}, S_{12}, S_{13}, S_{14} are turned off and switches S_{n1}, S_{n2}, S_{n3}, S_{n4} are turned on. In this case, the resonant tank is connected to SC_n instead of SC_1. The stored charge is delivered from the resonant tank to supercapacitor SC_n to increase its voltage. The voltage across the resonant inductor is the voltage difference between supercapacitor SC_2 and capacitor C_r.

Similarly, a second order LC differential equation can be derived as:

$$L_r C_r \frac{d^2 V_{cr}}{dt^2} + V_{Cr} = V_{SC2} \quad (3\text{-}9)$$

The solution for the differential equation is:

$$V_{Cr} = A_1 cos\omega t + A_2 sin\omega t + V_{SC2} \quad (3\text{-}10)$$

The initial voltage for the resonant capacitor at the instant t_1 is $V_{Cr}(t_1) = V_p$, and the initial current for the resonant inductor is $i_r(t_1) = 0$.

Therefore, the constants of the differential solution are given by:

$$A_3 = (V_p - V_{SC2})\, cos\omega t_1 \quad (3\text{-}11)$$

$$A_4 = \left(V_p - V_{SC2}\right) sin\omega t_1 \tag{3-12}$$

Substituting these constants into equation (3-10), the resonant capacitor voltage is given by:

$$V_{Cr} = (V_p - V_{SC2})\, cos\omega t cos\omega t_1 + \left(V_p - V_{SC2}\right) sin\omega t sin\omega t_1 + V_{SC2}$$

$$= (V_p - V_{SC2})\, cos\omega(t - t_1) + V_{SC2} \tag{3-13}$$

The resonant current is given by :

$$i_r = (V_p - V_{SC2})\, C_r \omega sin\omega(t - t_1) \tag{3-14}$$

Based on the above mathematical analysis, it can be seen that when the equalizer starts to compensate voltages, the voltage of the resonant capacitor is its initial voltage V_i. After one quarter of the switching period, the resonant capacitor voltage reaches V_{SC1}, the same voltage level of discharged supercapacitor. When half of the switching period passed, that is, $\omega(t - t_0)=\pi$, the resonant capacitor voltage becomes $2V_{SC1} - V_i$. When $\omega(t - t_1)=\frac{3\pi}{2}$, the resonant capacitor voltage reaches V_{SC1} again.

Therefore, the resonant capacitor has a sinusoidal oscillating voltage waveform with a positive peak value of $2V_{SC1} - V_i$ and a negative peak value of V_i.

3.7 Analysis of the Equivalent Circuit

The equivalent circuit of the charging, or discharging process can be derived as a simple resistor-inductor-capacitor network with a supercapacitor as the main voltage source. Figure 3.7 illustrates the equivalent circuit model.

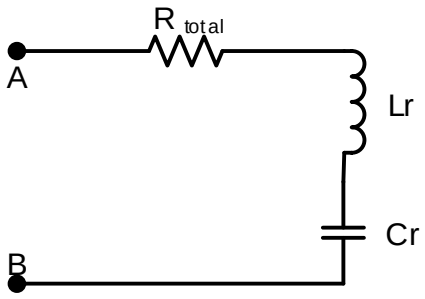

Figure 3.7 Equivalent circuit during energy transportation process.

The impedance of the circuit is given by:

$$Z = R_{total} + jwL_r + \frac{1}{jwC_r} \tag{3-15}$$

where R_{total} is the total resistance of the circuit, which includes the on time resistance of the MOSFET switches, the internal resistance of the resonant inductor, the internal resistance of the resonant capacitor, and the resistance of the supercapacitors. Therefore, the magnitude of the impedance is given by:

$$|Z(f)| = \sqrt{{R_{total}}^2 + (2\pi f L_r - \frac{1}{2\pi f C_r})^2} \tag{3-16}$$

where F is the frequency in Hertz.

Since the resistance, inductance and capacitance are all known parameters with fixed values, the impedance is dependent only on the circuit switching frequency. The impedance of the equivalent circuit can be changed by modifying the frequency of the resonant tank voltage, which is controlled by the frequency of the MOSFET switches supplying the voltage waveform of the supercapacitors to the resonant tank.

3.8 Fourier Analysis of Resonant Inductor Current

When the proposed converter operates, the voltage across the resonant tank is equal to the voltage of the supercapacitors. In the case where Vsc_1 and Vsc_n are applied to the resonant tank separately, the voltage of the resonant tank is Vsc_1 for almost half of the switching cycle and Vsc_n for the other half of the switching cycle, as shown in

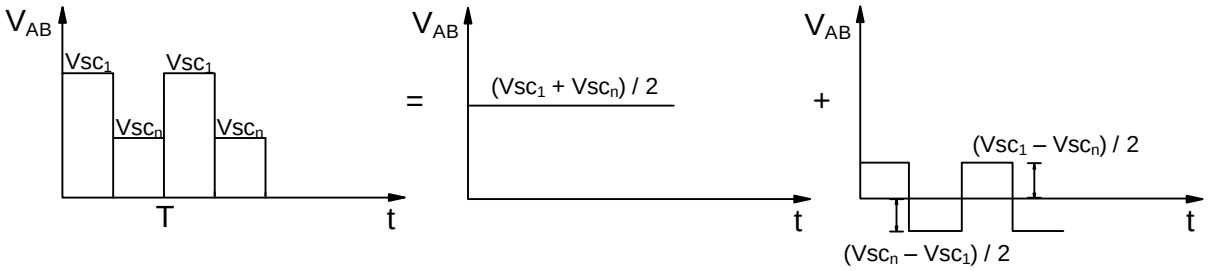

Figure 3.8. A short dead time is added between the switching transitions from the set of switches controlling SC_1 and the set of switches controlling SC_n. This dead time is negligible in the analysis of the equivalent circuit. Therefore, in a switching cycle, a pulsing voltage is applied to the resonant tank. This pulsing voltage consists of two components, one is a constant voltage with its magnitude equal to average voltage of the two supercapacitors, and a square wave with an amplitude that is the same as the voltage difference between the two supercapacitors.

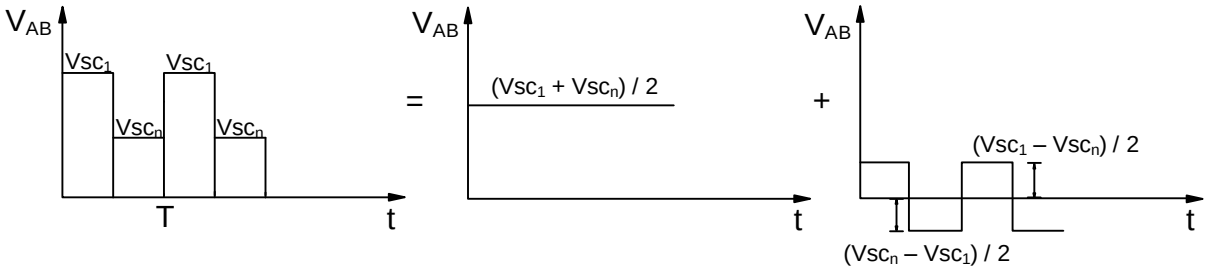

Figure 3.8 Decomposition of resonant tank ladder waveform.

Since the average voltage across the resonant inductor is zero in the steady state, the constant voltage component is solely applied to the resonant capacitor. Therefore, only the square wave voltage is applied to the resonant inductor. Using a Fourier series for the square voltage, it is clear that it consists of a DC component and multiple AC components including a fundamental component at the switching frequency and higher order harmonics, as given by:

$$\mathrm{V(t)} = \mathrm{a_0} + \sum_{\mathrm{n=1}}^{\infty} (\mathrm{a_n} \cos \frac{\mathrm{n2\pi t}}{\mathrm{T}} + \mathrm{b_n} \sin \frac{\mathrm{n2\pi t}}{\mathrm{T}}) \tag{3-17}$$

The coefficient $\mathrm{a_0}$ represents the DC component and can be calculated as:

$$\begin{aligned} \mathrm{a_0} &= \frac{1}{T} \int_0^T V(t) dt \\ &= \tfrac{1}{T} \textstyle\int_0^{0.5T} Vsc_1 dt + \tfrac{1}{T} \int_{0.5T}^{T} Vsc_n dt \\ &= \tfrac{Vsc_1 + Vsc_3}{2} \end{aligned} \tag{3-18}$$

The coefficient $\mathrm{a_n}$ can be calculated as follows:

$$\begin{aligned} \mathrm{a_n} &= \frac{2}{T} \int_0^T V(t) \cos \frac{\mathrm{n2\pi t}}{\mathrm{T}} dt \\ &= \tfrac{2}{T} \textstyle\int_0^{0.5T} Vsc_1 \cos \frac{\mathrm{n2\pi t}}{\mathrm{T}} dt + \tfrac{2}{T} \int_{0.5T}^{T} Vsc_n \cos \frac{\mathrm{n2\pi t}}{\mathrm{T}} dt \\ &= 0 \end{aligned} \tag{3-19}$$

Similarly, coefficient $\mathrm{b_n}$ can be calculated as follows:

$$\begin{aligned} \mathrm{b_n} &= \frac{2}{T} \int_0^T V(t) \sin \frac{\mathrm{n2\pi t}}{\mathrm{T}} dt \\ &= \tfrac{2}{T} \textstyle\int_0^{0.5T} Vsc_1 \sin \frac{\mathrm{n2\pi t}}{\mathrm{T}} dt + \tfrac{2}{T} \int_{0.5T}^{T} Vsc_n \sin \frac{\mathrm{n2\pi t}}{\mathrm{T}} dt \end{aligned} \tag{3-20}$$

$= \frac{2Vsc_1 - 2Vsc_n}{n\pi}$

Although the pulsating voltage waveform is applied to the resonant tank, only a sinusoidal waveform of resonant inductor current appears in the resonant tank since the resonant tank converter acts as a tuned filter and removes all the higher order harmonic components. Therefore, only the fundamental component significantly contributes to the formation of the resonant inductor current waveform and energy transport process. Therefore, only coefficient $b_1 = \frac{2Vsc_1 - 2Vsc_n}{\pi}$ is significant in the analysis. Coefficient b_1 represents the peak value of the inductor voltage. The RMS value of the resonant inductor voltage is given by:

$$V_{rms} = \frac{\sqrt{2}Vsc_1 - \sqrt{2}Vsc_n}{\pi} \tag{3-21}$$

Since the impedance of the circuit is given by (3-16), the peak and RMS values of the resonant inductor current can be derived as given by (3-22) and **Error! Reference source not found.**, respectively. Since all parameters in these two equations are known, the peak and RMS values are easily calculated. These values are significant in the selection of the resonant inductor and MOSFET switches.

$$I_{peak} = \frac{2Vsc_1 - 2Vsc_n}{\pi\sqrt{{R_{total}}^2 + (wL_r - \frac{1}{wC_r})^2}} \tag{3-22}$$

$$I_{rms} = \frac{\sqrt{2}Vsc_1 - \sqrt{2}Vsc_n}{\pi\sqrt{{R_{total}}^2 + (wL_r - \frac{1}{wC_r})^2}}$$

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3.9 Component Stress Analysis

The switches on the different levels within the circuit have the same current stress ratings. The current flowing through each switch equals the current flowing through the resonant tank. However, for the switch voltage stress, special attention should be paid to the top group and bottom group of switches. If there are only three supercapacitors connected in series, most of the switches withstand only one supercapacitor voltage. But for the top level group and bottom level group of switches, they need to withstand the voltages of the series supercapacitors. The voltage stress for the different levels of switches for a three supercapacitor topology is provided in Table 3.1.

Table 3.1 Voltage stress for MOSFET switches in different switch conduction periods

S_{11}, S_{12}, S_{13}, S_{14} turn on	Voltage Stress for S_{21}, S_{22}	Voltage Stress for S_{23}, S_{24}	Voltage Stress for S_{31}, S_{32}	Voltage Stress for S_{33}, S_{34}
	V_{SC1}	V_{SC2}	$V_{SC1}+V_{SC2}$	$V_{SC2}+V_{SC3}$
S_{21}, S_{22}, S_{23}, S_{24} turn on	Voltage Stress for S_{11}, S_{12}	Voltage Stress for S_{13}, S_{14}	Voltage Stress for S_{31}, S_{32}	Voltage Stress for S_{33}, S_{34}
	V_{SC1}	V_{SC2}	V_{SC2}	V_{SC3}
S_{31}, S_{32}, S_{33}, S_{34} turn on	Voltage Stress for S_{11}, S_{12}	Voltage Stress for S_{13}, S_{14}	Voltage Stress for S_{21}, S_{22}	Voltage Stress for S_{23}, S_{24}
	$V_{SC1}+V_{SC2}$	$V_{SC2}+V_{SC3}$	V_{SC2}	V_{SC3}

From the table shown above, general conclusions can be drawn for a case with N series connected supercapacitors.

When top level switches S_{11}, S_{12}, S_{13}, S_{14} are on, the voltage stress for the bottom level switches S_{N1}, S_{N2}, S_{N3}, S_{N4} is (N-1) times the series connected supercapacitor voltage, i.e. (N-1) V_{SC}. When the bottom level switches S_{N1}, S_{N2}, S_{N3}, S_{N4} are on, the voltage stress for the top level switches S_{11}, S_{12}, S_{13}, S_{14} is also (N-1) times the series connected supercapacitor voltage (N-1)V_{SC}.

However, for the rest of the switches, if the series connected supercapacitor number is an odd number and the sequence number counting from the top is less than $\frac{N+1}{2}$, then the stress for that pair of switches is $(N-n)\mathrm{V_{SC.}}$ Otherwise, the stress is $(n-1)\mathrm{V_{SC.}}$ On the other hand, if the number of series connected supercapacitors is even and the sequence number counting from the top is less than $\frac{N}{2}$, then the stress for that pair of switches is $(N-n)\mathrm{V_{SC.}}$ Otherwise, the stress is $(n-1)\mathrm{V_{SC.}}$

3.10 Voltage Equalization Realization Algorithm

In order to equalize supercapacitor voltages in the string, an algorithm is necessary to select which supercapacitors are to be connected to the equalization converter. The voltage equalization control process is illustrated in Figure 3.9. First, the voltages of supercapacitors are measured by voltage measurement devices. Second, the control device arranges the voltages in descending order. Then the process enters into a repetitive loop by selecting the highest voltage and lowest voltage first. If the highest voltage is larger than the rated voltage, then the switches corresponding to the highest voltage supercapacitor and lowest voltage supercapacitor should be activated to redistribute the charge on these two supercapacitors. If the highest voltage is below the rated voltage, then the voltage difference is calculated by the controller. If the voltage difference between the highest and lowest voltage supercapacitors is within an allowable range, e.g. 20mV, then there is no need to equalize the voltages of all the supercapacitors and the voltage equalization process completes. Otherwise, the corresponding switches are activated until the allowable voltage difference is reached.

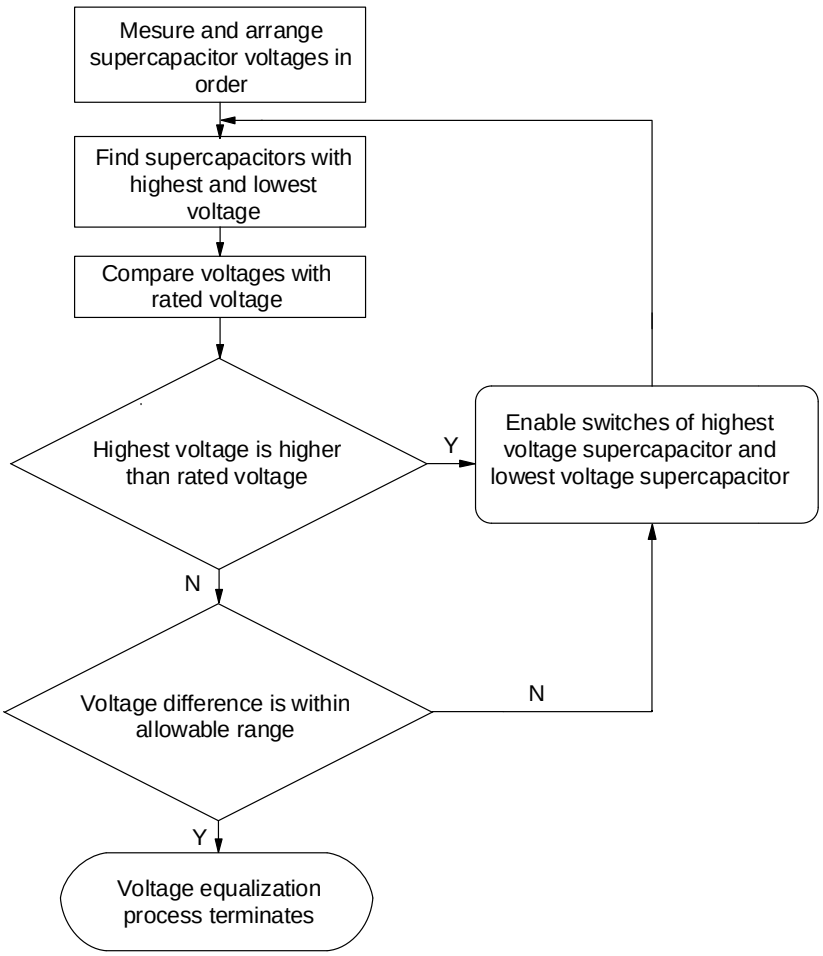


Figure 3.9 Algorithm for voltage equalization process

If three series supercapacitors are used as an example, then the detailed voltage equalization algorithm is provided in Figure 3.10. The allowable voltage difference is set to 10 mV. This example algorithm follows the general process outline in Figure 3.9. The algorithm works to successfully equalize all cells and terminates when all cells are within 10 mV of each other.

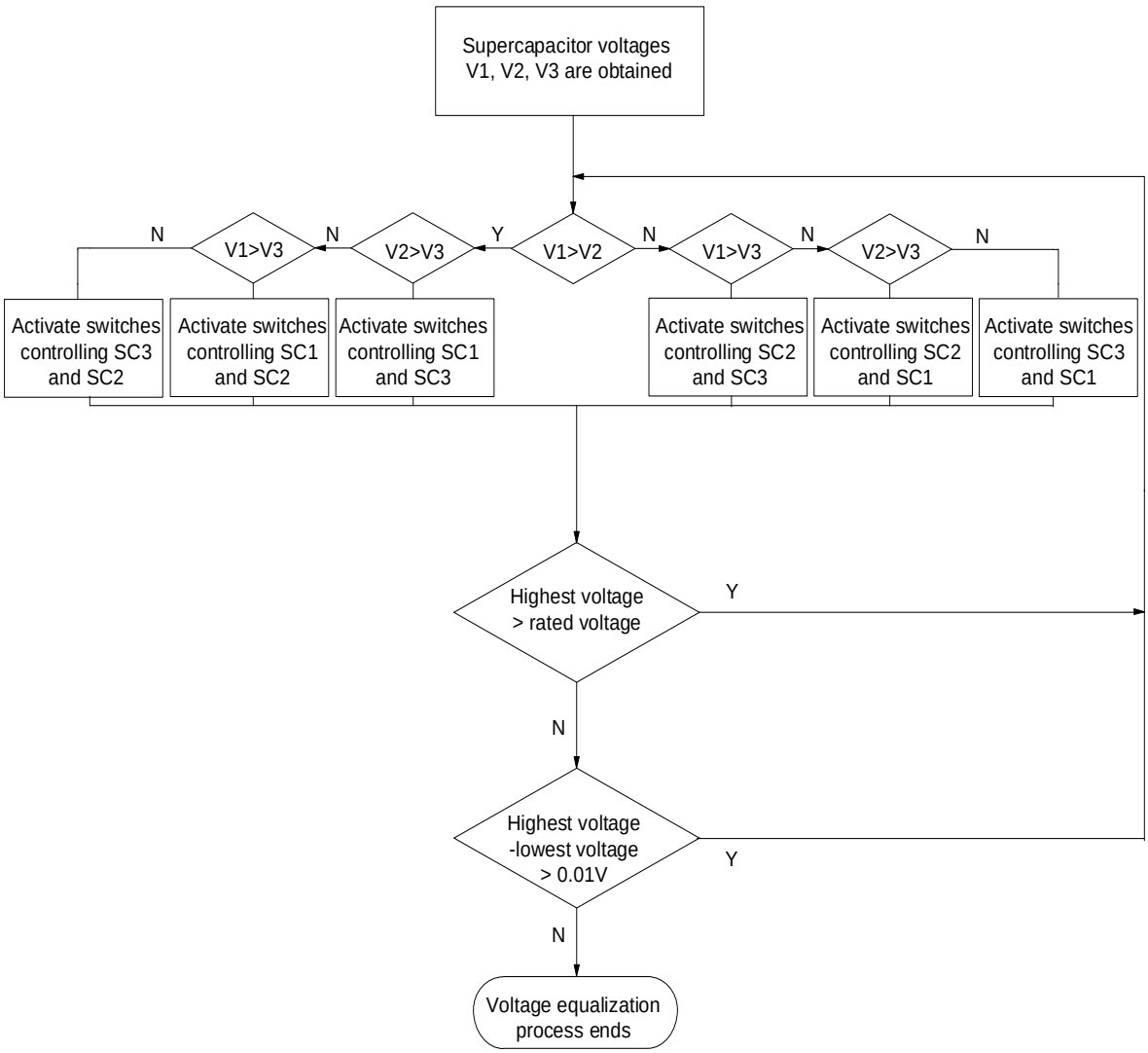


Figure 3.10 Detailed algorithm for the proposed three supercapacitor voltage equalization process.

3.11 Summary

In this chapter, the proposed topology for voltage balancing of supercapacitors has been introduced. A theoretical analysis of the circuit component waveforms in different operational intervals is included. A mathematical analysis based on the equivalent circuit of the proposed converter was developed and a theoretical analysis of the inductor current waveform is included. The voltage stress analysis for each level of switches has also been presented, which is required for MOSFET switch selection.

Chapter 4: Simulation and Experimental Results

4.1 Overview

In this chapter, simulation and experimental results are presented in order to verify the functionality of the proposed voltage equalization converter. The chapter is arranged as follows. Simulation results are presented in Section 4.2. In Section 4.3, the experimental hardware prototype is presented and the components used for the prototype are detailed explained. Experimental waveforms that verify the performance of the converter are presented and evaluated. A conclusion is drawn based on performance of the simulated and experimental waveforms in Section 4.4.

4.2 Simulation Results

In order to verify the validity of the theoretical analysis in the previous chapter, a simulation analysis was conducted using the power electronics simulation software PSIM 9.3.2 from Powersim Technologies. A three-supercapacitor voltage equalization converter system model was built for the topology. The simulation schematic is provided in Figure 4.1. Each of the three supercapacitors had a capacitance of 300 F and the voltages of SC_1, SC_2 and SC_3 were initially set to 2.50V, 2.30V and 2.00V, respectively. The sets of switches were controlled by pulse width modulation signals with a duty cycle of 49% each. In each switching period, only two sets of switches were operated. These two sets of switches were manipulated by complementary signals. A dead time of 1% of the switching period was selected to provide a path for the resonant inductor current between the complementary switching actions. The resonant inductor was selected to be 2.2 µH and the resonant capacitor value was 10 µF. The initial voltage of the resonant capacitor was set to zero. Therefore, the resonant frequency was

33.9 kHz calculated, using $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$. In order to operate near resonance, the switching frequency was set to 34 kHz.

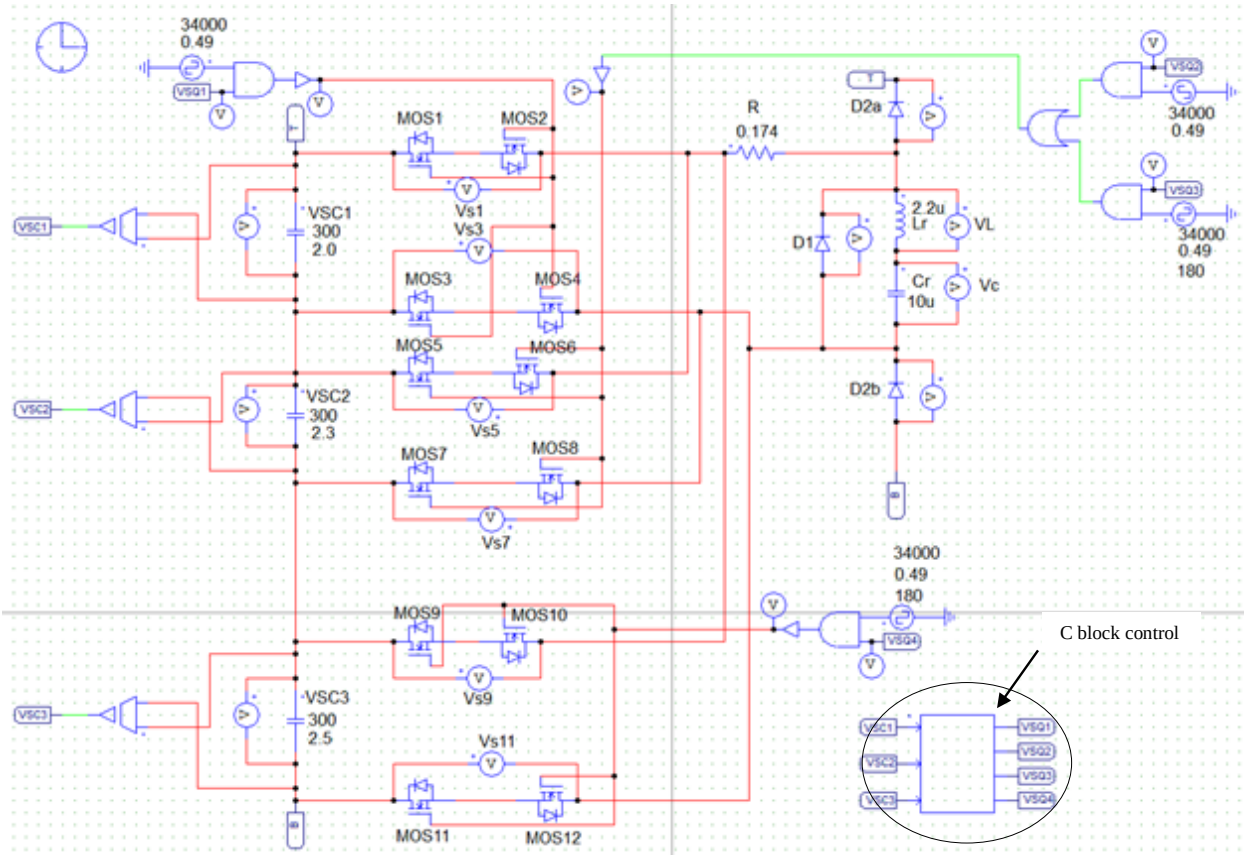


Figure 4.1 Simulation diagram for the three supercapacitor voltage equalization topology.

The simulated waveform for the resonant inductor current is provided in Figure 4.2. As can be observed, the waveform is sinusoidal, which means only the fundamental component in the resonant tank voltage significantly contributes to the resonant current. This matches the theoretical analysis presented in the previous chapter regarding resonant tank voltage Fourier series decomposition. This can be further verified by the Fast Fourier Transform (FFT) of the current waveform, as illustrated in Figure 4.3. In the resonant inductor current FFT results, the fundamental component of resonant inductor current is 1.72 A, while the other odd

components of the waveform including the third, fifth and seventh-order harmonics are 530 µA, 170 µA and 77 µA, respectively. The fundamental component is more than three orders of magnitude higher than the harmonics, and therefore, it is clearly the dominant component.

Figure 4.4 shows the general longer duration (i.e. four switching cycles) changing behavior of the resonant inductor current. The initial peak value of the resonant inductor current is 3.5 A. This peak value gradually decreases cycle by cycle through the rebalancing process. When the voltage equalization process completes, the value of the resonant inductor current is zero, which means there is no charge transport in the circuit, since there is no voltage difference between the supercapacitors.

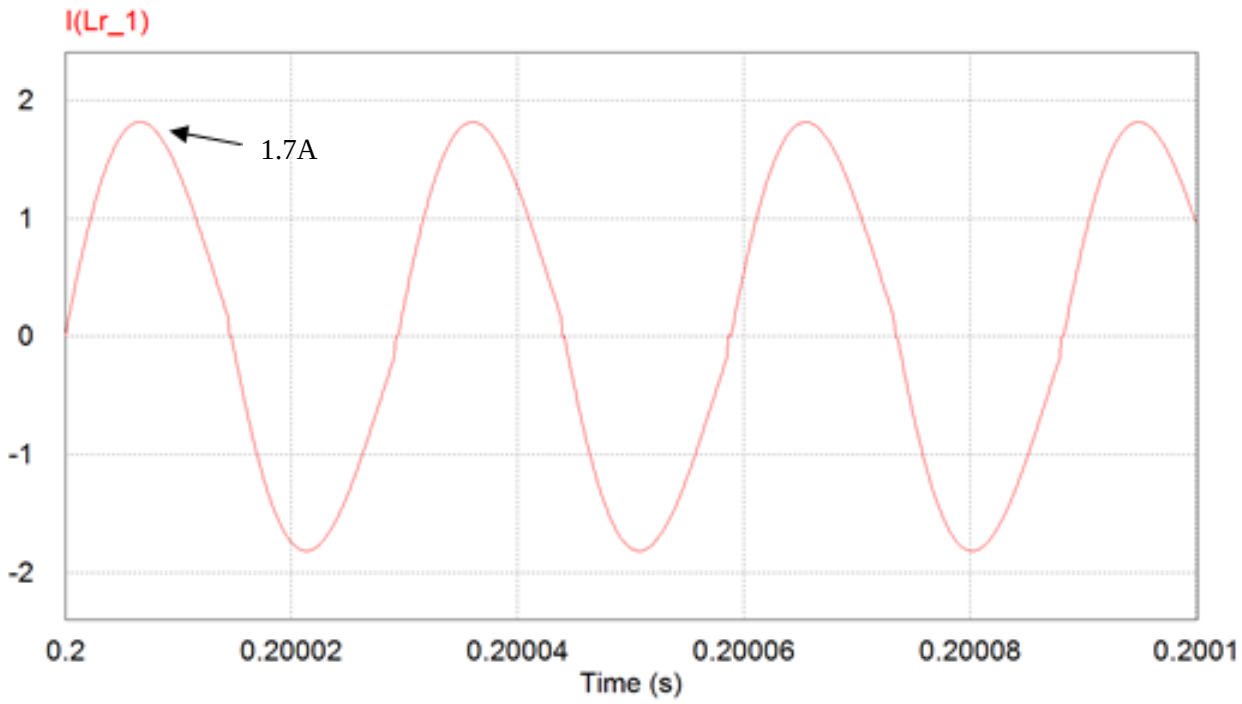


Figure 4.2 Simulation waveform of resonant inductor current.

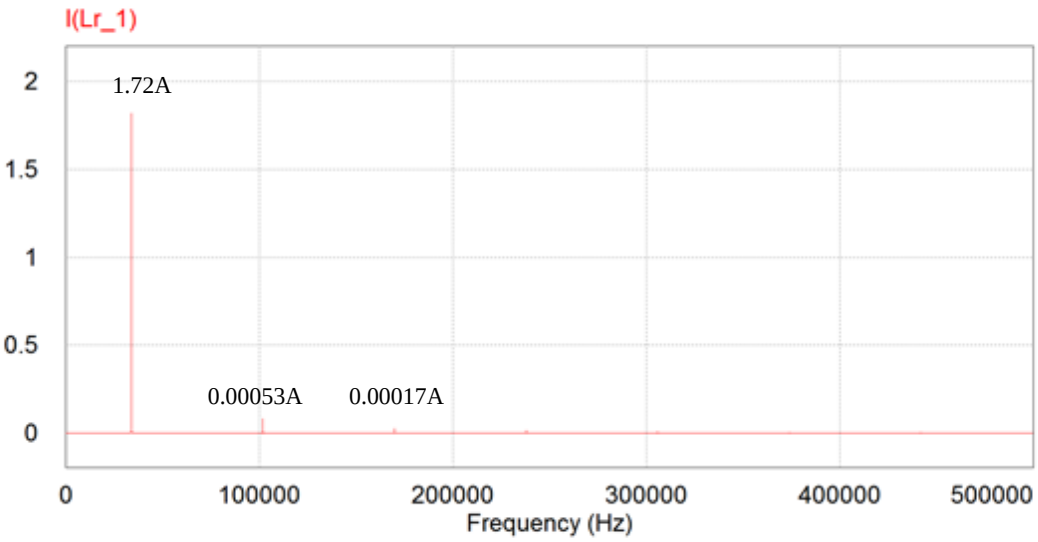


Figure 4.3 FFT analysis of resonant inductor current.

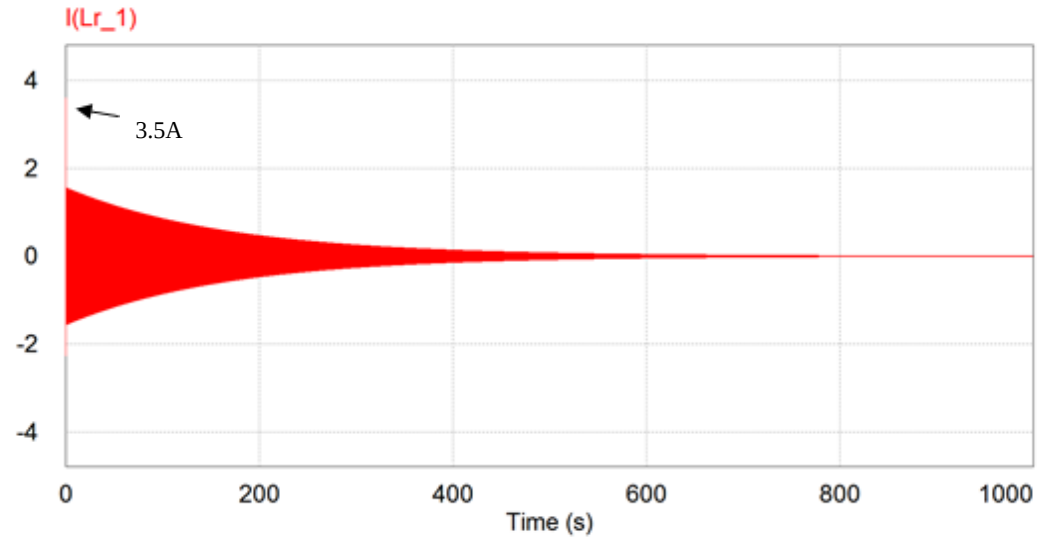


Figure 4.4 General changing behavior of resonant inductor current.

The simulation waveform of the resonant capacitor voltage is provided in Figure 4.5. As can be observed, the resonant capacitor voltage is also sinusoidal with its average voltage being nearly equal to average voltages of all the supercapacitors, which is 2.25V in this example.

The highest and lowest values of resonant capacitor sinusoidal voltage occur exactly when the resonant inductor current reaches zero, as the current leads the voltage by 90 degrees.

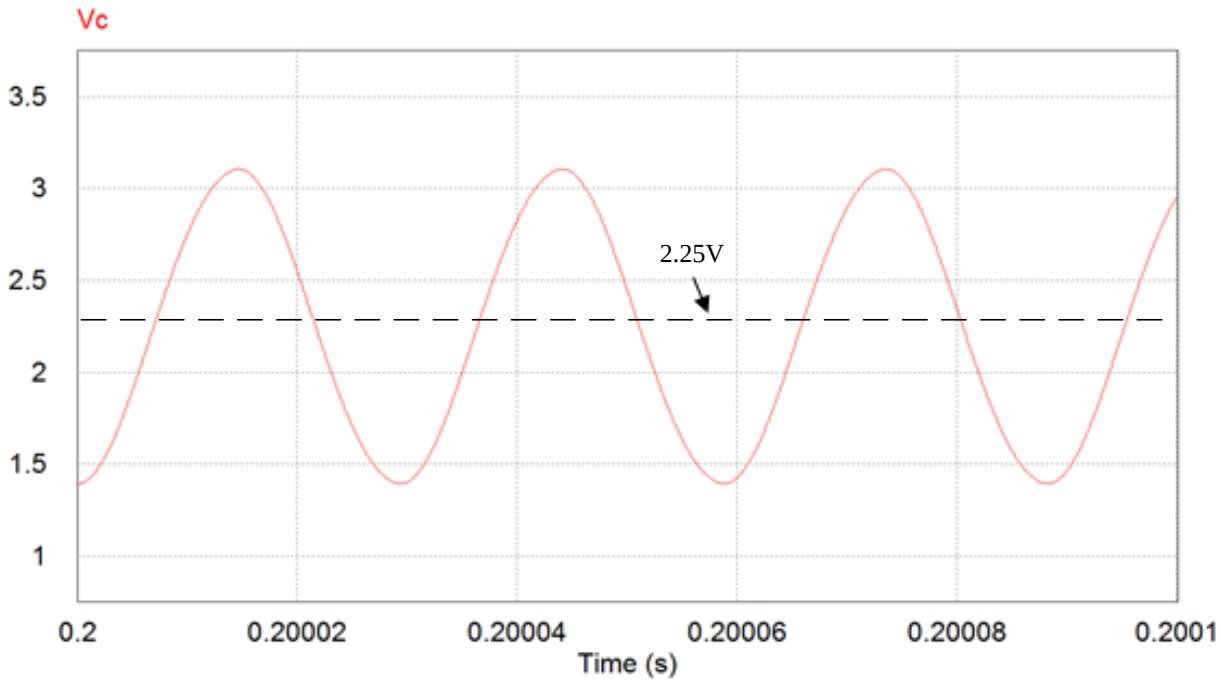


Figure 4.5 Simulation waveform of resonant capacitor voltage.

Figure 4.6 shows the current waveform for two MOSFET switches. As can be observed, since the directional definition of the MOSFET switch current is from drain to source, one of the common source connected switches on the same circuit level has a negative current, but with the same waveform shape and magnitude. The MOSFET switch waveform for the same circuit level switches is only half of the resonant inductor current waveform since they only conduct for half of the switching cycle.

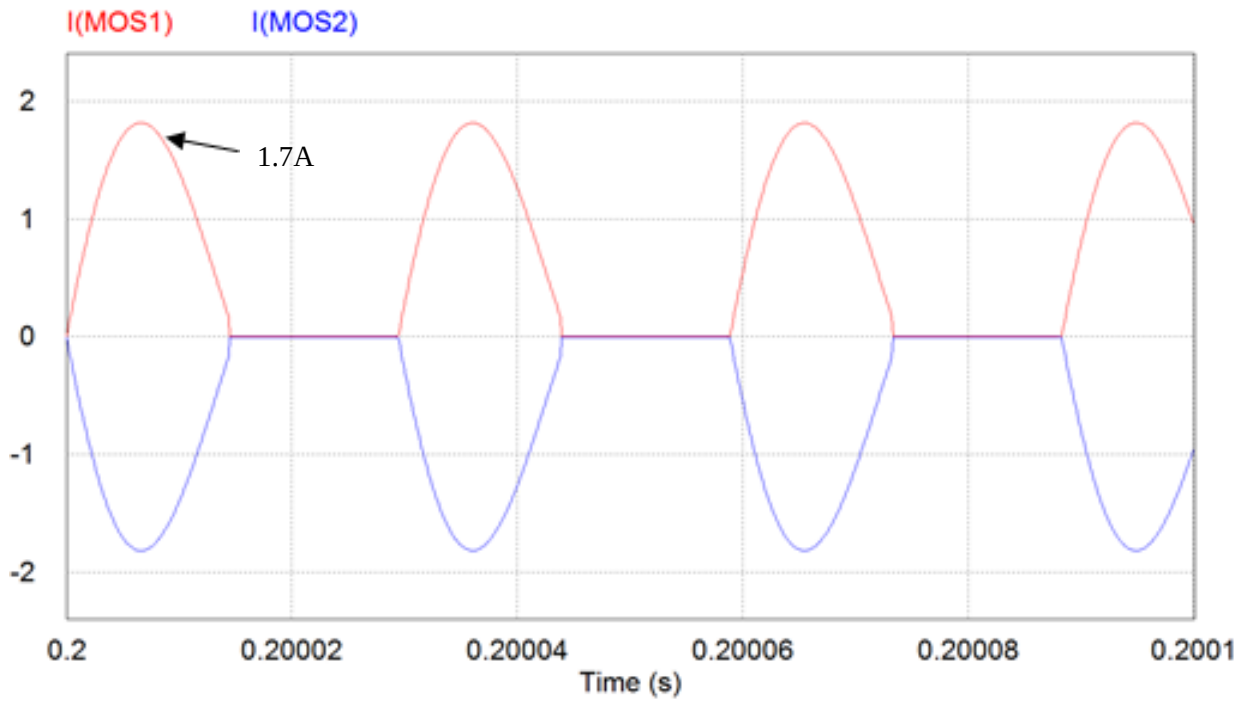
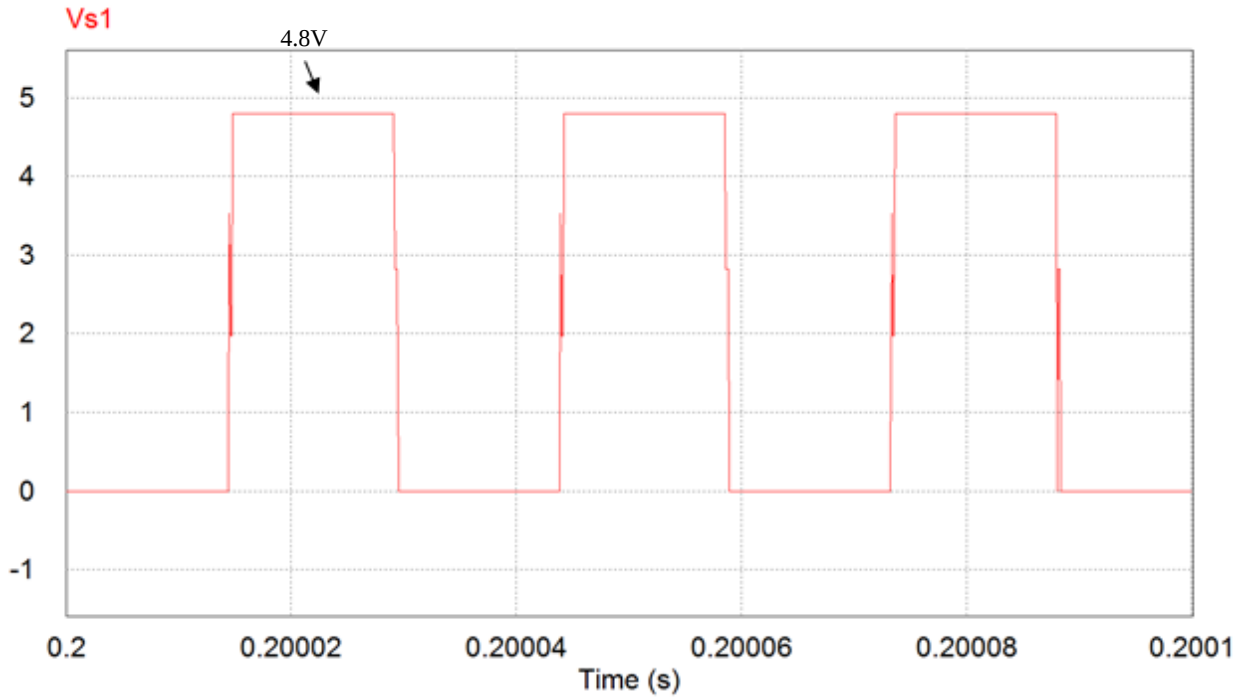
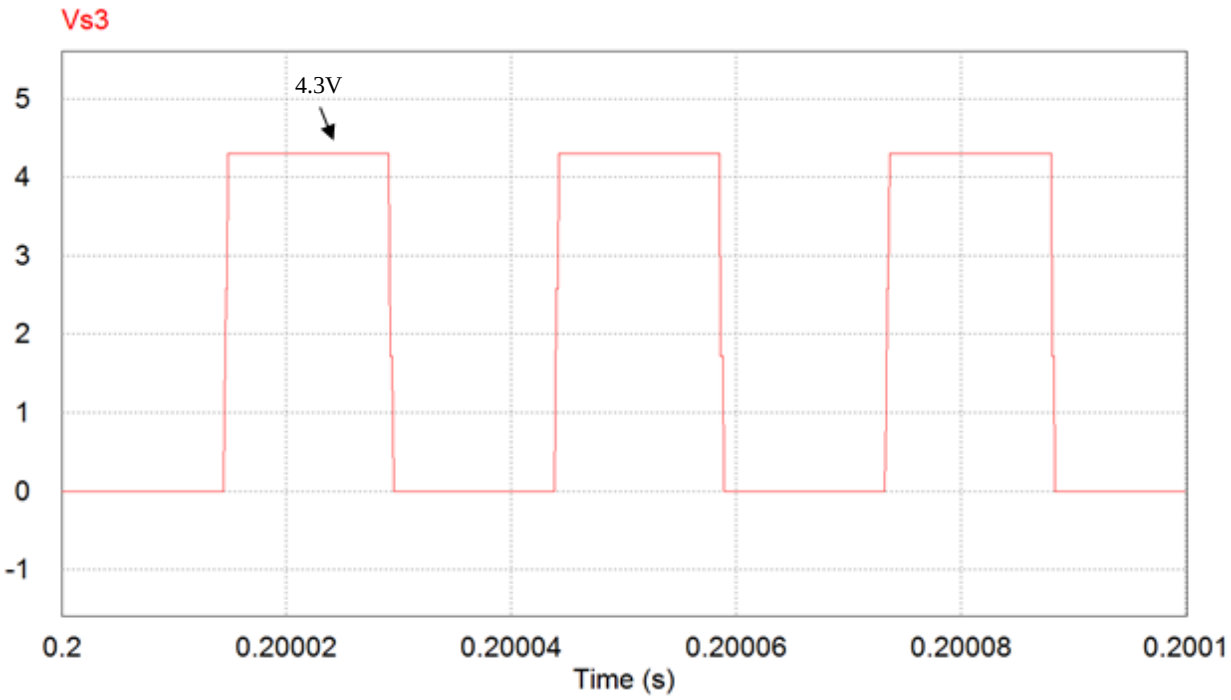


Figure 4.6 Simulation waveform of MOSFET switch current.

Figure 4.7 shows the simulation waveform of the MOSFET switch voltages for the highest and lowest level converters. The voltage across the switches at the higher circuit level is the voltage sum of supercapcitor SC_1 and SC_2, which is 4.8V. The voltage of the switches at lower circuit level is the voltage sum of supercapcitor SC_2 and SC_3, which is 4.3V.



(a)



(b)

Figure 4.7 Simulation waveforms of a single set of MOSFET switch voltages at different circuit level. (a) Voltage waveforms of higher circuit level switches. (b) Voltage waveforms of lower circuit level switches.

The voltage equalization trend is illustrated in

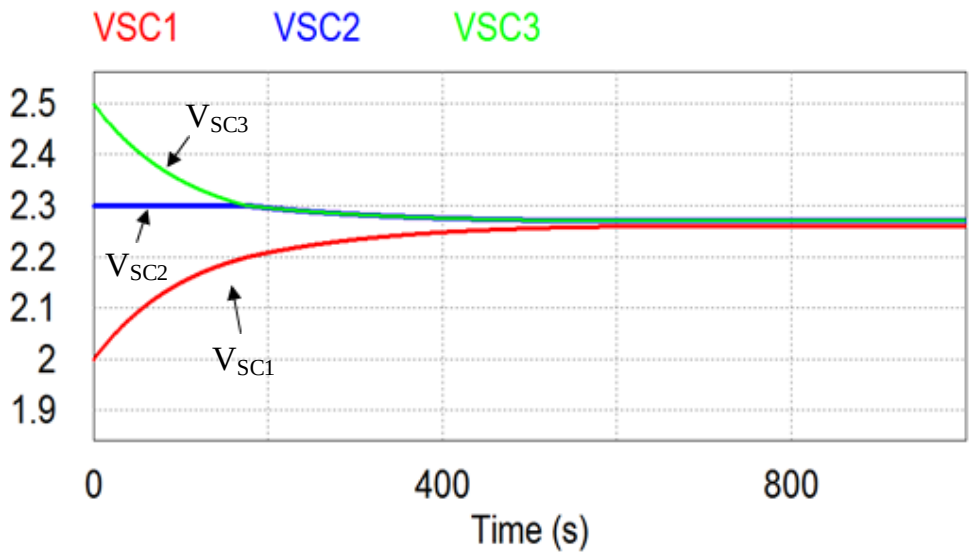


Figure 4.8. The initial voltage difference of 500 mV between the most deviated supercapacitors SC_1 and SC_3 is reduced to 10 mV at 600 seconds.

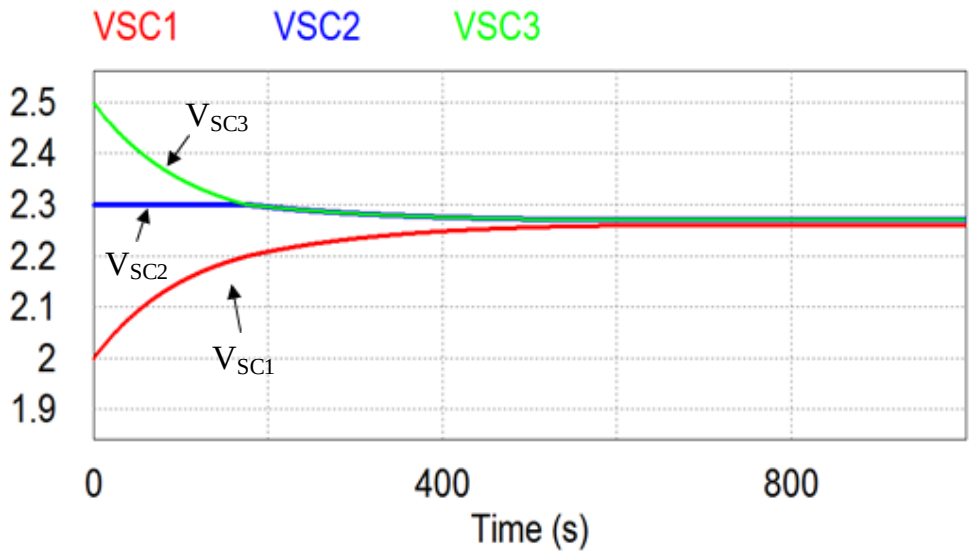


Figure 4.8 Simulation waveform of voltage equalization process.

4.3 Experimental Results

The proposed voltage equalization circuit was built and tested experimentally for three series connected supercapacitors. A photo of the prototype is provided in Figure 4.9. The supercapacitors were assembled on a perforated board and were connected to a printed circuit board using 14 gauge wires. The connectors between the perforated board and the PCB allow a flexible disconnection between charged supercapacitors and the converter board.

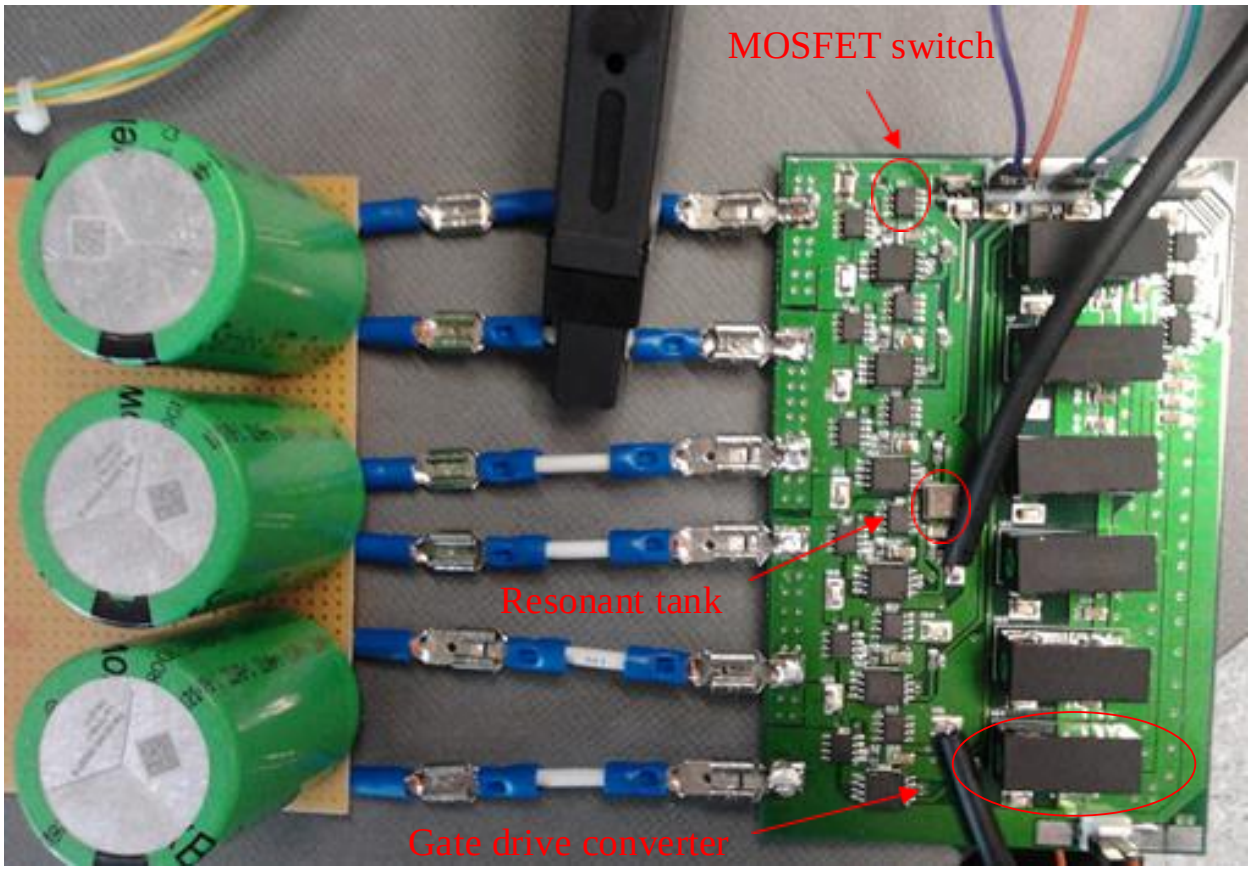


Figure 4.9 Photograph of the proposed circuit board prototype for supercapacitor voltage equalization.

The components were selected using the voltage and current ratings from the simulation results. Table 4.1 shows the key circuit components selected for the prototype.

Table 4.1 Proposed converter component list

Component	Value
Supercapacitor SC_1-SC_n	Cooper Bussman PowerStor capacitors, 300 F
Resonant inductor L_r	2.2 µH (XAL5030MEB)
Resonant capacitor C_r	10 µF (12063D106KAT2A)
MOSFET switches S_{11}-S_{n4}	N-Ch MOSFET switches IRF8721, R_{on} = 8.5 mΩ

Three Cooper Bussman PowerStor supercapacitors, XB3550, were selected because of their low capacitance tolerance of +/- 10%, low equivalent series resistance of 7 mΩ and wide operating temperature range of -25°C to 70°C. The capacitance for each supercapacitor is 300F and the rated voltage is 2.5V. Their surge voltage is 2.85V for 1 second.

For supercapcitor voltage detection, AD629 difference amplifiers from Analog Devices were used. This unity gain difference amplifier can convert differential voltages into single ended signals accurately under very high common-mode voltages. The resonant inductor was selected to be 2.2 µH and the resonant capacitor was 10 µF. For the purpose of the converter performance comparison between simulation results and experimental results, the voltages of the supercapacitors were pre-charged to the same voltage level as the voltages in the simulation. The initial voltages for the three supercapacitors were therefore 2.5V, 2.3V and 2.0V, respectively.

The MOSFET switches used in the design were IRF8721 from International Rectifier. These switches were selected because of their low drain-to-source resistance, $R_{ds,}$ typically 8.5 mΩ and low gate charge, 8.3 nC at V_{gs}= 4.5V. For the N-type MOSFET switches, the threshold

voltage varies between 0.7 and 1V. The MOSFETs can be turned on by applying a gate to source voltage, $V_{gs,}$ higher than the threshold voltage.

For the proposed topology, two MOSFET switches in each circuit level have their sources connected. The drains of the switches are connected to a supercapacitor at one end and the LC resonant tank at the other. This common source connection allows for the use of only one gate drive circuit. The switches connected on different circuit levels have floating grounds. The gate drivers for different circuit levels of switches require different voltage supplies and the reference points of these voltage supplies should be isolated from the sources of the switches they control.

In this design application, since multiple power supplies are undesirable in practice, isolated voltage supplies were used to provide floating gate driver voltages. The isolated voltage supplies are obtained using isolated DC-DC converters, TMR3-1223 from Traco Power. These DC-DC converters provide electrical isolation up to 1500 V. They can be powered by variable input voltages from 9V to 18V and the output voltage of the converters is fixed to 15 V.

For the gate driver selection, the control signals and power signals should be isolated. An ACPL-H312 gate drive optocoupler was selected due to its wide input operating voltage range, high switching speeds and high common-mode rejection voltage. It has high output peak current, up to 2.5 A.

In the circuit, six isolated DC-DC converters were all powered by a DC voltage supply with at 15 V. The outputs of the DC-DC converters were all voltages regulated to 15V, which is within the recommended operating voltage supply ratings of the gate drive optocouplers. A gate resistance was placed between the gate of the MOSFET switch and the output of the gate

driver. Generally, gate resistance cannot be high because switching speed will be limited. However, the gate resistance cannot be too low, otherwise the electrical magnetic interference (EMI) generated can become unacceptably high. The gate resistance was selected to limit the peak gate current below the maximum current of the gate driver. Based on the design specification, the gate resistance was required to be at least 15 V/ 2.5 A= 6 Ω. Using a 50% safety margin, 10 Ω gate resistors were used.

The voltage equalization control circuit was realized by an AVR ATmega328 microcontroller. This microcontroller has an advanced 20 MIPS architecture with six channel, 10-bit analog to digital converter (ADC). In the application of supercapacitor voltage equalization circuit, the voltages of the supercapcacitors have two terminals with positive leads on the top and negative leads at the bottom. Consequently, these double ended supercapacitor voltages should be modified to suit the input of the microcontroller. In the design, the double ended voltages are first converted into single ended voltages using unity gain differential amplifiers. The outputs of the unity gain differential amplifiers were connected to three of the six ADC converter units in the microcontroller, transferring the sensed single-ended signals into the inputs of the ADC converter units. There are also six digital PWM output channels in the microcontroller. Each of the six PWM channels has controllable duty cycles, phase differences, and frequencies.

The main function of the microcontroller is to sense the supercapacitor voltages and then make comparisons between the values of the supercapacitor voltages. When the microcontroller finds the highest voltage supercapacitor and lowest voltage supercapacitor, a decision is made inside the microcontroller regarding which set of MOSFET switches should be operated. If the voltage difference between the highest voltage supercapacitor and lowest

voltage supercapacitor is smaller than 10 mV, the switches in the equalization converter are not required to operate. The microcontroller should apply a command to terminate PWM signal generation. Control signals are generated on the basis of the final decisions made and sent to the inputs of the corresponding gate drivers, allowing the control of the MOSFET switches.

The experimental measured resonant inductor current and resonant capacitor voltage waveforms are illustrated in Figure 4.10 and Figure 4.11, respectively. The waveform for the resonant inductor current is sinusoidal, with zero average value, matching the simulation results. The waveform of the resonant capacitor voltage is also sinusoidal with its average voltage being the average supercapacitor voltage of those being balanced, e.g. 2.25V.

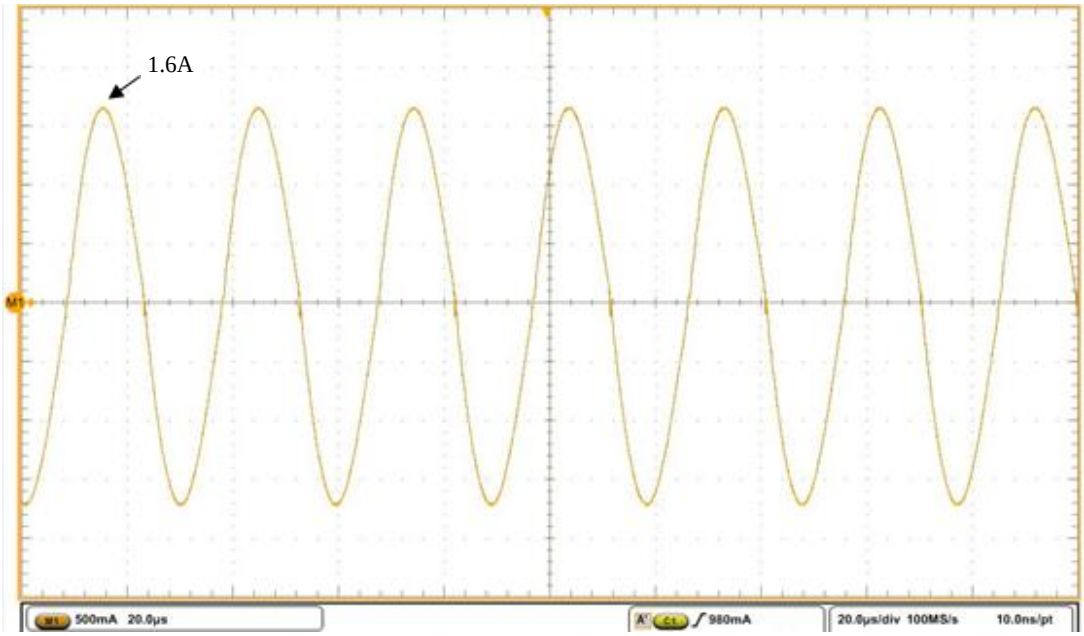


Figure 4.10 Experiment measurement waveform of resonant inductor current during the initial operation of the converter. Current scale = 0.5A/div; Time scale = 20µs/div.

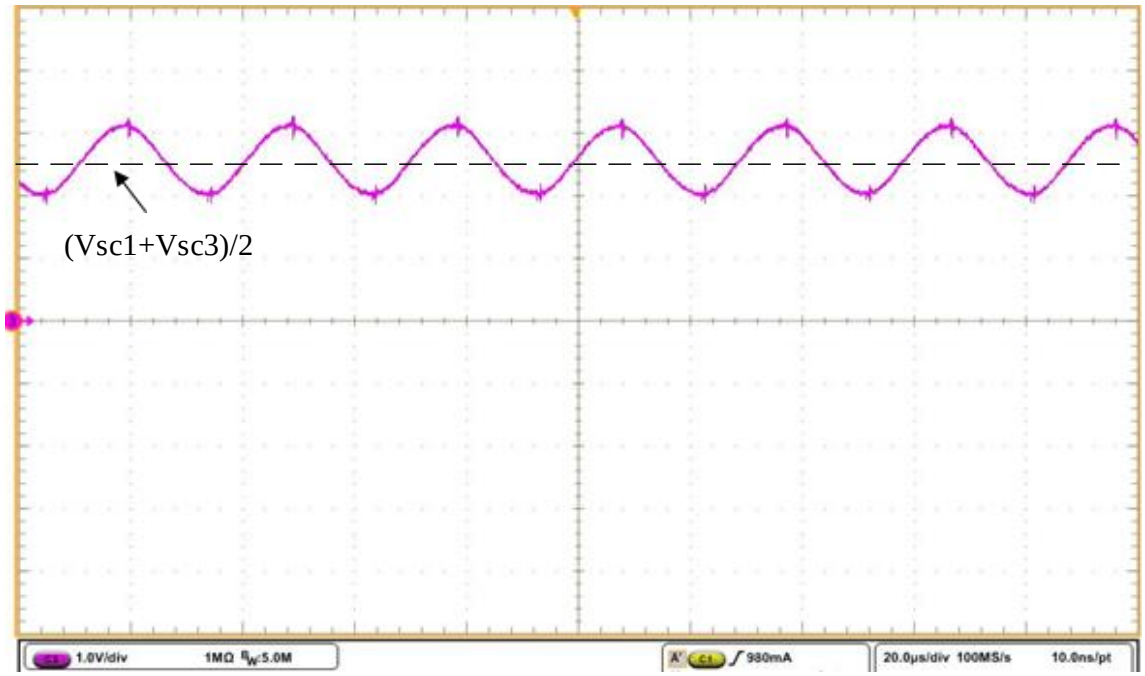


Figure 4.11 Experiment measurement waveform of resonant capacitor voltage during the initial operation of the converter. Voltage scale = 1.0V/div; Time scale = 20µs/div.

Figure 4.12 shows the voltage equalization profile for supercapacitors SC1, SC2 and SC3. The initial largest voltage difference of 527 mV was gradually reduced. The deviation between Vsc1 and Vsc3 was reduced to 10 mV when the voltage equalization process terminated. The total equalization time was less than 15 minutes.

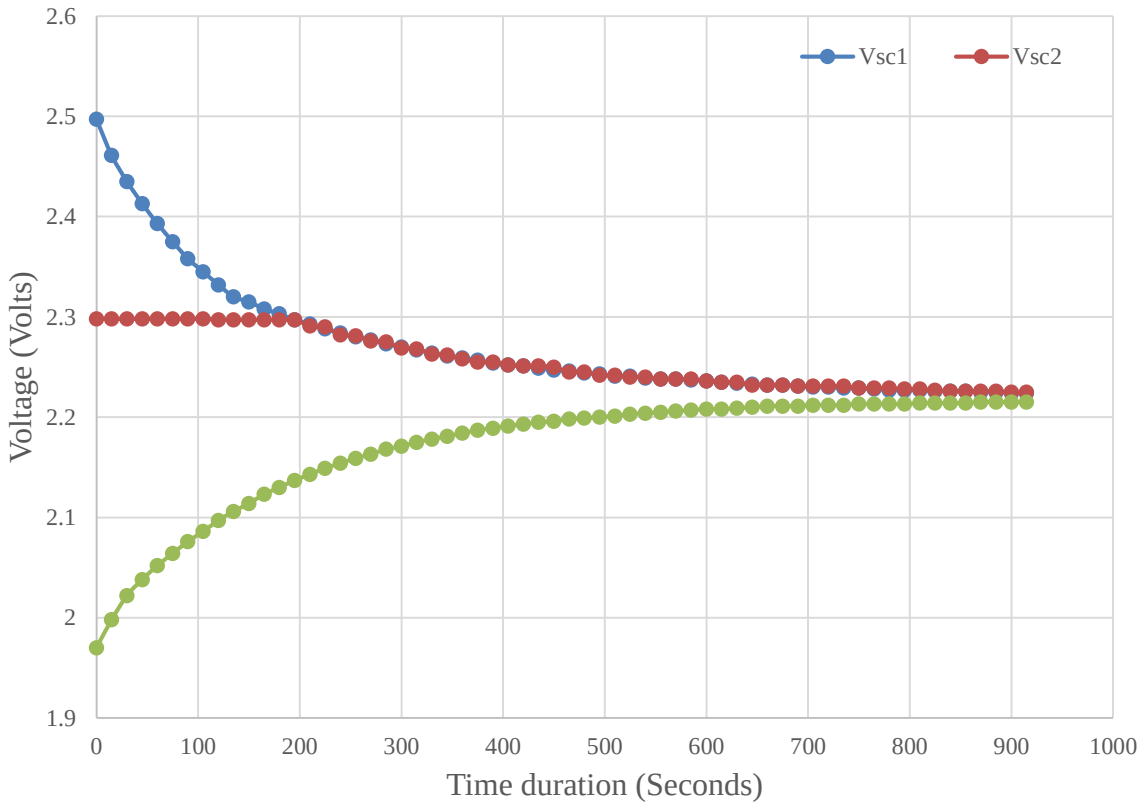


Figure 4.12 Experiment measurement waveform of voltage equalization characteristics

4.4 Summary

In this chapter, simulation results were presented to demonstrate the validity of the theoretical analysis regarding sinusoidal waveforms of resonant inductor current and resonant capacitor voltage. Experimental results were presented for a prototype of a three supercapacitors system, and the components used for building the prototype were described. The experimental prototype was implemented to verify the theoretical and simulation results in the previous and this chapter, respectively. The expected waveforms were achieved therefore showing the correlation between the simulated waveforms and experimental waveforms.

Chapter 5: Conclusions

This chapter summarizes the research presented in this thesis and concludes with suggested improvements for the proposed voltage equalization circuit for future work.

5.1 Research Summary

The demands for new energy sources and improved energy efficiency in the application of electric vehicles has resulted in the development of large capacity batteries and capacitors. In comparison to conventional capacitors, supercapacitors have high energy capacity. Because of their high power density, low internal resistance, excellent dynamic response, infinite charge and discharge cycles and long lifetime, supercapacitors have become increasingly popular in the energy industry.

The technologies used in supercapacitor production have led to extremely high capacitances for supercapacitor cells. The typical value of a commercial supercapacitor can reach up to 3000 F. With improvements in capacitor manufacturing, large value capacitors are expected to become common and low cost. However, capacitor cell voltages are limited to 2.5 V to 2.7 V. The lower voltage of a single cell means that in order to achieve a much higher voltage for real world applications, including electric vehicle drivetrains, it is necessary to connect cells in series. Usually, for the application of a typical electrical vehicle, the voltage rating is around

400 V. Therefore, the total number of series connected supercapacitor cells is more than 100.

However, the capacitance tolerances of each cell affect the uniformity of supercapacitors. Even for capacitors produced at the same time, their capacitance may be different. As a result, the voltage of each supercapacitor varies when charged. Since the cells are usually charged in

series by a constant source, the cells connected in the string with low capacitances have higher voltages, which can lead to the failure of a supercapcitor cell, while the cells connected in the string with high capacitances are charged to a lower voltage which means the entire capacity of the supercapacitor string cannot be fully utilized. Therefore, voltage cell balancing is important for series connected supercapacitor applications.

Currently, the methods of supercapacitor voltage equalization vary. The published methods include passive voltage equalization and active voltage equalization. The passive voltage balancing methods mainly use a simple connection of resistors and switches to dissipate the extra energy received by individual cells. These topologies are appealing in low voltage applications but generally, they have poor efficiency and they are not desirable in high applications, though they are already used in modern transportation industries. Active voltage equalization methods, including the switched capacitor methods and DC-DC transformer-based power converters can achieve voltage equalization with much higher efficiency. The basic principle of voltage equalization for these topologies is to redistribute the energy from one section of the supercapacitor string to the other sections.

This thesis (work) has presented the advantages of some published topologies over others and the corresponding disadvantages. The disadvantages of the mentioned topologies include high relative costs and the relative weight of the components, high voltage and current stress on the switches used, and long voltage equalization time. For most active voltage equalization approaches, the control of the topology is complex. For the single inductor topology, although the cost of the package is lower compared to others, the control of the switches is quite complex. The bi-directional Cûk converter can achieve bidirectional energy flow, but the relative costs of the circuit are high and the control pattern of the switches is also complicated. The single

switch voltage multiplier is appealing due to its low relative cost. However, the diodes used in the circuit produce losses and the speed for the voltage balancing process is low. Furthermore, the voltage and current stresses for the switch and diodes are high. For the buck-boost shunting converter, each cell is connected to a buck-boost converter and therefore it can control supercapacitors independently. However, the switch and diode stresses are relatively high with the increasing number of cells connected in the string. The control patterns of the switches are also complex. The selective flyback converter has a relatively fast voltage balancing speed and the equalization process has high efficiency since the energy is transferred back to the supercapacitor string. However, the topology is a transformer-based converter and therefore its costs are relatively higher compared with transformer-less topologies. The half-bridge multi-winding output DC-DC converter has a lower number of switches, but this converter has a multi-winding transformer needs to be customized specifically to satisfy the arbitrary number of cells. In addition, the size of the topology is extremely large with increasing number of cells connected in a string.

The major motivation of the proposed topology design is to reduce the voltage equalization time, while minimizing losses and not using complicated multi-winding transformers. The proposed topology uses a series LC resonant tank. By minimizing the circuit impedance near the resonant frequency, the proposed circuit topology can equalize supercapacitor voltages quickly be maximizing charge transfer in each switching cycle. The proposed voltage equalization converter only equalizes those supercapacitors which start with very high voltage differences, e.g. 750 mV. The circuit topology has multiple cells in a single converter unit structure, enabling high extendibility. Therefore, the high extendibility renders more adaptability to voltage level variation in industrial applications. In comparison with multiple

voltage equalization units, the single resonant tank also reduces the relative costs and relative size of the circuit package since only two components are required.

Table 5.1 provides a comparison of different topologies in terms of voltage equalization time, relative size and relative cost of circuit packages.

Table 5.1 Performance comparison among voltage equalization topologies

Topology	Specification	Initial Voltage Deviation (mV)	Final Voltage Deviation (mV)	Voltage Equalization Time (Minutes)	Relative Size	Relative Cost
Single inductor converter [31]	4.0 AH Batteries	300	50	20	Medium	Low
Time shared flyback converter [21]	2.65 Ah Batteries	200	50	67	Medium	Medium
Selective flyback converter [35]	1.3 AH Batteries	200	50	90	Medium	Medium
Quasi-resonant converter [38]	10.0 AH Batteries	1000	50	42	Medium	High
Buck- boost shunting converter [34]	4.0 AH Batteries	560	50	45	Medium	Medium
Cuk converter [32]	10.0 AH Batteries	500	50	25	Medium	High
Inductor shunting converter [27]	2.2 AH Batteries	250	50	40	Medium	Low
The proposed converter	300F Capacitors	527	50	7.5	Small	Low

As can be observed from this table, the proposed voltage equalization converter has short voltage equalization time, small relative size, and low relative cost.

PSIM simulation and experimental results were presented in Chapter 4 to verify the validity of the operation of the circuit and the theoretical analysis presented in Chapter 3. A three supercapacitor prototype was built and tested design was presented and the converter successfully balanced two cells starting with an initial voltage difference of 527 mV down to 10 mV in 15 minutes.

5.2 Suggestions for Future Work

Although the conclusions drawn from the analysis regarding the proposed voltage equalization scheme are positive, there are still practical design issues regarding the topology.

The DC-DC converters used for the isolation between different levels of switches are very expensive, which directly increase the cost of the entire package. For future design considerations, small pulse transformers powered by a single DC-DC power converter could be employed to provide a floating switch reference.

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