ACTIVE ADAPTIVE AUXILIARY CIRCUIT FOR STABILIZING DC DISTRIBUTION SYSTEMS WITH CONSTANT POWER LOADS

by

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Abstract

The portion of high-bandwidth power converters in modern DC distribution systems has been increasing and is projected to dominate over time. These devices having fast response act as constant power loads (CPLs) and possess the so-called negative incremental input impedance characteristics at the input terminals, which may ultimately cause dynamic interactions and instability at certain interfaces in the system. Most existing approaches that address this problem use passive or active damping to reshape the source/load impedances so that stability may be achieved. The drawbacks of most existing methods include energy losses in passive components and/or requirement of changing the internal controls in existing loads.

This thesis presents a new active damping methodology using an auxiliary converter circuit to stabilize DC distribution systems with CPLs. A simplified single frequency criterion is proposed for identifying the damping parameters. The proposed auxiliary converter circuit exchanges the energy between very strong power bus and a potentially unstable bus with CPLs, which requires very small injected damping current and achieves lossless damping (conserves the energy during transients). The methodology may operate by emulating fixed or operating-point-depended virtual *RC* values of the equivalent damping, with the latter having potential advantages of achieving faster damping.

To verify and demonstrate the proposed concept, the auxiliary converter circuit has been designed and built with innovative compensated average current control mode. The experimental studies have been carried out on a reduced scale subsystem of a DC microgrid installed by Alpha Technologies Ltd., in Kaiser building at UBC. It is envisioned that the proposed active damping methodology using low-power auxiliary converter circuit may be very cost-effective and practical solution for the future DC systems with modular design and multiple sources/loads being constructed by different vendors with limited knowledge of their parameters and access to their internal controls.

Preface

I am the primary contributor to the research described in this thesis as well as to all corresponding publications associated with it. A part of research results has been already published in conference proceedings, while the rest has been submitted and/or is under the final preparation for submission to IEEE journal. In all manuscripts and thesis, I formulated the problems, derived equations, built the models, completed hardware implementations, conducted simulations and the experiments, and analyzed the results. The publications that came out from this thesis were prepared by me and then iteratively revised by the co-authors, my primary research supervisor Dr. Juri Jatskevich, and our colleague Dr. Zhenyu Shan. Dr. Zhenyu Shan also helped me in hardware implementation and conducting the experiments described in Chapters 4 and 5.

Some material from Chapter 2 has been submitted for publication. O. Pizniur, Z. Shan and J. Jatskevich, "Flyback-Convereter-Based Source System Identification for Investigation of Dymanic Stability with Constant Power Loads," in *Proceedings of IEEE 16th Workshop on Control and Modeling for Power Electronics* (COMPEL), Jul. 12–Jul.15, 2015, Vancouver, Canada, pp. 1–6. Dr. Jatskevich and Dr. Shan provided useful discussion and then revised and proofread the manuscript.

Some material from Chapters 3 and 4 has been published. O. Pizniur, Z. Shan and J. Jatskevich, "Ensuring Dynamic Stability of Constant Power Loads in DC Telecom Power Systems and Data Centers Using Active Damping," in *Proceedings of IEEE 36th International Telecommunication Energy Conference* (INTELEC), Sept. 28–Oct. 2, 2014, Vancouver, Canada, pp. 1–8. Dr. Jatskevich and Dr. Shan provided useful discussion and then revised and proofread the manuscript.

Some material from Chapters 3, 4 and 5 is in being reviewed for submission to a journal paper. O. Pizniur, Z. Shan and J. Jatskevich, "Active Auxiliary Converter Circuit for Stabilizing DC Distribution Systems with Constant Power Loads". Dr. Jatskevich and Dr. Shan provided useful discussion and then revised and proofread the manuscript. Dr. Shan also helped me with hardware implementation of the auxiliary circuit prototype and conducting the experiments.

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List of Abbreviations

AC	Alternating Current
AVM	Average-Value Model
ACCM	Average Current Control Mode
BCM	Boundary Conduction Mode
CCM	Continuous Conduction Mode
CPL	Constant Power Load
DC	Direct Current
DCM	Discontinuous Conduction Mode
DER	Distributed Energy Resources
DM	Detailed Model
GM	Gain Margin
HVAC	House Ventilation and Air Conditioning
LPF	Low-Pass Filter
PCCM	Peak-Current Control Mode
PVCCM	Peak-Valley Current Control Mode
PWM	Pulse-Width Modulation
PI	Proportional-Integral
THD	Total Harmonic Distortion

Acknowledgements

I want to express my endless gratitude to the entire faculty, staff and my fellow colleagues at the UBC Electric Power and Energy System Group for their support during my postgraduate studying. I owe special thanks and profound appreciation to my supervisor, Dr. Juri Jatskevich, who helped me from the very beginning to excel in this research and acquire relevant extensive knowledge by providing his continuous guidance and professional expertise. It was a great pleasure to work with such knowledgeable and dedicated hardworking individual. In addition to that, I want to acknowledge financial support obtained from the Natural Science and Engineering Research (NSERC) of Canada, Strategic Project Grant entitled "Advanced Integrated AC-DC Systems for Energy Efficient Buildings and Communities in Canada" led by Dr. Juri Jatskevich, without which my studying path would have been much more burdensome.

I am also grateful to Dr. W. Dunford and Dr. Y. C. Chen for dedicating their valuable time to serve on my examining committee, and for all their useful comments and feedback that have helped to improve the quality of this thesis.

I also would like to thank my colleagues, Dr. Zhenyu Shan for his invaluable comments and discussions of this research as well as great help in hardware implementation of experimental prototype. I also would like to thank research engineer Mr. Hua Chan for his help with setting up the experiments and programming of the constant power load.

Finally, my parents and girlfriend deserve a separate recognition of their role in my completion of this program. I express my sincere gratitude to my parents for their constant support and priceless contribution to my upbringing and educational path I took by aiming for excellence in my work and life, which brought me to the point where I am now. I also would like to thank my girlfriend Olga for her endless moral support and love, which made it possible for me to finish the program while simultaneously working in industry.

Присвячується моїм батькам,

дівчині, родині та Україні

To my beloved parents,

girlfriend, family and Ukraine

Chapter 1: Introduction

1.1 Motivation

It is envisioned that the trend of using more DC systems will grow over time and some point in the future may even dominate over the conventional AC systems. DC distribution systems pose a number of advantages such as reduced losses, higher power quality, compactness, fast and accurate control of power flow, as well as controllable transient response to disturbances and faults in the system [1]. Modern DC distribution systems increasingly use switching-mode power converters for energy transformation and power distribution. Specifically, power distribution in aircraft [4], vehicular systems [5] large ships [6], and even buildings [2], [3] require modular and efficient high bandwidth power devices to satisfy critical system requirements on flexibility of control, high power density, as well as robustness with respect to outages and component failures.

A generic DC distribution system is shown in Figure 1.1, which for the purpose of discussion in this section assumes one DC bus (whereas more complicated configurations are also possible). Most actual loads, e.g., light-emitting diode modules, computers and inverter-fed motors (Load 1 to Load *N*) are interfaced to the power system through converters (Source 1 to Source *N*). For many types of electronic loads, these converters, when tightly regulated, behave as constant power loads (CPLs) [7], [8]. Within their control bandwidth in small-signal sense, the CPLs have negative incremental input impedance, as illustrated in Figure 1.2. Specifically, when the source voltage decreases, the current drawn by the load increases, i.e. $dv/di < 0$, which results in negative incremental impedance. It was observed that the phenomenon of negative incremental impedance in the system may lead to possible oscillations and subsequent stability problems due to –180-degree impedance phase shift of CPLs. Considering that DC systems are rapidly expanding into many applications, the problem of potential dynamic instability due to negative incremental impedance of CPLs gains more importance and will require effective solutions in the nearest future.

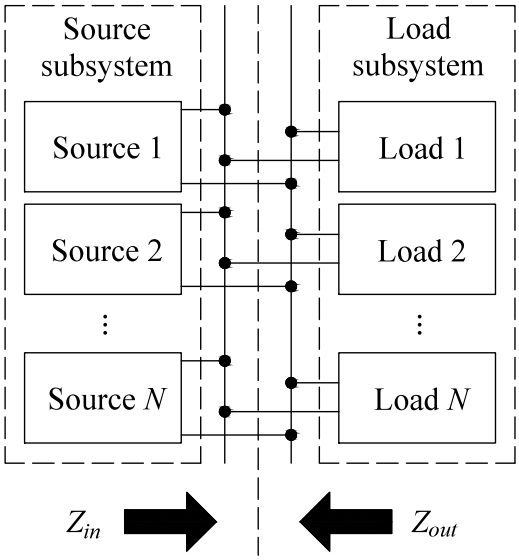


Figure 1.1 A typical DC distribution system subdivided at a particular DC bus interface.

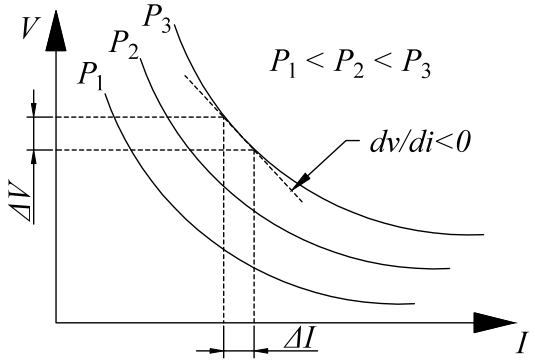


Figure 1.2 Input *V-I* characteristics to explain the negative incremental impedance of CPLs.

1.1.1 Alpha Technologies DC Distribution System

To give the reader a better insight, here we present an example of already available DC distribution systems a part of which is considered for the purpose of research presented in this thesis. Alpha Technologies Ltd. has recently completed a 450 kVA energy management system for an AC-DC Distributed Energy Resources (DER) network comprised of power converters and 1 MWh battery banks. The system is installed at three different locations on the UBC campus to shave the peak power demand from the buildings, provide uninterrupted power supply and feed future DC loads. A high-level diagram and photo of the system installed in Kaiser Building are shown in Figure 1.3 and Figure 1.4 respectively. Loads such as inverters, ventilation and air

conditioning (HVAC), controllers, computers and LED lighting seen are anticipated on both 380 VDC and 24 VDC busses as per the system's original design. Potentially, if the system is subdivided into source and load parts at a certain interface, it can be represented in the form of the one shown in Figure 1.1.

The electronic loads, e.g. computers, have floating power demand depending on the required computational load. The embedded step-down converters power the motherboards of computers or other intelligent equipment. These converters will tightly regulate the output voltage regardless of fluctuations in the input voltage. As a result, when the input voltage decreases, the converter input current increases and vise versa, thus exhibiting a negative incremental impedance characteristic of CPL at the computer's power input in small signal sense. Since such loads behave as CPLs, the problem of instability may be anticipated in the systems similar to the one installed in Kaiser Building, and this system may serve as a research test-bed.

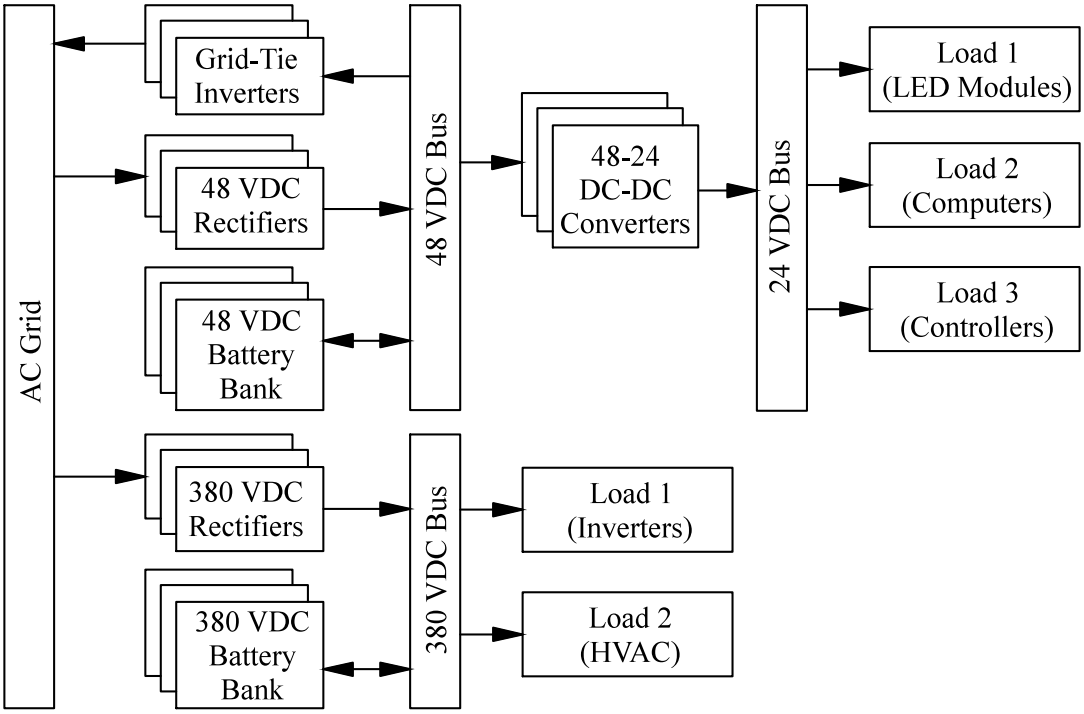


Figure 1.3 Alpha Technologies DC microgrid installed in Kaiser building at UBC.

Figure 1.4 Photo of several components of Alpha Technologies DC microgrid in Kaiser building at UBC.

Figure 1.5 contains additional components of the system that are envisioned to be added in the near future to the configuration depicted in Figure 1.3. The future configuration may include extra alternative energy sources, for example, solar panels fed through Maximum Power Point Tracking (MPPT) device, bi-directional converters and 380 V DC Grid-Tie inverters. This will yield higher autonomy and better power management within the local grid. As a result, one 380 VDC battery bank can be removed because 48 VDC and 380 VDC busses are presently interconnected through a bidirectional converter. Therefore, in case of AC system failure, all the DC busses will be powered from both 48 VDC battery bank and solar panels. The concept of having single battery bank (instead of multiple), for example in a DC-building, is very beneficial in terms of maintenance, required space and overall cost, so it will likely appear in future DC distribution systems.

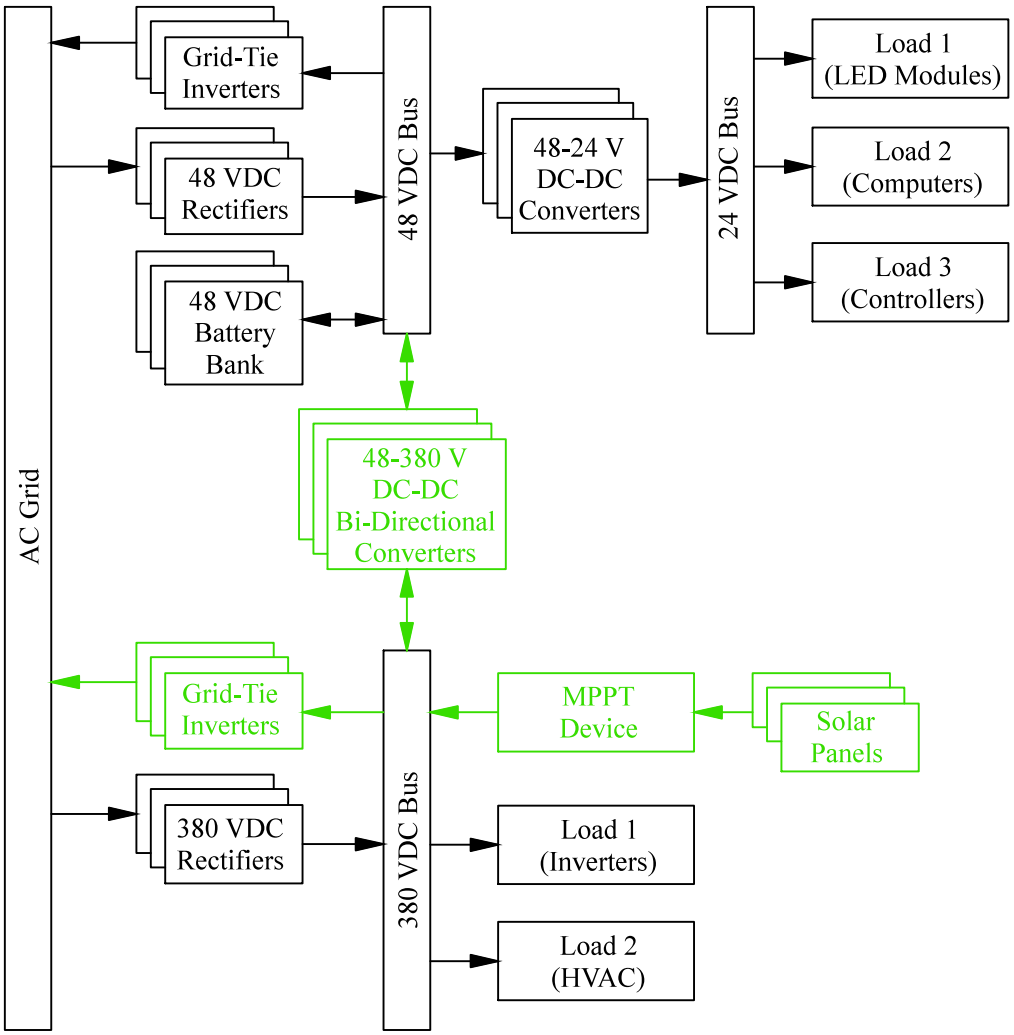


Figure 1.5 Future extended Alpha Technologies DC microgrid in Kaiser building at UBC.

1.1.2 Increasing Challenge of Dynamic Stability

The effect of negative incremental impedance from the CPLs may cause instability in the DC distribution systems [9], [10], [11]. Typically, each converter is routinely designed by a particular manufacture and tuned as a standalone device. Therefore, when a number of different converters (which may even be designed and built by different manufacturers) are interconnected, it introduces extra risks on the system stability, as possible dynamic interactions between converters were not taken into account. The origins of these interactions were originally studied and explained in [12]. To ensure stability of a system including individually designed converters, magnitude ratio of the source output impedance Z_{out} and the load input impedance Z_{in} must be smaller than one, i.e., $||Z_{out}||/||Z_{in}|| < 1$. This criterion is too conservative in general, and it

leads to over-design of the system with unnecessary large passive components and correspondingly higher costs. Therefore, a more reasonable criterion is considered, i.e. the impedance ratio of the so-called minor loop gain Z_{out}/Z_{in} must satisfy the Nyquist stability criterion for the system to be stable [13].

In low frequency region, the output impedance of a source is typically much lower than the input impedance of a load. However, in high frequency region, the source impedance Z_{out} may increase and load impedance Z_{in} decrease having -180-degree phase due to CPL. In this situation appropriate impedance reshaping is required to compensate for the CPL effect on the system.

A forbidden region based methodology that is used to calculate the required compensation for the load impedance according to a desired stability margin was presented in [14], [15], [16], [17], [18]. The main challenge of practical application of any forbidden region criterion lies in the necessity to know the models of the sources and loads and to solve large systems of equations required to calculate the optimal damping parameters for high-order systems as it was done in [19]. It is therefore difficult to envision that such approaches will be easily applicable to the future DC distribution systems wherein many components/converters and loads may be built by different manufacturers and their internal designs would remain unknown to a large extent.

1.2 Existing Solutions for Suppressing Instability

So far, the methods, which allow altering impedance ratio, have included either passive or active damping approaches, where active ones can be subdivided into linear and nonlinear. Passive damping is described with considerable details in [20], [21] includes *RL* and *RC* circuits connected at the interface where oscillations may occur. The drawbacks of the passive damping approach are: non-scalability and significant energy losses during large-signal transients. At power-levels of MWs, the application of passive damping becomes problematic.

The most promising method of active damping is modification of either the source or the load impedance by means of different linear and nonlinear control strategies [22], [23], [24], [25]. In the linear case [26], [27], the stabilization will mimic behavior of the load as if passive elements were connected to the bus. This methodology directly contradicts with modularity and scalability of future DC distribution systems, where the system integrator may not have the knowledge to access all the internal details of all sources and all loads.

Two recent works [28], [29], should be separated into an independent group utilizing active damping. In this type of active damping method, a separate bi-directional circuit with reduced size capacitor as an energy buffer is used to generate a damping current. A noticeable advantage is the use of a relatively compact circuit to suppress oscillations. In the linear case, a large passive *RC* damping circuit is imitated by a DC-DC converter acting as an ideal transformer with much smaller capacitor on the other end. Nevertheless, this approach comes at the cost of several drawbacks. Firstly, the volume of the buffer capacitor limits the amount of energy for damping. Secondly, the losses are not removed, and active power is dissipated in circuit and capacitor losses. Lastly, the terminal voltage of the buffer capacitor fluctuates considerably obstructing the control of the bi-directional power converter and subjecting the circuit to higher stresses. Another nonlinear passivity-based approach was presented in [30] which is hard to implement in practice due to its ultimate complexity (a prototype has been never introduced).

The challenges associated with using the existing damping approaches coupled with the vision of future DC distribution systems with desirable freedom to interconnect many and possibly unknown sources and loads in a modular and scalable manner requires a new paradigm for a universal global damping solution, which can be easily integrated into existing systems without modifying them internally. This solution should have high efficiency and adaptive behavior depending on the system's operating point.

1.3 Research Objectives

In this thesis, we propose a novel concept to stabilize a typical multi-voltage DC power distribution system such as the one depicted in Figure 1.6. This concept is based on an add-on auxiliary circuit, which can impact dynamic performance of the system as desired so that the stability may be achieved and guaranteed. In a multi-voltage DC distribution system, there is a necessity of having easy-to-use energy storage for peak shaving and uninterrupted power supply purposes. Therefore, one of the buses will typically have batteries attached to it, i.e. the power bus in Figure 1.6 (equivalent to 48 VDC bus in Figure 1.5). This power bus yields ultra-low output impedance and robustness, and at this bus the extra damping is not required. However, the low-voltage bus shown in Figure 1.6 (24 VDC bus in Figure 1.5) is powered just by converters thus requiring additional damping to compensate for the CPLs. Ultimately, the auxiliary circuit is

anticipated to bridge the low voltage bus and the power bus acting as a controlled current source and achieving a pre-programmed active damping without using extra energy storage elements.

The active damping methodology proposed in this thesis envisions the future DC distribution systems with freedom to interconnect many (and possibly unknown) sources and loads in a modular and scalable manner without modifying them internally. The proposed new paradigm for a universal global damping solution envisions a use of a low power auxiliary converter circuit that may be placed between the busses of the DC distribution system for the purpose of ensuring their small-signal stability. Specifically, to develop and demonstrate the new methodology, this thesis considers the following research objectives:

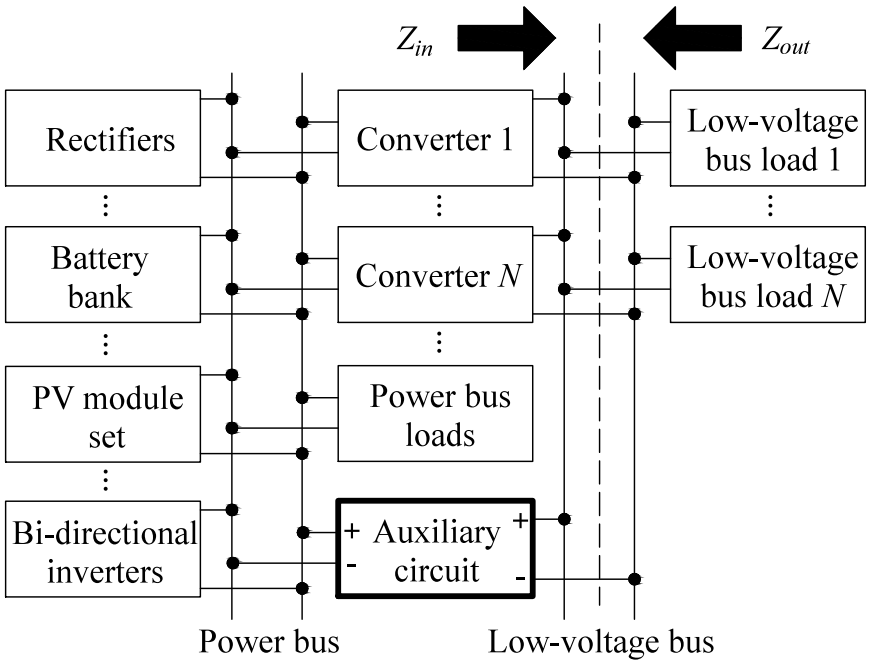


Figure 1.6 The proposed auxiliary-circuit-based approach is used to stabilize a multi-voltage DC power distribution system.

Objective 1 – System analysis to identify practical parameters for stability margin assessment

As an alternative to using full Nyquist stability criterion over entire frequency range (which is practically difficult to do), an easy-to-use parameters and criterion should be identified such that it can be readily used for the subsequent design of damping circuits. To properly understand the considered CPL instability phenomenon and propose a practical criterion for assessment of

stability margin, a system based on the Alpha Technology DC microgrid is considered in this thesis. Accurate average-value and small-signal models for both source and load sides are required so that simulations impedance analysis of the system under investigation can be performed. The appropriate models should be devised with reasonable details in order to study the CPL instability phenomenon. System identification is required for the source side since it is a commercially available converter for which we do not have full details and parameters required for the average model.

Objective 2 – Propose a new active damping methodology with flexible interfacing and programmable parameters

Propose auxiliary-circuit-based active damping that can be readily applied to DC distribution systems of various configurations with no modification to the original sources and loads (some of which may be not well-known) and with minimal power requirement and minimal power losses (no dissipation of active power for the purpose of damping). The proposed auxiliary-circuit requires proper damping current reference for stabilizing the system. A methodology for calculating the damping parameters for shaping the system's impedance characteristics based on the desired performance goals is required. For the purpose of active damping of various DC distribution systems, it is advantageous to be able to emulate linear passive behavior of damping and adaptive nonlinear damping (which depends on the system's operating point).

Objective 3 – Experimental verification using elements of the existing DC microgrid system

The proposed active damping methodology should be verified on a scaled version of existing DC distribution system. To achieve this, we will need to build a practical active auxiliary converter circuit, which will be capable of stabilizing the DC distribution system using the proposed active damping technique. A very fast and accurate current control scheme is required to achieve the required injection of the damping current. The design of the auxiliary converter circuit should include the power stage analysis with subsequent control scheme that together achieves the anticipated design goals.

Chapter 2: Modeling of DC Grids for Stability Studies

2.1 General Source-Load System Approach

Small-signal stability of DC systems has been studied and analyzed in many literature sources, for example in [12], [31], [32], and [33]. In general, it can be summarized that given the Nyquist stability criterion, a system will be unstable if two conditions exist at the same frequency:

1) Source impedance magnitude $||Z_{out}||$ is greater than load impedance magnitude $||Z_{in}||$
2) Phase angle ratio of Z_{out}/Z_{in} is equal to -180 degrees

Based on small-signal impedance analysis, the DC system has to be divided into source and load subsystems as depicted in Figure 2.1. For the purpose of analysis presented in this section, an ideal voltage source v_s in series with output impedance Z_{out} represents the actual power source. The impedance Z_{in} in small-signal sense represents the actual load, which has the CPL characteristic. Therefore, investigation of instability in DC distribution system requires the availability of valid source/load average-value and small-signal models. Having those models will make it possible to run simulations and analyze the system in frequency-domain using impedances.

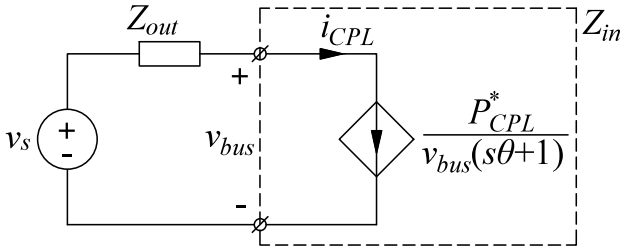


Figure 2.1 An equivalent model of a DC distribution system subdivided at an arbitrary interface into source and constant power load.

2.1.1 Nth Order Source Impedance Model

The output impedance Z_{out} of feeding converters and other devices on the power bus with the transmission cable effect can be represented by an n^{th} order transfer function in zero-pole-gain form as

$$Z_{out} = K\frac{(s-z_n)(s-z_{n-1})...(s-z_1)(s-z_0)}{(s-p_m)(s-p_{m-1})...(s-p_1)(s-p_0)}. \tag{2.1}$$

Each term in the numerator and denominator of (2.1) can be considered as a unique vector with magnitude and phase. For the case of a pole, the magnitude and phase are described by (2.2) and (2.3) respectively as

$$\left\|s-p_i^{out}\right\| = \sqrt{(\pm\alpha^2)+(\omega-\omega_i^{out})^2} \tag{2.2}$$

and

$$\Phi(s-p_i^{out}) = \tan^{-1}\left(\frac{\omega-\omega_i^{out}}{-\alpha}\right), \tag{2.3}$$

where $s = j\omega$. Then, by following the basic rules, the source impedance magnitude (2.4) and phase (2.5) can be determined as product and sum of their child vectors' magnitude and phase respectively by

$$\left\|Z_{out}\right\| = K\frac{\prod_{i=1}^{m}\left\|j\omega-z_i^{out}\right\|}{\prod_{i=1}^{n}\left\|j\omega-p_i^{out}\right\|} \tag{2.4}$$

and

$$\Phi(Z_{out}) = \sum_{i=1}^{n}\Phi(j\omega-z_i^{out}) - \sum_{i=1}^{m}\Phi(j\omega-p_i^{out}). \tag{2.5}$$

2.1.2 Generic First-Order Constant Power Load Model

In small-signal sense, the input impedance of a CPL is derived as

$$Z_{in} = \frac{dv_{bus}}{di_{CPL}} = \frac{d}{di_{CPL}}\left(\frac{P_{CPL}^*}{i_{CPL}}\right) = -\frac{P_{CPL}^*}{i_{CPL}^{\ 2}} = -\frac{v_{bus}}{i_{CPL}} = -R_{in}, \tag{2.6}$$

where P_{CPL}^* is a given commanded (reference) power. In addition, i_{CPL} and v_{bus} are the load current and bus voltage, respectively. From (2.6), it is observed that input current and bus voltage have ideal −180-degree phase with respect to each other. However, a practical CPL has

limited control bandwidth, which means that the −180-degree phase shift exists within a certain frequency range. This characteristic can be expressed by adding a real zero to (2.6), i.e.

$$Z_{in} = -R_{in}(s\theta + 1), \tag{2.7}$$

where the cut-off frequency of CPL characteristic is determined by $1/\theta$. Correspondingly, the current of CPL takes the form of

$$i_{CPL} = \frac{P^*}{v_{bus}(s\theta + 1)}. \tag{2.8}$$

2.1.3 Small-Signal Source-Load Impedance Interactions

In [31] and [32], it was shown that the system of Figure 2.1 is stable if and only if all of the following conditions are satisfied:

1) The actual source is stable when unloaded
2) The actual load is stable when powered from an ideal power source
3) And the system described by the transfer function

$$H(s) = \frac{v_{bus}}{v_s} = \frac{1}{1 + \frac{Z_{out}}{Z_{in}}} \tag{2.9}$$

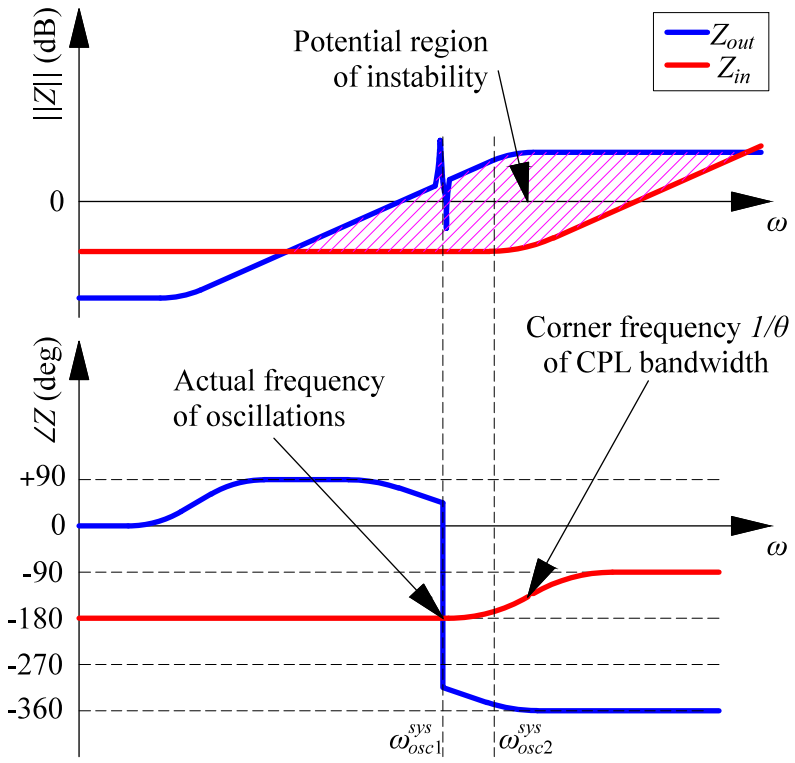
is stable too.

Here, $H(s)$ is a closed loop transfer function with a minor loop gain $T_{sys} = Z_{out}/Z_{in}$. Therefore, (2.9) will be stable when T_{sys} satisfies the Nyquist stability criterion

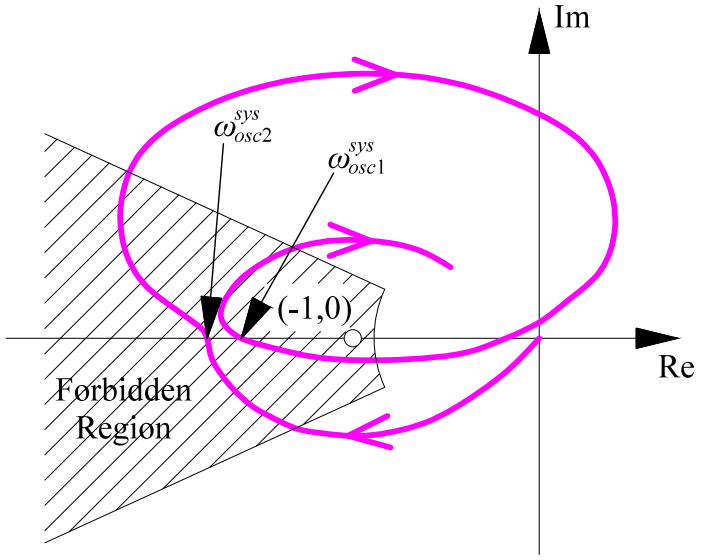
$$\begin{cases} \left\| T_{sys} \right\| < 1 \\ OR \\ \Phi[T_{sys}] \neq 180\,\text{deg}. \end{cases} \tag{2.10}$$

The system's oscillation frequencies depend on the values of conjugate complex right-hand-sides poles of T_{sys} taking the form of $p_i^{sys} = \alpha_i^{sys} \pm j\omega_i^{sys}$. The impedance characteristics in frequency domain of a typical DC distribution system with CPLs are depicted in Figure 2.2 (a). It is observed from the plots that the Nyquist criterion (2.10) at two points, ω_{osc1}^{sys} and ω_{osc2}^{sys}, is not satisfied, and the oscillations will occur.

Although this sample system has two unstable modes {two encirclements of point (-1,0) on the Nyquist plot are located within the so-called forbidden region [18], see Figure 2.2 (b)}, for the practical purposes in this thesis we will consider only the first one as the frequency of interest for the purpose of CPL reshaping. The reason behind this is that the instability at ω_{osc1}^{sys} happens earlier than at ω_{osc2}^{sys}, i.e. $\omega_{osc1}^{sys} < \omega_{osc2}^{sys}$. Therefore, when the CPL impedance is reshaped not to have the negative incremental effect taking into account the lower frequency ω_{osc1}^{sys}, the higher frequency one, ω_{osc2}^{sys}, will be factored in inherently. The unstable mode frequencies can be determined analytically from (2.4), (2.5) and (2.7) considering (2.10). Alternatively, the dominating unstable mode frequency can be measured or determined experimentally during the system operation. Therefore, considering the first (lower) frequency point will be used as a practical criterion for the subsequent damping methodology.



(a)



(b)

Figure 2.2 Small-signal characteristics of a typical DC distribution system with high-order source subdivided at an assumed source-load interface: (a) its source-load impedance Bode diagram; and (b) the Nyquist plot of T_{sys} with overlapped forbidden region.

2.1.4 State-of-the-Art Passive and Active Damping Methods

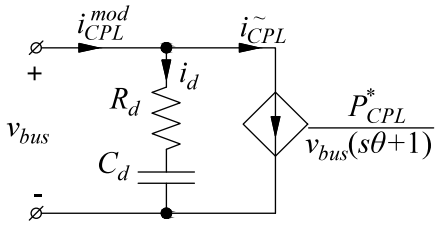


Figure 2.3 Passive damping of CPL by *RC* parallel circuit.

Passive circuits, e.g., parallel *RC*, parallel *RL* and series *RL* circuits are widely used for CPL damping in a DC systems [20]. An example of parallel *RC* circuit installation is shown in Figure 2.3. The impedance of this type of circuit is described as

$$Z_d^{RC} = \frac{(sRC+1)}{sC}. \tag{2.11}$$

With appropriate resistor and capacitor values, the system oscillations caused by CPL may be suppressed.

Due to the drawbacks of passive damping methods in terms of flexibility, efficiency and scalability, an active damping approach was proposed in [23]. This damping is used to directly reshape the input impedance of the CPL and is depicted in Figure 2.4. This approach is essentially a nonlinear control scheme, according to which the instantaneous value of the input power of the equivalent/modified CPL load is calculated as

$$P_{CPL}^{\text{mod}} = \left(\frac{v_{bus}}{v_{bus}^{\sim}} \right)^u P_{CPL}^*, \tag{2.12}$$

where $v_{bus}^{\sim} = \frac{v_{bus}}{s\tau+1}$ is the sensed bus voltage passed through a low pass filter. Under this control algorithm, the CPL response is softened in high-frequency region in terms of both impedance and phase. So far, there has not been given straightforward guidelines on how to properly select scaling factor u and time constant τ so that the desired damping goals are achieved. As a disadvantage, this method requires to have the internal structure of the load's controller to be changed, which may not always be possible or practical considering the envisioned DC distribution system with flexibility and modularity.

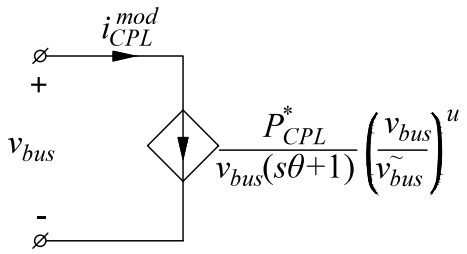


Figure 2.4 Active damping based on changing the CPL internal controller structure.

2.2 DC Source Flyback Converter System Identification

As discussed in Section 2.1.1, a high-order source model is considered for conducting source-CPL interactions investigation. In this work, we will use as a source building block commercially available source in a form of 2 kW 48-24 V DC-DC converter, model CXDF 48-24/2kW, which is manufactured by Alpha Technologies Ltd. This converter is widely used in telecom applications and 4 modules (8 kW in total) were installed into Alpha Lab AC-DC microgrid described in Chapter 1 of this thesis. Since we possessed only partial information on the converter's power stage, and no information on its control was available, a comprehensive identification was required to construct a model with required accuracy and level of detail.

2.2.1 Detailed Model of the Flyback Source Converter

The high-level block diagram of the considered converter is shown in Figure 2.5. The DC source is a six-phase interleaved flyback converter with separate input and output filter collector boards consisting of capacitor bank as well as common-mode EMI-suppressing chokes. In this work, for simulation and frequency response analysis, the effect of choke will be neglected as it affects only the common-mode component of the input/output currents and does not impact the overall system's dynamics for differential-mode currents. In addition to separate input and output filter, each phase has its own 3rd order input and output filters. The PWM signal has 60-degree phase shift for each of the six phases, where the duty cycle for is generated depending on the desired output voltage. In general, the interleaved control makes it possible to achieve higher converter control bandwidth and efficiency with better components utilization and more compact design [36]. From the manufacturer, we obtained the description of almost all components required for the detailed model (DM) composition with exception to magnetizing inductance of the transformer, the operating mode, and the overall control scheme. For the purpose of building

a valid DM and its verification against real converter, these parameters must be obtained by estimation and/or experimental identification.

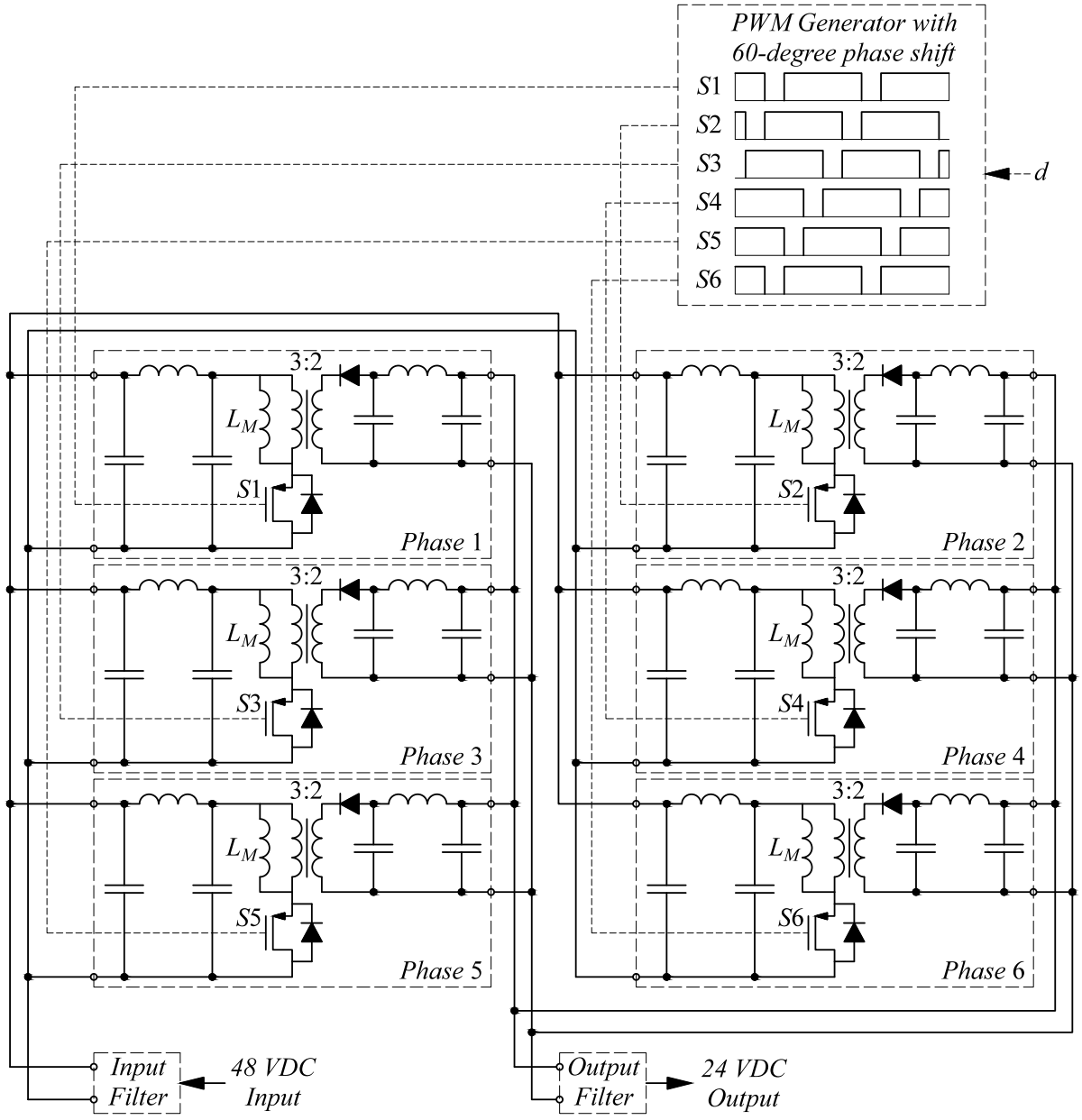


Figure 2.5 Power stage of the considered six-phase interleaved flyback DC-DC converter.

2.2.2 Converter Magnetizing Inductance and Control Scheme Identification

Magnetizing inductance is an important parameter of flyback converters, which significantly impacts its dynamics and overall performance. It is very common to refer magnetizing inductance to the primary side of the main transformer as it was done in Figure 2.5.

The installed transformer, model E43/10/28, is manufactured by Ferroxcube and its basic dimensions and parameters are summarized in Table 2.1.

Total air gap l_g, [m]	0.5*e*-3
Transformer turns ratio n_1:n_2	3:2
Equivalent mean magnetic path length l_m, [m]	61*e*-3
Magnetic core cross-section A_C, [m^2]	2.29*e*-4
Relative permeability μ_e	120
Specific inductance A_L, [H/n^2]	550

Table 2.1 Flyback converter transformer parameters.

Given the transformer parameters, there are several ways to calculate its magnetizing inductance. For the purpose of confidence in results, we will utilize several methods. Firstly, the magnetizing inductance can be estimated by taking into account the equivalent mean magnetic path length and relative permeability as [37]

$$L_M = \frac{n_1^2 \mu_0 \mu_e A_C}{l_m}. \tag{2.13}$$

Secondly, by taking into account the fact that air gap dominates the transformer properties (i.e. its reluctance is much higher than the one of magnetic core), equation (2.13) can be simplified as

$$L_M = \frac{n_1^2 \mu_0 A_C}{l_g}. \tag{2.14}$$

Lastly, the magnetizing inductance can be obtained by factoring in the core specific inductance as [38]

$$L_M = n_1^2 A_L. \tag{2.15}$$

The equations (2.13), (2.14) and (2.15) all yielded very similar value for transformer magnetizing inductance, which is assumed to be L_M = 5 μH.

Any DC-DC converter would have two modes of operation: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). In CCM, the main inductor current never reaches a zero value within one switching period (always conducting). In DCM, the inductor

current has a certain period between switching cycles when it reaches zero value (non-conducting period). These modes are significantly different in terms of dynamics, and converter's operation in these modes is determined by multiple parameters such as inductor value, switching frequency and load current. Given the similarity of buck-boost and flyback converter characteristics, the steady-state conversion ratio M of flyback output V_o to input V_g voltages in CCM can be described as [21]

$$M_{CCM} = n\frac{D}{1-D}, \tag{2.16}$$

and in DCM as

$$M_{DCM} = n\frac{D}{\sqrt{K}}, \tag{2.17}$$

where n is the transformer's windings ratio, i.e. $n = n_1 / n_2$, D is steady state control duty cycle, and K is the conduction mode coefficient. The latter can be described by

$$K = \frac{2L_M n^2}{R_{load} T_{sw}}, \tag{2.18}$$

where R_{load} is an equivalent resistor representing real load connected to the output terminals of the flyback converter, and T_{sw} is the switching period.

In order to determine the flyback converter mode of operation we need to compare (2.18) to a so-called critical conduction mode coefficient K_{crit}. The critical conduction mode coefficient sets the boundary between CCM and DCM, and if $K < K_{crit}$, then the converter operates in DCM. Essentially, the converter's voltage conversion ratios would be both equal for CCM and DCM at the boundary between them (boundary conduction mode (BCM)), i.e. $M_{CCM} = M_{DCM}$. Consequently, we can rearrange equations (2.16) and (2.17) in terms of critical conduction mode coefficient, $K_{crit} = K$, when the converter operates in BCM as

$$K_{crit} = (1-D)^2. \tag{2.19}$$

Then substituting (2.16) expressed in terms of D into (2.19) will yield an equation for K_{crit},

$$K_{crit} = \left(\frac{n}{n+M}\right)^2. \tag{2.20}$$

Our source flyback converter having six phases is rated to operate at $V_o = 27$ VDC, $V_g = 52$ VDC

and I_{load} = 75 A (equivalent to R_{load} = 2.16 Ohm @ 27 VDC for one phase) with switching frequency of 130 kHz. Taking into account these values, the conduction mode coefficients can be calculated from (2.18) and (2.20) as, K = 0.26 and K_{crit} = 0.31. Since $K < K_{crit}$, a straightforward conclusion can be drawn that each phase of our source flyback converter operates in DCM.

The last part remaining to be identified is the control scheme of the converter. In order to get an intuitive insight into its operation, a load application/rejection study with R_{load} = 1 Ohm was conducted. The converter's measured output voltage and current transient is depicted in Figure 2.6. As can be seen from the measured waveforms in Figure 2.6, once the load is applied, the output voltage dips due to parasitic inductance of the load. The internal control of the converter rapidly compensates for that and then slowly recovers the output voltage to the commanded value. Based on classic control theory, the fast recovery (20 ms transient) corresponds to an inner feedback loop, which in this case could be load feed-forward for DCM operation. Similarly, the slow recovery (200 ms transient) corresponds to outer control loop with lower bandwidth. Considering the observed transient in Figure 2.6, we have come up with control concept of the converter as shown in Figure 2.7. This figure also contains high-level power stage model with details shown in Figure 2.5. The assumed control of the converter operates as follows:

- Fast inner output voltage control loop is built as in DCM steady state, the feed-forward command for the duty cycle is calculated continuously from combination of (2.17) and (2.18) as

$$d = n\frac{v_o}{v_g}\frac{1}{\sqrt{\frac{2L_M n^2}{v_o^* i_{load} T_{sw}}}}, \tag{2.21}$$

  where v_o^*, v_o, v_g and i_{load} are the instantaneous commanded output voltage, the measured output voltage, the measured input voltage, and the measured output current at one phase, correspondingly.
- Slow outer voltage control loop is realized as a simple proportional-integral (PI) controller with K_p = 0.01 and K_i = 0.3.

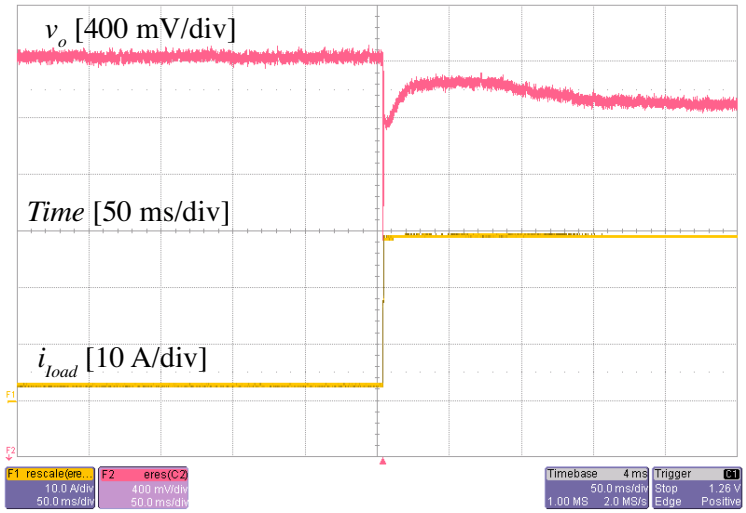


Figure 2.6 Converter's measured output voltage and current transients during 1 Ohm (700 W) step load application study.

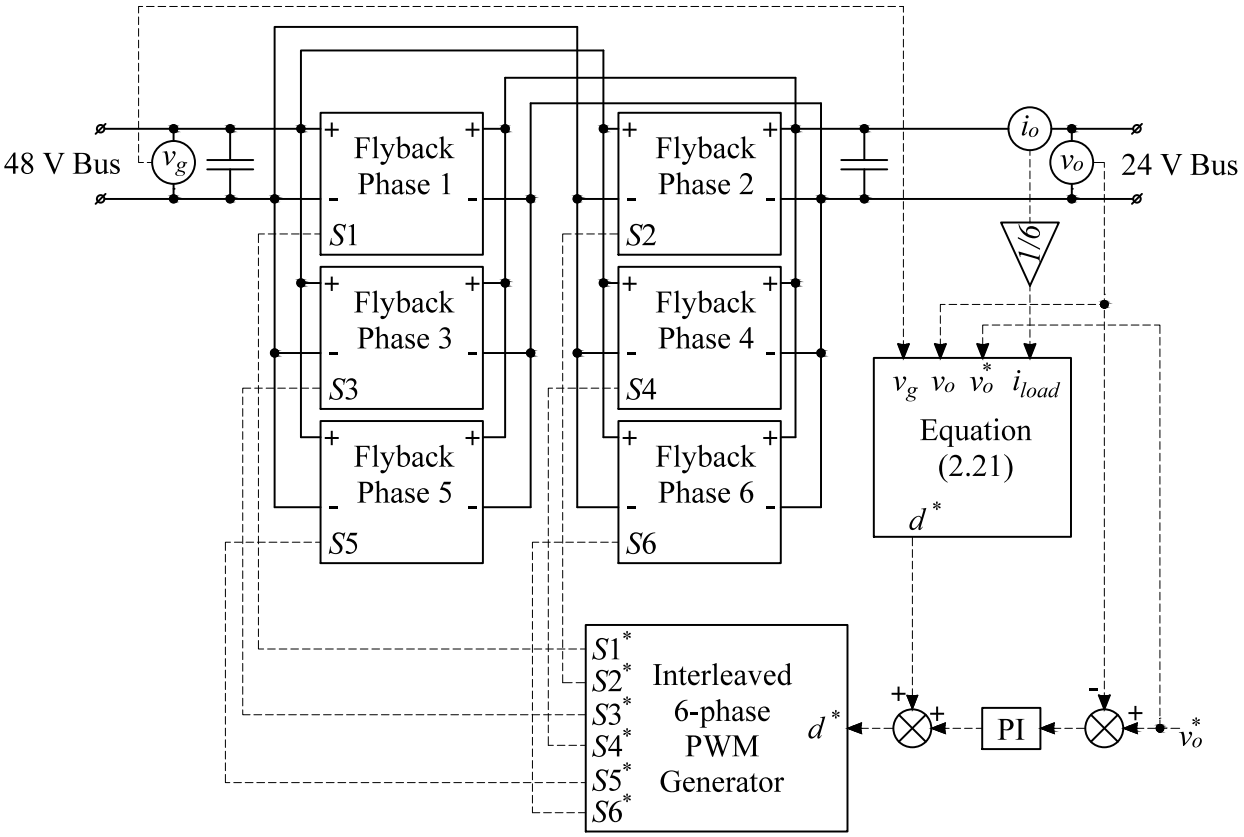


Figure 2.7 Proposed high-level DM of the six-phase interleaved DC-DC flyback converter with double-loop voltage control operating in DCM at 130 kHz with L_M = 5 µH.

2.2.3 Dynamic Average-Value Modeling

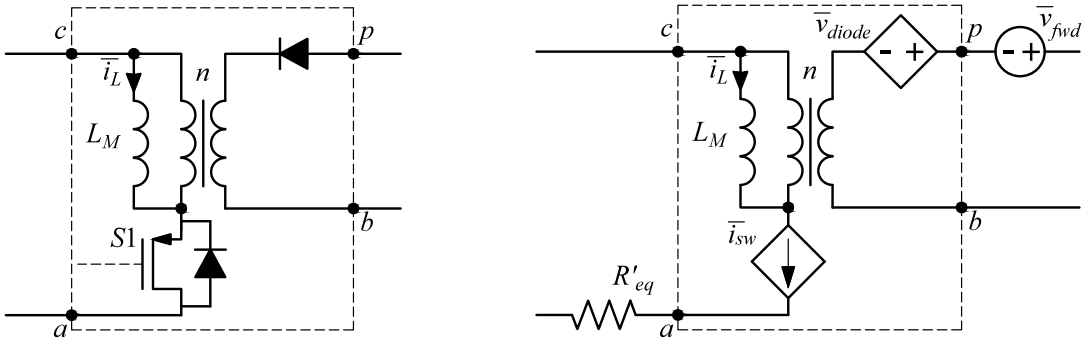


Figure 2.8 Switching cell for a flyback converter: (a) switching cell comprising the DM; and (b) equivalent corrected non-switching AVM cell.

Each phase of the flyback converter can be represented as a nonlinear average-value model (AVM) by the corrected procedure given in [39]. To be more specific, the converter's switching cell ***cpba***, as shown in Figure 2.8 (a), consisting of transistor, diode and transformer is modified so that controlled current and voltage sources replace the discrete elements, as depicted in Figure 2.8 (b). Their parasitics are modeled by separate elements outside of the switching cell considering the energy conversation principle [40]. The transistor ON resistance, transformer primary and secondary side resistances are incorporated into the equivalent resistance R_{eq}, which is estimated to be 0.1 Ohm for the source converter under study. The corrected equivalent resistance is calculated as [39]

$$R'_{eq} = \frac{4R_{eq}}{3d^*}. \tag{2.22}$$

The diode forward voltage drop is represented by a constant voltage source $\overline{v}_{fwd}$ and estimated to be 0.6 V. The values for average switch current $\overline{i}_{sw}$ and diode voltage $\overline{v}_{diode}$ are given by [39]

$$\overline{i}_{sw} = \frac{d^*\overline{i}_L}{d^* + d_2} \tag{2.23}$$

and

$$\overline{v}_{diode} = (1-d_2)\overline{v}_{pb} - d^* n\overline{v}_{ca}, \tag{2.24}$$

where d_2 is the duty ratio constraint for the flyback diode-conducting subinterval. Explicit equation for corrected d_2, which takes into account converter's parasitics and losses is given by

$$d_2 = \frac{\left(\frac{2L}{d^* T_{sw}} + \frac{4}{3} R_{eq}\right) \overline{i}_L}{v_g} - d^*. \tag{2.25}$$

Substituting (2.25) into (2.23) and (2.24) yields equations for commanding the controlled current sources in the average switching cell as

$$\overline{i}_{sw} = \frac{d^* v_g}{\frac{2L}{d^* T_{sw}} + \frac{4}{3} R_{eq}}, \tag{2.26}$$

$$\overline{v}_{diode} = \left(1 - \frac{\left(\frac{2L}{d^* T_{sw}} + \frac{4}{3} R_{eq}\right) \overline{i}_L}{v_g} + d^*\right) \overline{v}_{pb} - d^* n \overline{v}_{ca}. \tag{2.27}$$

Ultimately, the interleaved flyback converter model with average switching cell ***cpba*** for each phase is shown in Figure 2.9. Since direct feedback of some measured system variables introduced algebraic loops, the low-pass filters (LPF) with very small time constant have been used. Each of the controlled sources within the average switching cell is commanded based on system variables inputs and equations (2.26) and (2.27).

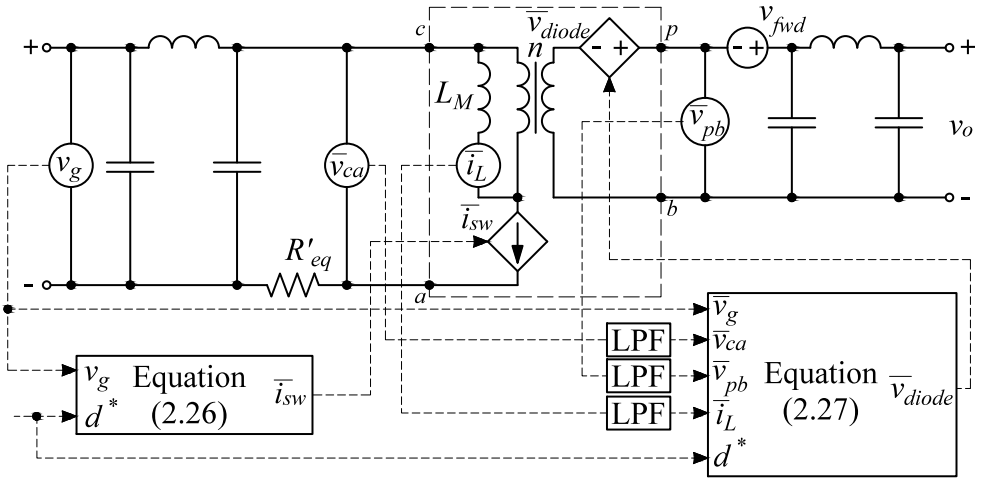


Figure 2.9 Per-phase corrected AVM of the source flyback converter depicting the dependent voltage and current sources.

After obtaining the appropriate average switching cells as shown in Figure 2.9, the interleaving of all separate phases may be ignored, and for the purpose of further modeling the six phases may be replaced using one AVM with appropriate scaling of input and output currents as depicted in Figure 2.10. The two assumed control loops are also depicted in Figure 2.10.

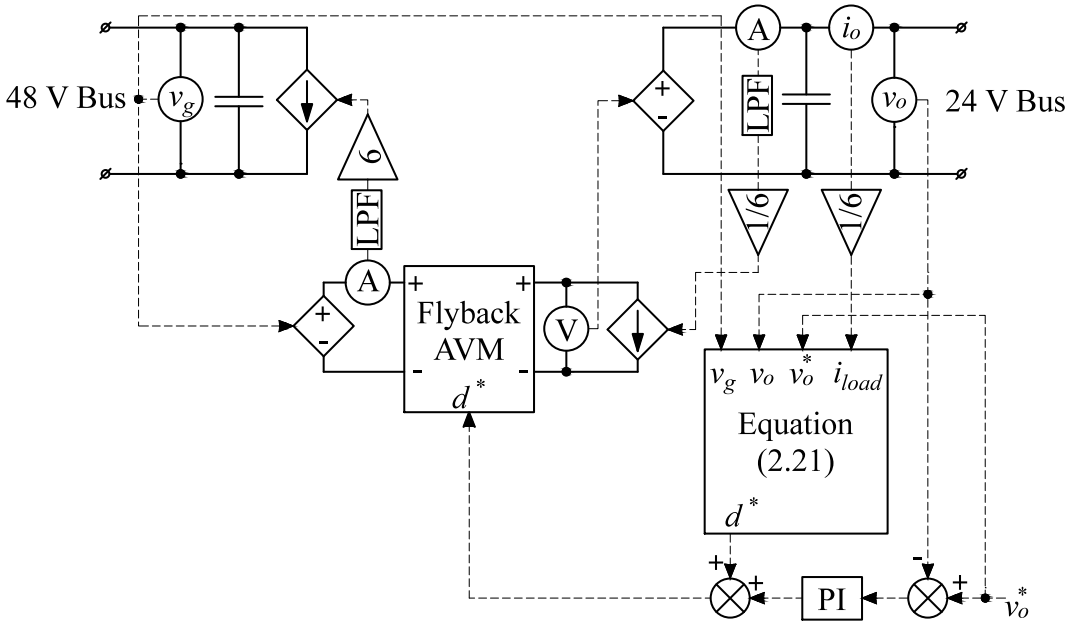
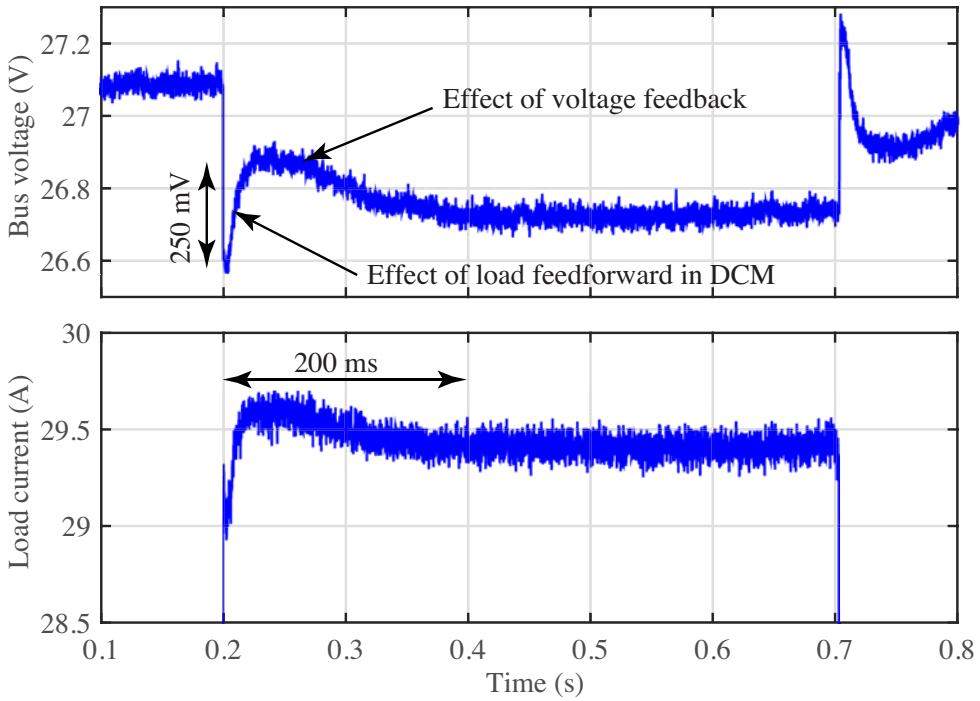


Figure 2.10 Proposed corrected AVM of the DC six-phase flyback converter with double-loop voltage control.

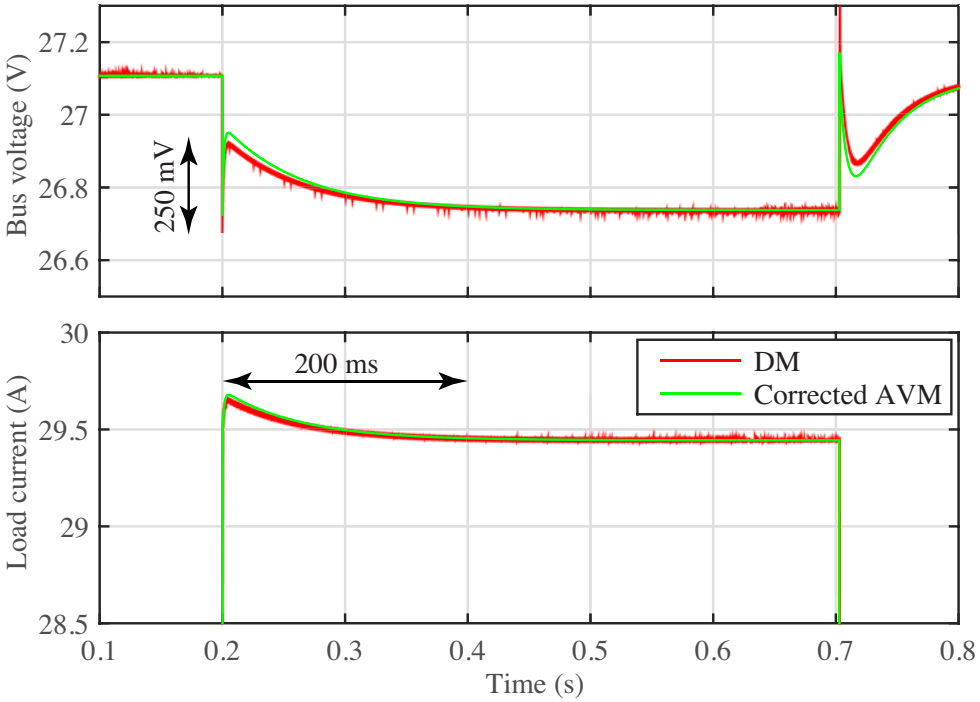
2.2.4 Verification of Detailed and Average-value Models in Load Transients

Both DM and AVM of the source were created for simulation and system study purposes. A load application and rejection studies depicted in Figure 2.11 were conducted in order to verify the models against the hardware source converter. Parameters of the study include the following: V_o = 27 VDC, R_{load} = 1 Ohm, L_{load} = 10 μH.

As it can be seen in Figure 2.11, both detailed and average models correspond very well to the measured results (both models go to steady state in approximately 200 ms as it does the hardware measurement). In this study, we are more interested in slower transient since it has stronger impact on the bandwidth of source converter and interactions with CPLs.



(a)



(b)

Figure 2.11 Transient response of the Alpha Technologies CXDF 48-24/2kW DC/DC converter to step load application/rejection: (a) experimental results; and (b) detailed and corrected average model simulations.

Chapter 3: Proposed Active Damping Approach Using Auxiliary Circuit

3.1 Active Linear Damper Emulating a Virtual Low-Pass RC Filter

Theoretically, if one applies an ideal shunt current source to the unstable bus depicted in Figure 2.1, the CPL behavior can be altered in a desired manner as seen from the input terminals. In linear case, this current source would mimic an *RC* circuit behavior. However, instead of wasting energy, it would be recycling it into the neighboring bus according to the concept of the auxiliary circuit shown in Figure 1.6. Taking into account the *RC* circuit impedance described by (2.11), an equivalent system diagram can be constructed for implementation of active linear damping as shown in Figure 3.1. Here, the commanded current is generated according to the required damping impedance Z_d and the bus voltage v_{bus}. In an actual circuit, the damping current command is generated by expanding the equation $i_d^*(s) = v_{bus} / Z_d^{RC}$ as

$$i_d^*(s) = \frac{v_{bus}}{R} - \frac{i_d^*}{s}\frac{1}{RC}. \tag{3.1}$$

The integrator term of the commanded current can be discretized for digital implementation as

$$\frac{i_d^*}{s} = i_d^*[n-1] + i_d^*[n](t[n] - t[n-1]), \tag{3.2}$$

where [n] and [n-1] denote the current and previous discretization steps, respectively.

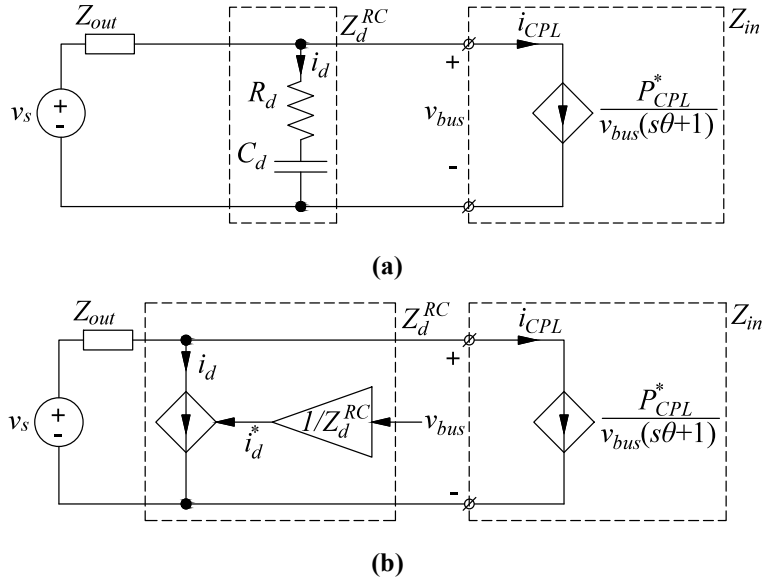


Figure 3.1 Proposed active damping approach: (a) passive equivalent circuit; and (b) equivalent linear damping current injection representation.

3.1.1 Routh-Hourwitz Criterion and Gain Margin Goal for Determining Virtual Filter Parameters

To apply active linear damping, we need to calculate appropriate values for virtual *RC* circuit that is to be emulated by the auxiliary active damping circuit. A method to calculate the parameters of an *RC* damper based on Routh-Hurwitz criterion has been proposed in [20]. This methodology can be potentially applied to higher order systems [34]. In this section, we propose a hybrid method to derive the parameters of *RC* damper for a high-order system by applying both Gain Margin and Routh-Hurwitz criterion methodologies, respectively.

An *RC* damping circuit has two main parameters, *R* and *C*, which can be calculated by composing at least two independent equations. It is assumed that the system oscillation frequencies ω_{osc1}^{sys}, $\omega_{osc2}^{sys} \ldots \omega_{oscN}^{sys}$ are known and obtained as described in Chapter 2. The system stability can be estimated from the loop gain T_m using the Nyquist criterion in terms of its magnitude. We modify the source impedance by referring the damping impedance Z_d^{RC} to the source side as seen in Figure 3.1 (a). Then, according to this criterion and a given gain margin (GM) for each unstable mode, the first set of equations can be outlined as

$$\begin{cases} \left| \dfrac{Z_{out}(j\omega_{osc1}^{sys}) \cdot Z_d^{RC}(j\omega_{osc1}^{sys})}{[Z_{out}(j\omega_{osc1}^{sys}) + Z_d^{RC}(j\omega_{osc1}^{sys})] / Z_{in}(j\omega_{osc1}^{sys})} \right| < \left| \dfrac{1}{GM_1} \right| \\ \cdots \\ \left| \dfrac{Z_{out}(j\omega_{oscN}^{sys}) \cdot Z_d^{RC}(j\omega_{oscN}^{sys})}{[Z_{out}(j\omega_{oscN}^{sys}) + Z_d^{RC}(j\omega_{oscN}^{sys})] / Z_{in}(j\omega_{oscN}^{sys})} \right| < \left| \dfrac{1}{GM_N} \right|. \end{cases}, \tag{3.3}$$

In addition, the system stability can be evaluated applying the Routh-Hurwitz criterion to the closed-loop transfer function. From there, we can get the second set of equations. Considering the damper impedance Z_d^{RC}, the denominator of (2.9) becomes

$$D(s) = [Z_{out} + Z_d^{RC}] / Z_{in} + Z_{out} Z_d^{RC}. \tag{3.4}$$

For any n^{th} order closed-loop system, the denominator of its transfer function can be expressed as

$$D(s) = d_n s^n + d_{n-1} s^{n-1} + \cdots + d_1 s + d_0. \tag{3.5}$$

A necessary but not sufficient condition for the system stability is that all polynomial coefficients of (3.5) must be positive [35], i.e.

$$\begin{cases} d_n > 0 \\ d_{n-1} > 0 \\ \dots \\ d_0 > 0. \end{cases} \tag{3.6}$$

Without loss of generality in further analysis, we will assume that our source impedance is limited 4th order representation (which should be sufficient for many practical purposes). Thus, by factoring in first order damping impedance, we will obtain a 5th order closed loop transfer function. Then, for a 5th order system, we can write a supplementary to (3.6) set of equations as follows [35]

$$\begin{cases} d_4 d_3 - d_5 d_2 > 0 \\ (d_4 d_1 - d_5 d_0)^2 - (d_4 d_3 - d_5 d_2)(d_2 d_1 - d_3 d_0). \end{cases} \tag{3.7}$$

Then, (3.6) and (3.7) form a second set of equations for virtual damper *RC* parameters calculations. In (3.3) and (3.4), the output impedance Z_{out} is expressed as a polynomial equivalent to (2.1),

$$Z_{out} = \frac{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0}, \tag{3.8}$$

where the parameters a_0, a_1, …, a_4, and b_0, b_1, …, b_4, can be extracted from the model T_{sys} described in Chapter 2. The damping circuit impedance is described by (2.11) and small-signal impedance of a CPL, neglecting high-frequency dynamics, is given by (2.6). Finally, d_0, d_1, …, d_n are derived from (3.4) using (2.6), (2.11) and (3.8) as

$$\begin{cases} d_5 = CR_l a_4 - CRa_4 + CRR_l b_4 \\ d_4 = R_l b_4 - a_4 - CRa_3 + CR_l a_3 + CRR_l b_3 \\ d_3 = R_l b_3 - a_3 - CRa_2 + CR_l a_2 + CRR_l b_2 \\ d_2 = R_l b_2 - a_2 - CRa_1 + CR_l a_1 + CRR_l b_1 \\ d_1 = R_l b_1 - a_1 - CRa_0 + CR_l a_0 + CRR_l b_0 \\ d_0 = R_l b_0 - a_0. \end{cases} \tag{3.9}$$

Considering discussion in Chapter 2, the system will have only one dominant oscillatory mode of interest to us, i.e. ω_{osc1}^{sys}. Consequently, (3.3), (3.6) and (3.7) are combined to form a system, by solving which we can find the optimal *RC* parameters for stabilizing the system with CPLs as

$$\begin{cases} \left| \dfrac{Z_{out}(j\omega_{osc1}^{sys}) \cdot Z_d^{RC}(j\omega_{osc1}^{sys})}{[Z_{out}(j\omega_{osc1}^{sys}) + Z_d^{RC}(j\omega_{osc1}^{sys})] / Z_{in}(j\omega_{osc1}^{sys})} \right| < \left| \dfrac{1}{GM_1} \right| \\ d_5 > 0 \\ d_4 > 0 \\ d_3 > 0 \\ d_2 > 0 \\ d_1 > 0 \\ d_4 d_3 - d_5 d_2 > 0 \\ (d_4 d_1 - d_5 d_0)^2 - (d_4 d_3 - d_5 d_2)(d_2 d_1 - d_3 d_0) > 0, \end{cases} \tag{3.10}$$

such were both desired gain margin and Routh-Hurwitz criterion are satisfied. Alternatively, observing from (3.6) and (3.9), the system cannot be stabilized when

$$R_l < \frac{a_0}{b_0}. \tag{3.11}$$

3.2 Adaptive Active Nonlinear Damper as Variable Low-Pass RC Filter

As far as nonlinear adaptive damping is concerned, in this thesis we will use damping technique proposed in [23] as a baseline. Theoretically, this methodology can be transferred into a separate ideal current source, which will implement the damping of CPL behavior.

3.2.1 Injected Damping Current Calculation

The model shown in Figure 3.2 (a) depicts the load from Figure 2.1 with a shunt current source representing the proposed active damping auxiliary circuit.

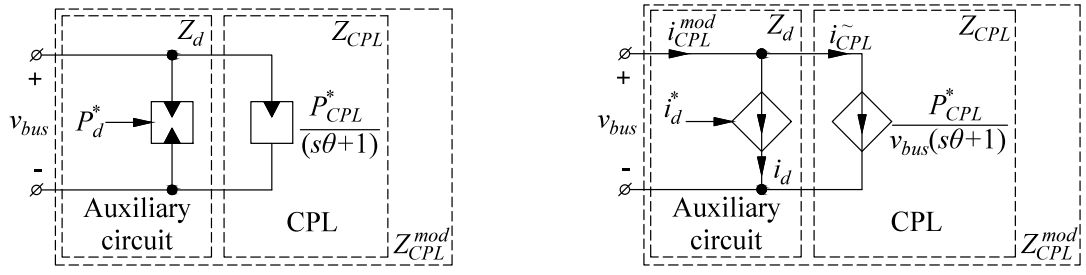


Figure 3.2 A CPL as seen from the input terminals with controlled shunt damping auxiliary circuit connected to the bus: (a) its equivalent power model; and (b) its corresponding ideal current source model.

From model depicted in Figure 3.2, it is obvious that the instantaneous total power is the sum of damping power and power consumed by CPL,

$$P_{CPL}^{\text{mod}} = P_d^* + \frac{P_{CPL}^*}{(s\theta+1)}. \tag{3.12}$$

Substituting (3.12) into (2.12) with $i_d = P^*_d / v_{bus}$ and $i_d = i_d^*$, the instantaneous value of current reference for the auxiliary circuit is found as

$$i_d^* = \frac{P_{CPL}^*}{v_{bus}(s\theta+1)}\left(\left(\frac{v_{bus}}{\tilde{v}_{bus}}\right)^u - 1\right) = \tilde{i}_{CPL}\left(\left(\frac{v_{bus}}{\tilde{v}_{bus}}\right)^u - 1\right). \tag{3.13}$$

The current source-based model of the proposed approach is shown in Figure 3.2 (b). Equation (3.13) determines the damping current command to the auxiliary circuit so that nonlinear active damping is achieved without changing the internal controls of the load. This is very beneficial especially for large scale DC distribution system where different companies design the components, and adjusting controls in every single building block becomes unrealistic.

3.2.2 Nonlinear and Small-Signal Models of the Active Damping Filter

In order to get a better understanding of the system's dynamic behavior, an impedance model is considered further. Specifically, we need to find the nonlinear damping branch impedance $\hat{v}_{bus} / \hat{i}_d$ and the total altered CPL impedance $\hat{v}_{bus} / \hat{i}_{CPL}^{\text{mod}}$. In Laplace domain, the circuit's behavior can be described as {see Figure 3.2 (b)}

$$\begin{cases} \tilde{v}_{bus} = \dfrac{v_{bus}}{s\tau+1} \\ \tilde{i}_{CPL} = \dfrac{i_{CPL}}{s\theta+1} \\ i_{CPL} = \dfrac{P_{CPL}^*}{v_{bus}} \\ i_d^* = \tilde{i}_{CPL}\left(\left(\dfrac{v_{bus}}{\tilde{v}_{bus}}\right)^u - 1\right) \\ i_{CPL}^{\text{mod}} = \tilde{i}_{CPL} + i_d^*. \end{cases} \tag{3.14}$$

Linearization of (3.14) yields

$$\begin{cases} \hat{v}_{bus}^{\sim} = \dfrac{\hat{v}_{bus}}{s\tau+1} \\ \hat{i}_{CPL}^{\sim} = \dfrac{\hat{i}_{CPL}}{s\theta+1} \\ \hat{i}_{CPL} = -\hat{v}_{bus}\dfrac{P_{CPL}^{*}}{V_{bus}^{2}} \\ \hat{i}_{d}^{*} = \hat{v}_{bus}\dfrac{P_{CPL}^{*}}{V_{bus}^{2}}u - \hat{v}_{bus}^{\sim}\dfrac{P_{CPL}^{*}}{V_{bus}^{2}}u \\ \hat{i}_{CPL}^{\text{mod}} = \hat{i}_{CPL}^{\sim} + \hat{i}_{d}^{*}. \end{cases} \tag{3.15}$$

As a result, the input impedance of the shunt current source is obtained as

$$Z_{d}^{*} = \frac{\hat{v}_{bus}}{\hat{i}_{d}^{*}} = \frac{V_{bus}^{2}}{P_{CPL}^{*}}\frac{(s\tau+1)}{su\tau} \tag{3.16}$$

and the input impedance of the modified CPL becomes

$$Z_{CPL}^{\text{mod}} = \frac{\hat{v}_{bus}}{\hat{i}_{CPL}^{\text{mod}}} = \frac{V_{bus}^{2}}{P_{CPL}^{*}}\frac{(s\tau+1)(s\theta+1)}{s\tau(u-1)-1}. \tag{3.17}$$

The DC gain of (3.16) and (3.17) is exactly the magnitude of CPL input impedance

$$\frac{V_{bus}^{2}}{P_{CPL}^{*}} = \left|\left|Z_{in}\right|\right| = R_{in}, \tag{3.18}$$

which is time-varying with respect to the system's operating point.

Based on further comparisons of transfer functions (2.11) and (3.16), a straightforward conclusion can be drawn: the nonlinear active controller in a form of shunt current source behaves very similar to a variable passive *RC* circuit, with its parameters described by

$$\begin{cases} R = \dfrac{V_{bus}^{2}}{P_{CPL}^{*}u} = \dfrac{R_{in}}{u} \\ RC = \tau \\ C = \dfrac{u\tau P_{CPL}^{*}}{V_{bus}^{2}} = \dfrac{u\tau}{R_{in}}. \end{cases} \tag{3.19}$$

3.2.3 Shaping the Constant Power Load Input Impedance

After having analytical insight into the behavior of proposed damping approach, we need to select the parameters u and τ so that our CPL input impedance has the desired shape. Further investigation of (3.17) allows us to express the gain (3.20) and phase (3.21) for modified CPL as

$$\left\|Z_{CPL}^{\text{mod}}\right\| = \frac{V_{bus}^2}{P_{CPL}^*}\sqrt{\frac{(\omega^2\tau^2+1)(\omega^2\theta^2+1)}{(\omega^2\tau^2(u-1)^2+1)}} \tag{3.20}$$

and

$$\Phi(Z_{CPL}^{\text{mod}}) = -\pi + \tan^{-1}(\omega\tau) + \tan^{-1}(\omega\theta) + \tan^{-1}(\omega\tau(u-1)). \tag{3.21}$$

The Bode plot of (3.17) for various u and fixed τ is depicted in Figure 3.3 (a). Looking at Figure 3.3 (a), it is obvious that the selection of parameter u impacts both magnitude and phase of the altered CPL input impedance. The modified CPL impedance increases as u increases for $0 < u < 1$ and decreased for $u > 1$. Furthermore, selecting $u = 0$ and $u = 0.5$ almost does not have impact on the CPL impedance phase shape. Starting from the value of $u = 1.5$ and higher, the phase converges towards 0 deg. Taking into account these impedance and phase characteristics, we can either increase impedance or shift the CPL phase towards zero to ensure stability of the system.

When shaping the CPL input impedance, our main objectives would be to keep its magnitude unchanged to maintain the same amplitude of current during transients, and ensure the phase angle is close to zero in the frequency region where the oscillations may occur (thus ensuring resistive behavior, i.e. $\Phi(Z_{CPL}^{\text{mod}})\Big|_{(\omega=\omega_{oscN}^{sys})} = 0$). From (3.20), it is seen that by setting $u = 2$ the main objective of maintaining the same CPL impedance magnitude can be achieved, which can be observed from Figure 3.3 (a). Then, by substituting $u = 2$, phase equation (3.21) can be transformed into

$$\Phi(Z_{CPL}^{\text{mod}}) = -\pi + 2\tan^{-1}(\omega\tau) + \tan^{-1}(\omega\theta). \tag{3.22}$$

Each term of (3.22) is shown in Figure 3.3 (b). Here, the part of curve $2\tan^{-1}(\omega\tau)$ where the phase changes from 0 to +180 degrees is represented with lower ω_A and higher ω_B frequencies, respectively, and can be approximated by a straight line with slope m as

$$\Phi(Z_{CPL}^{\text{mod}})\Big|_{\omega_A}^{\omega_B} = \frac{\pi}{2} + m\log\left(\frac{\omega}{\omega_C}\right). \tag{3.23}$$

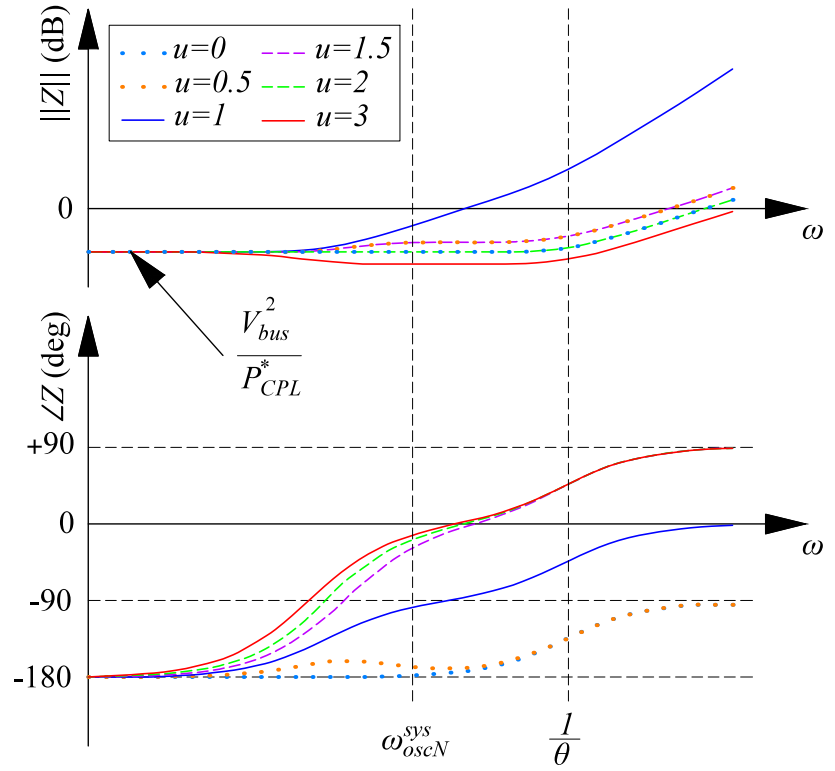
For our purposes, we will consider that the phase asymptote has the same slope as the actual curve at +90-degree point. Then, by taking the derivatives of $2\tan^{-1}(\omega\tau)$ and (3.23), and equating them, taking into account that $\omega = \omega_C$, we will find the solution for *m*. By knowing the slope, we can find the frequencies ω_A and ω_B where the phase crosses 0 and 180 degrees as

$$\begin{cases} \omega_A = \omega_C e^{-\pi/2} \approx 0.21\omega_C \\ \omega_B = \omega_C e^{\pi/2} \approx 4.81\omega_C. \end{cases} \tag{3.24}$$

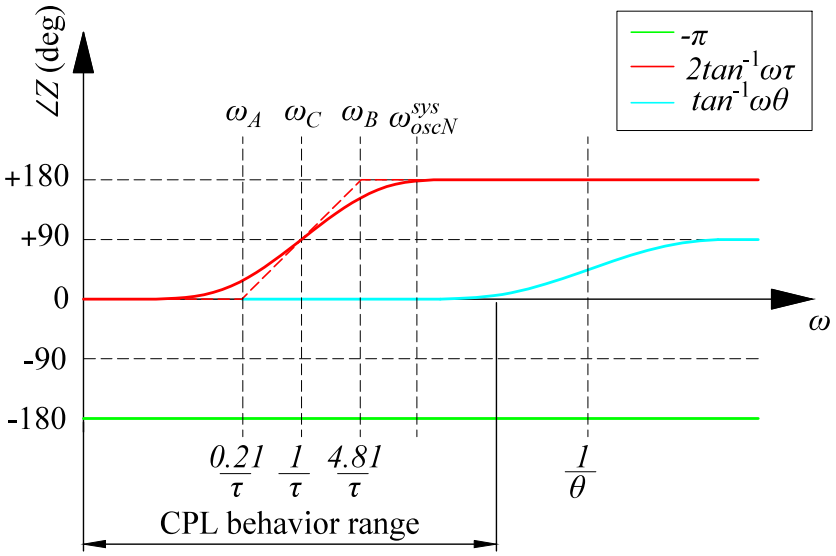
Consequently, if one considers $\omega_B \approx \omega_{oscN}^{sys}$ thus ensuring almost resistive behavior, τ can be expressed as

$$\tau = 4.81 / \omega_{oscN}^{sys}. \tag{3.25}$$

Therefore, equation (3.25) along with $u = 2$, sets forth the base for making the CPL behave similar to a resistor at the frequency range of interest. In addition to that, the nonlinear nature of ideal current source control yields its adaptive behavior and makes its operation automatically changing with respect to the operating point of the system. Finally, the derived non-linear damping methodology can also be used for calculating the linear (passive or active) damping *RC* parameters without involving any complicated numerical procedures. It is simpler to be used and can be used to stabilize the system "on fly" taking into consideration only the triggered unbounded oscillatory mode, which can be easily measured during the system's operation.



(a)



(b)

Figure 3.3 Input impedance characteristics of modified CPL: (a) its frequency response for different values of parameter *u*; and (b) its phase expressed using separate terms.

3.3 Simulation Studies with Constant Power Loads

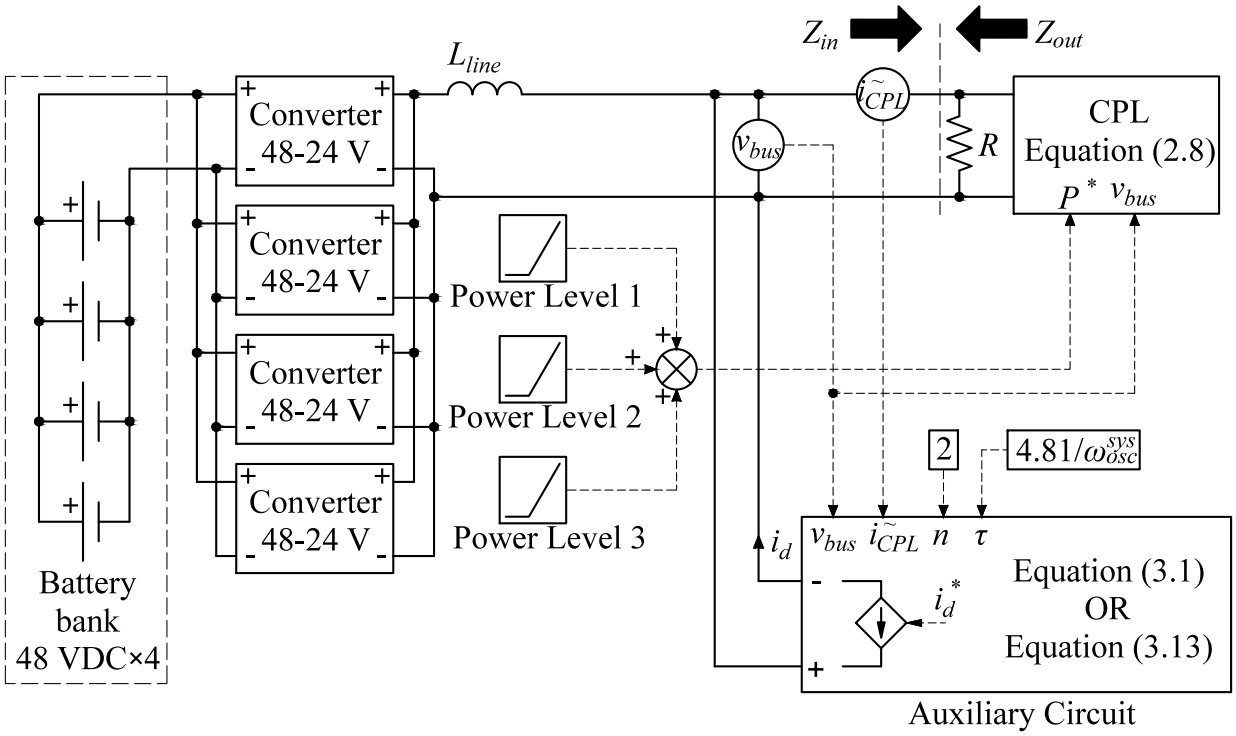


Figure 3.4 The considered DC system model used for verification of the proposed linear and nonlinear active damping techniques.

To verify the proposed linear and nonlinear active damping approaches, model of the 48-24 VDC power distribution system is considered in this section. This system is a part of the DC microgrid depicted in Figure 1.5. The high-level block diagram of this DC system model is depicted in Figure 3.4. The model was developed in MATLAB/PLECS simulation package based on procedures given in Chapter 2 and Chapter 3. The total power capacity of the bus is 8 kW and it can serve a combination of DC loads within its rated output. Here, the battery model is based on typical state-of-discharge curves with fixed internal resistance [41]. Since the battery has ultra-low impedance, the AC-DC rectifiers of the real system are neglected for the purpose of studies in this section. In addition, a 32 μH inductance is assumed for a 20-m-long and 80-mm^2 line cable. The self-inductance for the single cable is calculated [42] by

$$L_{line} = 2l\left(\ln\left(\frac{2l}{d}\left(1+\sqrt{1+\left(\frac{d}{2l}\right)^2}\right)\right)-\sqrt{1+\left(\frac{d}{2l}\right)^2}+\frac{\mu}{4}+\frac{d}{2l}\right), \tag{3.26}$$

where d is diameter of the cable, l is total length, and μ is absolute magnetic permeability of the conducting material of the cable. Also, a 0.65 kW resistive load was assumed connected on the bus at all times introducing some passive damping and softening the bus impedance. The CPL time constant θ was selected to be 10e-4 corresponding to the bandwidth of 3 kHz. The simulation is performed at 2.5, 5 and 7.5 kW CPL power levels, respectively. For these simulations, we used an ideal algebraic current source, which is commanded based on the system variables following equations (3.1) and (3.13). Two slew rates of 3.7 A/ms and 37 A/ms are applied separately to the CPL changes.

The corresponding simulated unstable voltage and power transient waveforms are shown in Figure 3.5 and Figure 3.6. As it can be seen, the system without damping becomes unstable after the second increase. In Figure 3.5, the oscillations start to grow instantaneously after second 5kW load is applied (large-signal load increase), whereas in Figure 3.6 the oscillations start to grow gradually (slow load application). In both cases, the dominating small-signal oscillatory mode was triggered by change of the system's state.

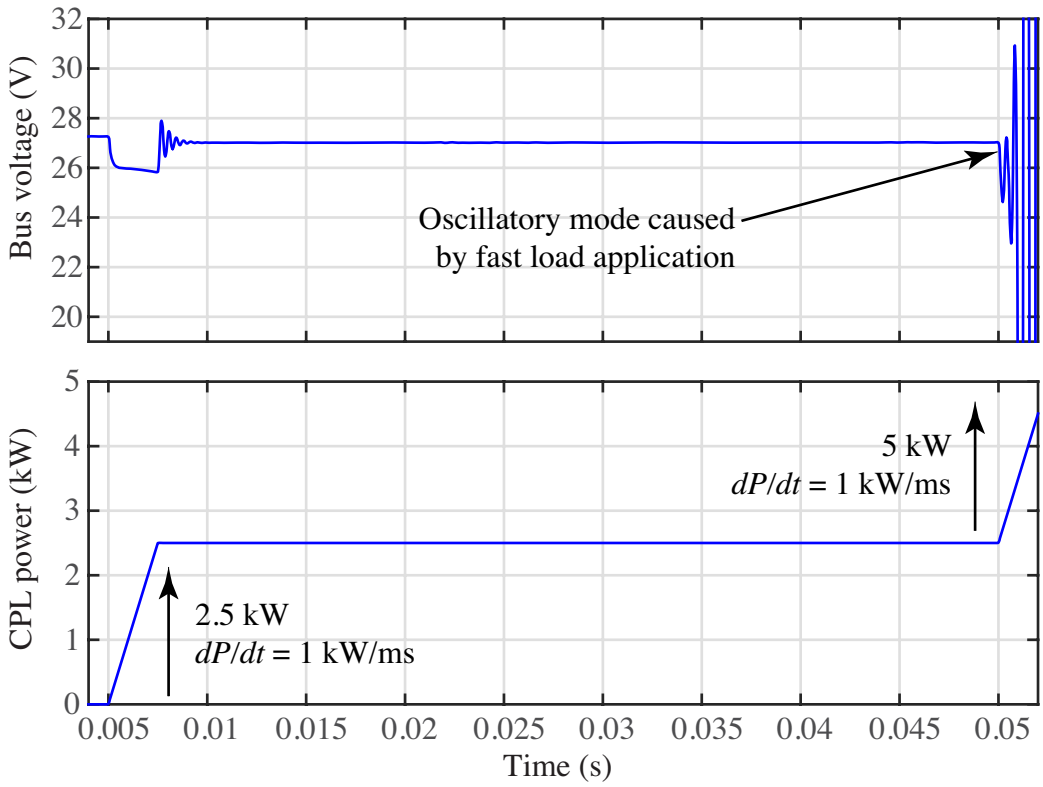


Figure 3.5 Unstable transient response during fast load increase with slew rate of 37 A/ms.

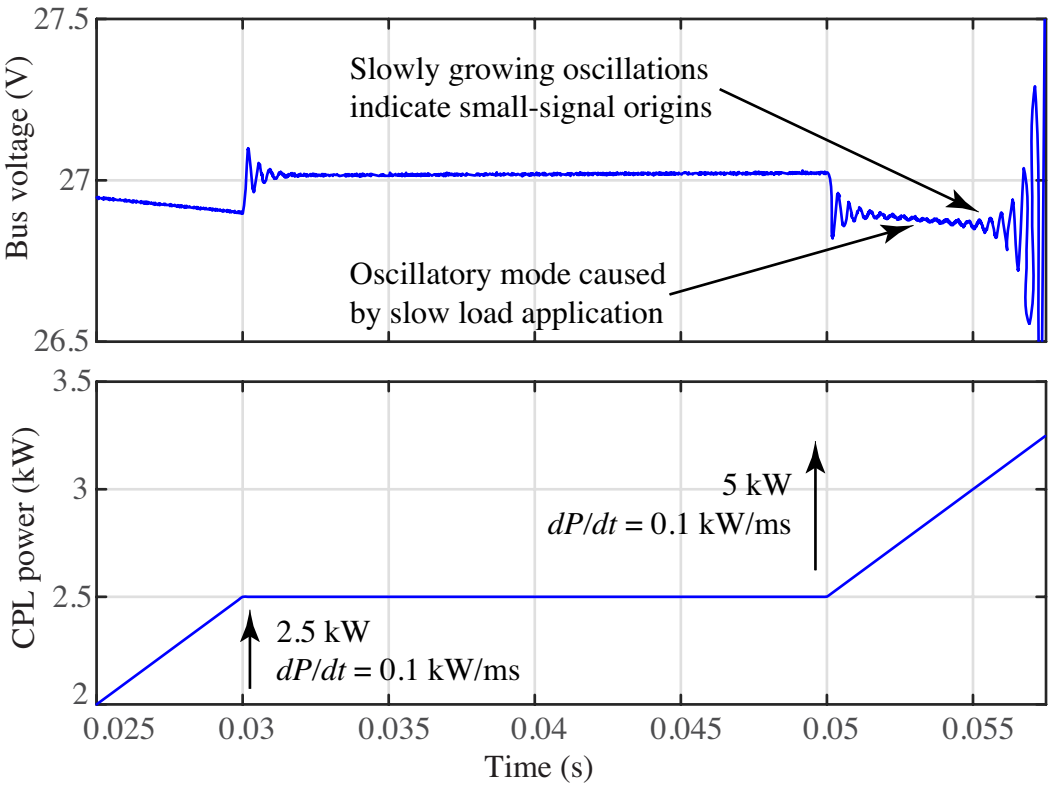


Figure 3.6 Unstable transient response during slow load increase with slew rate of 3.7 A/ms.

The impedances of the 24 VDC bus in small-signal sense was extracted from the average-value model by using system analysis tools of MATLAB. The small-signal minor loop gain of the above test is shown in Figure 3.7. Observing from the bode plot, the minor loop gain is under 0 dB at 2.5 kW, which means that the Nyquist criterion is satisfied at this state. However, the Nyquist criterion becomes unsatisfied at higher power levels with positive gain margin of 6 and 8 dB for 5 and 7.5 kW load levels, respectively. This is clearly caused by the decreased CPL input impedance and its -180 deg. phase shift bringing the system loop gain over the stability margin. Using the eigenvalue analysis of the un-damped minor loop gain Z_{out}/Z_{in}, the system oscillation frequency of 2.87 kHz is determined, which can be also observed from the bode plot in Figure 3.7.

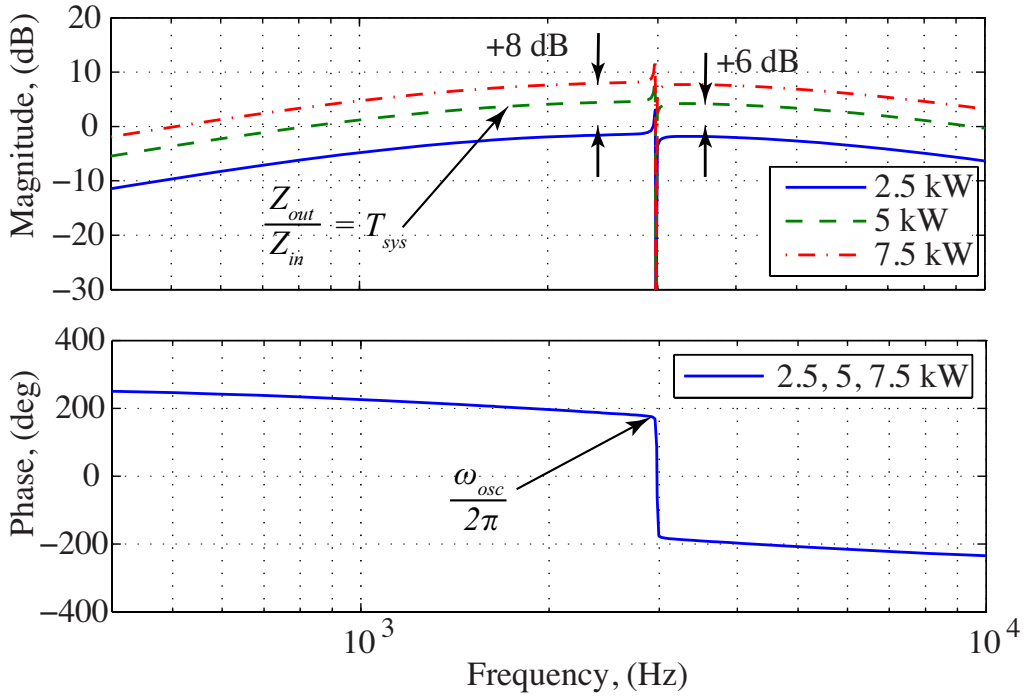


Figure 3.7 Minor loop gain T_{sys} of undamped DC distribution system.

3.3.1 Linear Damper with Fixed RC Parameters

To stabilize the system and obtain sufficient stability margins, the minor loop gain Z_{out}/Z_{in} must be reshaped using damping technique. In this study, we apply the active damping auxiliary circuit to emulate a passive *RC* damper. First, the parameters of the damping circuit must be calculated. Assuming that a -10 dB gain margin is required, and taking into account oscillation frequency $\omega_{osc1}^{sys} = 2\pi(2.87 \cdot 10^3)$, we can solve the system (3.10) for optimal *RC* parameters (MATLAB nonlinear least square solver LSQNONLIN is used). It is worth noticing that there is an alternative way to calculate *RC* damping parameters using (3.19), which is much simpler to utilize. The damping parameters calculated using both methods are summarized in Table 3.1.

	Hybrid Routh-Hurwitz and Gain Margin Method		Equation (3.19)	
	5 kW	7.5 kW	5 kW	7.5 kW
R (Ohm)	0.1	0.07	0.07	0.05
C (μF)	3000	7000	4000	5200

Table 3.1 Calculated equivalent damping circuit parameters emulating linear *RC* shunt circuit.

The test with enabled active damping auxiliary circuit and parameters obtained by hybrid Routh-Hurwitz and Gain Margin Method is performed under the same conditions as in previous unstable study. The corresponding transients observed at the 24 VDC bus are shown in Figure 3.8 and Figure 3.9. As it can be observed, the damping circuit designed with 10 dB gain margin stabilizes the system in both slow and fast load application cases.

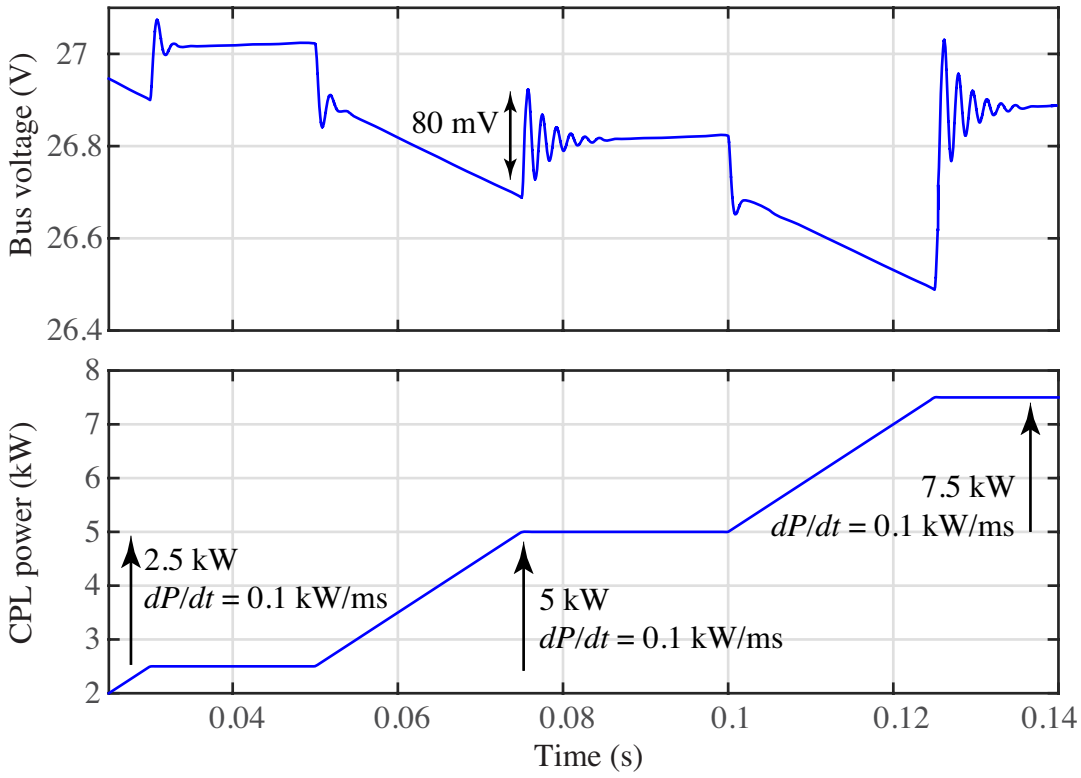


Figure 3.8 Stable transient response with active damping emulating fixed linear *RC* shunt during slow load changes with slew rate of 3.7 A/ms.

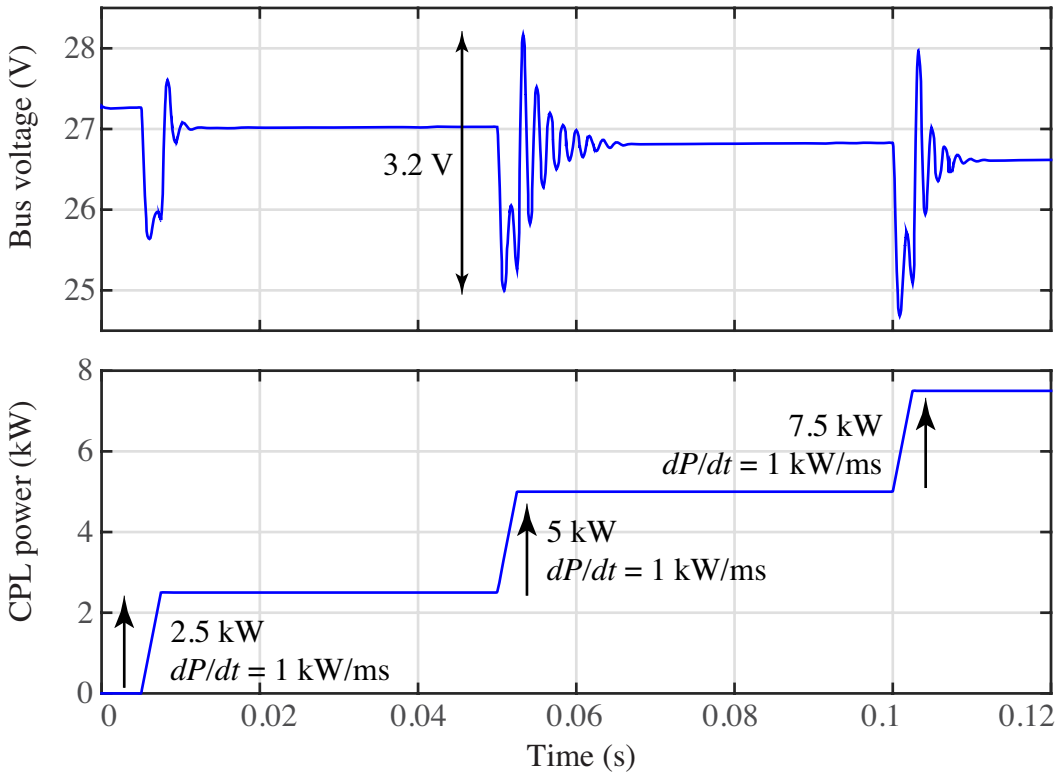


Figure 3.9 Stable transient response with active damping emulating fixed linear *RC* shunt during fast load changes with slew rate of 37 A/ms.

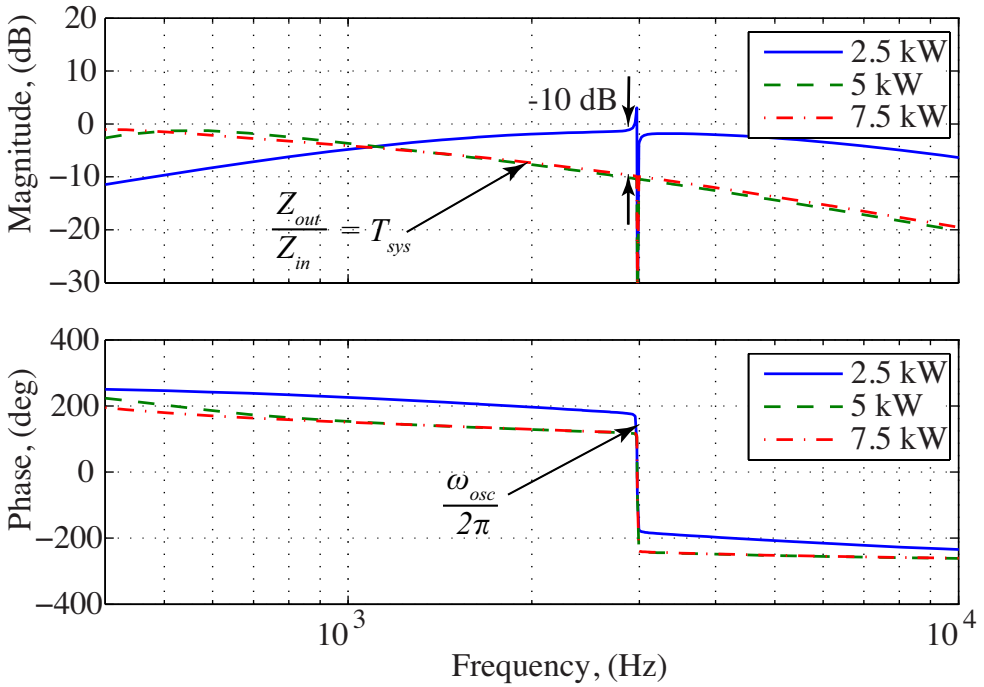


Figure 3.10 Minor loop gain T_{sys} of damped DC distribution system with -10 dB gain margin.

In addition, we extracted the minor loop gain for the stabilized system, which is shown in Figure 3.10. It is clearly seen that now the Nyquist stability criterion is fulfilled, i.e. $||T_m|| < 0$, with exactly -10 dB gain margin as calculated. This investigation shows that the *RC* parameters of the emulated damping circuit are sufficient to stabilize the DC distribution system.

To further investigate the effect of active linear stabilization, the damping current and damping power during step change from 5 to 7.5 kW are plotted in Figure 3.11. A passive *RC* damping circuit will have energy losses. The energy dissipation on the resistor of the passive *RC* damper is

$$E_d = R\int_{t1}^{t2} i_d^{\,2}\, dt, \tag{3.27}$$

where t_1 and t_2 respectively represent the start and end time of one transition period. Based on the results in Figure 3.11, the energy dissipation during one damping cycle is 0.028 J, which translates into approximately 0.1 kW power loss when the transient occurs once a second. However, the auxiliary circuit considered in this thesis would recycle this energy.

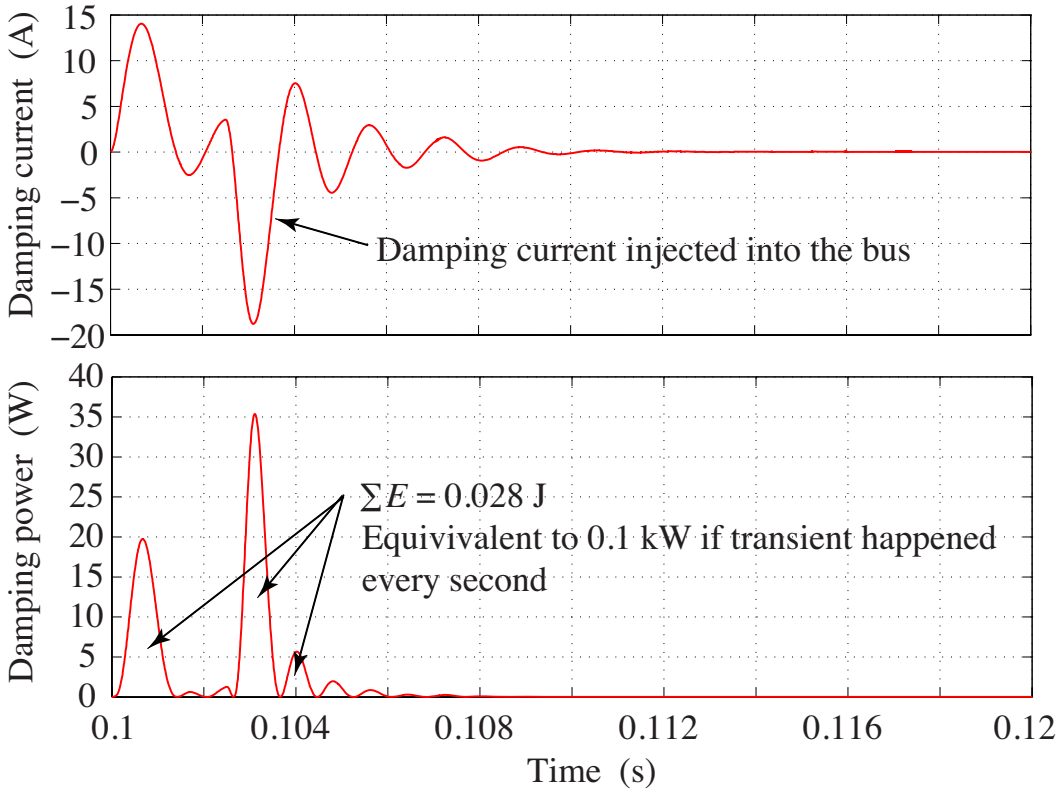


Figure 3.11 Linear damping current and power during CPL step change from 5 to 7.5 kW.

3.3.2 Adaptive Nonlinear Damper with Operating-Point-Dependent Parameters

After we have analyzed the system's behavior with linear damping, we conduct similar to Section 3.3.1 investigation with nonlinear damping current generation capability, which is calculated according to (3.13). In particular, the parameters τ and u are selected as per procedure given in Section 3.2 so that it matches the *RC* values obtained by Routh-Hurwitz Criterion for the previous experiment. The corresponding slow and fast transient responses are shown in Figure 3.12 and Figure 3.13. Comparing Figure 3.13 to Figure 3.9 reveals a significant advantage of the nonlinear approach: the bus voltage during the load increase to 2.5 and 5 kW does not fluctuate as much as it did when linear damping approach was utilized, which shows the advantage of using the adaptive damping parameters. Indeed, inspecting (3.13) we can see that the amplitude of the required damping current depends on instantaneous CPL current; while in linear fixed parameter case described by (3.1), all parameters are fixed. Therefore, we had to use the *RC* values calculated for worst-case scenario, i.e. 7.5 kW. Figure 3.14 shows the advantageous behavior the operating point-dependent damping parameters.

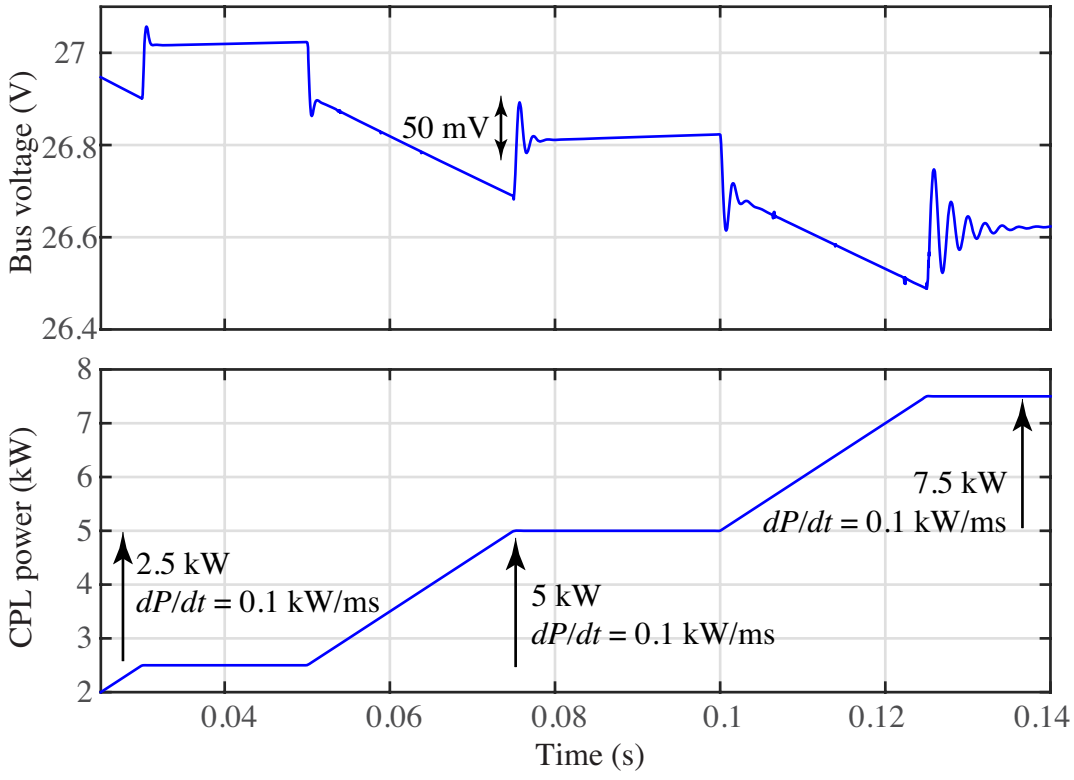


Figure 3.12 Stable transient response under nonlinear active damping during load step change with slew rate of 3.7 A/ms.

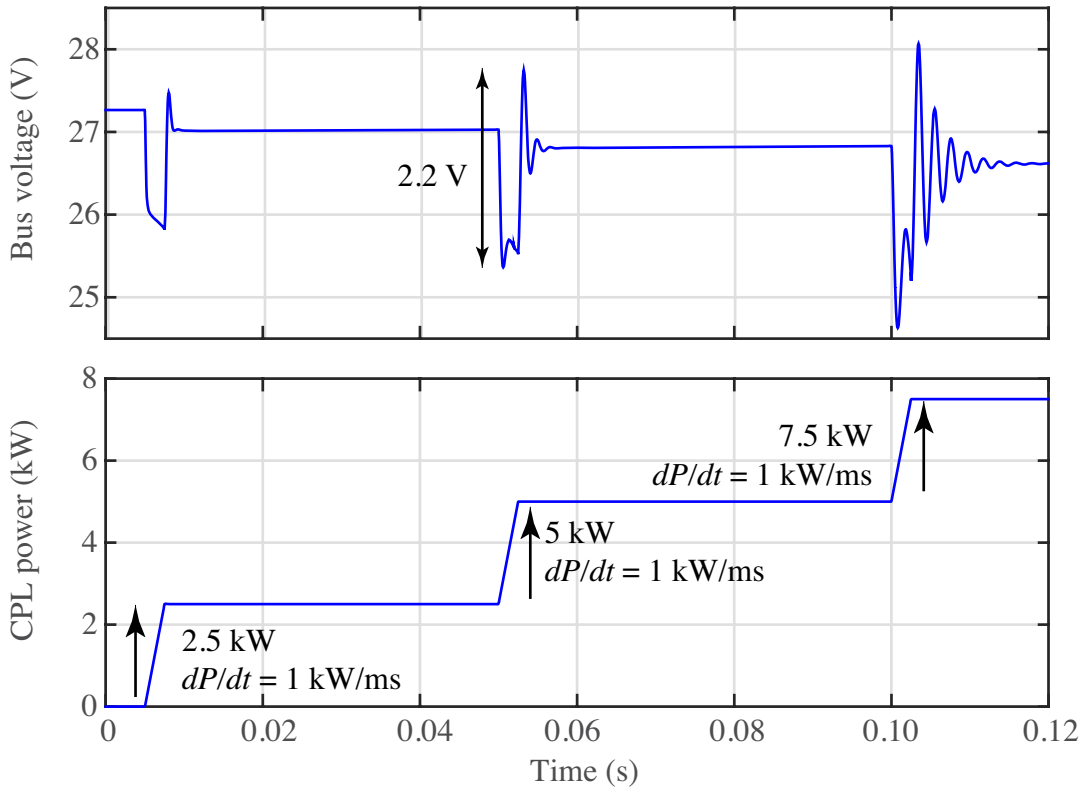


Figure 3.13 Stable transient response under nonlinear active damping during load step change with slew rate of 37 A/ms.

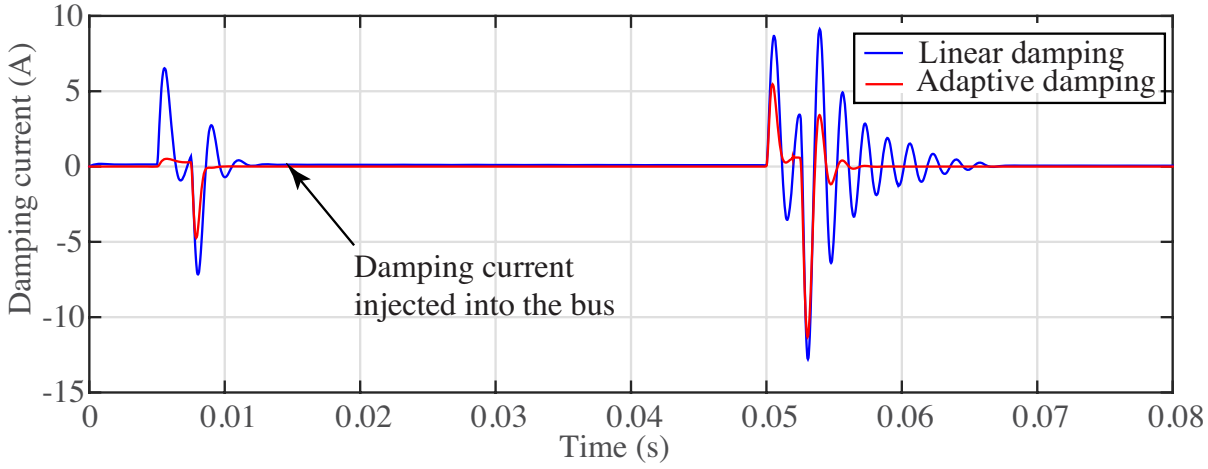


Figure 3.14 Damping current injected into the bus during 2.5 and 5 kW increases in load for adaptive and fixed damping parameters.

Chapter 4: Practical Implementation of the Proposed Active Damping

To verify the proposed active damping methodology based on active damper, we present an auxiliary converter circuit operating as a controlled current source. As shown in Figure 1.6, this converter circuit has terminals on two sides. One is side connected to the bus requiring damping of CPL, and the other side is connected to the strong power bus for energy balancing. The circuit consists of three parts: power stage, digital controller and output filter.

4.1 Proposed Power Stage and its Basic Analysis

The proposed auxiliary converter circuit shown in Figure 1.6 should be capable of bidirectional power flow. In this thesis, a simple bidirectional buck-boost topology shown in Figure 4.1 is chosen to verify the proposed active damping approach. In Figure 4.1, the voltage source v_s on the left hand side and v_l on the right hand side represent the high-voltage strong power bus and low voltage unstable bus, respectively. This topology is applicable to our prototype system where the high-voltage side is connected to the 48 V DC bus containing batteries, and the low-voltage side is the 24 V DC bus with CPL which may become unstable. For other applications requiring higher voltage gain, more complicated topologies with galvanic isolation may be used. In Figure 4.1, we have also included the parasitic resistances R_L, R_s and R_l for the main inductor L, the source v_s and the load v_l busses, respectively.

To understand the desired control strategy, we analyze the power stage of the buck-boost synchronous bi-directional converter and derive its small-signal model. It must be noted that this type of topology always works in CCM since at every instant of time either SH or SL switch conducts.

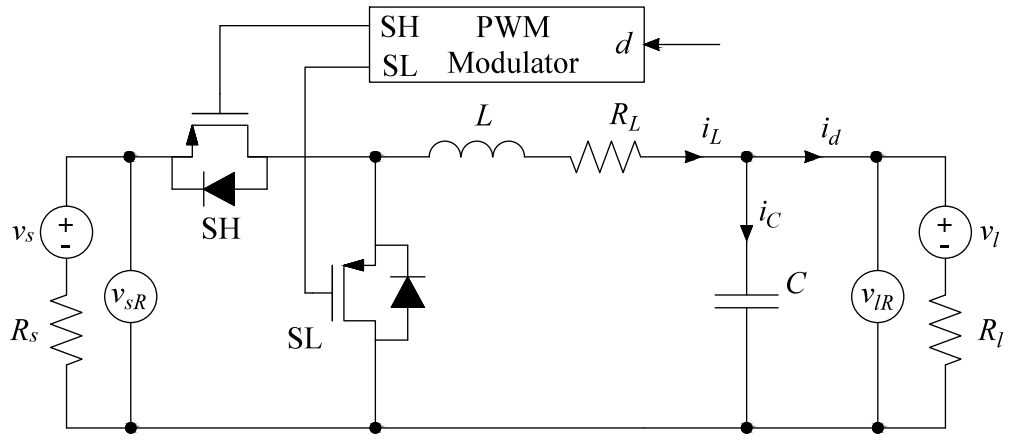


Figure 4.1 Power stage of the proposed auxiliary converter circuit using a buck-boost bidirectional topology.

4.1.1 Average Value Model

For a synchronous buck-boost converter, there are two subintervals within a switching period. During the first subinterval, the switch SH is ON and switch SL is OFF. Thus, for the first subinterval, the circuit in Figure 4.1 can be described by

$$\begin{cases} L\dfrac{di_L}{dt} = -i_L(R_L + R_s) + v_s - v_C \\ C\dfrac{dv_C}{dt} = i_L - \dfrac{v_C - v_l}{R_l}. \end{cases} \tag{4.1}$$

During the second subinterval, the switch SH is OFF and SL is ON. The converter is described by the following state equations

$$\begin{cases} L\dfrac{di_L}{dt} = -i_L R_L - v_C \\ C\dfrac{dv_C}{dt} = i_L - \dfrac{v_C - v_l}{R_l}. \end{cases} \tag{4.2}$$

Averaging over one switching period yields the following average value model

$$\begin{cases} L\dfrac{d\langle i_L\rangle}{dt} = -\langle i_L\rangle R_L - d\left(\langle i_L\rangle R_s + \langle v_s\rangle\right) - \langle v_C\rangle \\ C\dfrac{d\langle v_C\rangle}{dt} = \langle i_L\rangle - \dfrac{\langle v_C\rangle - \langle v_l\rangle}{R_l}. \end{cases} \tag{4.3}$$

In equilibrium, the system (4.3) becomes

$$\begin{cases} 0 = -I_L R_L - DI_L R_s + DV_s - V_C \\ 0 = I_L - \dfrac{V_C}{R_l} + \dfrac{V_l}{R_l}. \end{cases} \tag{4.4}$$

Then, (4.4) can be solved for inductor current as,

$$I_L = \frac{DV_s - V_l}{R_l + DR_s + R_L}. \tag{4.5}$$

4.1.2 Small-Signal AC Equivalent Model

When the converter is in equilibrium, separate DC and AC terms can represent each of its state and input variables such that (4.3) becomes

$$\begin{cases} L\dfrac{d(I_L + \hat{i}_L)}{dt} = -(I_L + \hat{i}_L)R_L - (D + \hat{d})\left((I_L + \hat{i}_L)R_s + (V_s + \hat{v}_s)\right) - (V_C + \hat{v}_C) \\ C\dfrac{d(V_C + \hat{v}_C)}{dt} = (I_L + \hat{i}_L) - \dfrac{(V_C + \hat{v}_C) - (V_l + \hat{v}_l)}{R_l}. \end{cases} \tag{4.6}$$

By neglecting high-order and steady state terms, (4.6) is simplified to

$$\begin{cases} L\dfrac{d\hat{i}_L}{dt} = -\hat{i}_L R_L - D(\hat{i}_L R_s - \hat{v}_s) - \hat{d}(I_L R_s - V_s) - \hat{v}_C \\ C\dfrac{d\hat{v}_C}{dt} = \hat{i}_L - \dfrac{\hat{v}_C}{R_l} + \dfrac{\hat{v}_l}{R_l}. \end{cases} \tag{4.7}$$

Thereafter, the standard state space form can be written as

$$\frac{d}{dt}\begin{bmatrix} \Delta i_L \\ \Delta v_C \end{bmatrix} = \begin{bmatrix} -\dfrac{R_L + DR_s}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_l C} \end{bmatrix}\begin{bmatrix} \Delta i_L \\ \Delta v_C \end{bmatrix} + \begin{bmatrix} \dfrac{V_s - I_L R_s}{L} & \dfrac{D}{L} & 0 \\ 0 & 0 & \dfrac{1}{R_l C} \end{bmatrix}\begin{bmatrix} \Delta d \\ \Delta v_s \\ \Delta v_l \end{bmatrix}. \tag{4.8}$$

The control input to inductor current transfer function can be derived from (4.8) by setting the redundant state variable to zero, i.e. $\hat{v}_s = 0$ and $\hat{v}_l = 0$, as

$$H_{id} = \frac{\hat{i}_L}{\hat{d}} = \frac{V_s - R_s I_L}{sL + R_L + DR_s + \dfrac{1}{sC + \dfrac{1}{R_l}}}. \tag{4.9}$$

From (4.5), it is seen that the system's parasitic resistances drastically affect the steady state inductor current. In practical applications, $R_L, R_s, R_l \to 0$, thus making the auxiliary circuit very sensitive to varying D and behave as an integrator with infinite DC gain. Equation (4.9) supports the aforementioned statement and tells us that the control scheme should be able to maintain the commanded damping current in order to stabilize the DC system. If we set d to be constant, i.e. $d(t) = D$, and integrate the first equation in (4.3) over one switching period neglecting R_L, we get more insight on how the duty cycle affects the circuit behavior,

$$\left\langle i_L \right\rangle_{T_{sw}} = \left\langle i_L \right\rangle_{T_{sw}}^{0} + \frac{D\left\langle v_{sR} \right\rangle - \left\langle v_{lR} \right\rangle}{L} T_{sw}. \tag{4.10}$$

From (4.10), it is easy to notice that if $D = D_0 = \frac{\left\langle v_{lR} \right\rangle}{\left\langle v_{sR} \right\rangle}$, the circuit will operate in steady state with previous inductor current value, i.e. $\left\langle i_L \right\rangle_{T_{sw}}^{0}$. If D deviates from its steady state value, the inductor current will start to change with the slope of $\frac{D\left\langle v_{sR} \right\rangle - \left\langle v_{lR} \right\rangle}{L}$. Therefore, for 48-24 V DC buck-boost converter, the steady state duty cycle is $D_0 \approx 0.5$.

4.2 Control of the Proposed Power Stage Auxiliary Circuit

The main objective of the auxiliary converter circuit is to have the average inductor current to follow the commanded value as close as possible. The two commonly-used techniques to control the output current of DC/DC converter with natural overcurrent protection include the peak current control mode (PCCM) [43] and the average current control mode (ACCM) [44]. Each of them has its own advantages and disadvantages, so more detailed consideration is needed to select the appropriate control method.

4.2.1 Peak-Valley Current Control Mode

The classic peak current control mode (PCCM) ensures that inductor peak current follows the reference. However, if we implemented this type of control in our bi-directional converter, we would see the actual average inductor current being shifted for a half of current ripple amplitude. In order to compensate for this phenomenon, another control loop is required, which

can significantly affect the circuit performance in terms of bandwidth and filtered current distortion.

In this section, instead of pure PCCM, we investigate a hybrid bi-directional peak-valley current control mode (PVCCM), where the peak or valley control is selected based on the sign of the commanded inductor current. If the current is positive – the PCCM is selected, and if negative – the valley current control mode (VCCM) is selected. Figure 4.2 shows the control diagram for the PVCCM utilizing the basic logic elements as well as two RS flip-flops. The commanded inductor current $i^*_{L\_peak}$ is compared to the measured instantaneous inductor current i_L^{sense} and the appropriate commands for switches SH and SL are generated. This method is applied to our buck-boost power stage topology, and the generated inductor current is shown in Figure 4.3.

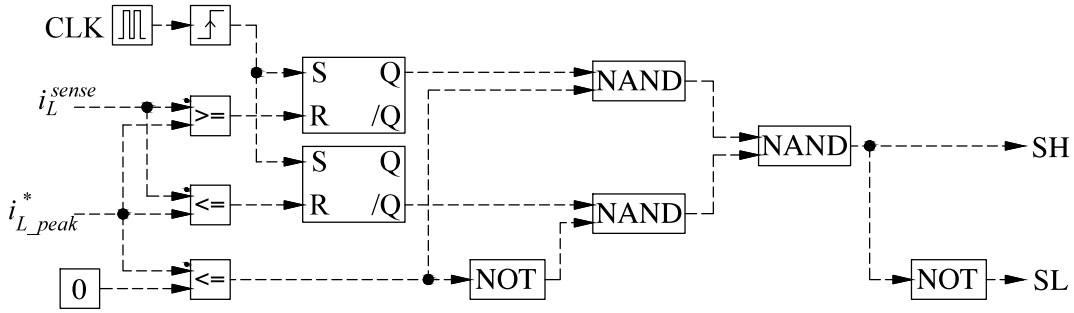


Figure 4.2 Simplified logic diagram implementing the peak-valley current control mode.

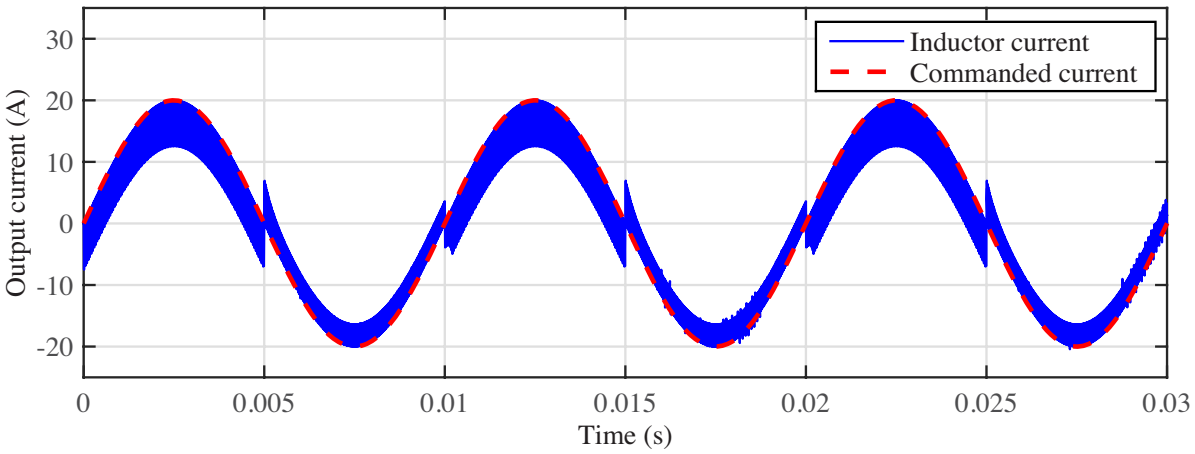


Figure 4.3 Buck-boost converter inductor current under PVCCM with f_{sw} = 80 kHz, v_s = 52 V, v_l = 27 V, L = 36 µH and i^* = 20sin(2π200).

As it can be seen in Figure 4.3, the anticipated average inductor current corresponds to the commanded current at zero-crossing points and it is symmetrical with respect to zero axis, which is not the case with PCCM where the whole waveform is shifted for a half of switching ripple amplitude. The average current amplitude can be corrected by outer control loop, but instead of correcting the vertical shift of the whole waveform, it will correct the current amplitude with respect to zero axis. Nevertheless, as it can be seen in Figure 4.3, the main disadvantage of PVCCM would be high distortion of the filtered bi-directional current waveform and extra need for slope compensation, which results in low-bandwidth performance and more complicated control of the auxiliary circuit. Therefore, a new strategy must be employed to achieve the desired performance characteristics.

4.2.2 Standard Average Current Control Mode

Even though analog ACCM has been developed as elaborated in [44], we will proceed with digital implementation as it offers flexibility of control, tolerance to components parameters variations and simplicity in hardware realization. A novel predictive digital current programmed control for non-synchronous buck-boost converter was presented in [45]. Using the methodology in [45], we re-derive the control strategy for the synchronous buck-boost converter operating in ACCM and improve its performance by introduction of the linear predictive technique of commanded current for the next switching cycle.

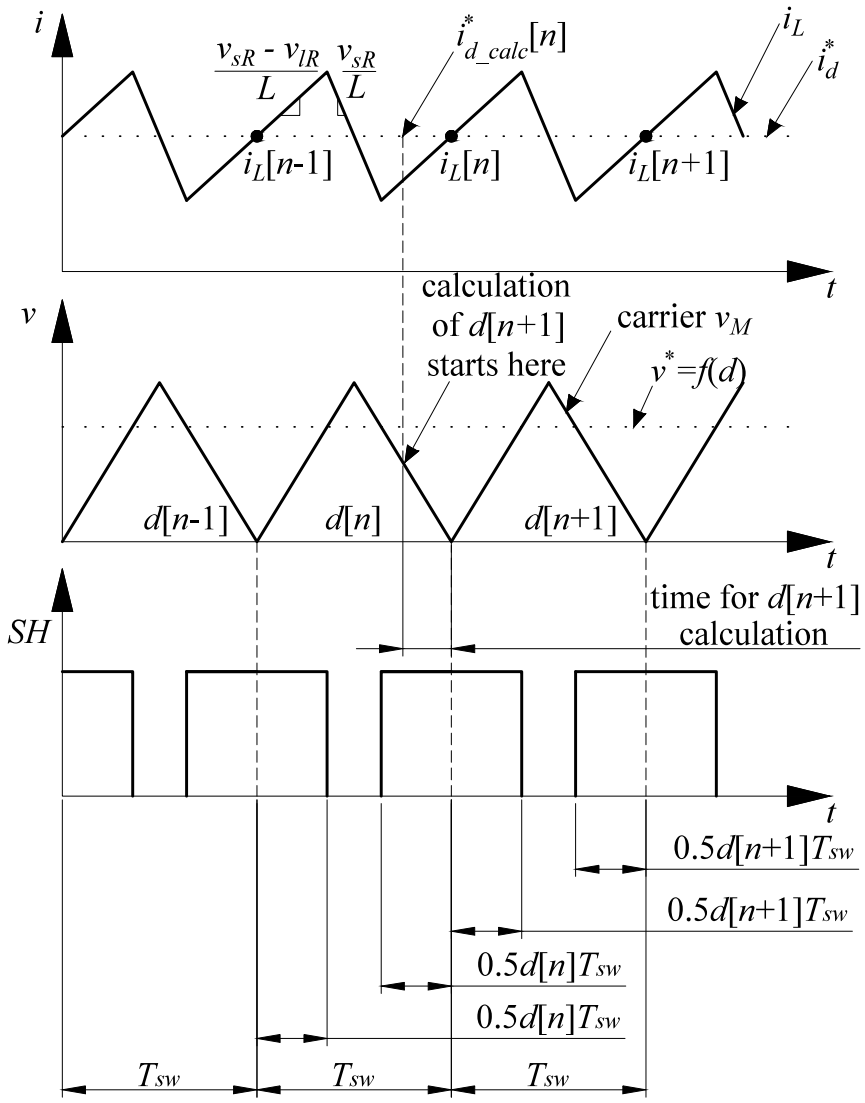


Figure 4.4 ACCM in buck-boost converter under triangular wave PWM.

The proposed ACCM strategy under the triangle modulation is shown in Figure 4.4. The duty cycle of switches is calculated cycle-by-cycle taking into account the desired average inductor current $\langle i_L \rangle$ which must be equal to commanded current i_d^* derived in Chapter 3. The derivation below neglects the effect of main inductor parasitic resistance, which will be eventually compensated by the outer control loop. It was proven in [45] that the system with this modulation is stable for the ACCM regardless of the duty ratio *d*. Taking into account the circuit

variables at the last switching cycle, the inductor current $i_L[n]$ sampled at points where $\langle i_L \rangle = i_d^*$, is predicted at the beginning of the n^{th} switching cycle as

$$i_L[n] = i_L[n-1] + \frac{(v_{sR} - v_{lR})d[n]T_{sw}}{L} - \frac{v_{lR}d'[n]T_{sw}}{L}, \tag{4.11}$$

where $d'[n] = 1 - d[n]$. Then, inductor current becomes

$$i_L[n] = i_L[n-1] + \frac{v_s d[n]T_{sw}}{L} - \frac{v_l T_{sw}}{L}. \tag{4.12}$$

Similarly, taking into account (4.12), the inductor current $i_L[n+1]$ can be formulated as

$$i_L[n+1] = i_L[n-1] + \frac{v_{sR}d[n]T_{sw}}{L} + \frac{v_{sR}d[n+1]T_{sw}}{L} - 2\frac{v_{lR}T_{sw}}{L}. \tag{4.13}$$

Then, the duty cycle $d[n+1]$ can be derived from (4.13) as

$$d[n+1] = -d[n] + \frac{(i_{d\_calc}^*[n] - i_L[n-1])L}{v_{sR}T_{sw}} + 2\frac{v_{lR}}{v_{sR}}, \tag{4.14}$$

where the future average inductor current is considered to be equal to the commanded current at the moment of calculation, i.e. $i_L[n+1] = i_{d\_calc}^*[n]$. Since the actual value of $i_d^*[n+1]$ cannot be sampled at the n^{th} period, in this thesis, the present command value $i_{d\_calc}^*[n]$ is used to approximate the required variable.

4.2.3 Proposed Corrected Average Control Mode with Current Prediction

From Figure 4.4, it is observed that the approximation of $i_{d\_calc}^*[n] = i_L[n+1]$ will cause $1.25T_{sw}$ time delay between the actual output and the reference current to the auxiliary circuit. In order to achieve the output tracking the reference, we should write $i_d^*[n+1] = i_L[n+1]$. The value of $i_d^*[n+1]$ is unknown at the moment of $d[n+1]$ calculation and must be precisely estimated via prediction. In this thesis, a linear extrapolation technique, as shown in Figure 4.5 is applied to achieve this prediction.

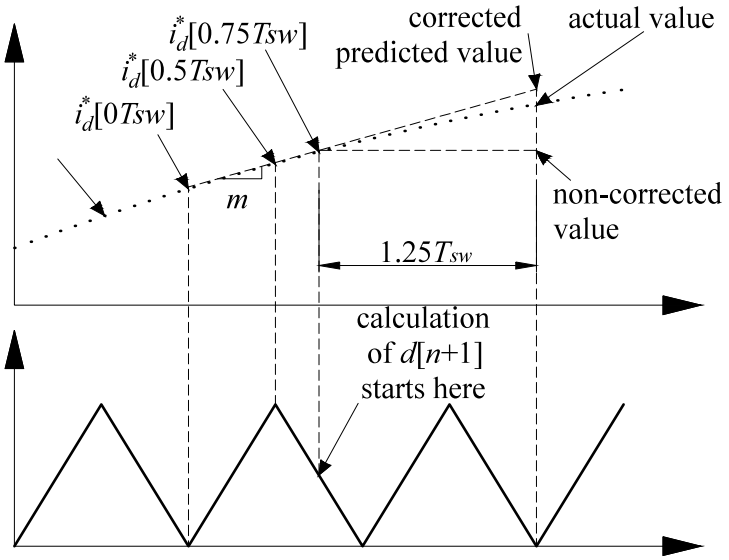


Figure 4.5 Commanded current value prediction by linear extrapolation

From Figure 4.5, the value of commanded current is estimated using the knowledge of the previous values as

$$i^*_{d\_calc}[n+1] = i^*_d[0.75T_{sw}] + 2.5(i^*_d[0.5T_{sw}] - i^*_d[0T_{sw}]). \tag{4.15}$$

Then, (4.14) can be extended to

$$d[n+1] = -d[n] + 2\frac{v_{lR}}{v_{sR}} - \frac{i_L[n-1]L}{v_{sR}T_{sw}} + \frac{(i^*_d[0.75T_{sw}] + 2.5(i^*_d[0.5T_{sw}] - i^*_d[0T_{sw}]))L}{v_{sR}T_{sw}}. \tag{4.16}$$

Figure 4.6 contains the time-domain comparison of the standard (4.14) and the proposed corrected (4.16) ACCM, where a sinusoidal waveform was selected as a current reference. Observing in Figure 4.6, the corrected ACCM has a noticeable advantage of almost zero phase lag of average inductor current in comparison to the standard control method. Therefore, proposed corrected ACCM is applied to our experimental prototype.

In the experimental prototype, the digital controller is implemented using a floating-point DSP TMS320F28335 from Texas Instrument. The PWM unit requires duty-cycle value before the beginning of each switching-period. Therefore, the PWM register of the DSP is overwritten with the $d[n+1]$ value obtained from (4.16) before the end of n^{th} switching period.

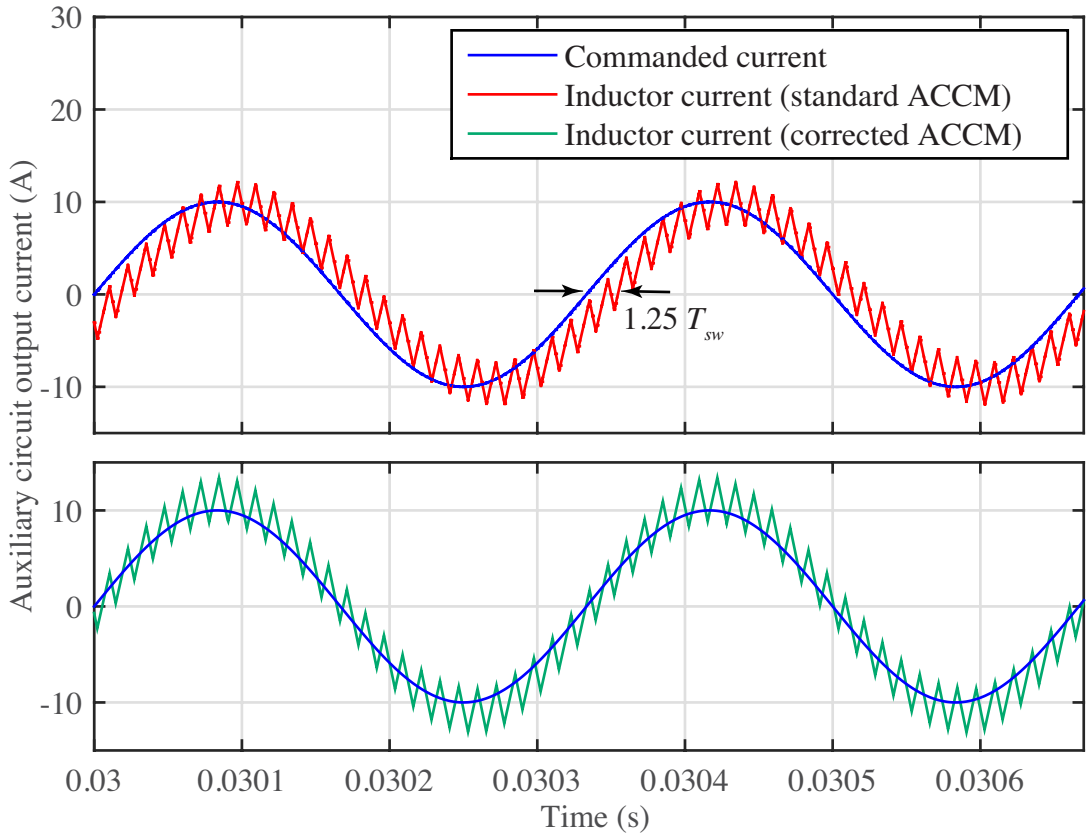


Figure 4.6 Comparison of standard and proposed corrected ACCM with f_{sw} = 80 kHz, v_s = 52 V, v_l = 27 V, L = 36 µH and i^* = 10*sin*(2π3000).

4.3 Output Filter Specifications and Design

The circuit shown Figure 4.1 requires a more advanced filter than just a capacitor to suppress the switching frequencies ripple. The filter must be designed so that, on the one hand, its cut-off frequency is located way before the switching frequency f_{sw}, but on the other hand, the lower frequencies are allowed to pass without attenuating the desired damping behavior of the auxiliary circuit. One of the most common types is an *LC* filter connected to the output of the converter. In our case, we will have the filter only on one low-voltage side, as the high-voltage side is a strong power bus with low impedance, thus insusceptible to high current ripple. The design procedure for *LC* filters is well elaborated in [21]. Two basic parameters of this filter are the cut-off frequency f_0 and characteristic impedance R_{0f} described by

$$\begin{cases} f_0 = \dfrac{1}{2\pi\sqrt{L_f C_f}} \\ R_{0f} = \sqrt{\dfrac{L_f}{C_f}}. \end{cases} \tag{4.17}$$

The input impedance of a circuit of interest is not affected as long as the filter's characteristic impedance is much lower. If one considers the synchronous buck-boost converter shown in Figure 4.1, the converter's input impedance as seen from the low side will be [21]

$$Z_e = Z_i\big|_{\Delta v_s=0} = sL. \tag{4.18}$$

Finally, one can solve (4.17) for filter parameters given the desired bandwidth of the auxiliary converter circuit, which sets the value of f_0 and the desired characteristic impedance to be $R_{0f} << \left|\left|Z_e\right|\right|\big|_{\omega=2\pi f_0}$.

After L and C parameters have been selected, a proper damping circuit must be design in order to reduce the Q-factor of the filter to an appropriate level. For this case, we will use a parallel damping branch with a blocking capacitor C_b and series a resistor R_f. Setting the maximum allowed peak output impedance of the filter $\left|\left|Z_0\right|\right|_{\max}$, one can find the values for the damper circuit as [21]

$$h = \frac{R_{0f}^2}{\left|\left|Z_0\right|\right|_{\max}^2}\left(1+\sqrt{1+4\frac{\left|\left|Z_0\right|\right|_{\max}^2}{R_{0f}^2}}\right), \tag{4.19}$$

$$R_f = R_{0f}\sqrt{\frac{(2+h)(4+3h)}{2h^2(4+h)}}, \tag{4.20}$$

$$C_b = hC_f. \tag{4.21}$$

Final version of the auxiliary circuit with low-pass filter, ACCM and nonlinear damping current calculator is shown in Figure 4.7. The circuit is connected to the stable strong power bus and the unstable bus: Equation (3.14) is used to calculate the required damping current to shape the CPL impedance. Equation (4.16) is used to calculate the proper duty ratio for the PMW generator based on the required damping current.

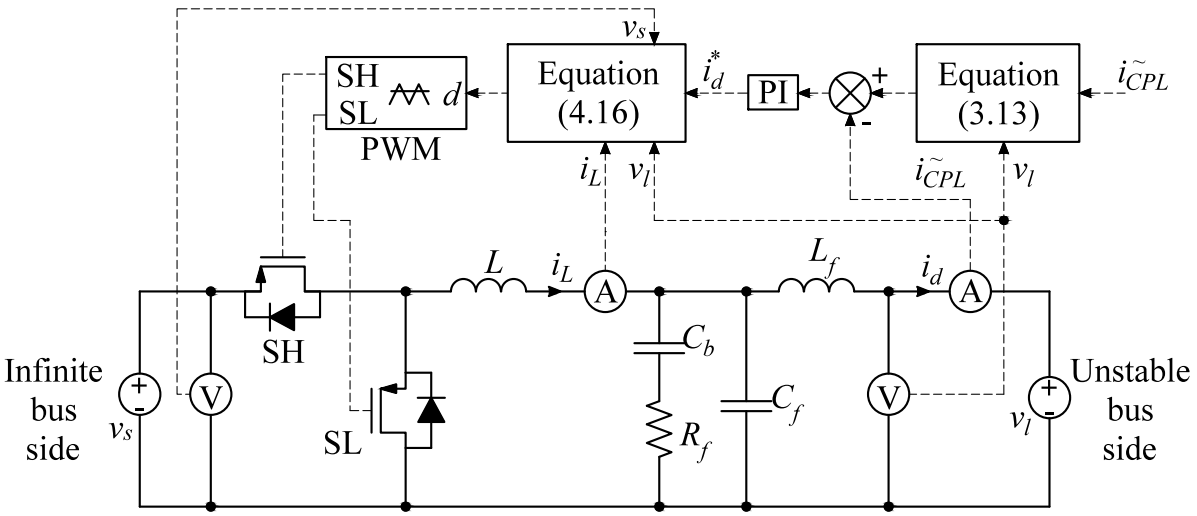


Figure 4.7 Complete diagram of the auxiliary converter circuit with controls.

Chapter 5: Hardware Verification of the Proposed Active Damping Methodology

5.1 Experimental Setup and its Components

A block diagram of the experimental setup used to verify the proposed active damping methodology is shown in Figure 5.1. The experiment in this thesis is performed on a scaled version of the system presented in Chapter 1 and 3. Specifically, the total power level is reduced from 8 kW to 2 kW and line inductance is increased from 32 μH to 80 μH and 52 μH for 1 kW and 1.6 kW tests, respectively. The line inductance of 80 μH corresponds to 42-m-long cable with 20-mm^2 cross-sectional area, and inductance of 52 μH corresponds to 28-m-long cable with 20-mm^2 cross-sectional area, respectively. The CPL is implemented as a buck converter being commanded constant output voltage, the amplitude of which is calculated from the load application ramp reference. The auxiliary converter circuit is connected to the strong power 48 VDC bus, which is used to stabilize the 24 VDC unstable bus loaded with CPL. During the experiment, we acquired the following waveforms: unstable bus voltage v_{bus}, source converter output voltage v_s, CPL input current $\tilde{i}_{CPL}$, and injected stabilizing damping current i_d. The auxiliary circuit's internal structure is depicted in Figure 4.7. The source converter has been comprehensively described in Chapter 2.

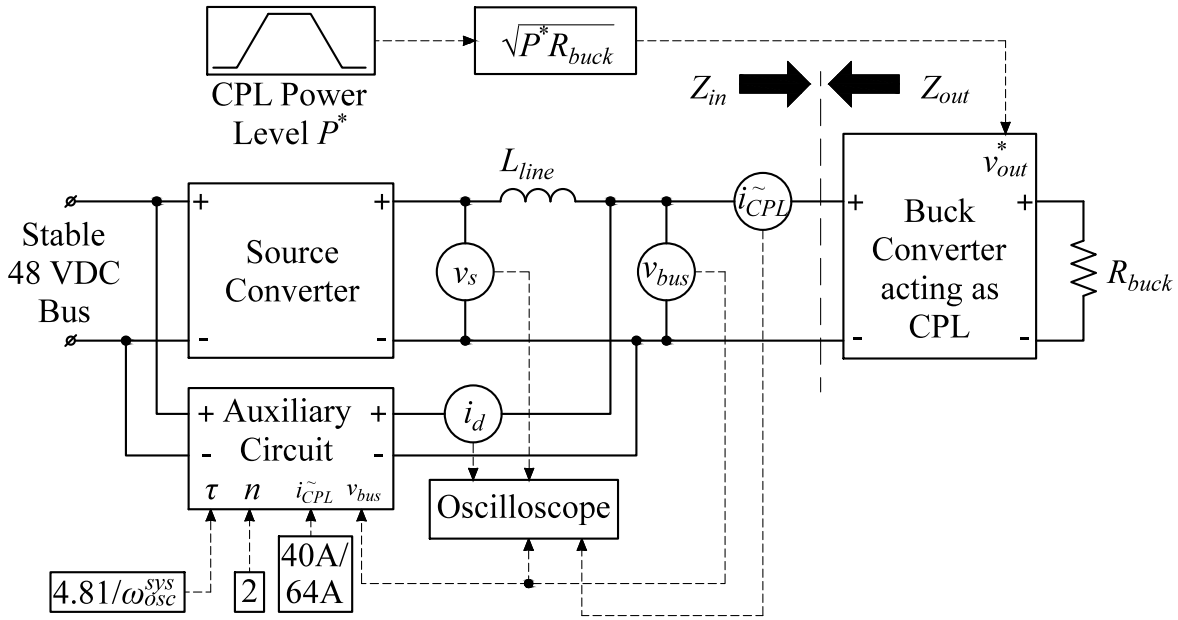


Figure 5.1 Block diagram of experimental setup used for verification of the proposed active damping methodology.

5.1.1 Load Setup Description

A voltage-mode buck converter feeding a resistor serves as the CPL. With its controller implemented using a DSP, the output voltage of the converter is tightly regulated at its reference v_{out}^* regardless of the filtered input voltage $v_{bus}^{\sim}$. Then, the duty cycle of the buck converter d_{buck} is calculated by a pure feed forward command as

$$d_{buck} = \frac{v_{out}^*}{v_{bus}^{\sim}}. \tag{5.1}$$

The control bandwidth of such CPL highly depends on the switching frequency. In our prototype, the 40 kHz switching frequency is applied, and the control bandwidth around 1 kHz is easily achieved. Both detailed and average models based on averaged switching cell [21] were constructed for the corresponding frequency analysis and simulations.

5.1.2 Hardware Realization of the Proposed Auxiliary Converter Circuit

The most important aspects of the auxiliary circuit design are the switching frequency, the main inductor, the output filter, and the damping current injection calculator. These parameters

will set the bandwidth of the circuit, and consequently determine whether or not it can follow the damping current reference generated as described in Chapter 3. The switching cell and output filter are designed based on the frequency response characteristics of the source/load system under study. Figure 5.2 depicts a Bode plot of the minor loop gain T_{sys} for 1 kW and 1.6 kW CPL power levels, respectively. It is observed that the oscillation may occur around 400 Hz, as the condition (2.10) is not fulfilled here. Final parameters of the experimental system are summarized in Appendix A.

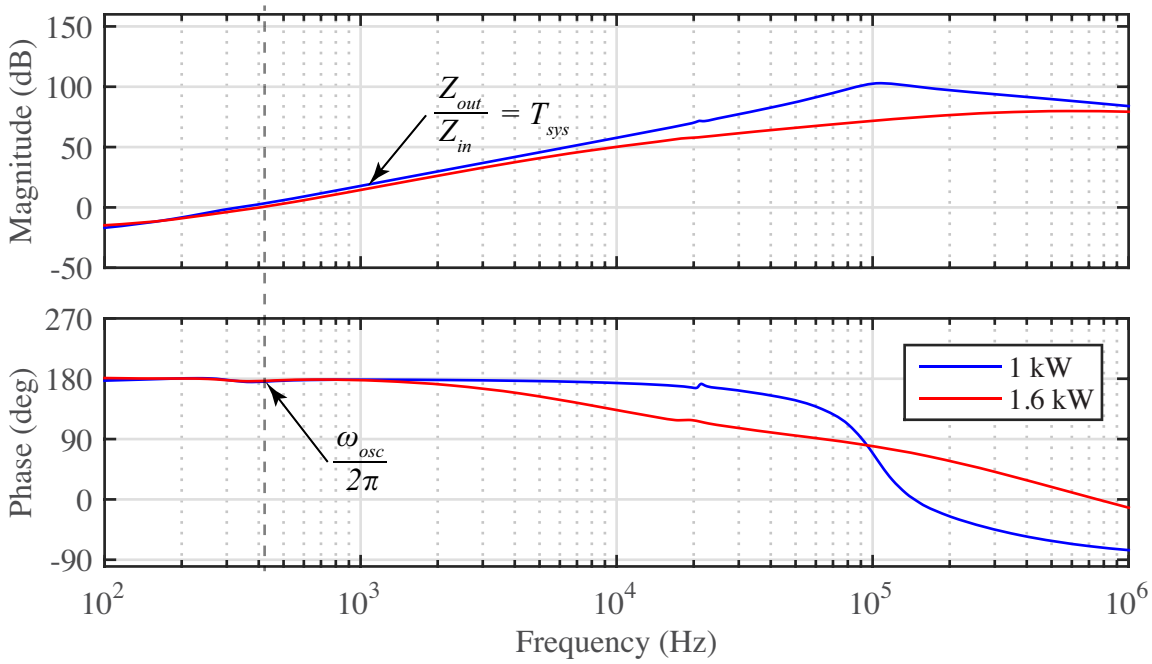


Figure 5.2 Simulated minor loop gain T_{sys} of the system under study.

Switching frequency: The switching frequency of the auxiliary converter circuit has to be much higher than potential frequency of one of the oscillatory modes of the system. In [46], it is recommended to have the switching frequency 800 times higher than the required frequency of sinusoidal current for the power factor correction (PFC) applications. Nevertheless, it was shown in [47] that the switching frequency can be further lowered by 3 times without losses in total harmonic distortion (THD). Our application requires generation of 400 Hz sinusoidal current and it does not have so stringent requirements on the THD. Therefore, in our experiment, also taking into account the improved corrected ACCM we set the auxiliary converter circuit switching to 80 kHz.

Main inductor: When switching frequency is fixed, the inductor can be selected based on the required current ripple Δi_L. Using basic analysis, and neglecting the parasitics, the output current ripple of the synchronous buck converter in Figure 4.1 can be derived as

$$L = \frac{(v_{sR} - v_{lR})dT_{sw}}{\Delta i_L}. \tag{5.2}$$

Using (4.10), we determined that the auxiliary converter circuit will almost always work around duty cycle D = 0.5. Taking into account that source and load voltages are relatively constant, we select the inductor so that its maximal average current $i_L = 0.25\tilde{i}_{CPL}$ and ripple $\Delta i_L = 0.2 i_L$.

Output filter: Having the frequency of potential CPL oscillations and switching frequency, we need to deign the filter so that switching harmonics are attenuated but the unstable oscillations frequencies will be passed, i.e. $f_{osc} < f_0 < f_{sw}$. We set $f_0 = 25\% f_{sw}$, $R_{0f} = 5\% \left\| |Z_e| \right\|_{\omega = 2\pi f_0} = 0.2$ Ohm, and solve for filter parameters by (4.17) – (4.21).

Damping current injection calculation: With the system oscillation frequency around 400 Hz, the parameters u and τ are selected using the procedure introduced in Chapter 3. For the purpose of experiment simplification, we limited the CPL current used in (3.13) at the value of 40 A for 1 kW and 64 A for 1.6 kW, respectively. Ultimately, the current $\tilde{i}_{CPL}$ as well as frequency of oscillations can be measured or estimated in real time and then application of (3.13) will yield adaptive behavior.

5.2 Experimental Case Studies

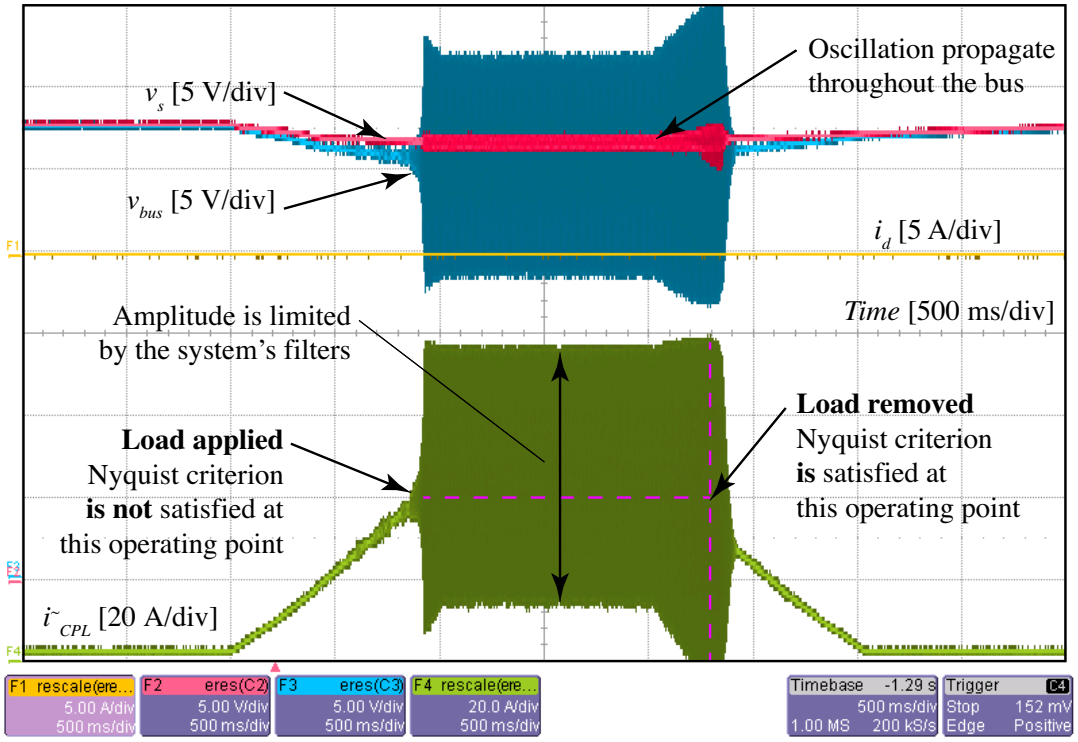
The prototype DC system described in previous chapter (see Appendix B), was built in order to verify the viability of proposed approach. The experiment is organized as follows: Firstly, we study the gradual load application without damping and verify the unstable behavior of the system. Then both slow and fast load applications are investigated with the proposed auxiliary converter circuit activated. To verify our analysis, the obtained experimental results are compared against simulations. All simulations are conducted at two power levels with different line inductances for each case.

5.2.1 Investigation of Unstable Operation

The first set of experiments was conducted with the load applied with the slew rate of 1 W/μs. The corresponding waveforms are depicted in Figure 5.3 and Figure 5.4, which clearly demonstrate the unstable response of the system to the increase of the CPL load. At the same time, the simulations were run to verify the model described in this thesis. From the Figure 5.3 and Figure 5.4, it is clear that the oscillations start to grow when condition (2.10) is not fulfilled anymore. Once the CPL load is decreased, the oscillations decay from the power level below which the condition (2.10) is satisfied.

Figure 5.5 and Figure 5.6 present the details on the power level where the instability starts to grow. As it can be seen, the oscillatory mode happens even during very slow transient proving that the CPL instability caused by the impedance interaction is a small-signal phenomenon. Nevertheless, it is worth noticing that the large signal transient around the unstable operating point will trigger the system's oscillatory modes. Both experimental results and simulations show that oscillations start to grow from the same operating point located at approximately 37 A for 1 kW and 60 A for 1.6 kW, respectively, which proves the consistency and validity of the experimental setup and its corresponding model.

In steady state, the amplitude of oscillations is limited by the CPL input filter and therefore the system does not blow up. Moreover, it can be seen that both output voltage v_s of the converter and voltage at the end of line cable v_{bus} oscillate. This observation demonstrates that even if one of the interfaces is unstable, the oscillatory mode may propagate throughout the entire system, potentially impacting its performance, power quality, and reliability. Due to the source converter output current protection, the oscillations on the edges of 1.6 kW load application profile are damped, and amplitude is lower than what we see in simulations. There is also a slight difference between the frequency of experimental oscillations, 285 Hz, and simulation ones – 400 Hz, which may be attributed to large scale of the system under investigation, significant parasitics and distributed parameters, which are not taken into account in simulations.



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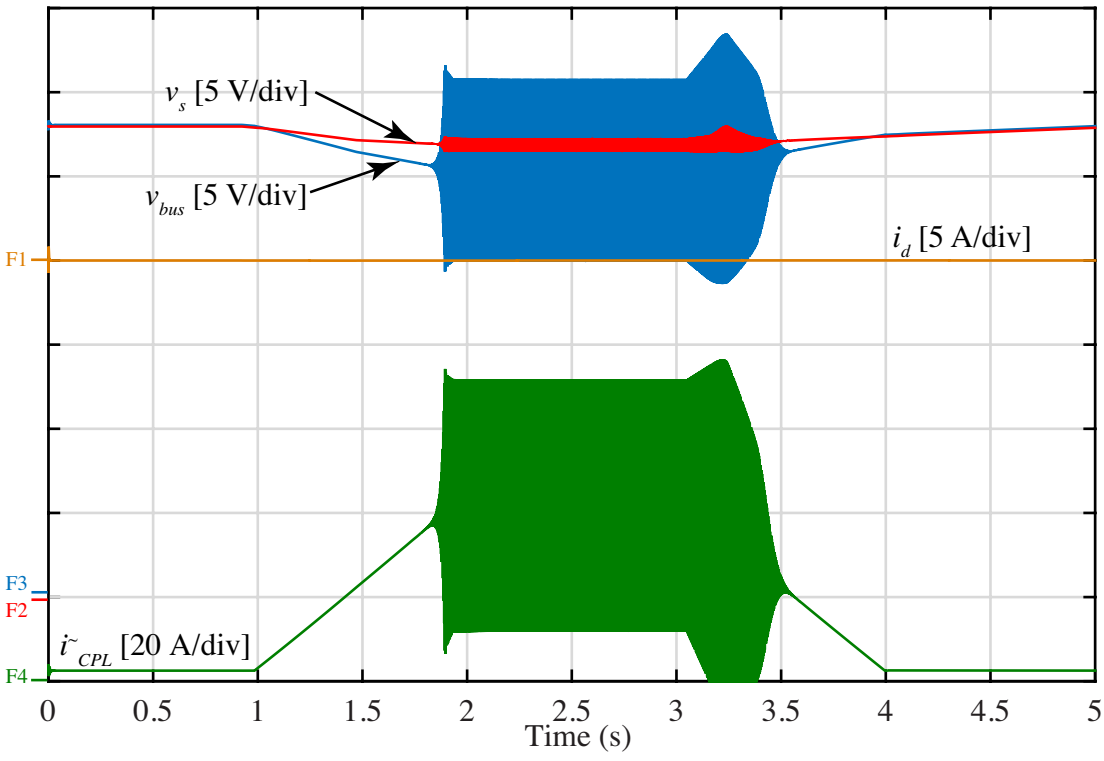
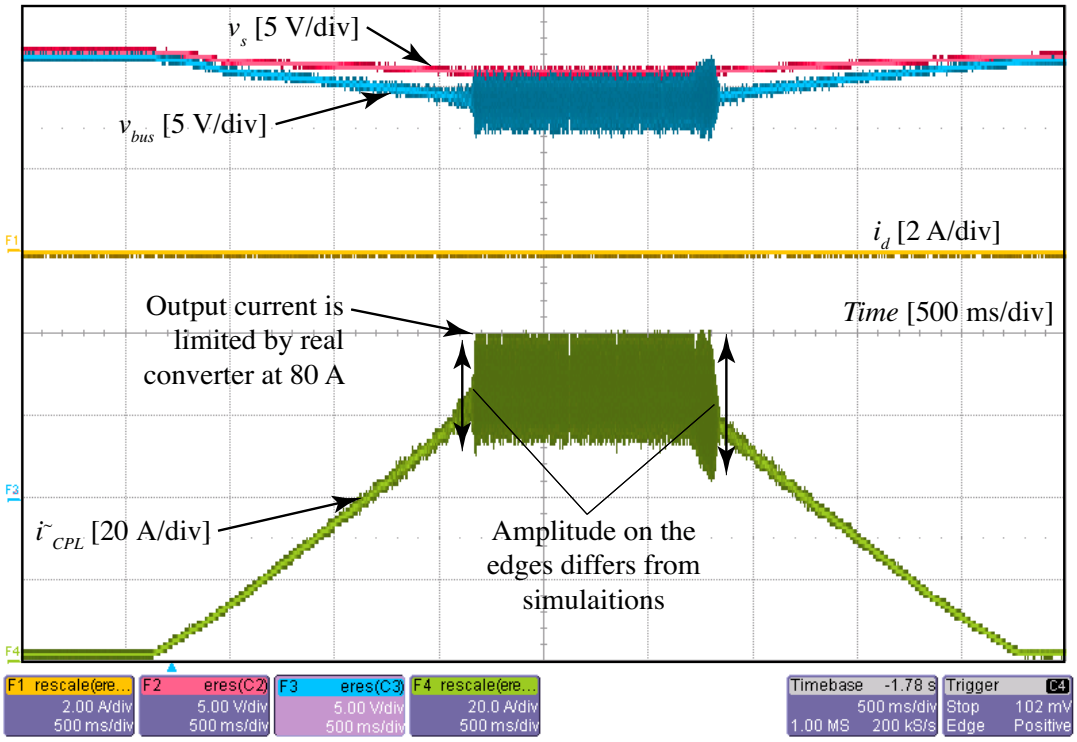


(b)

Figure 5.3 Unstable system response to 1 kW CPL applied at the slew rate of 1 W/ms: (a) experimental results; and (b) simulations for the same conditions.



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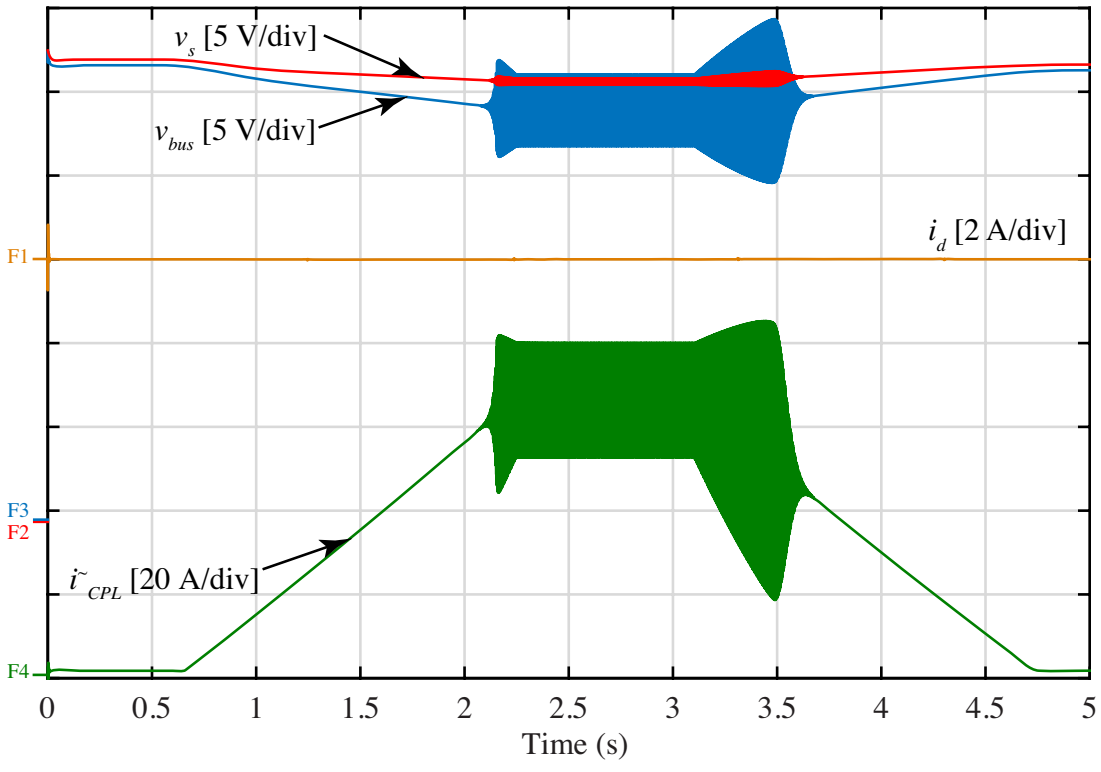
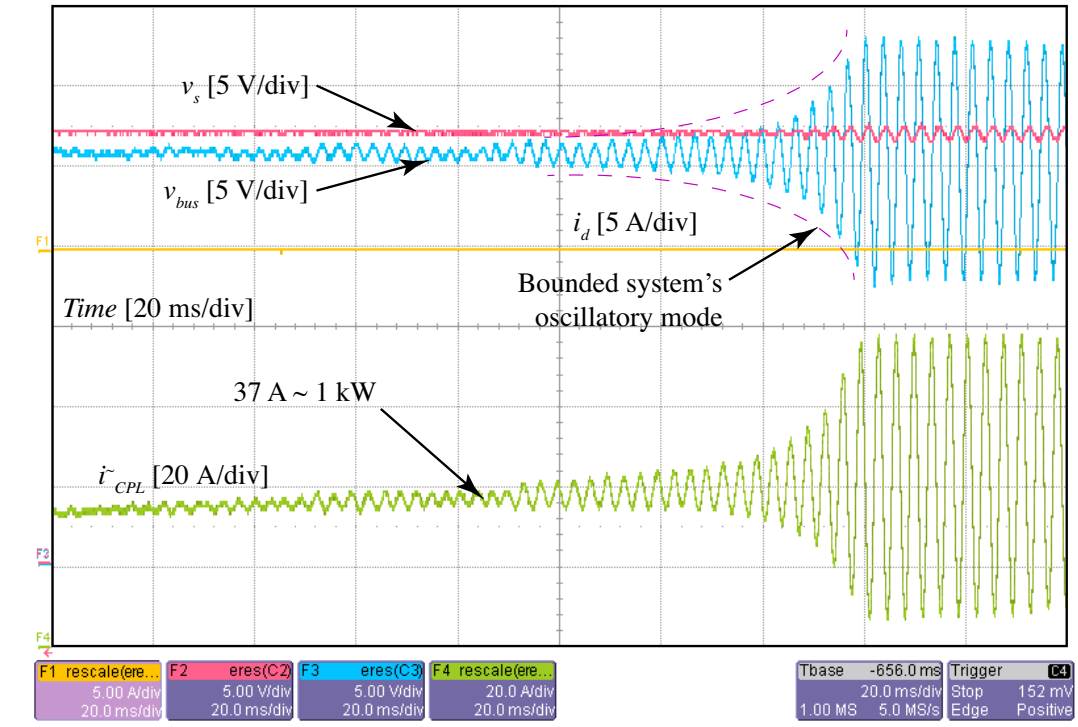


(b)

Figure 5.4 Unstable system response to 1.6 kW CPL applied at the slew rate of 1 W/ms: (a) experimental results; and (b) simulations for the same conditions.



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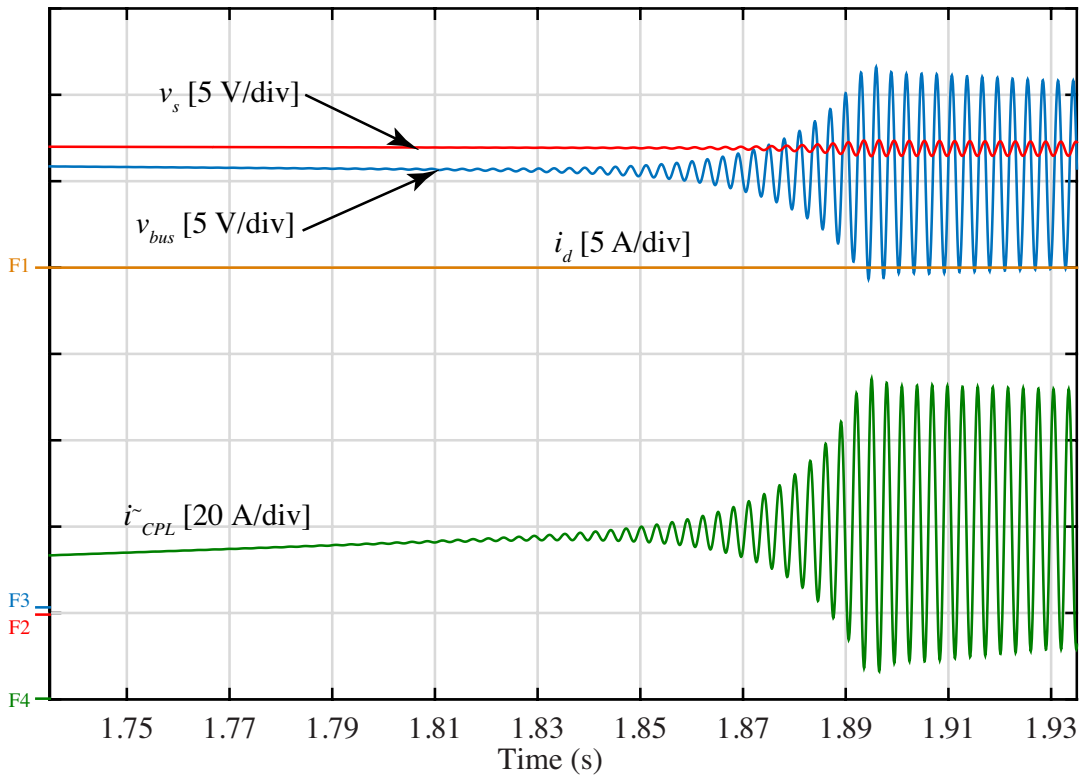
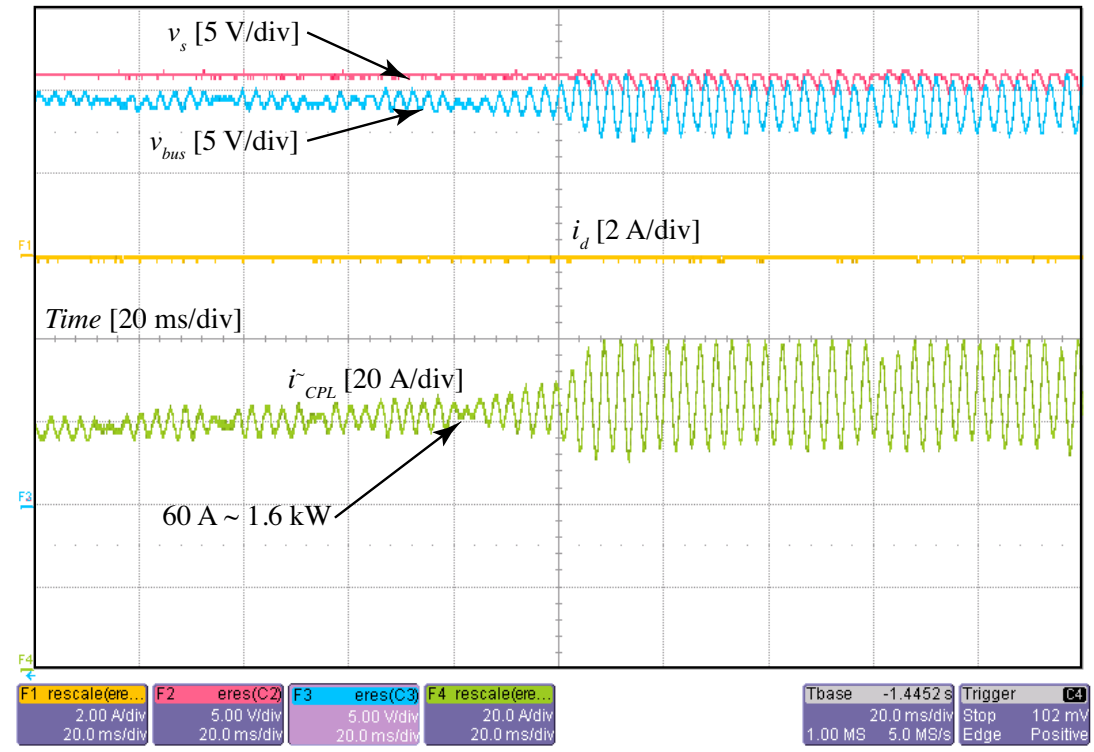


(b)

Figure 5.5 Details on unstable system response to 1 kW CPL applied at the slew rate of 1 W/ms: (a) experimental; and (b) simulations for the same conditions.



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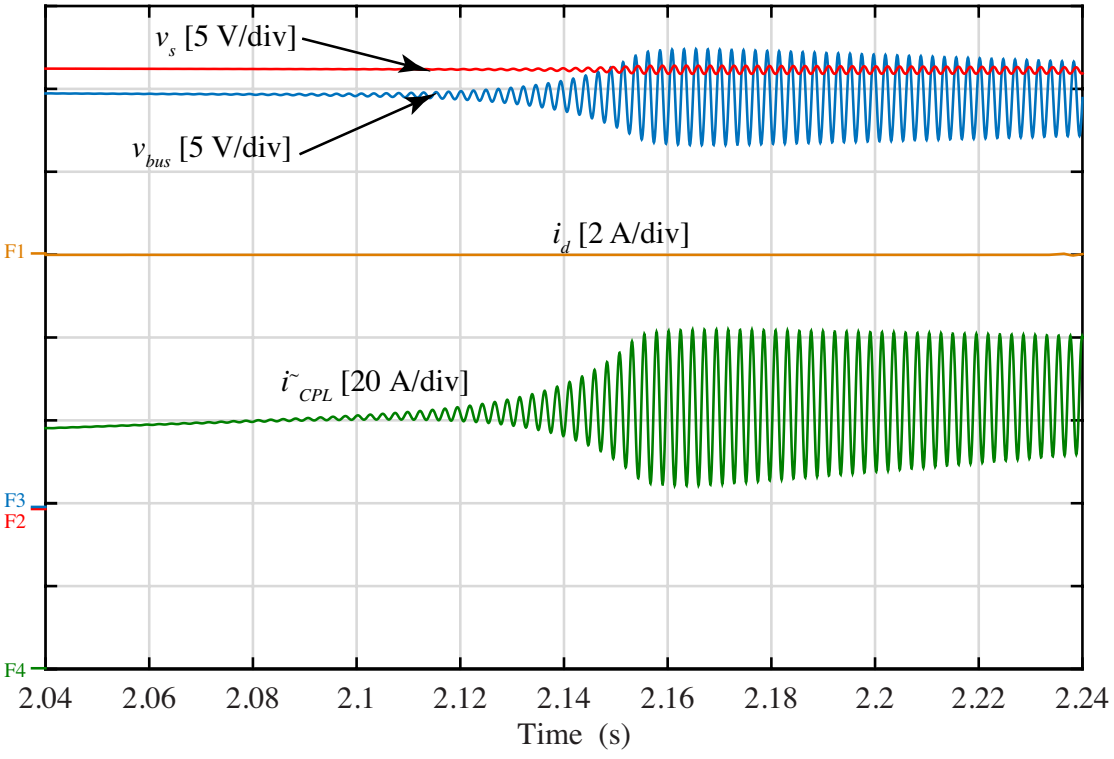


(b)

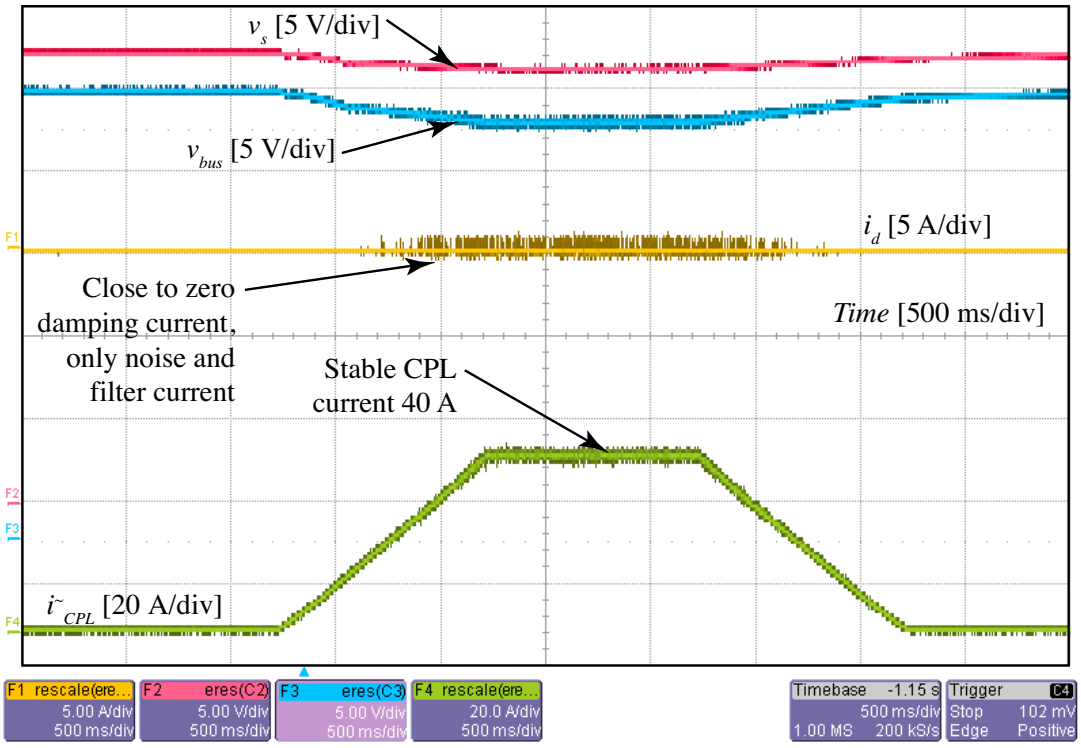
Figure 5.6 Details on unstable system response to 1.6 kW CPL applied at the slew rate of 1 W/ms: (a) experimental; and (b) simulations for the same conditions.

5.2.2 Stable Operation with Proposed Auxiliary Converter Circuit

Finally, a series of studies has been conducted with the proposed auxiliary converter circuit, active damping current of which is generated according to (3.13) with fixed values of CPL current at 40 A for 1 kW and 64 A for 1.6 kW tests, respectively. The equivalent emulated resistor and capacitor are R_{eq} = 0.33 Ohm and C_{eq} = 6000 uF for 1 kW study and R_{eq} = 0.2 Ohm and C_{eq} = 8100 uF for 1.6 kW study, respectively. Figure 5.7 and Figure 5.8 show the results of slow CPL application with the slew rate of 1 W/ms. Figure 5.9 to Figure 5.12 show the results of fast CPL application with the slew rate of 100 W/ms.

As seen in Figure 5.7 and Figure 5.8, during the slow CPL load increase (emulating small-signal disturbances), substantial damping current is not observed and the required energy for suppressing the potential oscillations is very low. The damping current ripple still exists because of the auxiliary converter circuit output filter passive elements.

During fast CPL load increase (emulating large-signal disturbances), a noticeable damping current becomes present as shown in Figure 5.11 and Figure 5.12. The amplitude of damping current depends on the speed of load transient and the auxiliary circuit damping parameters τ and u. It is worth stating that damping current differs for the 1 kW and 1.6 kW studies as the term $\tilde{i}_{CPL}$ in (3.13) varies depending on the operating power level of the system. However, it is clear that the damping current of the auxiliary converter circuit is relatively small with respect to the total power capacity of the system, which is very beneficial. Therefore, in addition to the previously mentioned advantages, the proposed methodology is very appealing in terms of size and components ratings.



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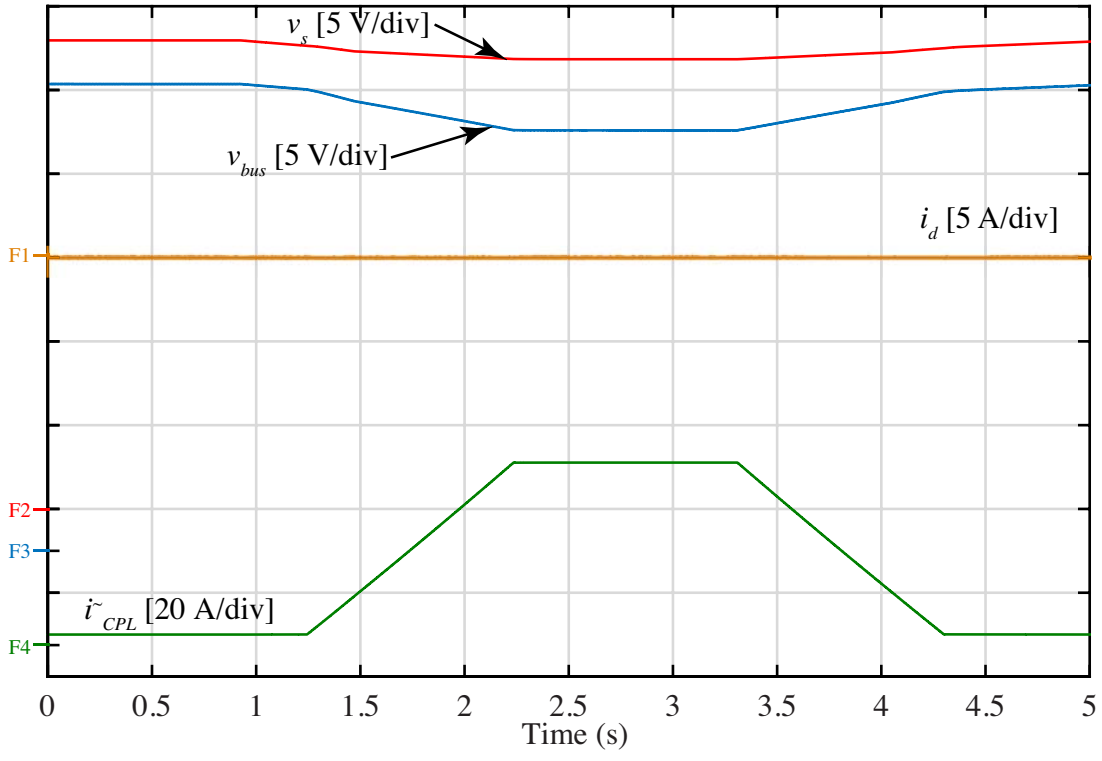

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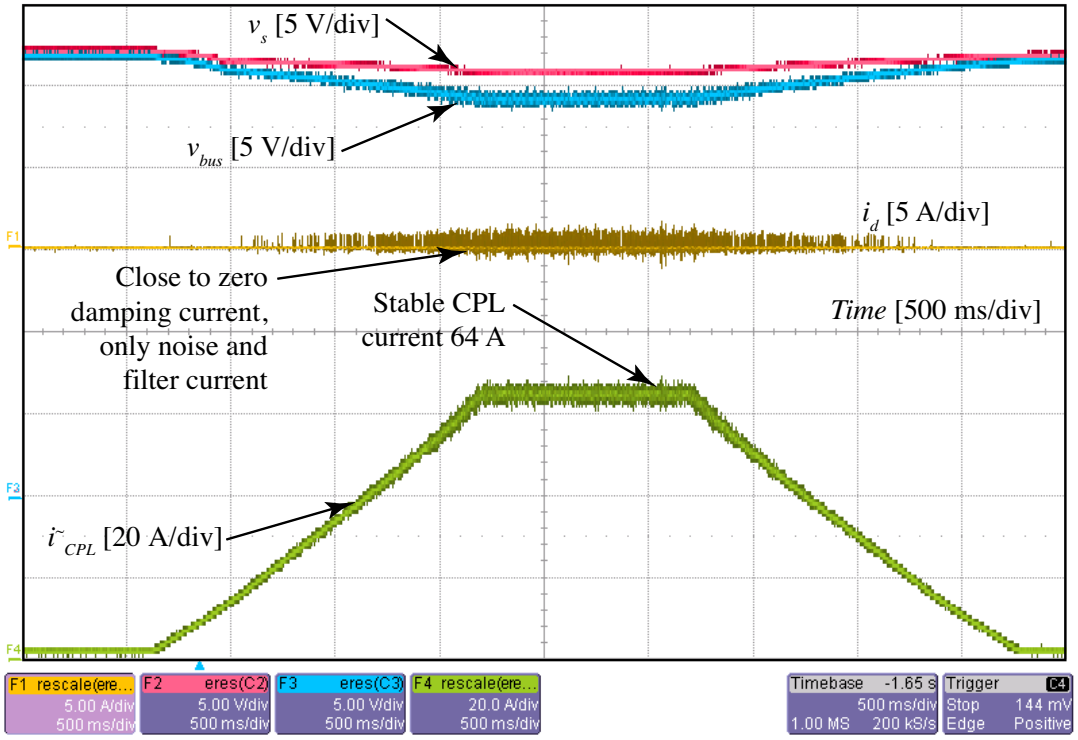
Figure 5.7 Stable system response to 1 kW CPL applied at the slew rate of 1 W/ms with the auxiliary circuit connected to the bus: (a) experimental results; and (b) simulations for the same conditions.



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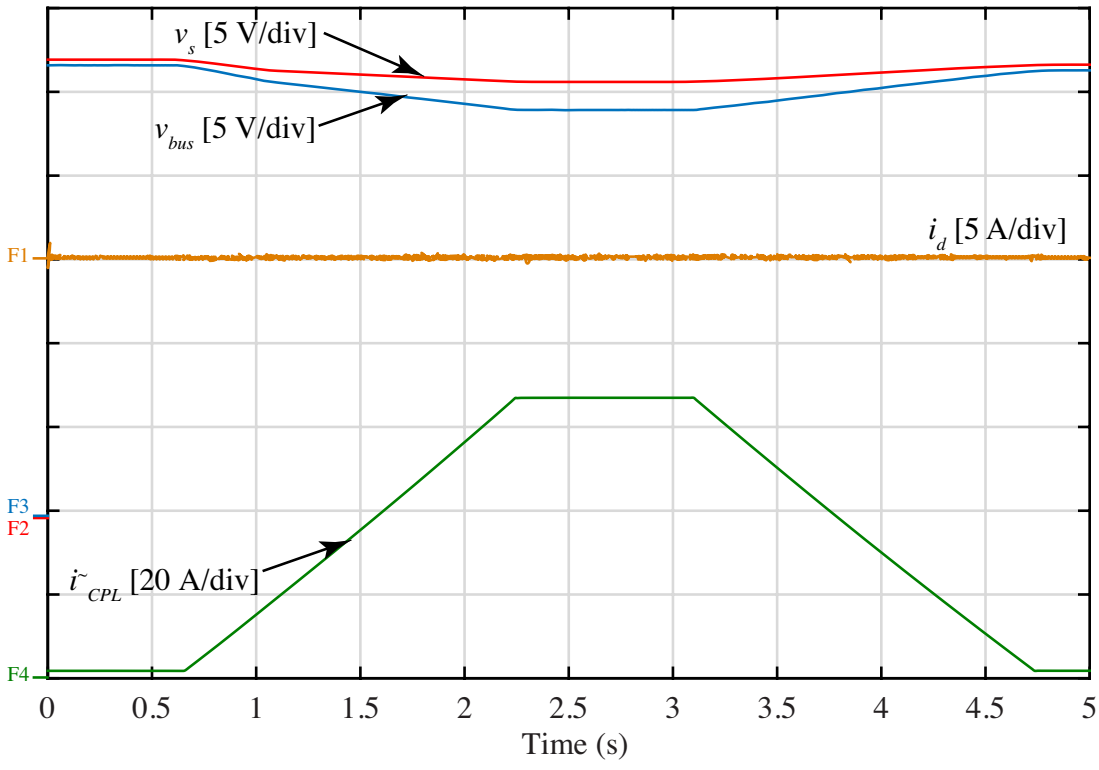

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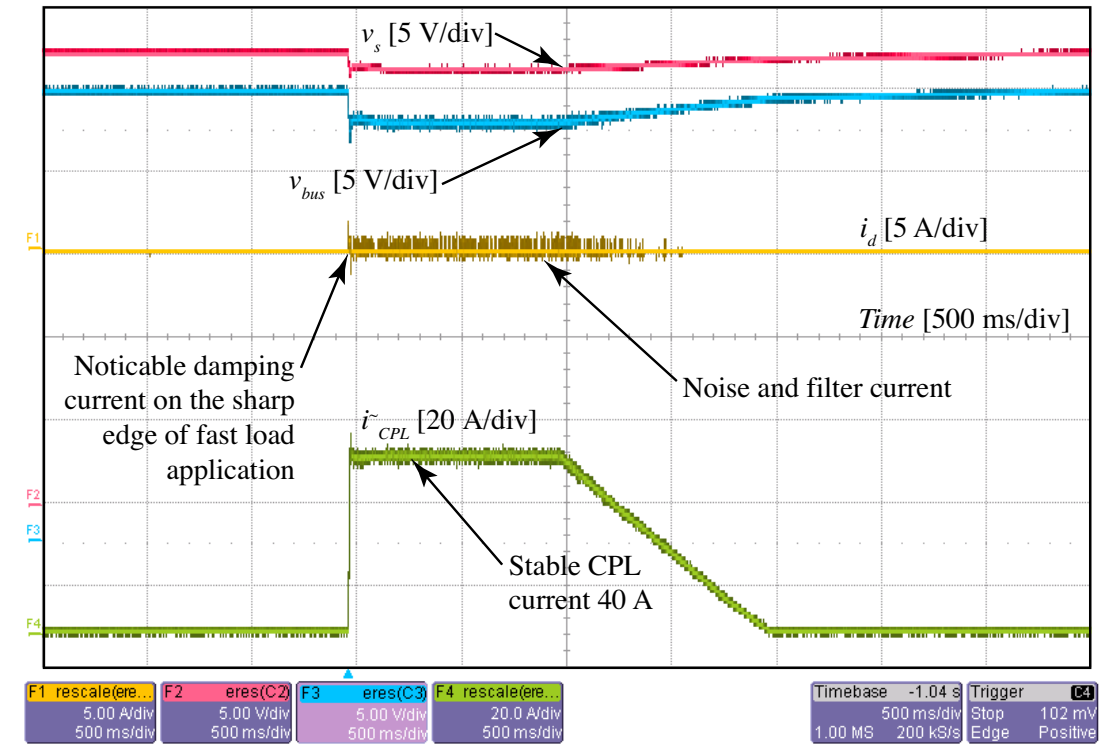
Figure 5.8 Stable system response to 1.6 kW CPL applied at the slew rate of 1 W/ms with the auxiliary circuit connected to the bus: (a) experimental results; and (b) simulations for the same conditions.



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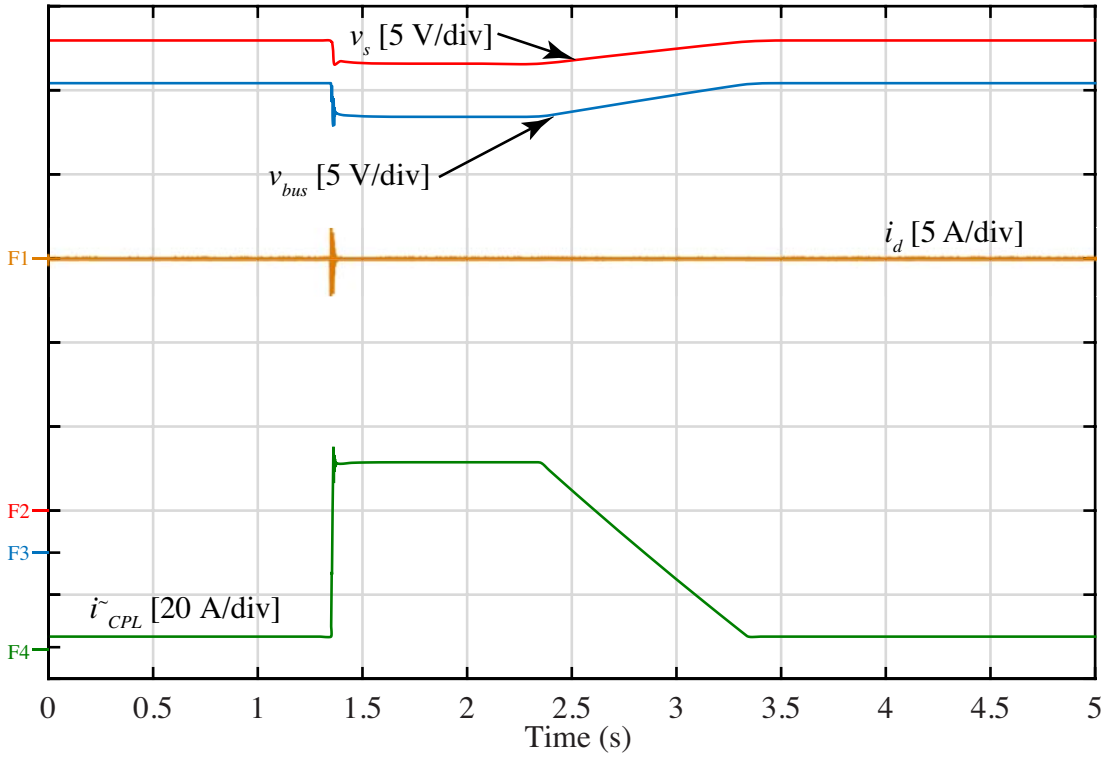
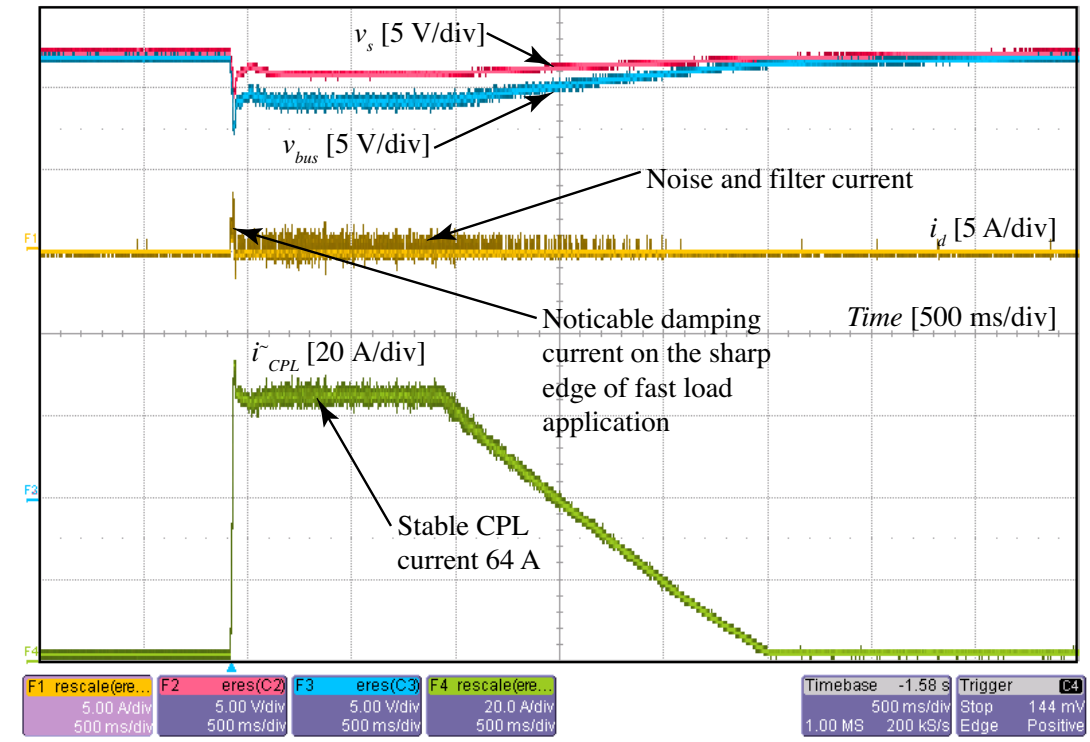
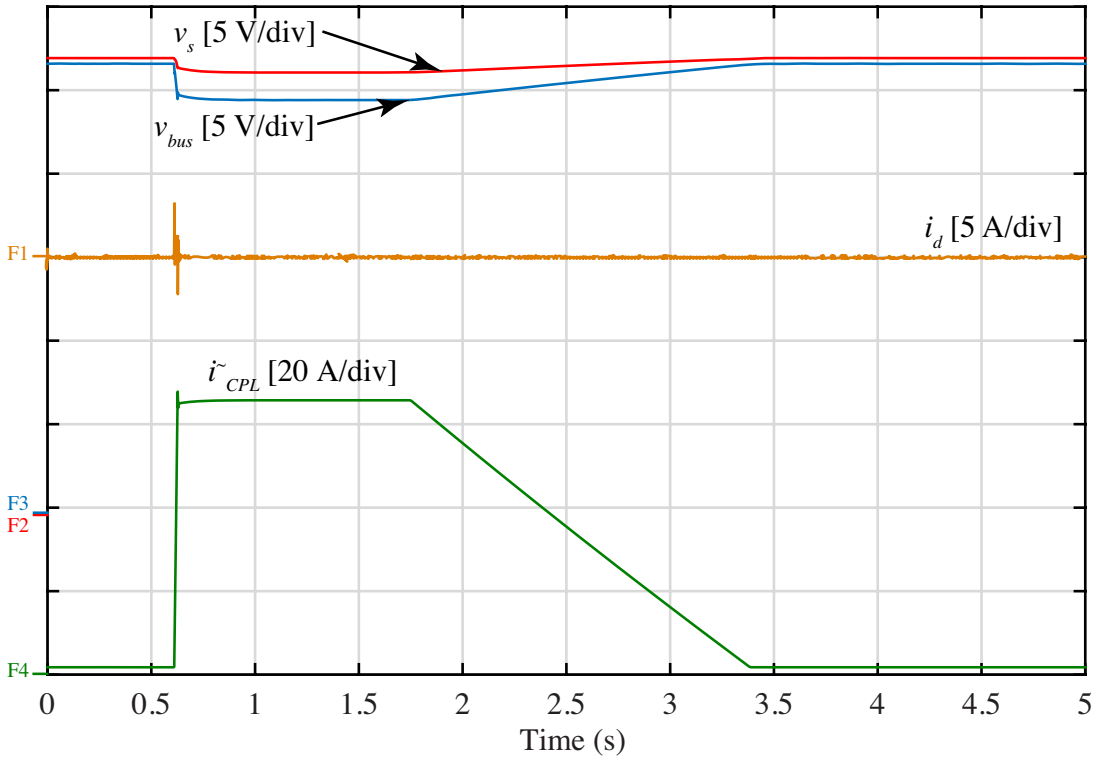


(b)

Figure 5.9 Stable system response to 1 kW CPL applied at the slew rate of 100 W/ms with the auxiliary circuit connected to the bus: (a) experimental results; and (b) simulations for the same conditions.

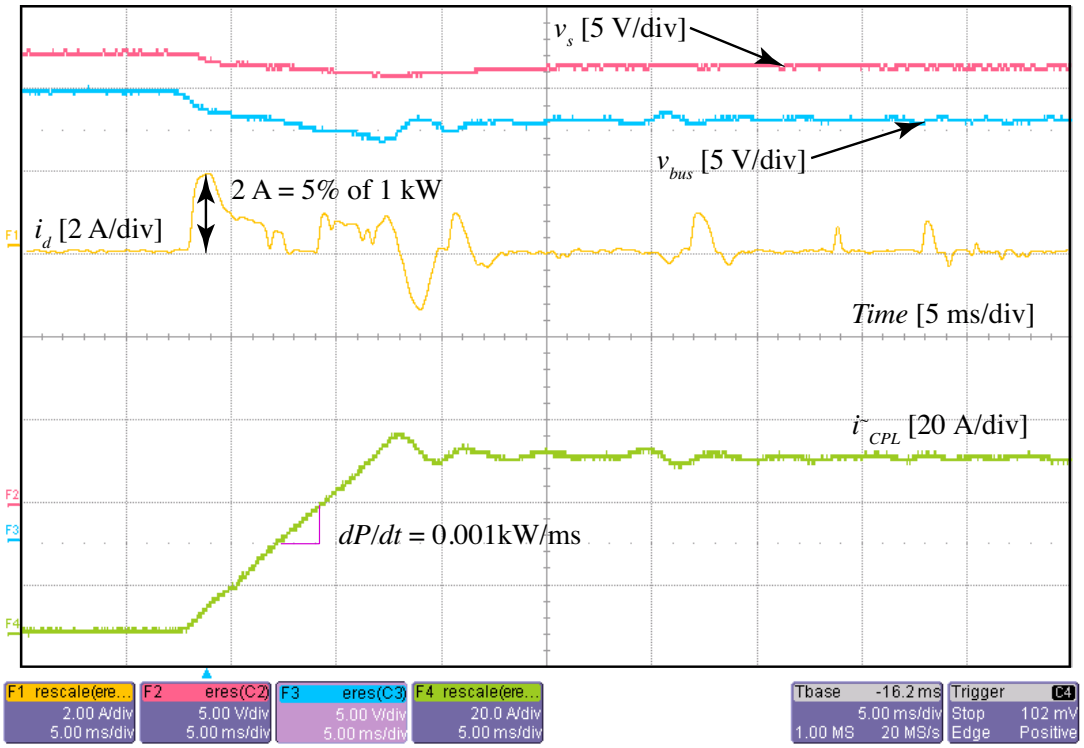


(a)

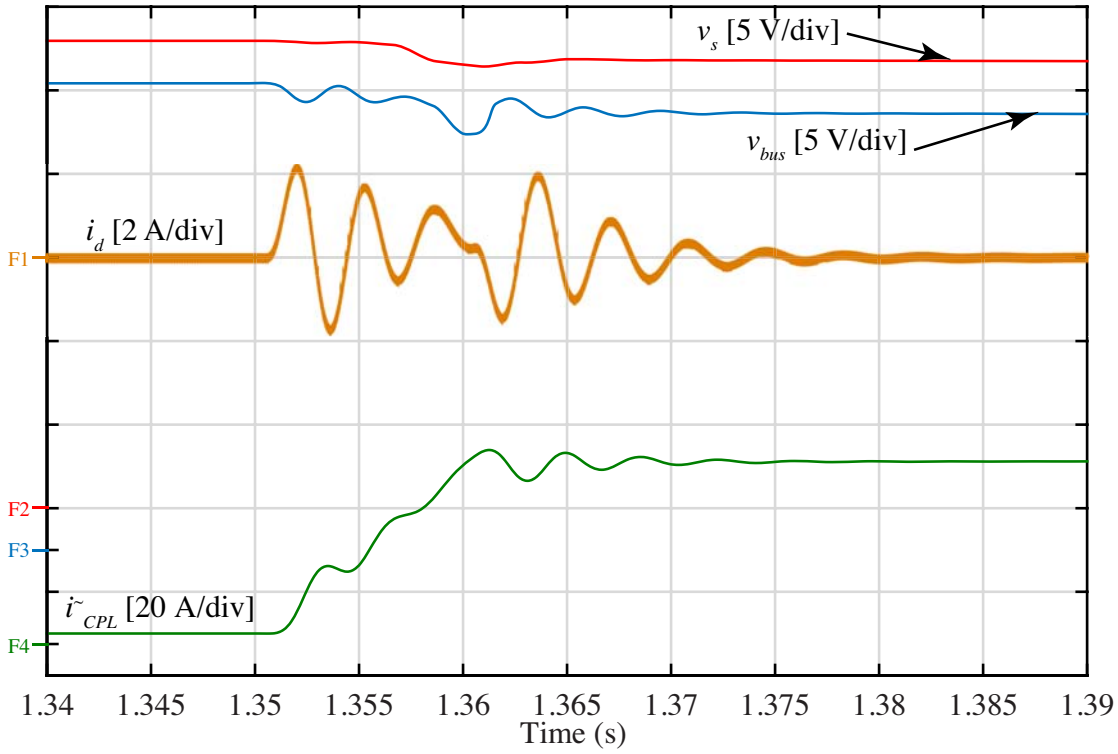


(b)

Figure 5.10 Stable system response to 1.6 kW CPL applied at the slew rate of 100 W/ms with the auxiliary circuit connected to the bus: (a) experimental results; and (b) simulations for the same conditions.

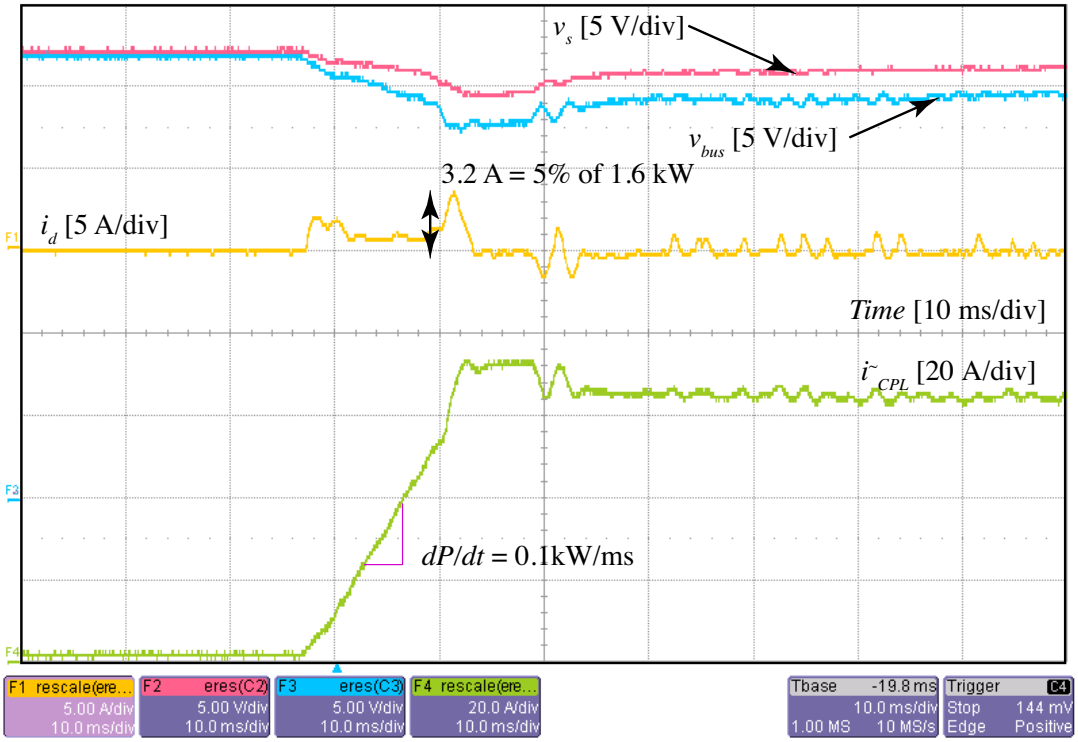


(a)

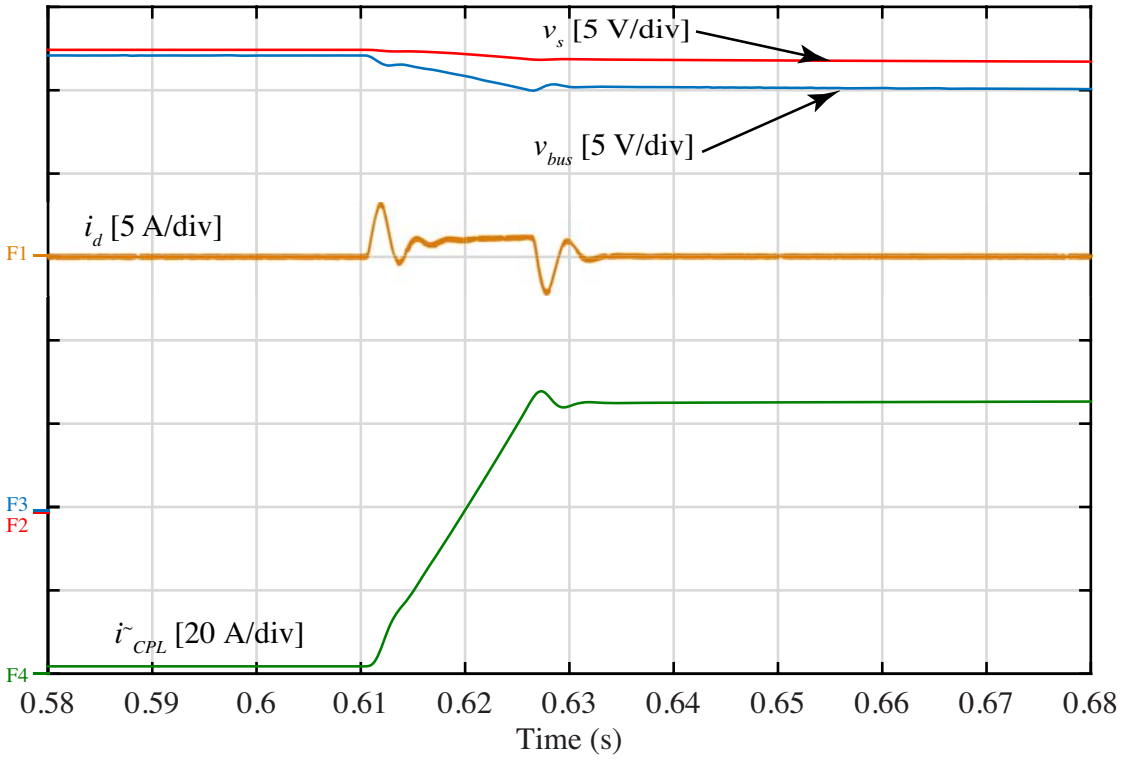


(b)

Figure 5.11 Details on stable system response (see Figure 5.9) to 1 kW CPL applied at the slew rate of 100 W/ms with the auxiliary circuit connected to the bus: (a) experimental results; and (b) simulations.



(a)



(b)

Figure 5.12 Details on stable system response (see Figure 5.10) to 1.6 kW CPL applied at the slew rate of 100 W/ms with the auxiliary circuit connected to the bus: (a) experimental results; and (b) simulations.

Chapter 6: Conclusions and Summary

6.1 Summary of Achieved Objectives and Contributions

It is envisioned that in the future the portion of CPLs in DC power distribution systems will be increasing. CPL-caused instability problems in DC systems due to the source-load impedance interactions at certain interfaces have been considered in this work. To address this problem, we have proposed an innovative active adaptive damping methodology, which is based on changing the state of unstable DC power distribution system by energy interchange with a neighboring strong power bus so that stability can be ensured with predefined margins. This approach is demonstrated using a bidirectional auxiliary converter circuit, which by acting as a controlled current source can change the impedances on the unstable bus. The overall methodology has been demonstrated on a practical reduced-scale DC system that has been installed by Alpha Technologies Ltd. in Kaiser building at UBC.

Due to increasing number of multi-voltage DC distribution systems with battery energy storage, and sources/loads that are possibly developed by different vendors with limited access to their internal controls, the proposed concept of adding a low-power auxiliary active damping circuit appears to be a viable solution of achieving stability in current and future DC grids. With respect to each of the objectives of this thesis, the contributions of my work may be summarized as follows:

Objective 1 – System analysis to identify practical parameters for stability margin assessment (addressed in Chapter 2). To study the source-load impedance interactions causing instability, the appropriate models of the system were required. A comprehensive source identification procedure was developed and applied to the commercial source for determining its power stage parameters, operating mode and the control algorithm. Both average and small-signal models were established with subsequent verification against the load application/rejection experiment. The general small-signal models for source and load were analyzed, and proposed to be used for the CPL instability studies. The origins of instability were discussed in details and conclusions were made on how to factor in multiple oscillatory modes in CPL impedance shaping techniques. For the purpose of designing active damping, a simplified criterion was suggested based on considering only the first (lower) frequency point at which the instability

may occur, as apposed to using the full Nyquist stability criterion for finding all possible points of instability and oscillatory modes (which would be difficult to realize). This approach may be more practical for DC systems with many components (sources and loads) some of which may have unknown parameters.

Objective 2 – Propose a new active damping methodology with flexible interfacing and programmable parameters (addressed in Chapter 3). An auxiliary circuit considered in this thesis required calculation of current injection for performing the active damping for stabilizing the system. Small-signal models from Chapter 2 were used to identify proper damping current injection for impedance-shaping techniques so that the desired performance goals were achieved. A simple (linear) fixed parameter damping approach was presented, and its parameters' selection has been derived utilizing hybrid Gain Margin Routh-Hurwitz criterion. In addition, in comparison with hybrid Gain Margin Routh-Hurwitz criterion, a much simpler analytical method of calculating the virtual *RC* values based on linearized adaptive controller was constructed. Then a non-linear active damping was presented, which essentially emulates a variable *RC* damping circuit, parameters of which depend on the system's operation point proving the adaptive behavior. The proposed adaptive damping control algorithm was demonstrated to be more efficient in time domain in terms of performance and suppressing the oscillatory modes in the system and the controller-required energy.

Objective 3 – Experimental verification using elements of the existing DC microgrid system (addressed in Chapters 4 and 5). Performance and functionality requirements for the auxiliary converter circuit were analyzed, and a bi-directional buck-boost topology with digital average-current control model (ACCM) was suggested. A novel commanded current extrapolation technique is proposed for removing the phase delay present in conventional current control mode. Experimental system including auxiliary converter circuit with its controls was developed and built. The simulations and experimental studies demonstrate the effectiveness of the proposed active damping methodology. It is shown that a very low damping current (and small energy) is required for stabilizing the system (in small-signal sense) in comparison with the system's size and power rating.

6.2 Future Work

This thesis focused on stability analysis and possible solutions for DC distribution systems using a single source/load interface. For the future research, it is envisioned that the proposed damping methodology can be used with more advanced bi-directional converters that have galvanic isolation, higher efficiency and bandwidth, as well as extended to multiple source-load interfaces. Further investigations are required on the topic of high-order damping approaches, which will be capable of more precise shaping of the system impedances. Specifically, the non-linear controller discussed in this thesis can be potentially extended from an equivalent first-order *RC* circuit to an n^{th}-order. Alternatively, more research is required on source-side damping techniques, so that its output impedance may be modified rather than the input impedance of the CPLs. The objective would be to modify the source in such a manner that its bandwidth increases while allowing the original CPL characteristics to be unchanged. In addition, extra advanced research can be done by combining small-signal stabilization proposed in this thesis in conjunction with load transient suppression methodologies [48], [49].

Finally, this methodology can be also potentially applied to AC systems with tightly regulated loads similar to CPLs using *dq*0 coordinate system transformation [50], harmonic linearization [51] techniques, and/or positive/negative impedance approaches.

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Appendices

Appendix A: Description and parameters of the source, load and auxiliary circuit for the experiment

Source	
Model	CXDF 48-24/2kW
Input voltage range	42-60 VDC
Output voltage range	24-27 VDC
Switching frequency	130 kHz
Parasitic transmission line inductance	80 μH (1 kW) and 52 μH (1.6 kW)
Constant power load	
Type	Synchronous buck
Input voltage range	20-30V
Output voltage range	5-30 V
Switching frequency	40 kHz
Main inductor	83 μH
Controller type	Duty cycle feed forward
Auxiliary circuit (power stage)	
Type	Synchronous buck-boost
Main inductor (L)	36 μH
Switching frequency	80 kHz
Output filter capacitor (C_f)	47 μF
Output filter inductor (L_f)	1.5 μH
Filter damping capacitor (C_b)	22 μF
Filter damping resistor (R_f)	0.6
Auxiliary circuit current (controller)	
Auxiliary circuit time constant τ	0.002
Auxiliary circuit amplification factor u	2
Equivalent resistor @ i_{CPL} = 40 A	0.33 Ohm
Equivalent capacitor @ i_{CPL} = 40 A	6000 μF
Equivalent resistor @ i_{CPL} = 64 A	0.2 Ohm
Equivalent capacitor @ i_{CPL} = 64 A	8100 μF

Appendix B: Experimental setup used to verify the proposed active damping method