EXPERIMENTS AND SIMULATIONS ON NEGATIVE/POSITIVE BIAS
TEMPERATURE INSTABILITY IN 28NM CMOS DEVICES

by

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B.A.Sc., The University of British Columbia, 2014

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF
THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF APPLIED SCIENCE

in

THE FACULTY OF GRADUATE AND POSTDOCTORAL STUDIES

(Electrical and Computer Engineering)

THE UNIVERSITY OF BRITISH COLUMBIA

(Vancouver)

October 2015

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Abstract

CMOS transistors come with a scaling potential, which brings along challenges such as process variation and NBTI/PBTI (Negative/Positive Bias Temperature Instability). My objectives during this project are to investigate effects of aging on CMOS devices as well as to show experimental results in order to model the effect of N/PBTI specifically targeting the 28nm technology node. The direct effect of transistor aging is a degradation of device threshold voltage, which can lead to performance degradation or malfunctions. Places such as server farms, data centers, and outer space-crafts, where device reliability for a long period is significant and accessibility is an issue, can benefit from an aging reversal process. In addition, as transistor channel lengths become smaller, they are more prone to a reduced lifetime. The exact causes of aging are not entirely known until this day and as a result, no real mechanism to reverse the process has been fully implemented on FPGAs or ASICs. I believe the true solution to these scalability challenges lay within the device structure and materials used in CMOS transistors, however, accelerated recovery at high temperatures can also help in reversing the effect of aging by a noticeable amount. I have been able to use this technique to reverse the effect of threshold voltage degradation in FPGAs.

In this thesis, I present experimental results on the effect of degradation and recovery on a commercial FPGA. I then use the experimental results to calculate degradation parameters of transistor aging in this technology node and propose experimental setups for a 28nm ASIC.
Preface

This thesis is the original intellectual product of the author Shahin Bayat. Some materials used in chapters 1, 2, 3, and 4 in this work are going to be submitted to a conference.

All of the work presented in this thesis have been done in the Systems-on-Chip (SoC) laboratory at the University of British Columbia, Vancouver Campus.
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<th>Description</th>
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<tbody>
<tr>
<td>CMOS</td>
<td>Complementary-Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>I/O</td>
<td>Input/Output</td>
</tr>
<tr>
<td>FDSOI</td>
<td>Fully Depleted Silicon on Insulator</td>
</tr>
<tr>
<td>NBTI</td>
<td>Negative Bias Temperature Instability</td>
</tr>
<tr>
<td>PBTI</td>
<td>Positive Bias Temperature Instability</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>MOSRA</td>
<td>MOSFET Reliability Analysis</td>
</tr>
<tr>
<td>LUT</td>
<td>Look Up Table</td>
</tr>
<tr>
<td>VHSIC</td>
<td>Very High Speed Integrated Circuit</td>
</tr>
<tr>
<td>VHDL</td>
<td>VHSIC Hardware Description Language</td>
</tr>
<tr>
<td>TDDDB</td>
<td>Time Dependent Dielectric Breakdown</td>
</tr>
</tbody>
</table>
Acknowledgements

I would like to thank and acknowledge the help and support of many friends, family, and supervisors at UBC who made some of the best years of my life even more memorable and pleasant. First, I would like to offer my enduring gratitude to my supervisors, Professor André Ivanov, and Dr. Cristian Grecu for their continuous support throughout my studies at UBC. I owe particular thanks to Dr. Cristian Grecu whose insightful comments and recommendations taught me to question more deeply and understand the subject matter better. I am very fortunate for having the opportunity to work with these great mentors.

I would also like to thank my friends and the friendly staff at the Systems-on-Chip (SoC) laboratory who always helped me with the questions I had and difficulties I went through in the past 2 years in particular my dear friend, Arash Sheikholeslam. In addition, my special gratitude goes to Dr. Roberto Rosales and Dr. Roozbeh Mehrabadi for their continuous support with CAD tools and technical problems.

Lastly, I want to thank my parents and my dear brother who supported me throughout every stage of my life and I owe all that I have achieved to them.
Dedication

I would like to dedicate this work to my parents and my brother whose support throughout all years of my life has motivated me to improve myself. I owe everything to you guys and if this didn’t workout I will find other ways of making you proud. 😊
Chapter 1: Introduction

Aging reduces the switching speed of transistors in circuits, which can result in circuit failure, and forces companies to set circuits work with clock speeds set with an overhead in mind in order for the circuit to be operational in its lifetime [1]. Aging in CMOS transistors changes the threshold voltage of the operating devices, which affects both AC, and DC behavior of a circuit. Shift in the threshold voltage also comes as a result of temperature, AC and DC bias stress. The effect of aging has become more severe as the operating voltage of CMOS transistors has become lower. This lowering of the operating voltages makes a shift in the threshold voltage cause a larger impact on circuit behavior. In the recent years the supply voltages have gone down from 5V to 1V as opposed to the threshold voltages going down only from 0.7V to 0.3V.

Negative/Positive Bias Temperature Instability is the most important aging mechanism in the literature today, which takes place due to the creation of interface traps and is highly dependent on the oxide electric field [2].

Circuit reliability issues such as BTI (Bias Temperature Instability) are becoming more and more relevant as CMOS technology nodes keep scaling. Negative Bias Temperature Instability (NBTI) has been considered a significant reliability concern for a long time. However, Positive Bias Temperature Instability (PBTI) has not been the dominant factor in device reliability until the introduction of High-K dielectric materials [3]. Silicon dioxide was commonly used as the material in the gate dielectric until the introduction of High-K dielectric for sub-45nm CMOS technology nodes. Materials such as hafnium silicate, zirconium silicate, hafnium dioxide, and zirconium dioxide which are considered the popular High-K dielectric choices have shown significant charge trapping compared to the conventional silicon dioxide.
The effect of High-K dielectric has been similar for NBTI in PMOS devices, but the effect of PBTI is now more severe as opposed to the past when PBTI did not contribute much to aging [4] [5]. Because of the small contribution of PBTI before the introduction of High-K dielectric, most of the previous work in modeling the effect of aging has ignored this phenomenon by characterizing aging using ring oscillators consisting of inverter stages only [6] [7]. In the previous works, ring oscillators consisting of an odd number of inverters would be subject to stress under temperature and bias voltage and frequency measurements before and after stress would yield aging models. However, the results are a mix of NBTI and PBTI and this was acceptable in the past with previous technology nodes above 45nm because PBTI did not contribute much to circuit reliability [8]. Presently, in order to fully characterize aging in a technology node each of NBTI and PBTI need to be measured separately and require dedicated test structures.

During the lithography process of CMOS devices, an annealing step follows oxidation of the gate in order to passivate the dangling Si bonds at the surface of Silicon. The resulting Si-H bonds are weak and break easily throughout device operation and under stress causing H atoms to diffuse into the gate oxide and leaving Si dangling bonds at the surface again also known as interface traps [9] [10]. Figure 1.1 shows that the electric current passing through the channel consisting of electric charges which can get stuck in these traps. Accumulation of charges at the channel/oxide interface leads to the channel being shielded from the gate terminal, and in turn requires a higher voltage to achieve inversion. This degradation in device operation is known as NBTI/PBTI because PMOS and NMOS devices operate with a negative or positive voltages respectively and the combination of the bias voltage stress and high temperatures shifts the
threshold voltages up. In this theoretical model, which is called reaction-diffusion, reaction stands for the dissociation of hydrogen from the dielectric and channel and diffusion stands for its diffusion into the oxide [2].

![Figure 1.1 Reaction-diffusion mechanism in NBTI](image)

Removing the stress causes the device to enter into a recovery phase in which the threshold voltage shifts close to its original value, but not fully. N/PBTI have temporary and permanent effects [11] and their temporary effects are removed when stress from transistors is removed, but long term stress causes permanent shifts in threshold voltage of device resulting in degradation in frequency of circuits. In this thesis, I will discuss methods in order to reverse the permanent effects of NBTI in order to recover the device back to its original parameters.

Aging in transistors has different mechanisms namely destructive and non-destructive mechanisms. Non-destructive aging refers to changes in device characteristics that do not
necessarily cause a breakdown; destructive aging refers to a failure caused by an unrecoverable breakdown of the device such as Time Dependent Dielectric Breakdown (TDBB). BTI has permanent and temporary effects which are non-destructive [12].

1.1 Motivations and Goals

How does N/PBTI effect the 28nm CMOS technology in FPGAs and ASICs? The goal of this work is to find the relationship between frequency degradation and stress time explained by the theory of reaction-diffusion and charge trapping model in N/PBTI. I am interested in finding how much N/PBTI each contribute separately to device degradation in the 28nm technology node. I will look at this relationship between frequency and stress for a variety of oscillators in the Artix 7 series FPGA chip as well as simulation results using HSPICE and MOSRA. Another goal of this research is to find out if we can recover frequency and device characteristics using only elevated temperatures as claimed in [13] which claims to fully recover device parameters caused by NBTI such as threshold voltage by fully baking the device at temperatures higher than 325 °C. Based on the experimental data collected from the Artix 7 series FPGA, I will extract parameters to model degradation which can help in order to estimate device degradation and threshold voltage shift over any period of time as a result of N/PBTI. Finally, I have designed a chip implementing the test setups to measure the effects of N/PBTI in the 28nm FDSOI technology node and have a test plan ready to test the chip when it is back from fabrication.
1.2 Contributions

1.2.1 Stress Variation Measurements in FPGAs

Experiments using ring oscillators have been carried out on the Xilinx Artix 7 FPGA chip, which uses a 28nm technology in order to test the effect of NBTI. The FPGA board is stressed and frequencies of the oscillators are recorded before and after stress with high temperature. The change in frequency which translates into change in $V_{TH}$ (Threshold voltage) is of importance to model aging for this technology node. This part of the thesis will help to realize the effect of aging and its severity on FPGAs as well as to provide a proof-of-concept for moving forward with an ASIC design to test/monitor device degradation and recovery.

1.2.2 Effects of NBTI and PBTI Using Simulations and ASICs

Circuits are designed on a 28nm FDSOI (Fully Depleted Silicon on Insulator) chip to model the effect of NBTI/PBTI in this technology node. Single transistors, dedicated oscillators consisting of NAND/NOR gates are implemented as well as an on chip temperature sensor and a comparator in order to effectively monitor and control the on-chip temperature. Also, simulation results are presented in this section as well as a test plan containing the procedure to test the chip. Data extracted from the experiments in this section will help designers to design their circuits with sufficient overhead in order to minimize the long term effects of aging such as shift in frequency and subsequently, threshold voltage.

1.2.3 Result Analysis

In this section, I have compared the results of MOSRA simulations in HSPICE for N/PBTI at elevated temperatures to show the effect of PBTI in the 28nm High-k metal
technology. Experimental results for degradation and recovery extracted from the Artix 7 series FPGA chip are then shown for 3 oscillators to show that the results obtained are comprehensive across a number of oscillators. Lastly, I will show the relationship between frequency and threshold voltage shift and extract degradation parameters based on models proposed in [14] and [15] and estimate the lifetime of the Artix 7 series FPGA chip for 10 years.

1.3 Thesis Organization

The rest of the thesis is organized as follows. Chapter 2 presents aging and BTI degradation and recovery as it manifests itself in the Artix 7 series FPGA chip by showing experimental results for a number of oscillators varying from 21-41 stages. Aging simulations were performed and reported in Chapter 3 for NAND, NOR and inverter chain oscillators. Next, the ASIC and the structures used for testing are described in detail with a test plan in order to test the chip. Chapter 4 goes over the results by relating frequency shift to threshold voltage shift and finally by extracting parameters required in order to model degradation for transistors in the 28nm technology node. Finally, Chapter 5 presents conclusions and future work and discusses the significance of this work and the experimental results that are extracted.
Chapter 2: Stress Variation Measurements in FPGAs

I started working with the Nexys 4 FPGA in order to gather experimental results to prove that degradation and recovery are in fact measurable to serve as a proof-of-concept before the ASIC was designed. The use of an FPGA in this work is to prove the concept of degradation and recovery in the 28nm technology node before moving on to designing an ASIC. The FPGA board I am using is the Nexys 4 based on the Artix-7 FPGA chip from Xilinx. Results provided in this section are going to provide a proof-of-concept and motivation for this research. FPGAs are a cost effective way for us to prove the concept of degradation and recovery before designing the more expensive ASIC.

2.1 Design and Implementation

The circuit used in this section consists of a 21-stage ring oscillator followed by a clock divider as shown in figure 2.1. The ring oscillator provides a frequency in the 50-51 MHz range and there was no equipment available at the SoC lab to accurately measure this frequency. The only frequency counter available is the HP 34401A multimeter, which can measure up to 300 KHz of frequency. Therefore, using a frequency divider and a scaling factor of 250 I dropped the frequency to 200 KHz to be in the measurable frequency range. This will ensure that the frequency I read from the oscillator is as accurate as possible since the shift in frequency is not huge.

Two 21-stage ring oscillators are implemented on the Artix 7 series FPGA chip as shown in figure 2.1 using lookup tables (LUTs) and are enabled using the switches on the board. The stress test consists of stressing the chip at 110 °C using a temperature controlled device that I
have designed. The board is taken off stress every 6 hours for measurements. One of the two oscillators is always turned off throughout the stress phase using a switch, which enables/disables the oscillator to act as a reference oscillator. The second oscillator is always on during the stress phase. Ring oscillators consist of an odd number of inverters or NAND/NOR gates, which have to be implemented using lookup tables (LUTs) in VHDL. Using hard macro LUTs instead of defining logic gates in VHDL is necessary in order to implement ring oscillators because the FPGA synthesizer reduces any odd number of inverters/NAND/NOR gates in a chain to a single gate in order to maintain design efficiency. The reasons why NAND/NOR ring oscillators are appropriate for studying the effects of N/PBTI can be found in Chapter 3.

![Ring oscillator structure](image)

**Figure 2.1** Ring oscillator structure used in Artix 7 series FPGA chip. The clock divider in the end is put to ensure the frequency is low enough for the frequency counter to measure it.

### 2.2 Experiment Setup

In order to stress the chip, I had to design my own temperature control system with a resistive heating element to heat up the chip and not the entire FPGA. The circuit shown on Figure 2.2 consists of a resistive heating element in conjunction with a temperature sensor with a 1 °C resolution and a transformer to convert 110V to 24V to be used by the temperature sensor since the sensor is rated to work with 10-30V.
Figure 2.2 Temperature control system designed in order to stress and recover the FPGA/ASIC chip.

A diagram of the control system used to explain the operation of this system shown on Figure 2.2 is illustrated below in Figure 2.3. This circuit allows the user to set any temperature from the range of -50-130 °C and will keep the resistive heating element at the set temperature.

Figure 2.3 Feedback control loop of the temperature control system.
2.3 Measurements

Alternating Current (AC) stress is a form of current in which the flow of electric charge periodically reverses direction. Stress tests under high temperature and AC voltage for a number of ring oscillators have been carried out on the Artix 7 FPGA chip and the results are shown in in this Chapter. The FPGA board was put under stress using my temperature controlled system shown in Figure 2.2 for 24 hours and the frequency of the ring oscillator was measured every 6 hours. I have run the stress tests on a number of ring oscillators such as inverter, NAND, and NOR chains with different number of stages in order to have comprehensive results that are based on a number of oscillators in order to extract accurate degradation parameter models.
2.3.1 Degradation

The first experiment here has been done by stressing a pair of inverter based oscillators at 110 °C and one being off (reference oscillator) throughout the experiment just to showcase the significant effect of bias voltage aside from temperature on N/PBTI. 110°C is chosen as the main temperature of interest throughout this work because the Artix 7 series FPGA supports up to 80 °C and after 110 °C there is the possibility of thermal breakdown of the dielectric [16] and in this FPGA chip every 10 °C rise in temperature above 80 °C doubles the failure rate [17]. Figure 2.4 shows the results of frequency shift for 24 hours with data points collected every 6 hours.

![Inverter Ring Oscillator - Frequency Degradation over 24 hours with 24 hours of normal Recovery Vs. Time (Hours)](image)

**Figure 2.5** Inverter ring oscillator illustrating the effect of stress at high temperatures over 24 hours on an operational and a non-operational ring oscillator with reference to frequency shift in percentage.

R² in Figure 2.5 is the r-squared value for a linear trendline, meaning the closer it is to 1, the more linear the line is and \( Y = 0.0902x + 0.4096 \) is the equation of the linear line passing...
through the curve. This equation is repeated for most illustrations in this work and is extracted from the data points collected.

As illustrated in Table 2.1, there is around 1.7 % difference between the frequency shift of the reference inverter oscillator which was turned off using an enabler gate and the oscillator which was on and was also under bias stress and supply voltage. This shows that the effect of the bias voltage on transistors is significant at high temperature stress of 110 °C.

<table>
<thead>
<tr>
<th>Time (hours)</th>
<th>Frequency Shift (%) Reference oscillator at 110 °C</th>
<th>Frequency Shift (%) Gate stressed inverter oscillator at 110 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0.315</td>
<td>1.205</td>
</tr>
<tr>
<td>12</td>
<td>0.417</td>
<td>1.88</td>
</tr>
<tr>
<td>18</td>
<td>0.492</td>
<td>2.136</td>
</tr>
<tr>
<td>24</td>
<td>0.542</td>
<td>2.242</td>
</tr>
</tbody>
</table>

Table 2.1 Measurement results for frequency shift of a reference oscillator vs. gate stressed oscillator at 110 °C.

The next experiment consisted of aging the chip under two temperatures of 110 °C and 80 °C to show the effect of temperature on frequency shift as a result of threshold voltage shift and the results are shown in Figure 2.6. The comparison of the two temperatures is of interest because 80 °C is the maximum temperature advertised for the Artix 7 series FPGA chips and 110
°C is said to increase the failure rate. In the next section of the thesis, I will present results on normal and accelerated recovery with the goal of reversing the frequency shift caused as a result of temperature and bias voltage stress.

Figure 2.6 Inverter ring oscillator frequency shift with gate stress compared at different temperature stresses over 24 hours.

<table>
<thead>
<tr>
<th>Time (Hours)</th>
<th>Frequency Shift (%)</th>
<th>Frequency Shift (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Gate Stressed Inverter Oscillator at 80 °C</td>
<td>Gate Stressed Inverter Oscillator at 110 °C</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0.762</td>
<td>1.205</td>
</tr>
<tr>
<td>12</td>
<td>1.381</td>
<td>1.881</td>
</tr>
</tbody>
</table>

\[
y = 0.0902x + 0.4096 \\
R^2 = 0.8532
\]

\[
y = 0.082x + 0.1864 \\
R^2 = 0.951
\]
### Table 2.2 Measurement results of 2 gate stressed oscillators at 2 different temperatures to showcase the effect of temperature over 24 hours on frequency shift.

<table>
<thead>
<tr>
<th>Time (Hours)</th>
<th>Frequency Shift (%)</th>
<th>Frequency Shift (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Gate Stressed Inverter Oscillator at 80 °C</td>
<td>Gate Stressed Inverter Oscillator at 110 °C</td>
</tr>
<tr>
<td>18</td>
<td>1.736</td>
<td>2.136</td>
</tr>
<tr>
<td>24</td>
<td>1.972</td>
<td>2.242</td>
</tr>
</tbody>
</table>

2.3.2 Recovery

Normal recovery of device characteristics such as threshold voltage and frequency happens when the circuit is off stress at room temperature and when the FPGA chip is turned off [14]. I expected some level recovery just at room temperature based on [18] for the temporary effects of N/PBTI to be recovered, hence conducted a series of stress and recovery tests.

Accelerated recovery is to increase the rate of this process by increasing temperature and can be used to reverse the permanent effects of N/PBTI. The idea to use high temperatures to recover aging degradation has been taken from [14] and [13]. In the next section, I will provide results for degradation and recovery under different stress conditions for a variety of ring oscillators consisting of inverter/NAND/NOR gates and inverter ring oscillators varying from 21-41 stages.

2.3.2.1 Inverter Based Ring Oscillator

In this section two experiments have been carried out to show the effect of normal vs. accelerated recovery for the Artix 7 Series FPGA chip. Accelerated recovery consists of using my temperature control system to heat up the chip to 110 °C while having the device turned off.
Experiment one consists of a series of 21-stage ring oscillators in the Artix 7 series FPGA chip being stressed using my temperature control system at 110°C for 24 hours. Next, I have taken the chip off stress for 24 hours and have collected data points every 6 hours to measure the amount of frequency recovered at room temperature. Figure 2.7 shows the frequency degradation shift under accelerated degradation at 110 °C and recovery at 25°C for 24 hours.

![Inverter Ring Oscillator - Frequency Degradation over 24 hours with 24 hours of normal Recovery Vs. Time (Hours)](image)

*Figure 2.7 Inverter ring oscillator frequency degradation with 110 °C stress over 24 hours with normal recovery at 25 °C room temperature.*

Table 2.3 provides full results on this experiment and the normal recovery with a 0.54 % frequency recovery over 24 hours.
<table>
<thead>
<tr>
<th>Time (Hours)</th>
<th>Frequency Shift (%)</th>
<th>Time (Hours)</th>
<th>Frequency Shift (%)</th>
<th>Time (Hours)</th>
<th>Recovered Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Pre-Recovery</td>
<td></td>
<td>Post-Recovery</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>24</td>
<td>2.242</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>1.205</td>
<td>30</td>
<td>1.916</td>
<td>6</td>
<td>-0.712</td>
</tr>
<tr>
<td>12</td>
<td>1.881</td>
<td>36</td>
<td>1.793</td>
<td>12</td>
<td>0.088</td>
</tr>
<tr>
<td>18</td>
<td>2.136</td>
<td>42</td>
<td>1.717</td>
<td>18</td>
<td>0.419</td>
</tr>
<tr>
<td>24</td>
<td>2.242</td>
<td>48</td>
<td>1.695</td>
<td>24</td>
<td>0.547</td>
</tr>
</tbody>
</table>

Table 2.3 Measurement results over 24 hours comparing the shift in frequency for accelerated degradation and normal recovery at room temperature.

The second experiment in this Section was setup using a 21-stage ring oscillator on another Artix 7 FPGA chip. The experiment again consists of stressing the chip under 110 °C temperature for 24 hours, but this time the accelerated recovery stage consists of heating up the chip up to 110 °C using the temperature control system while the chip is turned off. Figure 2.8 shows results for accelerated recovery and degradation using an illustration of frequency shift vs. time in hours.
Figure 2.8 Inverter ring oscillator frequency shift for accelerated degradation and recovery at 110 °C over 24 hours with gate stress.

Table 2.4 Measurement results over 24 hours comparing the shift in frequency for accelerated degradation and recovery at 110 °C.

<table>
<thead>
<tr>
<th>Time (Hours)</th>
<th>Frequency Shift (%) Pre-Recovery</th>
<th>Time (Hours)</th>
<th>Frequency Shift (%) Post-Recovery</th>
<th>Time (Hours)</th>
<th>Recovered Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>24</td>
<td>2.715</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>1.495</td>
<td>30</td>
<td>2.011</td>
<td>6</td>
<td>-0.516</td>
</tr>
<tr>
<td>12</td>
<td>2.132</td>
<td>36</td>
<td>1.724</td>
<td>12</td>
<td>0.409</td>
</tr>
<tr>
<td>18</td>
<td>2.591</td>
<td>42</td>
<td>1.592</td>
<td>18</td>
<td>0.1</td>
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<tr>
<td>24</td>
<td>2.715</td>
<td>48</td>
<td>1.403</td>
<td>24</td>
<td>1.311</td>
</tr>
</tbody>
</table>
Based on the results shown in Table 2.4, accelerated recovery at 110 °C has restored around 1.3% of frequency in 24 hours which is more than the normal recovery at room temperature and shows that accelerated recovery using high temperatures can help to reverse some of the permanent effects of aging which would not be recovered otherwise under regular conditions.

Next, Figure 2.9 compares the difference between accelerated and normal recovery (room temperature) every 6 hours and shows that accelerated recovery has a trend that keeps increasing over time more than normal recovery at room temperature. Recovered frequency is the difference between pre-recovery and post-recovery frequency. For instance in Table 2.4, Frequency recovered = pre-recovery frequency – post recovery frequency, which yields -0.516 % at the 6 hour recovery point.

![Inverter Ring Oscillator - Normal Vs. Accelerated Recovery in Frequency Shift (%)](image)

**Figure 2.9** Comparing the results of normal vs. accelerated recovery at 25 °C and 110 °C over 24 hours.

Frequency shift over 24 hours has been greater than the gain in 6 hours resulting in a negative value for the first 6 hours of recovery.
2.3.2.2 NOR Based Ring Oscillator

The next set of experiments were run on the same FPGA chip on a NOR oscillator structure in order to have comprehensive results from common oscillator structures used in electrical circuits. There is no differences between the oscillators used in terms of the number of devices used in the LUT as inverter/NAND/NOR ring oscillators are all implemented using the 4-1 LUT, but this will ensure that my degradation data is comprehensive in order to extract and accurate degradation parameters. Figure 2.10 shows the frequency degradation of a NOR oscillator at 110 °C with recovery at 25 °C.

Figure 2.10 NOR ring oscillator frequency degradation with 110 °C stress over 24 hours with normal recovery at 25 °C room temperature.

The detailed results are shown in Table 2.5 for comparison and after 24 hours there is 0.62 % frequency recovery at just 25 °C room temperature.
Chapter 2: Stress Variation Measurements in FPGAs

<table>
<thead>
<tr>
<th>Time (Hours)</th>
<th>Frequency Shift (%) Pre-Recovery</th>
<th>Time (Hours)</th>
<th>Frequency Shift (%) Post-Recovery</th>
<th>Time (Hours)</th>
<th>Recovered Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>24</td>
<td>2.456</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>1.413</td>
<td>30</td>
<td>2.229</td>
<td>6</td>
<td>-0.815</td>
</tr>
<tr>
<td>12</td>
<td>2.012</td>
<td>36</td>
<td>2.013</td>
<td>12</td>
<td>-0.002</td>
</tr>
<tr>
<td>18</td>
<td>2.312</td>
<td>42</td>
<td>1.914</td>
<td>18</td>
<td>0.398</td>
</tr>
<tr>
<td>24</td>
<td>2.456</td>
<td>48</td>
<td>1.832</td>
<td>24</td>
<td>0.624</td>
</tr>
</tbody>
</table>

Table 2.5 Measurement results over 24 hours comparing the shift in frequency for accelerated degradation and normal recovery of a NOR ring oscillator at room temperature.

Accelerated recovery at 110 °C again resulted in similar results as the inverter chain oscillator with around 1.3 % recovery over a 24-hour period and results are shown in Figure 2.11.
Figure 2.11 NOR ring oscillator frequency shift for accelerated degradation and recovery at 110 °C over 24 hours with gate stress.

Table 2.6 provides results for accelerated degradation and recovery at 110 °C and shows a frequency recovery of 1.31% after 24 hours.
<table>
<thead>
<tr>
<th>Time (Hours)</th>
<th>Frequency Shift (%) Pre-Recovery</th>
<th>Time (Hours)</th>
<th>Frequency Shift (%) Post-Recovery</th>
<th>Time (Hours)</th>
<th>Recovered Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>24</td>
<td>2.71</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>1.562</td>
<td>30</td>
<td>2.122</td>
<td>6</td>
<td>-0.561</td>
</tr>
<tr>
<td>12</td>
<td>2.11</td>
<td>36</td>
<td>1.814</td>
<td>12</td>
<td>0.288</td>
</tr>
<tr>
<td>18</td>
<td>2.42</td>
<td>42</td>
<td>1.662</td>
<td>18</td>
<td>0.761</td>
</tr>
<tr>
<td>24</td>
<td>2.71</td>
<td>48</td>
<td>1.391</td>
<td>24</td>
<td>1.311</td>
</tr>
</tbody>
</table>

Table 2.6 Measurement results over 24 hours comparing the shift in frequency for accelerated degradation and recovery of a NOR ring oscillator at 110 °C.

Figure 2.12 illustrates the difference between normal recovery at 25 °C and accelerated recovery at 110 °C which shows recovery at 110 °C increases recovery by almost twice as much as room temperature recovery and this matches the data from the previous experiment on the inverter ring oscillator which is expected.
Figure 2.12 Comparing the results of normal vs. accelerated recovery at 25 °C and 110 °C for a NOR ring oscillator over 24 hours. Frequency shift over 24 hours has been greater than the gain in 6 hours resulting in a negative value for the first 6 hours of recovery.

2.3.2.3 NAND Based Ring Oscillator

The last set of experiments were run on a NAND chain oscillator and the results are shown below in Figure 2.13.
Figure 2.13 NAND ring oscillator frequency degradation with 110 °C stress over 24 hours with normal recovery at 25 °C room temperature.

Frequency shift over the 48 hours is reported below in Table 2.7. Results show that there seems to be some more degradation as well as recovery than inverter and NOR chain oscillators. The difference is minimal, however, and could be explained by the placement of the ring oscillators on the FPGA chip and that the location of every oscillator varies by a bit.
<table>
<thead>
<tr>
<th>Time (Hours)</th>
<th>Frequency Shift (%) Pre-Recovery</th>
<th>Time (Hours)</th>
<th>Frequency Shift (%) Post-Recovery</th>
<th>Time (Hours)</th>
<th>Recovered Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>24</td>
<td>2.77</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>1.632</td>
<td>30</td>
<td>2.433</td>
<td>6</td>
<td>-0.802</td>
</tr>
<tr>
<td>12</td>
<td>2.281</td>
<td>36</td>
<td>2.203</td>
<td>12</td>
<td>0.078</td>
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<tr>
<td>18</td>
<td>2.612</td>
<td>42</td>
<td>2.12</td>
<td>18</td>
<td>0.494</td>
</tr>
<tr>
<td>24</td>
<td>2.77</td>
<td>48</td>
<td>2.006</td>
<td>24</td>
<td>0.765</td>
</tr>
</tbody>
</table>

Table 2.7 Measurement results over 24 hours comparing the shift in frequency for accelerated degradation and normal recovery of a NAND ring oscillator at room temperature.

Accelerated recovery has also result in an extra recovery of around 0.7% over 24 hours in comparison to room temperature recovery as shown from data in Figure 2.14.
Figure 2.14 NAND ring oscillator frequency shift for accelerated degradation and recovery at 110 °C over 24 hours with gate stress.

<table>
<thead>
<tr>
<th>Time (Hours)</th>
<th>Frequency Shift (%)</th>
<th>Time (Hours)</th>
<th>Frequency Shift (%)</th>
<th>Time (Hours)</th>
<th>Recovered Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Pre-Recovery</td>
<td></td>
<td>Post-Recovery</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>24</td>
<td>2.915</td>
<td>0</td>
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</tr>
<tr>
<td>6</td>
<td>1.691</td>
<td>30</td>
<td>2.232</td>
<td>6</td>
<td>-0.541</td>
</tr>
<tr>
<td>12</td>
<td>2.294</td>
<td>36</td>
<td>1.902</td>
<td>12</td>
<td>0.393</td>
</tr>
<tr>
<td>18</td>
<td>2.666</td>
<td>42</td>
<td>1.821</td>
<td>18</td>
<td>0.846</td>
</tr>
<tr>
<td>24</td>
<td>2.955</td>
<td>48</td>
<td>1.522</td>
<td>24</td>
<td>1.433</td>
</tr>
</tbody>
</table>

Table 2.8 Measurement results over 24 hours comparing the shift in frequency for accelerated degradation and recovery of a NAND ring oscillator at 110 °C.
The last comparison between normal 25 °C recovery and accelerated recovery at 110 °C for the NAND ring oscillator shows that accelerated recovery at 110 °C results in twice as much frequency recovery over 24 hours than what is achievable at room temperature. Recovery in the three experiments performed here on inverter, NOR, and NAND oscillators has resulted in 1.4% recovery over 24 hours with 110 °C accelerated recovery and around 0.7% at room temperature recovery.

![NAND Ring Oscillator - Normal Vs. Accelerated Recovery in Frequency Shift (% Vs. Time (Hours)](image)

**Figure 2.15** Comparing the results of normal vs. accelerated recovery at 25 °C and 110 °C for a NAND ring oscillator over 24 hours. Frequency shift over 24 hours has been greater than the gain in 6 hours resulting in a negative value for the first 6 hours of recovery.

Lastly, I have measured the effect of increasing the number of stages (LUTs) in ring oscillators in the Artix 7 series FPGA chip and can conclude based on Figure 2.16 and 2.17 that increasing the number of stages increases the frequency shift. This shift in frequency and its
relationship to the number of LUTs is not fully linear and one cannot conclude that adding an $X$ number of stages will necessarily increase device degradation by $kX$ amount.

![Inverter Ring Oscillator - Accelerated degradation vs. room temperature recovery for 3 oscillators](image)

**Figure 2.16** Effect of increasing the number of stages on frequency shift for an inverter oscillator with normal recovery.

Figure 2.16 illustrates the effect of increasing the number of stages on frequency shift of the oscillators with normal recovery at 25 °C. The 41 stage ring oscillator degraded around 0.8% more and recovered an extra 0.5% in comparison to the 21 stage ring oscillator. Figure 2.18 illustrates the same analysis as Figure 2.17 except with accelerated recovery and shows similar behavior with the exception of higher degradation and recovery values. It is important to remember that increasing the number of the stages also reduces the frequency at which the oscillators operate at and hence reduce the AC stress caused to the oscillators.
Figure 2.17 Effect of increasing the number of stages on frequency shift for an inverter oscillator with accelerated recovery.

Accelerated recovery at 110 °C for the 21-stage inverter ring oscillator has recovered 1.3% frequency shift and the 41 stage ring oscillator has recovered 1.6%. Room temperature recovery on the other hand has recovered 0.5% for the 21-stage oscillator and 1.1% for the 41-stage oscillator. In the next Chapter I will go over the effects of N/PBTI using simulation and the design of ASICs in order to measure these effects accordingly. The importance of NAND/NOR structures to measure for N/PBTI is also discussed in Chapter 3.
Chapter 3: N/PBTI in Simulations and ASICS

ASIC implementations are essential tools for studying the effects of NBTI/PBTI because of their importance in the industry and how extensively are used in electronic devices. A stress phase to demonstrate the effect of NBTI consists of increasing the temperature and supply voltage of transistors on chip [10] [2]. Because of the limitations faced when experimenting and modeling via an FPGA device and not being able to increase supply voltage directly using FPGA boards I have to use ASICs to have full control over temperature and supply voltage. For this project I have had access to the 28nm FDSOI technology provided by STMicroelectronics and have designed a number of oscillators using inverter and NAND/NOR gates in order to measure for N/PBTI separately. As discussed earlier inverter gate oscillators are not suitable structures for us to measure NBTI and PBTI separately [8] [19] [7] and in this work, the goal is to differentiate between the two in order to obtain data that is more accurate.

3.1 Conventional Inverter Based Ring Oscillator

Figure 3.1 shows the common three-stage ring oscillator in which every stage consists of an inverter that is made of a PMOS and an NMOS transistor. This circuit falls short of separating the effect of NBTI from PBTI. For instance, when you have a high logic at the first stage, the first NMOS circled in red in the first stage experiences stress. This results in a logic 0 at the output of the second stage which then stresses the PMOS transistor and as a result the circuit degrades under both NBTI and PBTI. We require a structure that enables us to stress the NMOS and the PMOS transistors individually.
Figure 3.1 Traditional inverter based ring oscillator. In case of logic 1 at the first stage, the red and blue circled devices (NMOS, PMOS) are stressed together when the circuit is operational.

3.2 NOR Based Ring Oscillator Structure to Measure NBTI

Let us now consider the circuit shown in Figure 3.2 where each stage of the ring oscillator consists of a NOR gate. In this case, there are two signals under our control in order to have the circuit in the two modes of stress and measurement. Stress mode consists of increasing the supply voltage and the Stress_Signal to the stress voltage level. This ensures that PMOS transistors P1-P3 at every stage are turned off and NMOS devices N2, N4, N6 of every stage are turned on in order to force a logic 0 at the output of every stage. DUT1-3 will experience NBTI as a result and isolate every stage from the next. In measurement mode, supply voltage is reduced to an operating voltage VDD and Stress_Signal is forced to ground in order to have the circuit operate as a simple ring oscillator [8].
In this circuit the PMOS transistor P1-P3 of every stage can have an effect on the delay and hence the frequency of operation. This delay can be reduced by sizing those PMOS devices larger than the rest. This will ensure that the effect of NBTI is mostly from the DUTs in the top stack of every stage and increasing the accuracy of our measurements.

In order to show the effect of NBTI, I have manually changed the threshold voltage of the PMOS transistors for eight points ranging from 3-24% shift and have also used three of the different types of NMOS transistors available. LVT (low threshold voltage), RVT (regular threshold voltage), and HVT (high threshold voltage) transistors were used in the inverter chain oscillators and the results of frequency shift are compared to the NOR oscillator. As illustrated in Figure 3.3, the NOR oscillator shows more sensitivity to the changes in the threshold voltage shift of the PMOS transistors and as a result is a more accurate structure to test for the changes in threshold voltage shift of PMOS transistors.
Chapter 3: N/PBTI in Simulations and ASICs

Figure 3.3 Frequency degradation of a NOR oscillator as a function of PMOS threshold voltage shift in % for inverter oscillators with 3 different PMOS transistors with 3 different threshold voltages.

3.3 NAND Based Ring Oscillator Structure to Measure PBTI

Figure 3.4 shows the NAND based ring oscillator in which we have two input signals of supply voltage and Stress_Signal2. In stress mode the supply voltage should be at stress voltage mode and the Stress_Signal2 signal is grounded to ensure that the top NMOS devices N1-N3 in the bottom stack are turned off in order to isolate the bottom NMOS transistors DUT1-3. Grounding the Stress_Signal2 signal also forces the output of every stage to logic 1 in order to put the bottom NMOS devices DUT1-3 in stress mode to experience PBTI. In measurement mode, both input signals are forced to VDD so that the circuit is converted to a ring oscillator to measure frequency. Just like the NOR based ring oscillator sizing the top NMOS device N1-N3
larger than the bottom NMOS ensures that the effect of PBTI on the delay and frequency of the circuit mostly comes from DUT1-3 [8].

Figure 3.4 NAND based ring oscillator structure in order to isolate NMOS transistors to measure PBTI [19].

Figure 3.5 illustrates the sensitivity of the NAND based ring oscillator shown in Figure 3.4, which has a higher slope than the rest of the inverter chain structures in terms of sensitivity. This Figure again shows that the NAND based ring oscillator is the preferred structure to test for the effect of PBTI separately.
Figure 3.5 Frequency degradation of a NAND oscillator as a function of NMOS threshold voltage shift in % for inverter oscillators with 3 different PMOS transistors with 3 different threshold voltages.

3.4 Degradation in Ring Oscillators Using Simulations

Ring oscillators are often used in mixed signal applications as voltage controlled oscillators (VCO) and can also be used to evaluate new technology nodes and the speed of a process. This section of the thesis will provide evaluation of aging and degradation in ring oscillators. It is known that aging in ring oscillators causes a drop in oscillator switching frequency [14] [7]. I will present degradation simulation results for AC and DC stress on oscillators for the 28nm technology node. I have been able to successfully separate the effect of NBTI from PBTI in simulations using the previous mentioned NAND/NOR oscillators. Finally, the effect of temperature on these ring oscillators is shown.
I have run my simulations using MOSFET Reliability Analysis (MOSRA) in HSPICE. MOSRA allows for BTI and reliability simulations in order to detect reliability failures before the design process begins which allows designers to specify $V_{TH}$ guardbands to account for aging during IC lifetime”. MOSRA provides the user with the ability to use the built-in reliability models or use their own. In this work, I have used the built-in models provided by MOSRA to run my simulations [20].

As discussed earlier in the introduction, BTI causes the amount of charge in the gate dielectric to change by trapping and de-trapping of electric charges. In the case of DC stress, the trapped charges keep accumulating, further increasing $V_{TH}$ and decreasing channel carrier mobility [21]. AC stress on the other hand, allows for the trapped charges to be de-trapped depending on trapping/de-trapping time constants used in the MOSRA models. De-trapping leads to partial recovery of N/PBTI which is modeled in this simulation software [22]. Another important factor that has a direct effect on BTI is operating temperature of the device. Because of the variations in the device operating voltage and temperature, there is some level of partial recovery that happens throughout degradation and MOSRA models take into account the mentioned conditions in device degradation. The models realize the amount of stress caused to the device and converts them to key MOSFET model parameters such as $V_{TH}$ or mobility, which are then converted into other key parameters such as frequency of a circuit. The models for N/PBTI are based on two key phenomenon in device aging one relating to the contribution of the interface traps as shown in Equation 3.1 and one relating to the contribution of the traps deep inside the dielectric layer as shown in Equation 3.2 [20].
\[ \Delta V_{TH,IT} \sim \exp \left( -\frac{E_a}{KT} \cdot \left[ \frac{\varepsilon}{t_{ox}} (V_{gs} - V_{TH}) \right]^{TITCE} \cdot \exp[TITFD \cdot E(V_{gs}, V_{ds})] \cdot t^{NIT} \right) \]

Equation 3.1 NBTI model for the contribution of interface traps. [20]

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Definitions</th>
</tr>
</thead>
<tbody>
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<td>(E_a)</td>
<td>Activation Energy</td>
</tr>
<tr>
<td>(K)</td>
<td>Boltzmann’s Constant</td>
</tr>
<tr>
<td>(T)</td>
<td>Junction Temperature</td>
</tr>
<tr>
<td>(\varepsilon)</td>
<td>Dielectric permittivity</td>
</tr>
<tr>
<td>(T_{ox})</td>
<td>Oxide Thickness</td>
</tr>
<tr>
<td>(V_{gs})</td>
<td>Gate to source voltage</td>
</tr>
<tr>
<td>(V_{th})</td>
<td>Threshold voltage</td>
</tr>
<tr>
<td>(TITCE)</td>
<td>“Inversion charge exponent for interface trap inducing threshold voltage degradation” [23]</td>
</tr>
<tr>
<td>(TITFD)</td>
<td>“Oxide electric field dependence for interface trap inducing threshold voltage degradation” [23]</td>
</tr>
<tr>
<td>(E(V_{gs}, V_{ds}))</td>
<td>strength of the electric field of the dielectrics</td>
</tr>
<tr>
<td>(t)</td>
<td>Time</td>
</tr>
<tr>
<td>(NIT)</td>
<td>Number of Interface Traps</td>
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</tbody>
</table>
### Chapter 3: N/PBTI in Simulations and ASICs

#### Parameters Definitions

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Definitions</th>
</tr>
</thead>
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</tr>
<tr>
<td>TOTTD</td>
<td>“Temperature dependent component for oxide trap inducing threshold voltage degradation.” [23]</td>
</tr>
<tr>
<td>NOT</td>
<td>Number of Oxide Traps</td>
</tr>
</tbody>
</table>

Table 3.1 Variables and constants used in Equations 3.1 and 3.2.

\[
\Delta V_{TH,OT} \sim \exp \left[ - \frac{TOTFD + TOTTD}{E(V_{gs}, V_{ds})} \right] \cdot t^{NOT}
\]

Equation 3.2 NBTI model for contribution of traps deep inside the oxide layer. [20]

The terms used in the two equations above are described in Table 3.1. There is some partial recovery in BTI degradation of CMOS devices especially in AC stress condition because of the time-varying nature of AC stress [3]. This effect is also considered in MOSRA by Equation 3.3 where the parameters are explained in Table 3.2.

\[
\Delta V_{TH,AC} = TTD0 \cdot \Delta V_{TH} \cdot \exp(-TDCD \cdot g)
\]

Equation 3.3 [20]
### Parameters and Definitions

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>TTD0</td>
<td>Recovery model coefficient</td>
</tr>
<tr>
<td>TDCD</td>
<td>“Duty cycle dependent exponent for transient degradation of threshold voltage.” [23]</td>
</tr>
<tr>
<td>g</td>
<td>“A function of bias and time which represents a measure of the duty cycle of the waveform applied on the device during the transient simulation.” [23]</td>
</tr>
</tbody>
</table>

Table 3.2 Variables and constants used in equation 3.3.

Based on Equation 3.3, the total degradation based on N/PBTI becomes smaller when considering the effect of partial recovery. In the next section, results are presented to show comparisons between AC and DC degradation based on the models presented above.

The MOSRA software flow consists of two phases: pre-stress simulation and post-stress simulation as shown on Figure 3.6. During the first phase of the simulation, MOSRA simulates the electrical stress of selected MOSFET devices in the circuit based on the models provided by MOSRA or custom models provided by the user. The stress calculated based on the provided models is then integrated over the duration of the simulation time. Finally, the results of integration over the simulated time are extrapolated to calculate the final stress over the user-specified time of circuit operation. The second phase of the simulation translates the device degradation simulation results into circuit level degradation device [20]. For instance, if one intends to simulate a ring oscillator, the individual inverters are aged in the first phase of the
simulation and their device characteristics are extracted to be used to characterize aging in the entire ring oscillator.

![Diagram](image)

**Figure 3.6 MOSRA tool flow. [20]**

### 3.4.1 AC Degradation

In this section, I have used an AC signal to stress the oscillators and have measured the effect of N/PBTI in the 28nm technology node using a number of ring oscillators ranging from 9-31 stages. These oscillators have been designed with a fanout of one because optimizing the fanout to obtain higher frequencies is not of interest. I am interested in an initial frequency and the subsequent frequency shift as a result of degradation and recovery.
Figure 3.7 illustrates the effect of NBTI on the NOR oscillator shown previously. Stress time of 27 hours is applied as well as stress voltages at 1.2V, 1.4V and 1.6V. As expected, frequency degradation at a higher stress voltage is higher and reaches up to 0.2 % in 27 hours. We discussed previously that in High-k dielectric transistors the effect of PBTI has been reported to be higher than NBTI and Figure 3.8 can confirm those with the 28nm FDSOI technology, which uses the High-K metal gate. The effect of PBTI seems to be significantly higher than NBTI in our simulations and reaches up to 10% in 27 hours for a 1.6V stress voltage.

![Figure 3.7 NBTI AC frequency degradation vs stress time for 3 different gate stress voltages.](image-url)

\[
y = 0.0012x + 0.0318 \\
R^2 = 0.5689
\]

\[
y = 0.0041x + 0.0858 \\
R^2 = 0.6171
\]

\[
y = 0.0014x + 0.0383 \\
R^2 = 0.5697
\]
3.4.2 DC Degradation

DC degradation is another type of aging analysis that we have done, even though, it is not as realistic as AC degradation since most circuits are stressed by AC in real world environments. The results, however, can help to understand the 28nm technology and its shortcomings.

Figure 3.9 illustrates the effect of NBTI in our NOR oscillator. Stress time has been set to 1000000 seconds or 27 hours for 3 different stress voltages of 1.2V, 1.4V, and 1.6V. There is around 3% reduction in frequency for a stress voltage of 1.6V in only 24 hours.

The effect of PBTI is again more visible in this technology node with the High-K metal gate as shown in Figure 3.10. The stress time and voltage remain the same, however, frequency degradation hits as much as 32% in 27 hours for a stress voltage of 1.6V. These simulations are set to run at room temperature (25°C) to show the stress effect of bias voltage.
Figure 3.9 NBTI DC frequency degradation vs stress time for 3 different gate stress voltages.

Figure 3.10 PBTI DC frequency degradation vs stress time for 3 different gate stress voltages.
3.4.3 Temperature Degradation

In this section, the oscillators are stressed at high temperatures of 60 °C and 110 °C and frequency shift as a result of N/PBTI over 27 hours is shown. The temperatures chosen in this Section are the minimum and maximum temperatures that I have stressed my FPGA chip with and I will be using the same range of temperatures later to stress the ASIC.

![NBTI AC frequency degradation vs stress time for 60 °C and 100 °C.](image)

Figure 3.11 NBTI AC frequency degradation vs stress time for 60 °C and 100 °C.

As illustrated below in Figure 3.12, PBTI under AC stress and at high temperatures shows to effect frequency more than NBTI again because of the nature of High-K dielectric used in the 28nm technology node. For the same amount of stress, PBTI degradation shown in Figure 3.12 affects frequency by as much as 2.9% at 110 °C in 27 hours whereas NBTI only reaches 1.2% degradation in the same amount of time.
Figure 3.12 PBTI AC frequency degradation vs stress time for 60 °C and 100 °C.

3.5 28nm FDOSI ASIC Chip and Design Description

In order to characterize and model NBTI and PBTI, it is best to use ASICs in order to have control over the size of the transistors, bias/supply voltages and circuits such as the NAND/NOR structures discussed earlier in this Chapter. Using ASICs provides us with the ability to measure and model the effects of N/PBTI separately using NAND/NOR ring oscillators and single transistors. Using single transistors makes $V_{TH}$ extraction easier in order to realize the shift in $V_{TH}$ in comparison to ring oscillators and the reason is explained in Section 3.5.2.2.

3.5.1 Chip Design Description

My design consists of ring oscillators, single transistors, a temperature sensor, and a
comparator to control the on-chip temperature. The oscillators will be tested for N/PBTI by increasing temperature and the gate voltage in order to be stressed. A new oscillation frequency is recorded after the test and the shift in frequency corresponds to the shift in the threshold voltage which is of interest. By increasing $V_{TH}$ of a transistor, the power consumption increases and the chip operates under unwanted situations. The transistors and structures in my design are powered by a 0.9V DC supply. The chip outputs consist of high frequency RF signals at 1GHz to 1.5GHz for different ring oscillators and a single DC comparator output. There is also a temperature sensor circuit on my chip that senses changes in $V_{TH}$ as it increases by temperature and is able to output a DC voltage that corresponds to that temperature. The schematic of this CMOS sensor is shown in Figure 3.13 and is taken from the structure proposed in [24]. This structure uses the threshold voltage characteristics of a CMOS transistor to sense changes in temperature and it can output a linear voltage over the temperature range of 20-100 °C. The slope of the transfer function is 2mV/°C in my design which works as intended with my comparator described in Section 3.5.1.2 in order to achieve a resolution of ± 5 °C.
Figure 3.13 Temperature sensor circuit used in the chip [24].

Figure 3.14 Comparator circuit used in the chip [25].
This temperature sensor shown in Figure 3.13 which is based on the proposed structure in [25] is required in order to be fed into the comparator shown in Figure 3.14, which compares the temperature sensor output to a reference signal given by the user and disables/enables the oscillators depending on the temperature. Figure 3.15 shows the schematic of the design intended to stress ring oscillators under N/PBTI automatically.

Figure 3.15 Combination of comparator and temperature sensor in order to control ring oscillators precisely on-chip

Figure 3.16 below shows the final layout of my chip with IO placements around the package.
Signals that start with OS refer to the output of my ring oscillators and signals starting with S are the terminals of single transistors that I want to characterize. $V_{\text{ref}}$ refers to the DC input signal that will be fed to the comparator in order to control the temperature of the chip.

3.5.1.1 Ring Oscillators

There are three types of ring oscillators used in my design. NOR oscillators to test for NBTI, NAND oscillators to test for PBTI and conventional inverter based oscillators to
measure NPBTI which is a combination of N/PBTI. There are oscillators ranging from 9-31 stages in my design, which are connected to buffers at the output in order to increase the amplitude of the oscillations to be measured by the equipment in the lab. The output buffer consists of some inverters which are connected in series to drive a large load and is connected between the output of the ring oscillator and the I/O pads. Each inverter is larger than the previous inverter by a factor of A which is calculated by the following method and there are N stages for each buffer.

A large capacitive load of around 10pf is placed at the output of the inverter to work as the capacitive load of the I/O pads. This capacitance is so large that it makes the internal capacitances negligible. Based on the simulations two values for \( t_{\text{plh}} \) and \( t_{\text{phl}} \) which correspond to the delay of an inverter turning logic 0 into 1 and 1 to 0, respectively. This delay depends on how the NMOS and PMOS transistors in an inverter behave and how fast they respond to changes.

Using these two values we can calculate the values for \( R_n \) and \( R_p \) by the relationships:

\[
T_{\text{plh}} = 0.7 \times R_n \times C_{\text{Load}}
\]

\[
T_{\text{phl}} = 0.7 \times R_p \times C_{\text{Load}}
\]

We can then remove the large capacitive load and calculate the real propagation delays of the inverter gate. Using the real values of \( R_p, R_n, t_{\text{plh}}, t_{\text{phl}} \) we can calculate the real value of \( C_{\text{OUT}} \) by the following relationship:

\[
C_{\text{OUT}} = 0.7 \times (R_p + R_n) \times C_{\text{Load}}
\]

Number of inverter stages at the output buffer is calculated by,
\[ N = \ln \left( \frac{C_{\text{Load}}}{C_{\text{In}}} \right) \]

Lastly, \( A \) is calculated by [26],

\[ A = \left( \frac{C_{\text{Load}}}{C_{\text{In}}} \right)^{\frac{1}{N}} \]

In my design, \( A \) and \( N \) have final values of 4 and 5, respectively. Ideally, I would use counters in my design in order to capture frequency changes at the output more precisely, but that was something I did not anticipate to be required at the time of my design and I learned through working with the ring oscillators in the FPGA. Typically, the changes in frequency at higher frequency are very small and hard to measure [14]. This means that in order to record the changes in frequency effectively, one would require a very low frequency oscillator, or a frequency divider or a counter to count for the pulses for every \( n \) number of cycles. It is ideal to use a frequency divider on an FPGA to drop down the frequency and then measure the frequency shift with accuracy using a frequency counter or the N9030A spectrum analyzer. Having the frequency counter or clock divider off-chip provides an advantage in that stressing the chip only effects the DUT and not the secondary circuitry such as the clock-divider or the counters. This will result in more accurate measurements.

### 3.5.1.2 Comparator

The self-biasing, which happens by biasing the internal amplifier node, creates a negative-feedback loop. This will stabilize the bias voltages and as a result, any variations in processing parameters or conditions of the transistors that change the bias voltage of the
internal amplifier is corrected for by this structure through the negative feedback [25]. This structure ensures that the current running through it remains the same independent of the bias voltage and the output voltage works like a differential amplifier depending on the two inputs supplied. The size of the transistors in this circuit was tuned by trial and error in order to achieve a resolution of 10mV between the supplied inputs which corresponds to 5 °C in the temperature sensor circuit.

3.5.1.3 Temperature Sensor

The temperature sensor shown in Figure 3.13 has a dependence on the threshold voltage shift, which comes because of temperature changes and is characterized by Equation 3.4.

\[
V_{out} = \frac{V_{tn1} \cdot \sqrt{\frac{(W/L)^2}{(W/L)^3}} - V_{tn2} \cdot \sqrt{\frac{(W/L)^2}{M \cdot (W/L)^1}} - V_{tn3} \cdot \sqrt{\frac{(W/L)^2}{M \cdot (W/L)^1}}}{1 + \sqrt{\frac{(W/L)^2}{(W/L)^3}} - \sqrt{\frac{(W/L)^2}{M \cdot (W/L)^1}}}
\]

*Equation 3.4 Equation relating \(V_{TH}\) shift to the \(V_{OUT}\) of the temperature sensor [24].*

This equation has a linear dependence on the threshold voltage and M represents the current mirror gain. W and L represent the width and the length of each transistor and \(V_{tn}\) represents the threshold voltage of each of the NMOS transistors. The transistors in this
circuit are tuned to output the biggest $V_{\text{out}}$ possible based on Equation 3.4 for the range 20-100 °C which is my desired operating temperature for the chip. The transistors used in my design all have a 28nm length. The width of N3 and N2 is sized equally and ten times larger than the width of N1. This will make sure that $\frac{W_2}{W_3} = 1$ and $\frac{W_2}{W_1} = 10$ and these ratios resulted in $V_{\text{out}}$ to have a resolution of 2.5 mV/°C for the 20-100 °C temperature range.

3.5.2 ASIC Test Plan

In this section of the report, the test plan for chip is discussed in detail with the equipment required in order to measure changes in frequency caused by temperature and bias voltage stress.

3.5.2.1 Setup Diagrams for Each Phase of the Test

Figure 3.17, and 3.18 illustrate the frequency measurement phase and stress phase of the test plan respectively. These are the very high-level diagrams of the test phases. Detailed diagrams with the required equipment are shown in the next section of the thesis.
Figure 3.17 Diagram showing the frequency measurement phase of the test setup.

Figure 3.18 Diagram showing the stress phase of the test plan.
3.5.2.2 Frequency Measurements and Comparison

In the first step of the setup, frequency measurements must be made and the best way to do this is using a frequency divider externally using another FPGA and connecting the output of the clock divider to the spectrum analyzer. Below are steps to follow for frequency measurement of oscillator signals.

- Connect LXQ-30-2 with a 0.9 Volt signal to the header pins VDD and GND to start the ring oscillators.
- Connect the oscillator signals to the N9030A PXA spectrum analyzer using a frequency divider on the Artix 7 series FPGA. Then freeze the spectrum and mark the peak of the spectrum bandwidth with the marker. This will measure the oscillation frequency of the first set of ring oscillators.
- Disconnect VDD from LXQ-30-2 to stop oscillation on the reference ring oscillators.
- Next step is the stress mode, which is explained in the Section 3.5.2.3.
- After the stress is done on first set of oscillators, new measurements need to be done to compare the new frequencies to the reference non-stressed oscillators.
- This time, connect the spectrum analyzer to the second set of ring oscillators and freeze the spectrum to measure the peak with the marker.
- Now using the delta marker, we can see the difference in frequency of the stressed vs. non-stressed oscillators.

Another set of measurements are required in order to analyze device characteristics of single transistors that are used on the test chip. This is done by connecting the terminals of
each transistor (source/drain/gate) to the HP 4155A semiconductor parameter analyzer and extract the IV curves. $V_{TH}$ can then be extracted from the IV curves by Equation 3.5 which models the CMOS current in the saturation region. In this model $W$ is the width of the transistor, $C_0$ is the oxide capacitance per unit area, and $\mu$ is the free carrier mobility. $V_{GS}$ is also the intrinsic gate to source voltage [27].

$$I_D = \frac{W}{L_{eff}} \mu C_0 (V_{GS} - V_T)^2$$

Equation 3.5 Drain current of a CMOS transistor in the linear region [27].

The cables and connectors needed in this part of the setup are:

- BNC to SMA adapter at the PXA spectrum analyzer
- General power cables for the power supply.

### 3.5.2.3 Stress Mode Setup and Recovery Phase

This is the second step of the test setup, which is required in order to stress the second set of oscillators. The equipment used in this step are HP 4155A Semiconductor Parameter Analyzer to create the reference input signal for the comparator, my temperature control system, and the Xantrex, LXQ-30-2 DC Power Supply. Listed below are the steps to follow to stress the chip for secondary measurements.

- Disconnect VDD_1 from LXQ-30-2 to stop oscillation on the reference ring
oscillators.

- Connect VDD_2 to LXQ-30-2 with 1 to 2 volts for the gate bias stress.
- Connect 4155A Semiconductor Parameter Analyzer SMU1 output to V_{ref} signal. This device is of interest because it has a resolution of microvolts and it satisfies my needs for increments of 1-2 mV.
- Connect the other supply voltage terminal of LXQ-30-2 with power cables to VDD_3 signal to power up the comparator and the on-chip temperature sensor.
- Using my temperature control system, heat up the chuck on the probe until the desired temperature has been reached. The cables and connectors needed in this part of the setup are:
  - Triaxial to BNC from SMU1 output of the 4155A Semiconductor Parameter Analyzer to BNC
  - BNC TO SMA to connect to the probe at the probing station.

### 3.5.2.4 Detailed Setup Diagrams and Test Setup Equipment

My test setup consists of an initial measurement mode in which the frequency of the oscillators is measured followed by a stress mode, which consists of increasing the on chip temperature from 60 – 110°C and applying negative/positive biasing to the transistor gates to replicate the effect of N/PBTI. The detailed setup diagrams for each phase of the test are shown on Figures 3.19 and 3.20.
Figure 3.19 Detailed setup diagram of the first phase of the test setup.
Figure 3.20 Detailed setup diagram of the second phase of the test setup.

The lab equipment needed to create this scenario is as follows.

- Agilent N9030A PXA Signal Analyzer 3Hz - 26.5 GHz
- HP 4155A Semiconductor Parameter Analyzer (MPMSU)
- Xantrex, LXQ-30-2 DC Power Supply, 0-30V, 0-2A
- Signatone S-1160 Manual Probe Station with Hot Chuck
- Temperature and stress/recovery control system.
Chapter 4: Result Analysis

In this Chapter, I compare the results of the simulations as well as the experimental results extracted from the FPGA. I will then show the relationship between frequency and $V_{TH}$ and extract the degradation parameters of the Artix 7 series FPGA chip and estimate the device lifetime based on the models proposed in [14] and [15].

Figure 4.1 compares the degradation of NAND/NOR oscillators in simulations using the library models. Based on this data, PBTI shows significant degradation in comparison to NBTI which can be explained by the nature of the High-K dielectric used in this technology. PBTI at 60 °C degrades circuit operations and frequency more than NBTI at 110 °C which matches the experimental data in [4] which discusses that the 32nm High-K technology node suffers from PBTI degradation more than NBTI at elevated temperatures and supply voltages. In simulations at 110 °C, frequency shifted around 2.8% as a result of PBTI, which is around 1.8% higher than NBTI at this same temperature.

![NBTI Vs. PBTI AC frequency degradation (%) with temperature vs. Stress time (Hours)](image)

Figure 4.1 Simulation results comparing degradation and frequency shift for various oscillators.
Next, the degradation experiments on the Artix 7 series FPGA resulted in almost similar degradation based on the three type of oscillators we used. However, the trend was not exactly the same as the simulations and that was expected. We do not have access over individual transistors in the FPGA as we have implemented the ring oscillators using hard macro LUTs. In addition, a 4-1 LUT implements a NAND/NOR gate using the same number of components in the LUT as an inverter gate and therefore, the stress caused in the circuits is the same. In simulations and on the ASIC design we have access to every transistor in the oscillator and that has enabled us to use the NAND and NOR ring oscillators to our advantage in order to characterize NBTI and PBTI separately.

![Graph](image)

**Figure 4.2 Experimental results of frequency shift comparing accelerated stress and normal recovery.**

Figure 4.2 shows the experimental results on the Artix 7 series FPGA chip and compares accelerated degradation at 110 °C and 60 °C and summarizes the results extracted
in Chapter 2. Accelerated recovery as shown in Figure 4.3 increases the rate at which frequency shift recovers over time and in this work we have been able to increase this recovery by 50% by elevating the temperature from 25 °C to 110 °C.

Figure 4.3 Experimental results of frequency shift comparing accelerated stress and recovery.

Moreover, increasing the number of gates from 21 to 41 stages, also increased degradation from 2.6% to 3.1% and the recovery amount from 1.3% to 1.6% as shown in Figure 4.4 which suggests that increasing the number of LUTs has a direct effect on degradation and recovery.
Based on the results extracted from frequency degradation in this work we can extract the change to $V_{th}$ which is an important parameter in transistor reliability. Threshold voltage shift due to the BTI effects follows a logarithmic pattern which can be described by Equation 4.1.

$$\Delta V_{TH} = \theta_1 \left( A + \log(1 + Ct_1) \right)$$

Equation 4.1 Equation describing the logarithmic behavior of threshold voltage vs. stress time.

Where $\theta_1$ is defined by Equation 4.2 where $A$, and $C$ are constant fitting parameter which can be extracted from measurements.

$$\theta_1 \sim K_1 e^{\left(\frac{-E_a}{kT}\right)} e^{\left(\frac{-BV_{dd}}{kT_ox}\right)}$$

Equation 4.2 Equation relating threshold voltage shift to activation energy [14].
In Equation 4.2, k is the Boltzmann constant, t is time; T is temperature, and $E_a$ is the activation energy, $t_{ox}$ is oxide thickness, $K_1$ and B are constant fitting parameters. Since direct measurement of threshold voltage shift of a single transistor is not feasible on an FPGA device, we rely on ring oscillators to reflect the effect of threshold voltage shift. Based on [15] one can obtain Equation 4.3 which shows the relationship between the threshold voltage shift and the ring oscillator’s time delay.

$$\Delta t_d \sim \frac{\Delta V_{th}}{V_{dd}-V_{th}} \cdot t_{d0}$$

**Equation 4.3 Equation relating $V_{th}$ shift to delay/frequency.**

Where $t_{d0}$ is the original delay of the gate before any shift in $V_{th}$. Typical numbers for activation energy $E_a$ in silicon semiconductors generally range between 0.3-1.2 eV. However, activation energy values as a result of dielectric/oxide break down and hole/electron trapping range from 0.3-0.4 and in this experiment I chose 0.4 eV which seems to be a typical number for this technology node based on the literature [28] [14] [29].

Activation energy describes the minimum energy required for a chemical system with potential reactants to result in a chemical reaction and going over a barrier (required energy) as shown in Figure 4.5. In our experiments activation energy is an experimentally determined parameter which relates the sensitivity of the reaction-diffusion model to temperature. The higher the activation energy of a chemical process, the harder it is for that process to happen.
Increasing temperature as shown in the previous chapters increases the rate at which recovery and degradation happen.

![Activation energy in presence of a catalyst](image)

Figure 4.5 Activation energy in presence of a catalyst. Image from [30]

Finally, in order to extract the fitting parameters, using Equation 4.3, I converted $\Delta t_d$ into $\Delta v_{th}$. Using the fit function tool in Matlab I was able to extract the fitting parameters, A, B, C, and K1 to Equation 4.1 and the extracted values are shown in Table 4.1
<table>
<thead>
<tr>
<th>Fitting Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>K1</td>
<td>4e^{-1}</td>
</tr>
<tr>
<td>A</td>
<td>0.352</td>
</tr>
<tr>
<td>B</td>
<td>-2.2e^{-29}</td>
</tr>
<tr>
<td>C</td>
<td>0.764</td>
</tr>
</tbody>
</table>

Table 4.1 Fitting parameters extracted from Matlab.

The results have been plotted for 10 years of stress time at 3 different temperatures of (25, 50, and 110)°C.

Figure 4.6 – Threshold voltage degradation in 10 years based on the degradation parameters extracted using experimental data.
The results shown in Figure 4.6 show that stressing the current 28nm Artix 7 series FPGA chip for 10 years at 110 °C shifts the threshold voltage from 0.3V to 0.6V which might make the device unusable. Room temperature effects the threshold voltage only by 10%, however, that is not the case in most commercial devices as most processors run in the 70-100°C range. In conclusion, the effect of degradation as a result of elevated temperatures can seriously increase the threshold voltage of transistors. Places such as server farms which use processors for longer than usual periods (5 years), suffer from this degradation, however, accelerated recovery at elevated temperatures can help to reverse this process as shown in Figure 4.7. This Figure illustrates that accelerated recovery can recover V_{TH} shift by around 50% which means that it will change from 0.3V to 0.45V and shows accelerated recovery has helped in order to restore 0.15V in 10 years in comparison to room temperature recovery.

Figure 4.7 - Threshold voltage changes in 10 years based on the extracted activation energy at three different temperatures.
Chapter 5: Conclusions and Future Work

Transistor aging which comes as a result of device degradation at high temperatures and gate stress bias voltage reduces the lifetime of circuits by increasing the threshold voltage of devices overtime. This makes wearout estimation a necessity for future circuits given that the processors inside server farms or outer space crafts are not often replaced and this can lead to critical failure and malfunctions overtime.

In this work we concluded that N/PBTI is still a major issue with the 28nm High-k technology node based on our simulation results in Chapter 3 and that PBTI shows to cause 3% frequency degradation in 27 hours under AC and NBTI causes a 1.5% frequency shift under the same stress conditions which shows PBTI in fact contributes twice as much as NBTI in the 28nm High-K technology node. We have shown that the effect of PBTI cannot be largely ignored especially in High-K dielectric materials as they are shown to be more prone to device degradation of the NMOS in similar technology nodes [7] [4]. We started our work by showing that FPGAs are susceptible to aging and N/PBTI by stressing various ring oscillators and experiments using our own temperature control system to stress the FPGA chip. The oscillator with the gate stress voltage at higher temperatures suffered an extra 1.5% frequency shift compared to the oscillators that were stressed at lower temperatures. Next, we stressed the FPGA chips at different ranging from 60 °C - 110 °C and noticed that with AC stress at 110 °C we get around 2.5% frequency drop. We then used elevated temperatures to recover the frequency while having the devices turned off. At 110 °C on an inverter ring oscillator we have been able to recover up to 1.3% of a 2.7% loss in frequency over 48 hours.
Therefore, based on our experimental results we have concluded that high temperatures help in order to recover device degradation that matches the data found in [13] which claims to have achieved full recovery at temperatures above 325 °C. Finally, we extracted the degradation parameters based on the experimental results extracted from the Artix 7 series FPGA chip which can be used to estimate transistor lifetime using the relationship proposed in [14].

As part of this work we have designed an ASIC with a series of experimental structures to test for the effects of N/PBTI separately for the 28nm technology node.

This chip motivates the next milestone for this project to study the effect of reverse bias in NMOS/PMOS transistor while recovering and compare the effect of reverse bias voltage in recovery to temperature. Moreover, I would like to use on-chip counters and frequency dividers in the next iteration of the chip in order to have the entire circuitry on one device, but this has a downfall that the frequency divider and the counter will also age and probably affect the models. I am interested in modeling the effects of N/PBTI based on the 28nm ASIC and compare the simulation results to the experiments and come up with my own model relating the effect of threshold voltage shift to operating frequency of oscillators. Single transistors used on the chip should be able to help me extract the threshold voltage of transistors easier than in ring oscillators as explained earlier in Chapter 3. By using this data I will be able to compare the threshold voltages extracted from the ring oscillators to those extracted from single transistors and model this relationship. I also believe that N/PBTI is a function of the applied AC stress frequency in circuits and operating frequency in ring
oscillators [31], but this effect is not taken into account in the current models in the literature and I would like to model this frequency dependence.

Finally, based on my result analysis in Chapter 4 and the degradation parameters extracted, I concluded that the Artix 7 series FPGA’s $V_{TH}$ will shift by almost 100% to 0.6V in 10 years under 110 °C stress. This will make the chip unusable and would mean that my method of accelerated recovery can make the FPGA chip last longer.

The accelerated recovery method discussed in this work by using elevated temperatures can be used in multi-core processors, where a number of cores can be put to sleep while being recovered at high temperatures using the heat generated by other cores. This is while the rest of the cores are operational which can potentially be an industrial application of this work in the future. This would lead to circuits that recover from threshold voltage shift and degradation automatically.

In summary, this research showed that N/PBTI especially in High-K dielectric devices is still a major issue in circuit reliability in the 28nm technology node and that PBTI contributes more to device degradation than NBTI even at lower temperatures as shown in Figure 4.1. We also found that accelerated recovery at higher than room temperatures can help in order to reverse degradation by as much as 50% of the degraded frequency in 24 hours.
Bibliography


