**Study of Near-surface Stresses in Silicon around Through Silicon Vias at
Elevated Temperatures by Raman Spectroscopy and Simulations**

by

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Abstract

Three-dimensional (3-D) integration has emerged as an effective solution to overcome the wiring limit imposed on device density and performance with continued scaling. Through silicon vias (TSVs), which provides interconnection between stacked chips, are essential for the 3-D integration. However, due to the large mismatch of the thermal expansion coefficients (CTEs) between via-filling material (Cu) and Si, thermal stresses induced during processing can result in undesirable mobility shifts in devices and serious reliability problems. In this work, the near-surface stress distributions around TSV structures were studied using both experimental and numerical approaches.

Stress measurements and characterizations by micro-Raman spectroscopy at elevated temperatures are conducted to study the stress origin and evolution in TSV structures. Micro-Raman spectroscopy measures a combination of tensile and compressive near-surface stresses in the Si around TSVs. The results show that increasing the sample temperature towards the annealing temperature of the TSV sample will reduce the near-surface stresses around the TSVs. Temperature dependent measurements reveal that the stresses near TSVs have two components: 1) pre-existing stress before via filling, and 2) CTE mismatch-induced stress. To further understand the origins of the stress fields near TSVs, various TSV structures and via-filling materials are studied.

The CTE mismatch-induced stress can be simulated by finite element analysis. The results obtained from the micro-Raman measurements are compared with the simulations. In particular, the differential values between the experimental data and simulation results are extracted in order to estimate the pre-existing stresses in the TSV structures. Once the pre-

existing stress component is taken into account, a good agreement between the Raman measurement and the finite element calculation is obtained.

The CTE-mismatch-induced stress resulted mobility change and keep-out zone (KOZ) at elevated temperatures are also estimated. Higher temperatures are shown to reduce the CTE-mismatch-induced stress component, and result in the shrinkage of KOZs in Si. The pre-existing stress is shown to be significant in a region equal or larger than the KOZs induced by CTE-mismatch-induced stress only and should be characterized and considered in the KOZ determination and circuit design.

Preface

The work in this thesis is funded by Natural Science and Engineering Research Council of Canada (NSERC). Most of the work was done in Department of Materials Engineering at UBC during the past two years, including the stress analysis by micro-Raman spectroscopy, the thermal process with Linkam heating stage and the FEA simulations. Experimentally, all the original TSV samples were fabricated by our collaborators in Singapore. The author designed and conducted all the Raman measurements with the heating conditions, and did all the data analyses in this work. The original FEA model of the TSV structure was offered by collaborators, while the model improvements, stress simulations and calculations of mobility variation were conducted by the author.

All the original TSV samples were fabricated by Dr. Kaushik Ghosh in Prof. Chuan Seng Tan's group at Nanyang Technological University and Dr. Hong Yu Li in the Institute of Microelectronics, A*STAR, Singapore. Moreover, the original FEA model of the TSV structure was set up by Mr. Jiye Zhang in Prof. Chuan Seng Tan's group at Nanyang Technological University, Singapore. Without the contributions from the collaborators, this thesis could not have been accomplished.

In addition, one journal article has been submitted for review based on the work in Chapter 2 and 3. Another journal article is in preparation based on the work in Section 2.4.

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To my parents

Chapter 1 Introduction

1.1 Background and Motivations

1.1.1 Challenges of Advanced ICs: The Interconnect Bottleneck

In the past few decades, we have witnessed an incredible revolution brought by information technology, which is based on the advancement of photonic and electronic devices, commonly in the form of integrated circuits (ICs). In the manufacturing of modern ICs, the processes can be divided into two categories: Front-End-Of-The-Line (FEOL) and Back-End-Of-The-Line (BEOL). In the FEOL process, individual devices, such as transistors that amplify and switch electronic signals, are patterned and fabricated on the surface of a silicon wafer. Subsequently, in the BEOL process, insulating layers (dielectrics) and metal lines are deposited and fabricated to interconnect the devices on the wafer.

The semiconductor industry has faced several challenges over the last decade in continually extending Moore's law, which says that the number of transistors on a single chip would double approximately every two years [1]. For classical transistor scaling, device performance improves as gate length, gate dielectric thickness, and junction depth are scaled. In contrast, scaled chip wiring (interconnect) suffers from increased resistance due to a decrease in conductor cross-sectional area and may also suffer from increased capacitance if metal height is not reduced with conductor spacing. Thus, while transistor speed has been increasing, the delay caused by interconnects is getting longer and longer, which has become the performance-limiting factor for new designs and is referred to as the “interconnect bottleneck”. In analogy, the

challenges that we are facing for transistor and interconnect scaling are like “faster cars on slower roads”.

Fig. 1.1 plots the gate and interconnect delay time as a function of the feature size, which clearly shows that the interconnect delay has become the dominating factor in limiting the performance of the ICs when feature size is less than 0.6 μm , for repeater spacings $L=3000 \mu\text{m}$.

Figure 1.1 Delay time of interconnects [2]: Comparison of delay time for gate and interconnect. Reprinted with permission from [2], © 2001 IEEE.

The chief concern in the interconnect scaling issue is the interconnect delay [3], also known as Resistive-capacitive (RC) delay, which can be expressed by the following formula [4]:

$$RC = 2\rho\kappa\epsilon_0 \left(\frac{4L^2}{P^2} + \frac{L^2}{T^2} \right), \quad (1.1.1)$$

where $P=W+S$ is the pitch between neighboring interconnects, L is the total line length, W is the interconnect line width, S is the distance between the edges of adjacent interconnects, T is the height of the interconnect, ρ is the resistivity of the interconnect material, κ is the dielectric

constant of the dielectric materials between the interconnect lines, and ϵ_0 is the vacuum permittivity. Fig. 1.2 shows a cross-sectional view of the interconnect layer with the relevant parameters. With geometry scaling, P and T are smaller and smaller, while L becomes longer and longer for each generation, resulting in longer interconnect RC delays.

Figure 1.2 A scaling effect on RC delay in interconnects. Figure source: Ryu, Suk-Kyu's Ph.D. dissertation [5].

Since the interconnect RC delay is proportional to the resistivity of the interconnect material ρ and the dielectric constant of the insulating layer between the interconnects κ , reducing ρ and/or κ will reduce the RC delay. In an effort to reduce ρ , copper has replaced aluminum as the interconnect material since the 90's. To reduce the dielectric constant κ of the insulating materials, low- κ dielectric materials [6] with the dielectric constant lower than silicon dioxide ($\kappa = 3.9$) has been introduced into the interconnects. Many materials with lower dielectric constants such as fluorine-doped silicon dioxide ($\kappa = 3.5$) [7], carbon-doped silicon dioxide ($\kappa = 3.0$) [8], and porous silicon dioxide ($\kappa = 2.0$) [9], have been integrated into the IC

manufacturing process. Ultimately, by formation of air-gaps/bubbles ($\kappa = 1.0$) [10] in the trench dielectric levels, the effective dielectric constant of the interconnect structure can be further reduced. However, the air-gap structures at the trench level confront serious challenges concerning their structural integrity and mechanical stability [11] [12]. In fact, as of today, the semiconductor industry still has difficulties in implementing low- κ interconnects with κ lower than 2.5.

Besides lowering the metal resistivity and dielectric constant κ value, another approach in decreasing the interconnect delay is at the packaging level, which is the implementation of three-dimensional (3-D) integration of ICs. We will further explain this in the following sections.

1.1.2 3-D Integrated Circuits (ICs)

Briefly speaking, three-dimensional integration can be defined as a technology stacking multiple processed wafers containing ICs on top of each other and using vertical interconnects between the wafers. This 3-D structure provides opportunities for improving electrical performance and enabling integration of devices with incompatible process flows [13]. The most compelling advantage of this structure is that the vertical interconnects successfully address the 2-D interconnects problem by replacing long horizontal interconnects with short vertical interconnects [14]. As a result, the RC delay, cross talk and power dissipation will be greatly improved. With the total length of interconnect fixed, a 25% or greater decrease in worst-case wire length [15] or interconnect power [16] could be achieved. In addition, by providing the opportunity for the integration of heterogeneous devices and technologies, such as memory, logic, RF and sensing circuits, the advent of 3-D ICs allows for higher device density and smaller packaging size, which eventually would lead to the manufacturing cost reduction.

Fig. 1.3 compares the 2-D and 3-D approaches in solving the fundamental wiring limits. Fig. 1.3 (a) shows the 2-D SiP (System-in-Package) solution, which has lengthy interchip connections between the logic and memory chips. Serious memory latency can exist in this case. Fig. 1.3 (b) shows the 2-D SoC (System-on-Chip) solution, which improves the memory latency and device performance by combining blocks of logic and memory components in the chip. However, such approach increases the fabrication cost significantly since it requires different process technologies for the different functions. Fig. 1.3 (c) shows the 3-D integration scheme, in which the logic and memory components are connected vertically. In this scheme, much shorter interconnects are needed (Fig. 1.4), and therefore the memory latency can be significantly reduced and the chip performance can be improved.

Figure 1.3 Schematic diagrams showing the difference between 2-D and 3-D interconnects (Source: Beyne [17]): (a) 2-D SiP integration; (b) SoC integration; (c) 3-D integration. Reprinted with permission from [17], © 2006 IEEE.

Figure 1.4 Replacing the long global wire in the 2-D scheme by 3-D IC with vertical connections and shorter wire. Figure courtesy of Kuan-Neng Chen at National Chiao Tung University, Taiwan.

1.1.3 Through Silicon Vias (TSVs)

A critical structural element in the 3-D integration is the through silicon via (TSV) [17] [18] [19] as shown in Fig. 1.5, which replaces the long wiring in the 2-D schemes by vertical connections between the stacked dies. The use of TSVs in 3-D integration can effectively improve system performance and reduce manufacturing costs. However, the TSV fabrication process is a bottleneck because it requires a much deeper hole to be created vertically through the substrate material using a special etching process.

Figure 1.5 3-D integration using TSV structures: (a) Illustration of TSVs. Figure courtesy of Chuan Seng Tan at Nanyang Technological University, Singapore. (b) TSV samples. Figure is from online web source: Ron Maltiel [20].

The fabrication of TSVs involves three key processes [21] [22] [23] [24]: 1) via hole etching, 2) TSV materials filling, and 3) Si wafer thinning and wafer bonding/debonding. For a reliable and efficient TSV fabrication, each of the three processes needs to be optimized. In general, DRIE (Deep reactive-ion etching), also known as the “Bosch” process, is applied to create the deep hole vertically through the silicon wafer for via etching process.

However, careful control of the Bosch process is needed to prevent formation of scallop-shaped sidewalls (Fig. 1.6 (a)) [21] [25], as the scalloped contours not only prevent a conformal barrier and seed layer deposition, but also increase copper (the widely used via-filling material) diffusion into silicon despite the presence of the barrier layer [26]. During the electroplating of Cu, voids can sometimes form inside the TSVs (Fig. 1.6 (b)) [27], directly affecting the device reliability. In addition, the thinning-down process of the Si substrate by chemical-mechanical polishing (CMP) could cause wafer warpage (Fig. 1.6 (c)) [28], which leads to subsequent problems in 3-D stacking. To address various processing issues, several processing flows have been investigated [21] [29] [30]. As of today, two TSV integration processes are mostly used in the semiconductor industry: ‘via-middle’ and ‘via-last’ processes. The main difference in these two processes is the sequence of the TSV formation relative to the wafer thinning and wafer bonding/debonding processes.

Figure 1.6 Processing issues: (a) scallops at sidewall, where TEOS is an insulating liner material [21]; (b) voids inside TSV [27]; (c) wafer warpage [31]. Reprinted with permission from [21] [27] [31], © 2008, 2010 IEEE.

Via-middle process

Fig. 1.7 schematically illustrates the via-middle process, which is performed following the FEOL fabrication process. A typical via-middle process flow to fabricate TSVs with a diameter of 10 μm and a depth of 50 μm in the Si substrate is described as the following. First, lithography is conducted to pattern the via openings across the wafer. Next, DRIE is used to create the via holes of desired dimensions. This is then followed by deposition of an oxide liner of around 1 μm thick. The oxide layer (dielectric layer) reduces capacitance and improves electrical isolation between the TSVs and the Si substrate. In some cases, instead of oxide,

polymeric dielectric materials [32] [33] such as benzocyclobutene (BCB) or parylene have been deposited as the sidewall insulators. To prevent diffusion of Cu into the Si substrate, a thin barrier layer (~50nm) of Ta/TaN or Ti/TiN is deposited. For Cu electroplating, a thin Cu seed layer is first deposited in the vias and then the vias are filled by electroplating process. A subsequent annealing step could be applied to stabilize the Cu grain structures and relax the stresses in Cu for further processing that follows. At the final stage of the TSV fabrication, CMP is conducted to remove the Cu overburden, top Ta/TaN and oxide layers, and to planarize the wafer surface. The fabrication of TSV structures is followed by the BEOL process in which interconnects are made and bonding pads are patterned. Finally, the Si substrate is thinned down to the optimized TSV height (~50 μm).

Figure 1.7 Via-middle process for TSV structures. Figure is from online web source: Yannou, J. [34].

Via-last process

The via-last process also involves similar processes as described before, including drilling of via holes and deposition of dielectric layer and barrier layers. However, although the final structure constructed by the via-middle or via-last process could be the same, the sequence of processes in the via-last process (Fig. 1.8) is quite different from the via-middle process. In the via-last process, both FEOL and BEOL structures are first fabricated on the Si wafer. Then,

the wafer is thinned down up to the depth that is targeted for the TSV height. This is then followed by etching of the via holes from the back side of wafer to reach the interface of BEOL interconnect lines, and filling the holes by the sequence of dielectric layer, Ta/TaN barrier layer, Cu seed, electroplating of Cu, and finally a CMP process.

Figure 1.8 Via-last process for TSV structures. Figure is from online web source: Yannou, J. [34].

1.1.4 Thermomechanical Stresses in Cu TSV Structures and The Impact on Mobility

As mentioned above, the technology of through silicon via (TSV) becomes one of the most promising enablers for 3-D integration of circuits and systems. By providing direct die-to-die connections to form stacked structures in 3-D integration, better electrical performance and lower power consumption can be achieved. Copper is widely used as the via-filling material because copper is compatible with the back-end of line (BEOL) processes along with appropriate electrical and mechanical properties. However, the embedded TSVs can induce a large quantity of stresses in the surrounding silicon, which are not desirable. Particularly, due to the relatively large mismatch of coefficients of thermal expansion (CTE) between silicon (2.3 ppm/°C) and copper (17 ppm/°C) [35], TSV fabrication can cause substantial thermomechanical stresses in silicon around TSVs. In the TSV fabrication process, a subsequent annealing step at a high temperature (200 °C, for example) after the Cu electroplating is applied to stabilize the Cu grain

structures and relax the stresses in Cu. During the cooling down to room temperature, copper contracts much faster than Si, and pulls the surrounding silicon, causing thermomechanical stresses in the silicon area. The TSV-induced stresses can cause reliability problems such as copper via extrusion and interfacial delamination [25] [36] [37] [38] [39], and undesirable mobility shifts in devices through the piezoresistivity effect [40] [41]. As most devices are located within a fraction of a micron deep from the wafer surfaces, near-surface stresses in Si around TSVs, their resulting carrier mobility change, and TSV-stress aware design are crucial for the successful implementation of 3-D integration.

Extrusion of Cu vias is frequently observed in the TSV structures undergoing high temperature excursion. The via pop-up phenomenon can cause interfacial failure of a TSV (Fig. 1.9 (a)) or/and cracking in Si near the lower ends of TSVs (Fig. 1.9 (b)) during the thermal processing [42]. The via extrusion can be accompanied by interfacial delamination, as shown in Fig. 1.9 (c). Moreover, the effects of Cu plasticity have drawn considerable attention since it may also play an important role in via extrusion.

Figure 1.9 Reliability problems in TSV structures [42]: (a) Interfacial delamination; (b) Silicon cracking; (c) Via extrusion (Pop-up). Figure is from online web source: Cho, S. [42].

Moreover, by the piezoresistivity effect, TSV-induced stresses will cause hole and electron mobility variation in devices, which can result in performance non-uniformity without proper control. Keep-out-zone (KOZ) is defined as the area surrounding each TSV where all logic cells must “keep out” so that they are not influenced by the TSV-induced stresses significantly. In real designs, the presence of abundant TSVs in use already has a big impact on 3D-IC layout. Reducing KOZ areas is desirable to save circuit design floor space as illustrated in Fig. 1.10.

Figure 1.10 Layouts with small versus large KOZ around TSVs [43]. TSV landing pads are large yellow squares. Reprinted with permission from [43], © 2010 IEEE.

1.2 Scope of The Thesis

In this thesis, micro-Raman stress measurements along with numerical simulations are used to study the near-surface stress distributions in TSV structures for 3-D integration of ICs. Stress measurements by micro-Raman spectroscopy at elevated temperatures are conducted in order to completely understand the stress evolution in TSV structures. Through the temperature-dependent stress characterization, the origin of stress in TSV structures is explored. Thermal stresses, the stress-resulting carrier mobility change and keep-out zone (KOZ) of TSV structures are analyzed, based on which reliable design and processing can be suggested. This thesis is organized as follows.

As an introduction, Chapter 1 presents a brief review of the background and motivation for this work. The current challenges related to the interconnects are discussed. In the course of the technology trend to overcome the challenges, the advantages of 3D integration and through

silicon vias are introduced and the fabrication processes are described. At last, thermomechanical stress issues near TSVs in Cu TSV structures are explained.

In Chapter 2, micro-Raman spectroscopy is used to measure the near-surface stress distributions in the TSV structures. Both one-dimensional (1-D) line scan and 2-D mapping at elevated temperatures have been performed to analyze the stress distributions in Si around the Cu TSVs. Two more batches of TSV samples, including Cu filled TSVs and carbon nanotube filled TSVs, with different fabrication processes are characterized by micro-Raman spectroscopy in order to investigate the process dependence of the stress fields near TSVs. The temperature effects on elasticity of silicon, the calibration method and error analysis of micro-Raman spectroscopy are presented in this chapter.

In Chapter 3, finite-element analysis is performed to compare with the Raman results shown in Chapter 2. The coefficients of thermal expansion (CTE) mismatch-induced stresses in the close vicinity of Cu TSVs at elevated temperatures are simulated and compared with the experimental results. The near-TSV stress fields were found to originate not only from CTE mismatch-induced stresses, but also from pre-existing stresses before Cu deposition. Stress-induced carrier mobility change and keep-out zone (KOZ) are also calculated in this chapter.

In conclusion, Chapter 4 summarizes the results from the present study and suggests potential directions for future work.

Chapter 2 Stress Characterization of TSV Structures

To understand the failure mechanisms and the stress-resulting carrier mobility change, and further determine the size of KOZ in the TSV structures, it is essential to experimentally characterize the induced stresses and material behaviors under the thermomechanical conditions after TSV fabrication. Various techniques have been adopted to investigate the thermomechanical stress in Cu TSV structures. They include synchrotron radiation X-ray diffraction [44], the bending beam technique [45] (i.e., the measurement of curvature change under thermal annealing), cross-sectional transmission electron microscopy (TEM) with convergent beam electron diffraction [46] and micro-Raman analysis, which is the most effective method [47]. The high-resolution TEM accompanied by electron diffraction could accurately extract the localized stress information. However, the TEM sample preparation is a destructive process that invariably causes partial stress relaxation that leads to less accurate measurement.

Among these techniques for stress characterization, micro-Raman spectroscopy, as a non-destructive method, appears particularly useful and was recently applied to measure the near-surface local stress distribution in Si around Cu TSVs [48] [49]. All of the previous Raman measurements have been done, however, at room temperature (RT). Since many ICs such as central processing units of computer cores operate in a temperature range from room temperature up to 80°C and higher due to heat generated by active device switching and leakage current, a study of stresses around TSVs at elevated temperatures is necessary for complete understanding of Cu TSVs stress evolution. Stress measurements by micro-Raman spectroscopy are the focus of this chapter. Moreover, temperature-dependent stress characterization can provide a useful tool in studying the stress origin, which will be discussed in Chapter 3.

2.1 Stress Characterization by Raman Spectroscopy

2.1.1 Fundamentals of Raman Spectroscopy in Stress Characterization

Micro-Raman spectroscopy was recently used for the measurement of local stress distributions in Si near Cu TSVs [48] [50]. This method is a spectroscopic technique where the stress magnitude is deduced from the frequency shift of the impinging laser light as a result of inelastic scattering by the Si lattice [51] [52] [53] in comparison with a stress-free Si reference. The lateral spatial resolution of micro Raman spectroscopy is on the order of 0.5 μm , depending on the laser wavelength and the objective lens [53]. For Si, the Raman penetration depth ranges up to $\sim 0.2 \mu\text{m}$ with 442 nm input laser wavelength. Moreover, this technique can be used to measure the near-surface stresses in Si around TSVs even with an oxide layer covering the wafer surface because the laser can penetrate the oxide layer with nearly 95% transparency. Next, let's review the fundamentals of Raman spectroscopy briefly.

The spontaneous Raman effect, which is a form of inelastic light scattering, happens when a photon interacts with an atom or a molecule in either the ground rovibronic (rotation-vibration) state or an excited rovibronic state. This results in the atom/molecule being in a so-called virtual energy state for a short period of time before an inelastically scattered photon results. In Raman scattering, the resulting rovibronic state of the atom/molecule is a different rotational or vibrational state than the one in which the atom/molecule was originally, before interacting with the incoming photon. The difference in energy between the original rovibronic state and the resulting rovibronic state leads to a shift in the emitted photon's frequency away from the input photon wavelength, which is the so-called Rayleigh line on the Raman spectrum.

The inelastically scattered photon can be either of higher or lower energy than the incoming photon. The shift in energy gives information about the vibrational modes in the system.

If the final vibrational state of the atom/molecule is more energetic than the initial state, the inelastically scattered photon will be shifted to a lower frequency for the total energy of the system to remain balanced. This shift in frequency is designated as an anti-Stokes shift. If the final vibrational state is less energetic than the initial state, then the inelastically scattered photon will be shifted to a higher frequency, and this is designated as a Stokes shift. Raman scattering is an example of inelastic scattering because of the energy and momentum transfer between the photons and the atoms/molecules during the interaction. Rayleigh scattering is an example of elastic scattering, and the energy of the scattered Rayleigh scattering is of the same frequency (wavelength) as the incoming electromagnetic radiation. Fig. 2.1 is an energy-level diagram showing the states involved in Raman scattering and Rayleigh scattering. Stokes scattering peaks are stronger than anti-Stokes scattering peaks.

Figure 2.1 Energy-level diagram showing the states involved in Raman scattering processes.

Figure is from online web source: Wikipedia [54].

The effect of strain (ε_{ij}) on the Raman modes in (001) silicon can be described by the secular equation [51]:

$$\begin{vmatrix} p\varepsilon_{11} + q(\varepsilon_{22} + \varepsilon_{33}) & 2r\varepsilon_{12} & 2r\varepsilon_{13} \\ 2r\varepsilon_{12} & p\varepsilon_{22} + q(\varepsilon_{33} + \varepsilon_{11}) & 2r\varepsilon_{23} \\ 2r\varepsilon_{13} & 2r\varepsilon_{23} & p\varepsilon_{33} + q(\varepsilon_{11} + \varepsilon_{22}) \end{vmatrix} - \lambda I = 0 \quad ,$$

(2.1) where p , q and r are material parameters representing the phonon deformation potential, with $p = -1.43\omega_0^2$, $q = -1.89\omega_0^2$, and $r = -0.59\omega_0^2$ [52], and $\omega_0 \sim 520 \text{ cm}^{-1}$ is the Raman frequency of the unstrained Si crystal. The eigenvalues (λ_i) of the secular equation give the Raman frequency shift

$$\Delta\omega_i = \omega_i - \omega_0 \approx \frac{\lambda_i}{2\omega_0} \quad (i = 1 \sim 3). \quad (2.2)$$

Assuming linear elasticity, the strain components are related to the stress components (σ_{ij}) by Hooke's law:

$$\begin{Bmatrix} \varepsilon_{11} \\ \varepsilon_{22} \\ \varepsilon_{33} \\ 2\varepsilon_{23} \\ 2\varepsilon_{13} \\ 2\varepsilon_{12} \end{Bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{bmatrix} \begin{Bmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{23} \\ \sigma_{13} \\ \sigma_{12} \end{Bmatrix}, \quad (2.3)$$

where $S_{11} = 7.68 \times 10^{-12} \text{ Pa}^{-1}$, $S_{12} = -2.14 \times 10^{-12} \text{ Pa}^{-1}$, and $S_{44} = 12.7 \times 10^{-12} \text{ Pa}^{-1}$ [52] are the elastic compliance of Si.

The second rank Raman tensors describing three optical modes for the unstrained Si crystal are

$$R_1 = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & d \\ 0 & d & 0 \end{pmatrix}, R_2 = \begin{pmatrix} 0 & 0 & d \\ 0 & 0 & 0 \\ d & 0 & 0 \end{pmatrix}, R_3 = \begin{pmatrix} 0 & d & 0 \\ d & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix}. \quad (2.4)$$

Under the effect of strain, the Raman tensors become [55] [56] [57]

$$R'_i = \sum_{k=1}^3 R_k (v'_i \cdot v_k), \quad (2.5)$$

where v'_i and v_k are the eigenvectors of the secular equation with and without the strain, respectively.

The intensity of the Raman signal for each optical mode is

$$I_k = C |e_i \cdot R'_k \cdot e_s|^2, \quad (2.6)$$

where e_i and e_s represent the polarization vectors of the incident and scattered light, respectively, and C is a constant scalar. Most Raman systems have a backscattering configuration, where the incident light is nearly perpendicular to the sample surface. For backscattering from (001) Si surface, both the incident and scattering vectors, e_i and e_s , can be assumed to be parallel to the surface plane. The relationship between the Raman intensity and the polarization vectors in Eq. (2.6) suggests the possibility to select a specific Raman mode by properly choosing the polarization of the incident and scattered light. In the case of unstrained silicon, there are three

degenerate optical modes, having the same frequency ($\omega_0 \sim 520 \text{ cm}^{-1}$) but different polarizations [57]: two transverse optical modes (TO) and one longitudinal optical (LO) mode. However, with strain, the three optical modes in general have different frequencies (ω_i) and different intensities (I_i), corresponding to three Raman peaks. When the three Raman peaks are indistinguishably close, the average frequency shift is taken as [55]

$$\Delta\omega = \frac{I_1\Delta\omega_1 + I_2\Delta\omega_2 + I_3\Delta\omega_3}{I_1 + I_2 + I_3}. \quad (2.7)$$

Now let's consider a specific example. On the (001) Si surface, the stress along the [110] direction can be represented as $(\sigma_r, \sigma_\theta)$ in a cylindrical coordinate. In the reference coordinate with respect to the crystal axes, the stress components are

$$\sigma_{11} = \sigma_{22} = \frac{\sigma_r + \sigma_\theta}{2}, \quad (2.8)$$

$$\sigma_{12} = \frac{\sigma_r - \sigma_\theta}{2}, \quad (2.9)$$

$$\sigma_{31} = \sigma_{32} = \sigma_{33} = 0. \quad (2.10)$$

By Eq. (2.3), the strain components are obtained as:

$$\varepsilon_{11} = \varepsilon_{22} = \frac{S_{11} + S_{12}}{2}(\sigma_r + \sigma_\theta), \quad (2.11)$$

$$\varepsilon_{33} = S_{12}(\sigma_{11} + \sigma_{22}) = S_{12}(\sigma_r + \sigma_\theta), \quad (2.12)$$

$$\varepsilon_{12} = \frac{S_{44}}{2}\sigma_{12} = \frac{S_{44}}{4}(\sigma_r - \sigma_\theta), \quad (2.13)$$

$$\varepsilon_{13} = \varepsilon_{23} = 0. \quad (2.14)$$

Insert Eqs. (2.11~14) into the secular equation (2.1), and the eigenvalues are obtained as

$$\lambda_1 = \frac{p(\varepsilon_{11} + \varepsilon_{22}) + q(\varepsilon_{11} + \varepsilon_{22} + 2\varepsilon_{33}) + 4r\varepsilon_{12}}{2} = \frac{p(S_{11} + S_{12}) + q(S_{11} + 3S_{12})}{2}(\sigma_r + \sigma_\theta) + \frac{rS_{44}}{2}(\sigma_r - \sigma_\theta), \quad (2.15)$$

$$\lambda_2 = \frac{p(\varepsilon_{11}+\varepsilon_{22})+q(\varepsilon_{11}+\varepsilon_{22}+2\varepsilon_{33})-4r\varepsilon_{12}}{2} = \frac{p(S_{11}+S_{12})+q(S_{11}+3S_{12})}{2}(\sigma_r + \sigma_\theta) - \frac{rS_{44}}{2}(\sigma_r - \sigma_\theta), \quad (2.16)$$

$$\lambda_3 = p\varepsilon_{33} + q(\varepsilon_{11} + \varepsilon_{22}) = [pS_{12} + q(S_{11} + S_{12})](\sigma_r + \sigma_\theta). \quad (2.17)$$

In a backscattering configuration with $e_i = (110)$ and $e_s = (100)$, the Raman intensities are zero for the first two modes ($I_1 = I_2 = 0$), and only the third Raman mode is detectable ($I_3 \neq 0$). Thus, by Eq. (2.2), the Raman shift for the third mode is related to the stress components as:

$$\Delta\omega_3 \approx \frac{\lambda_3}{2\omega_0} = \frac{pS_{12}+q(S_{11}+S_{12})}{2\omega_0}(\sigma_r + \sigma_\theta). \quad (2.18)$$

To determine the effective proportionality factors between the Raman shift and the stress sum for the specific experimental conditions, calibration measurements by high-resolution XRD on an equi-biaxially stressed film system were conducted, yielding the relation [48]

$$\sigma_r + \sigma_\theta(MPa) = -470\Delta\omega_3(cm^{-1}). \quad (2.19)$$

The obtained sensitivity factor corresponds to phonon deformation potential parameters in between the values derived by Chandrasekhar [58] and Anastassakis [59]. Note that the reference frequency ω_0 also depends on the system calibration, typically with $\pm 0.02 \text{ cm}^{-1}$ spectral resolution, which corresponds to a stress resolution of $\sim 10 \text{ MPa}$ [60] [61].

2.1.2 Raman Measurement Conditions in This Work

A LabRAM HR Raman confocal microscope by Horiba Scientific was used for the Raman measurements. The input HeCd laser used is 442 nm wavelength. 2400 grating was selected for high spectral resolution, and the focused laser spot size is about $0.8 \mu\text{m}$ with a $100\times$ objective lens (NA=0.9). The penetration depth of the 442 nm laser is approximately 200 nm into Si in this case. The confocal hole size and the exposure time of each Raman acquisition were

set as 50 μm and 5 sec with twice measurements, respectively. In previous studies [62], the effects of laser power on the full-width at half-maximum (FWHM) and the signal-to-noise ratio were measured in order to determine the optimum laser power for the Raman measurements. In particular, for stress measurements it is important to reduce the input laser power by filters to a level such that the heating of the Si (which causes Si Raman peak shift and broadening) is below the detection limit. The suitable laser power density was reported to be $\sim 2 \text{ mW}/\mu\text{m}^2$ [62]. In this work, D0.6 filter was chosen to reduce the original laser power ($\sim 2 \text{ mW}/\mu\text{m}^2$) by $10^{0.6}$ (i.e. around four times). The filtered laser power on the sample surface was therefore less than $1 \text{ mW}/\mu\text{m}^2$, so that the heating effect induced by the laser power is negligible and excluded [59]. Fig. 2.2 (a) is a representative Raman spectrum of silicon at RT which shows a full-width at half-maximum (FWHM) of 3.0 cm^{-1} and a signal-to-noise ratio of 100 approximately.

Both one-dimensional (1-D) line scan and 2-D mapping were performed to analyze the stress distribution in Si around the Cu TSVs. Typically, channel directions in transistors belong to the $\langle 110 \rangle$ direction family. Therefore, the line scan measurements were performed along $[110]$ and $[100]$ directions for comparison on the (001) Si wafer with a fixed step size.

To compare different measurements, we need to determine the Si/TSV interface so that stress distribution from different TSVs can be aligned. As metals are highly reflective, input photons can barely be absorbed or participate in the Raman scattering processes. Therefore, metals don't produce any Raman signals. Our laser spot has a diameter of 0.8 micron. When the laser spot center is at the Si/TSV interface, half of the area is on Cu or TSV liner, and the position at 50% of the intensity drop was defined as the Si/TSV interface in this work. Fig. 2.2 (b) shows the measured Raman intensity and frequency for Si around a 10- μm -diameter Cu TSV obtained by a line scan at RT along the $[110]$ direction. Close to the Si/TSV interface, the

intensity of the Raman signal drops gradually from 30000 to 0 counts approximately. 50% of the intensity drop was defined as the locations of the Si/TSV interface in this work.

Figure 2.2 (a) A representative Raman spectrum of silicon at RT, (b) measured Raman intensity and frequency for Si around a 10- μm -diameter Cu TSV along the [110] direction.

To extract the stresses from the Si Raman shift, the change of the Si-Si Raman vibration peak position due to stress $\Delta\omega$ can be calculated by

$$\Delta\omega(T) = \omega_s(T) - \omega_0(T), \quad (2.20)$$

where ω_s is the Si-Si peak position under stress at temperature T , and ω_0 is the reference Si-Si peak position of stress-free Si at the same temperature.

The measured Si Raman peaks were fitted by Lorentzian fitting to determine the peak positions with a resolution of $\pm 0.03 \text{ cm}^{-1}$. Then, the sum of the radial stress σ_r and the circumferential stress σ_θ can be calculated from a linear relationship between $\Delta\omega$ and $\sigma_r + \sigma_\theta$ according to the equation (2.19):

$$\sigma_r + \sigma_\theta \text{ (MPa)} = -470\Delta\omega \text{ (cm}^{-1}\text{)}. \quad (2.21)$$

Strictly speaking, the equation above works only at room temperature. Considering that the Young's modulus of silicon changes with temperature, the proportionality factor 470 between the Raman shift and the stress sum might change correspondingly at elevated temperatures. This issue will be further discussed in the following section. The bottom line is that the change in the proportionality factor in Equation 2.21 is negligible for the temperature range used in this work.

2.1.3 Temperature Effects on The Elasticity of Silicon and Stress Calculation

As seen in Equation 2.18, the proportionality factor between the Si stress and the Si Raman peak shift depends on the elements of Si compliance tensor: S_{11} , S_{12} , and p , q . The compliance tensor is the inverse matrix of the elasticity tensor. Under 1-D tensile test, the elasticity tensor reduces to a scalar, often called the Young's modulus E . As our goal is to investigate the temperature dependence of the proportionality factor between the Si stress and the Si Raman peak shift, it is important to first investigate the Young's modulus E 's temperature dependence.

The corresponding temperature coefficient is called the temperature coefficient of Young's modulus (TCE). As with E , the temperature behavior of elasticity is more properly described by the temperature coefficients of the individual components of the elasticity tensor:

TS_{11} , TS_{12} , etc. Si belongs to the class m3m in point group theory, and it will experience uniform thermal expansion in all directions [63] (2.6 ppm/°C at room temperature [64]) and also a uniform change in elasticity in all directions, at least to first order. Several different measurements of the temperature coefficients of elasticity are reported in the literature [65] [66] [67]. The value of silicon TCE for typical axial loading situations is nearly identical in all crystal orientations and equal to approximately 60 ppm/°C near room temperature. The results given by Bourgeois *et al.* [68] are the most carefully performed experiments that we are aware of, and those values agree with recent experimental results [69]. Note that the temperature coefficients are not simple linear quantities. By using the values from [68], the TCE of silicon in uniaxial-load cases is about 64 ppm/°C at room temperature (25°C) and 75 ppm/°C at 125°C.

In terms of theory, based on the TCE values mentioned above and the elastic compliance of Si at room temperature (i.e. $S_{11} = 7.68 \times 10^{-12} \text{ Pa}^{-1}$, $S_{12} = -2.14 \times 10^{-12} \text{ Pa}^{-1}$ at 25°C), the elastic compliance of Si at 125°C can be calculated as $S_{11} = 7.73 \times 10^{-12} \text{ Pa}^{-1}$, $S_{12} = -2.15 \times 10^{-12} \text{ Pa}^{-1}$, approximately. Insert these values to the equation (2.2.18) with $p = -1.43\omega_0^2$, $q = -1.89\omega_0^2$, $\omega_0 = 520 \text{ cm}^{-1}$ (25°C) and 518 cm^{-1} (125°C) [70], so that the proportionality factor between the Raman shift and the stress sum at two different temperatures can be calculated as approximately -519 (25°C) and -517 (125°C), respectively. Since the change (0.4%) is very small, the proportionality factor between the Raman shift and the stress sum can be treated as a constant through the temperature range of this study. Thus, in this work, the equation (2.2.21) is used to calculate the sum of the stress ($\sigma_r + \sigma_\theta$) both at room temperature and elevated temperatures (up to 100°C). Experimentally, to determine the effective proportionality factor between the Raman shift and the stress sum for the specific experimental conditions, calibration measurements by high-resolution X-ray diffraction (XRD) on an

equibiaxially stressed film system were conducted. The experimental proportionality factor is -470 (25°C) based on the XRD calibration [62].

2.1.4 Plasma Line Calibration and Error Analysis

From Equation 2.21 $\sigma_r + \sigma_\theta$ (MPa) = $-470\Delta\omega$ (cm^{-1}), we can see that a small change in the Raman peak position, say 0.02 cm^{-1} , can be translated to about 10 MPa change in stress. However, not all changes in Raman peaks are due to stress changes. Often, temperature change and equipment vibration can cause Raman peak changes, and we need to find ways to exclude those effects. The determination of the peak position can be improved by using a reference band. Indeed, this will allow one to remove the influence of external parameters such as environmental temperature that can also affect the frequency of the monitored Raman peak. Ideally this reference should be acquired simultaneously with the Raman measurements. This is why the plasma lines from the laser source itself are usually very well suited as they provide sharp emission of well-known frequency that are collinear with the Raman spectra. For example, if Si Raman peak shifts to $\omega_{\text{Si}} 520.4 \text{ cm}^{-1}$ as supposed to 520.7 cm^{-1} for stress-free Si at RT, we need to refer this Si peak to the plasma line frequency ω_{PL} at 283.17 cm^{-1} . If ω_{PL} stays the same, then $\Delta\omega_{\text{Si}} - \Delta\omega_{\text{PL}} = \Delta\omega_{\text{Si}}$ is real. If ω_{PL} changes at the same time, it indicates that some environment factors changes the plasma line and the Si peak frequencies, and $\Delta\omega_{\text{Si}}$ should be corrected to $\Delta\omega_{\text{Si,corrected}} = \Delta\omega_{\text{Si}} - \Delta\omega_{\text{PL}}$.

Unfiltered radiation from the source HeCd laser contains numerous plasma lines that have intensities which are competitive with the intensities of the bands in Raman spectra. Commonly, interference filters are used in order to prevent mistaken assignments and so to isolate desired Raman lines. After removing the filter, plasma lines will appear in Raman spectra.

Although the plasma lines are normally regarded as a nuisance, they are potentially useful for calibrating spectrometers if the positions of the plasma lines have been recognized and differentiate from the measured Raman peaks of the sample. Since the plasma lines are from the emission of the ion laser itself, they are independent on the testing samples. Thus, the plasma emission lines from the ion laser can be treated as an internal standard during the measurements through monitoring the shifts caused by the thermal and mechanical vibrations of the spectrometer.

The wavenumbers of the plasma lines can be calculated from the corresponding wavelengths based on the He-ion emission spectrum. Table 2.1 shows some of the calculated plasma lines of the He-ion laser. The calculated plasma lines agree with the measured plasma lines in our experiment, as shown in Fig. 2.3 with blue arrows. Due to the individual difference of each laser, the measured positions of the plasma lines have some variations, compared with the calculated values. For this work, as Si peak is around 520 cm^{-1} , the most convenient plasma line to use is the one at 283 cm^{-1} , such that both the Si peak and the reference plasma line can be obtained in one scan.

Table 2.1 Calculated and measured plasma lines of the He-ion laser. Kimmon is the laser vendor of the Raman spectroscopy of this work.

Ref. [71]	Plasma lines in <i>nm</i>	Calculated plasma lines in <i>cm</i>⁻¹	Measured plasma lines in <i>cm</i>⁻¹
NIST	447.15	282.86	283.17
Kimmon	501.00	2686.75	2709.09
Kimmon	508.00	2961.79	2983.82
Kimmon	534.00	3920.24	3911.15
Kimmon	538.00	4059.47	4052.60
NIST	587.56	5627.33	5627.37

Figure 2.3 Measured plasma lines of the He-ion laser from the laser source of this work.

In this work, the main sources of errors are from the peak fitting and the thermal and mechanical vibrations of the spectrometer. As mentioned in Section 2.1.2, Lorentzian fitting of the peak position has a resolution of $\pm 0.03 \text{ cm}^{-1}$. The shifts caused by the thermal and mechanical vibrations of the spectrometer during the measurements were monitored by a reference plasma line. For example, when we were doing 1-D line scan, both the Si peak of the TSV sample and the laser plasma line were measured at the same time and shown in the spectrum as Fig. 2.4. During the whole scanning process, the plasma line position was

monitored all along to make sure there were no large variations of the shifts ($> 0.1 \text{ cm}^{-1}$) due to the thermal and mechanical vibrations of the spectrometer. As shown in Fig. 2.5, the plasma line positions during the line scan are basically stable with only a slight variation ($\sim 0.03 \text{ cm}^{-1}$) which is within the error range of the peak fitting.

Figure 2.4 Measured silicon Raman peak and the reference plasma line.

Figure 2.5 Measured plasma line positions during 1-D line scan.

On the other hand, the measurement errors can be seen in the regions far away from the TSVs, where the stress ($\sigma_r + \sigma_\theta$) should approach zero. Raman peak positions of the zero-stress reference points were also carefully monitored for each scan or mapping. In general, the error bar of the Raman measurements in this work is estimated to be equal to the fitting error $\pm 0.03 \text{ cm}^{-1}$, which translates to around $\pm 15 \text{ MPa}$ for the stress ($\sigma_r + \sigma_\theta$).

2.2 Stress Characterization for Batch 1 Cu TSVs

2.2.1 Batch 1 Cu TSV Structures and Fabrication Process

In this work, Cu filled TSV arrays were fabricated on 8-inch p-type Si (001) wafers with a 1.28- μm -thick top SiO_2 layer. The wafer resistivity ranges from 6 to 9 $\Omega\cdot\text{cm}$. Fig. 2.6 (a) shows the schematic diagram of the cross-section of TSVs after the fabrication process. The diameter (Φ) of the TSVs varied from 5 to 10 μm with a fixed depth of 10 μm . The pitch was set at three times the corresponding TSV diameter (i.e., for $\Phi=10\text{ }\mu\text{m}$, pitch=30 μm). The dielectric liner is a conventional plasma-enhanced tetraethyl orthosilicate (PETEOS) liner about 200 nm thick. It was deposited in a plasma-enhanced chemical vapor deposition (PECVD) chamber at temperature $< 400^\circ\text{C}$ using a tetraethyl orthosilicate (TEOS) precursor. A tantalum (Ta) barrier and a Cu seed were sputtered and followed by a super-conformal Cu electroplating (ECP) step to fill the TSV holes completely. After annealing (200 $^\circ\text{C}$, 30 min in N_2 ambient), the Cu overburden was then removed by chemical mechanical polishing (CMP). During the cooling process to room temperature, Cu TSVs shrank faster than silicon due to its relatively larger CTE, inducing a tensile radial stress and a compressive circumferential stress in the nearby silicon.

The detailed fabrication process steps have been reported by Zhang *et al* [72]. Fig. 2.6 (b) represents the optical microscopy plan view of the TSV arrays ($\Phi=10\text{ }\mu\text{m}$) after the CMP step. Fig. 2.6 (c) shows the focused ion beam (FIB) cross-sectional image of the Cu-filled TSV with PETEOS liner. The image reveals that conformal coverage of both liner material and void-free Cu filling were achieved. There are no observable signs of interfacial delamination or Cu debris in the Cu TSV structures. Thus, these samples are suitable for thermo-mechanical stress study.

Figure 2.6 (a) Schematic diagram of the cross-section of TSVs after fabrication, (b) optical microscopic view of the TSV array ($\Phi=10\ \mu\text{m}$) after the CMP step and no signs of Cu debris are found, (c) cross-sectional image of a Cu TSV of about 5 μm in diameter and 10 μm in depth. Figure courtesy of Chuan Seng Tan at Nanyang Technological University, Singapore.

2.2.2 1-D Line Scan and 2-D Mapping Conditions

Both one-dimensional (1-D) line scan and 2-D mapping were performed to analyze the stress distribution in Si around the Cu TSVs. Typically, channel directions in transistors belong to the $\langle 110 \rangle$ direction family. Therefore, the line scan measurements were performed along $[110]$ and $[100]$ directions for comparison on the (001) Si wafer with a step size of 250 nm.

As discussed in Section 1.2, temperature-dependent stress measurements provide a useful tool to understand the origin of the stresses, and it also provides useful information of the stress level under circuit operation temperature. Here we use 1-D line scan and 2-D mapping with a heating stage to study the stress distributions in Si around Cu TSVs at the elevated temperatures.

A Linkam PE120-XY heating stage was mounted on the motorized XY stage of the Raman microscope to heat the TSV samples during the Raman measurements. Four temperatures, 23 (RT), 50, 75 and 100 °C were used in this study. Both 8 μm and 10 μm diameters TSVs have been tested by the line scans. The 2-D mapping measurements were set to map a square area ($32 \times 32 \mu\text{m}^2$) with one TSV ($\Phi=10 \mu\text{m}$) inside. For 2-D mapping, the step size is 1 μm in order to be time-efficient, and the mapping was also performed at 23 (RT), 50, 75 and 100 °C. Fig. 2.7 (a) and (b) show the detailed line scan and 2-D mapping ranges, and the coordinate system used.

Figure 2.7 (a) 1D line scan ranges, (b) 2D mapping area for TSV arrays with $\Phi=10\ \mu\text{m}$, and pitch= $30\ \mu\text{m}$ and (c) the coordinate system used and key crystal directions.

2.2.3 1-D Line Scan Results

The temperature-dependent near-surface Si $\sigma_r + \sigma_\theta$ distribution in the close vicinity of TSVs from Raman measurements is shown in Fig. 2.8 (a)-(c). It was observed that the near-surface stress in Si surrounding the Cu TSV decreased substantially when temperature increased from 23 (RT) to 100°C . This is expected, as Cu was annealed at 200°C for 30 min, where Cu grain growth happened and the Cu grains after the growth were almost stress-free. The annealing temperature is therefore the stress-free reference temperature. During the cooling process to RT, Cu TSVs shrank faster than silicon due to its relatively larger CTE, inducing a tensile radial stress σ_r and a compressive circumferential stress σ_θ in the nearby silicon. Raising the temperature towards the reference temperature will reduce the thermal stresses.

Figure 2.8 $\sigma_r + \sigma_\theta$ distribution as a function of distance at four different temperatures (23 (RT), 50, 75 and 100°C): (a) from the 10- μm -diameter TSV edge, along the [110] direction; (b) from the 10- μm -diameter TSV edge, along the [100] direction (c) from the 8- μm -diameter TSV edge, along the [110] direction.

In the immediate vicinity of the Si/TSV liner interface, $\sigma_r + \sigma_\theta$ is compressive. Along the [110] direction, it decreased from 219 MPa at 23°C to 80 MPa at 100°C for Si around a 10- μm -diameter TSV. A similar trend was also observed in Si around an 8- μm -diameter TSV. As

there is less Cu volume in smaller Cu TSVs, the stresses are expected to be smaller. As Si is an anisotropic material, the stress along the [100] is different from that along the [110] direction, and is observed to be less than along the [110] direction as shown in Fig. 2.8 (b). In the $\sigma_r + \sigma_\theta$ profiles, tensile stress peaks exist at about 2 μm away from the TSV liner/Si interface, which are likely from the pre-existing stresses before Cu filling as discussed in Chapter 3. $\sigma_r + \sigma_\theta$ approaches zero when the distance is further than a few microns away from the interface.

2.2.4 2-D Mapping Results

Fig. 2.9 illustrates the $\sigma_r + \sigma_\theta$ distribution for the same 10- μm -diameter TSV within a square area ($32 \times 32 \mu\text{m}^2$) at four different temperatures (23 (RT), 50, 75 and 100°C, respectively) by 2-D Raman mapping. The crystal symmetry and some process non-uniformity can be seen. It reveals that the region of the compressive stress (i.e. the blue region) narrowed down when temperature increased, indicating a decrease of the compressive stress in Si surrounding the Cu TSV, which is in agreement with the 1-D scan results.

Figure 2.9 2-D $\sigma_r + \sigma_\theta$ distribution for Si around a 10- μm -diameter TSV at four different temperatures (23 (RT), 50, 75 and 100 °C).

One of the major contributions of this work is that we revealed that the pre-existing stress before Cu deposition plays a key role in the near-TSV stress fields besides the CTE-mismatch stresses, which was not discussed in prior-art (more details are discussed in Chapter 3). The pre-existing stresses are dependent on the process conditions. To explore the process dependence, two other TSV structures with different processing conditions were studied and discussed below.

2.3 Measurements of Batch 2 40- μm -diameter Cu TSV Structures

Compared with the 10- μm -diameter Batch 1 Cu TSV sample, 40- μm -diameter Cu TSV arrays were fabricated on another 8-inch Si (001) wafer with some differences in the process, which is referred as Batch 2 Cu TSVs. The original wafer had a thickness of 750 μm and 1- μm -thick top SiO_2 layer. The diameter (Φ) of the TSVs was fixed at 40 μm with a depth of 60 μm . The pitch varied from two to three times the TSV diameter (i.e., from 80 to 120 μm). The dielectric liner is a deposited SiO_2 liner but the thickness increased to 1 μm compared to the 0.2 μm liner of the TSVs discussed earlier. The tantalum (Ta) barrier and the Cu seed were sputtered

and followed by a super-conformal Cu electroplating (ECP) step to fill the TSV holes completely. After TSV metallization, top metal (1000Å Ti/2000Å Au) layers were sputtered on the wafer surface. The annealing temperature was 300°C 60 min, in N₂ ambient. After the annealing process, both the top metal (1000Å Ti/2000Å Au) and the top oxide layers were removed by chemical mechanical polishing (CMP). The wafer was then thinned down to 100 μm. Fig. 2.10 (a) and (b) illustrate the schematic diagrams of the cross-sections of a 40-μm-diameter Cu TSV after the top metal sputtering and the CMP step, respectively. Fig. 2.10 (c) shows the optical microscopy plan view of the TSV arrays after the fabrication process. The sample shows no observable signs of interfacial delamination or Cu debris in the Cu TSV structures. Thus, it is suitable for thermo-mechanical stress study using Raman spectroscopy.

(a)

(b)

(c)

Figure 2.10 Schematic diagrams of the cross-section of a 40-μm-diameter Cu TSV: (a) after the top metal sputtering and (b) after the CMP step, (c) optical microscopic view of the TSV array (pitch=120 μm) after the fabrication process.

Here, the line scan conditions along the [110] direction were set the same as those for the 10-μm-diameter Cu TSV sample, except the scanning range was increased to 30 μm and the step size was adjusted to 1 μm. The temperature-dependent near-surface Si $\sigma_r + \sigma_\theta$ distribution along the [110] direction in the close vicinity of 40-μm-diameter Cu TSVs from Raman measurements is shown in Fig. 2.11. Compared with the results of the 10-μm-diameter, the compressive near-surface stress $\sigma_r + \sigma_\theta$ in Si surrounding the 40-μm-diameter Cu TSVs decreases similarly when temperature increased from 23 (RT) to 100 °C. Along the [110] direction in the immediate vicinity of the Si/TSV liner interface, it decreased from 384 MPa at 23 °C to 199 MPa at 100 °C. As there is much more Cu volume than the 10-μm-diameter Cu TSVs, the stresses in the 40-μm-diameter Cu TSV sample are expected to be much larger. The difference is the tensile stress profiles. In the $\sigma_r + \sigma_\theta$ profiles for the 40-μm-diameter Cu TSV sample, there are no significant peaks of tensile stress compared with the 10-μm-diameter Cu TSV sample. The tensile stress profiles for the 40-μm-diameter Cu TSV sample show quite flat as the distance increases from

TSV edge, and have an observable decrease when temperature increased from 23 (RT) to 100 °C. This means that the pre-existing stress which may exist in the 40- μm -diameter Cu TSV sample is completely different from that in the 10- μm -diameter because of the different fabrication process. The certain value of the pre-existing stress in the 40- μm -diameter Cu TSV sample will be further discussed in Chapter 3.

Figure 2.11 $\sigma_r + \sigma_\theta$ distribution as a function of distance at four different temperatures (23 (RT), 50, 75 and 100 °C) from the 40- μm -diameter TSV edge, along the [110] direction.

2.4 Carbon Nanotube (CNT) Filled TSV Structures

Besides Cu, carbon nanotubes (CNTs) are another type of TSV filling material due to their high thermal conductivity. Table 2.2 shows the comparison of typical physical properties between Si, Cu and carbon nanotube (CNT). From the comparison, we can see that CNT is chosen to be an alternative via-filling material in TSV structures due to its superior thermal

conductivity (k) and low electrical resistivity (ρ). Literature reports that even air-filled CNT bundles show both conductivities to be 1.4x to 5.7x higher than Cu [73]. Due to the negative axial CTE, it is expected that CNT should have different thermomechanical behaviours during the thermal process compared with Cu, which may overcome the reliability problems such as via extrusion and interfacial delamination caused by Cu TSVs.

Table 2.2 Typical physical properties of Si, Cu and CNT at RT [74].

Material	Young Modulus (GPa)	Poisson's Ratio	Thermal Conductivity (W/mK)	Electrical Resistivity ($\Omega \cdot m$)	CTE ($10^{-6}/K$)
Silicon (Si)	169 along $\langle 110 \rangle$ 130 along $\langle 100 \rangle$ (anisotropic)	0.064 along $\langle 110 \rangle$ 0.28 along $\langle 100 \rangle$ (anisotropic)	149	1×10^{-1} to $4 \times 10^{-6}^*$	2.3
Copper (Cu)	128	0.34	385	1.68×10^{-8}	16.4
Carbon Nanotube (CNT)	1300	0.0344	3500	0.29×10^{-8} to 1.2×10^{-8} [73]	Axial: -0.6^{**} Transv.: 6.6 **
* The resistivity of silicon depends strongly on the presence of impurities in the material					
**CNT CTE is an average value as there is a range found in the literature					

In this section, CNT-filled TSVs and control samples which have void vias without CNT filling were fabricated and conducted by Raman measurements to investigate the near-surface stress distributions. The comparison between void vias and filled vias gives us an opportunity to prove our hypothesis on the “pre-exisitng” stress.

In this work, CNT-filled TSVs and void vias were fabricated in separated regions on 8-inch Si (001) wafers with a $\sim 1\text{ }\mu\text{m}$ top SiO_2 layer. The average diameter (Φ) of the TSVs is $12\text{ }\mu\text{m}$ with a fixed depth-to-diameter aspect ratio ($\text{AR}=8$). The average pitch is $24\text{ }\mu\text{m}$. After the same process of via etching and dielectric liner deposition, high-density carbon nanotubes were filled into the TSV holes for the CNT-filled sample through two thermal steps: 1) an annealing before CNT growth at 450°C for 10 min in H_2 flow for CNT catalyst activation and 2) the CNT growth at 550°C for 30 min under $\text{H}_2/\text{C}_2\text{H}_2$ flow. After the CNT growth, the TSV holes were filled by carbon nanotubes completely as shown in Fig. 2.12 (a). We can assume that at the growth temperature, the newly grown CNTs are stress-free. Fig. 2.12 (b) shows a cross-sectional image of the CNT-filled TSVs and some process non-uniformity can be seen. CNT protrusions and the roughness of top-surface due to scattered carbon nanotubes on the wafer were then smoothed out by a CMP process. After the CMP, the schematic of the cross-section is the same as the Cu TSV in Fig. 2.6 (a), except that the filling material is CNT. On the contrary, the control sample is completely absent for these steps. Fig. 2.12 (c) shows the optical microscopy plan view of void vias and CNT-filled TSVs after the fabrication process.

(a)

(b)

(c)

Figure 2.12 (a) SEM top view of a CNT-filled TSV, (b) cross-sectional image of the CNT-filled TSVs, (c) optical microscopic view of void vias and CNT-filled TSVs after the fabrication process. Images courtesy of Dr. Kaushik Ghosh at Nanyang Technological University, Singapore.

The Raman line scan conditions along the [110] direction for the void vias and the CNT-filled samples at four temperatures, 23 (RT), 50, 75 and 100 $^{\circ}\text{C}$, were set the same as those for the

10- μm -diameter Cu TSV sample. The scanning distance is 10 μm , and the scanning path is shown in Fig. 2.13.

Fig. 2.14 (a) shows the comparison of stress distributions between the void vias and the CNT-filled samples at RT. Compared to a TSV with CNT filling, the difference in the stress curves is within measurement error bar, indicating the pre-existing residual stress is dominant in the CNT-filled sample. These measurements prove our hypothesis that the processing history before via filling can induce a pre-existing residual stress in Si around the TSVs and it may be relevant to the thermal process of the dielectric liner in the vias.

The processing differences between these two structures are 450 $^{\circ}\text{C}$ catalyst activation, 550 $^{\circ}\text{C}$ CNT growth, and CMP. During the CNT growth, the newly grown CNT should be stress free. After the cooling step, the Si stress is almost back to the pre-existing stress. There are two possible explanations for this phenomenon: 1) the CTE of CNT filling is very close to Si; 2) there is a weakly bounded interface or air gaps between the CNT filling and the TSV liner, which means that when the CNTs shrank during cooling, they didn't drag the surrounding Si. Explanation 1 is not likely as CNT and Si have quite different CTE, as shown in Table 2.4.1.

Next, we heated the samples up, and the near-surface Si $\sigma_r + \sigma_{\theta}$ distributions at elevated temperatures are shown as Fig. 2.14 (b) and (c), respectively. The difference for different temperatures is (~ 15 MPa) within the error bar of the measurements. Fig. 2.14 (c) shows that within experimental errors, the stress distribution of the CNT-filled sample did not change much with the temperature increase, indicating that the thermal stress induced by the CNT-filled TSV is negligible. This observation is consistent with the explanation 1 and 2 as well.

Figure 2.13 1D line scan ranges for CNT-filled TSVs and void vias (avg. $\Phi=12\text{ }\mu\text{m}$ and pitch= $24\text{ }\mu\text{m}$).

Figure 2.14 $\sigma_r + \sigma_\theta$ distribution as a function of distance at four different temperatures (23 (RT), 50, 75 and 100°C): (a) the stress comparison between the void vias and the CNT-filled TSVs at RT, (b) for the void vias, and (c) for the CNT-filled TSVs.

2.5 Summary

Micro-Raman spectroscopy has been employed to study the near-surface stress distributions and origins in Si around TSVs at elevated temperatures. The results show that a temperature rise towards the annealing temperature of a TSV will reduce the near-surface compressive stresses around Cu TSVs. For CNT-filled TSVs, the stress distribution doesn't change much with temperature, and it is very similar to the stress distribution before CNT filling.

From these observations, we propose that the stresses near TSVs are likely from two sources: 1) pre-existing stress before via filling, and 2) coefficients of thermal expansion (CTE) mismatch-induced stress. The pre-existing stress in TSV structures is dependent on process conditions. To understand the process dependence of the stress fields near TSVs, various TSV structures and materials are evaluated. With these experimental data, we are ready for finite element analysis and in-depth discussion on the origins of the stresses.

Chapter 3 Stress Modeling and Estimation of Mobility Variation

Combined with finite element analysis, the CTE mismatch-induced stresses and the possible pre-existing stresses in the TSV structures can be evaluated, which are discussed in this chapter.

3.1 Stress Modeling and Simulations

3.1.1 Finite Element Analysis (FEA)

3-D finite element analysis (FEA) was conducted to simulate the stress distributions in Si around TSVs using a widely used commercial software package, COMSOL (v4.3b). A batch one 10- μm -diameter Cu TSV was simulated first. The structure for simulations consisted of a 10- μm -diameter Cu TSV with a depth of 10 μm in a (001) Si substrate. Due to the axis symmetry nature of the model, only a quarter of the TSV and the surrounding Si needs to be simulated (as shown in Fig. 3.1). The conformal top oxide layer (1 μm), oxide liner (0.2 μm) and Cu filling in the TSV were also taken into account. The tantalum diffusion barrier layer is 20 nm thick, and can be neglected in the stress simulations [75]. The material properties used in the simulations (as shown in Table 3.1) were set the same as those reported by Tsai et al [75]. For silicon, anisotropic modulus and Poisson's ratio were used. The reference temperature used was the annealing temperature 200°C, at which the structure was assumed to be stress-free.

Stress changes during a thermal load, i.e. cooling from the reference temperature to the measurement temperature (23 (RT), 50, 75 and 100°C), were calculated. As a result of cooling, Cu cores contract more than Si due to the larger CTE of Cu. Since Cu was confined in the TSVs,

thermo-mechanical stresses were then induced and exerted on the surrounding oxide liner and Si. The radial stress σ_r in Si is tensile, and the circumferential stress σ_θ is compressive. The stresses, such as σ_r , σ_θ , σ_x , σ_y , σ_z and the sum of the in-plane stress terms, i.e. $\sigma_r + \sigma_\theta$, in Si substrate can be obtained from the simulation results.

Figure 3.1 3-D FEA model for the 10- μ m-diameter TSV showing a quarter of the Cu via (orange) embedded in Si (blue) along with a top oxide layer (gray) and a thin oxide liner (gray) at the Cu/Si interface.

Table 3.1 Physical properties of materials in TSV.

Material	Young's modulus (GPa)	Poisson ratio	Density (kg/m^3)	CTE (ppm/ $^{\circ}C$)
Silicon	169 along $\langle 110 \rangle$ 130 along $\langle 100 \rangle$ (anisotropic)	0.064 along $\langle 110 \rangle$ 0.28 along $\langle 100 \rangle$ (anisotropic)	2329	2.3
Copper	110	0.35	8960	17
PETEOS liner	72	0.16	2200	0.5

3.1.2 Comparison between Raman and FEA results

Fig. 3.2 shows the simulation results of $\sigma_r + \sigma_\theta$ in comparison with experiment results at the laser penetration depth (0.2 μm) for a 10- μm -diameter TSV along [110] direction at different temperatures (23 (RT), 50, 75 and 100°C). Compared with the Raman stress measurement results under the same temperature (same data as in Fig. 2.8 (a)), the FEA results present a similar temperature dependence, which is that the compressive stress $\sigma_r + \sigma_\theta$ close to the TSV decreases as the temperature increases. At the immediate vicinity of the Si/TSV liner interface, the simulated compressive stress along the [110] direction decreased from 245 MPa at 23°C to 78 MPa at 100°C (i.e. 68% reduction). The simulation results do not agree with the measurement data in $1\ \mu\text{m} < x < 5\ \mu\text{m}$ region, where the Raman measurements show tensile stress peaks around 30 MPa at 23°C and increasing to around 60 MPa at 100°C. Similar tensile stress peaks were reported in previous studies [62], but no explanation was given.

Figure 3.2 FEA simulation and experiment results of $\sigma_r + \sigma_\theta$ as a function of distance from the 10- μm -diameter Cu TSV edge along the [110] direction at different temperatures (23 (RT), 50, 75 and 100°C).

A reasonable explanation we propose here is the pre-existing residual stress which has been induced in Si around the TSVs before Cu filling. Fig. 3.3 (a) shows the differential values between experiment and simulation results of $\sigma_r + \sigma_\theta$ at different temperatures (23 (RT), 50, 75 and 100°C). From this figure, we can see that within experimental errors, the differences between the measured stress and the simulated stress did not change with temperature, indicating that the pre-existing residual stress is not sensitive to a temperature change in this range. This stress component is significant for the $x < 5 \mu\text{m}$ region, and is negligible (less than 10 MPa) for the $x > 5 \mu\text{m}$ region. We suspect that it depends on the processing history before Cu filling, which was confirmed in section 3.1.3. This pre-existing residual stress may be from the liner deposition step. Once this component is taken into account, the simulation results match experiment results very

well (shown in Fig. 3.3 (b)). This agreement verifies the models and material parameters used in the simulations.

Figure 3.3 (a) The differential values between the experiment data and simulation results of $\sigma_r + \sigma_\theta$ at 23 (RT), 50, 75 and 100 °C showing the pre-existing stress component, (b) the sum of the pre-existing stress (the average value) and the simulated CTE-mismatch-induced stress in comparison with the measured $\sigma_r + \sigma_\theta$ at 23 (RT), 50, 75 and 100 °C.

Fig. 3.4 illustrates the simulated 2-D $\sigma_r + \sigma_\theta$ distribution in an area of $25 \times 25 \mu\text{m}^2$ with a quarter of the 10- μm -diameter TSV inside at four temperatures, 23 (RT), 50, 75 and 100°C , which is also calculated at the laser penetration depth ($0.2 \mu\text{m}$). It shows a reduction of the blue region with the increase of temperature indicating a decrease in the compressive $\sigma_r + \sigma_\theta$ stress in Si, which is consistent with the 2-D Raman mapping results in Fig. 2.9.

Figure 3.4 FEA simulation results of 2-D $\sigma_r + \sigma_\theta$ distribution for Si and a quarter of 10- μm -diameter Cu TSV at four temperatures (23 (RT), 50, 75 and 100°C).

3.1.3 Simulations for Batch 2 Cu TSV Structures

The stress distributions in Si around TSVs for 40- μm -diameter Cu TSV structures were also simulated by 3-D finite element analysis (FEA). The model for simulations consisted of a 40- μm -diameter Cu TSV with a depth of 60 μm in a (001) Si substrate. Only a quarter of the TSV and the surrounding Si was simulated due to the axis symmetry nature of the model, as shown in Fig. 3.5. Compared with the 10- μm -diameter TSV model, the thickness of oxide liner was changed to 1 μm and there was no top oxide layer for the 40- μm -diameter TSV model. Same material physical properties were used in the simulations as shown in Table 3.1. Also, the anisotropic modulus and Poisson's ratio for silicon were taken into account. The reference temperature was set the same as the annealing temperature 300°C, at which the structure was assumed to be stress-free. A thermal load, i.e. cooling from the reference temperature to the measurement temperature (23 (RT), 50, 75 and 100°C), was simulated.

Figure 3.5 3-D FEA model for the 40- μm -diameter TSV showing a quarter of the Cu via (orange) embedded in Si (blue) along with a thin oxide liner (gray) at the Cu/Si interface.

Fig. 3.6 shows the simulation results of $\sigma_r + \sigma_\theta$ in comparison with experiment results at the laser penetration depth (0.2 μm) for a 40- μm -diameter TSV along [110] direction at different temperatures (23 (RT), 50, 75 and 100 $^\circ\text{C}$). Compared with the Raman results under the same conditions (same data shown as in Fig. 2.11), the FEA results present a similar temperature dependence, which is that both the compressive and the tensile stress $\sigma_r + \sigma_\theta$ decreases as the temperature increases. At the immediate vicinity of the Si/TSV liner interface, the simulated compressive stress along the [110] direction decreased from 372 MPa at 23 $^\circ\text{C}$ to 190 MPa at 100 $^\circ\text{C}$. The simulation results do not agree with the measurement data in $5 < x < 20 \mu\text{m}$ region, where the simulations show tensile stress peaks around 115 MPa at 23 $^\circ\text{C}$ and decreasing to around 83 MPa at 100 $^\circ\text{C}$ while the Raman results don't show such tensile stress peaks.

Figure 3.6 FEA simulation and experiment results of $\sigma_r + \sigma_\theta$ as a function of distance from the 40- μm -diameter TSV edge along the [110] direction at different temperatures (23 (RT), 50, 75 and 100 $^\circ\text{C}$).

Fig. 3.7 (a) shows the differential values between experiment and simulation results of $\sigma_r + \sigma_\theta$ at different temperatures (23 (RT), 50, 75 and 100°C). From this figure, we can see that within experimental errors, the differential values of stress did not change with temperature, indicating that the pre-existing residual stress is not sensitive to a temperature change in this range. This stress component is significant for the $x < 20 \mu\text{m}$ region, and is negligible (less than 15 MPa) for the $x > 20 \mu\text{m}$ region. Compared with the 10- μm -diameter Cu TSV sample, the pre-existing residual stress in the 40- μm -diameter Cu TSV sample is quite different, which is compressive and smaller. This proves that the pre-existing residual stress depends on the processing history. We suspect there are probably some differences in the detailed steps during the liner deposition leading to the difference in pre-existing stresses between the 10- μm -diameter and 40- μm -diameter Cu TSVs. Again, once the pre-existing stress component is taken into account, the simulation results match experiment results very well (shown in Fig. 3.7 (b)).

Figure 3.7 (a) The differential values between the experiment data and simulation results of $\sigma_r + \sigma_\theta$ at 23 (RT), 50, 75 and 100 °C for the 40- μm -diameter TSV, **(b)** the sum of the pre-existing stress (the average value) and the simulated CTE-mismatch-induced stress in comparison with the measured $\sigma_r + \sigma_\theta$ at 23 (RT), 50, 75 and 100 °C.

3.2 Mobility Change and KOZ Calculation

Stress impacts on carrier mobility in Si have been well studied [76]. In 3-D integration of integrated circuits, stress around TSVs can change carrier mobility and thus transistor performance. 30% shift in the saturation drain current (I_{DSAT}) of nearby transistors has been reported due to TSV induced thermal stresses [77]. This stress-induced performance variability is generally not desired, and a keep-out zone (KOZ) is commonly used in IC layout design to define an area surrounding a TSV where logic cells should not be placed for this consideration.

From the measurement results and discussions above, we can see that the pre-existing stress has a big impact on stress in $x < 5 \mu\text{m}$ range for batch 1 Cu TSVs. The sum of the pre-existing stress and the simulated CTE-mismatch-induced stress can fit the experiment data quite well as shown in Fig. 3.3 (b). It is therefore important to investigate how KOZ is influenced by these two different kinds of stresses. As pre-existing stresses are specific to process details and should be minimized to reduce KOZ, here we discuss the impact of the CTE-mismatch-induced stress on KOZ calculation first, assuming there is zero pre-existing stress.

3.2.1 Calculation Methods

In a cubic coordinate system, carrier mobility depends on three normal stress components along x, y, and z axis. The switching speeds of n-MOS and p-MOS are proportional to the electron and hole mobility respectively. In this work, the [110] direction was chosen as the x axis. Thus, the mobility change under stress can be calculated using the following equation:

$$-\frac{\Delta\mu_x}{\mu} = \pi_l\sigma_x + \pi_t(\sigma_y + \sigma_z), \quad (3.1)$$

where π_l and π_t are the piezoresistive coefficients. π_l and π_t depend on the current flow

direction, and the values for n-MOS and p-MOS with a channel direction along $\langle 110 \rangle$ direction family are shown in Table 3.2 [75]. It shows that the piezoresistance factor decreases by 20% when the temperature increases from 25°C (RT) to 100°C with the doping concentration below 10^{18} cm^{-3} [78]. This temperature dependence was included in the π_l and π_t values used in the KOZ calculations.

In order to compare our work with literature work, the keep-out zone (KOZ) is defined as the region with more than 10% change in carrier mobility as in Ref. [75].

Table 3.2 Piezoresistive coefficients for n- and p-MOS with channel directions along $\langle 110 \rangle$ [75] [78].

$\times 10^{-4}$ (MPa^{-1})	$\langle 110 \rangle$ direction			
	π_l		π_t	
	25°C (RT)	100°C	25°C (RT)	100°C
n-MOS (p-type Si)	-3.16	-2.53	-1.76	-1.41
p-MOS (n-type Si)	7.18	5.74	-6.63	-5.30

3.2.2 Results and Discussion

Fig. 3.8 shows the calculated contour plots of the carrier mobility change and the size of KOZ when p-MOS and n-MOS channels are along the x axis (i.e. $[110]$ direction) around a 10- μm -diameter TSV. KOZs are outlined by dash lines in the contour plots. The simulated mobility change maps are consistent with previous work [75].

Although the $\sigma_r + \sigma_\theta$ simulations in Fig. 3.4 show the Si lattice symmetry, where the $\sigma_r + \sigma_\theta$ stress along four directions in the $\langle 110 \rangle$ direction family are equivalent, the mobility

change map has no such symmetry. This is due to the fact that $\sigma_r + \sigma_\theta$ is defined in a polar coordinate system, while the mobility change is calculated based on a cubic coordinate system. For example, for a device located on the x axis, $\sigma_r + \sigma_\theta$ is the same as a device located on the y axis, but the σ_x , σ_y , σ_z values are different. The mobility change depends on the distance from the TSV, the crystal direction and the temperature. As expected, the KOZs narrowed down with the increase of temperature. p-MOS is shown to have relatively larger KOZs and more sensitive to the stress than n-MOS.

For circuit designers, it is most convenient to incorporate the TSV related stress effect with a design rule change. If we define that d_{KOZ} is the maximum distance from the KOZ edge to the TSV liner/Si interface, then this can be used as the distance within which no transistors should be laid out. The calculated results of d_{KOZ} with a single 10- μm -diameter TSV for p-MOS and n-MOS at RT and 100°C, respectively, are shown in Table 3.3. These data suggest that KOZ estimation at room temperature is larger than that at operation temperature, and it gives a safe margin during high temperature operation of the IC.

It should be noted that the above mobility change and KOZ calculations are based on CTE-mismatch-stress only without the consideration of the pre-existing stress. For samples, in this study, the pre-existing stress cannot be neglected in the region that is less than 5 μm away from the TSV liner/Si interface. Therefore, d_{KOZ} for p-MOS can be conservatively corrected to 5.2 μm for RT and 5 μm for 100°C. For n-MOS, the CTE-mismatch-stress induced KOZ is very small, and the KOZ is heavily influenced by the pre-existing stress component. Therefore, the origin and the modelling of pre-existing stresses are important in the KOZ determination and should be investigated in the future. The reduction of pre-existing stresses will also help to reduce d_{KOZ} .

Figure 3.8 Contour plots for mobility change and size of KOZ for p-MOS and n-MOS, the channel directions of which are along x axis, i.e. [110] direction.

Table 3.3 Values of calculated d_{KOZ} for n- and p-MOS at RT and 100 C.

d_{KOZ} (μm)	Channel along the x axis, i.e. [110] direction	
	RT	100°C
n-MOS (p-type Si)	0.4	0
p-MOS (n-type Si)	5.2	2.6

3.3 Summary

In this chapter, the characteristics of CTE mismatch-induced stresses in TSV structures were analyzed by FEA calculations. The main focus was on the near-surface stress distributions at elevated temperatures, in a range that most electronic devices operate. Through the differential values between the experimental results and the simulated CTE mismatch-induced stresses, the pre-existing residual stresses in the TSV structures can be evaluated. Stress-induced carrier mobility change and keep-out zone (KOZ) are also calculated for a reliable design.

The work in this Chapter demonstrated an approach in working with stress fields around TSVs. First, pre-existing stresses should be measured before TSV filling. Then, CTE-mismatch stresses can be calculated with FEA simulations. The sum of the two will give the total stress fields. Finally, the stress-induced mobility change and KOZs can be calculated to determine the design rule for circuit designers. For each product, after the process conditions before TSV filling is chosen, this approach is quick and effective in determining the design rule.

Chapter 4 Conclusions and Outlook

4.1 Conclusions

Three-dimensional (3-D) integration has emerged as an effective solution to overcome the wiring limit imposed on device density and performance with continued scaling. Through silicon via (TSV), which provides interconnection between the stacked chips, is essential for the 3-D integration. However, due to the large mismatch of the thermal expansion coefficients (CTEs) between via-filling material (Cu) and Si, thermal stresses induced during processing bring about undesirable mobility shifts in devices and serious reliability problems. In this context, the near-surface stress distributions in TSV structures are studied using both experimental and numerical approaches.

Stress measurements and characterizations by micro-Raman spectroscopy at elevated temperatures are conducted to study the stress evolution and origin in TSV structures. Micro-Raman spectroscopy measures a combination of tensile and compressive near-surface stresses in the Si around TSVs. The results show that a temperature rise towards the annealing temperature of the TSV will reduce the near-surface stresses around the TSV. Temperature dependent measurements reveal that the stresses near TSVs have two components: 1) pre-existing stress before via filling, and 2) coefficients of thermal expansion (CTE) mismatch-induced stress. The pre-existing stress in TSV structures is dependent on process conditions. To further understand the process dependence of the stress fields near TSVs, various TSV structures and materials are evaluated.

The CTE mismatch-induced stress can be modeled by finite element analysis. The results obtained from the micro-Raman measurements are compared with the simulations. In particular, the differential values between the experiment data and simulation results are extracted in order to estimate the pre-existing stresses in the TSV structures. Once the pre-existing stress component is taken into account, a good agreement between the Raman measurement and the finite element calculation is obtained, demonstrating that the models and material parameters used in the simulations are reasonable.

The CTE-mismatch-induced stress resulted mobility change and keep-out zone (KOZ) at elevated temperatures are also estimated. Higher temperatures are shown to reduce the CTE-mismatch-induced stress component, and result in the shrinkage of KOZs in Si. The pre-existing stress is shown to be significant in a region equal or larger than the KOZs induced by CTE-mismatch-induced stress only and should be characterized and considered in the KOZ determination and circuit design.

4.2 Outlook

As an outlook for future work, a few possible studies are suggested in order to have a full understanding of the pre-existing stress in Cu TSV structures. First, a control sample with the oxide liner deposition but without Cu filling can be prepared and measured by micro-Raman spectroscopy. By the stress analysis of the control sample, the pre-existing stress before via filling can be shown directly. Moreover, to explore the origin of the pre-existing stress, the detailed steps of the liner deposition need to be checked. Another control sample type, which has no liner deposition can be prepared and analyzed by micro-Raman spectroscopy. Through the comparison between the no-liner control sample and the previous testing results, the origin of the

pre-existing can be revealed. Moreover, the stress generation during liner deposition and other steps can be modelled by process simulation tools. Eventually, if the pre-existing stresses can be related with the process details, it will benefit the process optimization, circuit design and reliability study significantly.

References

- [1] Schaller, R.R., "Moore's law: past, present and future," *Spectrum, IEEE*, vol. 34, no. 6, pp. 52-59, 1997.
- [2] Havemann, R.H., et al., "High-performance interconnects: an integration overview," *Proceedings of the IEEE*, vol. 89, no. 5, pp. 586 - 601, 2001.
- [3] Li, B., et al., "Reliability challenges for copper interconnects," *Microelectronics Reliability*, vol. 44, no. 3, pp. 365-380, 2004.
- [4] Bohr, M.T., "Interconnect scaling-the real limiter to high performance ULSI," *International Electron Devices Meeting*, pp. 241-244, 1995.
- [5] Ryu, Suk-Kyu, THERMO-MECHANICAL STRESS ANALYSIS AND INTERFACIAL RELIABILITY FOR THROUGH-SILICON VIAS IN THREE-DIMENSIONAL INTERCONNECT STRUCTURES, Ph.D. Dissertation, Texas, Austin: The University of Texas at Austin, 2011.
- [6] Ma, Y.J., et al., "Structural and electronic properties of low dielectric constant fluorinated amorphous carbon films," *Applied Physics Letters*, vol. 72, no. 25, pp. 3353-3355, 1998.
- [7] Treichel, H., et al., "Low dielectric constant materials for interlayer dielectric: (Invited paper)," *Microelectronic Engineering*, vol. 40, no. 1, pp. 1-19, 1998.
- [8] Zhou, H., et al., "Effect of deposition methods on dielectric breakdown strength of PECVD low-k carbon doped silicon dioxide dielectric thin films," *Microelectronics Journal*, vol. 35, no. 7, pp. 571-576, 2004.
- [9] Bomchil, G., A. Halimaoui, and R. Herino, "Porous silicon: The material and its applications in silicon-on-insulator technologies," *Applied Surface Science*, Vols. 41-42, no. 0, pp. 604-613, 1989.
- [10] Gosset, L.G., et al., "Integration of SiOC air gaps in copper interconnects," *Microelectronic Engineering*, vol. 70, no. 2-4, pp. 274-279, 2003.
- [11] Gaillard, F., et al., "Chemical etching solutions for air gap formation using a sacrificial oxide/polymer approach," *Microelectronic Engineering*, vol. 83, no. 11-12, pp. 2309-2313, 2006.
- [12] Noguchi, J., et al., "Process and reliability of air-gap Cu interconnect using 90-nm node technology," *IEEE Transactions on Electron Devices*, vol. 52, no. 3, pp. 352-359, 2005.
- [13] Gu, S.Q., et al., "Stackable memory of 3D chip integration for mobile applications," *IEEE International Electron Devices Meeting*, vol. 33, no. 4, pp. 1-4, 2008.

- [14] Leduc, P., "what is 3d ic integration and what metrology is needed," *Conference on Frontiers of Characterization and Metrology for Nanoelectronics*, March 27-29, 2007.
- [15] Das, S., et al., "Timing, Energy, and Thermal Performance of Three-Dimensional Integrated Circuits," *Proc. Great Lakes Symposium on VLSI*, pp. 338-343, 2004.
- [16] Hofstee, H., "Future Microprocessors and Off-Chip SOP Interconnect," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 2, pp. 301-303, 2004.
- [17] Beyne, E., "The rise of the 3rd dimension for system intergration," *International Interconnect Technology Conference, IITC*, pp. 1-5, 2006.
- [18] Al-Sarawi, S.F., D. Abbott, and P.D. Franzon, "A review of 3-D packaging technology," *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging*, vol. 21, no. 1, pp. 2-14, 1998.
- [19] Karnezos, M., "3D packaging: where all technologies come together," *International Electronics Manufacturing Technology Symposium, IEEE/CPMT/SEMI*, pp. 64-67, 2004.
- [20] Ron Maltiel, "Ron Maltiel: Semiconductor Experts, Witnesses, Consultants and Patent Litigation Support," 2013. [Online]. Available: <http://semiconductorexpert.blogspot.ca/2013/01/tsmc-and-globalfoundries-3-d.html>.
- [21] Puech, M., et al., "Fabrication of 3D packaging TSV using DRIE," *Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS*, pp. 109-114, 2008.
- [22] Pargfrieder, S., et al., "Temporary Bonding and DeBonding Enabling TSV Formation and 3D Integration for Ultra-thin Wafers," *Electronics Packaging Technology Conference, EPTC*, pp. 1301-1305, 2008.
- [23] Fukushima, T., et al., "New Three-Dimensional Integration Technology Based on Reconfigured Wafer-on-Wafer Bonding Technique," *IEEE International Electron Devices Meeting, IEDM*, pp. 985-988, 2007.
- [24] Van Olmen, J., et al., "3D Stacked IC demonstrator using Hybrid Collective Die-to-Wafer bonding with copper Through Silicon Vias (TSV)," *IEEE International Conference on 3D System Integration, 3DIC*, pp. 1-5, 2009.
- [25] Ranganathan, N., et al., "A study of thermo-mechanical stress and its impact on through-silicon vias," *Journal of Micromechanics and Microengineering*, vol. 18, no. 7, p. 13, 2008.
- [26] Pavlidis, V.F. and E.G. Friedman, "Interconnect-Based Design Methodologies for Three-Dimensional Integrated Circuits," *Proceedings of the IEEE*, vol. 97, no. 1, pp. 123-140, 2009.
- [27] Wolf, M.J., et al., "High aspect ratio TSV copper filling with different seed layers," *Electronic*

- Components and Technology Conference, ECTC*, pp. 563-570, 2008.
- [28] Sandireddy, S. and T. Jiang, "Advanced wafer thinning technologies to enable multichip packages," *IEEE Workshop on Microelectronics and Electron Devices, WMED*, pp. 24-27, 2005.
 - [29] Yoon, S.W., et al., "3D TSV processes and its assembly/packaging technology," *IEEE International Conference on 3D System Integration, 3DIC*, pp. 1-5, 2009.
 - [30] Motoyoshi, M., "Through-Silicon Via (TSV)," *Proceedings of the IEEE*, vol. 97, no. 1, pp. 43-48, 2009.
 - [31] Khan, N., et al., "Development of 3-D Silicon Module With TSV for System in Packaging," *IEEE Transactions on Components and Packaging Technologies*, vol. 33, no. 1, pp. 3-9, 2010.
 - [32] Chen, Z., et al., "Thermo-mechanical characterization of copper filled and polymer filled tsvs considering nonlinear material behaviors," *Electronic Components and Technology Conference, ECTC*, pp. 1374-1380, 2009.
 - [33] Chinoy, P.B. and J. Tajadod, "Processing and microwave characterization of multilevel interconnects using benzocyclobutene dielectric," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 16, no. 7, pp. 714-719, 1993.
 - [34] Yannou, J., "3D IC and TSV interconnects 2010," Yole Development , 2010. [Online]. Available: http://www.slideshare.net/Yole_Developpement.
 - [35] Jiang, T., et al. , "Measurement and analysis of thermal stresses in 3D integrated structures containing through-silicon-vias," *Microelectronics Reliability*, vol. 53, no. 1, p. 53–62, 2013.
 - [36] Selvanayagam, C.S., et al., "Nonlinear thermal stress/strain analyses of copper filled TSV (through silicon via) and their flip-chip microbumps," *IEEE Transactions on Advanced Packaging*, vol. 32, no. 4, pp. 720 - 728, 2009.
 - [37] Lu, K.H., et al., "Thermomechanical reliability of 3-D ICs containing through silicon vias," *Electronic Components and Technology Conference, ECTC* , pp. 630 - 634, 2009.
 - [38] Lu, K.H., et al., "Thermal stress induced delamination of through silicon vias in 3-D interconnects," *Electronic Components and Technology Conference, ECTC*, pp. 40 - 45, 2010.
 - [39] Ryu, S.K., et al. , "Impact of near-surface thermal stresses on interfacial reliability of through-silicon vias for 3-D interconnects," *IEEE Transactions on Device and Materials Reliability*, vol. 11, no. 1, pp. 35 - 43, 2011.
 - [40] Thompson, S.E., et al., "Uniaxial-process-induced strained-Si: Extending the CMOS roadmap," *IEEE Transactions on Electron Devices*, vol. 53, no. 5, pp. 1010 - 1020, 2006.

- [41] Karmarkar, A.P., et al., "Performance and reliability analysis of 3D-integration structures employing through silicon via (TSV)," *IEEE International Reliability Physics Symposium*, pp. 682 - 687, 2009.
- [42] Cho, S., "Technical Challenges in TSV Integration," 2011. [Online]. Available: http://www.internationalsematech.com/meetings/archives/symposia/10202/Session%202-3D%20TSV/3D_Samsung.pdf.
- [43] Athikulwongse, K., et al., "Stress-driven 3D-IC placement with TSV keep-out zone and regularity study," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 669 - 674, 2010.
- [44] Wilson, C.J., et al., "Synchrotron measurement of the effect of dielectric porosity and air gaps on the stress in advanced Cu/Low-k interconnects," *IEEE International Interconnect Technology Conference, IITC*, pp. 72 - 74 , 2009.
- [45] Ryu, S.K., et al., "Characterization of thermal stresses in through-silicon vias for three-dimensional interconnects by bending beam technique," *Applied Physics Letters*, vol. 100, no. 4, p. 041901, 2012.
- [46] Kimoto, K., et al., "Measurement of Strain in Locally Oxidized Silicon using Convergent-Beam Electron Diffraction," *Japanese Journal of Applied Physics*, vol. 32, no. 2, p. L211, 1993.
- [47] Kwon, W. S., et al., "Stress evolution in surrounding silicon of Cu-filled through-silicon via undergoing thermal annealing by multiwavelength micro-Raman spectroscopy," *Applied Physics Letters*, vol. 98, no. 23, p. 232106 , 2011.
- [48] Hecker, M., et al., "Analytics and Metrology of Strained Silicon Structures by Raman and Nano-Raman Spectroscopy," *AIP Conf. Proc.*, vol. 931, p. 435–444, 2007.
- [49] Okoro, C., et al., "Extraction of the Appropriate Material Property for Realistic Modeling of Through-Silicon-Vias using μ -Raman Spectroscopy," *IEEE International Interconnect Technology Conference, IITC* , pp. 16 - 18 , 2008.
- [50] McDonough, C., et al., "Thermal and spatial dependence of TSV-induced stress in Si," *IEEE International Interconnect Technology Conference and Materials for Advanced Metallization, IITC/MAM*, pp. 1-3, 2011.
- [51] Ma, Q., et al., "High-resolution determination of the stress in individual interconnect lines and the variation due to electromigration," *Journal of Applied Physics*, vol. 78, no. 3, pp. 1614-1622, 1995.
- [52] Wolf, I.D., "Micro-Raman spectroscopy to study local mechanical stress in silicon integrated circuits," *Semiconductor Science and Technology*, vol. 11, no. 2, pp. 139-154, 1996.
- [53] Gardiner, D.J., *Practical Raman spectroscopy*, New York: Springer-Verlag, 1989.
- [54] "Raman spectroscopy," [Online]. Available: http://en.wikipedia.org/wiki/Raman_spectroscopy.

- [55] De Wolf, I., H.E. Maes, and S.K. Jones, "Stress measurements in silicon devices through Raman spectroscopy: Bridging the gap between theory and experiment," *Journal of Applied Physics*, vol. 79, no. 9, pp. 7148-7156, 1996.
- [56] Bonera, E., M. Fanciulli, and G. Carnevale, "Raman stress maps from finite-element models of silicon structures," *Journal of Applied Physics*, vol. 100, no. 3, 2006.
- [57] Wang, B., et al., "Controlling mode degeneracy in a photonic crystal nanocavity with infiltrated liquid crystal," *Optics Letters*, vol. 35, no. 15, pp. 2603-2605, 2010.
- [58] Chandrasekhar, M., J.B. Renucci, and M. Cardona, "Effects of interband excitations on Raman phonons in heavily doped n-Si," *Physical Review B*, vol. 17, no. 4, p. 1623, 1978.
- [59] Anastassakis, E., A. Cantarero, and M. Cardona, "Piezo-Raman measurements and anharmonic parameters in silicon and diamond," *Physical Review B*, vol. 41, no. 11, p. 7529, 1990.
- [60] Srikar, V.T., et al., "Micro-Raman measurement of bending stresses in micromachined silicon flexures," *Microelectromechanical Systems*, vol. 12, no. 6, pp. 779-787, 2003.
- [61] Chen, J. and I.D. Wolf, "Theoretical and experimental Raman spectroscopy study of mechanical stress induced by electronic packaging," *IEEE Transactions on Components and Packaging Technologies*, vol. 28, no. 3, pp. 484-492, 2005.
- [62] Ryu, S.K., et al., "Micro-Raman spectroscopy and analysis of near-surface stresses in silicon around through-silicon vias for three-dimensional interconnects," *APPLIED PHYSICS*, vol. 111, no. 6, p. 063513, 2012.
- [63] Nye, J. F., *Physical Properties of Crystals: Their Representation by Tensors and Matrices*, Oxford, U.K.: Oxford Univ. Press, 1985.
- [64] Lyon, K. G., et al., "Linear thermal expansion measurements on silicon from 6 to 340 K," *J. Appl. Phys.*, vol. 48, no. 3, p. 865-868, 1977.
- [65] Hall, J. J., "Electronic effects in the constants of n-type silicon," *Phys. Rev.*, vol. 161, no. 3, p. 756-761, 1967.
- [66] McSkimin, H. J. and Andreatch, J. P., "Elastic moduli of silicon vs hydrostatic pressure at 25.0 °C and -195.8 °C," *J. Appl. Phys.*, vol. 35, no. 7, p. 2161-2165, 1964.
- [67] Burenkov, Y. A. and Nikanorov, S. P., "Temperature dependence of the elastic constants of silicon," *Fizika Tverdogo Tela (Soviet Physics Solid State)*, vol. 16, no. 5, p. 1496-1498, 1974.
- [68] Bourgeois, C., et al., "Design of resonators for the determination of the temperature coefficients of elastic constants of monocrystalline silicon," *Proc. IEEE Int. Frequency Control Symp.*, p. 791-799., 1997.

- [69] Hopcroft, M. A., Silicon micromechanical resonators for frequency references, Ph.D. dissertation, Stanford, CA: Stanford Univ., 2007.
- [70] Hart, T.R., et al., "Temperature Dependence of Raman Scattering in Silicon," *Physical Review B*, vol. 1, no. 2, pp. 638-642, 1970.
- [71] "Strong Lines of Helium (He)," [Online]. Available:
<http://physics.nist.gov/PhysRefData/Handbook/Tables/heliumtable2.htm>.
- [72] Zhang, L., et al., "Through Silicon Via Fabrication with Low- κ Dielectric Liner and Its Implications on Parasitic Capacitance and Leakage Current," *Jpn. J. Appl. Phys.*, vol. 51, no. 4, p. 04DB03, 2012.
- [73] Abdul Kadir Kureshi, Mohd. Hasan, "Analysis of CNT Bundle and Its Comparison with Copper Interconnect for CMOS and CNFET Drivers," *Journal of Nanomaterials*, 2009.
- [74] Sinha, A., et al. , "Modeling Thermal Conductivity and CTE for CNT-Cu Composites for 3-D TSV application," *IEEE Nanotechnology Materials and Devices Conference*, pp. 262-266, 2010.
- [75] Tsai, M.Y., et al. , "Investigation on Cu TSV-induced KOZ in silicon chips: Simulations and experiments," *IEEE Transactions on Electron Devices*, vol. 60 , no. 7, pp. 2331 - 2337, 2013.
- [76] Ryu, S.K., et al., "Effect of Thermal Stresses on Carrier Mobility and Keep-Out Zone Around Through-Silicon Vias for 3-D Integration," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 2, pp. 255-262, 2012.
- [77] Mercha, A., et al., "Comprehensive analysis of the impact of single and arrays of through silicon vias induced stress on high-k/metal gate CMOS performance," *Proc. IEEE IEDM*, vol. 2, no. 2, pp. 1-4, 2010.
- [78] Kanda, Y., "A Graphical Representation of the Piezoresistance Coefficients in Silicon," *IEEE Trans. Electron Devices*, vol. 29, no. 1, pp. 64-70, 1982.