MODELLING AND APPLICATION OF SPIRAL INDUCTORS IN CMOS LC-VCOs

by

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Abstract

Communication systems are essential components of our everyday lives and they facilitate accessing and using the ever-increasing amounts of data that have surrounded us. The main objective of this research is to present solutions at the device, circuit, and system levels for key passive and active circuit building blocks of communication systems, namely, monolithic passive inductors and inductor-based voltage-controlled oscillators (LC-VCOs). These components are almost ubiquitously used in integrated wireless and wireline communication transceivers, as well as other computing devices.

Key contributions of this work are as follows: In the context of monolithic inductors, we have studied different inductor structures such as doubly-stacked inductors, vertical inductors, and coupled-rings. We have developed circuit models to accurately estimate their inductance and quality factor. The proposed analytical expressions provide designers with a reasonable estimate of their circuit performance and layout constraints. The result of proposed analyses is verified by the measurement results of test structures implemented in CMOS technology.

Regarding LC-VCOs, we have studied the effect of large signal oscillations on such VCOs by developing a mathematical model to solve the non-linear differential equation governing the LC tank circuit. The study shows that the VCO frequency and the amplitude of higher order harmonics are functions of circuit parameters such as the C-V characteristics of the varactor and the oscillation amplitude. Also, a low-power technique to boost the output amplitude of push-push VCOs is introduced. Measurement results of a proof-of-concept prototype test chip in 90-nm CMOS confirm the usefulness of the proposed technique.

Finally, at the system level, we present an analytical model to study the effect of coupling between adjacent LC-VCOs closely integrated on the same chip. This is usually the case in high-speed wireline transceivers such as those used in serial links. The proposed model explains the behavior of spurious sidebands as observed in the frequency spectrum of closely-running adjacent links. A redundant frequency mapping scheme is proposed that
significantly reduces this coupling effect. Measurement results of a highly packable clock synthesizer in a 65-nm CMOS confirm the validity of the analytical model and the effectiveness of the proposed mapping technique.
Preface

I, Reza Molavi, am the principle contributor of all chapters. Professor Shahriar Mirabbasi who supervised the research has provided technical consultation and editing assistance on the manuscript. Dr. Hormoz Djahanshahi also provided technical assistance in the design of low-power LC-VCOs and reviewed parts of the manuscripts. As described below, some of the chapters in this thesis have been written based on the following material.

Conference papers:

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3. R. Molavi, S. Mirabbas, H. Djahanshahi, “Analysis, Design and verification of fixed and variable Inductors in bulk CMOS,” to be submitted (Chapter 2)
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<th>Definition</th>
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<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>ADS</td>
<td>Agilent Design Systems</td>
</tr>
<tr>
<td>AM</td>
<td>Amplitude Modulation</td>
</tr>
<tr>
<td>AMOS</td>
<td>Accumulation-mode MOS varactor</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>CP</td>
<td>Charge Pump</td>
</tr>
<tr>
<td>CSU</td>
<td>Clock Synthesizer Unit</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
</tr>
<tr>
<td>DNW</td>
<td>Deep-Nwell</td>
</tr>
<tr>
<td>DSM</td>
<td>Deep-Sub-Micron</td>
</tr>
<tr>
<td>DUT</td>
<td>Device-Under-Test</td>
</tr>
<tr>
<td>EHF</td>
<td>Extremely-High-Frequency</td>
</tr>
<tr>
<td>EM</td>
<td>ElectroMagnetic</td>
</tr>
<tr>
<td>ESD</td>
<td>ElectroStatic Discharge</td>
</tr>
<tr>
<td>HVT</td>
<td>High $V_{th}$</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>ISF</td>
<td>Impulse Sensitivity Function</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>LP-CMOS</td>
<td>Low-Power CMOS</td>
</tr>
<tr>
<td>LTI</td>
<td>Linear Time-Invariant</td>
</tr>
<tr>
<td>LTV</td>
<td>Linear Time–Variant</td>
</tr>
<tr>
<td>MCM</td>
<td>Multi-Chip Module</td>
</tr>
<tr>
<td>MoM</td>
<td>Metal-oxide-Metal</td>
</tr>
<tr>
<td>OTN</td>
<td>Optical Transport Network</td>
</tr>
<tr>
<td>PFD</td>
<td>Phase-Frequency Detector</td>
</tr>
<tr>
<td>PGS</td>
<td>Patterned-Ground Shield</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-Locked Loop</td>
</tr>
<tr>
<td>PM</td>
<td>Phase Modulation</td>
</tr>
<tr>
<td>PNA</td>
<td>Performance Network Analyzer</td>
</tr>
<tr>
<td>ppb</td>
<td>parts-per-billion</td>
</tr>
<tr>
<td>PVT</td>
<td>Process Voltage Temperature</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RJ</td>
<td>Random Jitter</td>
</tr>
<tr>
<td>RMS</td>
<td>Root-Mean-Square</td>
</tr>
<tr>
<td>RX</td>
<td>Receiver</td>
</tr>
<tr>
<td>SERDES</td>
<td>Serializer/Deserializer</td>
</tr>
<tr>
<td>SiP</td>
<td>System-in-Package</td>
</tr>
<tr>
<td>SONET</td>
<td>Internet Synchronous Optical Networks</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Full Form</td>
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<tr>
<td>--------------</td>
<td>-----------</td>
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<tr>
<td>SRF</td>
<td>Self Resonance Frequency</td>
</tr>
<tr>
<td>SVT</td>
<td>Standard $V_{th}$</td>
</tr>
<tr>
<td>TJ</td>
<td>Total Jitter</td>
</tr>
<tr>
<td>TX</td>
<td>Transmitter</td>
</tr>
<tr>
<td>UHF</td>
<td>Ultra-High-Frequency</td>
</tr>
<tr>
<td>UTM</td>
<td>Ultra-Thick-Metal</td>
</tr>
<tr>
<td>UWB</td>
<td>Ultra-Wide-Band</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
</tbody>
</table>
Acknowledgements

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To the memories of my father

"Modern Human is mindful of the opinion of others; and does not readily rule out others' ideas even if they are in contrast with her/his own views "

Chapter 1

Introduction

The ever-increasing demand for high-speed communication has produced enormous interest for the deployment of microwave and mm-wave portion of the frequency spectrum \[1\][2]. The deployment of the radio spectrum from 3 to 10 GHz in ultra-wideband (UWB) technology has enabled high-bandwidth wireless communications at very low energy levels for short-range applications \[3\][4]. To facilitate the use of wideband signals for high-speed communication, the IEEE Standard Designation has introduced several distinct Microwave frequency bands as shown in Table 1-1[5].

<table>
<thead>
<tr>
<th>Band</th>
<th>Frequency Range</th>
</tr>
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<tbody>
<tr>
<td>C band</td>
<td>4 to 8 GHz</td>
</tr>
<tr>
<td>X band</td>
<td>8 to 12 GHz</td>
</tr>
<tr>
<td>K\textsubscript{u} band</td>
<td>12 to 18 GHz</td>
</tr>
<tr>
<td>K band</td>
<td>18 to 26.5 GHz</td>
</tr>
<tr>
<td>K\textsubscript{a} band</td>
<td>30 to 50 GHz</td>
</tr>
</tbody>
</table>

Table 1-1. Microwave frequency bands as defined by IEEE Standard Designation

Several communications systems operate in the C, X, K\textsubscript{a}, or K\textsubscript{u} bands of the microwave spectrum. These frequency bands allow large bandwidth usage while avoiding the crowded ultra-high frequency (UHF) bands (0.3 – 3 GHz) and staying below the atmospheric absorption of the extremely high frequencies (EHF) spectrum (above 50 GHz as shown in Figure 1-1). Satellite TV either operates in the C band for the traditional large dish fixed satellite service or K\textsubscript{u} band for direct-broadcast satellite. Military communications run primarily over X or K\textsubscript{a}-band links, while the K\textsubscript{a} band is
mainly being used for Milstar, police radar and Satellite communications [6]. (For example, satellite Kepler mission uses K_a frequency range to downlink the scientific data collected by its space telescope). Design of transceivers capable of communication at high frequencies is an emerging and popular topic of research [7][8].

Local oscillators (LOs), which are responsible of generating internal clocks and periodic signals, have a critical impact on the performance of the entire transceiver [9][10]. Voltage-controlled oscillators (VCOs) are one of the main building blocks of local oscillators.

![Atmospheric attenuation in dB/km as a function of frequency over the EHF band. Peaks in absorption at specific frequencies are a problem, due to atmosphere constituents such as water (H_2O) and carbon dioxide (CO_2)](image)

The large bandwidth employed for most K-band applications requires the design of wide tuning-range VCOs. Moreover, in most wireless applications many narrow-band channels reside close to each other, and even a slight non-linearity in the VCO could cause significant distortion from adjacent channels [11]. This is why there is usually a stringent requirement on the phase noise of VCOs [12]. In addition to the tuning range and phase
noise, several other requirements such as power consumption, oscillation amplitude, and die area have to be diligently considered in a VCO design.

1.1 VCOs in Phase-Locked Loops

Predominantly, local oscillators consist of one, or more, phase-locked loops (PLLs) that are responsible for signal generation at the desired frequencies [13][14]. Figure 1-2 shows a block diagram of a generic PLL employing an LC-VCO.

![Figure 1-2 A generic LC-VCO based PLL block diagram](image)

The frequency of the output clock generated by the VCO \( f_{vco} \) follows the expression \( f_{vco} = N f_{ref} \), where \( N \) is the divide ratio of the feedback clock and \( f_{ref} \) is the frequency of the reference clock (typically, a low-noise crystal oscillator). The PLL operation guarantees this relationship by employing a negative feedback that ensures the phase of the two signals, i.e., the reference clock and the output of the feedback divider, are locked to one another. Any deviation between the phases of these two signals will cause the combination of the phase-frequency detector and the charge-pump, PFD-CP, to generate
a corrective current pulse ($I_{CP}$ in Figure 1-2) into the loop filter [15]. This current modulates the loop filter output voltage that, in turn, varies the frequency of the VCO (output clock). Corrected VCO phase may be divided down through the optional feedback divider, eventually forcing PFD to respond, accordingly.

The design of VCO as the main block responsible for the clock generation is of pronounced importance for a proper PLL operation. The generic LC-VCO shown in Figure 1-2 (inset) is a simplified model of an LC-VCO which we will return to in Chapter 3. It consists of an active circuitry and an LC tank. The study of properties and characteristics of LC components and their impact on the performance of LC-VCOs constitutes the basis of this dissertation.

1.2 CMOS Implementation Challenges

Traditionally, the design of RF transceivers entailed a challenging integration problem. To achieve high performance, some critical RF and analog circuitry are still being implemented in silicon-germanium (SiGe) or gallium-arsenide (GaAs) technologies. On the other hand, most base-band and mixed-signal components, e.g., digital-to-analog converters (DACs), analog-to-digital converters (ADCs), and digital signal processing blocks (DSPs) are being fabricated in a complementary metal-oxide semiconductor (CMOS) technology. Furthermore, implementing high quality passive filters could require the usage of discrete components. Hence, most commercial RF transceivers had to adopt a multi-chip module (MCM) or system-in-package (SiP) solution to integrate most of the components resulting in an increase in the cost [16][17].

The incredible growth of the digital processes in recent years, mostly due to the continuous scaling in CMOS technology, has motivated designers to develop CMOS analog components for various applications and facilitating a single-chip solution. Furthermore, the transit frequency ($f_t$) of MOS devices has dramatically increased due to the evolution of deep-sub-micron (DSM) technologies ($f_t$'s exceeding 100's of GHz) enabling design of high-speed analog and RF circuit in CMOS.

Rapid advancements in RF CMOS design were further accelerated through the evolution of high-quality passive components on silicon substrate. As mentioned earlier, integrated
inductors are one of the critical constituents of the state-of-the-art CMOS LC VCOs [18-20]. Spiral inductors started to appear in the mixed-signal CMOS designs in the late 90s [19][20]. Originally, the modeling process of inductors for analog CMOS design was relatively time-consuming and required specific custom-developed tools such as ASITIC and ADS Momentum with moderate accuracies [21][22]. The accuracy of these tools would also depend on the type and complexity of subject structures. For example, ADS Momentum, as a 2.5-D simulation tool, uses pre-computed functions to simplify the electromagnetic simulation from 3-dimensions to 2-dimensions, and may pose modeling constraints if employed to compute the inductance for 3-D structure with several metal layers. Recently, a number of commercial tools such as Helic, SONNET and Integrand have emerged that feature inductor pcells (custom-made layout cells with parameterized properties) and are conveniently built into the mainstream design tools such as Cadence Virtuoso [23][24]. However, the relatively high cost, licensing issues, significant simulation time (required to model custom structures) and lack of analytical data limited their usage in research environments. The current trend towards using non-traditional inductor structures such as helical inductors and coupled rings in integrated circuit (IC) design, and the need for reliable models and analytical expressions to predict their performance metrics are the driving forces for our study of integrated passive inductors. The design of inductors in a mixed-signal chip may get further complicated if several spiral inductors are integrated close to one another. A common example is the integration of several LC-VCO-based PLLs on a single Serializer/Deserializer (SERDES) chip (for wireline communication) [25]. The coupling effect amongst these VCOs, also a subject of our study, may result in unwanted interactions between neighboring circuits and adversely impact their performance.

The implementation of LC-VCOs in CMOS also benefits from the use of accumulation-mode variable capacitors, also known as AMOS varactors, employed to tune the VCO frequency. Commonly referred to as "NMOS in n-well", this implementation of MOS device never enters into inversion regime [26], therefore, exhibiting a monotonic characteristic, as discussed in detail in Chapter 3. Despite several years of use in LC-VCO oscillators, the different impacts of AMOS varactors on the performance of the
VCO, are still being investigated. Several researchers have elaborated on the effects of these devices on the frequency tuning range of VCOs [27][28]. However, the complexity of the respective mathematical equations has impeded the development of a complete set of analytical solutions. Following few simplifying assumptions, this thesis derives the mathematical expressions relating the properties of AMOS varactor to the frequency tuning range and amplitude of output harmonics. These expressions provide design insights and intuitions as how to employ varactor non-linearity to operate the LC-VCOs for frequency synthesis at higher harmonics of the fundamental frequency. Using these guidelines, the design of a push-push (second-order harmonic VCOs) is presented.

1.3 Contributions

The objective of this dissertation is to present solutions at the device, circuit, and system levels for a key circuit building block, namely, LC-VCO, that is almost ubiquitously employed in integrated transceivers, as well as other communication and computing devices. The proposed solutions for LC-VCOs are useful in any PLL-based system employing one such oscillator. Hence, the solutions are either directly or indirectly applicable to other systems that incorporate PLL circuits such as clock and data recovery (CDR) systems. Key contributions of this work are as follows:

1.3.1 Analytical and Device-Level Models for Several Inductor Structures

In this work, we have studied different structures of passive inductors such as doubly-stacked inductors, vertical inductors, and coupled-rings (a popular structure for variable passive inductors) from a circuit perspective. We have thus developed circuit models to accurately estimate the inductance and quality factor of these structures. The analytical expressions proposed in this work provide designers with a reasonable estimate of their circuit performance and layout constraints. This information is of great value to RF system designers who are involved in the block specifications and floor-planing of the entire chip. The result of proposed analyses are verified by the measurement results of two test structures implemented in two different CMOS processes.
1.3.2 Second Harmonic Analysis and Amplification in Push-Push LC VCOs

We have studied the effect of large signals on the LC-VCOs by developing a mathematical model to solve the non-linear differential equation governing the LC tank circuit (in both the small-signal and large-signal regimes). The study shows that the VCO frequency is a function of the amplitude of the higher-order harmonics of the output voltage. It is also shown that amplitude of higher harmonics of the output voltage is a function of circuit parameters such as the C-V characteristics of the varactor and the output signal amplitude. Hence, it is proposed that an LC-VCO employing center-tapped inductor can extract and amplify this second-harmonic. This design proves useful for high-frequency applications and maximizes the frequency tuning range. Based on the proposed architecture, a K-band VCO is designed, simulated, fabricated, and successfully tested.

Also, a low-power technique to boost the output amplitude of \textit{push-push} VCOs is introduced. It is shown that a resonance effect created by the insertion of a second varactor, tuned in harmonious with the tank varactor, significantly increases the amplitude of the second-harmonic output. Measurement results of a proof-of-concept prototype test chip confirm the usefulness of the proposed technique.

1.3.3 Coupling Analysis for Densely Integrated PLLs

This work presents an analytical model to study the effect of coupling between adjacent LC VCOs closely integrated on the same chip. This model explains the existence of spurious sidebands as observed in the frequency spectrum of two (or more) closely-running adjacent links. A redundant frequency mapping scheme is proposed that reduces this coupling effect by up to 12 dB. Measurement results of a highly packable clock synthesizer in a 65-nm CMOS technology confirm the validity of the analytical model and the effectiveness of the proposed mapping technique.
1.4 Organization of Thesis

In Chapter 2, we study several structures of fixed and variable inductors. To compare the performance of different structures, three passive inductors are modeled and designed in 65-nm CMOS. Using EM simulations, measurement results, and performance comparison of these structures, a unified circuit model is proposed for the self-inductance of the different spiral designs. Next, we turn our attention to the structures of variable inductors, in particular, *coupled rings*. This efficient structure of variable inductors is analyzed from a design point of view and analytical expressions are developed to estimate the different metrics of the inductor. Finally, the simulations and measurement results of test structures in 65-nm CMOS are presented and compared with the analytical results.

Chapter 3 reviews several recent architectures for high-frequency LC-VCOs. From this study, it is suggested that push-push VCOs, employing the second-harmonic of the oscillation, are suitable for wide-tuning-range high-frequency designs. To establish the basis of second-harmonic generation in LC VCOs employing AMOS varactors, an analytical framework is developed. Based on the results of this analysis, circuit-level solutions are proposed to boost the amplitude of push-push LC-VCOs. The measurement results of a proof-of-concept prototype LC-VCO in 90-nm CMOS, designed based on the proposed technique, are presented.

Chapter 4 presents the coupling issues facing the dense integration of several LC-VCOs on a single chip. The coupling effect in LC-VCO-based PLLs is studied from an analytical perspective and is accompanied by measurement results.

Finally, the concluding remarks and future research avenues are presented in Chapter 5.
Monolithic inductors are commonly used in state-of-the-art high-speed analog, mixed-signal, and radio-frequency (RF) integrated circuits. The performance of these circuits depends on the inductance ($L$) and quality factor ($Q$) of such passive inductors. Since monolithic inductors are implemented on lossy silicon substrate in a CMOS technology, they typically have a poor quality factor, which leads to degradations in circuit efficacy, especially at RF and microwave frequencies.

In particular, passive components, including inductors and transformers, are extensively used in communication circuits for both wireless and wireline applications. Examples of these circuits include LC-oscillators, which demand a good phase noise performance to meet the stringent requirements of wireline and wireless communication standards, inductive load of amplifiers and mixers to improve their respective gain, and inductor-based matching circuits in wireless and wireline transceivers to extend the operation bandwidth of transmit and receive circuits. The trend toward higher levels of integration in deep-sub-micron (DSM) CMOS designs (e.g. 65-nm, 40-nm and beyond), tends to lower inductor quality factor due to closer proximity of the top metal layers to the substrate, and reduced thickness and hence increased resistance of the metal layers available in the stack. A recent DSM option, the ultra-thick-metal (UTM) with lower resistivity [29], ameliorates the resistance effect, however, there is an extra
manufacturing cost associated with using this option and it may only be available in selected processes. Given the available technology options and trade-offs between inductance, area, $Q$, and self-resonance frequency (SRF) of the inductor, an accurate EM field simulator capable of modeling all DSM effects for various 3D structures, becomes an essential ingredient for today’s integrated circuit design.

Our intention in this chapter is to study and analyze several structures of fixed and variable inductors. First, the design of several fixed inductor structures in CMOS process is discussed. To compare the performance of different structures, three passive inductors are designed. The modeling technique, EM simulations, measurement results, and performance comparison of these three structures are discussed in detail. Next, the design of coupled rings structures are studied from an analytical perspective. In order to verify the results of the proposed analysis, several coupled rings are designed and simulated. Measurement results of the coupled ring test structures implemented in CMOS show good agreement with the proposed analysis.

### 2.1 Inductor Modeling

In order to choose an appropriate structure we designed and characterized three different inductor structures in a 65-nm CMOS process with 7-0-1-1 metal stack (i.e., seven metal layers with regular-thickness denoted as $M_1$ to $M_7$, no metal layer with medium thickness, thick metal layer, $M_8$ and ultra-thick metal layer $M_9$). The differential inductance ($L_{\text{diff}}$) and the differential quality factor ($Q_{\text{diff}}$) are as follows [30]:

$$L_{\text{diff}}(f) = \frac{\text{Im}[Z_{11}(f) + Z_{22}(f) - Z_{12}(f) - Z_{21}(f)]}{2\pi f}$$  \hspace{1cm} (2-1)

$$Q_{\text{diff}}(f) = \frac{\text{Im}[Z_{11}(f) + Z_{22}(f) - Z_{12}(f) - Z_{21}(f)]}{\text{Re}[Z_{11}(f) + Z_{22}(f) - Z_{12}(f) - Z_{21}(f)]}$$  \hspace{1cm} (2-2)
In this work, we focus on three commonly used structures that are used in high-frequency applications. Shown in Figure 2-1, these three structures are:

(a) Two-turn single-layer lateral inductor in the top metal layer (M9); underpass on M8,

(b) Two-turn lateral doubly-stacked inductor (two parallel metal layers (ultra-thick M9 and thick M8) connected with many vias throughout); underpass on M7 and M6,

(c) Two-turn two-layer vertical (a.k.a. helical) inductor.

As shown in the Figure 2-1, structures (a) and (b) appear similar from a top view point due to their equal metal width (W) and spiral dimensions (outer diameter and interwinding spacing, S). However, due to the addition of M8 layer in structure (b), the values of $L_{diff}$ and $Q_{diff}$ will slightly be different.
The most popular lumped-model representation of monolithic inductors is the 9-element model depicted in Figure 2-2a [31]. $L_s$ and $R_s$ represent the inductance and the series resistance, respectively. $C_p$ models the parasitic capacitance consisting of the overlap capacitance between the spiral inductor and the underpass metal, and the fringing capacitances between metal wires. The oxide capacitance between the metal wire and the substrate is modeled by $C_{ox}$. $R_{sub}$ and $C_{sub}$ model the loss to the substrate.

Since one objective of this work is to identify suitable inductor structures for systems operating at multi-GHz frequencies, for the purpose of measurement, we focus our attention on high-speed wireline applications that operate up to 5 Gb/s. Thus the maximum frequency of interest for the inductor characterization experiments is considered to be approximately up to 3\textsuperscript{rd} harmonic of the maximum clock frequency (i.e., $3 \times 5/2 \text{GHz} = 7.5 \text{GHz}$). This will greatly simplify the 9-element model of the inductor to that of a simple series RL, as shown in Figure 2-2b. Parasitic capacitance to the silicon substrate, lateral fringe capacitors between the windings, skin effect, and substrate eddy currents do not have much impact on our comparison analysis. This assumption is later confirmed by the self-resonance frequency (SRF) of the inductors measured to be nearly two octaves above the simulation frequency.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure2}
\caption{(a) The 9-element model of an inductor (b) simplified model for a qualitative analysis up to 7.5 GHz}
\end{figure}
The inclusion of $M_8$ in the inductor structure (b) is equivalent to increasing the cross-section area of the inductor wires approximately by the thickness of this metal layer. In the technology used here, the top two metal layers ($M_9$ and $M_8$) have a thickness ratio ($TR$) of 3.8. Therefore, one expects the series resistance ($R_S$) in Figure 2-2(b) to reduce by $1-(3.8/4.8) \approx 21\%$ when stacking the two layers in parallel. This estimate is confirmed by Momentum simulations showing $R_S$ to drop from 1.9 $\Omega$ to 1.5 $\Omega$.

This effect also manifests itself as a proportional increase in the quality factor of the combination stack; in this case the simulated $Q_{\text{diff}}$ increased from 8.7 to 10.6, i.e., a 22% increase verifying the earlier calculations. The value of inductance also changes due to the change in the current density in each turn of the inductor. It can be shown that for a compact inductor with large ratio of the spiral inner radius, $r$, to the cross-section radius of the wire $a$ (i.e., the ratio $\frac{r}{a}$), the inductance value can be approximated as [32]:

\[
L_1 = L_2 = L \\
M = k \sqrt{L_1 L_2} \\
\frac{1}{L_{eq}} = \frac{1}{L_1 + M} + \frac{1}{L_2 + M} \\
k = 1 \Rightarrow L_{eq} = L \\
k < 1 \Rightarrow L_{eq} = L\left(\frac{1+k}{2}\right) < L
\]

\[
L_{eq} = L_1 + M + L_2 + M \\
k = 1 \Rightarrow L_{eq} = 4L \\
k < 1 \Rightarrow L_{eq} = 2L(1+k)
\]
\[ L \approx \mu_0 r \left[ \ln \left( \frac{8r}{a} \right) - 2 \right] \]  

(2-3)

This means that a change in the cross-section of the inductor wire by going from an effective cross-section radius \( a_1 \) to \( a_2 \) causes a small change in the inductance calculated by:

\[ \Delta L \approx \mu_0 r \left[ \ln \left( \frac{a_1}{a_2} \right) \right] \]  

(2-4)

Going from single-layer to doubly-stacked \( a_2 > a_1 \), hence \( \Delta L \leq 0 \), i.e. the inductance slightly decreases. Substituting for \( TR = 3.8 \) translates to 10 to 20 pH change in the inductance depending on the approximations used to define effective cross section radius. (Note the simulated and measured \( \Delta L = L_a - L_b \) of 23 pH in Table 2-2. From the circuit perspective, this can be visualized as shown in Figure 2-3. The equivalent inductance for structure (b) which is the case of two highly-coupled parallel inductors remains slightly smaller than each individual one, as shown in Figure 2-3b.

<table>
<thead>
<tr>
<th></th>
<th>( L_{\text{diff}} ) (5 GHz)</th>
<th>( Q_{\text{diff}} ) (5 GHz)</th>
<th>( R_{\text{DC}} ) (( \Omega ))</th>
<th>( Q_{\text{max}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor (a)</td>
<td>511pH</td>
<td>8.7</td>
<td>1.8</td>
<td>12.7</td>
</tr>
<tr>
<td>Inductor (b)</td>
<td>488pH</td>
<td>10.6</td>
<td>1.42</td>
<td>12.5</td>
</tr>
<tr>
<td>Inductor (c)</td>
<td>490pH</td>
<td>9.4</td>
<td>1.61</td>
<td>11.8</td>
</tr>
</tbody>
</table>

Table 2-2 Simulation results of all three inductor structures

Immediately, the advantage of the structure (c) becomes apparent from Figure 2-3C. Employing two highly-coupled series inductors, which is the property of the helical structure (c), results in an equivalent inductance nearly four times larger than each one of them. In fact, it can be shown that \( L_{\text{eq}} \) for helical inductors is proportional to \( m^2 \) where \( m \) is the number of vertical turns. Therefore, one can achieve large inductances with much smaller lateral dimensions hence saving area. Based on the above, doubly-stacked structures appear to offer a reasonable trade-off among inductance, area and the quality factor.
The structure (c), as shown in Figure 2-1, is physically smaller than the other two structures and relies on the vertical concentration of flux to achieve similar values of inductance as in structures (a) and (b). Since one turn is implemented in a lower metal layer, $M_8$, that is more resistive and comes in series with the top layer, it is predicted that this type of inductor will not offer higher values of $Q$, in low to medium range frequencies where substrate losses are still small.

However, such structure may well be attractive for applications where a large value of inductance is required, e.g. bandwidth extension by inductive peaking. Constructing several turns that are vertically stacked in series is achievable in multi-metal layer DSM technologies (state-of-the-art processes have up to 10 metal layers). Also, since Momentum is a 2.5-D EM simulator, the comparison between EM simulation and on-wafer S-parameter measurements allows us to verify the ability and quantify the accuracy of this design suite to model 3-D structures. Table 2-2 summarizes simulation results of all three inductors. In this table, the parameter $Q_{\text{max}}$, maximum quality factor across the frequency, indicates that the slight degradation in SRF for structures (b) and (c) can be attributed to the inclusion of the lower metal layers.

### 2.2 Measurement Results of Fixed Inductors

Several inductor test structures are implemented in a 65-nm for on-wafer probing and S-parameter characterization. In order to facilitate the de-embedding procedure, short and open structures are also placed on the test wafer. Agilent E8362B, 10 MHz – 20 GHz, performance network analyzer (PNA) is used for the two-port characterization of DUT. A Cascade RF-1 Microwave probe station and a GGB Picoprobes ground-signal-ground (GSG) probe are used for on-die S-parameters measurements of the inductors, as well as open and short de-embedding structures over the frequency range of 50 MHz to 10 GHz. To simplify the calculations, we adopted the two-step open/short de-embedding (OSD) technique [33]. Figure 2-4 is a schematic representation of the parasitic series impedance
and shunt admittance of interconnect leads and pads, respectively.

\[
\begin{align*}
Y_{P1} & = Y_{11OP} \\
Y_{P2} & = Y_{22OP} \\
Z_{S1} & = \frac{1}{Y_{11SH} - Y_{P1}} \\
Z_{S2} & = \frac{1}{Y_{22SH} - Y_{P2}}
\end{align*}
\]

Figure 2-4 Equivalent model of the inductor in the on-wafer test setup

<table>
<thead>
<tr>
<th>Inductor</th>
<th>(\mu_{L_{\text{diff}}}) (5 GHz)</th>
<th>(\sigma_{L_{\text{diff}}}) (5 GHz)</th>
<th>(\mu_{Q_{\text{diff}}}) (5 GHz)</th>
<th>meas. vs. sim error ((\Delta L)) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>495pH</td>
<td>8.4pH</td>
<td>7.7</td>
<td>-3.2</td>
</tr>
<tr>
<td>(b)</td>
<td>474pH</td>
<td>9.5pH</td>
<td>11.8</td>
<td>-2.9</td>
</tr>
<tr>
<td>(c)</td>
<td>502pH</td>
<td>9.1pH</td>
<td>9.3</td>
<td>2.5</td>
</tr>
</tbody>
</table>

Table 2-3 The de-embedded measurement results for 10 samples of each structure, average inductance (\(\mu_{L_{\text{diff}}}\)) and standard deviation (\(\sigma_{L_{\text{diff}}}\)) as well as average Q factor (\(\mu_{Q_{\text{diff}}}\)) are reported

The open-circuit Y-parameters represent the pad capacitance to ground, while the short-circuit Z-parameters are an indication of series parasitic inductances associated with inductor leads. The admittance of the pad capacitance (\(Y_{P1}\) and \(Y_{P2}\) for the two ports) and the impedance of inductor leads (\(Z_{S1}\) and \(Z_{S2}\)) can be formulated as follows:

The values of \(L_{\text{diff}}\) and
\( Q_{\text{diff}} \) are calculated using (2-1) and (2-1) and are summarized in Table 2-3. As can be seen, the measurement results are in a close agreement with the simulation results of Table 2-2, and there exists a small systematic error for lateral structures (a) and (b), which is different for the vertical structure (c) (\( \approx -3\% \) versus. +2.5\%). In the next section these results are used to design a dense inductor to enhance the bandwidth at the input of an impedance-matched amplifier.

### 2.3 Vertical Inductor for Series Peaking

Figure 2-5(a) shows the equivalent model of a 50 \( \Omega \)-matched amplifier running at up to 5.4 Gbps. The model includes the parasitic capacitances of the electrostatic discharge (ESD) structures, as well as those of the pad. A resistance of value of 100 \( \Omega \) (\( R_{\text{esd}} \)) is inserted in the signal path to limit an ESD-event current. \( R_{\text{term}} \) and \( C_{\text{in}} \) represent the termination resistance and amplifier input capacitance, respectively.

![Figure 2-5](image-url)

**Figure 2-5** (a) Schematic model for the input of an impedance-terminated receiver (b) Eye-diagram at point (A)
Figure 2-6 (a) Inclusion of series-peaking at the input of amplifier (b) The improved eye-diagram at point (A)

The signal received at internal point A, suffers from substantial loss due to the board traces, package impedances and ESD structures. The received signal eye diagram for a transmitted signal of 1 V_{pp} and 10 inches of FR4 trace is depicted in Figure 2-5b. As can be seen, the vertical eye-opening is fairly small (75 mV_{pp}) hence the amplifier input may not be able to recover the input data correctly.

Bandwidth extension using series-peaking is an attractive technique to boost the data eye-opening at this interface [34]. As illustrated in Figure 2-6a, a 4.7 nH inductor is placed in series with R_{esd}. Based on the corresponding simulated eye-diagram shown in Figure 2-6 (b), the vertical opening in the middle of the eye has been improved by 50% to 115 mV_{pp} at 5 Gbps. A 4.7 nH inductor can occupy a large area if implemented as a lateral structure, such as structures (a) or (b) in Section 2.1. However, since this inductor
is in series with $R_{\text{esd}}$, it can tolerate a low $Q$ and hence its resistance can be absorbed into that of the ESD structure. An implementation that particularly benefits from this approach is the compact vertical inductor (structure “c”) described earlier. An approximate formula for the inductance of spiral inductors is given by 

$$L = \mu_0 n^2 r$$

[32] where $r$ and $n$ are average spiral radius and number of lateral turns, respectively. Combining these with the findings of Section 2, we modify the approximate formula for a helical inductor as

$$L = \mu_0 n^2 m^2 r$$

(2-6)

where $m$ represents the number of vertical turns. Using $n = 4$ and $m = 3$, as illustrated in Figure 2-7, $r$ is calculated to be $\approx 25 \mu m$ to produce 4.7 nH of inductance. Momentum simulations show a compact 3-turn helical inductor with $r = 22.5 \mu m$ achieves an inductance of 4.7 nH and a resistance of 30 Ω. In practice, in the series-peaking network shown in Figure 2-6 (a), $R_{\text{esd}}$ is trimmed down accordingly by 30 Ω to absorb $R_S$ of the structure. To save process cost, this inductor does not use UTM option and the top two metal layers are default thick metals instead, i.e. $M_9$ and $M_8$. The bottom windings are made of the parallel connection of thin metal layers $M_6-M_7$, analogous to the structure (b) in Figure 2-1 to mitigate large series resistance of thin metal layers.

Figure 2-7 The vertical inductor designed for series peaking (a) Top-view (b) Lateral view
2.4 Variable Inductors

The most dominant application of integrated inductors is in the “tuned circuits” where one is interested in generating or amplifying signals from a certain band(s) of frequency spectrum while suppressing frequency components outside that band. The series-peaking design in the previous section is an example of tuned-circuit for bandwidth enhancement. The increasing number of wireless and wireline standards and the need for modern electronic devices to support multitude of these standards has made wideband and programmable tuned circuits more attractive. Varactors and switched-capacitor have extensively been used in the electronic circuits in response to this demand. However, as the operating frequency of tuned-circuits enters the microwave range, a number of issues limit their usability. To elaborate, consider a simple tuned LC network as shown in Figure 2-8(a).

![Figure 2-8](a) A lossy tuned LC circuit (b) The parallel equivalent circuit

Resistors $R_{SC}$ and $R_{SL}$ model the equivalent series loss of the capacitor and the inductor, respectively. As shown in Figure 2-8 (b), it is straightforward to show that these losses can be combined into a parallel component given by:
\[ R_p \approx (Q_L^2 R_{SL})(Q_C^2 R_{SC}) = \left( \frac{\omega^2 L^2}{R_{SL}} \right) \left( \frac{1}{\omega^2 C^2 R_{SC}} \right) \]  

(2-7)

\( R_p \) determines the overall quality factor of the tuned circuit and is usually kept high to minimize the noise and power consumption of the circuit. The value of \( R_p \) in the low frequencies is dominated by the first component, i.e. the inductive loss term, \( \omega^2 L^2 / R_{SL} \), while at higher frequencies the capacitive component \( 1 / (\omega^2 L^2 R_{SC}) \) becomes the dominant contributor. Also recall that the tunability of a passive component usually comes at the cost of compromised quality factor, making tunable capacitors less desirable when their loss dominates that of the tank. Thus, at high frequencies, where the impact of inductor loss is less evident, the viability of employing variable inductors, as an alternative option to extend the tuning range, grows.

Different techniques have been proposed in literature to construct variable passive inductors either by self-inductance switching [35-36] or mutual-inductance coupling switching [37-39]. The latter approach is more attractive since the loss of the switching component affects the performance to a smaller extent [37]. Figure 2-9 (a) shows the basic idea of mutual-coupling switching where a switch (SW in Figure 2-9 (a)) is inserted in the secondary path of two mutually-coupled inductors. When the switch is in OFF state, there is no current flowing through the secondary winding and the inductance looking into the input of the primary winding is approximately \( L_1 \). However, when the switch is in ON state, according to Lenz’s law, the current in the primary winding, induces a current in the secondary that, in turn, opposes the original magnetic flux. Therefore, the net magnetic flux through the main loop (primary) is smaller, hence the equivalent inductance is smaller. Note that the change in the inductance comes at the cost of translating the output impedance of the secondary winding, i.e., the series loss of \( L_2 \) plus the impedance of the switch, to the primary.
This translated impedance is effectively in series with the loss of primary winding and degrades the overall quality factor. The magnitude of translated impedance, as well as the net change in the value of inductance, is a function of the magnetic coupling between the two windings. This creates a subtle trade-off between the tunability of the coupled-inductors and their quality (factor). To analytically demonstrate the trade-off, consider the equivalent model of two coupled rings as shown in Figure 2-9 (b). It is straightforward to show that the input impedance of this circuit is given by:

\[
Z_{in}(\omega) = R_1 + j\omega L_1 + \frac{\omega^2 M^2}{R_2 + j\omega L_2 + Z_{SW}}
\]  

(2-8)
where \( M \) and \( Z_{SW} \) represent the mutual inductance and the switch impedance, respectively. Assuming \( Z_{SW} \approx R_{SW} \), and modeling the input impedance with a lossy inductor \((L_{eq}, \text{ and } R_{eq} \text{ as shown in Figure 2-9 (c)})\), the equivalent inductance is:

\[
L_{eq} = L_1 - \frac{\omega^2 M^2 L_2}{(R_2 + R_{SW})^2 + \omega^2 L_2^2} \quad (2-9)
\]

\[
\approx L_1 (1 - \frac{M^2}{L_1 L_2}) = L_1 (1 - k^2)
\]

where the assumption made here is that the quality factor of the secondary winding is sufficiently high \((Q_2 >> 3)\). Similarly, we can show that:

\[
R_{eq} = R_1 + \frac{\omega^2 M^2 (R_2 + R_{SW})}{(R_2 + R_{SW})^2 + \omega^2 L_2^2} \quad (2-10)
\]

\[
\approx R_1 + \frac{M^2}{L_2^2} (R_2 + R_{SW})
\]

The last term in Eq. (10) can be re-written as:

\[
R_{eq} \approx R_1 \left(1 + \frac{M^2}{L_2 L_1} \frac{(R_2 + R_{SW})}{L_2 \omega} \frac{L_1 \omega}{R_1}\right) \quad (2-11)
\]

\[
\approx R_1 (1 + k^2 \frac{Q_1}{Q_2})
\]

Hence, we calculate the quality factor of the variable inductor as:

\[
Q_{eq} = \frac{L_{eq} \omega}{R_{eq}} \approx \frac{L_1 \omega (1 - k^2)}{R_1 (1 + k^2 \frac{Q_1}{Q_2})} = Q_1 \cdot \frac{1 - k^2}{1 + k^2 \frac{Q_1}{Q_2}} \quad (2-12)
\]

The significance of (2-12) is that it emphasizes that the equivalent quality factor is independent of the value of the secondary inductance \( L_2 \), and only depends on the secondary inductor’s quality factor and its coupling to the primary. The ratio \( Q_1/Q_2 \) in the denominator of (2-12) should be kept small to improve the quality factor \( Q_{eq} \). The main
inductor, i.e. $L_1$, is typically implemented with top thick metal layers, and this poses a challenge to make $Q_1/Q_2$ smaller than unity. Also, consider that $R_{SW}$ is in the series path of the secondary inductor and should be made negligible compared to $R_2$ to avoid degrading $Q_2$. Hence setting a good design target as $Q_1/Q_2 \approx 1$, we can arrive at the following:

$$L_{eq} \approx L_1(1 - k^2), \quad Q_{eq} \approx Q_1 \cdot \frac{1 - k^2}{1 + k^2}$$

(2-13)

Note that while these results were derived for two coupled inductors, they also equally apply to coupling effect from other low-loss metallic structures to any inductor. For example, (2-12) can be used to predict the performance degradation for a particular inductor due to the vicinity to other nearby metallic structures.

Figure 2-10 depicts the plot of $L_{eq}$ and $Q_{eq}$ vs. the coupling factor $k$ from (2-13) As can be seen, there is only a small range of $k$ values for which this structure produces useful results. For $k < 0.2$, the resulting change in the inductance is less than 4%, which is a typical margin of error in the inductor modeling. As $k$ increases above 0.2, this structure produces tangible changes in the value of $L_{eq}$ at the cost of $Q_{eq}$ degradation. However, for $k > 0.55$, there is over 50% loss in the quality factor of the inductor, which translates to about 3 dB signal-to-noise degradation in the system. This may not be tolerable in high-performance applications, hence for most practical applications coupled rings with $0.2 < k < 0.55$ are desirable.
25

Figure 2-10 The variation of $L_{eq}$ and $Q_{eq}$ vs. the coupling factor ($k$)

With all its simplicity, (2-13) introduces a new variable, $k$, to a designer who seeks to optimize $L_{eq}$ and $Q_{eq}$ for a particular application. In order to relate $k$ to the circuit parameters, we need to calculate $L_1$, $L_2$ and $M$ for two coupled rings and substitute in $k = M/\sqrt{L_1L_2}$.

For simplicity, consider that the two inductors are formed by two co-centric loops of current as shown in the Figure 2-11. With this assumption, we can use the equation for the self-inductance of a current loop, derived in [32]:

$$L_1 = \mu\pi R_1, \quad L_2 = \mu\pi R_2$$

(2-14)

The mutual inductance, from the electromagnetic theory, is computed as $M = \phi_{12}/I_1 = \int B_1 \cdot dS/I_1$ where $\phi_{12}$ is the magnetic flux through the loop $P_2$ due to $I_1$ current and $dS$ is the surface element in loop $P_1$.
The magnetic field of \( I_1 \) at the center of the loop, i.e. point ‘O’ in Figure 2-11, is:

\[
B_1 = \frac{\mu I_1}{2R_1}
\]  

(2-15)

If \( R_2 \ll R_1 \), one can approximate the field inside \( P_2 \) with that of expression (2-15) hence

\[
M = \frac{\int B_1 \, dS}{I_1} \approx \frac{\mu I_1}{2R_1} \pi R_2^2 \cdot \frac{1}{I_1} = \frac{\mu \pi R_2^2}{2R_1}
\]  

(2-16)

which in combination with (2-14) results in:

\[
k \approx \frac{R_2}{2R_1} \sqrt{\frac{R_2}{R_1}}
\]  

(2-17)

This formula is only valid for small values of \( R_2 \). Nonetheless, it reveals an important property of co-centric coupled rings, i.e. the coupling factor is only a function of \( R_2/R_1 \), the radius ratio of the two rings that in turn is an indication of their relative proximity.

Unfortunately (2-17) falls short of predicting \( k \) with sufficient accuracy for practical values of \( R_2/R_1 \). The proper calculation requires more elaborate analysis; details are
presented in Appendix A. Interestingly, the final result still indicates that the coupling \( k \) is only a function of the ratio of the radii of the two loops (i.e., \( k = f(R_2/R_1) \)):

\[
\begin{align*}
    k & \approx \frac{2}{\pi \gamma} \left[ (1 - \frac{\gamma^2}{2}) \cdot K(\gamma) - E(\gamma) \right], \quad \gamma = \frac{2\sqrt{R_1R_2}}{R_1 + R_2} \\
\end{align*}
\]  

(2-18)

where \( K(\gamma) \) and \( E(\gamma) \) are complete elliptic functions of first and second order, respectively. The Tables of \( K \) and \( E \) function for different values of \( \gamma \) are widely available [40].

A simple expression that is valid for most practical values of \( k \), hereinafter called region of practical \( k \) tuning (0.2 < \( k \) < 0.55), is given by (derivation also presented in Appendix A):

\[
\begin{align*}
    k & \approx \sqrt{\frac{R_1}{R_2}} \left( 1 - \sqrt{1 - \left( \frac{R_2}{R_1} \right)^2} \right) \\
\end{align*}
\]  

(2-19)

Interestingly, for small values of \( R_2/R_1 \) where the relation \( \sqrt{1 - \left( \frac{R_2}{R_1} \right)^2} = 1 - 0.5(\frac{R_2}{R_1})^2 \) holds, (2-19) translates to that of (2-17); a result that is not unexpected.

### 2.5 Simulation Results

In order to confirm the analysis presented in the previous section, a 3D simulator (integrand) is used to simulate \( L_{eq} \) and \( Q_{eq} \) for different values of \( R_2 \) and \( R_1 \).

The primary inductor in this simulation is a single-turn inductor with the average radius of 58 \( \mu \)m implemented in the top two thick metal layers, i.e. doubly-stacked \( M_9 \) and \( M_8 \). The simulated values of the inductance and the quality factor are 209 pH and 12.6, respectively, at 5 GHz (first row of Table 2-4).
Figure 2-12 Different rings are placed with radii between $R_{\text{min}}=21\text{\,\mu m}$ to $R_{\text{max}}=86\text{\,\mu m}$ (for clarity only the smallest and the largest of the rings are shown); the primary ring is a single turn with $R=58\text{\,\mu m}$.

<table>
<thead>
<tr>
<th>Name of Structure</th>
<th>Track (W) μm</th>
<th>Radius (R) μm</th>
<th>$L_{\text{eq}}$ (5 GHz)</th>
<th>$L_{\text{eq}}$ (10 GHz)</th>
<th>$Q_{\text{eq}}$ (5 GHz)</th>
<th>$Q_{\text{eq}}$ (10 GHz)</th>
<th>$K$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary</td>
<td>6.5</td>
<td>$R_1=58$</td>
<td>209</td>
<td>206</td>
<td>12.6</td>
<td>19.4</td>
<td>n/a</td>
</tr>
<tr>
<td>1</td>
<td>6.5</td>
<td>$R_2=21$</td>
<td>205</td>
<td>202</td>
<td>11.9</td>
<td>18.4</td>
<td>0.14</td>
</tr>
<tr>
<td>2</td>
<td>6.5</td>
<td>$R_2=31$</td>
<td>197</td>
<td>194</td>
<td>11</td>
<td>16.7</td>
<td>0.24</td>
</tr>
<tr>
<td>3</td>
<td>6.5</td>
<td>$R_2=40$</td>
<td>179</td>
<td>175</td>
<td>9</td>
<td>13.7</td>
<td>0.39</td>
</tr>
<tr>
<td>4</td>
<td>6.5</td>
<td>$R_2=49$</td>
<td>127</td>
<td>119</td>
<td>4.6</td>
<td>6.5</td>
<td>0.66</td>
</tr>
<tr>
<td>5</td>
<td>6.5</td>
<td>$R_2=68$</td>
<td>126</td>
<td>118</td>
<td>4.9</td>
<td>6.9</td>
<td>0.66</td>
</tr>
<tr>
<td>6</td>
<td>6.5</td>
<td>$R_2=76.5$</td>
<td>171</td>
<td>167</td>
<td>8.9</td>
<td>13.5</td>
<td>0.43</td>
</tr>
<tr>
<td>7</td>
<td>6.5</td>
<td>$R_2=86$</td>
<td>188</td>
<td>184</td>
<td>10.5</td>
<td>16.1</td>
<td>0.33</td>
</tr>
</tbody>
</table>

Table 2-4 Physical dimensions of the main inductor and metal rings
In order to change the inductance, a family of metal rings are placed inside and outside this inductor as shown in Figure 2-12. The radii of these rings are varied from $R_{2\text{,min}}=21\mu m$ to $R_{2\text{,max}}=86\mu m$. Following the recommendations of the previous discussion, $Q_2$ is increased by implementing the metal rings in the top two metal layers which improves $Q_{eq}$. The equivalent inductance, quality factor and the coupling factor are simulated for each case and are also presented in Table 2-4.

Figure 2-13 and Figure 2-14 show the plots of simulated $L_{eq}$ and $Q_{eq}$, respectively. To compare the simulation results with those of presented analysis the values obtained from the analytical expressions of $k$, i.e., the elliptic equation of (2-18) and the simplified equation of (2-19), are employed in (2-13). As can be seen in both graphs, Elliptic expression closely predicts the coupling factor, the equivalent inductance and quality factor of the coupled rings.

Even the simplified expression of (2-19) when used in the region of practical $k$ tuning predicts $L_{eq}$ and $Q_{eq}$ with an error less than 10%. These results show that designers can safely use these simple expressions to design and floorplan their coupled rings even before they start using 3D simulators to fine-tune the design.
Figure 2-14  The variation of $Q_{eq}$ the radius of the coupled secondary ring; regions of practical $k$ tuning are highlighted

An interesting observation in Table 2-4 is how the simulation results of structures (4) and (5) compare against one another. This is where the transition between the internal and external rings occurs. Note that as implied from (2-13) there always exists two distinct rings (one inside the primary, and one outside) that produce the same $k$ hence $L_{eq}$. The comparison between rows (4) and (5) reveals one simple fact: for the same value of $k$, the external ring typically shows a better performance. To explain this, note that in Table 2-4, structures (4) and (5) show similar $\Delta L$, and $k$, however $Q_{eq}$ is higher for structure (5) ($Q_{eq}$ value of 6.9 for structure (5) vs. 6.5 for structure (4) at 5 GHz). This difference is mainly attributed to the external ring structure having a higher $Q_2$, hence higher $Q_{eq}$ according to (2-12). Analytically, if the radius of the outer ring is larger than that of the inner ring by a factor of $P$ (assuming other physical dimensions are constant), its inductance is higher by roughly a factor of $P \ln P$, while the series resistance is only larger by a factor $P$. Therefore, $Q_2$ for the outer ring is higher by a factor of $\ln P$. However, this comes at the cost of larger die area and the potential undesirable coupling to other near-by structures.
2.6 Measurement Results

To validate the analytical and simulation results of the previous sections, a few coupled-ring structures are simulated and laid out in a CMOS Process. The primary inductor is a two-turn doubly-stacked spiral (M₈ and M₉ are joined together by a large number of vias) with pattern ground shield underneath and a solid ground ring around the whole structure on all metal layers for best noise isolation. The simulation results of the primary inductor show an inductance of 405 pH and a quality factor of 11.8 at 5 GHz. In order to change the inductance value, two rings are placed inside and outside the primary. The outer ring is comparably narrower (lower $Q$), and is placed closer to the primary (5 µm away), while the inner ring is wider (higher $Q$), and placed farther inside the primary loop (15 µm away). Four variants of such structure were placed on die, as listed below and shown in Figure 2-15:

![Image of test inductors](image)

**Figure 2-15** The test inductors implemented in a CMOS process: (A) primary inductor with both rings open, (B) Inner loop shorted, outer loop open, (C) Inner loop open, outer loop shorted, (D) Both loops shorted
A) Both loops open

B) Inner loop shorted, outer loop open

C) Inner loop open, outer loop shorted

D) Both loops shorted

<table>
<thead>
<tr>
<th></th>
<th>(L_{eq}) (pH)</th>
<th>(Q_{eq})</th>
<th>Radius (µm)</th>
<th>Measured (k)</th>
<th>Estimated (k) (Eq. 19)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>405</td>
<td>11.8</td>
<td>48 µm</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>B</td>
<td>388</td>
<td>10.8</td>
<td>18 µm</td>
<td>0.2</td>
<td>0.19</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>inner ring shorted</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>329</td>
<td>6.1</td>
<td>67 µm</td>
<td>0.43</td>
<td>0.41</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>outer ring shorted</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>318</td>
<td>4.9</td>
<td>Both rings shorted</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Table 2-5 De-embedded measurement results for the four structures of Figure 2-14

The measured values of \(L_{eq}\), \(Q_{eq}\), and \(k\) are shown in Table 2-5 for all the four combinations mentioned above. It is interesting to observe that predictions of (2-18) using \(R_1\) and \(R_2\) for each ring are very close to those of the measurements. Note that the derivation of (2-18) in Appendix assumes a single loop of current for the primary inductor, while the implemented primary inductor is a two-turn spiral. Deriving the exact value of \(R_1\) for such a structure, i.e. the equivalent loop radius, entails more complicated calculations. However, as a first-order estimate \(R_1\) is approximated as \((D_{in}+D_{out})/4 \approx 48\mu m\), where \(D_{in}\) and \(D_{out}\) represent the inner and outer diameters of the two-turn spiral, respectively.

Note the large drop in the value of \(Q_{eq}\) for structures C and D. This is due to the outer ring being of a lower quality factor (outer ring \(Q_2\) is 5.5 at 5 GHz) compared to the primary ring (11.8 at 5 GHz). The value of \(Q_{eq}\) as predicted by (2-12) i.e. general
expression, is 6.7 compared to the measured value of 6.1. On the other hand, for structure B, the inner ring has a high quality factor \( Q_2 = 10.5 \) at 5 GHz, which causes less degradation on \( Q_{eq} \). This allows the use of (2-13) for \( Q_{eq} \), i.e. good design target expression, which predicts \( Q_{eq} \) of 10.9 for that structure (in close agreement with the measured value of 10.8).

### 2.7 Conclusion

On-chip spiral inductors are becoming increasingly popular in DSM analog and RF design. The accuracy of modeling tools and the designer’s intuition are both necessary elements for a successful design. This chapter attempts to tackle the two issues by design, analysis and measurement comparison of different inductor structures. To facilitate the usage of a few unconventional inductors such as helical and coupled-ring structures, analytical expressions are derived and presented. The proposed study allows for fast and reliable design and optimization of these structures in CMOS technology. Measurement results of the prototype test structures validate the usefulness of the proposed analysis.
Chapter 3

Analysis, Design, Optimization and Fabrication of Push-Push LC-VCO in CMOS

The design of high frequency oscillators entails a challenging trade-off among several parameters including the phase noise, frequency tuning range, power consumption and silicon area. The integration of high-performance mm-wave voltage-controlled oscillators (VCOs) into the low-cost digital CMOS technologies is a subject of wide research interest [41-44]. The relatively low $f_t$ frequency of CMOS process as compared to other technologies such as BiCMOS and HBTs, the higher flicker noise and the limitations of interconnect and device parasitics are among major bottlenecks of high frequency CMOS VCO design. Several architectures have been proposed to address the aforementioned challenges [42-44].

We start this chapter by an overview of popular oscillator architectures and recent designs in the realm of mm-wave LC-VCOs. Push-push VCOs are shown to be an attractive solution for high frequency designs. To study the nature of 2$^{nd}$ harmonic generation in LC-VCOs, an analytical framework is developed in section 3.4. The output voltage of an LC-VCO with an accumulation-mode MOS (AMOS) varactor is analyzed from a large-signal perspective and the amplitude of the 2$^{nd}$ harmonic is expressed in terms of the circuit parameters. It is shown that the magnitude of this harmonic is a strong function of the shape of the varactor C-V characteristics. The analysis is supported by simulations to confirm this dependence. The result of this analysis is verified by design, fabrication and measurement of two wide tuning-range low-phase-noise push-push VCOs employing thin-oxide and thick-oxide AMOS devices, respectively.
3.1 VCO Architectures

3.1.1 Ring Oscillators

The simplest form of an oscillator is composed of several gain stages in a feedback loop as shown in Figure 3-1. The principle conditions for oscillation of a negative-feedback amplifier known as “Barkhausen criteria” are as follows [45][46]

$$|H(j\omega)| \geq 1$$
$$\angle H(j\omega) = 180^\circ$$

(3-1)

where $H(j\omega)$ is the loop gain transfer function. Ring oscillators are very popular clock generators in the digital and mixed-signal applications mainly because of their wide tuning range and compact implementation. However, they suffer from a relatively large phase noise which prohibits their use in application with tough jitter specifications [47]. Particularly, in wireless applications where many neighboring channels reside a few kHz from each other, it is usually not possible to meet the stringent inter-modulation requirements using ring oscillators.
3.1.2 LC Oscillators

The inherently better phase noise of LC oscillators in comparison to their ring oscillators counterparts made them very popular in wireless applications [48]. In addition, the fine-tuning capability of this class of oscillators (using on-chip varactors, and variable inductors) without the need for extra voltage-to-current (voltage-to-voltage) converter blocks enables their efficient integration into a PLL[49].

Returning to the generic LC-VCO shown in Figure 1-2 (inset), we re-draw the circuit (Figure 3-2) and start analyzing this circuit by first ignoring the LC tank.

![Figure 3-2 Schematic of a generic LC-VCO](image)

The structure of two back-to-back inverters normally constitutes a latch, which is capable of holding an initial value simply like a memory cell.
From another perspective, there are only two (even) number of inverter stages in the loop and, one does not expect this loop to oscillate (unlike ring oscillators it does not satisfy the phase requirement of (3-1). However, the addition of an LC tank across the structure nullifies its memory property (note that inductor acts as a short in DC and does not allow the '1' and '0', i.e. a net DC voltage across inductor, to latch in the cell) and causes the loop to oscillate due to the resonance effect. Now, the inverters only act as energy-providers to compensate for the losses in the LC tank. This allows simplifying the active part of the circuit (as long as it provides the minimum required energy to sustain the oscillation) to reduce the output noise. One example of this simplification is the Colpitts oscillator shown in Figure 3-3.

![Colpitts Oscillator](image)

**Figure 3-3 Colpitts Oscillator**

In this classical Colpitts VCO with capacitive feedback from drain to source, it can be shown that the circuit oscillates if $g_m R_p \geq 4$ [46], where $g_m$ is the transconductance of MOS transistor and $R_p$ is the equivalent parallel resistance seen at the drain of the transistor, and includes non-idealities of inductors and capacitors. The frequency of oscillation is given by:
\[ \omega = \sqrt{\frac{1}{L(C_p + \frac{C_1C_2}{C_1 + C_2})}} \]  

where \( C_p \) is the parasitic capacitance that appears in parallel with the inductor, and the second term in parentheses is the series equivalent of \( C_1 \) and \( C_2 \). Due to the use of only one transistor in this architecture, it exhibits a good phase noise performance, and is, therefore an attractive solution for high-frequency oscillators.

Looking from a different perspective, we can treat the Colpitts circuit as a negative transconductance in parallel with an LC tank. If one connects the bottom plate of \( C_2 \) to the gate of the MOS device (AC ground) as in Figure 3-4, the input impedance is given by:

\[ Z_{in} = -\frac{g_m}{C_1C_2\omega^2} - j\left(\frac{1}{C_1\omega} + \frac{1}{C_2\omega}\right) \]  

It is evident from this equation that Colpitts structure presents negative (real) impedance at its drain node. This is an essential ingredient to guarantee the oscillation given the loss of low-quality on-chip inductors and capacitors.
With this in mind, we surmise that any parallel LC structure that has sufficient negative impedance to overcome its inherent loss may oscillate. This motivates the use of popular cross-coupled structure in LC VCOs with a negative transconductance of $-1/g_m$ [49] when used differentially. Therefore, by using cross-coupled PMOS and NMOS in parallel to the LC tank one comes to the complementary cross-coupled LC VCO shown in Figure 3-5. Note the similarity between the complementary cross-coupled structure and the back-to-back inverters introduced earlier in Figure 3-1. Viewing active devices as energy providers to the tank, either NMOS-pair, PMOS-pair or even the current source at the tail of the cross-coupled structures, may be dropped to simplify the circuit and allow more voltage headroom for the oscillation. Furthermore as depicted in Figure 3-5b and Figure 3-5c the connection to the supply or ground can be provided through the use of a center-tapped inductor.

**Figure 3-5** Several variations of cross-coupled VCO (a) complementary (b) NMOS-only (c) PMOS-only
3.2 LC-VCO Phase Noise

The noise on the output phase of VCO, as the clock generator for most wireline and wireless transceivers, may severely degrade the signal to noise ratio (SNR) in both the receive and transmit paths. The output of a VCO may be written as \( V(t) = A\cos(\omega_0 t + \varphi_n(t)) \) where \( A \) and \( \omega_0 \) are the amplitude, and fundamental frequency, respectively. The term \( \varphi_n(t) \) represents the random variations in the phase of oscillator in the time domain, and may be viewed as skirts to the ideal response of an oscillator in the frequency domain [48] (Figure 3-6a) The spectrum of phase-noise can be decomposed into three distinct regions, as shown in Figure 3-6b:

1) Rapid roll-off around the carrier (called close-in phase noise) with \( 1/\Delta f^3 \) roll-off rate where \( \Delta f \) is the offset from the carrier

2) \( 1/\Delta f^2 \) in the intermediate offsets (some-times called out-of-band region).

3) Flat region where the phase noise is dominated by the noise floor of the output path.

There are several methods of analyzing phase noise in oscillators. The linear time-invariant (LTI) model relies on finding the noise voltage across the tank by calculating the current noise, and then multiplying it by the impedance of tank around the resonance frequency. Using this analysis in combination with practical curve fit-fitting techniques, the Leeson formula is arrived at [50]:

\[
L[\Delta \omega] = \frac{2FKT}{P_{\text{sig}}} \left[ 1 + \left( \frac{\omega_0}{2Q\Delta \omega} \right)^2 \right] \left[ 1 + \frac{\Delta \omega_{\text{shift}}}{|\Delta \omega|} \right]
\]

(3-4)

In a more elaborate analysis, using linear time-variant (LTV) model of the phase noise, Hajimiri and Lee [51] introduced a cyclo-stationary function called Impulse Sensitivity Function (ISF), \( I(t) \), that explains many shortcoming of the LTI model. The use of this function captures the different behaviors of the oscillator when excited by noise sources in different instants of time. For example an input noise source applied at zero-crossing
Figure 3-6 a) Time, and frequency domain representation of phase noise, b) Different regions of LC VCO phase noise

Instant of an oscillator waveform can generate far greater phase noise than one applied at any maxima or minima. Using this LTV model phase noise of an oscillator can be rewritten as [51]:

\[ L_{SBC}(\Delta \omega) \approx 10 \log \left( \frac{i_n^2}{\Delta f \sum_{m=0}^{\infty} c_m^2} \right) \]  

(3-5)

where \( i_n^2 \) represents all noise sources (currents here) in the VCO, \( c_m \) are Fourier coefficients of ISF function, \( q_{max} = cV_{max} \) is the maximum charge across the tank, and \( \Delta \omega \) is the offset frequency. The importance of this expression is that it quantifies the phase noise in terms of the circuit parameters. For instance, it can be shown that the close-in phase-noise (1/\( f^3 \) region in Figure 3-6b) is closely related to the symmetry properties of cross-coupled pair. Therefore, matching the rise and fall times of VCO waveform can reduce the close-in phase noise. It can be shown that proper matching of rise and fall times significantly reduces the first Fourier coefficient (\( c_0 \)) of ISF function, hence the phase noise.
3.3 **High-Frequency and mm-Wave LC-VCO Design**

Since the proliferation of multi-gigahertz operation, several studies have been conducted toward the realization of high-performance oscillators. There has been much focus on LC-type VCOs specifically Colpitts, and cross-coupled architectures mainly due to their superior noise performance.

In [52] a 16 GHz differential Colpitts VCO is realized in 0.18µm BiCMOS technology. The choice of Colpitts in this design is mainly based on the fact that it generally possesses a smaller RMS, and DC values of ISF compared to the cross-coupled counterpart [53]. A schematic of this VCO is shown in Figure 3-7a. A PMOS-type Colpitts design is adopted in this work due to lower flicker noise of PMOS devices. The DC current source, in traditional Colpitts design, is replaced by an RF choke to avoid any headroom degradation caused by the use of active devices. A center-tapped inductor (connected to $V_{dd}$) provides the DC current for the core of the VCO. In order to drive the 50 Ω impedance of the measurement device a source-follower buffer is inserted at the output of VCO. This buffer architecture is preferred over the typical open-drain one to avoid the addition of a matching circuitry required at 16 GHz, though the latter provides a higher gain. This oscillator resonates at 16.5 GHz with a phase-noise of -115 dBc/Hz at an offset of 1 MHz. The entire circuit consumes 43 mW of power (30 mW core VCO, and 13 mW buffer).

In another work [54], an NMOS cross-coupled VCO with a PMOS current source is employed to achieve oscillation at 60 GHz. The use of PMOS at the center-tap of the inductor allows the bias of $V_{drain}$ (as depicted in Figure 3-7b) at around the mid-rail, i.e. $V_{dd}/2$. This allows full deployment of the varactor tuning range by sweeping the control voltage, $V_{tune}$, from 0 to $V_{dd}$. One particular aspect of the high-frequency VCO considered by this work is the critical impact of varactor $Q$ in supra-10 GHz applications. As discussed in the previous chapter, in the mm-wave frequency range the $Q$ of the tank is constrained by the varactor’s $Q_C$, see (2-7). In this work it is shown that the quality factor of varactor is given by:
Figure 3-7 a) 16 GHz Colpitts VCO in ref [52] b) High-frequency VCO in ref [54]

\[
Q_c \approx \frac{1}{\omega R_s C} = \frac{12}{\omega C_{ox} (R_{nw} L^2 + R_{poly} W^2)} \\
(3-6)
\]

where \( C_{ox} \) is the gate-oxide capacitance per area, \( R_{nw} \), and \( R_{poly} \) are sheet resistance of the n-well, and poly gates, respectively, and \( L, W \) represent the length, and width of each finger. The factor of 12 is based on the assumption that gate, and n-well contacts are connected from both sides. Since \( R_{nw} \) is higher than \( R_{poly} \), one should minimize \( L \) while make \( W \) large enough in order to both improve \( Q \), and not compromise the tuning range. The fabricated VCO achieves a tuning range of 5.8 GHz at 59 GHz with a phase noise of -89 dBc/Hz at 1 MHz offset. The current drawn from a 1.5 V supply is 16.5 mA.
In yet another recent work in [55], the VCO tuning is implemented using the intrinsic capacitance of the core transistors to avoid the use of lossy varactors. The idea behind this work is to employ the voltage-dependent junction capacitors of a MOS device in place of tank varactors. A triple-well NMOS device has several junction capacitances suitable for this purpose. In particular, one is able to change the drain-bulk capacitance by applying a voltage to the bulk node of this configuration. By varying the bulk voltage between 0 and 1V, the depletion capacitance of this region changes from 8.9 fF to 12.1 fF for the NMOS device used in this design ($V_{\text{bulk}}$ values exceeding 1V may forward bias the junction and should be avoided). This results in an overall cap change of 10% for the NMOS structure. Using a low-loss spiral inductor ($Q_L \approx 20$), this VCO achieves an oscillation frequency of 69.8 GHz. Measured tuning range of 4.5% (66.7 GHz to 69.8 GHz) is reported for this VCO.

A different approach to alleviate the problem of varactor loss at high frequencies is to tune the circuit for a lower frequency (lower varactor loss) and multiply up its output to generate the desired frequency. In [56] a source degeneration technique (as shown in Figure 3-8a) is proposed that allows the extraction of the 2nd harmonic content of the fundamental oscillation. It is analytically shown that the squaring function of $M_1$-$M_2$ pair provides a frequency doubling effect. This effect, in turn, generates two in-phase 2nd harmonic signals at the source node of the differential pair which is then extracted at the common-mode connection of the two degeneration capacitors, $C_S$, and is amplified through the use of a single-ended tuned amplifier. Therefore, to generate 60 GHz output signal, the LC tank circuit is required to operate only up to 30 GHz resulting in an improved quality factor. The VCO consumes 30 mW (including the VCO core and the following amplifier at $2f_o$) from a 1.2 V supply and the measured phase noise at 1 MHz offset is -89 dBc/Hz.

The concept of extracting and amplifying the 2nd harmonic offers oscillation frequencies above the fundamental frequency of a conventional oscillator. This family of oscillators called push-push are attractive solutions for the wide-tuning-range and high frequency VCO applications.
In [57] another extraction technique for push-push VCO is proposed, where the differential 2\textsuperscript{nd} harmonic signal is generated at two source nodes of NMOS and PMOS pairs. When VCO operates in the voltage-limited regime, a second harmonic current (due to the push-push effect) flows through the impedance from each source node to supply (ground) as shown in Figure 3-8b. The usefulness of the proposed architecture is experimentally verified by the implementation of a CMOS VCO in 0.13-\mu m CMOS process and an output frequency range of 5.47-5.77 GHz.

![Figure 3-8 a) Push Push VCO presented in [56] b) 2\textsuperscript{nd} harmonic extraction technique in [57]](image)

**3.4 Second Harmonic Generation in AMOS-Based LC tank**

As discussed, in the push-push VCO design the concept of harmonic amplification is used to constructively add the even-order harmonics of the VCO’s fundamental frequency. Works presented in the literature focus on extracting the signal from a common-mode node of the differential oscillator where the 2\textsuperscript{nd} harmonic is
generated by two *time-interleaved* voltage (current) switching caused by the two *halves* of the circuit, i.e. the common source of a cross-coupled pair or the power supply connection [56-58].

In this section, we analyze the LC tank in an AMOS-based LC VCO. A closer study of the non-linear differential equations governing the behavior of this tank reveals that the 2\textsuperscript{nd} harmonic signal may alternatively be generated by the periodic change of the tank capacitance.

### 3.4.1 Small-Signal Analysis

Figure 3-9 illustrates the equivalent model for a cross-coupled LC-VCO with an AMOS varactor. The negative transconductance, $-g_{active}$, is the equivalent transconductance of the cross-coupled active devices. In the steady state, the tank parallel loss, $R_{tank}$, and the negative active resistance, $-1/g_{active}$, cancel each other. The remaining circuit is a lossless LC tank with a variable capacitor (varactor) that oscillates given a non-zero initial condition. The charge stored on the capacitor $C$ at any instance of time is given by $dQ = C(V).dV$.

![Figure 3-9 LC Tank Circuit](image)

Thus, we have a differential equation, which defines the oscillation voltage $V(t)$:
\[
\frac{1}{L} \int V(t) \, dt = -\frac{dQ}{dt} = -C(V) \frac{dV}{dt}
\]  

(3-7)

(3-7) is a nonlinear integral differential equation [59] and results in the following second-order nonlinear differential equation

\[
C(V) \frac{d^2 V}{dt^2} + \left( \frac{dC}{dV} \right) \left( \frac{dV}{dt} \right)^2 + \frac{1}{L} V = 0
\]  

(3-8)

As can be seen from (3-8), an additional nonlinear term is present in this second order differential equation. Therefore, the solution is not as straightforward as an LC resonator with fixed values of \( L \) and \( C \).

However, employing a linearization technique, assuming a small-signal regime of operation, it can be shown that the solution is still periodic. For that purpose, we define \( h = \frac{dV}{dt} \), which then allows us to convert (3-8) into a system of first-order differential equations

\[
\begin{align*}
\frac{dV}{dt} &= h = f(h, V) \\
\frac{dh}{dt} &= \frac{1}{L} V + h^2 \left( \frac{dC}{dV} \right) = g(h, V)
\end{align*}
\]  

(3-9)

The behavior of (3-9) response can be predicted with the Jacobian matrix technique at the vicinity of static equilibrium point. To find the static equilibrium point, \( \frac{dV}{dt} \) and \( \frac{dh}{dt} \) are set to zero resulting in \(( \frac{dV}{dt}, V) = (h, V) = (0, 0)\). Note that this corresponds to zero current and zero voltage for the LC tank, which can intuitively be justified for the static equilibrium point. Hence, the Jacobian matrix at the equilibrium point by:
\[
\begin{bmatrix}
\frac{\partial f}{\partial V}(0,0) & \frac{\partial f}{\partial h}(0,0) \\
\frac{\partial g}{\partial V}(0,0) & \frac{\partial g}{\partial h}(0,0)
\end{bmatrix}
= \begin{bmatrix}
0 & 1 \\
\frac{1}{LC(0)} & 0
\end{bmatrix}
\] (3-10)

where \( C(0) = C_{DC} \) in (3-10) refers to the DC (bias) capacitance of varactor in the absence of any oscillation, i.e. \( V(t)=0 \). The eigenvalues of this matrix, which are the poles of the linearized system, determine the behavior of the system around the static equilibrium point, i.e., whether the response is oscillatory, over damped, or underdamped. Since the eigenvalues of this matrix are purely imaginary \( (\pm j/\sqrt{LC_{DC}}) \), \( V(t) \) oscillates around the equilibrium point with the angular frequency of \( \omega_0 = 1/\sqrt{LC_{DC}} \).

This solution is, of course, valid as long as \( V(t) \) stays in the small-signal regime of operation. However, in most practical LC-VCO designs \( V(t) \) does not satisfy this condition and the angular frequency \( (\omega) \) starts to deviate from the value given by \( \omega_0 \). To derive the analytical expression for the angular frequency we need to re-visit (3-7) accounting for the large signal variations.

### 3.4.2 Large-Signal Analysis

Figure 3-10a shows the cross section of an accumulation-mode varactor. \( n^+ \) regions are buried in an \( n \)-well which in turn guarantees the device does not enter inversion and creates a monotonic C-V characteristics [60].

To analyze large-signal oscillation, one requires to model the voltage-dependant nature of \( C(V) \) in order to solve (3-7). The C-V characteristics of a typical AMOS varactor (as shown in Figure 3-10b) is modeled as [61]:

\[ C(V) = C_{DC} + \frac{1}{LC} V^2 \]
where $C_0$, $C_1$, $V_0$ and $V_1$ are shown in the Figure 3-10b and $V_{GS}$ represents the instantaneous gate-source voltage across the varactor. Note that during the oscillation, the gate plate of varactor is continuously modulated by the output voltage while its source node is held at a fixed voltage (called $V_{ctrl}$) corresponding to the desired frequency. Therefore, one can write $V_{GS} \propto V(t)$ from an AC perspective.

In the steep region, (3-11) can be linearized as:

$$C(V) \approx C_0 + C_1 \cdot \left( \frac{V - V_0}{V_1} \right) = C_{DC} + KV \quad (3-12)$$

where $C_{DC}$ is a fixed term that includes all the parasitic capacitances in the tank, and $K = C_1/V_1$ represents the slope of C-V characteristics in the steep region. Using this approximation, (3-7) simplifies to:
Figure 3-11  Spectrum of arbitrary function V(t) and its square V^2(t)

\[
\frac{1}{L} \int V(t) \, dt = -\frac{dQ}{dt} = -[C_{DC} + KV] \frac{dV}{dt}
\]  

(3-13)

\[
\frac{1}{L} \int \dot{V}(t) \, dt = -C_{DC} \frac{dV}{dt} - K \frac{dV^2}{dt}
\]

\[
\frac{K}{2} \frac{d^2V^2}{dt^2} + C_{DC} \frac{d^2V}{dt^2} + \frac{1}{L} V = 0
\]  

(3-14)

As can be seen, (3-14) is a second-order differential equation in terms of V(t) and V^2(t).

The existence of the first term in (3-14) indicates an important property of this circuit:

**Since V(t) has a fundamental frequency of f_0, V^2(t) has an energy component at 2f_0 (due to the convolution effect as shown in Figure 3-11). Therefore, to satisfy (3-14) V(t) must itself have an energy component at 2f_0.**
The above proves the existence of higher-order harmonics in \( V(t) \) and allows us to express it using the Fourier series expansion:

\[
V(t) = \sum_{m=1}^{\infty} a_m \cdot \cos(m \omega t)
\]  
(3-15)

Using (3-13) and (3-15), one may express (3-7) as:

\[
\frac{1}{L} \sum_{m=1}^{\infty} \frac{a_m}{m \omega} \cdot \sin(m \omega t) = \sum_{m=1}^{\infty} m \omega a_m \sin(m \omega t) \times \left( C_{DC} + K \cdot \sum_{m=1}^{\infty} a_m \cos(m \omega t) \right)
\]  
(3-16)

From the expression of (3-14) we deduce that the first two harmonics are dominant terms of \( V(t) \). The 3\(^{rd} \) harmonic may occasionally become significant due to the power supply clipping (nevertheless with negligible impact on the 2\(^{nd} \) harmonic amplitude). Using the first two harmonics of \( V(t) \) in (3-6) after some algebra we drive the following expressions for the angular frequency \( (\omega) \), and the 2\(^{nd} \) harmonic \( (a_2) \):

\[
\omega = \frac{1}{\sqrt{L(C_{DC} - \frac{K^2 A^2}{6C_{bias}})}}
\]  
(3-17)

\[
a_2 = \frac{K.A^2}{3C_{DC}}
\]  
(3-18)

where \( A \) is the peak amplitude of the oscillation voltage across the LC tank. (3-17) reveals an important property of a linear capacitance in LC-VCOs. Although, the time-average value of \( C(V) \) from (3-13) is \( C_{DC} \), the frequency of oscillation \((f = \omega/2\pi)\) deviates from that of \( \omega_0 = 1/\sqrt{LC_{DC}} \).
The variation of $C(t)$ creates a nonlinear displacement current, $C.dV/dt$ through the varactor which has the net effect of shifting the frequency of oscillation to slightly higher frequencies (Note that the second term in the denominator of (3-17) is always positive).

To confirm the results of this analysis a cross-coupled LC-VCO, shown in Figure 3-12, is designed and simulated in SpectreRF. The inductor is a symmetrical inductor and its loss is modeled by a series resistor. The back-to-back inverters only exist to provide enough negative transconductance to cancel the loss of 1 nH inductor and, otherwise, sized to have the minimum loading on the tank, i.e. 15 fF of parasitic capacitance vs. the total tank capacitance of approximately 1 pF. To investigate the effect of varactor slope on the frequency of oscillation, VCO is first simulated with fixed value of capacitance summarized in the first column of Table 3-1. Using these values of capacitance, the frequency of oscillation ranges from 4.565 GHz to 5.575 GHz (second column). Next, the
fixed capacitors are replaced with linear varactors created in VerilogA (Appendix B) with C-V characteristics shown in Figure 3-13. Note that the C-V characteristics of Figure 3-13 does not have saturation levels of $C_{\text{min}}$ and $C_{\text{max}}$.

![Graph showing C-V characteristics](image)

**Figure 3-13 Characteristics of simulated VerilogA linear varactor**

<table>
<thead>
<tr>
<th>Fixed Capacitance (pF)</th>
<th>Simulated Freq (GHz) - Fixed</th>
<th>$V_{\text{ctrl}}$ (V) for an equivalent linear varactor</th>
<th>Simulated Freq (GHz) - Linear</th>
<th>$2^{\text{nd}}$ harmonic amplitude seen at the middle of inductor (mV)</th>
<th>$2^{\text{nd}}$ harmonic as predicted by (3-18) (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>5.575</td>
<td>1, point A</td>
<td>5.596</td>
<td>26.8</td>
<td>25.3</td>
</tr>
<tr>
<td>0.88</td>
<td>5.32</td>
<td>0.8, point B</td>
<td>5.336</td>
<td>24.1</td>
<td>23.0</td>
</tr>
<tr>
<td>0.96</td>
<td>5.097</td>
<td>0.6, point C</td>
<td>5.111</td>
<td>21.9</td>
<td>21.1</td>
</tr>
<tr>
<td>1.04</td>
<td>4.899</td>
<td>0.4, point D</td>
<td>4.911</td>
<td>20.1</td>
<td>19.5</td>
</tr>
<tr>
<td>1.12</td>
<td>4.724</td>
<td>0.2, point E</td>
<td>4.733</td>
<td>18.5</td>
<td>18.1</td>
</tr>
<tr>
<td>1.2</td>
<td>4.565</td>
<td>0 point F</td>
<td>4.574</td>
<td>17.15</td>
<td>16.9</td>
</tr>
</tbody>
</table>

**Table 3-1 Summary of simulation and analysis data for LC-VCO results**
The time-averaged value of varactor for each $V_{ctrl}$, i.e. $C_{DC}$, shown in Figure 3-13 corresponds to one of the fixed capacitor values, e.g. point A corresponds to 0.8 pF, point B to 0.88 pF, etc.

Simulation results confirm that the frequency of oscillation slightly shifts up and now varies from 4.574 GHz to 5.596 GHz. This shift in frequency (10-20 MHz) is solely due to the linear change of capacitance as the output voltage of the VCO modulates the varactor.

![Diagram](image)

**Figure 3-14 a) C-V characteristics of a piecewise linear varactor biased at $C_{bias}$ b) Periodic time-domain variations of the varactor experiencing voltage modulation at its gate**

More interestingly, the amplitude of the 2\textsuperscript{nd} harmonic observed at the differential nodes is closely predicted by the expression of (3-18). Since both the slope of C-V curve, i.e., $K$ in (3-18), and the oscillation amplitude of the tank, i.e., $A$, are constant, the numerator of (3-18) does not vary when using linear varactors. Therefore, as $C_{DC}$ decreases in the denominator of (3-18) by increasing $V_{ctrl}$, the amplitude of 2\textsuperscript{nd} becomes larger.

The foregoing analysis assumes a constant C-V slope across the varactor tuning range. However, for a realistic varactor as $V_{ctrl}$ approaches its extreme values, the slope of C-V characteristics becomes much smaller and eventually becomes zero. To see the impact of this saturation, consider Figure 3-14a which shows the piecewise linear model of a realistic varactor biased at control voltage of $V_{bias}$ corresponding to varactor value of $C_{bias}$. As the output voltage of VCO, $V(t)$, modulates the gate of the varactor, the
instantaneous value of capacitance, \( C(t) \), changes periodically. However, the shape of \( C(t) \), deviates from a pure sinusoid (Figure 3-14b). In order to use the results of (3-17) and (3-18), we need to calculate \( C_{DC} \) and \( K \). \( C_{DC} \) is simply the time average of \( C(t) \) shown in Figure 3-14b. On the other hand, examining (3-16) closely reveals that \( K \) can be obtained from the first Fourier coefficient \((c_1)\) of \( C(t) \) as \( K = c_1/A \). After some algebraic derivation we have:

\[
C_{DC} = \frac{1}{\pi} \left[ C_{bias} \sin^{-1}(R) + A K (1 - R \sqrt{1 - R^2}) + C_{\text{max}} \left( \frac{\pi}{2} - \sin^{-1}(R) \right) \right] \\
- \frac{1}{\pi} \left[ C_{bias} \sin^{-1}(X) + A K (1 - X \sqrt{1 - X^2}) + C_{\text{min}} \left( \frac{\pi}{2} - \sin^{-1}(X) \right) \right]
\]  
(3-19)

where \( R = \max (1, V_{\text{max}} - V_{\text{bias}}/A) \) and \( X = \min (-1, V_{\text{min}} - V_{\text{bias}}/A) \)

![Figure 3-15 C-V characteristics of a piecewise linear varactor](image)

\[
K = \frac{1}{\pi} \left[ K[\sin^{-1}(R) - R \sqrt{1 - R^2}] + (C_{\text{max}} - C_{\text{bias}}) \sqrt{1 - R^2} \right] \\
- \frac{1}{\pi} \left[ K[\sin^{-1}(X) - X \sqrt{1 - X^2}] + (C_{\text{bias}} - C_{\text{min}}) \sqrt{1 - X^2} \right]
\]  
(3-20)
To confirm, now assume that the linear varactors of Figure 3-12 are replaced with the piecewise linear varactors shown in Figure 3-15. As can be seen the only difference is the clipping of capacitance value for $V_{\text{ctrl}} < 0$ and $V_{\text{ctrl}} > 1\, \text{V}$.

In order to predict the tuning curve of VCO using (3-18), values of $C_{\text{DC}}$ and $K$ are calculated using (3-19) and (3-20) for different $V_{\text{ctrl}}$. The simulation results and the prediction of (3-18) and $1/\sqrt{LC_{\text{DC}}}$ are plotted in Figure 3-16.

Examining these plots indicate that the results of $1/\sqrt{LC_{\text{DC}}}$ fall short of accurately predicting the frequency of oscillation, particularly at the extremes of control voltage where the saturation of C-V characteristics have a significant impact on the behavior of the tank. On the other hand, results of (3-17) are in close agreement with the simulation results due to the inclusion of effective slope, $K$, in frequency calculations.

![Figure 3-16 Comparing the frequency tuning range of analytical expressions and spectreRF simulations using a VerilogA model for the varactor](image)
Figure 3-17 Comparing the 2nd harmonic amplitude of analytical expressions and spectreRF simulations using a VerilogA model

Also, plotted in Figure 3-17 are the simulated amplitude of the second harmonic as well as that predicted by (3-18). The curve peaks at the middle of the control voltage because the effective slope, $K$, as calculated by (3-20) is at its maximum when varactor is biased at the center of its steep region, i.e. point $C$ in Figure 3-15. Also, it is interesting to note that shape of amplitude is not symmetrical around its peak. In fact, the amplitude is smaller at the lower end of the tuning range due to larger $C_{DC}$, as expected by (3-19).

This result demonstrates a principle difference between the fundamental-mode and 2nd harmonic mode of operation. In the former, the amplitude of oscillation is determined by the current flowing through the cross-coupled devices and is given by the formula (for current-limited regime of operation)[60]:

$$A = \frac{2}{\pi} IR$$  \hspace{1cm} (3-21)

(3-21) implies that amplitude of the oscillation is not a function of control voltage and remains constant across the frequency tuning range. On the other hand, Figure 3-17 emphasizes that the amplitude of the second harmonic is a strong function of the varactor C-V characteristic and may vary quite substantially across the tuning range as the
varactor slope changes. This phenomenon should well be considered to generate reasonable output amplitude out of push-push VCOs.

3.5 Study of Varactors in CMOS Technology

At this point, let us study the C-V characteristics of different AMOS varactors available in CMOS technology and how they may impact the amplitude of the second harmonic. The following flavors of AMOS varactors are considered here:

1) A thin-oxide AMOS varactor with Standard Vt (SVT)
2) A thin-oxide AMOS varactor with Standard Vt in Deep N-Well (SVT-DNW)
3) A thin-oxide AMOS varactor with High Vt (HVT)
4) A thick-oxide AMOS varactor

Figure 3-18 C-V characteristics for different varactors (W=1.6 µm, L=400 nm, Multiplier=200)
The C-V characteristics of these varactors are shown in Figure 3-18. The thin-oxide AMOS varactor offers a steeper C-V characteristics which makes it a suitable candidate for harmonic amplification, as per (3-18). It also offers a smaller parasitic capacitance (hence a smaller $C_{bias}$) and a larger capacitance ratio ($C_{max}/C_{min}$) that, respectively, result in a higher frequency and an increased tuning range of the VCO. To confirm we employed both the thin-oxide and thick-oxide varactors to implement push-push LC-VCOs as described in the next section.

### 3.6 Design and Verification of Push-Push LC VCO in CMOS

Figure 3-19 shows the schematic of a cross-coupled push-push LC VCO designed to verify the analysis in the foregoing sections. The tail-current source of this VCO is removed to increase the headroom for operation at low supply voltage (1.2 V). A side-benefit of this approach is the elimination of the tail-current noise, which would otherwise fold back into the close-in phase noise of the VCO. This also eliminates the need for the tail current source, current mirror, and the associated bias circuitry. Furthermore, the increased oscillator swing due to the added headroom boosts the 2nd harmonic content quadratically, according to (3-18).

The value of the inductor is chosen relatively small to allow for a wide tuning range while it still provides an acceptable level of phase noise. It is implemented as a centre-tapped inductor ($L = 170$ pH) with a third terminal suitable to extract the 2nd harmonic.
The automatic sum of the VCO complementary outputs at this center tap suppresses the fundamental frequency of the VCO and amplifies its 2nd harmonic. Extracting the 2nd harmonic at this node eliminates the need for bulky inductors [62], external bias-T [63] or otherwise long interconnects needed to prevent the 2nd harmonic from sinking to the
supply in typical CMOS push-push VCOs. The simulated inductance and quality factor at 11.25 GHz (fundamental frequency of the LC tank) are $L = 170 \, \text{pH}$ and $Q = 9$, respectively. The leads of the inductor and routing metals are modeled using parasitic elements in Momentum ADS and back-annotated into the schematic. To amplify the 2nd harmonic over a wide frequency range, the center-tap output of the inductor is AC-coupled to the input of a transimpedance amplifier with a feedback resistance of $R_F = 4 \, \text{k}\Omega$. This configuration helps maintain proper operation of the circuit over process, temperature and supply voltage variations. It also avoids the use of tuned amplifier and the associated bulky passive components. The VCO core and buffers draws 15mA from a 1.2 V supply.

To investigate the effect of C-V characteristics on the amplitude of 2nd harmonic two flavors of varactors (SVT thin-oxide and SVT thick-oxide) with exact same size (64 fingers of $W=1.6 \, \mu\text{m} \, \text{L}=400 \, \text{nm}$) are used in two otherwise identical VCOs.

![Figure 3-21 Simulated tuning curve of the 25 GHz push-push VCO vs. the control voltage](image)
The tank oscillation at half the output clock frequency allows a broad tuning range of 20.1 GHz to 25.2 GHz at the output of VCO employing the thin-oxide varactor. The tuning range of the VCO employing thick-oxide varactor is smaller and limited from 22.5 GHz to 24.65 GHz, as expected. The simulated tuning curve of the VCO versus the control voltage is shown in Figure 3-21. Based on postlayout spectreRF PSS/PNOISE simulations, the oscillator exhibits a phase noise of -101 dBc/Hz at 1 MHz offset of a 24.5 GHz output (LC tank tuned at 12.25 GHz).

3.6.1 Measurement Results

The two push-push VCOs described in the previous section are fabricated in a 90-nm CMOS process. This VCO is targeted for K-band application when operating at the 2\textsuperscript{nd}-harmonic frequency (push-push mode). RF transistors and inductor layouts characterized and provided by the foundry are used. The output buffer is designed to drive the 50 Ω impedance of the measurement device. Cascade RF-1 Microwave probe station with Cascade RF quadrant PGSSGP probe (with power-ground-signal-signal-ground-power pin configuration) with 100 µm pitch between its pins is used for on-die measurements. Using the Cassecade calibration substrate (ISS 101-190), and following a standard set of short, open and load measurements the loss of probes and cables are de-embedded. The
frequency tuning curves of the oscillators are measured using Agilent PXA spectrum analyzer and are shown in Figure 3-22.

![Graph showing frequency tuning curves of oscillators](image_url)

**Figure 3-23** Measured output power of the two push-push VCOs when the output buffer is OFF

There is a close agreement between the simulation and measurement results. The error increases at the upper end of the tuning range for both graphs which can be attributed to parasitic and inductor modeling effects.

The output power (across 50-Ω load) of both push-push oscillator are also measured using the spectrum analyzer and shown in Figure 3-23. The output power for both curves peaks in around the middle of the tuning curve corresponding to the maximum effective slope. As expected, the peak power for the VCO with thin-oxide varactor is larger (by roughly ~ 3 dB) than that with thick-oxide varactor. As $V_{ctrl}$ moves away towards the extreme ends (min or max) of the tuning range, the effective slope of the varactor’s C(V) reduces, resulting in a reduced 2nd harmonic amplitude. Also note that the lowest power is observed at the lower end of $V_{ctrl}$ (corresponding to larger $C_{bias}$) again confirming (3-18). This also implies that design optimization for push-push VCOs must be carried out at this
extreme of $V_{ctrl}$ to guarantee satisfactory swing levels at the output. In other words, there is a trade-off between the tuning range and the output swing at the doubled frequency.

### 3.7 Low-Power Technique to Boost the Amplitude

As observed the amplitude of 2\textsuperscript{nd} harmonic generated in AMOS LC-VCOs, \((3-17)\), is weak and a relatively large power is required to bring it to an acceptable swing level. In this section we show that by employing a resonance technique inside the LC tank the amplitude of 2\textsuperscript{nd} harmonic may significantly be increased alleviating the power consumption burden.

To show the details, consider again the LC tank of a differential VCO with a centre-tapped inductor, as shown in Figure 3-24. In this differential structure, the fundamental oscillation frequency of the tank ($f_0$) appears as two voltage components in opposite phases at nodes 'A' and 'B'. On the other hand, the 2\textsuperscript{nd} harmonic voltages at these two nodes are in-phase \([64]\). Therefore, the signals from nodes 'A' and 'B' can be combined (added up) to cancel out the fundamental component while amplifying the 2\textsuperscript{nd} harmonic to generate a single-ended output.
In the absence of any asymmetry within the VCO core circuit, the generation of the 2\textsuperscript{nd} harmonic signals at nodes 'A' and 'B' is due to the non-linearity of the circuit components (e.g., varactors as explained in previous section) and its amplitude \((a_2)\), as explained in the previous section, is given by (3-18)

Since the 2\textsuperscript{nd} harmonic voltages at nodes 'A' and 'B' have the same amplitude and phase, when looking into the tank from the centre tap node 'O', from the 2\textsuperscript{nd}-harmonic standpoint the two inductor halves are in parallel. Therefore, the two halves constitute an equivalent inductance of \(L/4\), as depicted in Figure 3-25. If this inductive impedance resonates at \(2\cdot f_0\) with a proper capacitive load, the resulting resonance effect boosts the 2\textsuperscript{nd} -harmonic voltage well beyond its original low amplitude level. As discussed in previous section, this resonance-based boosting proves especially useful at either end of the VCO’s tuning range \((V_{ctrl,min} \text{ and } V_{ctrl,max})\), corresponding to \(f_{min} \text{ and } f_{max}\), respectively), where the 2\textsuperscript{nd} harmonic component is at its lowest level. This technique reduces the required gain and
thus the power consumption of the subsequent buffer(s) that amplify the $2^{nd}$ harmonic signal to its target level.

Figure 3-25  Differential outputs (nodes A & B) of a VCO LC tank carrying fundamental harmonic $f_0$ (in opposite phases) and 2nd harmonic (in-phase). Tank’s Thevenin equivalent model at the 2nd harmonic is shown on the right.

Interestingly enough, the value of the optimum capacitance $C_{opt}$ in Figure 3-25 to resonate with the inductance at the $2^{nd}$ harmonic (i.e., $2f_o$) is:

$$C_{opt} = \frac{1}{4\pi^2 (2f_o)^2 \left(\frac{L}{4}\right)} = C_{var}$$  \hspace{1cm} (3-22)

This means a varactor tuning in harmonious with the one in the VCO tank could be used. The calculation ignores the parasitic inductance $L_{par}$ of the centre-tap connection. However, in mm-wave applications the value of this parasitic inductance, which is typically on the order of tens of pH, is not negligible, hence, the last term in the denominator of (3-22) shall be re-written as $(L/4 + L_{par})$. In practice, the VCO output
goes through several buffering stages before driving the final load. The design of the buffer chain, considering its impact on the VCO output, entails an optimization task, which takes into account both the final load and the described 2nd-harmonic resonance effect.

![Diagram](image)

**Figure 3-26** (a) Large buffer transistor means large capacitance modulation that lowers the 2nd-harmonic swing at node O. (b) Fixed capacitance plus the gate capacitance of a smaller buffer transistor brings higher resonant swing at node O.

To explain this, consider Figure 3-26a, where the voltage swing of the 2nd-harmonic at the inductor’s centre tap modulates the capacitance value on this node. If the capacitive load is mainly comprised of MOS device(s), e.g., $C_{GS}$ of the buffer transistor in Figure 3-26a, the capacitance value becomes highly voltage-dependant. Thus, the instantaneous capacitance is modulated by the voltage swing on node 'O', which in turn causes deviation from the desired resonance frequency and results in a lower swing. In other words, the frequency of the autonomous circuit (VCO) is determined by the main LC tank, while that of the amplitude-resonance circuit is determined by $(L/4 \parallel C_o)$ where $C_o$ is the actual value of capacitance observed at node 'O'. Any deviation of the amplitude-resonance frequency from the desired value of $2f_o$ would cause sub-optimum amplification of the 2nd-harmonic amplitude. A preferred design choice shown in Figure 3-26b is when a large portion of the nodal capacitance $C_{opt}$ is not voltage-dependent, an approach that minimizes the capacitance modulation by the voltage swing at node 'O'. In this case, to optimize the 2nd-harmonic-amplitude resonance a
programmable switch is employed to add a proper fixed capacitance, namely, a metal-oxide-metal (MoM) capacitor, for the desired VCO frequency. It is worth noting that the core of the LC VCO is insensitive to any load variation at the common-mode node 'O', which is an advantage of this architecture. Thus, as discussed in the next section, one can use an array of switched capacitors to adjust the value of this fixed capacitor.

3.8 Implementation in CMOS and Measurements

To verify the proposed 2\textsuperscript{nd}-harmonic boosting technique, a push-push VCO is designed and implemented in a 90-nm low-power (LP) CMOS process. The core of VCO is similar to the push-push VCO implemented in the previous section and employs a thin-oxide varactor and a centre-tapped inductor (L = 170 pH) that generates a frequency range of 20.1 GHz to 24.8 GHz when operating at the 2\textsuperscript{nd}-harmonic frequency. The 2\textsuperscript{nd}-harmonic voltage is tapped off the centre tap of the inductor, boosted by the proposed resonance effect, and passed to the output through the buffer. Using an extracted RLC model of this centre tap, the value of the additional capacitor $C_{opt}$ for 2\textsuperscript{nd}-harmonic resonance was derived through simulations. The schematic of the VCO and the micrograph of the fabricated CMOS die are shown in Figure 3-27 and Figure 3-28, respectively.
To demonstrate the usefulness of the proposed technique, $C_{opt}$ is implemented as a switchable MoM capacitor at node 'O' ($C_1$ in Figure 3-27, controlled by NMOS switch 'M5'). When $V_{SW} = V_{dd}$, switch M5 turns ON and $(C_1 + C_{par})$ resonates with $(L/4 + L_{par})$ at the centre of the frequency tuning range, i.e., $2\cdot f_0 \approx 22.4$ GHz. $C_{par}$ represents the total parasitic capacitance on node 'O', including that from the buffer stage. The output frequency and power (across 50-$\Omega$ load) of this push-push oscillator are measured using the Agilent PXA spectrum analyzer, as shown in Figure 3-29a and Figure 3-29b, respectively. To study the effect of the 2$^{nd}$-harmonic resonance on the output amplitude, node 'O' was probed indirectly through the output buffer when the buffer was OFF.
Although in real application the buffer would be ON to boost the output power, this approach was taken for the measurements to avoid the amplitude saturation in the output buffer obscuring the observability of the amplitude resonance on the internal node 'O'. As per Figure 3-29b, when M5 is turned ON, the output power measured at node 'O' increases by up to 8 dB across the tuning range; the amplitude peaking is observable around the control voltage of 0.8 V. This demonstrates that by using a set of programmable switches, one can optimize the output power for other output frequencies and control voltages. The VCO core, excluding the buffer, draws 7.8 mA dc from a 1.2 V supply. Nominal output power across 50-Ω load when M5 is ON and the output buffer operates is about -13 dBm at mid-range frequency of 23 GHz. The total power consumption of the VCO and the buffer stage in this case is 14 mW.
Figure 3-29 (a) Measured frequency tuning range of the push-push VCO, (b) Measured output power of the VCO with and without the resonance capacitor C1 at node O. The output buffer was OFF to highlight the amplitude resonance effect.

3.9 Concluding Remarks

The effect of AMOS varactor non-linearity on the amplitude of the 2\textsuperscript{nd} harmonic in CMOS LC VCOs is analytically studied. This analysis provides designer with an accurate knowledge of LC VCO frequency tuning range as well as the amplitude of second harmonic signal generated inside the LC tank. Using the results of this study, a 25 GHz push-push VCO is designed and fabricated in a 90-nm CMOS technology. The VCO
achieves a wide tuning range \(100 \times (f_{\text{max}}/f_{\text{min}} - 1) \approx 24.7\%\) while keeping an acceptable compromise between the power consumption (18 mW) and the phase noise (-101 dBC/Hz at 1 MHz offset from 25 GHz). The use of a compact center-tapped inductor, the removal of bias currents, transmission lines and matching components, makes this VCO design a compact and inexpensive solution that is attractive for System-on-Chip implementations in general-purpose digital CMOS processes.

This chapter also proposes a technique to increase the output amplitude of the push-push VCO by boosting the 2\(^{\text{nd}}\)-harmonic through an LC resonance, hence facilitating the design of low-power-consumption VCOs [65]. Measurement results of a proof-of-concept push-push VCO implemented in a 90-nm LP CMOS process confirm the usefulness of this technique.
Chapter 4

Dense Integration of LC-VCOs and Coupling Issues

The design of clock multipliers for multi-rate multi-standard applications involves a trade-off between the output clock jitter and the frequency tuning range. Traditionally, a wide range is achieved via non-LC-based oscillators such as relaxation or ring oscillators [66-68] at the cost of higher phase noise and intrinsic jitter. LC VCOs are used for low-jitter multi-gigahertz applications, but their tuning range is inherently small [67][69]. Moreover, dense integration of multiple LC VCOs on a silicon die poses a new challenge due to mutual coupling between inductors and the resulting frequency pulling and induced phase jitter among adjacent oscillators.

In this chapter we present an analytical model to study the effect of coupling between adjacent LC VCOs when operating in a plesiochronous manner. Based on this study, a low-jitter highly compact clock synthesizer unit supporting a continuous (gapless) frequency range up to 5.8 GHz is designed and implemented in a 65-nm digital CMOS process. Measurement results are presented for densely integrated PLLs verifying the results of proposed analytical model. Finally, a redundant frequency mapping scheme is proposed to reduce the effect of coupling amongst plesiochronously running links.

4.1 Clock Jitter in Plesiochronous Neighboring PLLs

According to ITU standards for Telecommunications (ITU-T), two signals are plesiochronous if they have the same nominal rate, with any variation in rate being
constrained within specified limits. For example, two bit streams are plesiochronous if they are clocked off two independent clock sources that have the same nominal frequencies but may have a slight frequency mismatch measured in parts-per-million (ppm), which would lead to a drifting phase and cycle slips. In other words, two plesiochronous signals or systems are almost synchronous, but not quite perfectly.

One of the most challenging situations for noise coupling among densely-integrated SERDES links with independent rates is when adjacent links run in a plesiochronous manner with the line rates offset by around ±10 to ±500 ppm. In this case, magnetic coupling between LC VCOs causing noise and spurs within the bandwidth of the PLLs proves to be problematic, especially for Telecommunication standards with close-in jitter specifications (e.g., SONET OC-48 with jitter integration band from 12 kHz to 20 MHz).

We present a model that helps understand the behavior of the unwanted periodic jitter in two adjacent PLLs (here known as aggressor and victim), when the two PLLs operate at a small frequency offset and the magnetic isolation between their VCO inductors is finite.

To quantify this effect, consider two adjacent VCOs operating at slightly different frequencies, the victim VCO at $\omega_v$ and the aggressor VCO at $\omega_a = \omega_v + \Delta \omega$, separated by small frequency offset $\Delta \omega$ as shown in Figure 4-1a.
Assuming identical inductors used in the two VCOs in neighboring links, as shown in Figure 4-1b, the open-circuit voltage \( V_{n,OC}(t) \) induced by the aggressor on the victim can be calculated as follows:

\[
M = k\sqrt{L_1L_2} \quad , \quad L_1 = L_2 = L 
\]

\[
V_{n,OC}(t) = M \frac{dI_a(t)}{dt} 
\]

where \( k \) is the coupling factor between the inductors in the two VCOs (simulated using an EM simulation tool), and \( I_a(t) = I_{a,pk} \sin (\omega_a t) = I_{a,pk} \sin (\omega_o + \Delta \omega)t \) is the current flowing through the aggressor inductor. The noise voltage induced on the victim's inductor is then calculated as follows:

\[
V_{n,OC}(t) = kL\omega_a I_{a,pk} \cos(\omega_a t) 
\]

(4-1) indicates that when loaded by the tank impedance of the victim VCO, which also includes the impedance of the cross-coupled pair, the induced voltage, \( V_n(t) \), becomes smaller by a loading factor \( \alpha \). As can be seen in the example of Figure 4-2, this voltage appears as two asymmetric sidebands in the output voltage spectrum of the victim VCO. This is because the interference from the aggressor at some offset \( \Delta \omega \) from the victim VCO frequency, i.e. \( \omega_a = \omega_o + \Delta \omega \), can be modeled as the superposition of two amplitude-modulated (AM) and phase-modulated (PM) components. To explain this, we express the victim VCO's output voltage as:

\[
V_{VCO}(t) = A\cos(\omega_o t) + V_{n,pk}\cos((\omega_o + \Delta \omega)t) 
\]

where the first term represents the desired VCO output voltage oscillating at \( f_o \), while the second term is the interference due to the aggressor VCO as expressed by (4-2). Using the phasor representation in Figure 4-3 and assuming \( V_{n,pk} \ll A \), the victim’s output voltage may be re-written as:
Figure 4-2 A victim VCO oscillates at $f_o = 4.477$ GHz while an aggressor oscillating at $f_o +Δf = 4.479$ GHz induces sidebands at $(4.479$ GHz $- 4.477$ GHz) = 2 MHz away from the victim VCO. Note that the first upper sideband (at the aggressor frequency) is explained by constructive addition of AM and PM components and is larger in magnitude than the first lower sideband.

$$V_{VCO}(t) = A_V(t).\cos(\omega_o t + \phi_V(t)) \quad 4-4)$$

where $A_V(t)$ and $\phi_V(t)$ are defined as:

$$A_V(t) = A[1 + \left(\frac{V_{n,pk}}{A}\cos(\Delta \omega t)\right)] \quad (4-5)$$

$$\phi_V(t) = \left(\frac{V_{n,pk}}{A}\sin(\Delta \omega t)\right) \quad (4-6)$$
The term $A_V(t)$ represents a periodic amplitude modulation (AM) of the VCO’s carrier with a modulation index of $\frac{V_{n,pk}}{A}$ at frequency $\Delta f$ and generates two in-phase sidebands around the VCO frequency. The term $\phi_V(t)$ represents phase modulation (PM) with a modulation index of $\frac{V_{n,pk}}{A}$ and produces two opposite-phase sidebands around the VCO frequency. This explains the existence of a sideband at $(\omega_o - \Delta \omega)$ in Figure 4-2 that is smaller in magnitude than the sideband at the aggressor frequency $\omega_a = (\omega_o + \Delta \omega)$. The PM modulation of $\phi_v(t)$ can be described by a voltage perturbation $V_{C,ripple}$ at angular frequency $\Delta \omega = |\omega_a - \omega_o|$ on the control voltage of the VCO’s varactor. This voltage modulates the varactor capacitance, hence the frequency and phase of the oscillator, and creates sideband spurs. This modeling is useful since it allows us to evaluate noise-shaping behavior of the PLL on the induced phase interference, as described next.

The response of a PLL to a voltage disturbance at the input of its VCO heavily depends on the dynamics of the loop and the location of zeros and poles set for the stability of the PLL. This can be analyzed based on the closed-loop phase model of the victim PLL as shown in Figure 4-4.
As explained, $V_{C,\text{ripple}}$ represents a small-signal voltage perturbation referenced to the control voltage of the victim VCO that describes the frequency/phase modulation caused by the magnetic coupling from the aggressor VCO. The frequency of this unwanted modulation is the difference (offset) between the two VCO frequencies. The transfer function from this ripple voltage to the output phase of the victim VCO ($\phi_{\text{OUT}}$) is calculated as:

$$\frac{\phi_{\text{OUT}}}{V_{C,\text{ripple}}} = \frac{K_{\text{VCO}}S}{S^2 + \left(\frac{I_{\text{CP}}R_Z}{2\pi N K_{\text{VCO}}}\right)S + \frac{I_{\text{CP}}}{2\pi C_Z N} K_{\text{VCO}}}$$

(4-7)

$$\frac{\phi_{\text{OUT}}}{V_{C,\text{ripple}}} = \frac{K_{\text{VCO}}S}{S^2 + (\omega_{BW})S + \omega_{BW} \cdot \omega_Z}$$

(4-8)

where $K_{\text{VCO}}$, $I_{\text{CP}}$ and $N$ are the VCO gain, charge pump current and feedback divider ratio, respectively, in the charge-pump-based PLL. $R_Z$ and $C_Z$ are the values of the resistor and capacitor comprising the loop filter zero frequency. As implied by (4-8), the transfer function from the unwanted coupled spur to the output phase of the PLL has a band-pass characteristics, with the pass-band extending from the zero frequency ($\omega_z$) to the PLL’s unity-gain bandwidth frequency (denoted by $\omega_{BW}$).
We investigated the analytical results of this study in the context of several densely packed LC-VCO PLLs intended for wireline communications. In the next section, we briefly discuss the design details of this PLL first.

4.2 LC-VCO PLL Design

The block diagram of a wide tuning-range LC-VCO PLL designed for per-port integration in transceivers supporting various wireline telecommunication, and data communication standards is shown in Figure 4-5.
The PLL is fed by a stable crystal-based reference clock (REFCLK), and employs two LC VCOs, a programmable charge pump, a high-speed fractional feedback divider and flexible bank of post-PLL dividers (post-dividers) to multiply up the reference frequency to generate the intended half-baud-rate clock. This synthesizer employs a moderate bandwidth PLL, programmable from 400 kHz to 1.2 MHz, to attenuate fractional-N spurs, and the reference and charge-pump noise, while suppressing the VCO phase noise to comply with stringent jitter specifications of numerous wireline standards. As shown in Figure 4-6, the CSU provides complementary CMOS output clocks, CLKHR & CLKHRB, at half the baud-rate driving one transmitter (TX), which transmits data on both transitions of the differential clock (CLKHR-CLKHRB).

![Figure 4-6 Block diagram of one transceiver link](image)

The large tuning-range of the VCO (3.6 GHz to 5.8 GHz), coming from two LC tanks, combined with a flexible set of post-divider bank implementing multiple divide ratios with 50% output duty cycle, guarantees gapless frequency synthesis for baud rates from the VCO’s maximum frequency of 5.8 GHz down to 0.1 GHz. Relying on the wide VCO frequency range and the post-divider flexibility, a redundant frequency mapping is planned for critical Telecom. standard rates, most notably 2.488 Gb/s SONET and its derivatives, that employs alternative VCO rate and post-divider combinations to avoid
running adjacent VCOs at the same (or close) nominal rates. This allows dense integration of a large number of serializer-deserializer (SERDES) links each with a per-port frequency synthesizer, without any significant inductor coupling amongst adjacent VCOs. The CSU feedback path consists of a high-speed multi-modulus divider (MMD) running at the VCO rate that is controlled by a ΔΣ modulator (DSM) \[70\][71]. The 24b DSM uses a 3rd-order single-loop topology, allowing frequency synthesis resolution down to 2 parts-per-billion (ppb). A programmable integrated passive loop filter is used to suppress the reference clock and the DSM quantization noise from the VCO’s control voltage. A parallel combination of accumulation-mode (AMOS) varactors and PMOS capacitors is used to linearize the C-V characteristics of the on-chip capacitor to maintain optimal loop dynamics across the range of VCO’s control voltage $V_{\text{control}}$ (see Figure 4-5, inset).

Two LC VCOs with overlapping tuning ranges, each comprised of a cross-coupled NMOS and PMOS topology, generate the required 3.6 GHz to 5.8 GHz tuning range. Integrated inductor two stacked metal layers is used to achieve high quality factor ($Q$) and hence low VCO phase noise (see Chapter 2). To increase the headroom for low-voltage operation on 1-Volt supply, the tail current source of the VCO is eliminated.

It is worth noting that since there is no tail current source in this design, the $g_m$ of the devices and hence the total negative resistance is solely governed by the size of the NMOS and PMOS transistors. To guarantee the oscillation, it is necessary that $R_P \geq \frac{1}{g_{m}}$ across the frequency band, where $R_P$ is the equivalent shunt resistance of the inductor’s series loss resistance ($R_s$), and $g_m$ is the overall transconductance of the cross-coupled transistors. Assuming a relatively constant $R_s$ vs. frequency, the minimum required transconductance for oscillation varies by a factor of $(f_{\text{max}}/f_{\text{min}})^2$ across the frequency range of each VCO. Since the $g_m$ of the cross-coupled pairs has to be large enough to guarantee the oscillation start-up at the lower end of the frequency band, there is a waste of power at the higher end of the frequency range, especially at Fast process corner (FF), where the transistor threshold voltages are smaller. To alleviate this problem, a set of programmable parallel switches control the total resistance to ground, and hence the VCO’s power consumption (Figure 4-5, inset). This flexible scheme results in up to
30% power reduction for high-frequency settings or Fast silicon process corner. The wide tuning range of the VCO is achieved through the combination of coarse tuning using fixed switchable capacitors, implemented by a stack of interdigitated metal capacitors, and fine tuning of the AMOS varactors via the control voltage. A VCO calibration scheme which sets $V_{ctrl}$ to one of multiple voltage levels at startup (nominally $V_{dd}/2$) selects the optimum metal capacitor for the target rate and given process corner. Provisions have been made for temperature-aware calibration, i.e. to choose $V_{ctrl}$ for the calibration based on the calibration temperature, to offer additional margin for post-calibration variations of temperature and supply voltage.

The use of a dedicated flip-chip power bump near the VCO core is intended to minimize IR drop and power supply noise caused by other blocks in the SERDES, including adjacent PLLs. To further stabilize the VCO’s supply, a large decoupling capacitor, consisting of AMOS varactor and metal capacitor using metal layers M1-M2, is implemented underneath the patterned-ground shield (PGS) of the VCO’s inductor. The PGS is implemented in a higher metal layer (M3) to allow this implementation. The incremental effect on the inductor quality factor is negligible, while a large area of silicon die is reused to filter the sensitive VCO supply.

### 4.3 Clock Jitter Measurement in Plesiochronous Neighboring PLLs

Figure 4-7 plots the transfer function of (4-8) for the PLL described in the previous section. The shape of this transfer function implies that the plesiochronous links with rate offsets close to the bandwidth of the PLL have the largest impact on one another.
To support this analysis and key conclusion, an experiment is carried out in which the frequency offset between two adjacent PLLs is varied from 0 (synchronous operation) to values larger than the bandwidth of each PLL. The Total RMS Jitter ($TJ_{rms}$) of the PLL is measured in the time-domain for each offset case using an oscilloscope (the RMS jitter value is the 1-sigma of the clock jitter with a Gaussian distribution histogram) and the results are plotted as in Figure 4-8. The PLL under test has its zero frequency and bandwidth set to 90 kHz and 300 kHz, respectively. As seen in Figure 4-8, the total RMS jitter peaks around 200 kHz (that is near the transfer function peaking predicted by the transfer function of Figure 4-7 and drops off at frequencies below the zero frequency and above the bandwidth of the PLL, as expected from (4-8).
This behavior can also be explained by the PLL dynamics. That is if the induced spur is far below the loop’s zero frequency, the PLL response is fast enough to correct this variation and the jitter goes down. Conversely, if the spur is far above the PLL bandwidth, the VCO being an integrator does not follow fast changes on its control voltage hence the output spur will be small. Note that the jitter at zero offset reaches its lowest limit that is the intrinsic jitter (a.k.a. Random Jitter or $RJ_{rms}$) of the victim PLL. In other words, the lowest Total Jitter is achieved by synchronous operation.

In synchronous operation (0 ppm offset), the total jitter is dominated by the random jitter of a standalone PLL, which in turn depends on the noise contribution of the blocks within the PLL, as well as the PLL dynamics. Hence, the charge pump, the VCO, the feedback divider, and the passive loop filter are designed with careful attention to their random jitter contribution. This noise optimization, as will be discussed shortly, allows the use of a moderate-quality low-cost reference clock for this multi-rate PLL. In order to reduce

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Figure 4-8 Measured total jitter of the victim CSU vs. the offset frequency of aggressor link
the plesiochronous magnetic coupling effect, several techniques have been proposed that may be exercised including [72-74]. In this chapter, we propose a variation of the straightforward solution of spacing out the links physically, hence lowering the mutual coupling and the induced noise. An exercise employing this technique would be to power up every other link (rather than all links) on the chip and measure the resulting spurs. This is shown in Table 4-1. As can be seen, doubling the distance between the active links, results in about 12 dB reduction in the aggressor spur observed at the output spectrum of the victim PLL, which agrees with the fact that magnetic coupling is inversely proportional to the square of the distance between the inductors.

<table>
<thead>
<tr>
<th>Frequency offset (100 ppm)</th>
<th>Measured Spur (dBc)</th>
<th>Physical Distance (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>450 kHz</td>
<td>-44.3</td>
<td>560 (links 1 and 2)</td>
</tr>
<tr>
<td>450 kHz</td>
<td>-56.7</td>
<td>1120 (links 1 and 3)</td>
</tr>
</tbody>
</table>

Table 4-1 The measured effect of spacing on the coupling between two active links

However, if an aggressor VCO operates at a frequency corresponding to a frequency offset far above the bandwidth of the nearby victim PLL, the aggressor will have very little impact due to 20 dB/decade suppression of the coupled spur beyond the bandwidth of the victim PLL. As a result, rather than powering-down every other VCO, one can run them alternately at totally different frequencies to satisfy the above-mentioned frequency offset condition. This technique can be implemented if the dividers following each VCO provide the same final half-baud-rate clocks to their respective TX. In other words, the goal is to have a redundant frequency plan to achieve the same HRCLK(B) frequencies after the PLL post-dividers, while the VCOs run at totally different rates. In practical terms, every other VCO is tuned to a different frequency, hence circumventing the unwanted coupling between adjacent PLLs. In this case, one would only worry about the coupling between every other link, which means 12 dB improvement in the magnitude of unwanted coupled spurs. As an example of the frequency plan for 2.5 Gb/s operation,
odd-numbered CSUs have their VCOs tuned to 3.75 GHz and use the divide-by-3 post-PLL dividers to generate a 1.25 GHz output clock (i.e., the half-baud rate

clock for TX). The even-numbered CSUs generate the same 1.25 GHz output clock by tuning their VCOs to 5 GHz, followed by two stages of divide-by-2 in the CSU and the TX. This frequency scheme virtually eliminates noise coupling amongst plesiochronous neighboring links and allows for dense placement of the links with integrated per-port clock synthesizers.

4.4 Measurement Results and Comparison

Using the redundant frequency mapping technique proposed in the previous section 18 SERDES ports are integrated on a high-capacity single-chip multi-rate multi-protocol device as shown in Figure 4-9. Each clock synthesizer unit occupies an area of (560×700)μm², integrated along with a transceiver link making it 1.2mm tall, thereby
allowing a minimum integration pitch of 560μm for abutting multiple links. This device enables the convergence of high-bandwidth data, video and voice services over optical transport network (OTN) and offers advanced protocol mapping and multiplexing capabilities for more efficient multi-service integration on a single platform.

The VCO and its output multiplexer and buffers draw a typical current of 11 mA at 1 V, while the entire CSU draws under 20 mA. The measured tuning characteristics of the dual VCO vs. coarse tuning metal capacitor settings over process, temperature and supply voltage (PVT) variations are shown in Figure 4-10. Measurement results are within 0 to 2% of the simulations at \( V_{ctrl} = V_{dd}/2 \). The RMS jitter measured for SONET OC-48 application is 538 fs (integrated from 1 kHz to 40 MHz), as shown in Figure 4-11.
Figure 4-11 Closed-loop phase noise and RMS jitter measurement at 1.244 GHz output (FVCO = 4.976 GHz); RJ=538 fs, rms (1 kHz to 40 MHz) using a signal source analyzer (SSA)

Note that the PLL’s reference clock is the dominant phase noise contributor below 1 kHz. Despite the low output jitter of the CSU, its input reference clock has fairly relaxed requirements for most applications. The reference clock comes from a low-cost 2-psrms (12 kHz to 20 MHz) source, enters the chip through a single-ended pad and is conveniently auto-routed through the digital core to all the links.
Table 4-2 Summary of the CSU clock jitter for selected wireline standards

<table>
<thead>
<tr>
<th>STANDARD</th>
<th>DATA RATE (Mb/s)</th>
<th>VCO Frequency (MHz)</th>
<th>Post-PLL Divider Ratio</th>
<th>RJps-rms Isolated channel</th>
<th>RJps-rms All channels active</th>
<th>Integration Band</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fibre Channel FC_400</td>
<td>4250</td>
<td>4250</td>
<td>2</td>
<td>0.47</td>
<td>0.49</td>
<td>2.55 MHz to 2.125 GHz</td>
</tr>
<tr>
<td>Ethernet XAUI</td>
<td>3125</td>
<td>3906</td>
<td>2.5</td>
<td>0.48</td>
<td>0.55</td>
<td>1.87MHz to 1.556GHz</td>
</tr>
<tr>
<td>SONET OC-48</td>
<td>2488.32</td>
<td>4976.64</td>
<td>2×2</td>
<td>0.45</td>
<td>0.49</td>
<td>12 kHz to 20 MHz</td>
</tr>
<tr>
<td></td>
<td>3732.48</td>
<td>3×1</td>
<td>0.47</td>
<td></td>
<td>0.51</td>
<td></td>
</tr>
</tbody>
</table>

Table 4-2 summarizes measured RMS jitter of the CSU output for a few supported wireline standards. Comparative measurements are first presented for on an isolated link-under-test and then for full activity on all links. Also, both alternative configurations for odd and even channels are shown for the SONET OC-48 case. Table 4-3 presents the performance summary and comparison with prior art.

4.5 Conclusions

The design and integration of an array of LC-based clock synthesizers for multiple transceiver links supporting various wireline standards requires particular attention to the issue of electromagnetic coupling amongst LC VCOs. This work develops a modeling technique that explains the behavior of a victim synthesizer PLL due to this coupling effect. In addition, a highly packable clock synthesizer, employing redundant frequency mapping, is designed and fabricated in 65-nm CMOS technology. The measured clock jitter of this synthesizer is only 0.5 ps,rms (integrated from 12 kHz to 20 MHz) in SONET OC-48 application [78] when all adjacent links are up and running in a plesiochronous manner that is the worst-case scenario for noise coupling.
<table>
<thead>
<tr>
<th>Ref.</th>
<th>VCO Output Frequency (GHz)</th>
<th>RMS Jitter (psrms)</th>
<th>Active Area (mm²)</th>
<th>Power Nominal Supply</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>[67]</td>
<td>Ring VCO: 1.0 to 8.5</td>
<td>0.99 (1MHz-1.25GHz)</td>
<td>0.277</td>
<td>Ring VCO: 70mW</td>
<td>45-nm</td>
</tr>
<tr>
<td></td>
<td>LC-VCO: 8.3 to 11.1</td>
<td>0.55 (1MHz-1.25GHz)</td>
<td></td>
<td>LC-VCO: 60mW</td>
<td>SOI-CMOS</td>
</tr>
<tr>
<td>[68]</td>
<td>0.2 to 4</td>
<td>1.5</td>
<td>Not Reported</td>
<td>15mW</td>
<td>65-nm CMOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Analog: 1.8V</td>
<td>Analog: 1.8V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Digital: 1V</td>
<td>Digital: 1V</td>
</tr>
<tr>
<td>[75]</td>
<td>2.29 to 2.75</td>
<td>0.97</td>
<td>5.12 (entire core)</td>
<td>120mW</td>
<td>0.35-μm CMOS</td>
</tr>
<tr>
<td></td>
<td>(10kHz – 10MHz)</td>
<td></td>
<td></td>
<td>Analog: 3V, Digital: 2V</td>
<td></td>
</tr>
<tr>
<td>[76]</td>
<td>5.7 to 6.8</td>
<td>0.56</td>
<td>0.43</td>
<td>25mW</td>
<td>0.13-μm CMOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Not Reported</td>
<td></td>
</tr>
<tr>
<td>[77]</td>
<td>6.33 to 10.56</td>
<td>1.3</td>
<td>3.5 (entire core)</td>
<td>88.5mW</td>
<td>0.18-μm CMOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.5V</td>
<td></td>
</tr>
<tr>
<td>This Work</td>
<td>3.6 to 5.8 (~0 to 5.8 Gb/s baud rate using dividers)</td>
<td>0.45 (12kHz-20MHz)</td>
<td>0.39</td>
<td>20mW</td>
<td>65-nm CMOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.47 (2.5MHz - 2.12 GHz)</td>
<td></td>
<td>1V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.54 (1kHz-40MHz)</td>
<td></td>
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</table>

Table 4-3 Clock synthesizer performance summary and comparison
Chapter 5

Conclusions and Future Work

LC-VCOs are currently one of the most critical blocks in the design of high-speed clock synthesizers. In this dissertation, we proposed solutions at the device, circuit and system levels to address issues confronting designers in the design and integration of LC-VCOs. In the next section, we summarize the key accomplishments presented in previous chapters.

5.1. Accomplishments

5.1.1. Analytical Models and Expressions for Several Passive Inductor Structures

We designed, simulated and measured several inductor structures in CMOS technology. It is shown that the popular structures of doubly-stacked and helical inductor can be modeled as several inductors either in parallel (former structure) or series (the latter). Using a well-known formula for lateral inductors, a closed-form expression (5-1) for helical inductor is suggested and later employed to design series peaking circuit at the input of a receiver:

\[ L = \mu_0 m^2 n^2 r \]

(5-1)

Also, the inductance and quality factor of coupled rings are studied from a circuit perspective. It is shown that knowledge of coupling factor, k, is sufficient to estimate the metrics of the structure using (5-2)
\[ L_{eq} \approx L_1(1-k^2), \quad Q_{eq} \approx Q_1 \cdot \frac{1-k^2}{1+k^2} \quad (5-2) \]

To complete the discussion, analytical expressions for the coupling factor of coupled rings is proposed ((5-3) and (5-4))

\[ k \approx \frac{2}{\pi \gamma} \left[ (1 - \frac{\gamma^2}{2}) \cdot K(\gamma) - E(\gamma) \right], \quad \gamma = \frac{2\sqrt{R_1R_2}}{R_1 + R_2} \quad (5-3) \]

\[ k \approx \sqrt{\frac{R_1}{R_2}} \left( 1 - \sqrt{1 - \left( \frac{R_2}{R_1} \right)^2} \right) \quad (5-4) \]

Measurement results of coupled ring test structures in CMOS are presented to verify the findings of the analysis. The expressions presented here, are independent of the fabrication technology and can be used in any DSM CMOS technology.

During this study, we also studied the de-embedding techniques for the inductor characterization. The effect of undesired components is eliminated following a set of de-embedding steps allowing for an accurate characteristics derivation of the actual device-under-test (DUT).

Performance evaluation and comparison of variable passive inductor structures such as coupled rings with the active inductor topologies is of utmost importance. Design of tunable RF integrated circuits at mm-wave requires careful attention to several parameters. Depending on the circuit block and the required performance, either active or passive integrated inductors may be a suitable candidate for each application.
5.1.2 Second Harmonic Signal Generation and Amplification in LC-VCOs Employing AMOS Varactor

In this work we focused on the effect of C-V characteristics of AMOS varactors on the differential equation governing the behavior of an LC-VCO tank. First, using a linear approximation for the C-V characteristics of AMOS varactor and Fourier series expansion of differential equation, we obtained the expression in (5-5) and (5-6) for the frequency of oscillation and the amplitude of second harmonic in VCO

\[ a_2 = \frac{K.A^2}{3C_{bias}} \quad (5-5) \]

\[ \omega = \frac{1}{\sqrt{L(C_{bias} - \frac{K^2 A^2}{6C_{bias}})}} \quad (5-6) \]

Then, by introducing the equivalent slope and DC capacitance the analytical results are extended to include the effects of a piecewise linear C-V characteristics. Simulation results using VerilogA models for AMOS varactors verify the accuracy of proposed technique.

Next, a low-power technique to boost the amplitude of the second harmonic in push-push LC VCOs is introduced. This technique benefits from the fact that second harmonic signals appear as in-phase component in differential LC VCOs. Extracted at the center tap of a differential inductor, this component is significantly amplified by the addition of a varactor tuned in harmonious with the tank varactor.

A proto-type push-push LC VCO using switched capacitors is designed and fabricated in 90-nm LP CMOS process to test the applicability the proposed technique. This LC-VCO employed at its second harmonic covers a wide frequency tuning range of
20.1 - 24.8 GHz. As much as 8 dB of signal amplification is observed across the tuning curve of the test VCO.

Employing the characteristics of passive components such as AMOS varactors to create higher-order harmonic signals in LC-VCOs can be an interesting topic of future studies. The analytical framework developed in this work was focused on the study of push-push VCOs hence limiting to the second-order non-linear effects. For example, it can be shown that the second-order non-linearity in the C-V characteristics of AMOS varactor can contribute to the generation of third-order harmonics in LC-VCO (note that third-order harmonic may also be created by other non-linear effects such as supply clipping). Employing LC-VCOs to produce higher order harmonics can greatly benefit the development of mm-wave and high-frequency oscillators developed in CMOS.

5.1.3 Coupling Analysis for Plesiochronous Neighboring PLLs

We studied the effect of two neighboring PLLs coupling to one another from an analytical standpoint. We showed that the effect of magnetic coupling from an adjacent oscillator can be modeled as the superposition of two AM and PM spurious components on the victim VCO. Modeling the PM component as a small perturbation on the control-voltage of a VCO locked in a PLL loop, we showed that the magnitude of spur is governed by the shape of band-pass transfer function presented in (5-7)

$$\frac{\Phi_{OUT}}{V_{C,ripple}} = \frac{K_{VCO}S}{S^2+(\omega_{BW})S+\omega_{BW}.\omega Z}$$  (5-7)

The measurement results of several densely packed LC-oscillators in a single-chip multi-rate SERDES device are used to verify the proposed analysis. It is shown that for two neighboring links the lowest output jitter is achieved in synchronous operation, i.e. two links running at exactly the same rate, each only exhibiting their respective intrinsic jitter.
Also, for plesichronous neighboring PLLs a redundant frequency mapping scheme is presented which virtually doubles the distance between such neighboring links. This technique results in 12dB reduction of the spur magnitude induced by an aggressor VCO. Given the rapid growth of wireline communication and the need for the integration of many serial links on a single chip the study of electromagnetic coupling amongst densely-packed LC oscillators continue to be a topic of research in CMOS IC design. Intelligent frequency planning as well as creative circuit design techniques that mitigate the coupling issue allow for sustainable development of reliable high-speed data links.

The development of frequency mapping techniques and analytical models to study the coupling issues are the essential ingredients of designing the emerging multi-standard wireless and wireline transceivers. Also, the introduction of 3-dimensional integrated circuits, a.k.a. 3D ICs, requires careful attention to the issue of coupling among circuit blocks integrated in the vertical dimension.
References


Appendix A

Calculation of Coupling Factor ($k$) for Co-centric Coupled Rings

To calculate the mutual inductance for the two loops of radii $R_1$ and $R_2$ as shown in Fig. APP1, we need to calculate the flux encompassed by $P_2$ loop as given by:

$$\phi_{21} = \int B_1 \cdot dS = \int \nabla \times A \cdot dS = \int A \cdot dm$$  \hspace{1cm} (A-1)

where $A$ is the vector potential that defines the magnetic field $B_1$, and $dm$ is the length element on $P_2$, the perimeter of the loop with radius $R_2$. Note that in Fig. APP1, $R_2 < R_1$, however, the following analysis can similarly be performed for $R_2 > R_1$.

Assuming current $I_1$ flows in the main loop, one can re-write the integral using the definition of magnetic vector potential $A$ for an infinitesimal element $dl$:

$$\phi_{12} = \oint A \cdot dm = \oint \oint \frac{\mu_0 I_1 \cdot dl \cdot dm}{4\pi r}$$  \hspace{1cm} (A-2)

To calculate this expression, also known as Neuman formula [79], we need to compute $dl \cdot dm$ (dot product) and $r$ to perform the integration.

It is easy to see that $|dl| = R_1 d\theta$ and $|dm| = R_2 d\beta$, where $d\theta$ and $d\beta$ represent the angles created by infinitesimal elements of $dl$ and $dm$, respectively, as shown in Fig APP1. Hence the dot product in the numerator is:

$$dl \cdot dm = R_1 R_2 \cos(\beta - \theta) d\beta d\theta$$  \hspace{1cm} (A-3)

Also, from trigonometry we know that

$$r = \sqrt{R_1^2 + R_2^2 - 2R_1 R_2 \cos(\beta - \theta)}$$  \hspace{1cm} (A-4)
Re-writing (A-2), we have

$$\phi_{12} = \oint_{R_i} A dl = \frac{\mu_l}{4\pi} \int_{\beta}^{\theta} \int_{0}^{\infty} \frac{R_1 R_2 \cos(\beta - \theta)}{\sqrt{R_1^2 + R_2^2 - 2R_1 R_2 \cos(\beta - \theta)}} \, d\theta \, d\beta \quad (A-5)$$

This is a popular integral known in terms of the complete Elliptic functions K and E. The general form is:

$$\int \frac{\cos \theta \, d\theta}{\sqrt{a - b \cos \theta}} \approx \frac{4\sqrt{a+b}}{b} \left[ \frac{(1 - \gamma^2)}{2} \right] \left( K(\gamma) - E(\gamma) \right) \quad \gamma = \sqrt{\frac{2b}{a+b}} \quad (A-6)$$

Using $M = \varphi_{21}/l_1$ and substituting for $L_1$ and $L_2$ from Eq. (2-14) into $k = M/\sqrt{L_1 L_2}$, it is then straightforward to show that:

$$k \approx \frac{2}{\pi \gamma} \left[ \frac{(1 - \gamma^2)}{2} \right] \left( K(\gamma) - E(\gamma) \right) \quad , \quad \gamma = \frac{2\sqrt{R_1 R_2}}{R_1 + R_2} \quad (A-7)$$
Note that $\gamma$ is only a function of $R_1/R_2$, hence one only needs to know this ratio to use this approximation.

To derive the approximation of (2-19), note that field $B_i$ due to current $I_i$ is only a function of radial distance from the center of the loop. An approximation for field $B_i$ in (A-1) that satisfies boundary conditions ($r = 0$ and $r = R_i$) is

$$B_i (r) = \frac{\mu I_1}{2\sqrt{R_1^2 - r^2}}$$

(A-8)

This approximation also yields the well-known relation $L_1 = \mu \pi R_1$ for the self-inductance of the loop, where $r$ approaches zero ($r \to 0$, $R_i \approx R_2$). Hence we can use

$$\phi_2 = \int_{A_2} B_i \, dS = \int_{A_2} \frac{\mu I_1}{2\sqrt{R_1^2 - r^2}} 2\pi dr = \mu \pi I_1 \sqrt{R_1^2 - r^2} \bigg|_0^{R_2}$$

$$= \mu \pi I_1 R_1 \left( 1 - \sqrt{1 - \left( \frac{R_2}{R_1} \right)^2} \right)$$

(A-9)

Using the mutual flux expression of (A-9) in $M = \phi_2/I_1$ plus the self-inductances of (2-14) in the expression of $k = M/\sqrt{L_1 L_2}$ concludes the following for the coupling factor of the inductor:

$$k \approx \frac{R_1}{R_2} \left( 1 - \sqrt{1 - \left( \frac{R_2}{R_1} \right)^2} \right)$$

(A-10)
Appendix B

VerilogA Codes on AMOS Varactor

The following VerilogA code is used to model AMOS varactor as a hyperbolic tangent as defined by (3-11) in Chapter 3 [80].

```
`include "discipline.vams"

module varactor(p, n);
inout p, n;
electrical p, n;
parameter real c0 = 1p from (0:inf); // nominal capacitance (F)
parameter real c1 = 0.5p from [0:c0); // maximum capacitance change from nom (F)
parameter real v0 = 0; // voltage for nominal capacitance (V)
parameter real v1 = 1 from (0:inf); // voltage change for maximum capacitance (V)
real q, v;
analog begin
  v = V(p, n);
  q = c0*v + c1*v1*ln(cosh((v - v0)/v1));
  I(p, n) <+ ddt(q);
end
endmodule
```
The following VerilogA code is used to model a linear AMOS varactor for simulation purposes in Chapter3.

`include “discipline.vams”

module varactor(p, n);
  inout p, n;
  electrical p, n;
  parameter real c0 = 1p from (0:inf); // nominal capacitance (F)
  parameter real c1 = 0.5p from [0:c0); // maximum capacitance change from nom (F)
  parameter real v0 = 0; // voltage for nominal capacitance (V)
  parameter real v1 = 1 from (0:inf); // voltage change for maximum capacitance (V)
  real q, v;
  analog begin
    v = V(p,n);
    q = c0 * v + c1 * ((v - v0) * (v - v0)/v1))/2;
    I(p, n) <+ ddt(q);
  end
endmodule