A Steady-state Analytical Solution for MOSFET Channel Temperature Estimation

HeatMOS©

by

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Abstract

A steady state analytical solution for MOSFET (metal oxide semiconductor field effect transistor) channel temperature estimation has been derived and the analytical model has been used to develop a software tool called HeatMOS©. HeatMOS© estimates the MOSFET channel temperature based on information from the device layout and an industry standard BSIM3 compact model. The steady state solution is an approximation for the channel temperature distribution along its length. The HeatMOS© model has been designed to be integrated into a VLSI CAD flow to predict the steady state temperature of a full micro-chip. An equivalent M-network model for steady state temperature can be extended for each MOSFET device in a complete micro-chip. In future work, HeatMOS© can be combined with the models of interconnect to develop a full micro-chip thermal analysis software tool.

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List of Acronyms

1D	One Dimensional
2D	Two Dimensional
3D	Three Dimensional
μm	Micro-meter
ASIC	Application Specific Integrated Circuit
CAD	Computer-Aided Design
CMOS	Complementary Metal-oxide Semiconductor
EMR	Electro-migration Reliability
GDSII	Graphic Database Information Interchange
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
K	Kelvin
mA	Mili-ampere

MOS	Metal-oxide Semiconductor
nm	Nano-meter
SoC	System-on-a-Chip
SOI	Silicon on Insulator
V	Volt
VLSI	Very Large Scale Integration

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Chapter 1

Introduction

1.1 Background

Verifying the reliability of complex integrated circuits has become an increasingly complex design challenge as device geometries in fabrication processes continue to shrink (Alam et al., 2007). The low cost of fabricating integrated circuits (ICs) using CMOS (complementary metal-oxide semiconductor) continues to be the dominant fabrication technology. Micro-chips fabricated using CMOS technology are very complex and complete systems (SoC - system-on-a-chip) are common in the semiconductor industry. Predicting the operating temperature of these micro-chips should be done as early as possible to minimize the expense of resolving thermal issues late in the design phase.

The ITRS (International Technology Roadmap for Semiconductors) predicts that electro-thermal reliability will continue to present significant challenges as device geometries continue to shrink below 22 nm (ITR, 2009). Due to the high temperatures that can arise in current CMOS technologies, it has become extremely important to accurately estimate the temperatures within the micro-chip for EMR

(electromigration reliability) verification. Electromigration is a term applied to the transport of mass in metal and is accelerated by the Joule heating, the heat generated by current flowing through interconnects and devices (Black, 1969). Metal atoms are pushed by strong dc electron currents, sometimes resulting in voids in the interconnect (causing open circuits) or extruding through dielectric (causing short circuits). The Joule melting resulting from extremely high electrical current has been discussed in Fantini and Morandi (1985). There is a need to model the micro-chip temperature at a detailed level, during post-layout reliability verification, and to identify the specific metal interconnects most at risk for EMR. If certain parts of the micro-chip are heated beyond their reliability limit, it may cause a breakdown of the functionality and reliability in the whole system.

The thermal trends for the CMOS technology are demonstrated by recent data presented by the ITRS. As device sizes are reduced to nano-scale gate lengths the power density will continue to rise. Although the power density increases, the material properties of silicon, dielectric layers and metal layers remain constant and the effective thermal conductivity per unit of power will decrease. As a result the effective thermal resistance will increase per microwave of power (Semenov et al., 2003) (Figure 1.1).

Several factors contribute to the increase in power density as the device geometries shrink. First, the geometry is shrinking faster than the scaling in the supply voltage which directly contributes to an increase in power density. Second, the high frequency performance of CMOS devices improves as device geometry shrinks which means that the average clock rate in digital circuits is expected to increase.

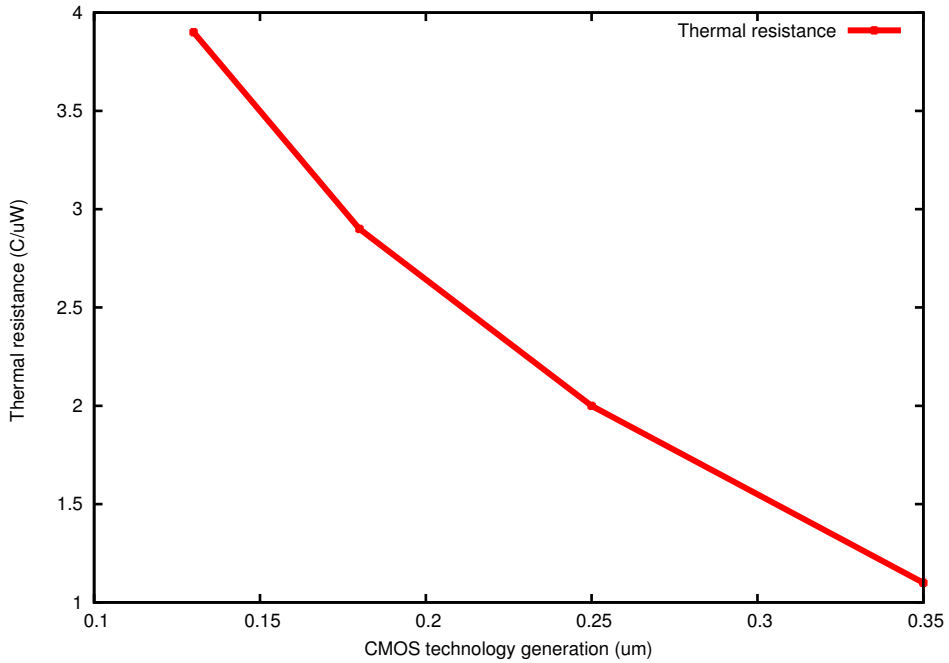

Figure 1.1: Transistor thermal resistance versus CMOS technology scaling

Dynamic switching results in power losses that are proportional to $\Lambda CV^2 f$, where C is the capacitance, f is the clock frequency, Λ is the activity factor ($0 \leq \Lambda \leq 1$), and V is the applied voltage (Sedra and Smith, 2007; Weste and Harris, 2004). Parallel efforts are made in reducing capacitance (i.e. device size), voltage, and activity factor (i.e. introduction of power management subsystem), at the same time dissipation is proportional to the square of the voltage, and voltage scaling has not kept pace with device scaling. These factors have been analyzed by the ITRS and projections on the relative increase in the operating temperature of devices are shown in Figure 1.2 (Semenov et al., 2003). The junction temperature rise will grow very rapidly and the importance of analyzing thermal profiles and the impact on EMR will become increasingly important.

The major contribution to the rising micro-chip temperatures is due to device and interconnect heating. The heat generated due to electric current flow is called Joule heating. If there is a way to estimate the temperature of a micro-chip from its layout, before manufacturing, we would be able to change the design to rectify the design issues arising from the thermal hot spots. Temperature estimation in the design phase of the integrated circuits will improve the confidence of designing for reliability and reduce the overall design time of a production micro-chip. The influence of the temperature on failure mechanisms which occur in the temperature range of -55°C to 125°C has been discussed by Pecht et al. (1992). Computer modeling of metallization failure of the integrated circuits due to electromigration has been discussed in Kirchheim and Kaeber (1991) and Sukharav et al. (2009).

There are some industrial solutions for estimating interconnects temperature. Soft-

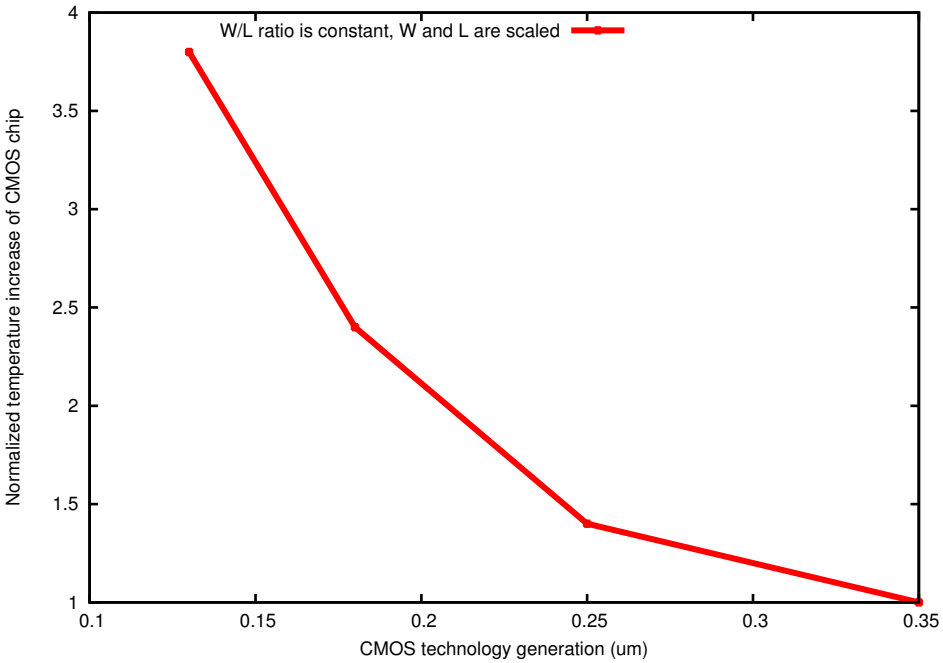

Figure 1.2: Impact of technology scaling on temperature increase

ware tools to estimate the micro-chip temperature at the package level are discussed by Melamed et al. (2009) and Oprins et al. (2009). Most of these tools use numerical approaches for temperature estimation which are slow and prohibitive for designs with millions of transistors.

There are two main sources of heat in integrated circuits. These are: the dynamic power generated by digital switching signals and the Joule heating generated by the resistance in the interconnects and the devices. Most of the power dissipation in large micro-chips is generated by digital switching signals where the dynamic power is proportional to fV^2, where f is the switching frequency and V is the applied voltage. On the other hand, Joule heat is proportional to I^2, where I is the electric current. In today's complex integrated circuits, switching frequencies are in the Giga Hertz (GHz) range while typical interconnect current and device currents are in the milliampere range.

Several approaches have been proposed to analyze the thermal performance of complex micro-chips. Analytical treatments of the 1-D steady state heat equation in IC interconnect have been presented previously in the context of interconnect temperature scaling analysis by Ajami et al. (2005), Im et al. (2002), and Chuan et al. (2009). An analytical solution of the interconnect heating and temperature estimation has been presented by Labun and Jagjitkumar (2008).

The focus of this research work is to develop a model for estimating device temperature based on device layout and steady state bias voltages.

1.2 Motivation

This research work is motivated by the need to have design tools to predict the steady state spatial variation of temperature on the integrated circuit in the design phase before the micro-chip is fabricated. A standard integrated design flow process primarily focuses on verifying the electrical performance of the design over process, temperature and voltage changes. However, design tools to model and predict the temperature behavior are not readily available. If efficient temperature modeling tools can be developed, then designers will have the ability to improve the reliability of designs in the early design phase rather than waiting for experimental results from a failure analysis.

Given the complexity of three-dimensional (3D) structures in complex integrated circuits, it is very important to have an efficient way to predict the temperature characteristics of the micro-chip. Brute force numerical solutions of the heat equation are computationally prohibitive for large IC's with millions of devices and multiple layers of interconnect. Therefore, a key focus of this research work is to investigate efficient solutions to estimate thermal characteristics that are scalable to very large and complex micro-chips.

In this research project, analytic models are developed to construct a thermal net list for the complete micro-chip. The net list is analogous to an electrical net list for a circuit. In this approach, a thermal circuit model is developed which can be used to predict the temperature.

The Multiphysics research group at UBC has developed a thermal modeling software tool called Therminator3D. This tool can be used to simulate the overall temperature profile of a micro-chip providing thermal models are developed for the interconnects and devices. Thermal models for interconnect have already been developed by other researchers (Labun and Jagjitkumar, 2008). On the other hand, thermal models for devices is much more limited and a tractable model that can be incorporated in a thermal simulation of the micro-chip is required. The goal of this research project is to address this limitation and develop an analytic model for CMOS devices.

The thermal effects in the MOSFET (Metal-Oxide Semiconductor Field Effect Transistor) are complex and multidimensional because the generated heat has spatial as well as time dependent behavior. In order to accurately estimate the temperature due to the generated heat, one must solve the differential heat equation. The heat is generated due to electric current flow and can be estimated by Joule heating. There can be different ways to solve the differential equation (e.g. finite element, finite difference (Chuan et al., 2009) and (Kuball et al., 2007), analytical), but in order to estimate the temperature rapidly so that it can be feasible to estimate the temperature of the full micro-chip during the design, analytic solutions are preferred. There has been some work done in this direction and the analytical approach has been successfully implemented in order to estimate interconnect temperature (Labun and Jagjitkumar, 2008). However the authors did not analyze the device temperature which is the primary focus of this research. Figure 1.1 shows that the device thermal resistance increases as the technology scales down (Semenov et al., 2003), which in turn leads to the higher temperatures.

The most effective way to meet the reliability target for each technology node is to incorporate design-for-reliability at the start of each technology generation. The most effective way to meet the reliability of each technology node is to have complete built-in-reliability and design-for-reliability solutions available at the start of development of each technology generation. This requires an in-depth understanding of the physics of each failure mechanism and the development of powerful and practical reliability engineering tools. High temperatures not only cause significant changes in the delay characteristics for both the transistors and the interconnects but also degrade micro-chip reliability. With technology scaling, micro-chip power densities are increasing that has led to high operating temperatures and the large thermal gradients, thereby resulting in serious reliability concerns (Tsai and Kang, 2000). Scaling the technology results in higher transistor density and higher clock frequencies. Higher clock frequencies will increases dynamic switching power because the dissipation in switching driving a capacitive load is proportional to fV^2, where f is the clock frequency and V is the applied voltage (Weste and Harris, 2004).

As device technology scales down, there is an exponential increase in the temperature $\triangle T$ between the MOSFET junction and the ambient temperature (Semenov et al., 2003). For example, as shown in Figure 1.2, $\triangle T$ has increased by a factor of three as CMOS gate lengths have reduced from 0.35 um to 0.13 um. The rapid increase in the thermal density with a reduction in scaling has increased the importance of analyzing the temperature. High temperatures or uneven temperature distributions may result not only in the reliability issues, but also in the timing failures of micro-chips. To resolve these issues, high-quality, accurate thermal

analysis, and thermally oriented placement optimizations are essential prior to fabrication (Tsai et al., 2006).

Other predictions in terms of the thermal trends in the nano-scale CMOS devices includes the total dissipation of the complex system-on-a-chip (SoC) circuits. ITRS data include for SoC dissipation is shown in Figure 1.3. The data shows that in ten years micro-chips could dissipate as much as 400 watts of heat energy(ITR, 2009). These trends demonstrate that the significant advances in terms of thermal management will be essential to keep junction temperatures within a reasonable operating temperature range. EMR failures become very significant at junction temperatures over 125 C.

1.3 Research Goals

Figure 1.4 shows a typical layout of a micro-chip. The devices are connected via interconnects. The interconnects can be represented by an equivalent resistor network for EMR verification. Each net in the interconnects network can be represented by equivalent pi-network (Labun and Jagjitkumar, 2008) for thermal analysis, and interconnect network models are required for an interconnect metallization and CMOS devices. Therefore an interconnect-transistor resistor network can be used to do a full micro-chip thermal analysis as shown in Figure 1.5. The transistor in this representation may be considered as a special type of resistor. One of the objectives of this research work is to find an equivalent resistor network representation of a transistor which can be integrated in interconnect-transistor resistor network for rapid full micro-chip thermal analysis.

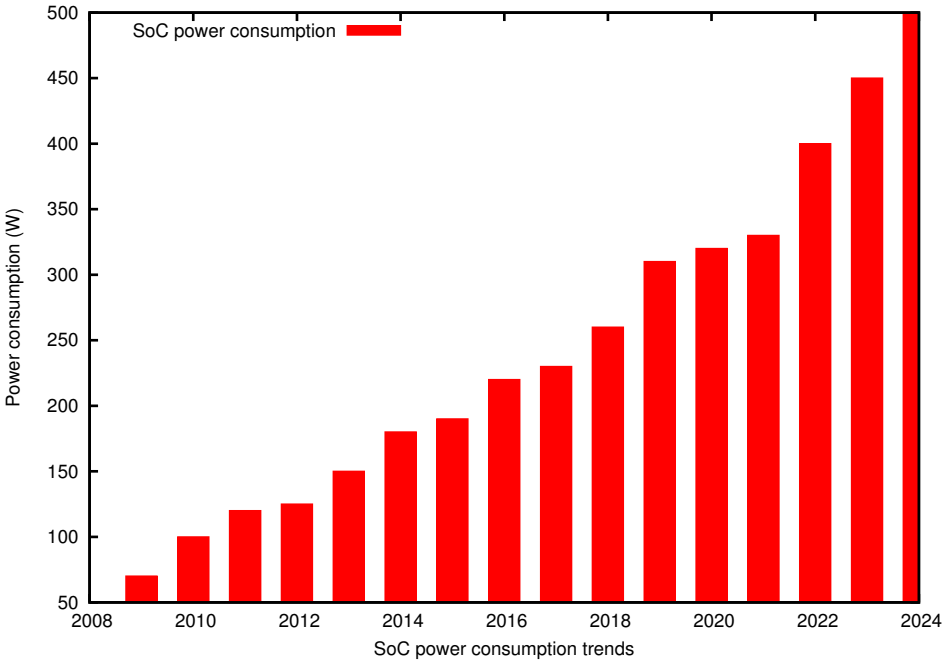

Figure 1.3: SoC power consumption trends

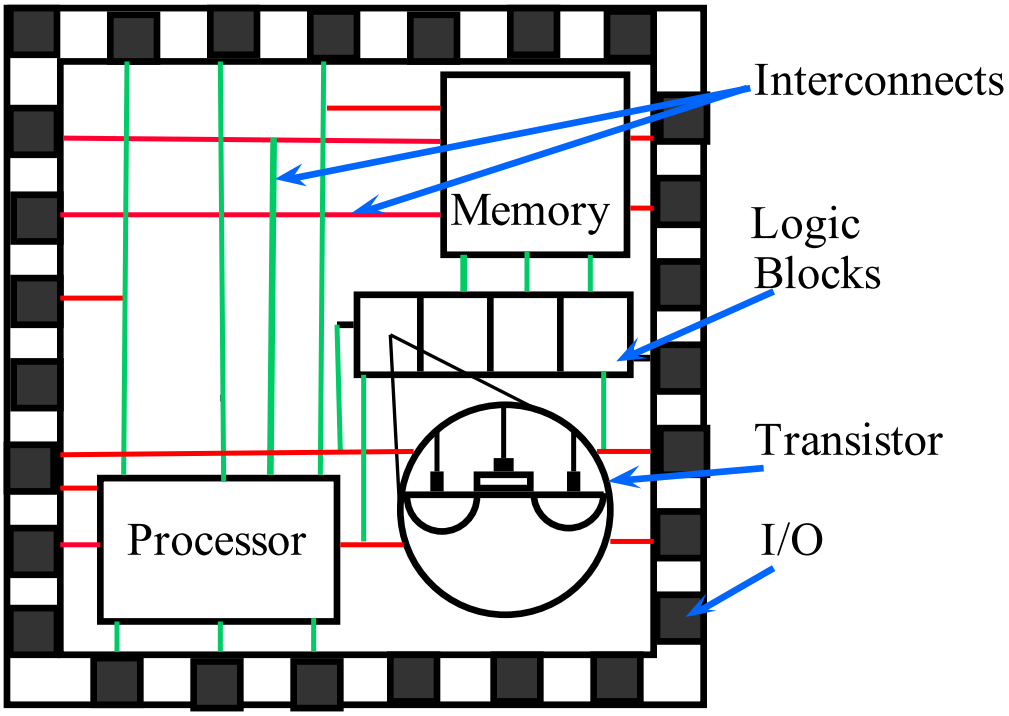

Figure 1.4: A typical micro-chip layout

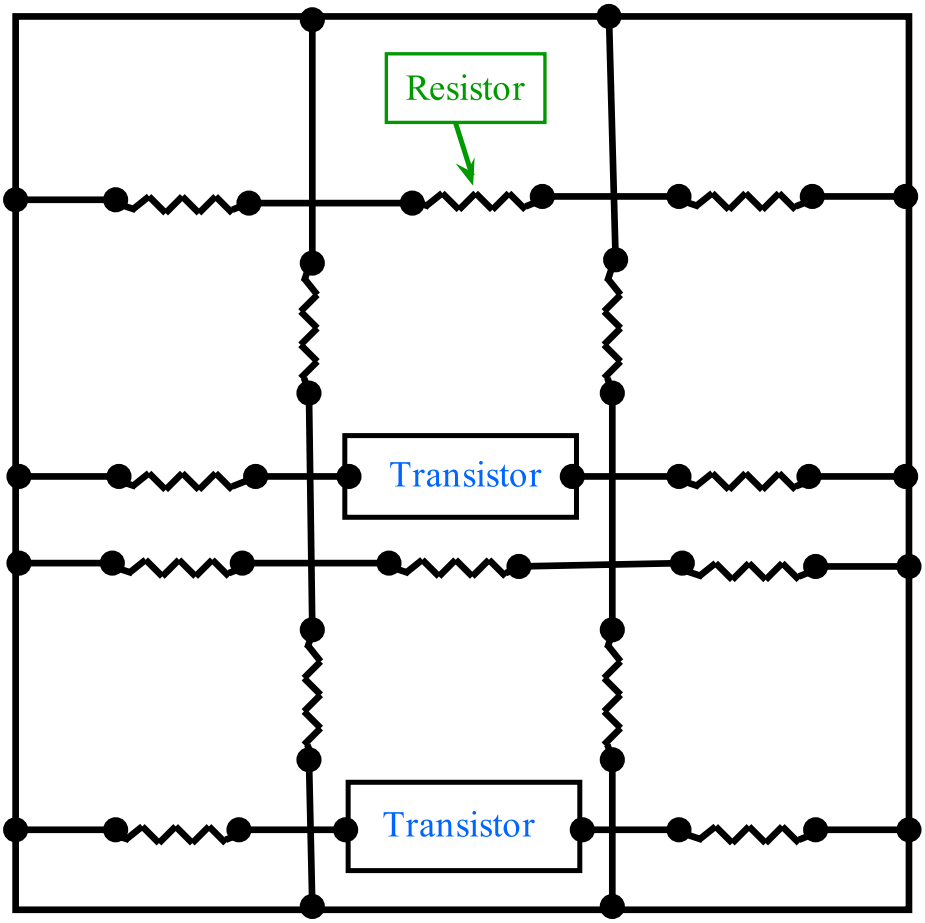

Figure 1.5: Interconnect-transistor network

The main objective of this research work presented in this thesis is to model the heating behavior of a transistor and to find an analytical solution for the temperature estimation. The research includes the following:

- To develop a mathematical model for the Joule heating due to switching drain current in a MOSFET channel.
- To find an analytical equation which solves the heat equation.
- To estimate the temperature profile of the channel.
- To develop a software package for estimating the channel temperature from the extracted device layout information and using information from a compact model. In this work, the SPICE BSIM3 format was chosen because of its relative simplicity.
- To develop an equivalent resistor network representation of the channel which can be integrated into the interconnect-transistor resistor network for full micro-chip thermal analysis.
- To validate the analytical solution using a numerical solution.

1.4 Scope and Organization

The scope of this thesis is limited to the research objectives, problem definition, solution and comparative studies with numerical solution of the heat equation using the finite difference methods. The thesis treats the heating problems in integrated

circuits and its solution is based on an analytical approach. Chapter 2 provides the background of the heating in the integrated circuits along with the problem definition of the MOSFET channel heating. Chapter 3 provides the mathematical model and the analytical solution for MOSFET channel temperature estimation. Chapter 4 describes HeatMOS©, a software package that has been developed through this research, implementing the analytical solution to estimate the channel temperature. Chapter 5 shows the results of HeatMOS© which are compared with numerical solutions using a finite difference solver. The conclusions and the future directions for this research are discussed in Chapter 6. The appendices provide other relevant informations such as different device parameters, SPICE netlist, and a pseudo code for the numerical solver.

Chapter 2

Heating in Integrated Circuits

The spatial variation of temperature across an integrated circuit (IC) is caused by charge carrier flow through the devices and the interconnects. The temperature variation in ICs is predominantly due to device heating and package level heat transport and is a subject of various chip-scale modeling approaches (Li et al., 2006). In the case of MOSFETs, the applied voltages at it its terminals create the longitudinal and transverse electric fields and charge carriers move from the source end to the drain end via drift and diffusion mechanisms (Park et al., 1991). Since the channel is a conducting path for the electric current, it can be considered as a resistor and the electric current flow in the channel leads to the Joule heating. The Joule heating causes the rise in the channel temperature.

Heat conduction in solids is governed by two principle mechanisms: diffusive heat conduction by electrons and heat conduction by lattice waves whose quanta are represented by phonons (Flik et al., 1992). Heat conduction by phonons in semiconductors is reviewed by Abeles(Abeles, 1963). In silicon the heat conduction is dominated by phonons (Sinha and Goodson, 2006). The hot electrons near the drain end transfer some energy to phonons and this creates a transient, non-

equilibrium, high temperature "hot spot" that effectively leads to higher thermal resistance (Sinha and Goodson, 2006).

Thermal conductivity analysis and conductivity measurements for silicon are provided by (Morris and Hust, 1961). The detailed thermal analysis at the dimensions less than a phonon mean free path (~100 nm) requires the transient solution of the Boltzmann transport equation (BTE), that may not be feasible for large, netlist-based, full micro-chip thermal analysis. The phonon transport of energy can be described by the BTE , which can capture the sub-continuum effects particularly important for short impulsive events such as ESD (electrostatic discharge). These sub-continuum effects are not modeled by the diffusion model of energy transfer. These sub-continuum effects should be accounted for during the transient analysis but in a steady state analysis the time-average temperature given by the diffusion model are appropriate.

The BTE for the phonons can be written as:

$$\frac{\partial e"}{\partial t} = -v \cdot \nabla e" + \frac{e"_{eq} - e"}{\tau_{phonon}} + q_{electron-phonon} \tag{2.1}$$

where $e"$ is the phonon energy per unit volume per unit solid angle, v is the phonon velocity, $e"_{eq}$ is the phonon equilibrium energy density, τ_{phonon} is the phonon scattering rate, $q_{electron-phonon}$ is the phonon energy absorption by hot electron.

The effective thermal conductivity of a complex silicon FET structure is technology-specific and could be obtained by the detailed modeling, but this is beyond the

scope of the thesis, which is aimed at a very compact model for netlist-based analysis. Our research is therefore directly applicable for the technology nodes above 180 nm (using the BSIM3 device model). The extension of this approach toward nanoscale technologies is discussed briefly in the Future Work.

2.1 Electrostatic Analogy of Heat Conduction

The analytical methods developed in this research to model heat conduction in the devices are based on analogous relationships between the form of equations for the heat conduction and the electrostatics. The fundamental analogies between the heat and the electrostatics are shown by comparison of the governing equations in Table 2.1. The temperature T in a conduction problem in the presence of a heat sources ϕ is governed by the analogy to Poisson's equation (Guass' Law) in the electrostatics. Similarly, the heat flow is analogous to the current flow in the electric circuits. In these equations, λ is the thermal conductivity in W/mK, ε is the permittivity in F/m, ϕ is the heat energy density in W/m^3, ρ is the electric charge density in C/m^3, T is the temperature in K, V is the electric potential in V, q is the heat flux in W/m^2, J is the electric current density in C/m^{2}s. Use of both analogies solves the heating problem (Labun, 2009).

Table 2.2 continues the analogy between electrical and thermal models by comparing material properties of thermal conductivity and electrical conductivity (Lide, 2004). Metals are good conductors of both heat and electrical current and dielectrics are poor conductors, although the ratio of conductance's is only two orders

Table 2.1: Thermal and electrostatic analogies

$\vec{\nabla} \cdot (\lambda \vec{\nabla} T) = -\phi$	$\vec{\nabla} \cdot (\varepsilon \vec{\nabla} V) = -\rho$
$\vec{q} = -\lambda \vec{\nabla} T$	$\vec{J} = -\sigma \vec{\nabla} V$

Table 2.2: Thermal and electrical conductivities (300 K)

Material	λ $(W m^{-1} K^{-1})$	σ $(\Omega^{-1} m^{-1})$
Cu	398	5.7×10^7
Al	237	3.7
W	174	1×10^7
Si (intrinsic)	83.5	10^{-3}
Si (doped)	60.5	10^{-3}
SiO_2	1.4	10^{-13}

of magnitude for heat. The tabulated values also show that the range in thermal conductivity properties is much smaller than the range in electrical conductivity. For example, the thermal conductivity of copper is four times of magnitude better than silicon, while the the electrical conductivity of copper is 10 orders of magnitude greater than silicon (Lide, 2004).

The analogy with Possion's equation leads to a capacitance/heat transfer coefficient analogy through the application of the divergence theorem to Poisson's equation. Table 2.3 Row 1 shows the identical construction of integral equations which in the

Table 2.3: Thermal and electrical versions of heat transfer or capacitance

$\int_{Volume} \overrightarrow{\nabla}(\lambda \overrightarrow{\nabla} T) d\Omega = \oint_{Area} (\lambda \overrightarrow{\nabla} T) d\overrightarrow{A} = \phi_{Volume}$	$\int_{Volume} \overrightarrow{\nabla}(\varepsilon \overrightarrow{V}) d\Omega = \oint_{Area} (\varepsilon \overrightarrow{\nabla} V) d\overrightarrow{A} = Q_{Volume}$
$\frac{1}{R_T} = \frac{\phi}{T}$	$C = \frac{Q}{V}$

electrical case are solved to obtain capacitance. The analogous thermal model for heat transfer shows that the reciprocal of the thermal resistance (R_T) is equal to the ratio of the heat density divided by the temperature difference across the material.

The relationship between the heat conduction and the electrostatics is completed using Ohm's law to relate the current flow with the heat flux. The Joule heating in a wire gives $I^2R = \phi_{Volume}$. The heat is conducted through the dielectrics according to the Ohm's Law analogy. Thus, capacitance tables (in homogeneous dielectrics) can be read as thermal resistance tables by multiplying by a constant factor.

2.2 Heat Equation

Before developing a heat model for a MOSFET channel, a model for heating in a resistor is derived first. Consider a resistor of uniform width and composition as shown in Figure 2.1. The resistor temperature variation over its cross-section is neglected. For metal interconnects embedded in a dielectric, this can be readily justified, since (by Table 2.2) the thermal conductivity within the resistor is much greater than the thermal conductivity of the surrounding insulator. In MOSFETs

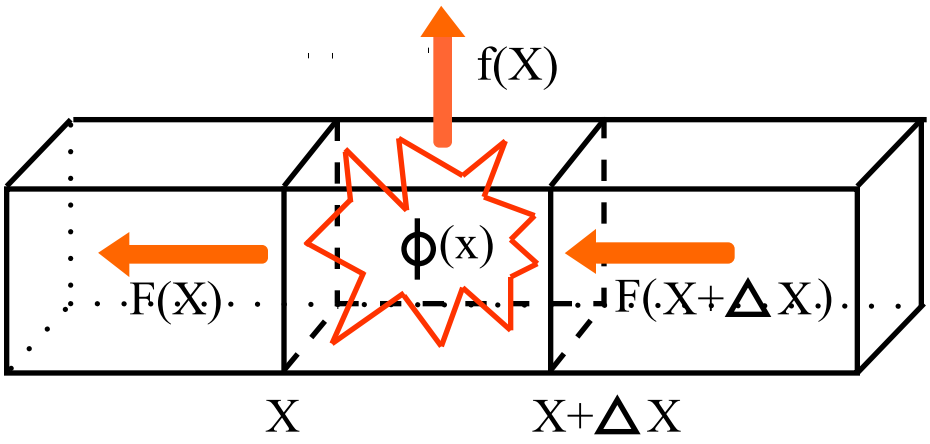

Figure 2.1: Conservation of heat (energy) within a differential slice of a resistor

the electric current is also confined to a well-defined region (the channel). Heat flow is confined by a poor thermal conductor above (the SiO_2 gate dielectric) and also below, in SOI devices. However, even in bulk MOSFETs, the useful approximation of a uniform temperature over the channel cross-section is not too far off the mark because of the localization of the heat source.

With reference to Figure 2.1, the heat per unit length, $mC_pT(x)\triangle x$ in a differential slice of a resistor segment of length $\triangle x$, where $T(x)$ is the temperature along the resistor's length, m is the mass per unit length, and C_p is the heat capacity. The time rate of change of the heat is then given by (Labun and Jagjitkumar, 2008)

$$mC_p\frac{\partial T}{\partial t}\triangle x = F(x+\triangle x) - F(x) + \phi(x)\triangle x - f(x)\triangle x \tag{2.2}$$

Where $F(x)$ is the diffusive heat flux. The heat flux is oriented along the resistor's length and is related to the temperature gradient by Fourier's law of heat conduction, including the "longitudinal" thermal conductance:

$$F(x) = G^{long} \frac{\partial T(x)}{\partial x} \tag{2.3}$$

The Joule heat per unit length is given by $\phi = I_{rms}^2 R$; R is the electrical resistance per unit length, assumed constant within a resistor; I_{rms} is the time-averaged rms current. The function $f(x)$ in equation (2.2) models the heat flux through the sides of the resistor to the surrounding environment at a temperature T^{ref}. If there is diffusive heat flux through the sides of the resistor to the local environment at some uniform, constant temperature T^{ref} (established, for example, by a full-chip temperature simulation including device heating), then one may define a "lateral" thermal conductance G^{lat} per unit length

$$f(x) = G^{lat} T(x) - T^{ref} \tag{2.4}$$

2.3 Heat Generation in MOSFETs

When the transistor is on and is in operation, the charge carriers move from the source to the drain and in this process these loose energy due to physical reasons such as collisions, scattering, phonon-electron interaction etc. The dissipated

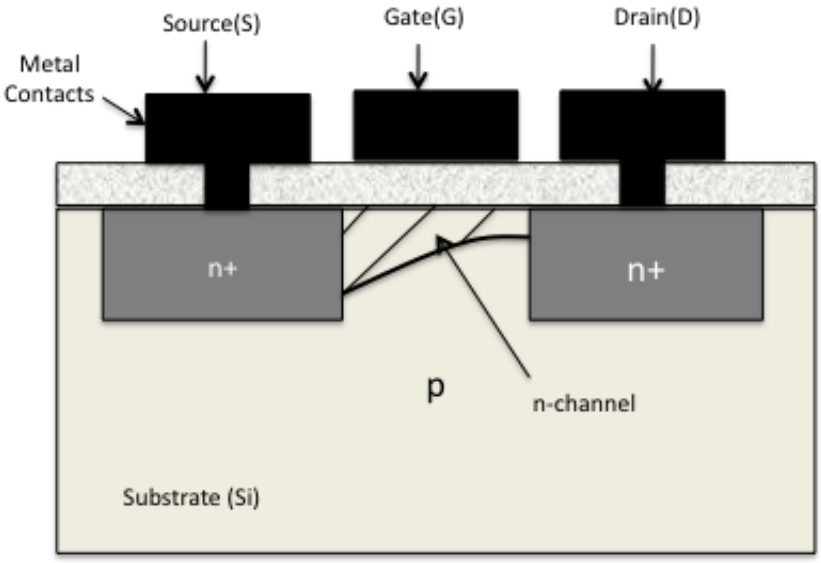

Figure 2.2: Cross-sectional view of an nMOS transistor

energy is released in the form of heat and leads to an increase in the device temperature. A cross-sectional view of a MOS transistor has been shown in Figure 2.2. The transistor is said to be in operation when there is a channel formed by applying appropriate voltages across substrate, source, drain, and gate terminals. The channel can be considered as a resistor of variable cross-sectional area, and the heat generated in the channel can be approximated by Joule heating similar to a resistor. Therefore, heat generation is concentrated in the region of the highest resistance, the pinched-off region of the channel near the drain end.

2.4 Summary

The heat generation in transistors has been presented with a focus on transistor channel heating. The basic equation for Joule heating has been explained, and it was shown that the heat equation is analogous to the solution of the Poisson equation in electrostatics. The basic heat equation for the Joule heating has been explained.

Chapter 3

Thermal Model and Analytical Solution

The one-dimensional heat equation (2.2) is applied to the thermal model of the MOSFET and solved analytically to give a closed-form expression for the channel temperature from the source to the drain. The thermal model uses the BSIM3 parameters.

3.1 BSIM3 MOSFET Model

BSIM3 is a physics-based, accurate, scalable, robust and predictive industry standard MOSFET SPICE model for circuit simulation and CMOS technology development. It was developed by the BSIM Research Group in the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley. BSIM3 is the industry-standard MOSFET model. The third iteration of BSIM3 Version 3 (commonly abbreviated as BSIM3v3), was established by SEMATECH as the first industry-wide standard model for MOSFETs in

December of 1996. The development of BSIM3 is based on Poisson's equation using the gradual channel approximation and coherent quasi 2D analysis, taking into account the effects of device geometry and process parameters. BSIM3 is appropriate for MOSFETs for 180 nm MOSFET technology and larger. BSIM3 models the following physical characteristics in MOSFET devices (Liu et al., 1999):

- Short and narrow channel effects on threshold voltage.
- Non uniform doping effects.
- Mobility reduction due to vertical field.
- Bulk charge effect.
- Velocity Saturation.
- Drain-induced barrier lowering (DIBL).
- Channel length modulation (CLM).
- Substrate current induced body effect (SCBE).
- Sub-threshold conduction.
- Source/Drain parasitic resistances.

BSIM3 uses a group device extraction strategy for parameter extraction. This requires measured data from devices with different geometries. All devices are measured under the same bias conditions. The BSIM3 device parameters for a 180 nm CMOS technology have been used in this research. The model parameters are given in appendix A.

3.2 MOSFET Channel

A simplified model of the MOSFET channel accounts for many characteristics of MOSFET devices and is sufficient for the compact thermal model developed in this thesis. The channel is a cloud of free charge carriers beneath the gate surface which conducts electric current. In the case of nMOS, the electron cloud forms the channel. The electron density is greater at the source end compared to the drain end and decreases towards the drain end (Masu and Tsubouchi, 1994). An example of the typical IV characteristics of an nMOS transistor is shown in Figure 3.1 (Weste and Harris, 2004). The electric current increases as we increase the drain voltage and after a certain voltage, the current becomes constant and the channel is said to be pinched off. Initially when there is no drain voltage, the electrons are attracted towards the positive gate voltage (enhancement mode n-channel MOSFET) and it is clear that the Joule heat constitutes only a small part of the micro-chip power consumption as compared to the power consumption due to switching activity. When the gate voltage is greater than the threshold voltage and the drain voltage is less than the gate voltage, the transistor is turned on, and a channel has been created which allows current to flow between the drain and the source. The MOSFET operates like a resistor controlled by the gate voltage relative to both the source and the drain voltages. Now, if the drain voltage is increased and becomes greater than the gate voltage, the transistor is said to be in the saturation or the active mode of operation. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is through a broad, three-dimensional channel and the current extends away from the interface. The onset of this region is also known as pinch-off to indicate the lack of channel region

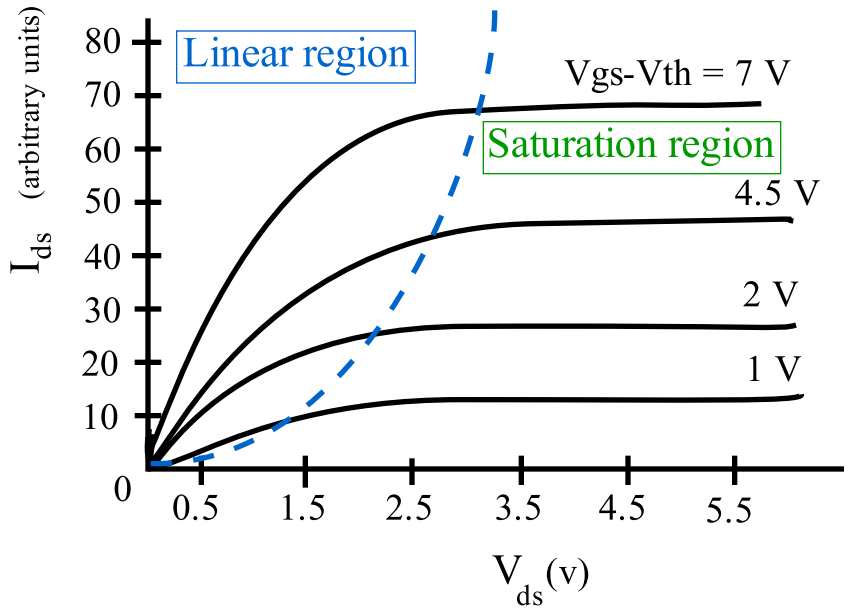

Figure 3.1: A typical I-V characteristic of an nMOS transistor

near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage.

Since the channel provides a conducting path for electric current, it can be considered as a resistor. The cross-sectional area of this resistor is higher at the source end and continuously decreases towards the drain end. When the gate voltage is greater than the threshold voltage, $V_{gs} > V_{th}$ and $V_{ds} \geq (V_{gs} - V_{th})$, where V_{ds} is the drain voltage, the channel depth at drain end decreases to almost zero, and the channel is said to be pinched-off (Weste and Harris, 2004). Beyond the pinch-off, the depletion region around the drain end provides a path for the drain current to flow. In the channel thermal model the region between the pinch-off point and the drain end

can be considered as a region of uniform cross-section. The conductivity of this channel resistor depends on complex physical parameters including area, doping concentration, mobility of charge carriers etc. The channel is controlled between the oxide layer and the substrate layer in vertical direction, and controlled between the source well and the drain well in horizontal direction as shown in Figure 3.3.

Let us consider the case of an nMOS transistor. Initially, when the gate voltage V_{gs} is less than the threshold voltage V_{th}, and the drain voltage is at the same voltage as the source, an inversion layer is formed beneath the gate, and the channel is said to exist between the source and the drain. The inversion layer can be assumed to have a uniform cross-sectional area from the source end to the drain end of the transistor. Now, if the gate voltage is increased beyond the threshold voltage of the transistor, a sufficient number of electrons accumulate in the inversion layer to conduct electric current. The electric current increases with the increase in the gate voltage. Since the drain and the source are at same voltage at this point, the height of the inversion layer, and hence the channel remain uniform (Weste and Harris, 2004). Now, if the drain voltage is increased, the voltage causes an electric current to flow between the source and the drain. The electric current flowing in the channel I_{ds} will be proportional to the effective gate voltage $V_{gs} - V_{th}$, and to the voltage V_{ds} which causes I_{ds} to flow. Under these conditions the channel is said to be in the linear or ohmic region. As V_{DS} continues to increase, the channel height near the drain end starts decreasing. However, in the linear mode of operation, the channel height at the drain end is approximately the same as that at the source end ($H_P \backsimeq 0.99H_O$). If $V_{ds} > (V_{gs} - V_{th})$, I_{ds} no longer increases linearly and becomes constant. The transistor is said to operate in the saturation region or in

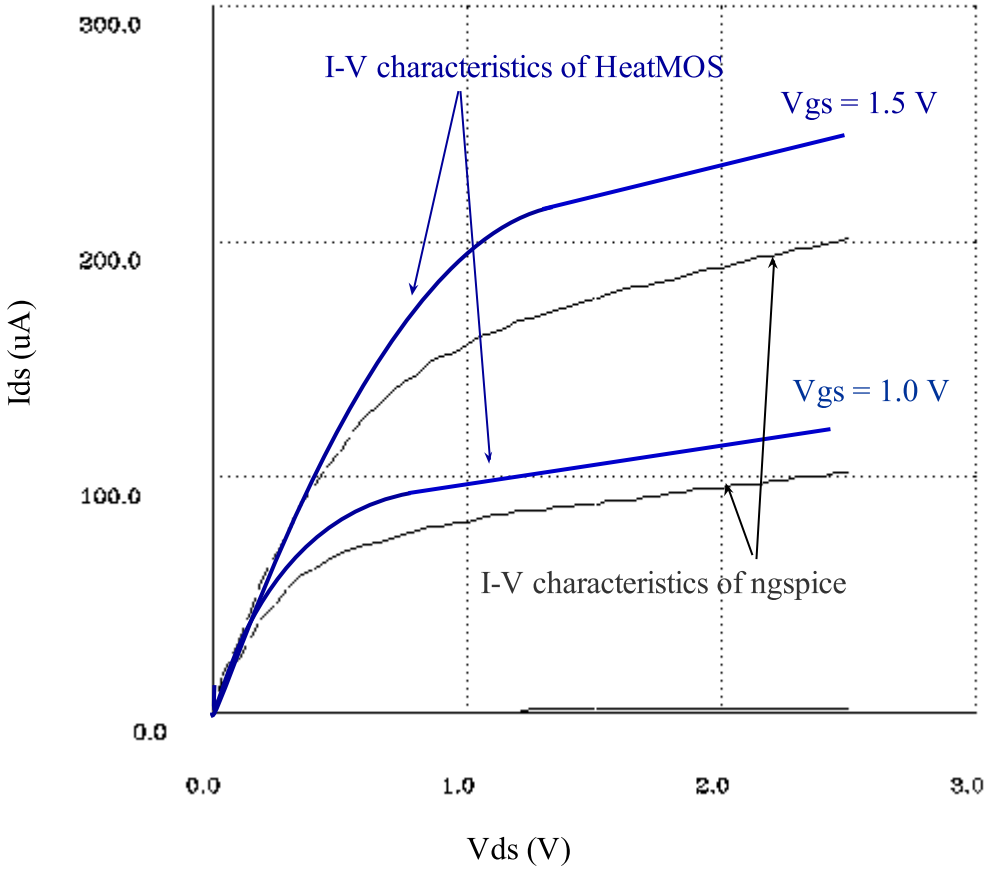

Figure 3.2: A comparison for I-V characteristics of an nMOS transistor

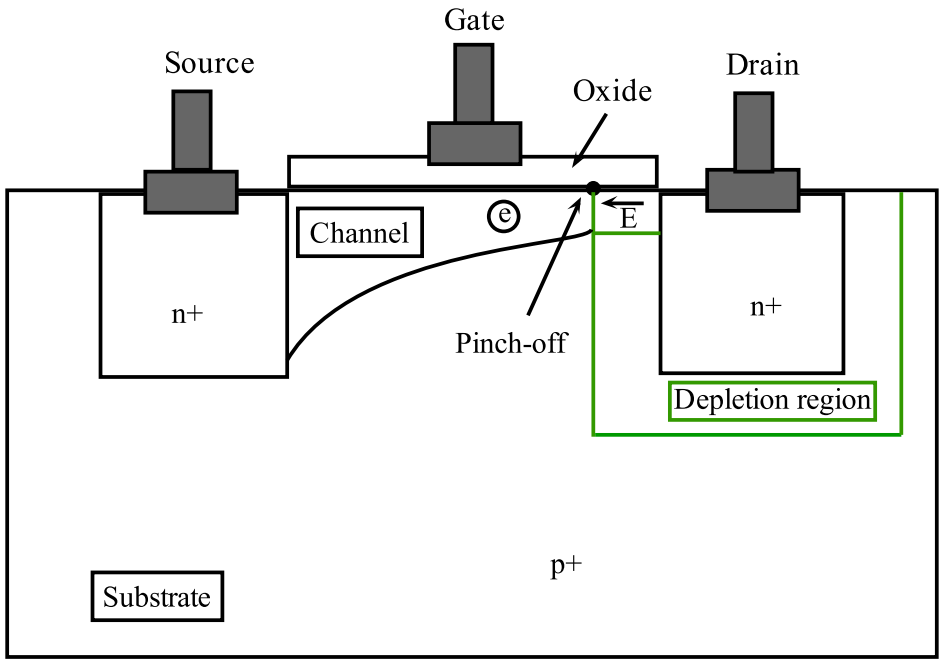

Figure 3.3: Simplified 2-D cross-section of an nMOS transistor

the on state. Other second order effects in the BSIM3 model such as drain-induced barrier lowering (DIBL), substrate current induced body effects (SCBE) have not been incorporated in HeatMOS© to calculate effective drain current, which are typically modeled in industrial quality SPICE simulators. A comparison of the the I-V characteristics of simplified device model used in HeatMOS© with the full BSIM3 model (ngspice simulator) is shown in Figure 3.2. The saturation current calculation equation will be explained in section 5.2.

3.2.1 Channel Geometry for Thermal Model

Figure 3.3 shows the channel region in a MOSFET. In the saturation region of operation the channel shrinks near the drain end and the drain current becomes almost constant. The drain current flows through the depletion region at the drain end. For the thermal model in saturation mode the channel is modeled as two separate regions.

- Region 1:

  Region 1 is a channel of constant width W_{eff} and non-uniform height which tapers from the source end to the pinch-off point (Figure 3.4). This region is approximated by an exponential function of the form $y = Ae^{-\alpha x}$ where where y is the vertical height and x is the horizontal length of the channel. An exponential function is selected for the model to lead to tractable analytic results and differs from the linear model used for the gradual channel approximation used to develop the electrical model for MOSFETs. However, the parameters A and α in the exponential model are determined from the BSIM3 model parameters and are matched for the operating point of the device.

  If L_1 is the length of the channel between the source end and the pinch-off point, H_O is the height of the channel at the source end and H_P is the height of the channel at the pinch-off point then

$$x = 0 \Rightarrow y = H_O$$

$$x = L_1 \Rightarrow y = H_P$$

$$H_P = H_O e^{-\alpha L_1} \Rightarrow \alpha = \frac{1}{L_1} ln\left(\frac{H_O}{H_P}\right)$$

$$y = H_O e^{-\left\{\frac{1}{L_1} ln\left(\frac{H_O}{H_P}\right)\right\} x} \tag{3.1}$$

- Region 2:

  Region 2 models the thermal conduction through the depletion region of the pinched off channel. In this region, the channel cross-section is uniform and has width W_{eff} and height H_P. The channel length in region 2 is denoted as L_2.

If L is the total length of the channel then

$$L = L_1 + L_2$$

Figure 3.4 shows the 3D view of channel formed beneath the gate.

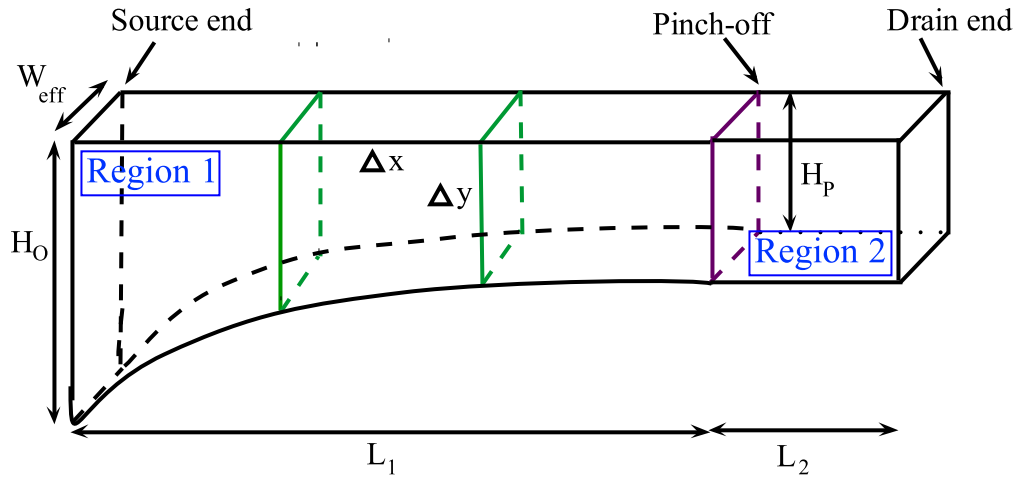

Figure 3.4: 3D view of the channel geometry for thermal model

3.2.2 Electrical Resistance

The conduction channel formed beneath the oxide layer is of non-uniform cross-sectional area in nature from the source end to the pinch-off point and has uniform cross-sectional area from the pinch-off point to the drain end.

The resistance of non-uniform cross-sectional area of region 1 can be approximated by integrating the resistance of a differential slice over the length from 0 to L_1:

$$R_1 = \int_0^{L1} \frac{\rho e^{\alpha x}}{W_{eff} H_O} dx = \frac{\rho}{W_{eff} H_O \alpha} \left(e^{\alpha L_1} - 1 \right) \tag{3.2}$$

$$\alpha = \frac{1}{L_1} ln \left(\frac{H_O}{H_P} \right) \tag{3.3}$$

$$L_{eff} = L_1 + L_2 \tag{3.4}$$

where,

ρ = Electrical resistivity

H_O = Height of channel at source end

H_P = Height of channel at pinch-off point

W_{eff} = Effective channel width

L_1 = Length of channel between source end and pinch-off point

L_2 = Length of channel between pinch-off point and drain end

L_{eff} = Effective channel length

The effective channel length and width can be approximated by (Liu et al., 1999)

$$L_{eff} = L_{Drawn} - 2dL \tag{3.5}$$

$$W_{eff} = W_{Drawn} - 2dW \tag{3.6}$$

$$dW = W_{int} + \frac{W_l}{L^{W_{ln}}} + \frac{W_w}{W^{W_{wn}}} + \frac{W_{wl}}{L^{W_{ln}} W^{W_{wn}}} \tag{3.7}$$

$$dL = L_{int} + \frac{L_l}{L^{L_{ln}}} + \frac{L_w}{W^{L_{wn}}} + \frac{L_{wl}}{L^{L_{ln}} W^{L_{wn}}} \tag{3.8}$$

where,

L_{Drawn} = Layout drawn length of transistor.

W_{Drawn} = Layout drawn width of transistor.

$W_{int}, L_{int}, W_l, W_w, W_{wl}, W_{wn}, L_l, L_w, L_{wn}, L_{wl}$ = BSIM3 parameters.

The electrical resistivity of the channel can be approximated as

$$\rho = \frac{1}{W_{eff} C_{ox} \mu_{eff}} \tag{3.9}$$

where,

C_{ox} = Capacitance of oxide layer.

μ_{eff} = Effective mobility of charge carriers.

Region 2 has a uniform cross-sectional area. This can be considered as a uniform bar of length L_2, width W_{eff}, and height H_P. Its resistance is given by

$$R_2 = \frac{\rho L_2}{W_{eff} H_P} \tag{3.10}$$

3.2.3 Channel Height Models

Initially when the channel starts taking its shape an inversion charge layer is formed beneath the oxide layer. The charge accumulates beneath the gate and forms an approximately uniform layer of a certain height and width from the source end to the drain end. It can also be approximated that when the channel takes on its non-uniform shape in the saturation region of operation, the drain end of the channel shrinks, while the source end of the channel remains same. The drain end of the channel shrinks to the height, H_P, the height at the pinch-off point. The height of the channel at the source end can be approximated by the thickness of the inversion layer (Masu and Tsubouchi, 1994).

The height of the channel at the source end is

$$H_O = t_{inv} = \frac{kT}{\sqrt{\frac{\varepsilon\varepsilon_o}{2qN_A\phi_s}}} \tag{3.11}$$

$$\phi_s = 2\frac{kT}{q} ln\left(\frac{N_A}{n_i}\right) \tag{3.12}$$

where,

k = Boltzmann's constant

T = Temperature

ε = Dielectric constant

ε_o = Permittivity of free space

q = Electron charge

N_A= Substrate doping concentration

n_i = Intrinsic silicon concentration

ϕ_s= Surface potential

We can approximate the height of the channel at the pinch off point H_P by the following method.

$$R_1 + R_2 = \frac{V_{DS}}{I_{sat}} \tag{3.13}$$

$$\frac{\rho\left(e^{\alpha L_1} - 1\right)}{W_{eff} H_O \alpha} + \frac{\rho L_2}{W_{eff} H_P} = \frac{V_{DS}}{I_{sat}}$$

Under the approximation $H_P <<< H_O$,

$$H_P = \frac{\rho L_2 I_{sat}}{V_{DS} W_{eff}} \tag{3.14}$$

where

I_{sat} = Electric current in saturation region of operation

V_{DS} = Drain-Source voltage

The height of the channel at the drain end is the same as at the pinch-off point, H_P, as it is assumed that the channel becomes uniform in nature from the pinch-off point to the drain end.

3.2.4 Channel Length Models

The channel length between the pinch-off point and the drain can be calculated using the channel length modulation approximation (Park et al., 1991).

The length of the channel between the pinch-off point to the drain is

$$L_2 = \frac{V_{DS} - VDS'}{E_L} \tag{3.15}$$

where

$E_L = \sqrt{\frac{qN_a(V_{DS}-VDS')}{2\varepsilon\varepsilon_O}}$

$VDS' \backsimeq -v_{sat}L_{eff}/\mu_{eff}$

v_{sat} = Saturation velocity of charge carriers

So, the channel length between the source end and the pinch-off point is

$$L_1 = L_{eff} - L_2 \tag{3.16}$$

3.2.5 Thermal Conductance

There are two kinds of thermal conductances: lateral thermal conductance and longitudinal thermal conductance. The conduction channel is formed beneath the oxide layer. The substrate can be approximated as having a uniform background temperature T^{ref}. The lateral thermal conductance must be taken to both the gate electrode above and a thermal reference somewhere in the substrate below. These may be combined into a single lateral conductance to a single, averaged reference temperature. Given the relative short channel length, when compared to the distant reference temperature (e.g substrate), the small variation in the height of the channel compared to that great distance is negligible. Therefore, the variation of thermal conductance along the height of the channel can be considered negligible. The lateral thermal conductance (G^{lat}) can be considered uniform along the length of the channel. For complex device structures a uniform, effective lateral thermal conductivity could be calibrated from detailed 2D or even 3D thermal conduction simulations.

The longitudinal thermal conductance (G^{long}) vary along the length of the channel and is of concern. Since the height of the channel is not uniform, a tractable solution to the heat equation arises if we can drive an expression of average thermal conductance in a similar manner to the electrical resistance of the channel. This weights the thermal conductance according to the localization of the heat source.

The average longitudinal thermal conductance is

$$G_{avg}^{long} = \frac{1}{L_{eff}} \int_0^{L_{eff}} G(x)dx \tag{3.17}$$

where L_{eff} is the effective channel length.

The longitudinal thermal conductance along the length is

$$G^{long}(x) = G_O e^{\gamma x} \tag{3.18}$$

where

$\gamma = -\frac{1}{L_{eff}} ln\left[\frac{G_O}{G_L}\right]$

G_O = Thermal conductance per unit length at source end (i.e. when $x = 0 \Rightarrow G^{long}(x = 0) = G_O$).

G_L = Thermal conductance per unit length at drain end (i.e. when $x = L \Rightarrow G^{long}(x = L) = G_L$).

The solution to the equation 3.17 is

$$G_{avg}^{long} = \frac{G_O}{\gamma L_{eff}} \left[e^{\gamma L_{eff}} - 1\right] \tag{3.19}$$

If λ is the thermal conductivity of channel, then $G_O = \frac{H_O W_{eff}}{\lambda}$ and $G_L = \frac{H_P W_{eff}}{\lambda}$.

2.2

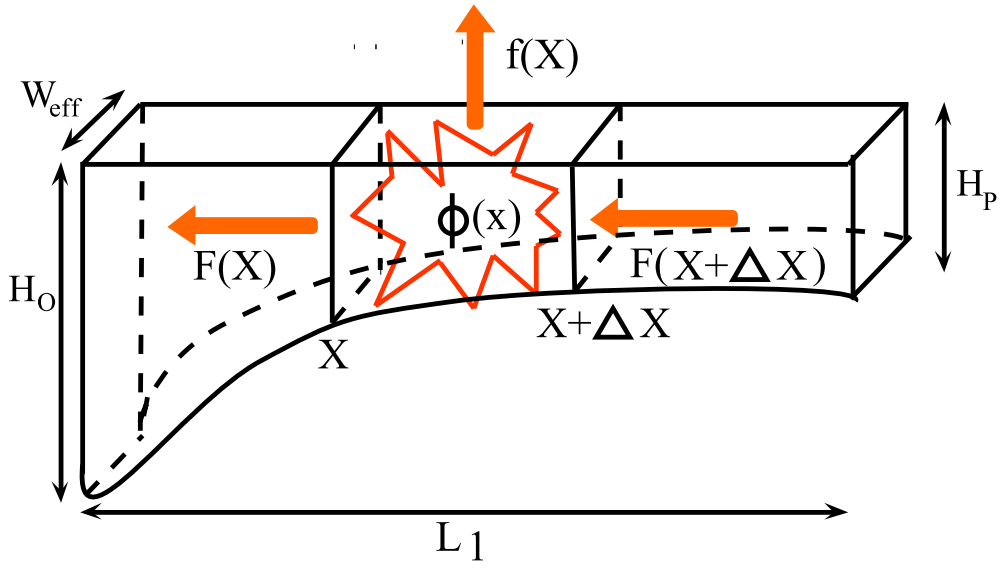

Figure 3.5: 3D view of region 1 of the channel

3.3 Solution of the Heat Equation

The basic heat equation 2.2 is solved for both regions in the following sections.

3.3.1 Region 1: Non-uniform cross-sectional area

Figure 3.5 shows region 1 of the channel.

For a differential length $\triangle x$ of the channel,

$$\phi(x)\triangle x = I_{DS}^2 R(x)\triangle x$$

$$R(x)\triangle x = \frac{\rho \triangle x}{W_{eff} H_O} e^{\alpha x}$$

where I_{DS} is the drain current.

The heat flux can be written as

$$F(x) = G_{avg}^{long} \frac{\partial T(x)}{\partial x}$$

$$F(x+\triangle x) = G_{avg}^{long} \frac{\partial T(x+\triangle x)}{\partial x}$$

$$f(x) = G^{lat} \left(T(x) - T^{ref} \right)$$

In the limit when $\triangle x \to 0$, the basic heat equation 2.2 takes the form of the 2nd order non-homogeneous differential equation.

$$G_{avg}^{long} \frac{d^2 T}{dx^2} - G^{lat} \left(T(x) - T^{ref} \right) + \frac{I_{DS}^2 \rho}{W_{eff} H_O} e^{\alpha x} = 0 \tag{3.20}$$

If the temperature function for region 1 is $T_1(x)$, equation 3.20 can be written as

$$G_{avg}^{long} \frac{d^2 T_1}{dx_1^2} - G^{lat} \left(T_1(x_1) - T^{ref} \right) + \frac{I_{DS}^2 \rho}{W_{eff} H_O} e^{\alpha x_1} = 0 \tag{3.21}$$

The solution of non-homogeneous differential equation 3.21 can be written as

$$T_1(x_1) = C_1 e^{\xi_1 x_1} + C_2 e^{-\xi_1 x_1} + T^{ref} - \frac{\Psi^2}{\alpha^2 - \xi_1^2} e^{\alpha x_1} \tag{3.22}$$

where

$$\xi_1 = \sqrt{\frac{G^{lat}}{G^{long}_{avg}}}$$

$$\Psi = \sqrt{\frac{I^2_{sat}\rho}{W_{eff} H_O G^{long}_{avg}}}$$

$$K_1 = \frac{\Psi^2}{\alpha^2 - \xi_1^2}$$

C_1 and C_2 are constants whose values will be determined.

3.3.2 Region 2: Uniform cross-sectional area

Figure 3.6 shows the 3D view of region 2 of the channel. The total resistance in region 2 is denoted as R_2.

For a differential length $\triangle x$ of the channel

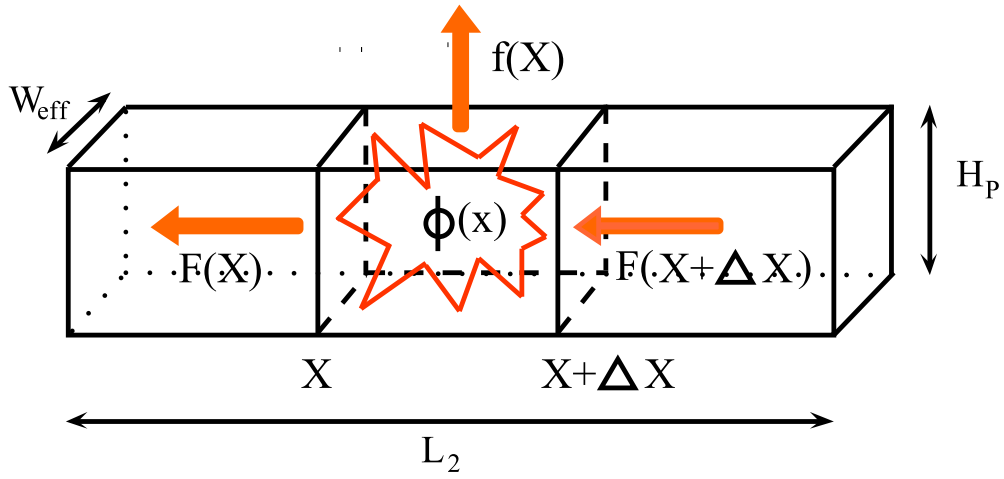

Figure 3.6: 3D view of the region 2 of the channel

$$\phi(x)\triangle x = I_{DS}^2 \left(\frac{R_2}{L_2}\right)\triangle x$$

The heat flux can be written as

$$F(x) = G_{avg}^{long}\frac{\partial T(x)}{\partial x}$$

$$F(x+\triangle x) = G_{avg}^{long}\frac{\partial T(x+\triangle x)}{\partial x}$$

$$f(x) = G^{lat}\left(T(x) - T^{ref}\right)$$

In the limit when $\triangle x \to 0$, the basic heat equation 2.2 takes the form of the second-order non-homogeneous differential equation 3.23.

$$G_{avg}^{long}\frac{d^2T}{dx^2} - G^{lat}\left(T(x) - T^{ref}\right) + I_{DS}^2 R_2 = 0 \tag{3.23}$$

If the temperature function of region 2 is $T_2(x)$, the equation 3.23 can be written as

$$G_{avg}^{long}\frac{d^2T_2}{dx_2^2} - G^{lat}\left(T_2(x_2) - T^{ref}\right) + I_{DS}^2 R_2 = 0 \tag{3.24}$$

The solution of differential equation 3.24 can be written as

$$T_2(x_2) = D_1 e^{\xi_2 x_2} + D_2 e^{-\xi_2 x_2} + \frac{\beta}{\xi_2^2} \tag{3.25}$$

where

$$\xi_2 = \sqrt{\frac{G_2^{lat}}{G_{avg}^{long}}}$$

$$\beta = -\frac{G_2^{lat}}{G_{avg}^{long}}T^{ref} - \frac{I_{DS}^2}{G_{avg}^{long}}R_2$$

$$K_2 = \frac{\beta}{\xi_2^2}$$

D_1 and D_2 are constants whose values will be determined using the boundary conditions.

3.3.3 Boundary Conditions and Complete Solution

The channel is between the source end and the drain end. The end point temperatures are determined by the boundary conditions. If the temperature of the source end is T_O and the drain end is T_L, then the two boundary conditions can be written as

$$T_1(x_1)\mid_{x_1=0} = T_O \tag{3.26}$$

$$T_2(x_2)\mid_{x_2=L_2} = T_L \tag{3.27}$$

Since the channel is one entity, the pinch-off point is a virtual point. The temperature at the pinch-off point as determined by equation 3.22 should be the same as it is determined by equation 3.25. Further the heat flux leaving region 1 enters into region 2. These facts give us two more conditions:

$$T_1(x_1)\mid_{x_1=L_1} = T_2(x_2)\mid_{x_2=0} \tag{3.28}$$

$$G_{avg}^{long}\frac{dT_1}{dx_1}\mid_{x_1=L_1} = G_{avg}^{long}\frac{dT_2}{dx_2}\mid_{x_2=0} \tag{3.29}$$

Using equations 3.22, 3.25, 3.26, 3.27, 3.28, and 3.29, the unknown coefficients, C_1, C_2, D_1, and D_2 can be calculated. The values of these coefficients are given below.

$$T_O = C_1 + C_2 + T^{ref} - \frac{\Psi^2}{\alpha^2 - \xi_1^2} \tag{3.30}$$

$$T_L = D_1 e^{\xi_2 L_2} + D_2 e^{-\xi_2 L_2} + \frac{\beta}{\xi_2^2} \tag{3.31}$$

$$C_1 e^{\xi_1 L_1} + C_2 e^{-\xi_1 L_1} + T^{ref} - \frac{\Psi^2}{\alpha^2 - \xi_1^2} = D_1 + D_2 + \frac{\beta}{\xi_2^2} \tag{3.32}$$

$$G_{avg}^{long}\left(C_1\xi_1 e^{\xi_1 L_1} - C_2\xi_1 e^{-\xi_1 L_1} - \alpha\frac{\Psi^2}{\alpha^2 - \xi_1^2}e^{\alpha L_1}\right) = G_{avg}^{long}\left(D_1\xi_2 - D_2\xi_1\right) \tag{3.33}$$

$$C_1 = C_1^{'} - C_1^{''} \tag{3.34}$$

$$D_1 = D_1^{'} - D_1^{''} \tag{3.35}$$

where

$$C_1^{'} = \frac{\left(\xi_2 + \xi_2 e^{2\xi_2 L_2}\right)}{\left(e^{\xi_1 L_1} - e^{-\xi_1 L_1}\right)\left(1 + e^{2\xi_2 L_2}\right)\xi_2 - \left(e^{\xi_1 L_1} + e^{-\xi_1 L_1}\right)\left(1 - e^{2\xi_2 L_2}\right)} \times \left\{ T_L e^{\xi_2 L_2} - (T_O - T^{ref}) e^{-\xi_1 L_1} - T^{ref} + \frac{\Psi^2}{\alpha^2 - \xi_1^2}(e^{\xi_1 L_1} - e^{-\xi_1 L_1}) + \frac{\beta}{\xi_2^2}(1 - e^{\xi_2 L_2}) \right\}$$

$$D_1^{'} = \frac{\left(e^{\xi_1 L_1} + e^{-\xi_1 L_1}\right)}{\left(e^{\xi_1 L_1} - e^{-\xi_1 L_1}\right)\left(1 + e^{2\xi_2 L_2}\right)\xi_2 - \left(e^{\xi_1 L_1} + e^{-\xi_1 L_1}\right)\left(1 - e^{2\xi_2 L_2}\right)} \times \left\{ T_L e^{\xi_2 L_2} - (T_O - T^{ref}) e^{-\xi_1 L_1} - T^{ref} + \frac{\Psi^2}{\alpha^2 - \xi_1^2}(e^{\xi_1 L_1} - e^{-\xi_1 L_1}) + \frac{\beta}{\xi_2^2}(1 - e^{\xi_2 L_2}) \right\}$$

$$C_1^{''} = \frac{\left(1 - e^{2\xi_1 L_1}\right)}{\left(e^{\xi_1 L_1} - e^{-\xi_1 L_1}\right)\left(1 + e^{2\xi_2 L_2}\right)\xi_2 - \left(e^{\xi_1 L_1} + e^{-\xi_1 L_1}\right)\left(1 - e^{2\xi_2 L_2}\right)} \times \left\{ (T_O - T^{ref})\xi_1 e^{-\xi_1 L_1} - T_L e^{\xi_2 L_2}\xi_2 + \frac{\Psi^2}{\alpha^2 - \xi_1^2}(\alpha e^{\alpha L_1} + \xi_1 e^{-\alpha L_1}) + \frac{\beta}{\xi_2^2}\xi_2 e^{\xi_2 L_2} \right\}$$

$$D_1^{''} = \frac{\left(e^{\xi_1 L_1} - e^{-\xi_1 L_1}\right)}{\left(e^{\xi_1 L_1} - e^{-\xi_1 L_1}\right)\left(1 + e^{2\xi_2 L_2}\right)\xi_2 - \left(e^{\xi_1 L_1} + e^{-\xi_1 L_1}\right)\left(1 - e^{2\xi_2 L_2}\right)} \times \left\{(T_O - T^{ref})\xi_1 e^{-\xi_1 L_1} - T_L e^{\xi_2 L_2}\xi_2 + \frac{\Psi^2}{\alpha^2 - \xi_1^2}(\alpha e^{\alpha L_1} + \xi_1 e^{-\alpha L_1}) + \frac{\beta}{\xi_2^2}\xi_2 e^{\xi_2 L_2}\right\}$$

$$C_2 = T_O - C_1 - T^{ref} + \frac{\Psi^2}{\alpha^2 - \xi_1^2}$$

$$D_2 = T_L e^{\xi_2 L_2} - D_1 e^{2\xi_2 L_2} - \frac{\beta}{\xi_2^2} e^{\xi_2 L_2}$$

The temperature of the channel along its length from the source end to the drain end can be written as

$$T(x) = \begin{cases} T_1(x_1), & 0 \le x_1 \le L_1 for 0 \le x \le L_1 \\ T_2(x_2), & 0 \le x_2 \le L_2 for L_1 \le x \le L \end{cases} \tag{3.36}$$

where

$$L = L_1 + L_2 \tag{3.37}$$

3.3.4 The Average Channel Temperature

The average temperature of the channel can be found by integrating the temperature function over the length and by dividing the total length.

$$T_{avg} = \frac{1}{2}\left[\frac{1}{L_1}\int_0^{L_1} T_1(x_1)dx_1 + \frac{1}{L_2}\int_0^{L_2} T_2(x_2)dx_2\right]$$

$$T_{avg} = \frac{1}{2}\left[\frac{1}{L_1}\int_0^{L_1}\left\{C_1 e^{\xi_1 x_1} + C_2 e^{-\xi_1 x_1} + T^{ref} - K_1 e^{\alpha_1 x_1}\right\}dx_1 + \frac{1}{L_2}\int_0^{L_2}\left\{D_1 e^{\xi_2 x_2} + D_2 e^{-\xi_2 x_2} + K_2\right\}dx_2\right]$$

$$T_{avg} = \frac{1}{2L_1}\left\{\frac{C_1}{\xi_1}\left(e^{\xi_1 L_1} - 1\right) - \frac{C_2}{\xi_1}\left(e^{-\xi_1 L_1} - 1\right) + L_1 T^{ref} - \frac{K_1}{\alpha_1}\left(e^{\alpha_1 L_1} - 1\right)\right\} + \frac{1}{2L_2}\left\{\frac{D_1}{\xi_2}\left(e^{\xi_2 L_2} - 1\right) - \frac{D_2}{\xi_2}\left(e^{-\xi_2 L_2} - 1\right) + K_2 L_2\right\}$$

3.3.5 The Maximum Channel Temperature

If T_1^{max} is the maximum temperature given by the temperature function $T_1(x)$ and T_2^{max} is the maximum temperature given by the temperature function $T_2(x)$,

$$\frac{dT_1}{dx_1} = 0 \Rightarrow x_1 = x_1^{max}$$

$$T_1^{max} = T_1(x_1)\mid_{x_1=x_1^{max}}$$

$$\frac{dT_2}{dx_2} = 0 \Rightarrow x_2 = x_2^{max}$$

$$T_2^{max} = T_2(x_2)\mid_{x_2=x_2^{max}}$$

where $0 \leq x_1^{max} \leq L_1$ and $0 \leq x_2^{max} \leq L_2$.

The maximum channel temperature T_{max} at a distance x_{max} along the length of the channel from the source end to the drain end is the greatest of T_1^{max} and T_2^{max}.

If $T_1^{max} \geq T_2^{max} \Rightarrow T_{max} = T_1^{max}$ and $x_{max} = x_1^{max}$.

If $T_2^{max} > T_1^{max} \Rightarrow T_{max} = T_2^{max}$ and $x_{max} = L_1 + x_2^{max}$.

For x_2^{max}:

$$D_1\xi_2 e^{\xi_2 x_2^{max}} - D_2\xi_2 e^{-\xi_2 x_2^{max}} = 0$$

$$x_2^{max} = \frac{1}{2\xi_2} ln\left[\frac{D_2}{D_1}\right]$$

For x_1^{max} :

$$C_1\xi_1 e^{\xi_1 x_1^{max}} - C_2\xi_1 e^{-\xi_1 x_1^{max}} - K_1\alpha_1 e^{\alpha_1 x_1^{max}} = 0$$

The above equation for x_1^{max} does not have a closed form solution and a numerical solution is needed. It is not feasible to calculate x_1^{max} under these conditions. However, the maximum temperature along the length can be calculated via a simple technique. The channel is subdivided into small lengths and at each point $T(x)$. After calculating all the values at each point, the maximum channel temperature can be found.

3.3.6 The Channel Temperature at Pinch-off

The channel temperature at pinch-off point T_{pinch} is given as

$$T_{pinch} = T_1(x_1) \mid_{x_1=L_1}$$

3.4 M-Network Representation of the Channel

The analytical solution gives promising results. HeatMOS© is able to do a thermal analysis of the transistor channel and estimates temperature along its length. The approach can be used for a complete micro-chip electro-thermal reliability verification. In a complete micro-chip EMR verification methodology, each of the resistors that forms a net is represented by an equivalent interconnect network (Labun and

Jagjitkumar, 2008) and (Alam et al., 2007). Based on this research work an equivalent M-network model is proposed to model channel temperature. The M-network model is shown in Figure 3.7 and can be used to integrate the channel temperature into a full micro-chip thermal analysis. The channel has two regions with conductance η_1 and η_2 corresponding to region 1 and 2 of the channel respectively. The current sources S_1 and S_2 correspond to the source end and the drain end of the channel, respectively. The currents at the nodes of the M-network are given by F_O (at the source end) and F_L (at the drain end). The temperatures at the source and the drain end are T_O and T_L respectively. The temperature at the pinch-off point T_{pinch} (the junction of region 1 and region 2 in the channel) corresponds to a voltage source at pinch-off point. The source end and drain end are the ports of a M-network. The additional conductances θ_1 and θ_2, correspond to the source end and the drain end respectively. These conductances represent a conduction path to ground that is not usually important electrically (and so for electrical analysis, $\theta_1, \theta_2 = 0$) but will be important thermally (and so for thermal analysis, $\theta_1, \theta_2 > 0$).

The heat currents, F_O and F_L, can be given by

$$F_O = G_{avg}^{long} \frac{dT_1}{dx} \mid x = 0 \tag{3.38}$$

$$F_L = G_{avg}^{long} \frac{dT_2}{dx} \mid x = L_2 \tag{3.39}$$

Kirchhoff's current law can be applied to the both sides of the M-network of Figure

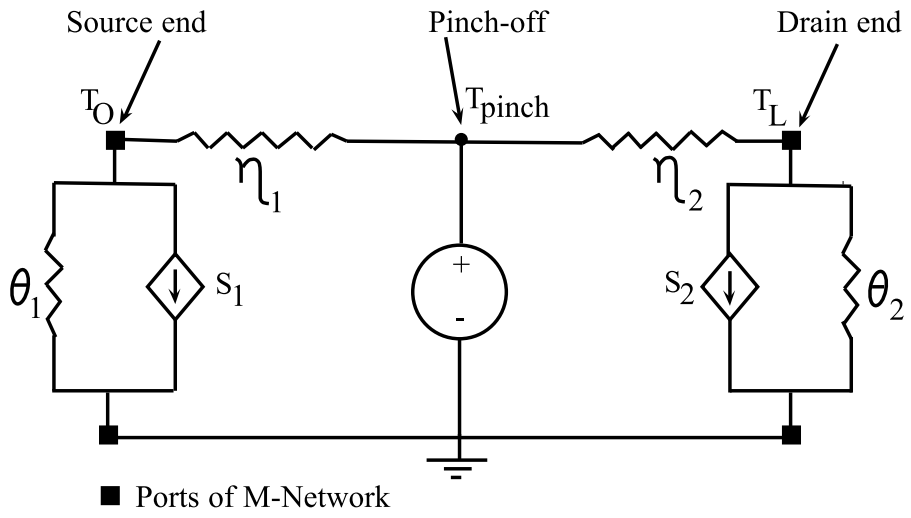

Figure 3.7: Resistor M-network used for EMR verification

3.7.

$$F_O = \eta_1 T_{pinch} - (\eta_1 + \theta_1) T_O - S_1 \tag{3.40}$$

$$F_L = (\eta_2 + \theta_2) T_L - \eta_2 T_{pinch} + S_2 \tag{3.41}$$

where

$$T_{pinch} = C_1 e^{\xi_1 L_1} + C_2 e^{-\xi_1 L_1} + T^{ref} - K_1 e^{\alpha_1 L_1}$$

Equations 3.38, 3.39 can be solved and compared with equations 3.40, 3.41 to find

out the values of η_1,η_2, θ_1, θ_2, S_1, and S_2.

$$\eta_1 = G_{avg}^{long} 2\xi_1$$

$$\theta_1 = G_{avg}^{long} \frac{4\xi_1\xi_2}{M} e^{-\xi_1 L_1} + G_{avg}^{long}\xi_1 - \eta_1 \left\{ \frac{2\xi_2 e^{-\xi_1 L_1}}{M} + 1 \right\} + e^{-\xi_1 L_1}$$

$$S_1 = G_{avg}^{long} \left\{ \frac{2\xi_1}{M}\gamma_1 - K_1(\alpha_1 + \xi_1) \right\} - T^{ref}\xi_1 - \frac{\eta_1}{M}\left\{ e^{\xi_1 L_1} - e^{-\xi_1 L_1} \right\}\gamma_1 - T^{ref} e^{-\xi_1 L_1} + T^{ref} + K_1 \left\{ e^{-\xi_1 L_1} - e^{\alpha_1 L_1} \right\}$$

$$\eta_2 = -\frac{e^{\xi_1 L_1}}{\left(e^{\xi_1 L_1} - e^{-\xi_1 L_1}\right)} \left\{ \frac{M e^{-\xi_1 L_1}}{2\xi_2} + G_{avg}^{long} e^{\xi_2 L_2} e^{-\xi_1 L_1} \left[\left(e^{\xi_1 L_1} + e^{-\xi_1 L_1} \right) + \xi_1 \left(e^{\xi_1 L_1} - e^{-\xi_1 L_1} \right) \right] \right\}$$

$$\theta_2 = \eta_2 \left\{ \frac{2\xi_2 e^{\xi_2 L_2}\left(e^{\xi_1 L_1} - e^{-\xi_1 L_1} \right)}{M} - 1 \right\} - G_{avg}^{long} \left\{ \frac{2\xi_2}{M} e^{2\xi_2 L_2} \left[\left(e^{\xi_1 L_1} + e^{-\xi_1 L_1} \right) + \xi_2 \left(e^{\xi_1 L_1} - e^{-\xi_1 L_1} \right) \right] - \xi_2 \right\}$$

$$S_2 = G_{avg}^{long}\left\{\xi_2 K_2 + \frac{2\xi_2 e^{\xi_2 L_2}}{M}\gamma_2\right\} + T^{ref}\left\{e^{-\xi_1 L_1} - 1\right\} - K_1\left\{e^{-\xi_1 L_1} - e^{\alpha_1 L_1}\right\} - \frac{\eta_2}{M}\left\{e^{\xi_1 L_1} - e^{-\xi_1 L_1}\right\}\gamma_1$$

where

$$M = \left(e^{\xi_1 L_1} - e^{-\xi_1 L_1}\right)\left(1 + e^{2\xi_2 L_2}\right)\xi_2 - \left(e^{\xi_1 L_1} + e^{-\xi_1 L_1}\right)\left(1 - e^{2\xi_2 L_2}\right)$$

$$\gamma_1 = \xi_2\left(1 + e^{2\xi_2 L_2}\right)\left\{-T^{ref}\left(e^{-\xi_1 L_1} + 1\right) + K_1\left(e^{\alpha_1 L_1} - e^{-\xi_1 L_1}\right) + K_2(1 - e^{\xi_2 L_2})\right\} + \left(1 - e^{2\xi_2 L_2}\right)\left\{-T^{ref}\xi_1 e^{-\xi_1 L_1} + K_1\left(\alpha_1 e^{\alpha_1 L_1} + \xi_1 e^{-\xi_1 L_1}\right) + K_2\xi_2 e^{\xi_2 L_2}\right\}$$

$$\gamma_2 = T^{ref}\left\{\left(e^{-\xi_1 L_1} - 1\right)\left(e^{\xi_1 L_1} + e^{-\xi_1 L_1}\right) + \xi_1 e^{-\xi_1 L_1}\left(e^{\xi_1 L_1} - e^{-\xi_1 L_1}\right)\right\} + K_1\left\{\left(e^{\alpha_1 L_1} - e^{-\xi_1 L_1}\right)\left(e^{\xi_1 L_1} + e^{-\xi_1 L_1}\right) - \left(\alpha_1 e^{\alpha_1 L_1} + \xi_1 e^{-\xi_1 L_1}\right) + \left(e^{\xi_1 L_1} - e^{-\xi_1 L_1}\right)\right\} + K_2\left\{\left(1 - e^{\xi_2 L_2}\right)\left(e^{\xi_1 L_1} + e^{-\xi_1 L_1}\right) - \xi_2 e^{\xi_2 L_2}\left(e^{\xi_1 L_1} - e^{-\xi_1 L_1}\right)\right\}$$

3.5 Summary

An analytic solution for estimating channel temperature in a MOSFET device has been derived. The solution is composed of two sets of equations corresponding to the tapered channel region and the pinch-off region. Equations were also derived for estimating the average channel temperature and the temperature at the pinch-off point. The analytic equations are used to calculate equivalent model values in a M-network that can be incorporated in top level micro-chip simulations to predict the spatial variation of temperature across the micro-chip and assist designers in identifying potential EMR failure points. The foundation for the development of the software to estimate temperature of MOSFET channel has been set.

Chapter 4

HeatMOS©

4.1 About HeatMOS©

HeatMOS© is a software tool which solves the heat equation for MOSFET devices analytically and estimates the channel temperature profile. The HeatMOS© software tool is developed as part of this research project. The program uses physical device parameters extracted from BSIM3 models (Liu et al., 1999). HeatMOS© reads the device geometry information from an extracted layout in the SPICE format. It calculates saturation electric current and other required variables for the analytical model. HeatMOS© then calculates the channel temperature using the analytical model and the outputs temperature distribution along the channel length.

The input variables required for HeatMOS are listed below:

1. SourceTemp: Source end temperature.
2. DrainTemp: Drain end Temperature.
3. RefTemp: Reference temperature of the medium of the channel.

4. Vgs: Gate voltage.
5. Vds: Drain voltage.
6. Vbs: Substrate bias voltage.
7. Ids: Drain current; this is optional parameter, if not given will be calculated (device is in saturation region).
8. Netlist: Extracted spice netlist from layout.

HeatMOS© outputs:

1. The channel temperature distribution along the length of the channel and a text file containing the temperatures at different points along the channel length.
2. The drain current.
3. The average thermal conductance.
4. The average channel temperature.
5. The maximum channel temperature.
6. The temperature at pinch-off point.
7. The effective length and width of the channel.

A sample output of of HeatMOS has been provided in Appendix D.

4.2 Integration in the VLSI CAD Flow

Figure 4.1 shows a typical post-logic synthesis VLSI (Very-large-scale Integration) CAD (Computer-aided Design) flow. Reliability verification is necessary for nano-scale technologies to ensure the reliability of integrated circuit. As can be seen from the figure, thermal verification is needed after physical verification. Heat-MOS© can be integrated with interconnect temperature estimation CAD tools (e.g. Therminator (Labun and Jagjitkumar, 2008)) to do a complete micro-chip thermal verification. If the integrated circuit design does not pass reliability verification, there is still a chance to modify the layout of the circuit in its design phase.

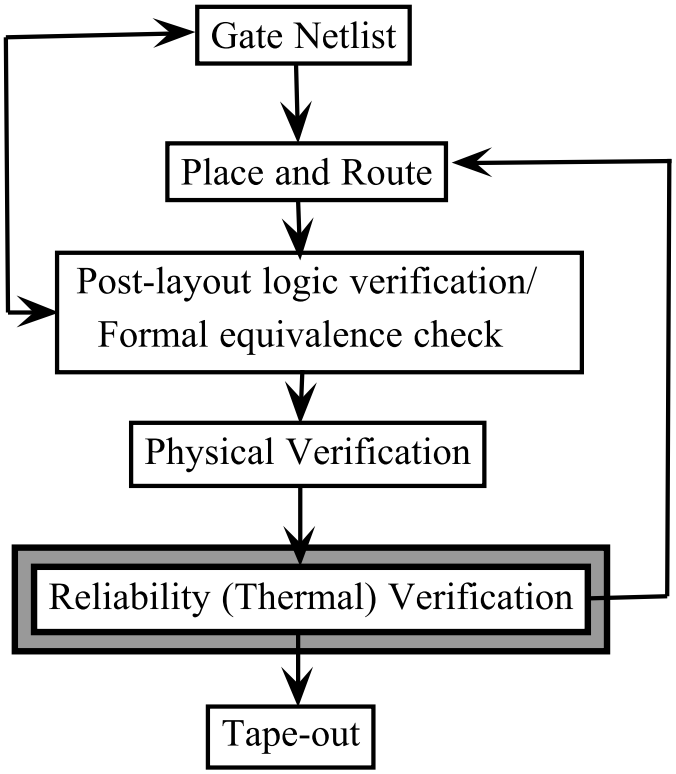

Figure 4.1: VLSI CAD flow

Chapter 5

Results and Discussions

HeatMOS solves the heat equation analytically. For a comparative analysis of the results of HeatMOS, the heat equation for both regions of the channel has been solved using the finite difference approach (numerical approach). The finite difference approach is based on Taylor's approximation (Strikwerda, 2004) for 2nd order derivatives given by equation 5.1

$$\frac{f(x-h)-2f(x)+f(x+h)}{h^2} = f''(x) + \frac{f^{(4)}(v)}{12}h^2 \tag{5.1}$$

where, h is a small interval and $f''(x)$ is the second derivative of function $f(x)$.

The second term on the right hand side of equation 5.1 is the remainder term and can be considered as an approximation error. The detailed finite-difference method and its pseudo code is given in appendix C.

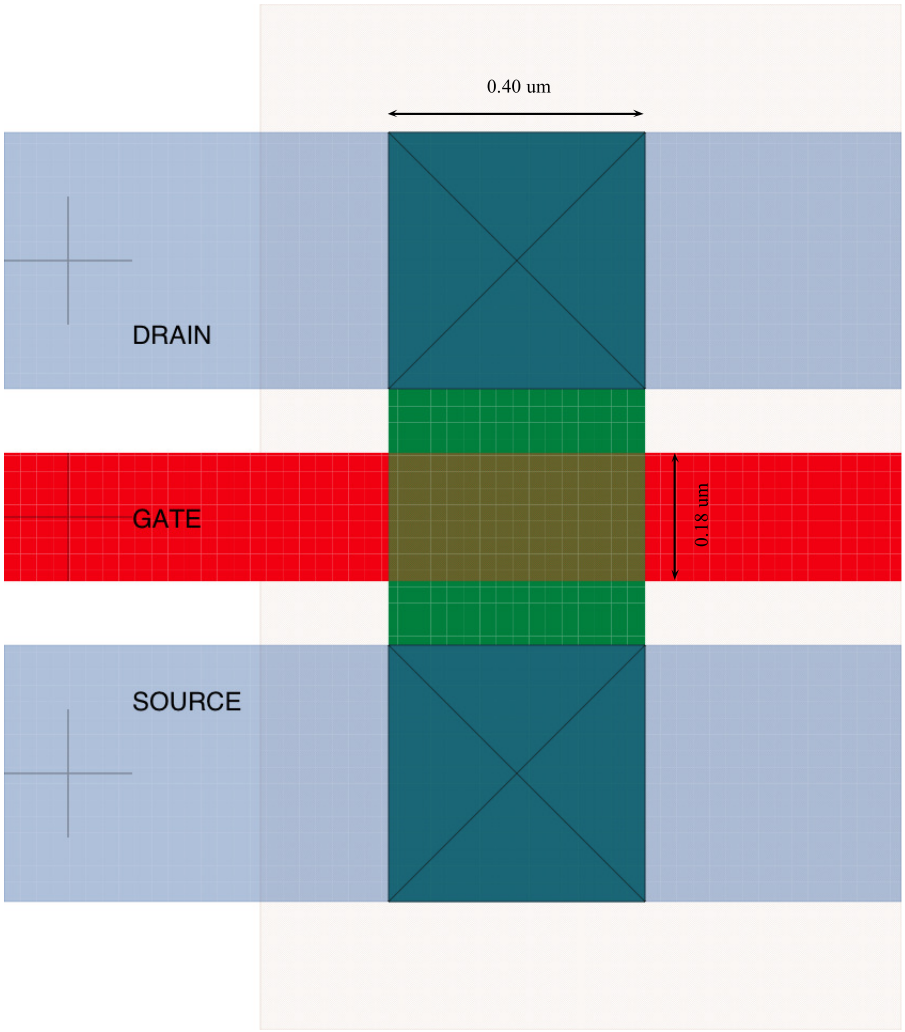

Figure 5.1: An nMOS layout

If we apply voltages to the terminals of this nMOS transistor, an electric current will flow in the channel. In a complex micro-chip, the source and the drain of this transistor will be connected to other nets via vias and contacts. The temperatures of these vias can be estimated by interconnect estimations tools such as Terminator3D (Labun and Jagjitkumar, 2008). If we neglect the distance between the source and the drain ends of the channel and the contacts, the source and the drain ends will be approximately at the same temperature as the contacts connecting these vias.

The thermal channel model is verified by running a number of different test scenarios with a typical nMOS device. The layout of the device is shown in Figure 5.1 and has a drawn length of 0.18 μm and a drawn width of 0.40 μm. The full SPICE BSIM3 model for the device is given in Appendix A. HeatMOS includes a utility to approximate the IV characteristics of the device using a simplified device model and the results are shown in Figure 5.2. The IV characteristic at the pinch-off point is not smooth because the curve-fitting spline functions have not be modeled in HeatMOS. The program also support a direct input of the operating device current which can be extracted from full BSIM3 SPICE simulations. This feature is included in the test scenarios described below.

5.1 Verification

Let us consider a few test scenarios to verify that HeatMOS© compiles and provides the results that are consistent with numerical simulations. Te objective of

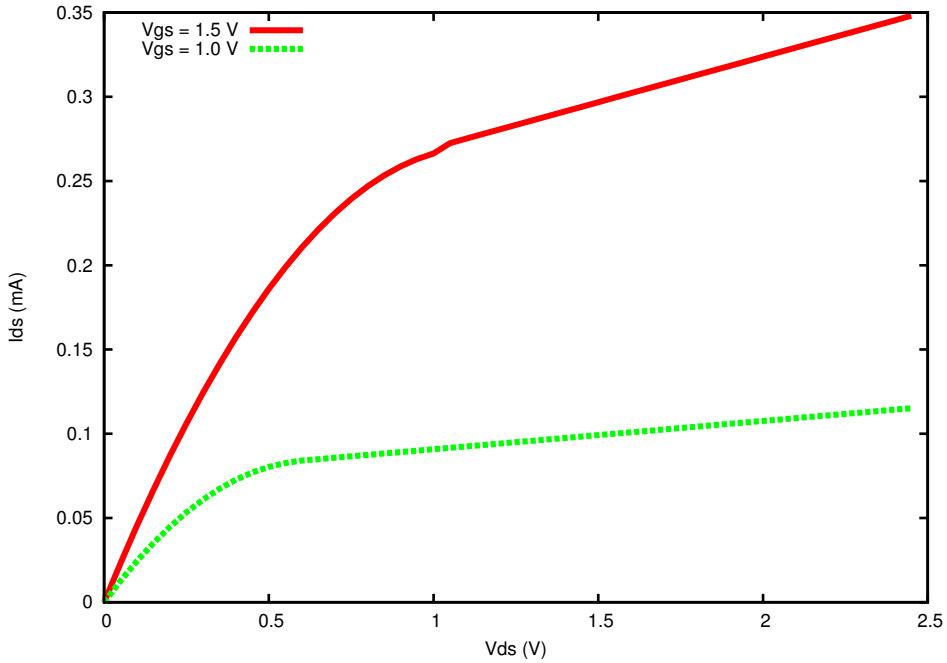

Figure 5.2: I-V characteristics of nMOS device under test produced by HeatMOS©

these tests is to verify that HeatMOS provides accurate results under different test scenarios and free from run-time errors.

5.1.1 Test Scenario using Externally Supplied Drain Current

The objective of this test is to verify that HeatMOS© can analyze channel temperature using an externally supplied current. Sometimes designer's may want to analyze the temperature behavior for higher current than calculated from circuit simulations. In this test, a current of 2 mA has been supplied externally by designer, the layout drawn length of device under test is 0.28 μm and the width is 0.40 μm, the applied gate voltage is 1.0 V and the drain voltage is 1.5 V, the source end temperature is set to 565 K, the drain end is set at 567 K, and the reference temperature has been set to 456 K. The results of this test scenario are shown in Figure 5.3. HeatMOS© calculates an average channel temperature of 586.19 K and the maximum channel temperature is 588.68 K at a distance of 0.2115 μm from from the source end. The temperature at the pinch-off point is 588.46 K at a distance 0.2093 μm from the source end.

As we can see from the Figure 5.3 the difference between the analytic solution and numerical solution is significant and the peak temperature difference is approximately 4 K. The difference is due to the round-off error in the finite difference approximation and the chosen step size. In this test scenario the gate voltage and drain voltage are different and electric current has been provided externally and not been calculated by HeatMOS©. The accuracy of the numerical solution can be improved by reducing the step size as is shown by the blue line in Figure 5.6.

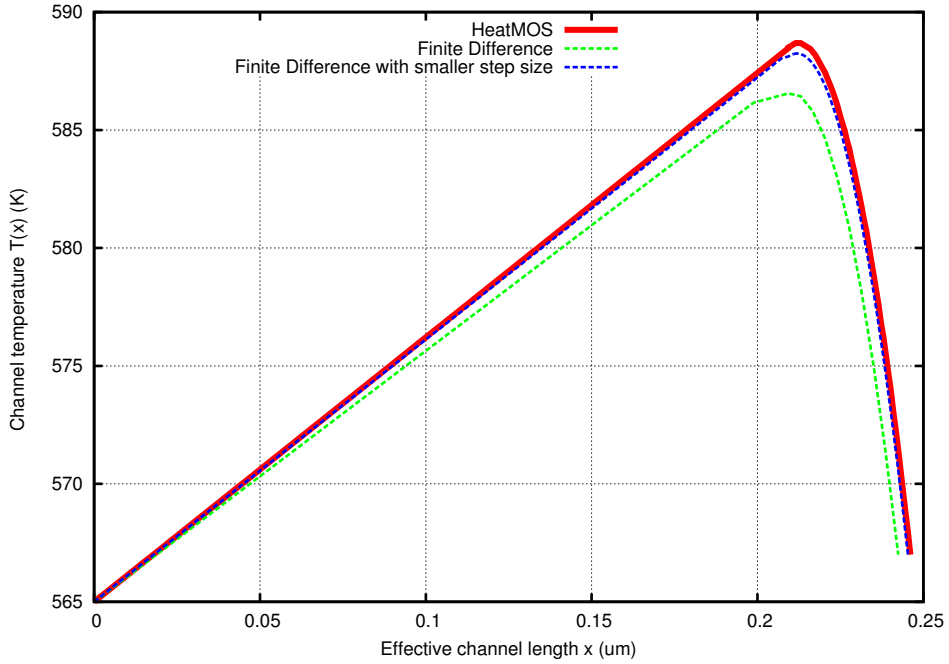

Figure 5.3: $SourceTemp = 565K \mid DrainTemp = 567K \mid RefTemp = 456K \mid V_{gs} = 1.0V \mid V_{ds} = 1.5V \mid I_{ds} = 2mA \mid v7 - nmos.spice$

5.1.2 Test Scenario for a Smaller MOSFET Device

In this test, the layout drawn length and width of the device are 0.18 μm and 0.40 μm, and gate and drain voltages are both 1.5 V. The source end temperature is 565 K, the drain end temperature is 567 K, and the reference temperature has been set at 456 K. The results of this test scenario are shown in Figure 5.4. Results from HeatMOS© show the average channel temperature is 575.87 K and the maximum channel temperature is 570.52 K at a distance of 0.114 μm from the source end. The temperature at the pinch-off point is 570.36 K at a distance 0.109 μm along the length of the channel from the source end. HeatMOS© calculates a saturation current of 0.269 mA.

As we can see from the results of this test the channel becomes hotter towards drain end. It would be interesting to verify HeatMOS© keeping the source, the drain and the reference temperature all at the same time.

5.1.3 Test Scenario for the Case When the Source, Drain, and the Reference Temperatures are Same

In this test, the layout drawn length of the device under test is 0.18 μm and the width is 0.40 μm, the applied gate voltage is 1.5 V, the drain voltage is 1.5 V, and the source, drain, and reference temperatures all are set to 10 K. The results of this test scenario are shown in Figure 5.5. The drain current calculated by HeatMOS© is 0.2699 mA, the average channel temperature is 5.05 K, and the maximum channel temperature is 8.1 K at a distance of 0.1124 μm along the length of the channel

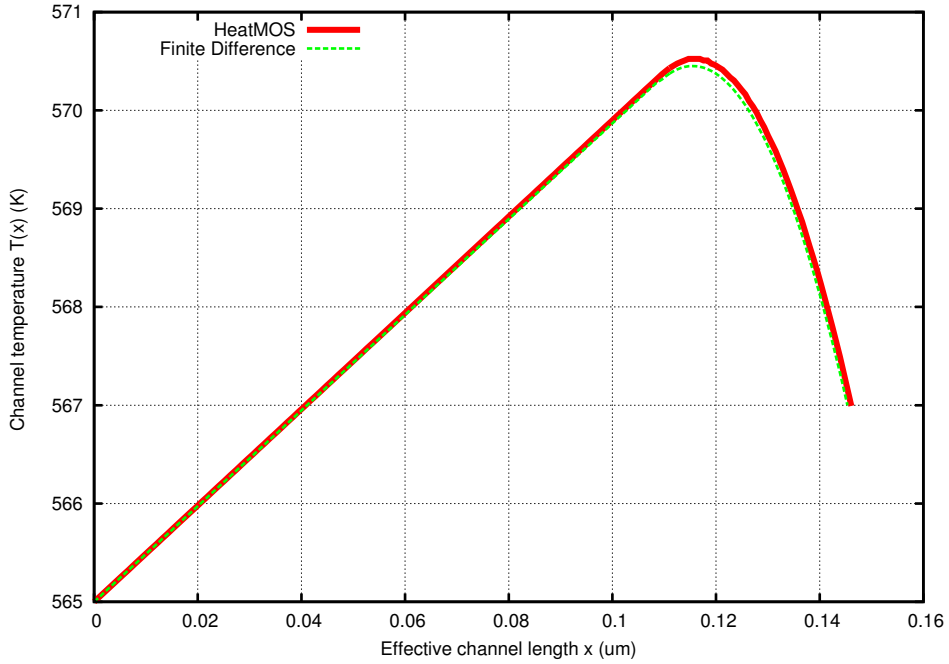

Figure 5.4: $SourceTemp = 565K \mid DrainTemp = 567K \mid RefTemp = 456K \mid V_{gs} = 1.5V \mid V_{ds} = 1.5V \mid v8 - nmos.spice$

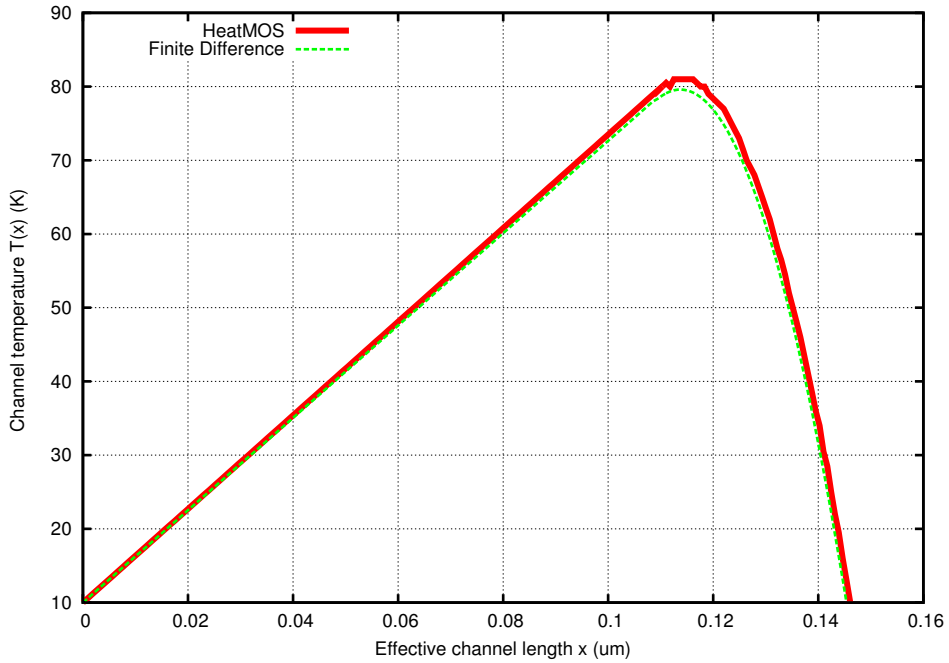

Figure 5.5: $SourceTemp = 10K \mid DrainTemp = 10K \mid RefTemp = 10K \mid V_{gs} = 1.5V \mid V_{ds} = 1.5V \mid v8 - nmos.spice$

from the source end. The temperature at the pinch-off point is 7.95 K at a distance of 0.109 μm from the source end.

The above verification tests shows that HeatMOS© is free from runtime errors, bugs, and provides meaningful results. There is a possibility to write other corner test scenarios to find out hidden bugs in the software. Some of the following test scenarios are focused to verify the HeatMOS© results when the device under test operates in different modes of operation.

5.2 Saturation Mode of Operation

In the saturation mode, the MOSFET is on and it conducts current between the source and the drain. The charge carriers flow in the channel and the current becomes constant ($I_{DS} = I_{sat}$) and can be approximated by (Weste and Harris, 2004)

$$I_{sat} = \frac{1}{2}\frac{W_{eff}}{L_{eff}}\mu_n C_{ox}\left(V_{GS} - V_{Th}\right)^2\left\{1 + \lambda\left(V_{DS} - VDS\right)\right\} \tag{5.2}$$

$$VDS = \left(V_{GS} - V_{Th}\right) - \frac{1}{2}\lambda\left(V_{GS} - V_{Th}\right)^2$$

where W_{eff} is the effective channel width, L_{eff} is the effective channel length, μ_n is the electron mobility, C_{ox} is the gate oxide layer capacitance per unit area, V_{GS} is the applied gate voltage, V_{Th} is the threshold voltage of the nMOS transistor, and λ is the fitting parameters for channel length modulation. In this mode of operation $V_{DS} > VDS$. The nMOS threshold voltage for the BSIM3 technology file used in this work is $0.39V$. The value of λ is 0.20. Let us consider a few test cases in this mode of operation.

5.2.1 Test Scenario When Gate and Drain are at Same Voltage

In this test, the source and drain temperatures have been set to 325 K respectively, and the reference temperature has been set to 300 K. The applied gate voltage is 1.5 V and the drain voltage is 1.5 V. The layout drawn width of the nMOS is

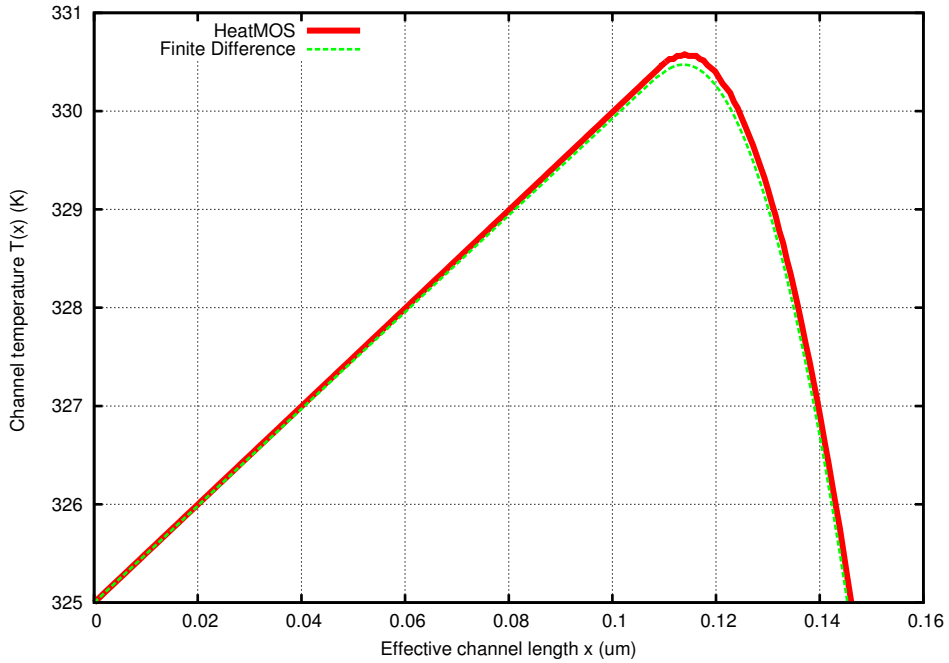

Figure 5.6: $SourceTemp = 325K \mid DrainTemp = 325K \mid RefTemp = 300K \mid V_{gs} = 1.5V \mid V_{ds} = 1.5V \mid v8 - nmos.spice$

0.40 μm and the the length is 0.18 μm. HeatMOS© calculates a saturation drain current of 0.2699 mA. The results of this test scenario are shown in Figure 5.6. The average channel temperature for this case is 332.50 K and the maximum channel temperature is 330.57 K at a distance of 0.113 μm from the source end. The temperature at the pinch-off point is 330.46 K at a distance 0.109 μm along the length of the channel from the source end.

As we can see from this test that the temperature varies between 325 K to 330.57 K. It would also be interesting to note that in this case the source and the drain has

been at the same voltage level. It would be interesting to check the temperature along the length of channel if the gate and the drain voltages are different.

5.2.2 Test Scenario for the Case of Different Gate and Drain Voltages

In this test, the source and the drain end temperatures are set to 325 K respectively, and the reference temperature is set to 300 K. The applied gate voltage is 1.8 V and the drain voltage is 2.2 V. The layout drawn width of nMOS is 0.40 μm and the length is 0.18 μm. HeatMOS© calculates a saturation drain current of 0.4322 mA. The results of this test scenario are shown in Figure 5.7. The average channel temperature for this case is 336.78 K and the maximum channel temperature is 338.12 K at a distance 0.1137 μm from the source end. The temperature at the pinch-off point is 337.81 K at a distance 0.108 μm from the source end.

The temperature difference between the minimum and the maximum temperature in this case is 13.12 K. We can see that upon increasing the gate and drain voltage the maximum channel temperature rises. The channel temperature variation is complex and is not based on one factor (e.g. voltage change), therefore the correlation between voltage and temperature is not explicit. However in simple terms it indicate that upon increasing the gate and drain voltage, the drain current increases and it leads to higher temperature in the channel as the more heat is generated in the channel due to electric current flow. Let's consider another test scenario with very high voltage on the gate and drain ends.

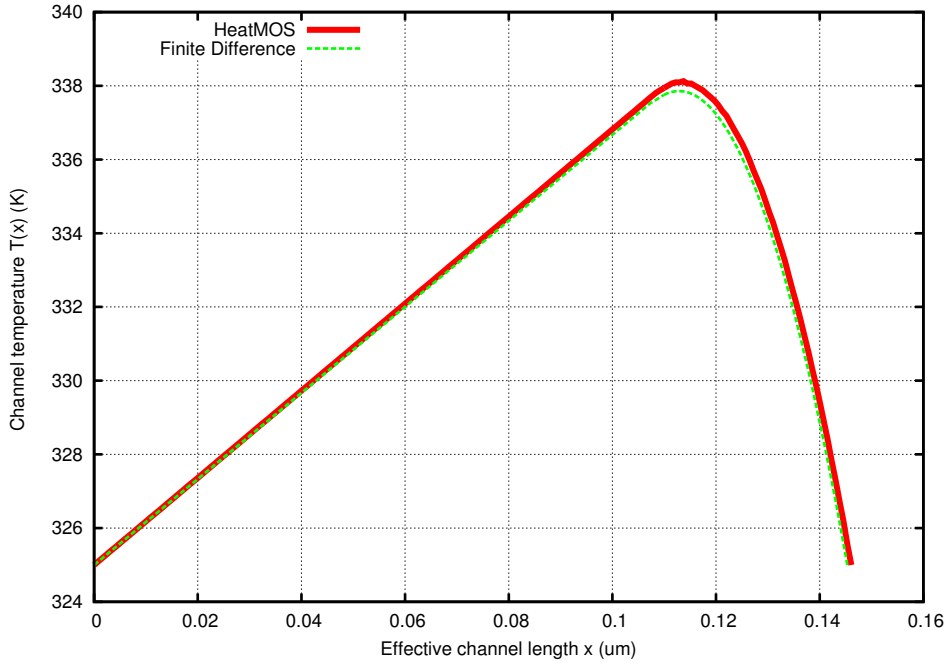

Figure 5.7: $SourceTemp = 325K \mid DrainTemp = 325K \mid RefTemp = 300K \mid V_{gs} = 1.8V \mid V_{ds} = 2.2V \mid v8 - nmos.spice$

5.2.3 Test Scenario for the Case of High Gate and Drain Voltages

In this test, source and drain temperatures are set to 325 K respectively, the reference temperature has been set to 300 K. The applied gate and drain voltages are both 5.0 V. The layout drawn width of the nMOS is 0.18 μm and the the length is 0.40 μm. HeatMOS© calculates a saturation drain current of 4.52 mA. This is a high value for the drain current. The results of this test scenario are shown in Figure 5.6. The average channel temperature for this case is 460.66 K and the maximum channel temperature is 556.00 K at a distance 0.1102 μm from the source end. The temperature at the pinch-off point is 550.26 K at a distance 0.10631 μm from the source end.

As we can see form this test that the maximum temperature difference is 231 K which is a very high value. This indicates that the higher drain current leads to higher temperature which is expected. It would be interesting to see the temperature distribution for the same test on a larger device.

5.2.4 Test Scenario for a Large MOSFET Device with High Drain Current

In this test, the source and the drain end temperatures have been set to 325 K respectively, and the reference temperature has been set to 300 K. The applied gate and drain voltages are both 5.0 V. The layout drawn width of the nMOS is 0.40 μm and the length is 0.28 μm. HeatMOS© calculates the saturation drain current of 2.689 mA. The results of this test scenario are shown in Figure 5.9. The average

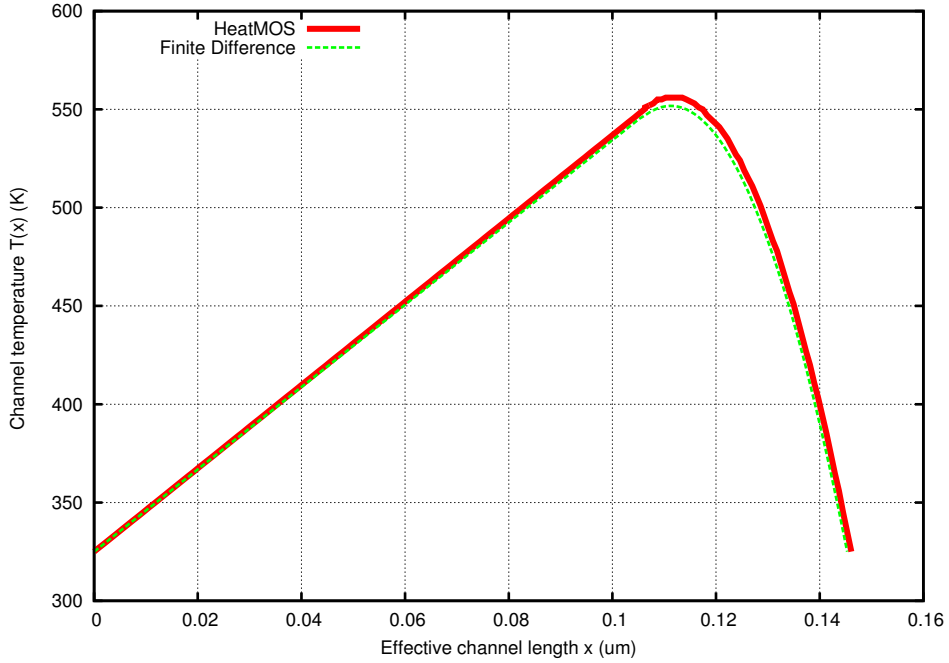

Figure 5.8: $SourceTemp = 325K \mid DrainTemp = 325K \mid RefTemp = 300K \mid V_{gs} = 5.0V \mid V_{ds} = 5.0V \mid v8 - nmos.spice$

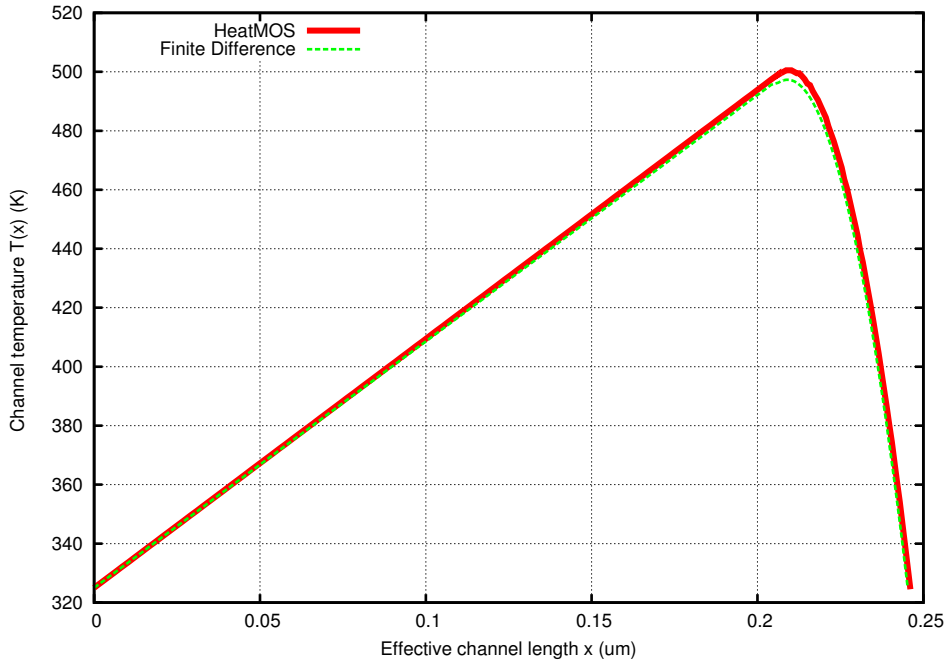

Figure 5.9: $SourceTemp = 325K \mid DrainTemp = 325K \mid RefTemp = 300K \mid V_{gs} = 5V \mid V_{ds} = 5V \mid v7 - nmos.spice$

channel temperature for this case is 429.03 K and the maximum temperature is 500.50 K at a distance 0.208 μm from the source end. The temperature at the pinch-off point is 499.17 K at a distance 0.206 μm from the source end.

The results show that the maximum channel temperature peaks at 175.5 K above the source and drain terminal temperatures which is about 50 K cooler than the previous case. Clearly the larger device has more area to dissipate heat in the channel. Let's consider another arbitrary test scenario.

5.2.5 Test Scenario for Different Source/Drain Temperatures and Voltages

In this test, the source end temperature is set to 318 K, the drain end temperature is set to 324 K, and the reference temperature is set to 298 K. The applied gate voltage is 1.2 V and the drain voltage is 1.8 V. The layout drawn width of the nMOS is 0.40 μm and the length is 0.18 μm. HeatMOS© calculates a saturation drain current of 0.145 mA. The results of this test scenario are in Figure 5.9. The average channel temperature for this case is 327.91 K and the maximum temperature is 326.97 K at a distance of 0.118 μm from the source end. The temperature at the pinch-off point is 326.58 K at a distance of 0.109 μm from the source end.

5.3 Linear/Ohmic Mode of Operation

When the MOSFET operates in the linear mode, the drain current increases linearly with the drain voltage. Under these conditions the MOSFET behaves as a voltage dependent resistor where the resistance is determined by the gate voltage. The current and the voltage follow the ohmic relationship in this mode of operation. The drain current in this mode of operation is given by (Sedra and Smith, 2007)

$$I_{DS} = \mu_n C_{ox} \frac{W_{eff}}{L_{eff}} \left[2.0(V_{GS} - V_{Th})V_{DS} - V_{DS}^2\right] \tag{5.3}$$

where, W_{eff} is the effective channel width, L_{eff} is the effective channel length, μ_n is the electron mobility, C_{ox} is the gate oxide layer capacitance per unit area, V_{GS}

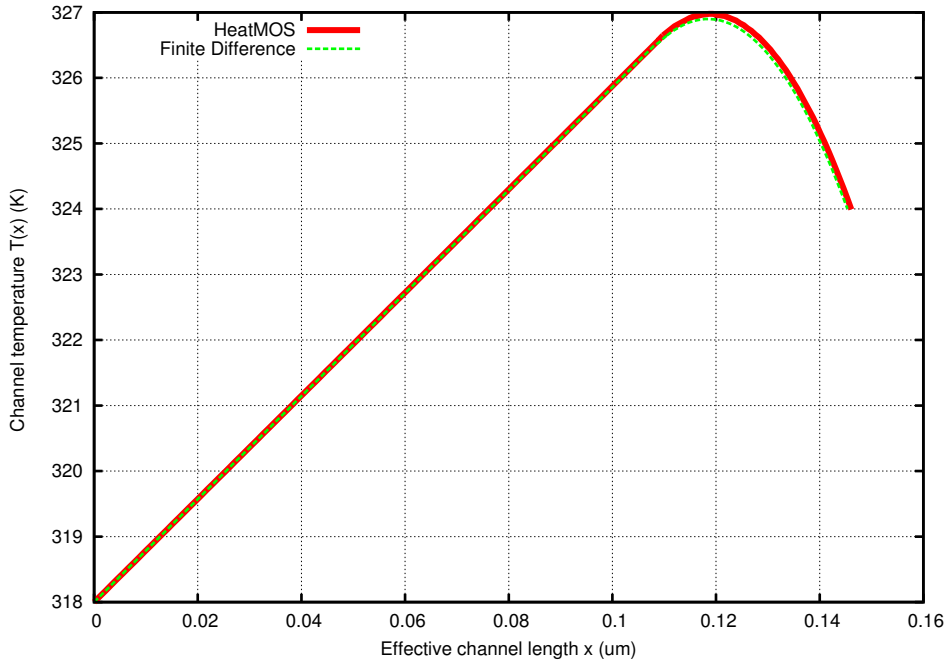

Figure 5.10: $SourceTemp = 318K \mid DrainTemp = 324K \mid RefTemp = 298K \mid V_{gs} = 1.2V \mid V_{ds} = 1.8V \mid v8 - nmos.spice$

is the applied gate voltage, V_{DS} is applied drain voltage, and V_{Th} is the threshold voltage of the nMOS. In this mode of operation $V_{DS} < VDS$.

Let us consider a few test cases in this mode of operation.

5.3.1 Test Scenario for the Case of Different Temperatures at the Source and the Drain

In this test, the source end temperature is set to 300 K, the drain end temperature is set to 325 K, and the reference temperature has been set to 300 K. The applied gate voltage is 1.5 V and the drain voltage is 1.0 V. The layout drawn width of nMOS is 0.40 μm and the length is 0.18 μm. HeatMOS© calculates the linear mode drain current of 0.0245 mA. The results of this test scenario are in Figure 5.11. The average channel temperature for this case is 317.86 K and the maximum channel temperature is 325 K at a distance of 0.146 μm from the source end. The temperature at the pinch-off point is 318.97 K at a distance of 0.110 μm from the source end.

Let's consider another test scenario with larger device under test.

5.3.2 Test Scenario for a Larger Device in the Ohmic Operating Region

In this test, the source end temperature is set to 318 K, the drain end temperature is set to 324 K, and the reference temperature is set to 300 K. The applied gate voltage

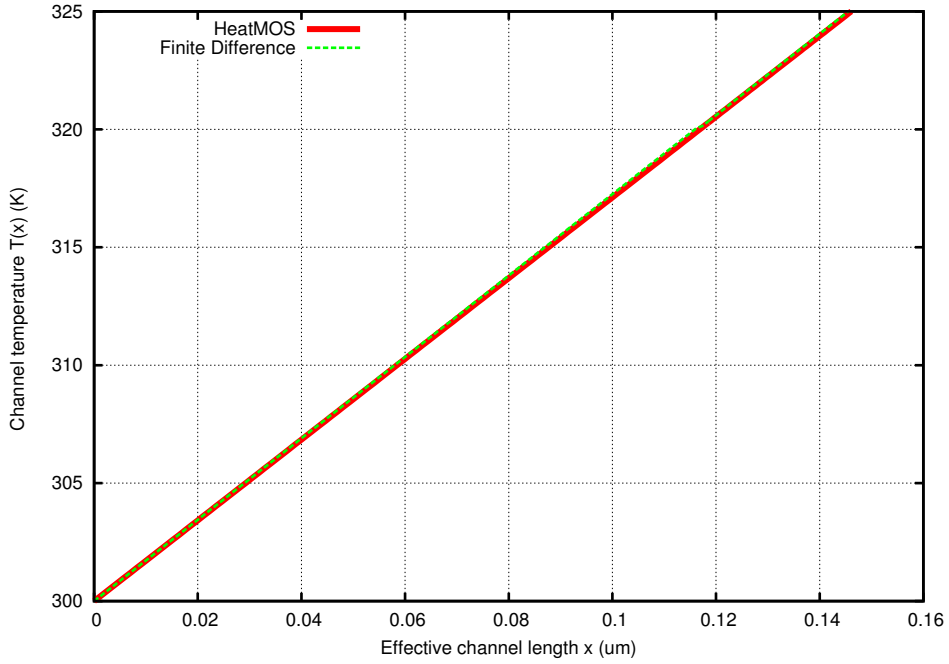

Figure 5.11: $SourceTemp = 300K \mid DrainTemp = 325K \mid RefTemp = 300K \mid V_{gs} = 1.0V \mid V_{ds} = 0.1V \mid v8 - nmos.spice$

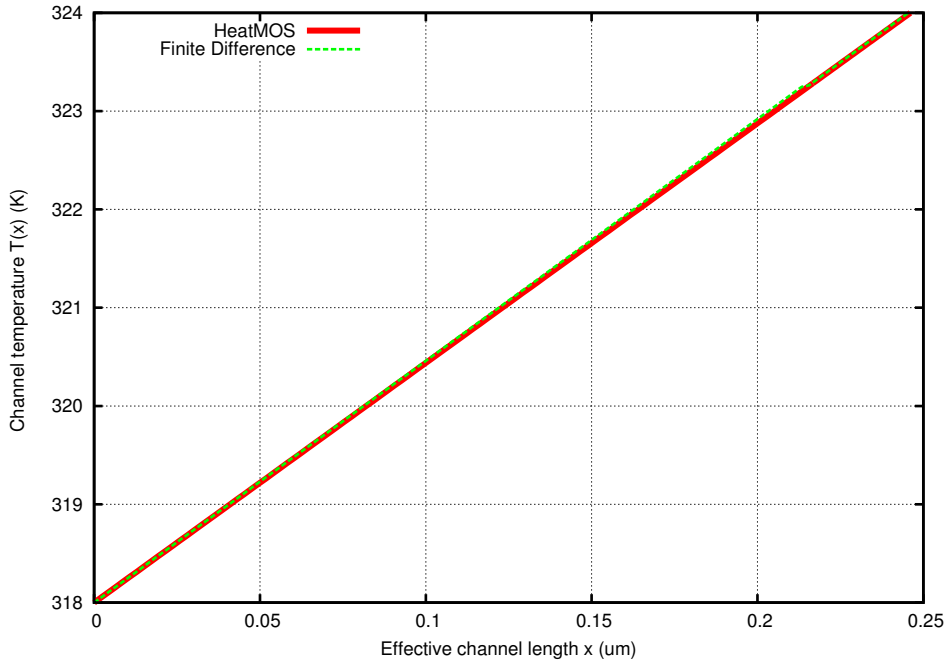

Figure 5.12: $SourceTemp = 318K \mid DrainTemp = 324K \mid RefTemp = 300K \mid V_{gs} = 1.0V \mid V_{ds} = 0.1V \mid v7 - nmos.spice$

is 1.0 V and the drain voltage is 0.1 V. The layout drawn width of the nMOS is 0.40 μm and the length is 0.28 μm. HeatMOS© calculates a drain current of 0.01455 mA. The results of this test scenario are shown in Figure 5.12. The average channel temperature for this case is 325.92 K and the maximum channel temperature is 324 K at a distance of 0.246 μm from the source end. The temperature at the pinch-off point is 323.25 K at a distance of 0.215 μm from the source end.

As we can see from the results that there is discrepancy between the analytical and numerical solutions in a few test scenarios. The two sources of error in finite dif-

ference method are round-off error, the loss of precision due to computer rounding of decimal quantities, and truncation or discretization error. The remainder term of a Taylor's polynomial is convenient for analyzing the local truncation error. Using the Lagrange form of the remainder from Taylor's polynomial for $f(x_0+h)$, the error term is

$$R_n(x_0+h) = \frac{f^{(n+1)}(\xi)}{!(n+1)}(h)^{(n+1)}, x_0 < \xi < x_0+h \tag{5.4}$$

Since the IR drop in the channel is very low in the ohmic region, the thermal effects are not as significant as devices in saturation. Therefore, although the error between the analytic and numeric results is larger in this region the impact on EMR verification is expected to be negligible. The weak-inversion mode is not very important as a very weak current flows through the channel and the rise in the temperature of the channel due to it can be neglected.

5.4 Average and Maximum Temperature Distributions

The average and maximum channel temperature distribution over a range of different values of the drain voltage and gate voltages with corresponding drain current are provided in the following subsections. For these test scenarios the source temperature has been set to 318 K, the drain temperature has been set to 324 K, and the reference temperature has been set to 298 K. The layout drawn channel length of the device under test is 0.18 μm and the channel width is 0.40 μm.

5.4.1 Channel Temperature Distribution with Drain Voltage and Drain Current

Figure 5.13 shows a plot of the average channel temperature distribution versus the drain current and the effective gate voltage. HeatMOS© is run in a loop. In the first iteration, the gate voltage has been kept constant at 0.5 V and the drain voltage is varied from 0.0 V to 4 V with a step size of 0.5 V. In the second iteration the gate voltage is set to 1.0 V iteration and the drain voltage is varied from 0.0 V to 4.0 V with a step size of 0.5 V. Figure 5.14 shows the maximum channel temperature distribution versus the drain voltage and drain current.

5.4.2 Channel Temperature Distribution with Effective Gate Voltage and Drain Current

In the same manner as described above, the drain voltage can be kept constant and the gate voltage can be varied to get a plot of the average and the maximum channel temperature distribution versus the drain current and the the effective gate voltage, $V_{gs} - V_{th}$. Figure 5.15 shows the average channel temperature distribution versus the drain current and the effective gate voltage, while Figure 5.16 shows the maximum channel temperature distribution versus the drain current and the effective gate voltage. In the first iteration, the drain voltage has been kept constant at 1.0 V and the gate voltage is varied from 0.0 V to 2.0 V with a steps size of 0.05 V. In the second iteration the drain voltage is kept constant at 1.5 V and the gate voltage is varied from 0.0 V to 2.0 V with a step size of 0.05V.

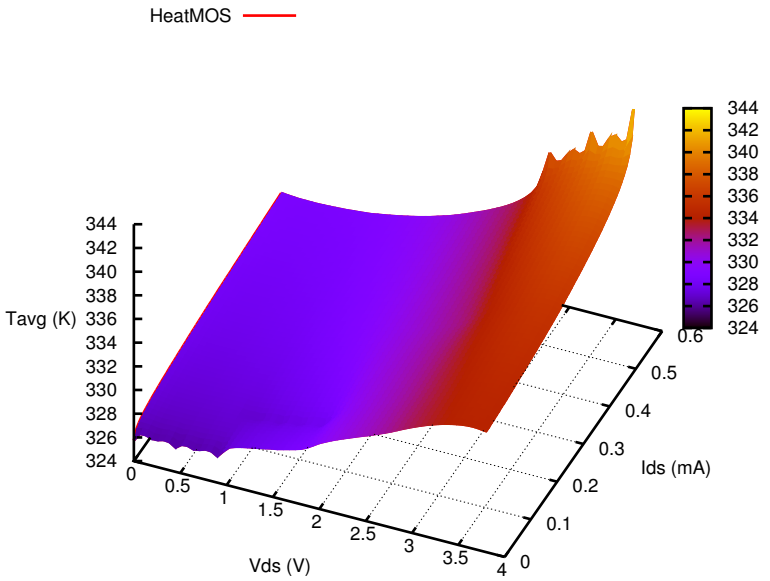

Figure 5.13: The average channel temperature versus the drain current and the drain voltage

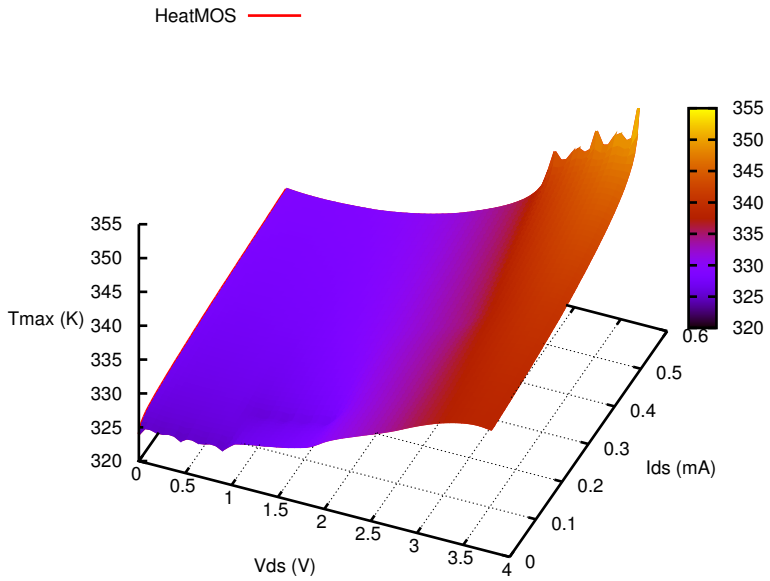

Figure 5.14: The maximum channel temperature versus the drain current and the drain voltage

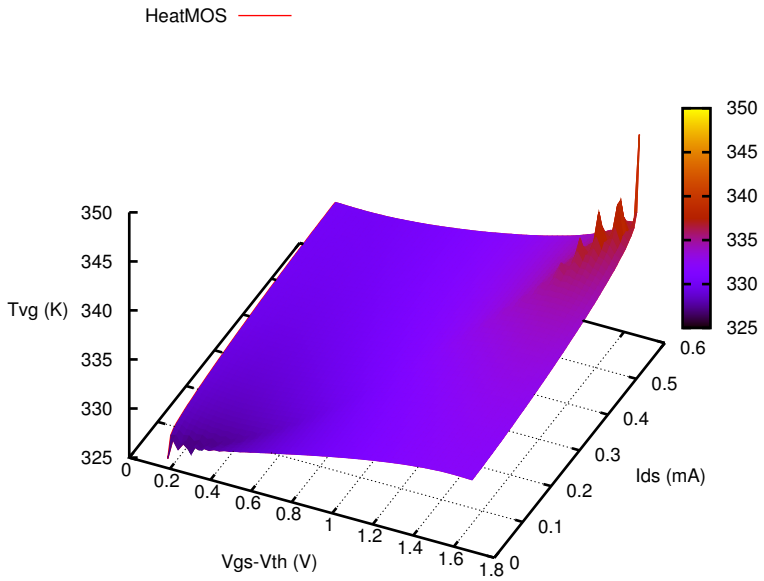

Figure 5.15: The maximum channel temperature versus the drain current and the drain voltage

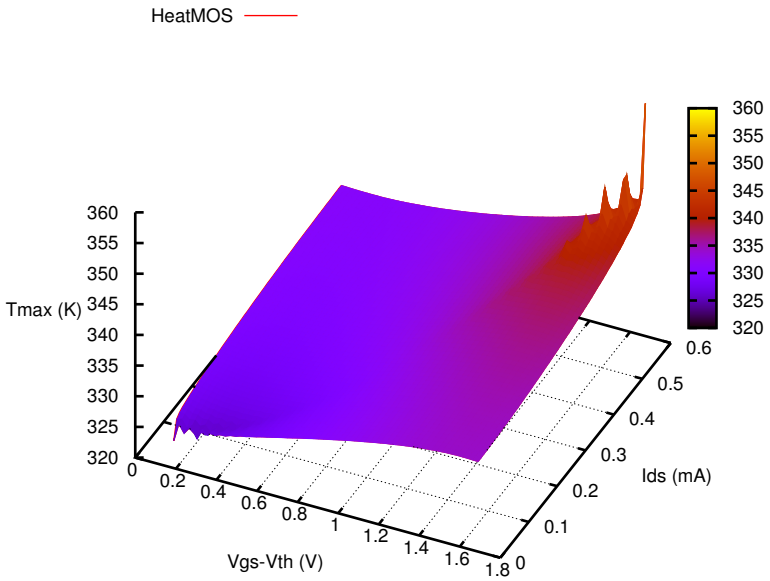

Figure 5.16: The maximum channel temperature versus the drain current and the effective gate voltage

5.5 Discussion

Comparative results of HeatMOS with finite difference simulations validates the analytic model developed in this work. However a comparison of HeatMOS© results with experimental results need to be done in order to validate the accuracy of the results provided by HeatMOS©. A review of published literature shows that very few experimental measurements have been published on the profile of channel temperature in semiconductor devices. The best example that was found were results that were published by Reale for an HEMT device Reale et al. (2007).

If we compare results predicted by HeatMOS with experimental work published in Reale et al. (2007), we find very similar thermal distributions are obtained for the HEMT and the results generated by HeatMOS for MOSFET devices. The HEMT is a device with similar topology to the FET, which would be expected to give a similar channel temperature profile from source to drain. However it is much larger than the current advance technology nodes, so the thermal diffusion model is definitely valid for the HEMT devices. Figure 5.17 shows a cross-sectional view of a HEMT device. The experimental results for an HEMT device given in Reale et al. (2007) are shown in Figure 5.18 . The measured data shows a very similar profile to the results predicted using HeatMOS©. If we look at some experimental results of HEMT-based (High Electron Mobility Transistor) based devices, it can be noticed that HeatMOS© results follows the similar pattern. As can be seen from the Figure 5.18, the temperature is greatest in centre of the channel and toward the drain region (Reale et al., 2007). This is the similar result provided by HeatMOS©. However

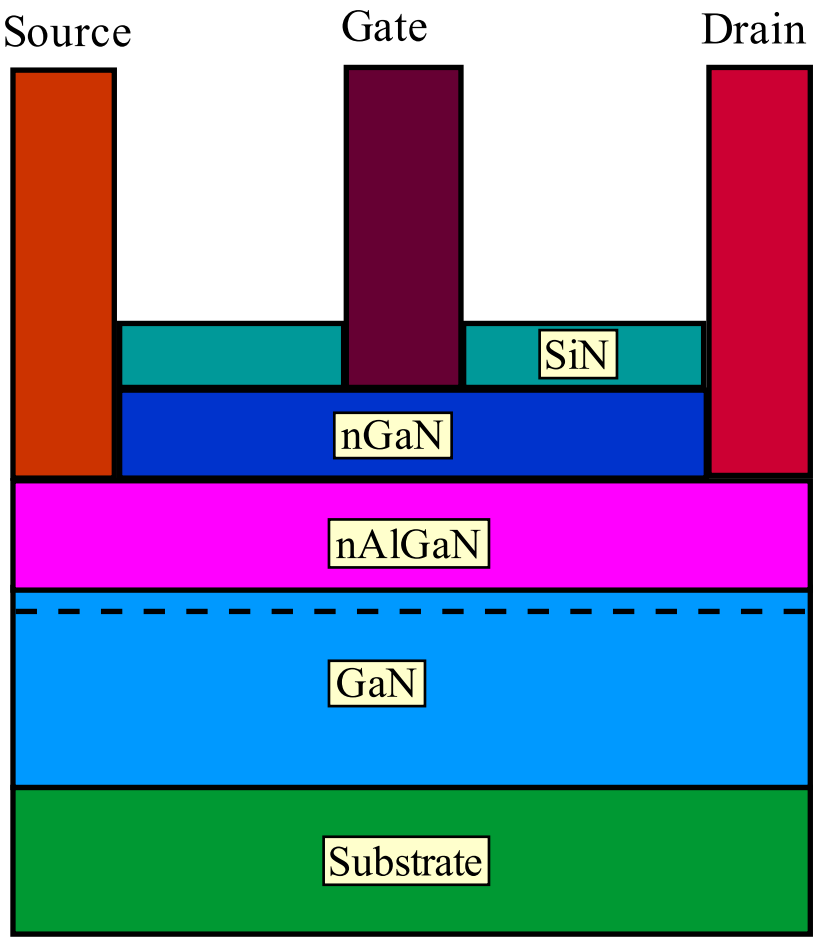

Figure 5.17: A typical cross-section of an HEMT device

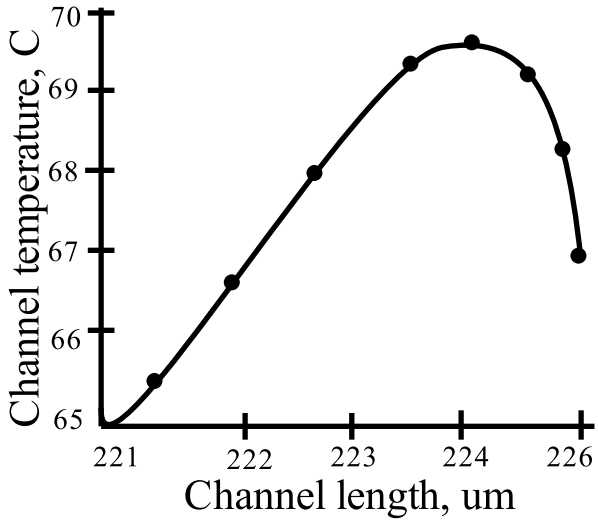

Figure 5.18: Experimental channel temperature of HEMT device

HEMT-based devices are different than MOSFET in a way that the channel is a junction between two materials with different band gaps instead of a doped region and further work is required to experimentally validate the thermal model.

5.6 Summary

HeatMOS© has been verified under different test scenarios. The results of HeatMOS© have been compared with numerical solutions using the finite difference method. A range of different test scenarios were compared to validate the model in the saturation region and the ohmic region. The test scenarios include changes to source and drain temperature, different gate and drain voltages and different device sizes. In all cases, there was good agreement between the analytic model

and numerical solutions. Finally, the trend in channel temperature predicted by the model was compared with experimental measurements which were found in the literature for an HEMT device. There are very few results available in the literature which report experimental results and this would be a good area for future research. The explanations of the different test scenarios have been provided along with differences with finite difference approach. The average and the maximum channel temperature distributions with the drain current variation and the drain and the gate voltage variations have been provided with explanations. Further, the discussions of HeatMOS© results and experimental results have been provided.

Chapter 6

Conclusions and Future Directions

6.1 Contributions

The analytical solution for the MOSFET channel temperature has been developed. The proposed solution for the predicting channel temperature is based on an electrical analogy and can be modeled as an M-network. The proposed solution and HeatMOS© can be integrated with other interconnect thermal analysis software tools to do a complete micro-chip thermal analysis rapidly. The results are comparable with numerical approaches. The advantage of an analytic model is that it will accelerate thermal modeling as compared with a rigorous thermal model using numeric solvers. The analytical thermal model for the device can be used to support EMR verification early in the design phase.

6.2 Limitations

The present implementation of HeatMOS© treats the channel as a non-uniform resistor in its simplest form. There are some limitations of HeatMOS for the thermal analysis. The following list of limitations contains two categories: fundamental limitations and limitations of the first implementation of HeatMOS©. The fundamental limitations are somewhat difficult to solve but limitations of the first implementation can be rectified in future versions of the HeatMOS©.

6.2.1 Fundamental Limitations

1. It is limited to steady state thermal solution. The ODE approach is not appropriate for the transient problem because there is no closed form solution.

2. It is currently limited to be used with BSIM3 CMOS model. However extension to BSIM4 model should not be too difficult.

3. It is limited to do the analysis for MOS devices down to channel lengths of 0.18 μm.

4. Heat transport is by diffusion only; no sub-continuum or quantum effects are considered. There is no separate treatment of, say, optical and acoustic phonons.

5. An exponential channel profile with a uniform pinch-off region is assumed for modeling the channel cross-section.

6. The effect of the process variation on temperature have not been considered. BSIM3 does not provide any information about the process variation on the temperature.

6.2.2 Limitations of First Implementation

1. It is limited to do an analysis for nMOS devices only in its current form. Only minor modifications are required to support pMOS devices (e.g. carrier mobility).

2. Junction effects are neglected in the analysis.

3. The effects of resistance between the contact and the source and the drain ends are neglected.

4. It is assumed that lateral thermal conductance is constant.

5. The body effect which describes the changes in the threshold voltage with a change in source-bulk potential has not be modeled.

6. The effects of leakage current on temperature distribution have not been modeled.

7. Channel thermal noise has not been considered.

8. The effects of substrate thermal noise have not been modeled.

6.3 Future work

The analytical approach can be fine-tuned in the future for thermal analysis taking into account the effect of various physical parameters (e.g. junction depth, variation in the lateral thermal conductance etc.). The next improvements in HeatMOS© would be to make it capable of estimating the pMOS channel temperature. This can be easily by including the pMOS device compact model parameters in HeatMOS© calculations and the analytical solution would be same as for the nMOS. The only difference is that in case of pMOS the charge carriers are holes instead of electrons so the physical properties of holes needs to be incorporated instead of electrons.

The effect of varying lateral thermal conductance can be taken into account along with the effect of contact resistance on thermal behavior. For full-chip thermal analysis and for EMR verification (Labun and Jagjitkumar, 2008), the M-network (Figure 3.7) can be connected to full micro-chip interconnects network and an interconnect network temperature estimation tool (e.g. Therminator) can be used to do full-chip thermal analysis.

The effects of process variation and leakage currents on temperature distribution can also be modeled. The analytical approach can be extended for double gate FinFET devices temperature estimation. However for nano-scale FinFET devices of below 90 nm geometries, the electron-phonon heat transport needs to be modeled. One idea may be to include the heat transport by phonon-electron interaction for a differential slice of the channel in the channel heat differential equation and solve the resultant differential equation. BTE (Boltzmann's transport equation) for

phonons may be quite useful to model the phonon's heat conduction in a differential slice of the channel. The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the gate of the device (Figure 6.1). The heart of FinFET is a thin ($\sim$ 10 nm) *Si* fin which serves as the body of the MOSFET (Hisamoto et al., 2000). A heavily doped poly-Si film wraps around the fin and makes electrical contact to vertical faces of the fin. The two faces of the fin act as two gates in place. The channel temperature estimation of such a device can be done by first splitting the channel between three regions: 1) region between the source end to left face of the fin 2) region between the left face and the right face of the fin and 3) the region between right face and the drain end of the transistor. With these partitions a similar approach could be taken to find the analytic solution for each region. However the shape of the each region of the FinFET's channel needs to be considered carefully. Also since the fin has nano-scale dimensions, the nanoscale effects (e.g. phonos heat conduction, thermal noise etc.) need to be considered in order to accurately estimate the channel temperature of FinFET device.

The proposed analytical approach is faster than numerical approaches. HeatMOS© can be modified to do temperature estimation for all transistors in a micro-chip based on its layout information. With some modifications in HeatMOS©, it can be possible to read the layout information from the industry standard layout exchange format, GDSII (Graphic Database System Information Interchange) stream format. The effects of channel thermal noise can also be modeled. It could be possible to do thermal analysis with more advanced device compact models, e.g. BSIM4 using the HeatMOS©.

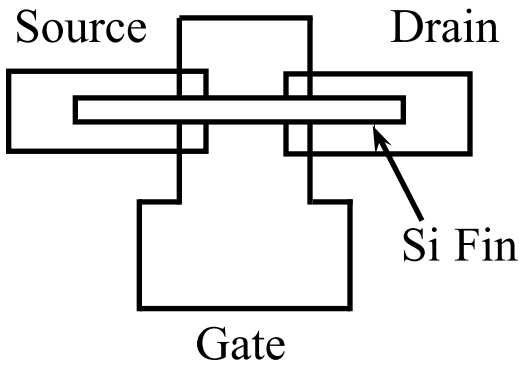

Figure 6.1: FinFET typical layout and schematic cross-sectional structures (Hisamoto et al., 2000)

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Appendix A

BSIM3 Model Parameters

The table A.1 provides the list of BSIM3 parameters for nMOS transistor used in HeatMOS©. The table A.2 provides the list of some other parameters used.

Table A.1: BSIM3 Parameters used in HeatMOS©

Parameter	Description	Value	Unit
Vth0	Threshold voltage	0.3696386	V
μ0	Mobility	670.0	cm^2/Vs
vsat	Saturation velocity	86301.58	m/s
Wl	Coefficient of length dependance for width offset	0.0	m^{Wln}
Wln	Power of length dependence for width offset	0.0	none
Wwn	Power of width dependence for width offset	1.0	none
Ww	Width dependence for width offset	0.0	m^{Wwn}
Wwl	Length and width cross term for width offset	0.0	$m^{Wwn+Wln}$
Ll	Length dependence for length offset	0.0	m^{Lln}
Lln	Length dependence for length offset	1.0	none
Lw	Width dependence for length offset	0.0	m^{Lwn}
Lwn	Width dependence for length offset	0.0	none
Lwl	Length and width cross term for length offset	0.0	$m^{Lwn+Lln}$
Lint	Length offset fitting parameter	$1.69494e-8$	m
Tox	Gate oxide thickness	$1.5e-8$	
Nsub	Substrate doping concentration	$6.0e16$	cm^{-3}

Table A.2: Other parameters used in HeatMOS©

Parameter	Description	Value	Unit
K	Boltzmaan constant	1.38×10^{-23}	$m^2kgs^{-2}K^{-1}$
ε_r	Oxide dielectric constant	3.9	none
ε_o	Permitivity of air	8.85×10^{-12}	F/m

Appendix B

SPICE Netlist

The SPICE codes for the devices under test have been provided below.

Program B.1 SPICE netlist "v8-nmos.spice" the nMOS transistor

```
* SPICE3 file created from ../Magic/Work/v1-nmos.ext
* technology: scmos
.option scale=0.01u
M1000 1 2 0 0 N1 w=40 l=18
 + ad=200000 pd=1800 as=200000 ps=1800

.include bsim3.lib

VDS 3 0
VGS 2 0
VIDS 3 1

.DC VDS 0 2.5 0.05 VGS 0 2.5 1

.control
set color0=white
set color1=black
run
plot i(VIDS)
.ENDC

.END
```

Program B.2 SPICE netlist "v7-nmos.spice" of the nMOS transistor

```
* SPICE3 file created from ../Magic/Work/v1-nmos.ext
* technology: scmos
.option scale=0.01u
M1000 1 2 0 0 N1 w=40 l=28
 + ad=200000 pd=1800 as=200000 ps=1800

.include bsim3.lib

VDS 3 0
VGS 2 0
VIDS 3 1

.DC VDS 0 2.5 0.05 VGS 0 2.5 1

.control
set color0=white
set color1=black
run
plot i(VIDS)
.ENDC

.END
```

Appendix C

Numerical Solution of the Heat Equation

The differential equation 3.20 can be solved by finite difference numerical method.

Let us consider,

$$T = f(x)$$

$$T(x) = \begin{cases} T_1(x_1) & 0 \leq x_1 \leq L_1 \\ T_2(x_2) & 0 \leq x_2 \leq L_2 \end{cases}$$

$$x_2 = x - L_1$$

$$L = L_1 + L2$$

Function $T(x)$ has a complex nature. For a length from 0 to L_1, it has temperature distribution given by function $T_1(x)$, and for length from L_1 to L, it has temperature distribution given by function T_2. Let us consider that the function T_1 is evaluated on J_1 number of points and T_2 is evaluated at J_2 number of points. T_j^1 is $T_1(x_j)$, the value of temperature function T_1 at point numbered x_j and T_j^2 is $T_2(x_j)$, the value of temperature function T_2 at point numbered x_j, T_j is the value of function T at point numbered x_j.

$\triangle x_1 = \frac{1}{J_1}; \triangle x_2 = \frac{1}{J_2}; J = J_1 + J_2;$

The differential equations 3.20 and 3.23 can be written as

$$T^{"} = \xi_1^2 T_1 - \xi_1^2 T^{ref} - \Psi^2 e^{\alpha x}; 0 \leq x \leq L_1$$

$$T^{"} = \xi_2^2 T_2 - \beta; L_1 \leq x \leq L$$

For each $0 \leq j \leq (J-1)$, the above equations can be written by using the Taylor's theorem as following.

$$\frac{T_{j-1}^1 - 2T_j^1 + T_{j+1}^1}{\triangle x_1^2} = \xi_1^2 T_j^1 - \xi_1^2 T^{ref} - \Psi^2 e^{\alpha x_j}; 0 \leq x_j \leq L_1$$

$$\frac{T_{j-1}^2 - 2T_j^2 + T_{j+1}^2}{\triangle x_2^2} = \xi_2^2 T_j^2 - \beta; L_1 \leq x_j \leq L_2$$

For the boundary conditions,

$T_0^1 = TO; T_J^2 = TL.$

The above equations can be solved using any matrix solver. The pseudo code of this approach has been given below. This can be solved using other software programs, e.g. Matlab, Octave.

```
% finite difference method

%————————————-

% ./HeatMOS -SourceTemp 318 -DrainTemp 324 -RefTemp 298 -VGS 1.2 -VDS
1.8 -Netlist v8-nmos.spice

%————————————-

format long;

%————————————————————————————————————

% Test scenario 1 : Verification test 1

% SourceTemp = 575; DrainTemp = 567; RefTemp = 456; VGS = 1.0;

% VDS = 1.5; Ids=2mA; v7-nmos.spice

%————————————————————————————————————

len1 = 2.093229e-07; len2 = 3.677829e-08;
```

xie1 = 8.791518e+00; psi1 = 5.274110e-10; alpha1 = 1.803726e+07;

xie2 = 8.791518e+00; beta2 = 3.790852e+16;

TO = 5.650000e+02; TL = 5.670000e+02; TRef = 4.560000e+02;

%——

% Test scenario : Verification test 2

% SourceTemp = 575; DrainTemp = 567; RefTemp = 456; VGS = 1.5;

% VDS = 1.5; v7-nMOS.spice

%——

% xie1 = 8.791518e+00; psi1 = 5.274110e-10; alpha1 = 1.803726e+07;

% xie2 = 8.791518e+00; beta2 = 3.790852e+16;

% TO = 5.650000e+02; TL = 5.670000e+02; TRef = 4.560000e+02;

% len1 = 2.093229e-07; len2 = 3.677829e-08;

%——-

% Test scenario : Verification test 3

% SourceTemp = 565; DrainTemp = 567; RefTemp = 456; VGS = 1.5;

% VDS = 1.5; v8-nMOS.spice

%——-

% xie1 = 1.077370e+01; psi1 = 5.808510e-11; alpha1 = 5.279674e+07;

% xie2 = 1.077370e+01; beta2 = 7.736773e+15;

% TO = 5.650000e+02; TL = 5.670000e+02; TRef = 4.560000e+02;

% len1 = 1.095764e-07; len2 = 3.652475e-08;

%——

%——

% Test scenario : Verification test 4

% SourceTemp = 10; DrainTemp = 10; RefTemp = 10; VGS = 1.5;

% VDS = 1.5; v8-nMOS.spice

%——-

% xie1 = 6.774943e+00; psi1 = 2.029696e-12; alpha1 = 1.793608e+07;

% xie2 = 6.774943e+00; beta2 = 1.389513e+17;

% TO = 1.000000e+01; TL = 1.000000e+01; TRef = 1.000000e+01;

% len1 = 1.095764e-07; len2 = 3.652475e-08;

%——-

%——-

% Test scenario : Saturation test 1

% SourceTemp = 325; DrainTemp = 325; RefTemp = 300; VGS = 1.5;

% VDS = 1.5; v8-nMOS.spice

% ————————————————————————————————————

% xie1 = 1.038507e+01; psi1 = 3.964484e-11; alpha1 = 4.897557e+07;

% xie2 = 1.038507e+01; beta2 = 1.092628e+16;

% TO = 3.250000e+02; TL = 3.250000e+02; TRef = 3.000000e+02;

% len1 = 1.095764e-07; len2 = 3.652475e-08;

%————————————————————————————————————

%————————————————————————————————————

% Test scenario : Saturation test 2

% SourceTemp = 325; DrainTemp = 325; RefTemp = 300; VGS = 1.8;

% VDS = 2.2; v8-nMOS.spice

%————————————————————————————————————

% xie1 = 1.027263e+01; psi1 = 6.417728e-11; alpha1 = 4.839836e+07;

% xie2 = 1.027263e+01; beta2 = 2.434460e+16;

% TO = 3.250000e+02; TL = 3.250000e+02; TRef = 3.000000e+02;

% len1 = 1.084309e-07; len2 = 3.767029e-08;

%————————————————————————————————————-

%————————————————————————————————————-

% Test scenario : Saturation test 3

% SourceTemp = 325; DrainTemp = 325; RefTemp = 300; VGS = 5.0;

% VDS = 5.0; v8-nMOS.spice

%————————————————————————————————————

% xie1 = 8.673537e+00; psi1 = 7.965811e-10; alpha1 = 3.447079e+07;

% xie2 = 8.673537e+00; beta2 = 3.913625e+17;

% TO = 3.250000e+02; TL = 3.250000e+02; TRef = 3.000000e+02;

% len1 = 1.063123e-07; len2 = 3.978895e-08;

%————————————————————————————————————

%————————————————————————————————————

% Test scenario : Saturation test 4

% SourceTemp = 325; DrainTemp = 325; RefTemp = 300; VGS = 5.0;

% VDS = 5.0; v7-nMOS.spice

%————————————————————————————————————

% xie1 = 9.219493e+00; psi1 = 4.448968e-10; alpha1 = 2.028882e+07;

% xie2 = 9.219493e+00; beta2 = 2.621273e+17;

% TO = 3.250000e+02; TL = 3.250000e+02; TRef = 3.000000e+02;

% len1 = 2.062546e-07; len2 = 3.984658e-08;

%——-

%——-

% Test scenario : Saturation test 5

% SourceTemp = 318; DrainTemp = 324; RefTemp = 298; VGS = 1.2;

% VDS = 1.8; v8-nMOS.spice

%——-

% xie1 = 1.109780e+01; psi1 = 1.988555e-11; alpha1 = 5.635639e+07;

% xie2 = 1.109780e+01; beta2 = 8.011858e+15;

% TO = 3.180000e+02; TL = 3.240000e+02; TRef = 2.980000e+02;

% len1 = 1.090203e-07; len2 = 3.708086e-08;

%——

%——

% Test scenario : Ohmic test 1

% SourceTemp = 300; DrainTemp = 325; RefTemp = 300; VGS = 1.0;

% VDS = 0.1; v8-nMOS.spice

%——

% xie1 = 4.472554e+00; psi1 = 8.362492e-12; alpha1 = 8.520509e+02;

% xie2 = 4.472554e+00; beta2 = 7.811362e+10;

% TO = 3.000000e+02; TL = 3.250000e+02; TRef = 3.000000e+02;

% len1 = 1.173697e-07; len2 = 2.873146e-08;

%——

%——

% Test scenario : Ohmic test 2

% SourceTemp = 318; DrainTemp = 324; RefTemp = 300; VGS = 1.0;

% VDS = 0.1; v7-nMOS.spice

%——

% xie1 = 4.472554e+00; psi1 = 4.964503e-12; alpha1 = 4.640764e+02;

% xie2 = 4.472554e+00; beta2 = 2.753005e+10;

% TO = 3.180000e+02; TL = 3.240000e+02; TRef = 3.000000e+02;

% len1 = 2.154926e-07; len2 = 3.060865e-08;

%——

```
lengthTotal = len1 + len2;

%J1 = 20; %J2 = 10;

J1 = 100;

J2 = 50;

dx1 = len1/J1;

dx2 = len2/J2;

xt1 = [0:dx1:len1] ;

x1 = xt1.' ;

xt2 = [0:dx2:len2] ;

x2 = xt2 .' ;

b = zeros(J1+J2, 1);

b(1)=TO;

b(J1+J2)=TL;

for i=2:(J1+J2-1)

if i < J1

b(i) = -(dx1^2)*(xie1^2)*TRef - (dx1^2)*(psi1^2)*(exp(alpha1*x1(i)));

elseif i > J1
```

```
b(i) = -(dx2^2)*beta2;

else

b(i) = 0.0;

endif

endfor

A=sparse(J1+J2, J1+J2);

A(1,1) = 1.0;

A(J1+J2, J1+J2) = 1.0;

for i=2:(J1+J2-1)

if i < J1

A(i, [i-1, i, i+1]) = [1.0, -(2.0-(xie1^2)*(dx1^2)), 1.0];

elseif i > J1

A(i, [i-1, i, i+1]) = [1.0, -(2-(dx2^2)*(xie2^2)), 1.0];

else

A(i, [i-1, i, i+1]) = [1.0/dx1, -(1.0/dx1 + 1.0/dx2), 1.0/dx2];

endif

endfor
```

```
Y=A\b;

for i=1:J1

x(i)=x1(i);

endfor

for j=1:J2

x(J1+j)=len1.+x2(j);

endfor

myfile = "chanTempFD.out" ;

FILE = fopen(myfile, "w");

for i=1:(J1+J2)

fprintf (FILE, "%e\t", x(i));

fprintf (FILE, "%e\n", Y(i));

endfor

fclose(FILE);

%————————————————————————————————
```

Appendix D

HeatMOS© Development

D.1 Development Environment

HeatMOS© has been developed in "C" programming language. It has been compiled using gnu c-compiler, g++4.0.1 for i686-apple-darwin9 machine. HeatMOS© has been executed on Apple MAC OS X version 10.5.8 machine with Intel Core 2 Duo 1 GHz processor and 1 GB of DDR2 SDRAM. To plot graphs Gnuplot version 4.4 software has been used. Octave version 3.2.3 software has been used for the numerical solution of the channel heat equation.

D.2 A Sample HeatMOS© Execution

A screen snapshot of sample HeatMOS© execution is split in two parts and shown in Figure D.1 and D.2. The top line in Figure D.1 shows the command for HeatMOS© execution. The temperature distribution along the length of the channel in being output in a text file, which can be used to plot graphs using a graph plotting software (e.g. gnuplot).

```
A301739:HeatMOS harajput$ ./HeatMOS -SourceTemp 318 -DrainTemp 324
 -RefTemp 198 -VGS 1.2 -VDS 1.8 -N v8-nmos.spice

==================================================
 !! HeatMos: MOSFET Channel Temperature Estimation !!
==================================================
Input parameters.....................
Source temperature TO = 3.180000e+02 K
Drain temperature TL = 3.240000e+02 K
Reference temperature TRef = 1.980000e+02 K
SPICE netlist = v8-nmos.spice

Gate voltage Vgs = 1.200000e+00 V
Drain voltage Vds = 1.800000e+00 V
Substrate voltage Vbs = -6.000000e-01 V
Threshold voltage Vth = 3.696986e-01 V
.....................................
.....................................
Reading Netlist ...
NetList File=v8-nmos.spice
scale(0.01)
scale(1.000000e-02)
MOSFET Found...
width(40)
length(18)
.....................................
DL = 1.694940e-08
DW = 0.000000e+00
calChanRho: inConc(1.000000e+23)
calChanRho: dopingConcSub(1.000000e+23)
calChanRho: u0(6.700000e-02)
calChanRho: eCharge(1.600000e-19)
rhoChan: rhoChan(1.554726e-03)
heightSource: Boltz(1.380000e-23)
heightSource: q(1.600000e-19)
heightSource: epsO(8.860000e-12)
heightSource: epsR(3.900000e+00)
heightSource: phiS(2.694731e-01)
heightSource: Na(6.000000e+22)heightSource: heightO(3.610371e-06)
calcLen2: VDS(-1.881905e-01)voltDS(1.800000e+00)
calcLen2: q(1.600000e-19)vsat(8.630158e+04)Nsub(6.000000e+22)
calcLen2: epsSi(1.040000e-10)u0(6.700000e-02)
calcLen2: len2(3.708086e-08)
calcLen2: El(5.361770e+07)
calcLen2: voltDS-VDS(1.988191e+00)
Channel Rho = 1.554726e-03
lDrawn = 1.800000e-07
wDrawn = 4.000000e-07
lEff = 1.461012e-07
wEff = 4.000000e-07
```

Figure D.1: A sample HeatMOS run part 1

```
thermK = 4.000000e-01
heightO = 3.610371e-06
heightP = 1.166275e-08
heightPoly = 7.220742e-06
heightOx = 1.500000e-08
heightSub = 7.220742e-05
Channle rho = 1.554726e-03
.................................

Electric Current Ids = 1.456564e-01 mA

Temperature Calculation Starts...
calcLen2: VDS(-1.881905e-01)voltDS(1.800000e+00)
calcLen2: q(1.600000e-19)vsat(8.630158e+04)Nsub(6.000000e+22)
calcLen2: epsSi(1.040000e-10)u0(6.700000e-02)
calcLen2: len2(3.708086e-08)
calcLen2: El(5.361770e+07)
calcLen2: voltDS-VDS(1.988191e+00)

len1 = 1.090203e-07; len2 = 3.708086e-08;
calcChanTemp: thermResPoly2(1.384899e+11)
calcChanTemp: thermResOx2(6.666667e+13)
calcChanTemp: thermResSub2(1.384899e+10)
calcChanTemp: gLat1(7.222242e-11), gLat2(7.222242e-11)
calcChanTemp: gLong1(6.274811e-13), gLong2(6.274811e-13)
calcChanTemp: K1(6.750389e-38),K2(9.789946e+13)

xie1 = 1.072842e+01; psi1 = 1.366793e-11; alpha1 = 5.260639e+07;
xie2 = 1.072842e+01; beta2 = 1.126813e+16;
TO = 3.180000e+02; TL = 3.240000e+02; TRef = 1.980000e+02;

calcChanTemp: A1(2.339232e-06),A2(-7.956383e-07)
calcChanTemp: A3(2.145684e+01);A4(2.145684e+01)
calcChanTemp: B1(-3.894626e+07);B2(1.050307e+15)
C1 = 4.386083e+06; C2 = -4.385963e+06;
D1 = -4.894973e+13; D2 = -4.894973e+13;
calcChanTemp: ElementSizeLen1(1.090203e-09)
calcChanTemp: ElementSizeLen2(7.416172e-10)
caclChanTemp: resChan2(1.235785e+04)
calcChanTemp: TEST0 T1(x=0)tempO  3.180000e+02 ===
calcChanTemp: TEST1 T2(x=L2)tempL 3.240000e+02 ===
calcChanTemp: TEST2 T1(x=L1)  3.282599e+02 ===
calcChanTemp: TEST3 T2(x=0) 3.282656e+02 ===
calcChanTemp: TEST4 gLong1*dT1/dx; x=L1 5.905236e-05 ===
calcChanTemp: TEST5 gLong2*dT2/dx; x=0 5.905236e-05 ===
calcChanTemp: TEST6 alpha^2-xie^2; 2.767432e+15 ===

Average channel temperature TavgAnalytic = 3.288883e+02 K
Maximum channel temperature TmaxBruteForce = 3.286562e+02 K at poi
nt x = 1.171781e-01 um
Channel temperature at pinch-off point Tpinch = 3.282599e+02 K at
point x = 1.090203e-01 um

==========================================
!! Channel Temperature Calculations Finished !!
==========================================
A301739:HeatMOS harajput$
```


Figure D.2: A sample HeatMOS run part 2