Photonic Device Design Flow

From Masklayout to Device Measurement

by

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B.A.Sc., The University of British Columbia, 2009

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF
THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF APPLIED SCIENCE

in

The Faculty of Graduate Studies

(Electrical and Computer Engineering)

THE UNIVERSITY OF BRITISH COLUMBIA

(Vancouver)

October 2012

Abstract

Mask layout design is an important part in silicon photonic device design flow; the space used and the quality of the mask directly affect the cost of fabrication and quality of the outcome. To effectively minimize time spent on drawing masks, fixing design violations, and reducing unused spacings between each structure, we use effective approaches in the mask design process to ensure the listed criteria are met. Using the PCell and the hierarchy drawing methods, GDS files that contain different device parameters can be generated efficiently. As a result, direct GDS modeling efficiency is improved. An experimental setup that is capable of obtaining high quality measurement data is critical to device measurement. The concept of an automated measurement station can effectively reduce work needed from the experimenter while providing quality results. With the implemented fiber-to-fiber and fiber array automated measurement station, multi-device measurement can be set up to run automatically in minutes whereas traditional manual measurement stations require one's presence and constant attention. In this thesis, we have illustrated several mask drawing approaches and showed the drawing steps of two masks in detail. We have described two automated experimental setups, fiber-to-fiber and fiber array, in detail and included various measurement results to show the capabilities of these two stations.

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Acknowledgments

I would like to thank my supervisor Dr. Lukas Chrostowski and professor Dr. Nicolas A.F. Jaeger for all the help and guidance they provided when I encountered difficulties in my research. Especially, I would like to thank Dr. Lukas Chrostowski for exposing me to the field of silicon photonics and providing me with such wonderful research experiences. I would also like to thank my parents for their unconditional love and support throughout the years of my education. Lastly, to all my colleagues, thank you for your support and guidance.

Chapter 1

Introduction

The dominant application of silicon photonics is in the optical interconnect technology [1,2]. Silicon photonics, a topic of advanced research, can be applied in high-performance computing, biological and chemical sensing, environmental monitoring, and medical and military technologies [2]. As the performance of silicon photonic designs continue to improve, the designs become more complex year after year. As a result, the steps involved in the design procedure are required to be refined as well.

The typical traditional photonic design steps are:

1. A design is modeled and simulated for its feasibility.
2. Designs are manually drawn into mask files with optimal parameter iterations.
3. The complete mask is sent to foundry for fabrication.
4. Construct a chip-testing station and measure the fabricated devices.
5. Publish the obtained results if they meet the standard.

As the demand for improvement in current state-of-the-art technology increases, silicon photonics has become a popular research topic in recent years. As technology improves, the foundries are now capable of offering more extensive fabrication procedures. These procedures include multiple depths of silicon etching, various concentrations of doping, and metal depositions. Research groups that focus on silicon photonic technology have also evolved from experimenting with simple photonic structures, such as ring resonators and straight waveguides, into studying more complicated systems. As a result, the importance of efficient mask design and device testing becomes more significant. Hence, the traditional design steps must evolve to meet the current research demands. The improved photonic design flow should emphasize on maximizing the efficiency and quality of the design flow while minimizing total design time. The improved design flow is illustrated in the following flowchart:

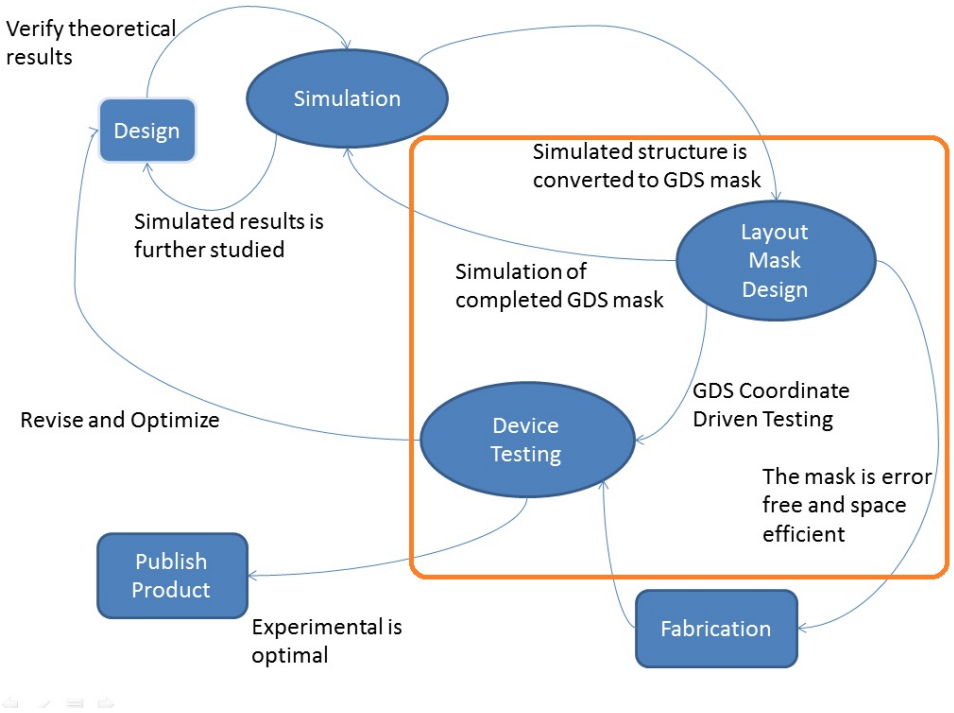


Figure 1.1: Photonic Design Flowchart

The focus of my thesis contribution is primarily on mask layout design and device testing (as highlighted in the orange box in the above flowchart). The first goal of my work is to generate space-efficient, error-free mask designs that fit the simulated performance requirements. To achieve this, the mask designer must communicate with the simulator frequently to determine the critical parameters of the design and the basic physical form of the device. Unlike in traditional design flow, where mask drawing is a one-time labor work, the simulation process and the mask layout procedure must now occur simultaneously to make the optimization of the device mask design possible. To improve communication efficiency, the mask design method must be carefully chosen so it can adapt to the parameter requirements needed. A well-designed final mask layout possesses the following characteristic:

- Can adapt to last minute changes
- Can be regenerated and reused for further design cycles

- Fits the experimental testing constrains
- Meets the fabrication requirements
- Is Space-Efficient
- Is Error-free

Traditionally, device testing is carried out manually and hence requires the presence of an experimenter. The second goal of my work is to construct automated measurement stations that provide GDS coordinate-driven testing. The purpose of the automated measurement system is to significantly reduce the work and time needed to obtain experimental results. GDS coordinate-driven testing uses grating coupler locations on the mask file as a reference to deduce the traveling path of the input/output fibers or fiber array for automated photonic device testing. Setting up a measurement station properly in order to obtain accurate results with maximized coupling efficiency and minimized noise level is important. It is ideal to have a well calibrated experimental setup and design the mask accordingly to minimize measurement work required. A well-calibrated experimental setup has the following characteristics:

- A stable measurement environment
- Properly angled optic fiber(s) to ensure maximum coupling efficiency
- An effective microscope setup that can provide clear view of the device and fiber during experiments
- Stages that allow easy fiber movement in all directions and fiber angle adjustments

1.1 Thesis Contributions

I am mainly involved in mask layout designs and device measurements. I have created a script library in Pyxis where each script represents a mask layout design PCell and built two automated setups in collaboration with Han Yun which are now being used in SiEPIC and CMC workshops. My supervisor, Dr. Lukas Chrostowski, has guided me by providing innovative ideas and concepts.

The publications that I am involved in are:

1. W. Shi, X. Wang, W. Zhang, H. Yun, C. Lin, L. Chrostowski, and N. A. F. Jaeger, "Grating-coupled silicon microring resonators", *Applied Physics Letters*, vol. 100, no.12, pp. 121118, 2012.

2. W. Shi, H. Yun, T. K. Chang, W. Zhang, C. Lin, N. A. F. Jaeger, L. Chrostowski, "Differential measurement of transmission losses of integrated optical components using waveguide ring resonators, *Photonics North*, Montreal, Canada, 2012.

3. C. Lin, L. Chrostowski, and N. A. F. Jaeger, "Design and Characterization of Embedded Ring Resonators, *The 15th Canadian Semiconductor Science and Technology Conference*, Vancouver, Canada, 2011.

4. W. Shi, X. Wang, C. Lin, H. Yun, Y. Liu, T. Baehr-Jones, M. Hochberg, N. A. F. Jaeger, and L. Chrostowski, "Electrically tunable resonant filters in phase-shifted contra-directional couplers", *IEEE Group IV Photonics Conference*, 09/2012

5. W. Shi, M. Greenberg, X. Wang, Y. Wang, C. Lin, N. A. F. Jaeger, and L. Chrostowski, "Single-band add-drop filters using anti-reflection, contra-directional couplers", *IEEE Group IV Photonics Conference*, San Diego, USA, pp. WA7, 09/2012.

6. W. Shi, H. Yun, W. Zhang, C. Lin, T. K. Chang, Y. Wang, N. A. F. Jaeger, L. Chrostowski,"Ultra-compact, high-Q silicon microdisk reflectors", *Optics Express*, vol. 20, issue 20, pp. 21840-21846 , 09/2012.

1.2 Thesis Organization

This thesis consists of five chapters. The first chapter introduces the evolved photonic device design flow and the importance of my thesis contribution. The requirements that need to be met in order to generate quality mask layouts and construct well-calibrated automated stations are also included. In Chapter 2, we discuss in detail the mask layout drawing methods developed. Also, we show complete masks with detailed step-by-step mask design illustrations. In Chapter 3, we introduce the fiber-to-fiber automated setup constructed and include discussions that illustrate its performance. Chapter 4 gives an overview of the automated fiber array setup and studies the stability of the station through a series of experiments. Lastly, Chapter 5 concludes my thesis with suggestions for future work.

Chapter 2

Mask Layout Design

The layout program we primarily use is Mentor Graphic Pyxis but we have also experimented with other programs such as DW2000 and KLayout. DW2000 is a drawing tool developed by Design Workshop Technology. This program is the program choice for my first mask design [25]. A technology package is provided with basic PCells such as straight waveguides, tapers, arcs and circles. Since we are inexperienced, our mask designs are simple structures such as ring structures and straight waveguide testing devices, etc. The mask is generated by manually placing each PCell onto the layout and adjusting the PCell parameters such as waveguide length, width, and circle radius etc. The errors such as improperly connected waveguides and misplaced etch layer are fixed manually. KLayout is a free software developed by Matthias Köfferlein [27]. This layout software has a clean user interface and provides a hierarchy tree which can locate different designs effectively. The main attraction of KLayout is its capability of making direct modifications to GDS files without converting the complete mask layout to other formats. These features promotes KLayout to be the main choice for final mask reviewing. The mask layout figures shown in this chapter are displayed in KLayout. Pyxis is developed by Mentor Graphics. Besides basic manual drawing features, Pyxis provides a scripting platform that offers numerous ways to approach mask designing. To achieve the mask design criteria mentioned in the previous chapter and to work in a commercialized environment to fit industry needs, hierarchy drawing methods and PCell developments can provide the re-usability of the mask we needed. Hence, Pyxis is our primary choice for mask design development.

The mask layout portion of the photonic device design flow can be divided into three stages: planning stage, drawing stage, and finalizing stage. The planning stage requires the coordination between the simulator and the mask designer to conceptualize a draft structure based on the theoretical analysis of a new design. This draft includes the core design of the device and lists out the core parameters that influence the device performance. During the drawing stage, this draft design is laid out with a drawing tool and the physical feasibility of the design is considered along with its pro-

jected device performance. Communication is required frequently between the simulator and the mask designer in order for the design to meet the performance expectation and fabrication constraints. The finalizing stage includes routing, tiling, and error checking. By carefully choosing the routing method of the device and the locations of input/output couplers, we ensure that the fabricated mask is feasible for device testing and the allocated spaces are efficiently used. In this chapter, we start by discussing the scripting platform of Pyxis and move onto various scripting techniques. We introduce drawing approaches developed for photonic device mask designs in detail and give two step-by-step mask design examples along with the difficulty faced in each example and a justification for the drawing approach choice of each design.

2.1 Mask Drawing with Pyxis

2.1.1 Manual Drawing vs. Scripting Drawing

Pyxis has the option of manual drawing like all other layout tools. Pyxis' transcript window documents each manual action performed by the user and displays the corresponding line of code executed. To create the ring resonator showed in Figure 2.1, three PCell calls are executed; the add_shape() PCell generates rectangles that correspond to the input coordinates and the add_ring() PCell creates a ring structure based on the radius and layer inputs. Program 2.1 illustrates the corresponding code executed from manual inputs.

Program 2.1 Ring Resonator Script

```
$add_shape([[-10,5.2],[10,5.7]], "Layer1", @internalk, @nokeep, "drawing");
$add_shape([[-10,-5.2],[10,-5.7]], "Layer1", @internalk, @nokeep, "drawing");
$add_point_device("add_ring", @block, [], [@to, [0,0], @rotation, 0.0, @flip, "none"],
 [["layer", "1"],["radius1","5"],["radius2","4.5"]], @placed);
```

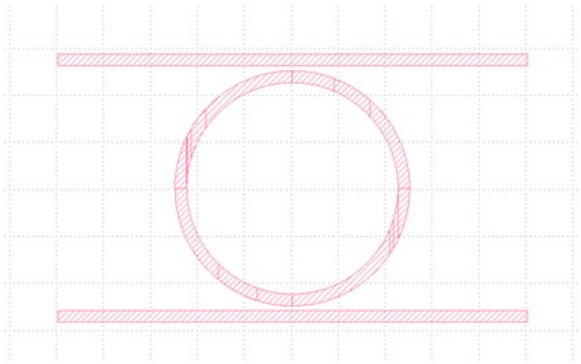


Figure 2.1: This disk resonator has a radius of 5 μm, waveguide width of 500 nm, and a gap size of 200 nm.

2.1.2 Library Components

Having a library of components is critical to layout drawings especially while working in collaboration with other people. Library components exist in two forms: existing GDS mask files and scripted PCells. Existing GDS masks can be re-used in new designs but this form of library component requires manual adjustments if one needs to change their physical footprint. On the other hand, PCell library components are more versatile; they are capable of function-like behaviors and generate the corresponding device according to the specified input values.

Common examples of GDS library components are the grating and edge coupler. These couplers are required in photonic designs because they are responsible for the input and output of the laser source. Grating couplers are sensitive to the wavelength of the input light [3]; therefore, different versions of grating coupler GDS masks are used for wavelengths ranging from 1450 to 1650 nm(see Figure 2.2). Edge couplers are tapers that gradually reduce the waveguide core width and output the light at the smaller end. These couplers have a higher coupling efficiency but are hard to align to a coupling fiber and require the coupler tips to be located at the chip edge.

The PCell examples we include here are the quarter-arc PCell and the transition taper PCell. To minimize loss when light is redirected around waveguide corners, a 90^o bend is used to guide the light. For a 220 nm high and 500 nm wide waveguide, the bend radius used is 5 μm (See Figure 2.3(a)). To minimize the loss when the light transitions between a strip waveguide to a ridge waveguide, a transition taper is applied to the transition

points (See Figure 2.3(b) for the generated mask example and Appendix A for the corresponding PCell script).

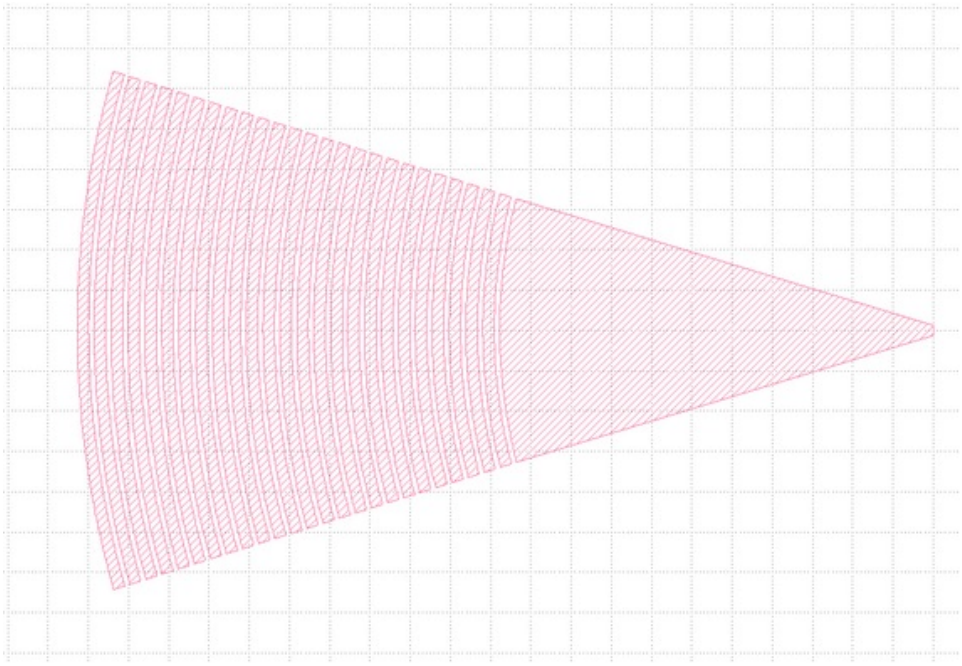
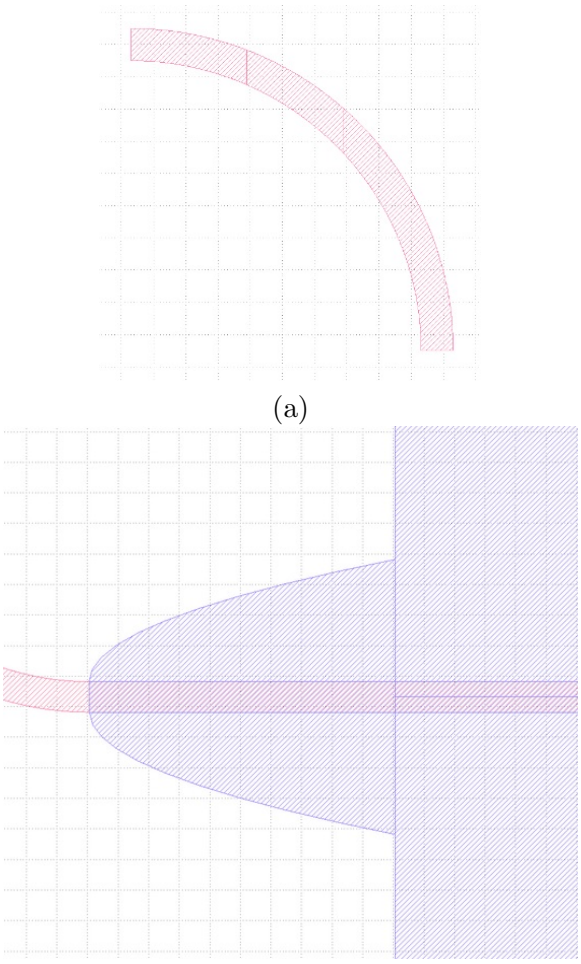


Figure 2.2: 1550 *nm* Grating Coupler [9]



(a)

(b)

Figure 2.3: (a) Quarter-Circle Arc PCell. (b) Transition Taper PCell.

2.1.3 Drawing Approaches

The physical nature of the device design must be considered prior to mask drawing in order to choose a suitable approach. For designs that require overwhelming repetition of the same structures, such as grating structure or multi-ring structure, we use GDS library components. For designs that have similar structures but different parameter variations, we use PCell library components. These drawing methods can be categorized into two primary

approaches: nested PCell approach and hierarchy approach.

The Nested PCell approach is a method that uses multiple PCells to create the final device structure. By inputing the parameter variations to the final PCell function using for-loops, we can generate complex device masks. The advantage of using this method is that the user only has to manage one PCell script. However, the final mask generated using this approach contains no hierarchy levels. Program 2.2 is an example of a ring resonator PCell created using nested PCell approach. Pyxis PCells' general form contains three functions; in this example, the functions are ring_resonator(), build_ring_resonator(), and ring_resonator_parameters(). By defining input parameters - gap, radius, and waveguide_width - in the basic functions, the code illustrated in Program 2.1 is parameterized into a nested PCell that generates ring resonator structures.

The hierarchy approach generates the final GDS layout by using GDS library components. Hence, the final layout is formed by a hierarchy of sub-layout files. The advantage of this approach is that it avoids the re-creation of identical structures. Referring to a pre-existing GDS effectively reduces the final mask layout file size and script drawing time compared to the nested PCell approach. The disadvantage of this approach is that managing the sub-cell files is troublesome when the required parameter iterations increase. To prepare for the final mask generation, the sub-cell GDS files with different parameters are generated first through sub-cell generation script. During the final mask generation, these generated sub-cells are referenced and placed onto the mask accordingly. The generation of the final mask layout uses an execution file (it is called a do-file in Pyxis) that defines the location of these these sub-cells. Program 2.3 is an example script that creates a ring sub-cell. The execution of this script uses input parameters that defines a ring structure as the cell name and creates the ring structure accordingly to generate the sub-cell.

Program 2.2 Pyxis Parameterized Device Script

```
function ring_resonator ()
{
    local device = %get_device_iobj();
    local gap = $get_property_value(device, "gap");
    local radius = $get_property_value(device, "radius");
    local waveguide_width = $get_property_value(device, "waveguide_width");
    build_ring_resonator(gap, radius, waveguide_width);
}
function build_ring_resonator(gap:number (default=0.2), radius:number
(default=5), waveguide_width:number (default=0.5))
{
    $add_shape([[-10,radius+gap],[10,radius+gap+waveguide_width]],"Layer1", @internalk,
    @nokeep, "drawing");
    $add_shape([[-10,radius+gap],[10,radius+gap+waveguide_width]],"Layer1", @internalk,
    @nokeep, "drawing");
    $add_point_device("add_ring", @block, [], [@to, [0,0], @rotation, 0.0, @flip, "none"],
     [["layer", "1"],["radius1",radius],["radius2",radius-waveguide_width]], @placed);
}
function ring_resonator_parameters(gap: optional number (default 0.2),
radius: optional number (default 5), waveguide_width: optional number (default 0.5))
{
    return[["gap",$g(gap)],["radius",$g(radius)],["waveguide_width",$g(waveguide_width)]];
}
```

Program 2.3 Pyxis Script: Hierarchy Approach

```
function ring_cell(gap:number (default=0.2), radius:number
(default=5), waveguide_width:number (default=0.5)
{
    local device_name=$format("gap_%1d_rad_%1d_width_%1d_ring",
    gap,radius,waveguide_width)
    $create_cell(device_name, @block, @geometry_editing, @ninety, "","")
    $reserve_cell();

    $add_point_device("add_ring", @block, [], [@to, [0,0], @rotation, 0.0, @flip, "none"],
     [["layer", "1"],["radius1",radius],["radius2",radius-waveguide_width]], @placed);

    $save_cell(@all);
}
```

2.1.4 Routing

Routing is an important step in designing layouts. A well thought out routing method can minimize a large amount of empty spacings, and thus allow more devices to be packed into the final layout. However, device packing is not the only concern; we must take into account the measurement setup constrains as well. For example, active mask designs require additional probes for current injection. Therefore, there are limited ways of positioning the input, output couplers and the n-doped and the p-doped contacts. Given all the constrains, it is challenging to come up with a suitable routing method that provides convenient chip testing and reduces empty spacings (see Section 2.2.2 for a detailed routing example).

2.1.5 Error Checking

In order for the fabricated device to meet the performance expectation, the mask submitted to the foundry is required to be error free. A rule file is provided by the foundry and is used to identify mistakes and violations. Using Pyxis' error checking platform, errors are identified and highlighted (see Figure 2.4). The error illustrated in this example is the acute angle error. Other examples of common errors and violations include:

- Misaligned waveguides
- Minimum spacing violation
- Minimum feature size violation
- Enclosure violation
- Layer density violation

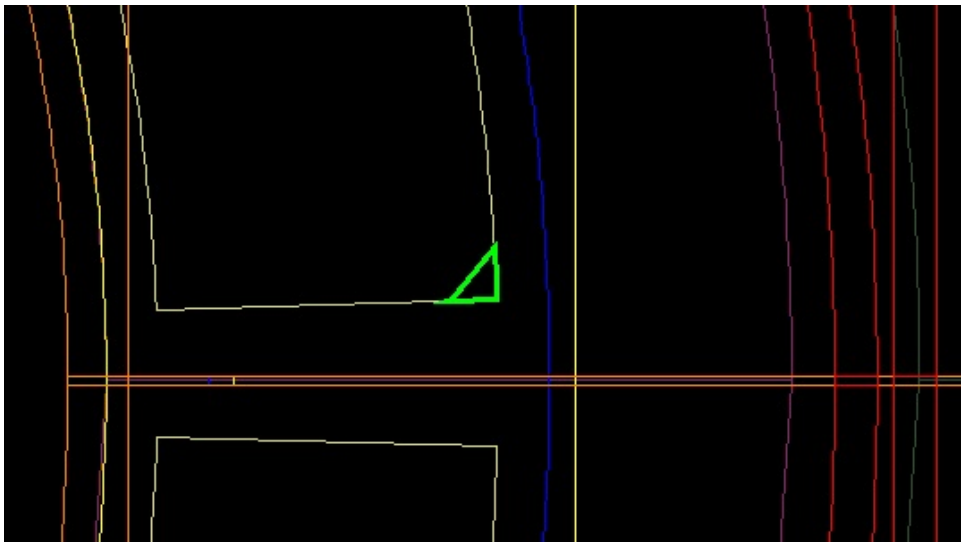


Figure 2.4: Error Checker Display in Pyxis

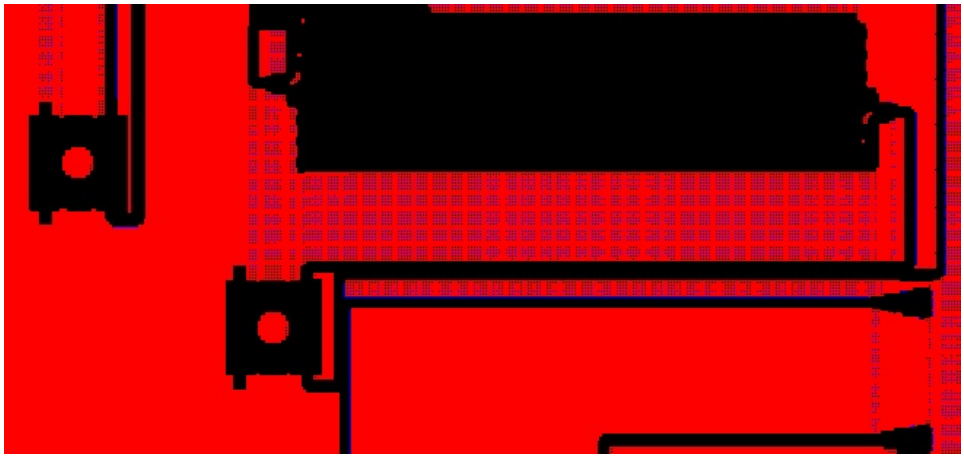


Figure 2.5: Tiling Mask

2.1.6 Tiling

The silicon layers and the metal layers in the fabrication process require the density of silicon or metal to be within a given margin; these density rules are

included in the error checking rule file. These density rules are implemented so the etched material density is within a margin during lithography. In the cases where the densities are not met, we tile in dummy features, such as a tiny square, in the empty spacings to raise the overall density of the particular layer. Keep-out layers are used to cover delicate design features so they will not be sabotaged by the tiling script. Figure 2.5 shows a typical tiled layout. This mask is tiled in the silicon layer, and two metal layers.

2.2 Completed Mask Designs

To demonstrate the mask design flow described in the previous section in detail, two complete mask examples are included in this section: the traveling wave modulator mask and the on-chip optical circuit. Both of the example masks are fabricated under the OpSIS IME process [4]. An illustration of the fabrication procedure is shown in Figure 2.6.

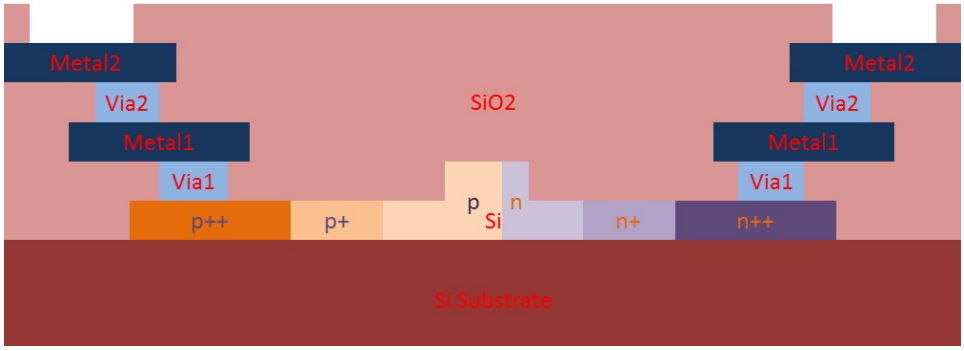


Figure 2.6: Fabrication Process Illustration

2.2.1 Traveling Wave Modulator

In this section, we describe the traveling wave modulator design in detail. This example is chosen to be included in this thesis because it implements the new design flow introduced in Chapter 1. The traveling wave modulator project emphasizes the importance of simulation-to-layout design loop. Frequent communications established between the mask designer and simulator achieve the optimization needed both in device performance simulation and final mask physical footprint [5]. The objective of this design is to reach a high speed operation of 25 $\frac{Gb}{s}$ to 40 $\frac{Gb}{s}$ with high extinction ratio and

match the performance specifications of the current state-of-the-art modulators [2]. The physical structure of this design is similar to the traditional Mach-Zehner Interferometer (MZI); the modulation of the signal is achieved by introducing a π phase shift difference between the two waveguides. The use of traveling wave electrodes allows for high-speed operation through using a depletion-mode reverse-biased diode. Due to its long length (mm), it operates at a low drive voltage and allows wide optical bandwidth operation [6]. The key of this design is achieving a velocity synchronization between the traveling wave electrode microwave velocity and optical signal velocity [6]. To address this, the structure proposed for the traveling wave modulator uses a capacitively loaded fin microwave waveguide, known as a slow-wave electrode [19]. Extended optical path lengths are implemented by "snaking" the optical waveguides to reduce the overall device footprint. The challenge of this design is minimizing loss from the parasitic resistance and capacitance introduced by the proposed structure while ensuring the optical signal velocity and electrode microwave velocity perfectly match.

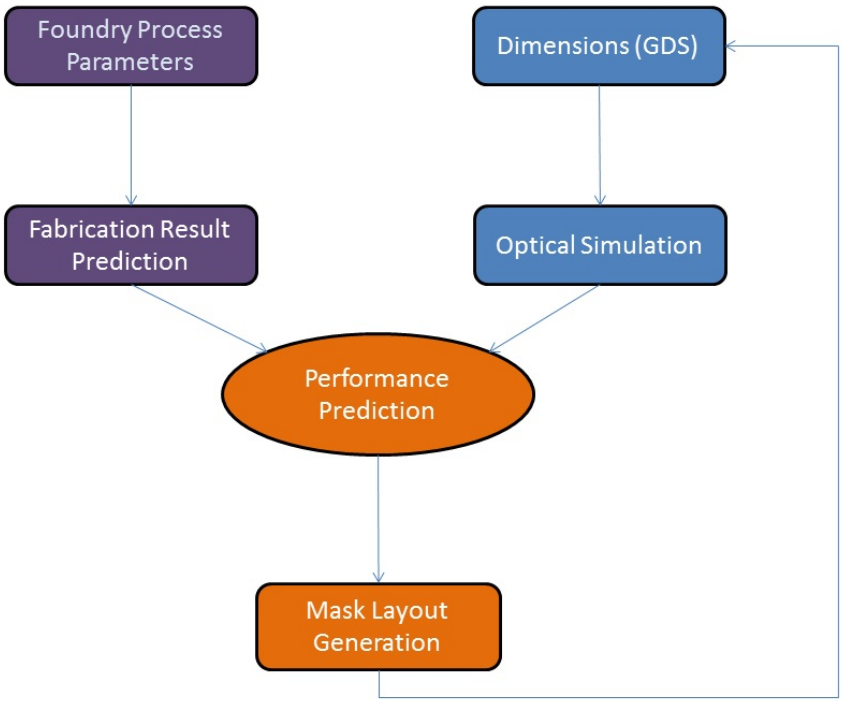


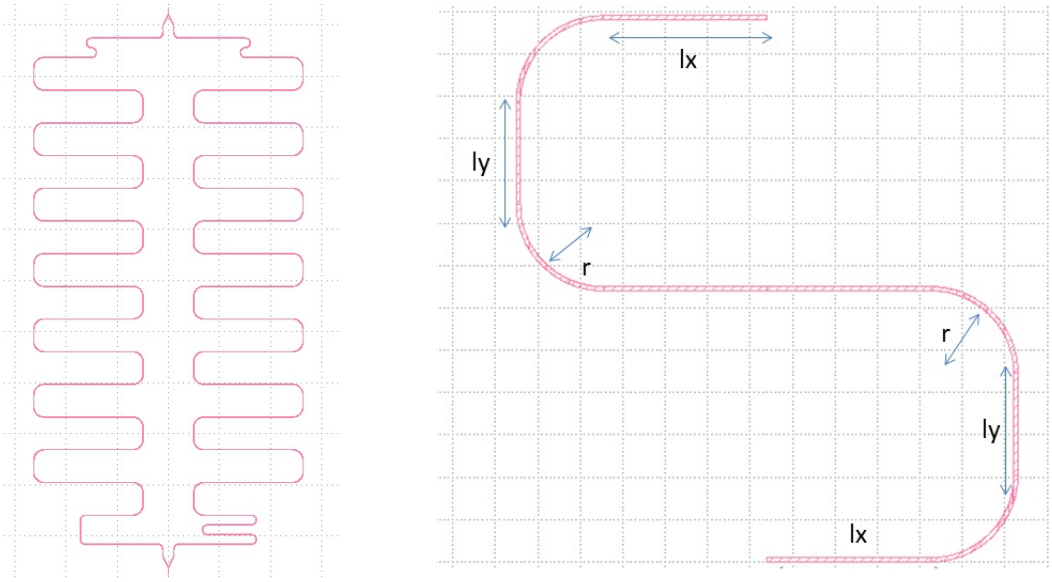
Figure 2.7: Traveling Modulator Design Flow

Modulator modeling, a major portion of the traveling wave modulator design, is carried out as illustrated in Figure 2.7. The foundry process simulations [4], the optical performance simulations [5], and the PCell design of this structure are carried out simultaneously. Device dimensions are adjusted and the generated GDS is fed to programs such as Sonnet or FDTD for direct GDS simulation. The OpSIS IME fabrication process offers the following features:

- Strip and Ridge Waveguide
- n, p doping for PN junction
- n+, p+ transition doping
- n++, p++ contact doping
- metal interconnect
- vias
- contact metal

Device Structure

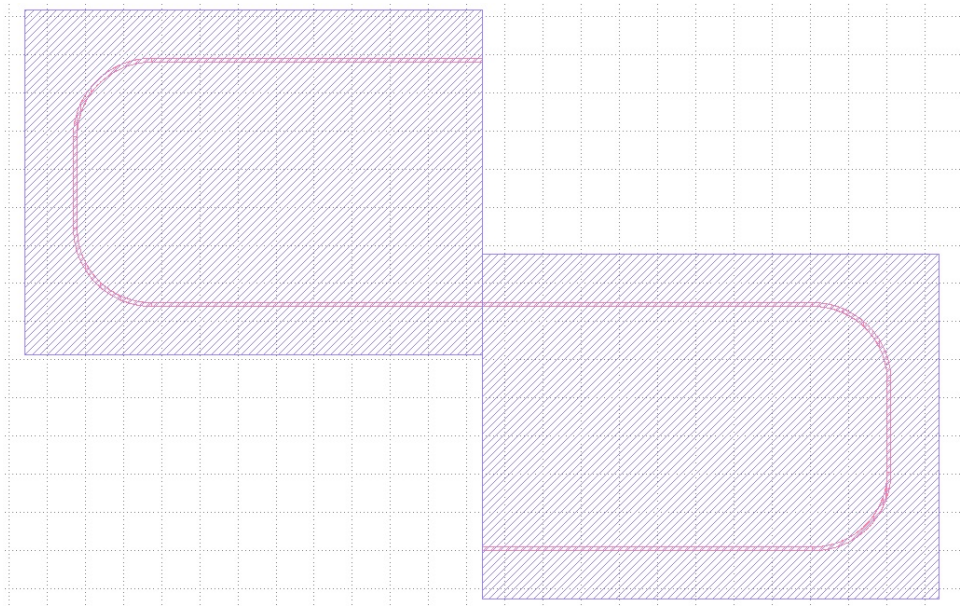
To achieve velocity matching, the footprint of this device consists of features that delay the microwave velocity and optical signal velocity. Taking this into account, the optical path of this device is defined as illustrated in Figure 2.8 (a). The input optical signal goes through a 50-50 splitter and the split signals travel along a S-shaped symmetric paths and are merged at the output end with another 50-50 splitter; this path is defined by combining the horseshoe paired structures into an array. In the design iterations, the input and output ends of the modulators are identical; the variation of this modulator is determined by the number of horseshoe pairs chosen and their physical length. The S-shaped horseshoe pair is a nested PCell. It is the core of the design and defines the overall geometry of the modulator. The parameters that dictate the length of optical path of the modulator are lx, ly, and r as illustrated in Figure 2.8 (b).



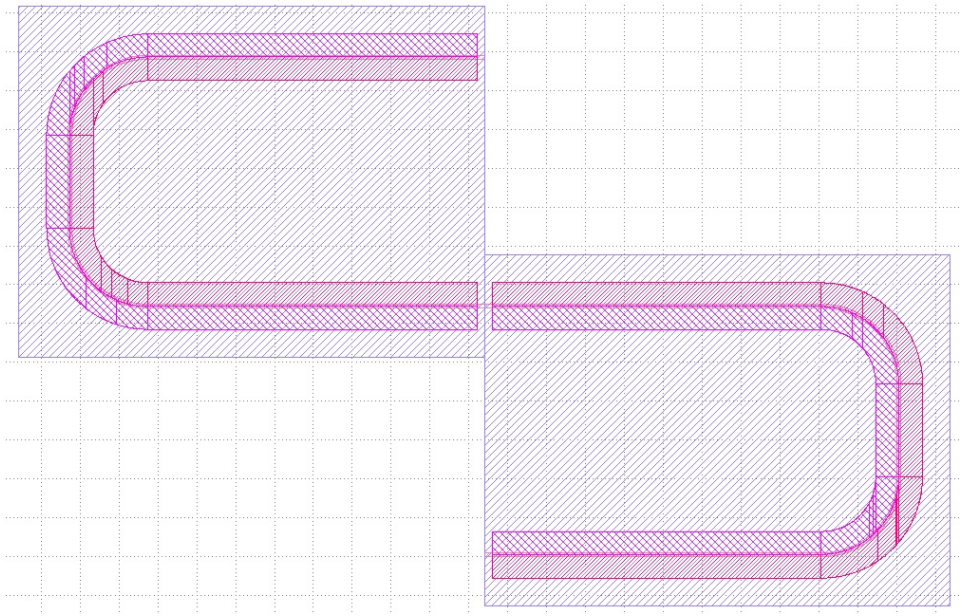
(a) (b)

Figure 2.8: (a) Modulator Waveguide Path (b) Horseshoe PCell Waveguide Parameters

The bend radius used in the horseshoe PCell design is 10 μm because the horseshoe pair is a ridge waveguide and larger bend radius is required to minimize optical loss (see Figure 2.9 (a)). In the PCell, the shallow etch of the ridge waveguide is internally parameterized to match the parameter variations of *lx*, *ly*, and *d*. The PN-junction is formed by applying N and P doping layer to the PCell. The two doping layers meet at the center of the waveguide with a slight offset to include a wider P region so the modulator can operate in a P doping favored environment [8](see Figure 2.10). The N and P doping layers have an S-shape geometry that closely match the waveguide (see Figure 2.9 (b)). With N and P layer applied, the added parameters that define the layers are *nw* and *pw*, which define N doping width and P doping width, respectively.



(a)



(b)

Figure 2.9: (a) Horseshoe PCell Ridge Layer Addition. (b) Modulator PN doping Layer Geometry.

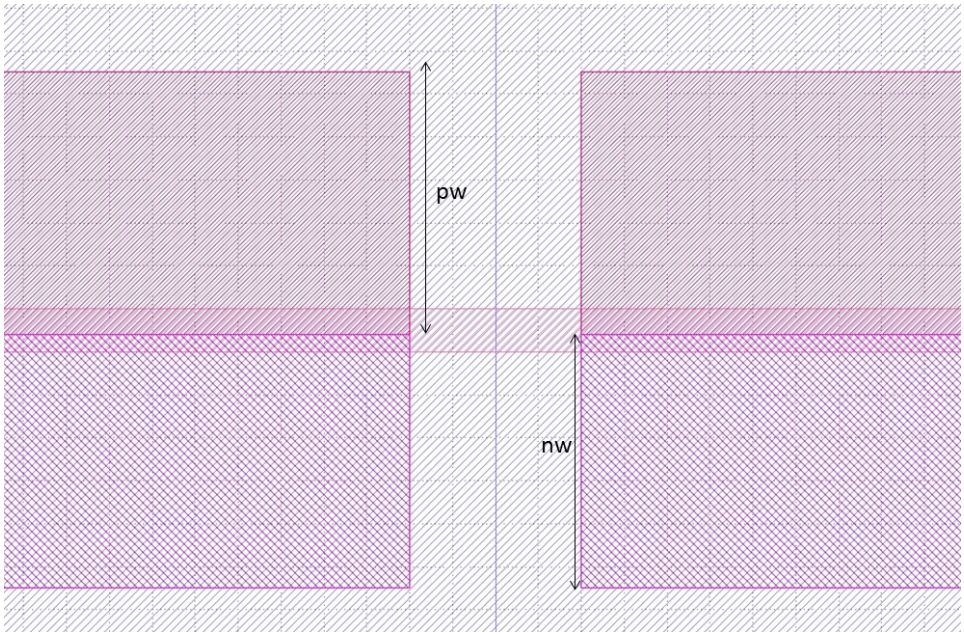
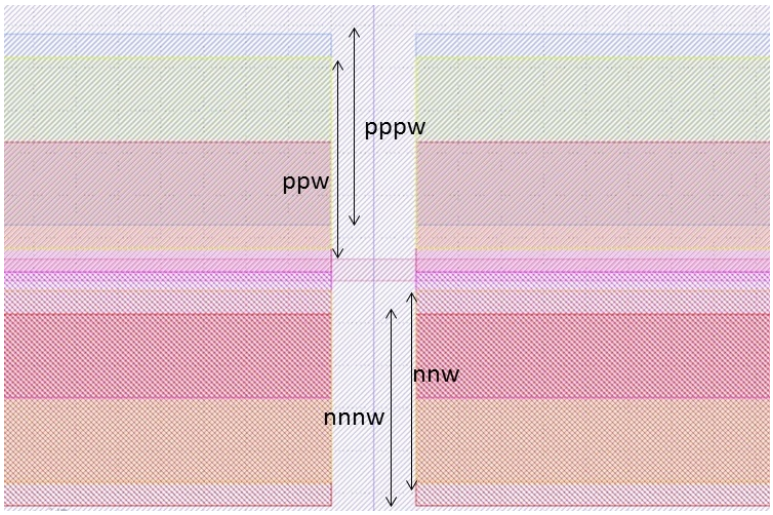
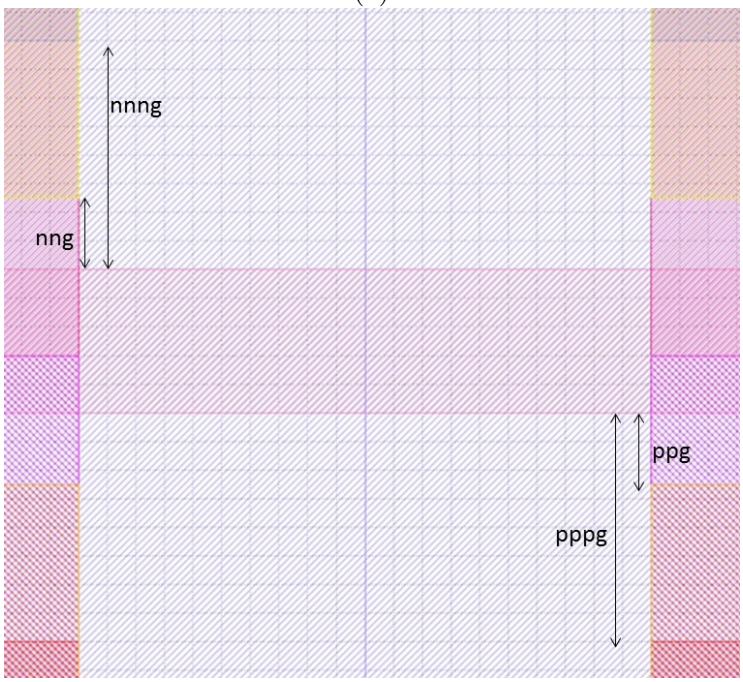


Figure 2.10: PN Junction Offset

The N+ and P+ doping layers are the transition layers that provides a more gradual change in the doping concentration profile. The N+ and P+ doping layers closely follow the snaking waveguide path. However, unlike N and P layers, the N+ and P+ layers have a gap between the waveguide and doping layer edge. As a result, the parameters introduced by the inclusion of N+ and P+ layers are *nnw*, *ppw*, *nng*, and *ppg* which corresponds to N+ layer width, P+ layer width, N+ layer gap, and P+ layer gap, respectively (see Figure 2.10 (a) and (b)). The layers with heaviest doping involved in the modulator design are the N++ and P++ doping layer. They are scripted in the similar fashion as N+ and P+ layers and the corresponding parameters introduced to the PCell are *nnnw*, *pppw*, *nnng*, and *pppg* which corresponds to N++ layer width, P++ layer width, N++ layer gap, and P++ layer gap respectively (see Figure 2.11 (a) and (b)). Figure 2.12 shows a horseshoe-structure with applied ridge etch layer and the doping layers.



(a)



(b)

Figure 2.11: (a) Doping Layer Width Definitions. (b) Doping Layer Gap Definitions.

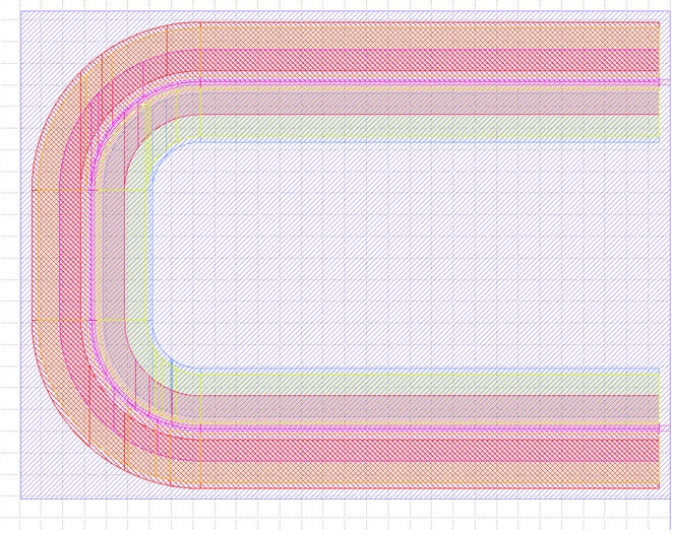


Figure 2.12: Horseshoe Geometry with Ridge and Doping Layers

To bias the PN junction, metal pads that receive electric signals from contacting probes are required to be connected to the P++ and N++ doping layers; hence, the fabrication process includes metal interconnect layers, Via1, Metal1, Via2, and Metal2. Via1 layer is an interconnect metal layer that links the heavy doping layers to the Metal1 layer. Typically, in other active photonic designs, Via1 structure footprint is minimized. But in our case, we require Via1 to be of a larger scale to uniformly distribute the electrons at the metal junctions. As a result, in order to meet the fabrication rule where Via1 is required to be enclosed by the heavily doped layer by a minimum spacing and the design considerations mentioned previously, the parameters that define Via1 structure in the PCell are chosen to be *v1g1*, *v1w*, and *v1L*. These parameters define the distance between the inner wall of Via1 to waveguide edge, Via1 width, and the gap to the edge of the heavy doping layer respectively (see Figure 2.13). Based on these parameters, the physical shape of Via1 forms two horseshoe shaped metal walls on either side of the center waveguide. The reason for the parameter choice is that we want to make sure the degree of freedom of the physical shape of the metal layers so the PCell is capable of generating wide variations of GDS drafts for re-simulation purposes.

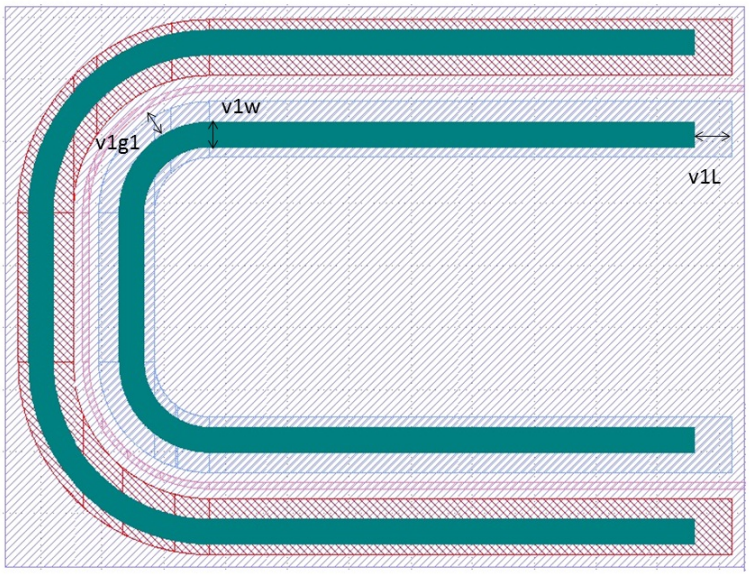


Figure 2.13: Via1 Layer (in dark green) Geometry

The next metal interconnect layers are Metal1 and Via2. To internally connect the Via1 and Via2 layers, Metal1 encloses both Via layers. Metal1 layer extends out on the outer rim of the waveguide and fills the center cavity of the inner side of the horseshoe structure (see Figure 2.14). The layers shown in Figure 2.14 are the waveguide layer, Via1 (solid dark green), Metal1 (shaded blue), and Via2 (solid red). The parameter introduced from the addition of the Metal1 layer is *m1g*. This parameter represents the distance between the waveguide edge to the Metal1 edge. The physical shape of Metal1 shown in figure is the configuration chosen for the final GDS mask. Other configurations have been considered and rejected based on their corresponding simulation results or unfeasible physical footprint. Ideally, like Via1 layer design, we want to increase Via2 size. Thus, the Via2 is placed as a solid block in the center cavity. The Via2 on the outer rim of the horseshoe pair is separated so the current is distributed more evenly. The parameters that define the inner Via2 structure are *v2w* and *v2L*.

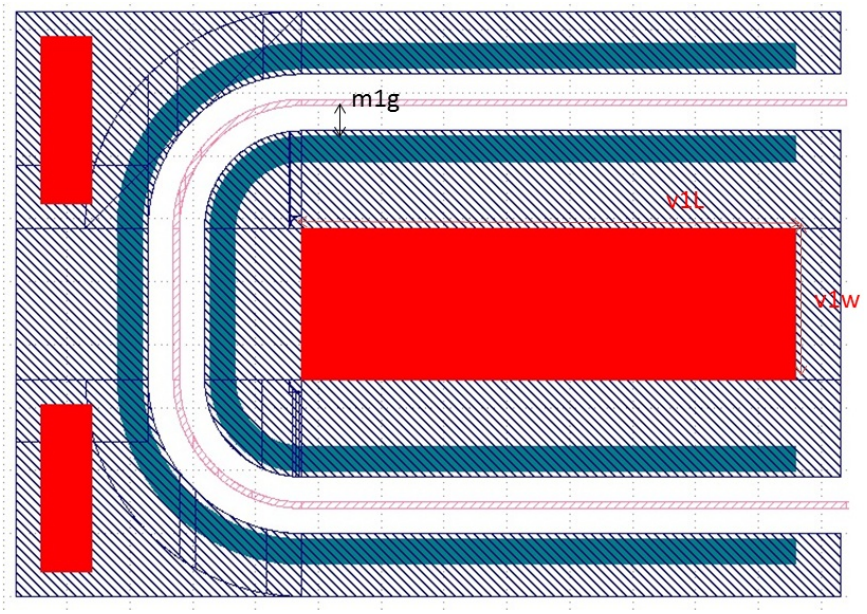
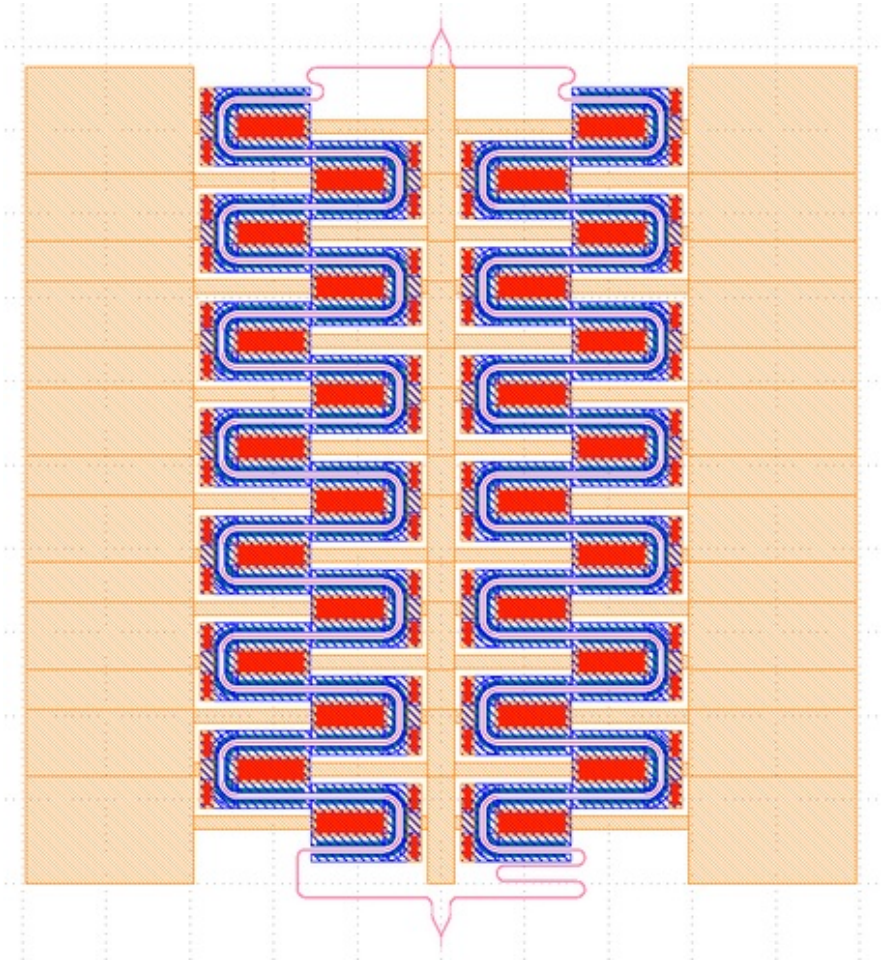


Figure 2.14: Modulator Metal Interconnect Layers

The Metal2 layer is the top metal layer that defines the fin electrodes which contribute to microwave velocity delay. Three electrodes are defined in this layer; these electrodes correspond to a proposed Signal-Ground-Signal (SGS) configuration. The length of the electrodes scales with the vertical array distance of the horseshoe arrays. The widths of the outer two electrodes and the center electrode are defined by the following parameters: *m2w1* and *m2w2*, respectively. The distance between the electrodes also plays an important role as indicated by the simulated results, and hence it is also parameterized; the corresponding parameter is *m2g*. Figure 2.15 (a) shows PCell array to illustrate the over all electrode design configuration and Figure 2.15 (b) shows the PCell that represents the horseshoe pair.



(a)

(b)

Figure 2.15: (a) Modulator Structure Overview. (b) Horseshoe Pairs PCell.

Description	Ratio	Number of Horseshoe Pairs	Modulated WG Length (mm)	Impedance Transformer (mm)	Probe Pads (mm)	Device Area (mm^2)
	4	32	8.192	0.6		1.703
	4	12	2.072	0.6		0.935
	4	7	1.792	0.6		0.743
With	3.5	36	8.064	0.6		1.856
Impedance	3.5	14	3.136	0.6		1.012
Transformer	3	42	8.064	0.6		2.087
	3	16	3.072	0.6		1.088
	2.5	50	8	0.6		2.384
	2.5	19	3.04	0.6		1.204
	4	32	8.192		0.2	1.463
	4	12	3.072		0.2	0.695
No	4	7	1.792		0.2	0.503
Impedance	2.5	50	8		0.2	2.154
Transformer	2.5	19	3.04		0.2	0.964
	2.5	11	1.76		0.2	0.656
Short	4	1	0.256		0.2	0.272
Device	2.5	1	0.16		0.2	0.272

Table 2.1: Device Summary

The PCell revealed in 2.15 (b) is intended to be directly used in simulation. Due to computing power issue, direct simulation on the PCell is not ideal because of the small mesh steps that are required to simulate round corners. Hence, the PCell corners are modified from 10 μm arcs into 90^o straight waveguide connections to match the mesh constraints. Based on the simulation results, we have decided to include 17 traveling wave modulator designs to the total assigned space of 22.0 mm^2(see Table 2.1). The short devices are included in the final mask so the response of the proposed horseshoe pair PN junction can be tested and used as a reference in the analysis of the complete traveling wave modulator structure. The ratios presented in Table 2.1 correspond to microwave and optical wave velocity matching. For example, in ratio 4 designs the optical wave is predicted to travel 4 times faster than the microwave through Sonnet simulations [5]; therefore, extra length is applied to the optical waveguide to achieve an in-phase modulation. Similar simulations are done for the other ratios; microwave speed is adjusted by changing the metal junction widths and lengths to modify the junction RC constants [5][6]. The values included in Table 2.2 are in μm; they represent the PCell parameters of the ratio 4 designs.

The last step of the modulator drawing procedure is the addition of contact pads. The pads and the attached impedance transformers are defined on the Metal2 layer (see Figure 2.16) [5]. Arranging the complete modulators onto the allocated mask space is not trivial. To minimize possible cross-talk between individual modulators, we align the modulators with a 200 μm horizontal and 100 μm vertical spacing. The empty spacings are filled with passive devices to maximize space efficiency. The traveling wave modulators use edge coupling. As a result, the input and output ends are required to be located on the left and right end of the chip. The routing method chosen for this mask is manual routing due to the irregular lengths of the devices and the edge coupling constraints. Keep-out layers are used to cover the core of the modulator design; we want to restrict the tiling of the Metal1 and Metal2 layers to be 50 μm away from the electrodes. Hence, in order to meet the final density requirement on the metal layers, the tile density from the tiling script is modified. Figure 2.16 shows an example of the final GDS of traveling wave modulators that contains 11 modulators; the rest of the modulators are merged with other layouts to space efficient purposes.

	Description	Ratio 4
lx	waveguide length	42.4
ly	waveguide width	12
d	distance between left and right PN junction	1
nw	N dope width	2.95
pw	P dope width	3.05
nnw	N+ width	4.5
ppw	P+ width	4.5
nng	distance of N+ to waveguide	0.25
ppg	distance of P+ to waveguide	0.25
nnnw	N++ width	4.5
pppw	P++ width	4.5
nnng	distance of N++ to waveguide	0.5
pppg	distance of P++ to waveguide	0.5
m1g	distance of Metal1 to waveguide	2
v2w	Via2 width	39.3
v2L	Via2 length	12
m2w1	Outer electrode width	100
m2w2	Center electrode width	16
m2g	Electrode Gap	140

Table 2.2: PCell Parameter Detail

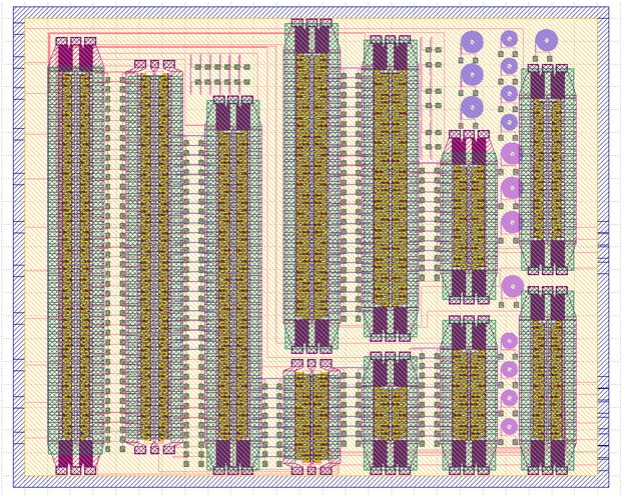


Figure 2.16: Traveling Wave Modulator Final GDS Layout

2.2.2 On-Chip Optical Circuit

On-chip optical circuit design is a project in collaboration with Optelian. The goal of this project is to demonstrate simple on-chip circuits consisting of a maximum of three optical components and provide Optelian with a final chip that uses edge coupling and simple probing device orientations (discussed in detail in a later section). This design example is included in this thesis to demonstrate the importance of device packing and routing. The components involved in the optical circuit design are a ring modulator, a photodetector, and three variations of variable optical attenuators (VOAs). The ring modulator and the photodetector are documented components from the OpSIS IME GDS library (see Figures 2.17 and 2.18) [21]. Both the ring modulator and the detector are modified slightly from GSG configuration to SG configuration (see layout section for detail). The photodetector and the ring modulator have been simulated and tested by OpSIS before they are included in the OpSIS library; hence the focus of our work is to design VOAs that act as a switch by attenuating the optical signal before it enters the photodetector. This design is fabricated on the same run as the traveling wave modulator discussed above (see Figure 2.6 for fabrication process illustration).

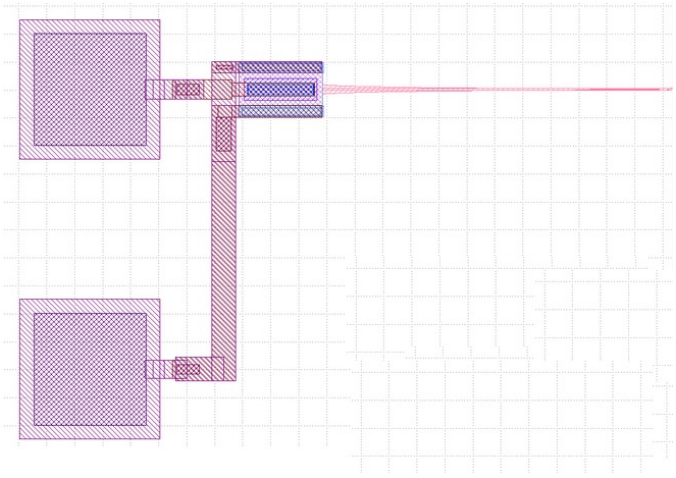


Figure 2.17: OpSIS IME Photodetector [21].

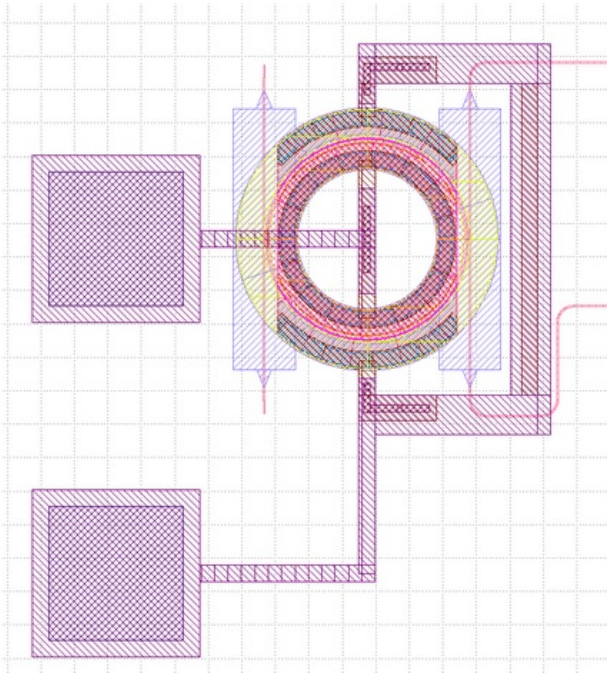


Figure 2.18: OpSIS IME Ring Modulator [21].

A total of three VOA designs are included in the on-chip optical circuit design. The first VOA has a similar MZI-like structure described above but implements a N++, I, P++ doping. Phase shift is achieved by applying an electric field to one of the branches [10,11,23]. The second VOA is a long single waveguide with N++, I, P++ doping. The optical signal is attenuated due to the optical loss increase from carrier injection when the PIN junction is forward biased [12,23]. The third VOA is a MZI-like structure that implements a N++, N, N++ junction to one of the branches [4]. The goal of this design is to achieve a π phase shift between the two waveguide branches by heating one of the branches to change its optical property.

MZI PIN VOA (Design 1)

To estimate the performance of the PIN junction VOAs, simulations carried out with Lumerical DEVICE and MODE Solution are compared to previous PIN structure measurement results [22][23]. The structure is a 500 nm wide, 500 μm long ridge waveguide. The heavily doped layers are 200 nm away from the waveguide edge. The simulation and measurement results

are compared in the following figures.

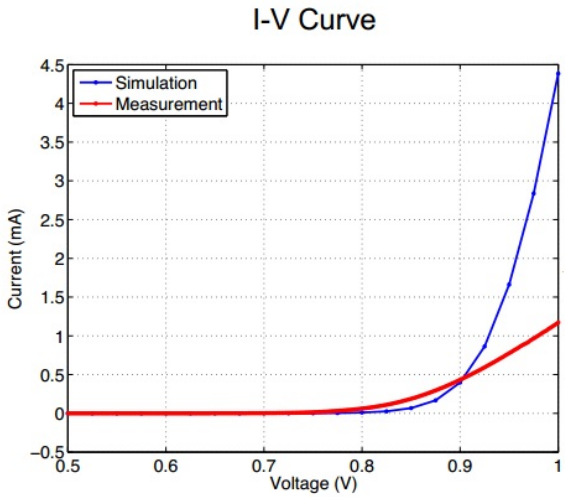


Figure 2.19: Current vs. Voltage [22]

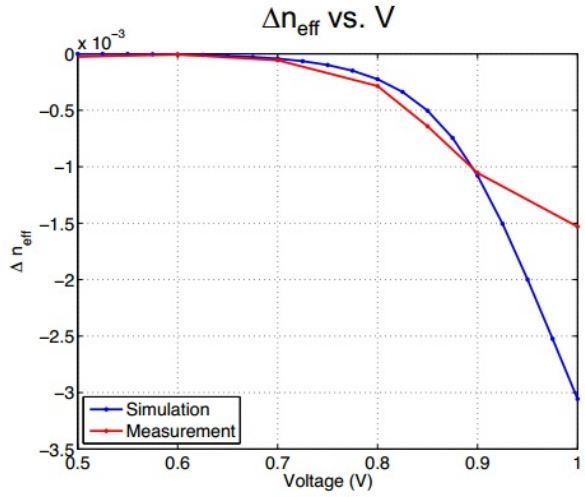


Figure 2.20: Effective Index vs. Voltage [22]

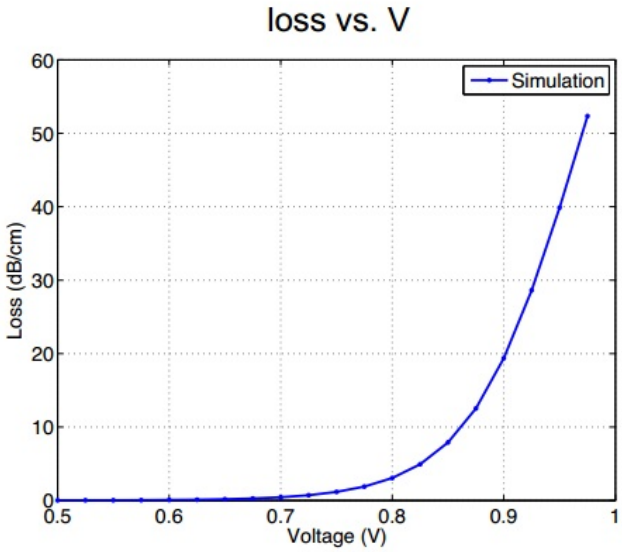


Figure 2.21: Loss vs. Voltage [22]

Using a lossless model that represents a simple MZI structure, the transfer function, $\frac{I_i}{I_o}$, and β are [23][24]:

$$\frac{I_i}{I_o} = \frac{1}{2}[1 + \cos(\beta_1 L_1 - \beta_2 L_2)] \tag{2.1}$$

$$\beta = \frac{2\pi n_{eff}}{\lambda} \tag{2.2}$$

Since the PIN VOA design has a symmetric structure, the condition required to satisfy a π phase shift is defined as:

$$\Delta n_{eff} = \frac{\lambda}{2L} \tag{2.3}$$

As a result, the Δn_{eff} required for a π phase shift of a 3 mm long MZI at wavelength 1550 nm is 2.58×10^{-4}. The VOA designs implement the PIN junction with an 800 nm doping-layer-to-waveguide gap rather than the 200 nm gap design of the old PIN structures; the doping layer gaps are increased to minimize loss due to doping [4]. Due to the changed PIN junction characteristic, the effect of voltage on Δn_{eff} is estimated to be 25% or less of the data illustrated in Figure 2.20. To compensate for the PIN junction variation, the length of the MZI VOA design is set to 3 mm. The

estimated voltage to achieve the required π phase shift for the 3 mm MZI VOA is 0.8V.

Long PIN VOA (Design 2)

The long PIN VOA is a single waveguide structure with a PIN junction that has an 800 nm doping-layer-to-waveguide gap. As a result, the loss, as illustrated in Figure 2.21, is expected to increase more gradually; the extinction ratio for a long PIN VOA with 1 cm length is approximated to be 15 dBm with a 1V applied voltage.

Temperature Tuning VOA (Design 3)

To estimate the efficiency of the temperature tuning VOA, we started out by predicting the resistance of the VOA structure (see Figure 2.22). The L_1, L_2, and L_3 values are 500 nm, 800 nm, and 7.9 μm, respectively.

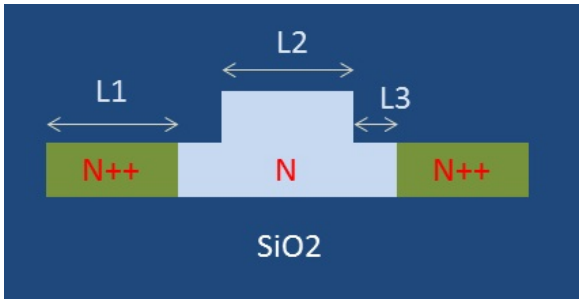


Figure 2.22: Temperature VOA Structure

The measured sheet resistance, ρ, values used for thick silicon, thin silicon, and N++ doped thin silicon are extracted from [4]. A total resistance of the MZI branch is 4.268 Ω. It is calculated using the following equation where L_{wg} is the waveguide length:

$$R = \frac{\rho_1 L_1}{L_{wg}} + 2\frac{\rho_2 L_2}{L_{wg}} + 2\frac{\rho_3 L_3}{L_{wg}} \tag{2.4}$$

Using a constant that represent the ^{o}C change per mW of 1 mm long waveguide, $T_c = 1.623 \times 10^{-4} \frac{^oCm}{mW}$ [7], we can deduce the temperature change due to the input current with the following formula (see Figure 2.23).

$$Temperature = T_c \times \frac{I^2 R}{L} \tag{2.5}$$

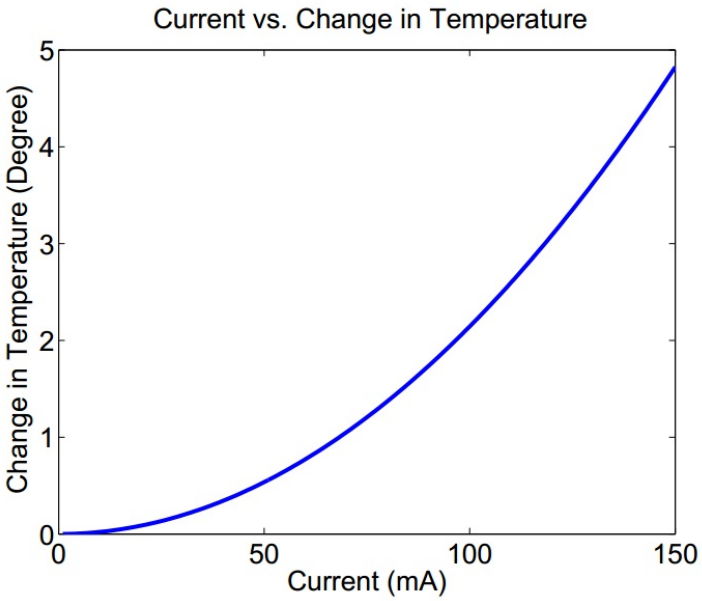


Figure 2.23: Current vs. Change in Temperature

Using MODE Solution, the effective index n_{eff} is extracted and curve fitted in Matlab (see Figure 2.24). Equation 2.1 is modified to include the effect of the change in temperature; β and the corresponding MZI transfer function are defined as the following [24]:

$$\beta = \frac{2\pi(n_{eff} + \frac{dn}{dT}\Delta T)}{\lambda} \tag{2.6}$$

$$\frac{I_i}{I_o} = \frac{1}{2}[1 + \cos(\beta_1 L - \frac{2\pi(n_{eff} + \frac{dn}{dT}\Delta T)}{\lambda} L)] \tag{2.7}$$

Using thermo-optical coefficient, $\frac{dn}{dT} = 1.86 \times 10^{-4} K^{-1}$ [24], we can plot the transfer function of the VOA versus the change in temperature and the transfer function versus input current (see Figures 2.25 and 2.26). The results suggest that to reach the first VOA turn off point, the temperature change required is 1.75 ^{o}C and the current required to reach that temperature is 80 mA.

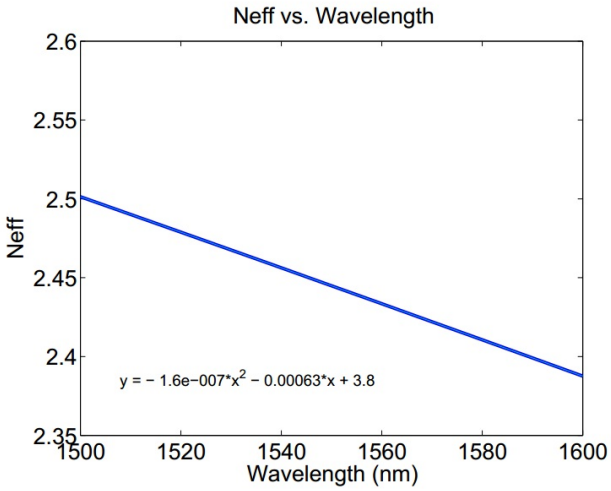


Figure 2.24: Effective Index vs. Wavelength

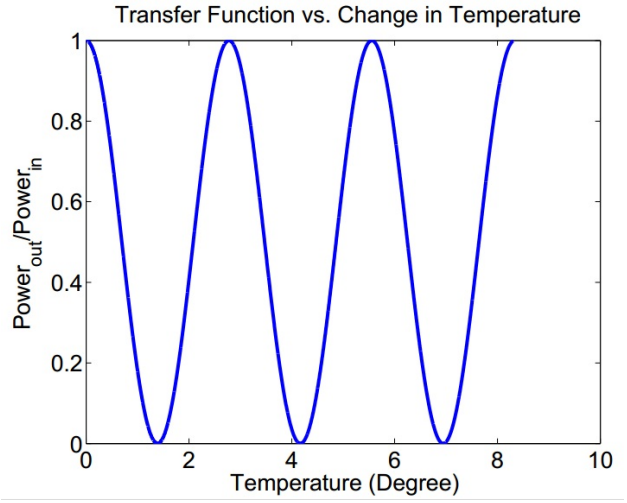


Figure 2.25: Transfer Function vs. Change in Temperature

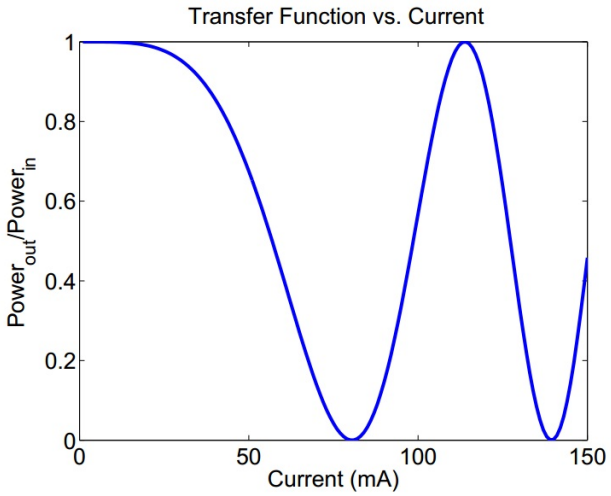


Figure 2.26: Transfer Function vs. Current

The performance prediction of the VOAs introduced above is summarized in Table 2.3. An insertion loss of 1.3 *dBm* is used to account for y-branch loss in the VOA performance calculations [18]:

	Design 1	Design 2	Design 3
Description	PIN VOA	Long PIN VOA	Heat Tuning VOA
Structure	MZI	Straight Waveguide	MZI
Junction Implemented	P++, I, N++	P++, I, N++	N++, N, N++
Extinction Ratio Predicted	12.9 *dBm*	15 *dBm*	Infinite
Wavelength Dependence	Independent	Independent	Independent
Insertion Loss	3.2 dB	4 dB	7 dB
Switch Current (off to on)	0.1mA	1.3mA	80 mA
Switch Voltage (off to on)	800 mV	1000 mV	320 mV
Switch Power (off to on)	0.080 mW	1.3 mW	25.6 mW
Device Length	3 mm	10 mm	3 mm

Table 2.3: VOA Performance Summary

VOA PCells

To build a PCell for these VOAs, we start by mapping out the Si layers first before the doping layers, the Via layers and the metal layers are applied. The MZI-like VOAs use a 50-50 splitter library component to direct the input optical into two branches and another 50-50 splitter to combine the optical signals before the output grating coupler. Both the strip and ridge waveguide are implemented in the VOA designs; the PCell of the transition taper described in section 2.1.2 is used at the waveguide junctions. The parameters that are responsible for the physical shape of this PCell are n and L, which correspond to the number of bends and length of the branch, respectively (See Figure 2.27(a)). The similar concept is used to design the third VOA (see Figure 2.27 (b)).

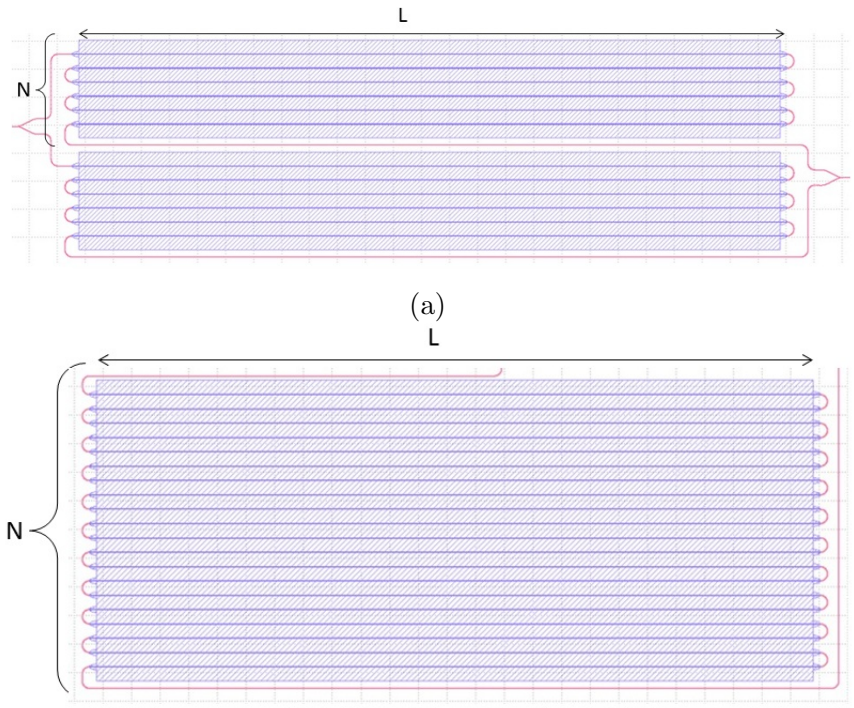
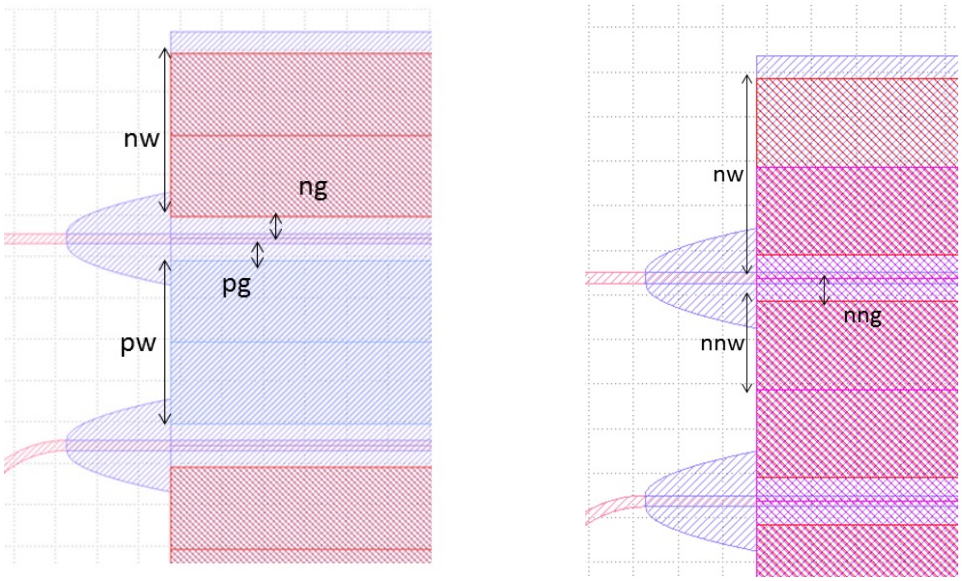


Figure 2.27: (a) MZI-Like VOA Waveguide Structure. (b) Single Waveguide VOA Structure

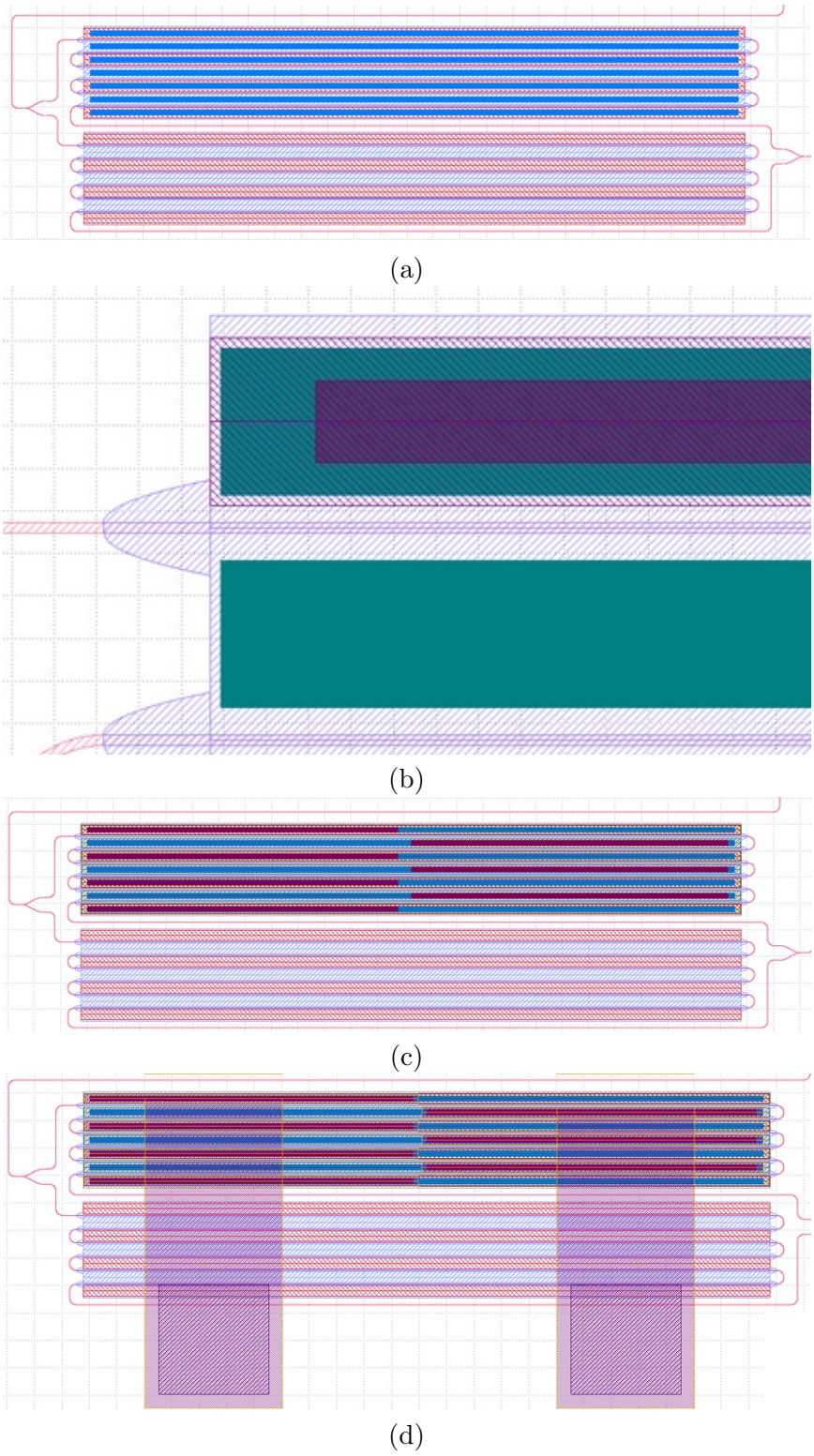
The doping layers are defined and parameterized in the fashion as illustrated in section 2.2.1. The PCell parameters and the corresponding junctions are illustrated in Figure 2.28.



(a) (b)

Figure 2.28: (a) PIN Junction Definition. (b) NnN Junction Definition.

The purpose of the metal interconnect layers is to provide a linkage between the metal pads and the heavily doped layers. The footprint of the interconnect layers is determined by the length and width of the heavily doped layers. Via1 and Metal1 layers are fitted onto the doping layers with the minimum gap requirement to the doping layer edges to avoid drawing violations. Via2 and Metal2 layers have the connection described above. The Via2 and Metal2 layers have a zig-zag configuration so the N++ doping layers are connected only on the left side and the P++ layers are connected only on the right side (see Figure 2.29). The N++, N, N++ junction is connected in the same style.



(a)

(b)

(c)

(d)

Figure 2.29: (a) Via1 Layer (blue). (b) Metal1 Layer (green). (c) Via2 Layer (red). (d) The complete MZI-like PIN VOA Design.

On-Chip Optical Circuit Layout

Understanding the performance of each component is critical to understanding the proposed on-chip optical link structure. Hence, besides the three-component optical link structure that consists of ring modulator, a type of VOA, and photodetector, single components and two-component links are placed onto the final mask as well. Unlike single-component designs such as the traveling wave modulator describe above, the footprint of each type of links or single components introduced in the optical circuit varies more vigorously. As a result, placing the components onto the final layer while attempting to minimize empty spacing and making experimental measurements trivial is a challenging task. The constrains considered are:

- Require both edge coupling and grating coupler.
- Only top and right edge are available for edge coupling.
- Three component links require VOA probes, modulator-detector probe, and input/output optic signal coupling.
- Minimize empty spacing.

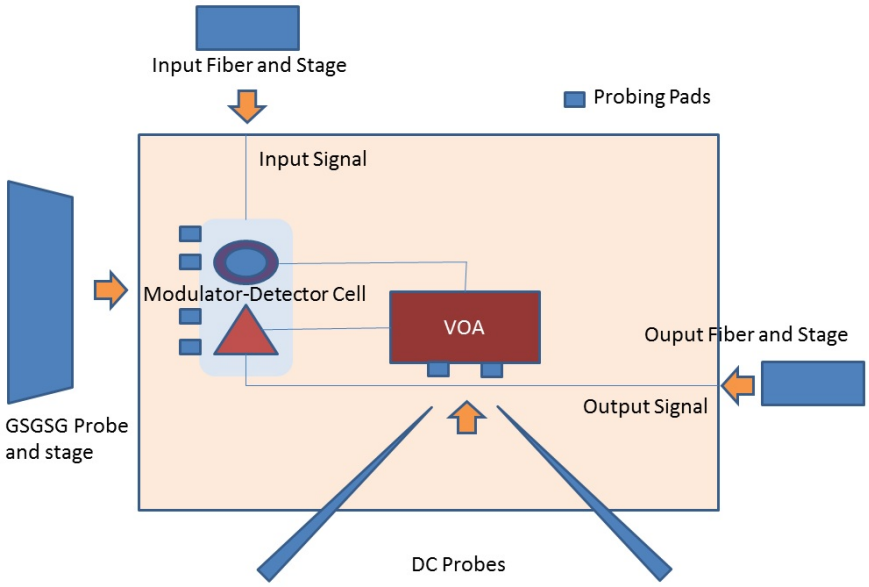


Figure 2.30: Edge Coupling Testing Orientation.

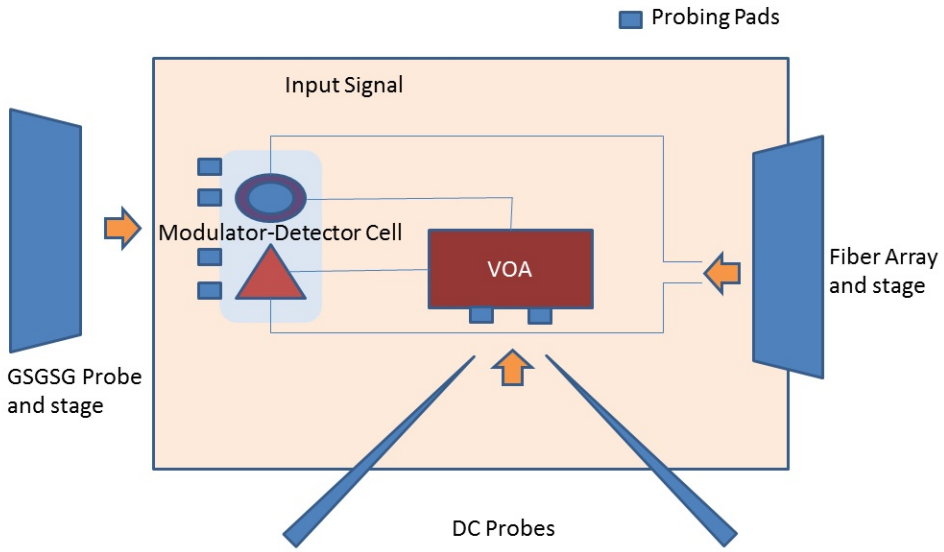


Figure 2.31: Fiber Array Testing Orientation.

The photodetector and ring modulator probing pads are reduced. The change from GSG probing to SG probing is established by connecting the interconnect metal layer (Metal1) that links to the ground pads together. By doing so, the electric signal that drives the ring modulator and electrical signal detection required for the photodetector can be from a customized GSGSG probe that is capable of providing separated signals. By combining the ring modulator and the photodetector in this fashion, the testing of the linked component is possible. The concept orientation for device measuring is illustrated in Figures 2.30 and 2.31.

Considering the constraints and the irregular link component pattern, the final GDS mask is chosen to be laid out manually. As a result, the routing required for the input and output waveguides for both edge coupling and grating coupling are performed manually as well. To pack and route the on-chip circuit design, all the combinations of the links and single components are generated via calling PCell or GDS. To effectively pack these components to minimize the waste of space, the components are manually placed onto the allocated space one by one as compactly as possible while allowing versatile waveguide routing. The links between the components and the input and output couplers are established via manually connecting the input and output ports of the components together using the quarter-arc

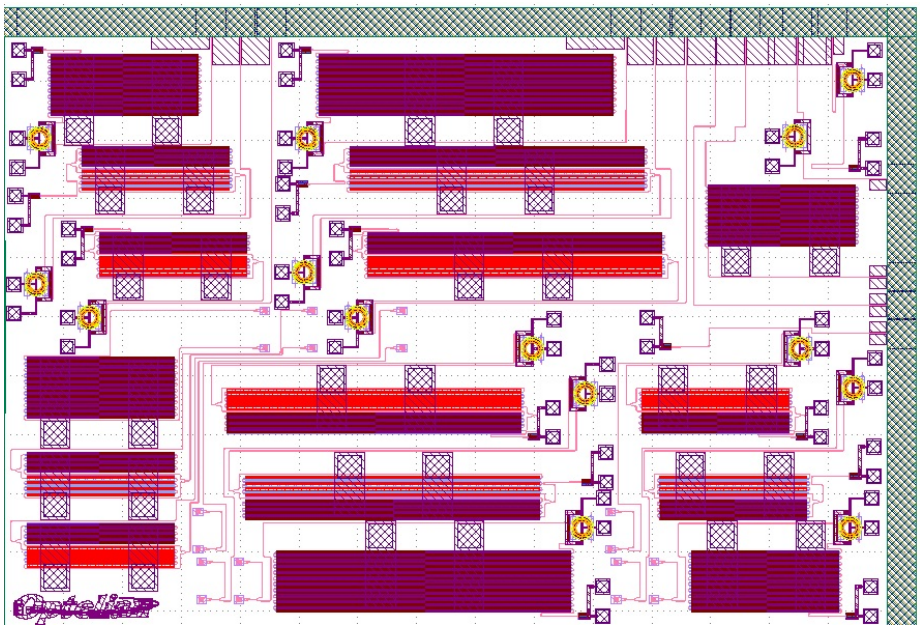
PCell as the 5 μm radius waveguide bends. Due to limited allocated space, the final GDS does not fit all the combinations of the links. Hence, the spaces allocated for this design are prioritized as the following (see Figure 2.32 (a) for the final GDS mask and (b) for a 3-component link example):

1. 3-component links with edge coupling (top left corner)
2. 3-component links with grating coupling (bottom right corner)
3. 2-component links with both type of coupling (bottom left corner)
4. Single Components (packed in left over spacing)

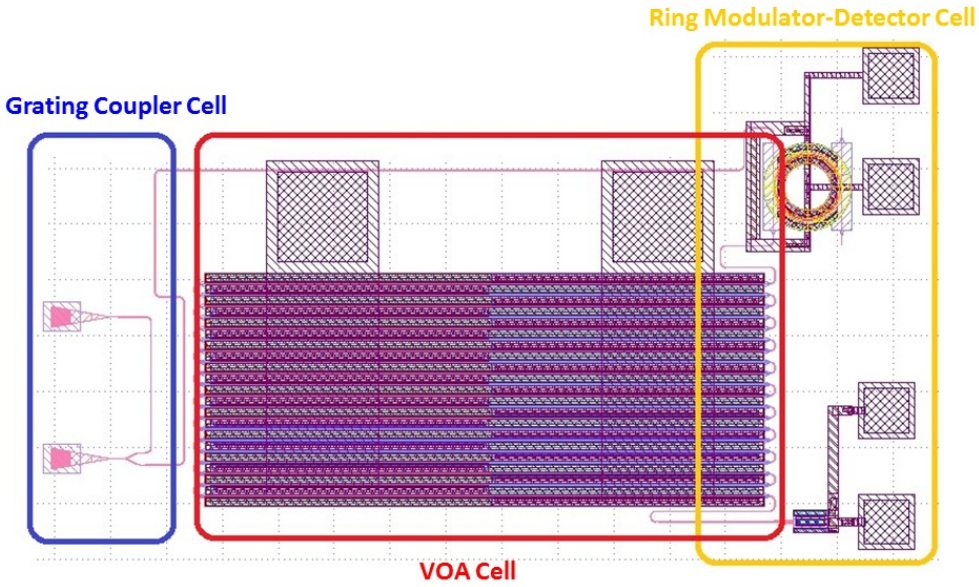
A summary of the components of the on-chip optical circuit are documented in Table 2.4.

Description	Ring Modulator	VOA Type	VOA Length (mm)	Detector	Coupling Method
3-Component Link	Yes	1	10	Yes	Edge
	Yes	2	3	Yes	Edge
	Yes	3	3	Yes	Edge
	Yes	1	20	Yes	Edge
	Yes	2	6	Yes	Edge
	Yes	3	6	Yes	Edge
	Yes	1	10	Yes	Grating
	Yes	2	3	Yes	Grating
	Yes	3	3	Yes	Grating
	Yes	1	20	Yes	Grating
	Yes	2	6	Yes	Grating
	Yes	3	6	Yes	Grating
2-Component Link	Yes			Yes	Edge
Single Component	Yes				Edge
				Yes	Edge
		1	10		Edge
		1	10		Grating
		2	3		Grating
		3	3		Grating

Table 2.4: On-Chip Optical Circuit Device Summary



(a)



(b)

Figure 2.32: (a) On-Chip Optical Circuit Final GDS Layout. (b) 3-Component Link (located at bottom right corner of the final mask)

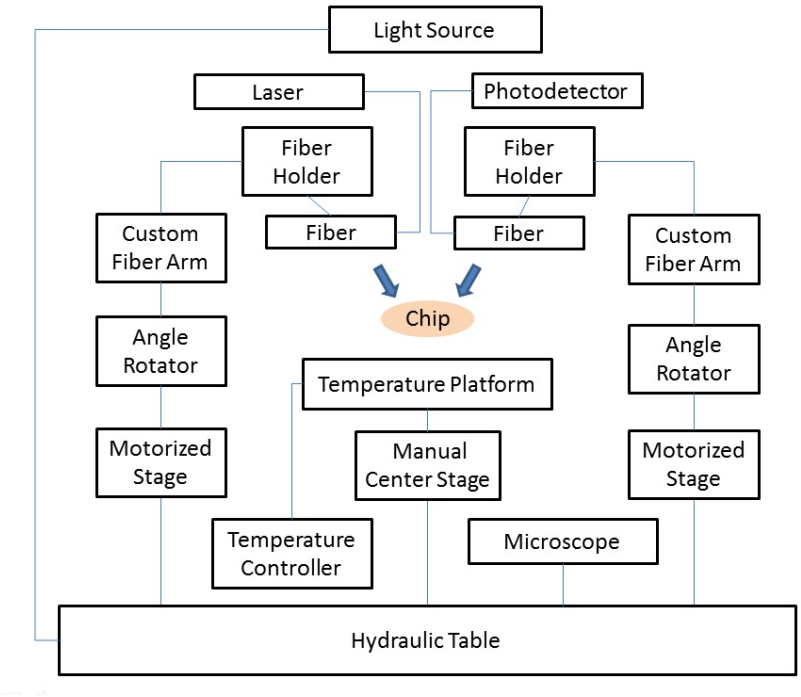
Chapter 3

Measurement Setup: Fiber-to-Fiber Automated Measurement Station

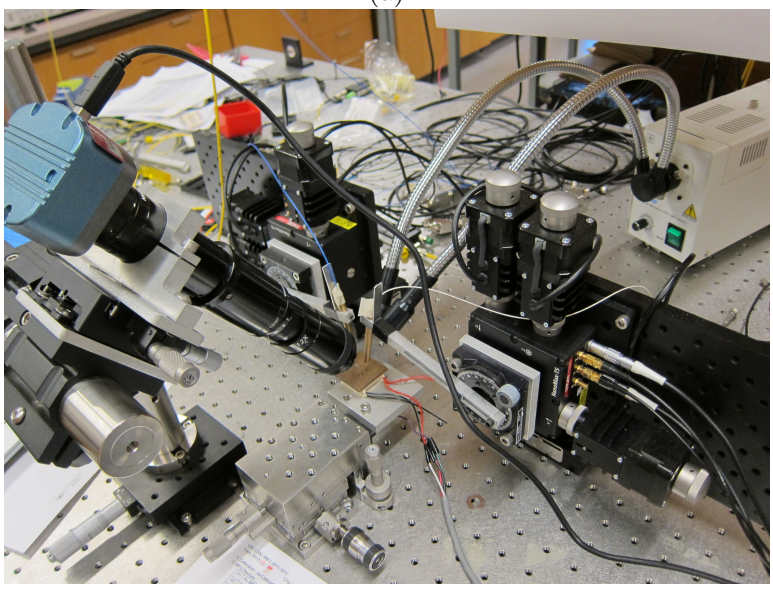
The fiber-to-fiber automated measurement station is an improved version of our previous manual measurement stations. In the outdated manual setup, it is difficult to align to the optimal fiber position because the manual actuators are not as stable compared to the newly implemented motorized actuators. The manual actuators have a tendency to backlash upon the release of the actuator handle; the coupling power drops several *dBm* because of this. Therefore, we propose the fiber-to-fiber automated measurement station to improve our photonic device measurement results.

3.1 Station Overview

The chip is placed on top of the temperature-controlled platform which is on top of the center manual stage. The center stage elevates the chip to the desired height in relation to the fiber stages. To the left and right of the center stage, the coupling fibers are held in fiber-mounts which are mounted to angle rotators. The angle rotators are fixed to motorized stages. The right motorized stage is mounted to a 1-axis travel stage so the distance between the input and output fibers can be adjusted to fit various input and output coupler distances. The microscope is mounted to the edge of the table and is at the bottom-side of the central stage; the light source is located at the opposite side and is relative to the microscope to provide clear images. Figure 3.1 shows the block diagram setup and a photograph of the system.



(a)



(b)

Figure 3.1: (a) Fiber-to-Fiber Setup Block Diagram Illustration. (b) Fiber-to-Fiber Setup.

3.1.1 Station Specifications

To improve the automated fiber-to-fiber setup performance, the following criteria are required:

1. Stage Automation
    - To achieve automation, stages are required to be controlled through Matlab. The stages used are from Thorlabs. These stages are responsible for automatic fiber positioning. The internal piezoelectric actuators are used for fine alignment once the fibers are in the proximity of the grating couplers [15].
2. Temperature Control
    - The temperature controller is used to tune or maintain the temperature of heat-sensitive devices during a measurement. The temperature is observed to fluctuate within a range of $\pm 0.005^{\circ}C$ [16].
3. Laser Source and Photodetector
    - The laser source used for our measurement is the HP8164A [17]. The typical range of the wavelength sweep performed is from 1460 *nm* to 1580 *nm*. A photodetector is also implemented on this module.
4. Fiber-to-Fiber Distance Adjustment
    - A manual stage is used for coarse fiber-to-fiber distance variation. With the addition of this 1-axis 10 *cm* travel manual stage, the fiber-to-fiber automated setup can be adjusted to fit various input-to-output coupler distances.
5. Fiber-to-Coupler Angle Adjustment
    - To optimize the incident angle between the coupling fibers and the grouting coupler, an angle rotator is implemented. The affect of fiber-to-grating coupler angle on the response is discussed in detail in section 3.3.1.

6. Fiber Arm and Holder

    - The input and output fibers are held in a coupler holder (see Figure 3.2). This holder is connected to a custom-designed aluminum arm and is connected to the angle rotator to make fiber angle adjustments possible.

7. Laser Coupling

    - We choose cleaved fiber over lensed fiber to couple the laser into the grating coupler because stripped fiber can be re-stripped and re-cleaved when damaged. As a result, the insertion loss is around -18 dB (about 6 dB less than lensed fiber). The input fiber is a polarization maintaining single mode fiber. The output fiber is a multi-mode fiber; we choose to use multi-mode fiber because it captures all the modes at the output end and thus, have better coupling power.

8. Microscope and Light Source

    - The clear chip-fiber view is achieved by setting up the microscope and its corresponding light source at an angle to the center stage (see Figure 3.3). This makes device alignment trivial.

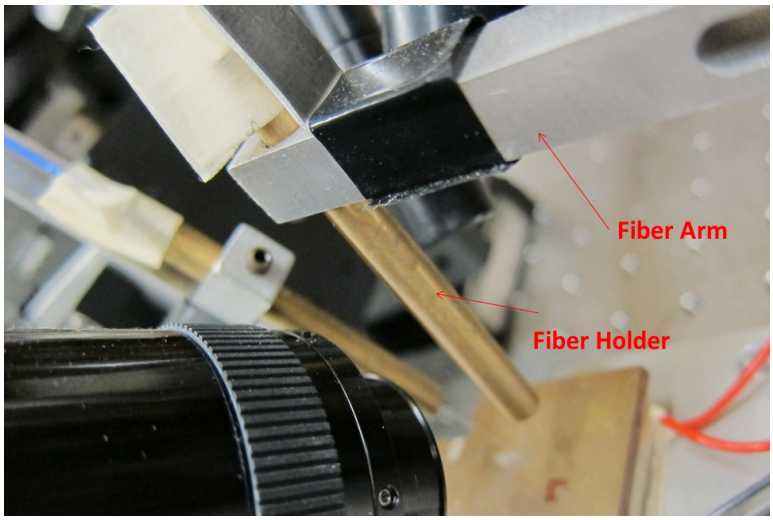


Figure 3.2: Fiber Holder and Fiber Arm.

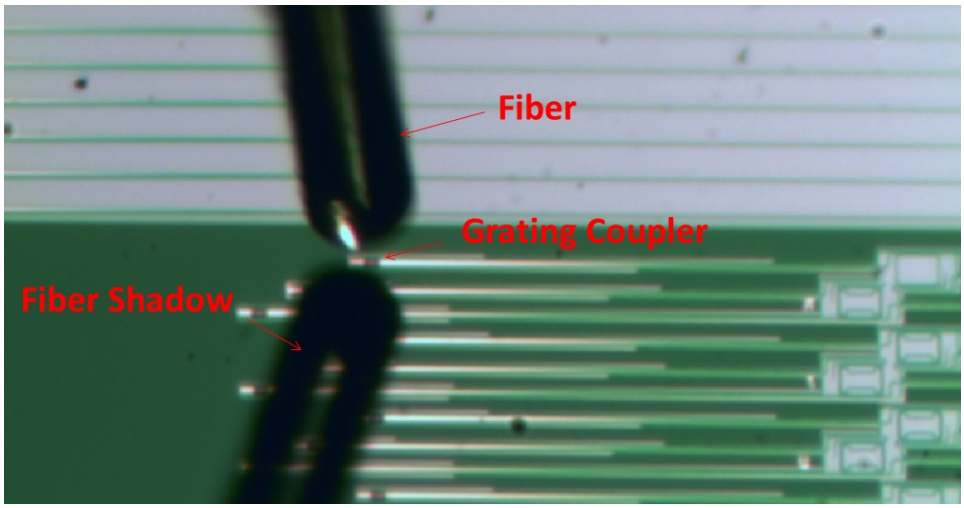


Figure 3.3: Fiber-Chip Microscope Image

3.2 GUI Software

The fiber-to-fiber automated setup supports both semi-manual and fully-automated measurements. Manual device characterization is used for undesired input and output grating coupler configuration. The automated device measurements are suitable for coupler configurations that are within the movement limitations of the motorized actuators. To allow automated measurements, the ActiveX drivers that correspond to motorized actuators and the piezoelectric actuators are merged into a single master graphic user interface (GUI) in Matlab. By doing so, the movements of the motors and the auto-alignment feature of the piezoelectric actuators can be accessed through Matlab. The signal from the output fiber is split by a 50-50 splitter. One of the split signals is sent to the laser photodetector, and the other is used for piezoelectric fine alignment. The flowcharts illustrated in Figure 3.4 (a) and (b) show the typical measurement flow for manual and automated device characterization respectively.

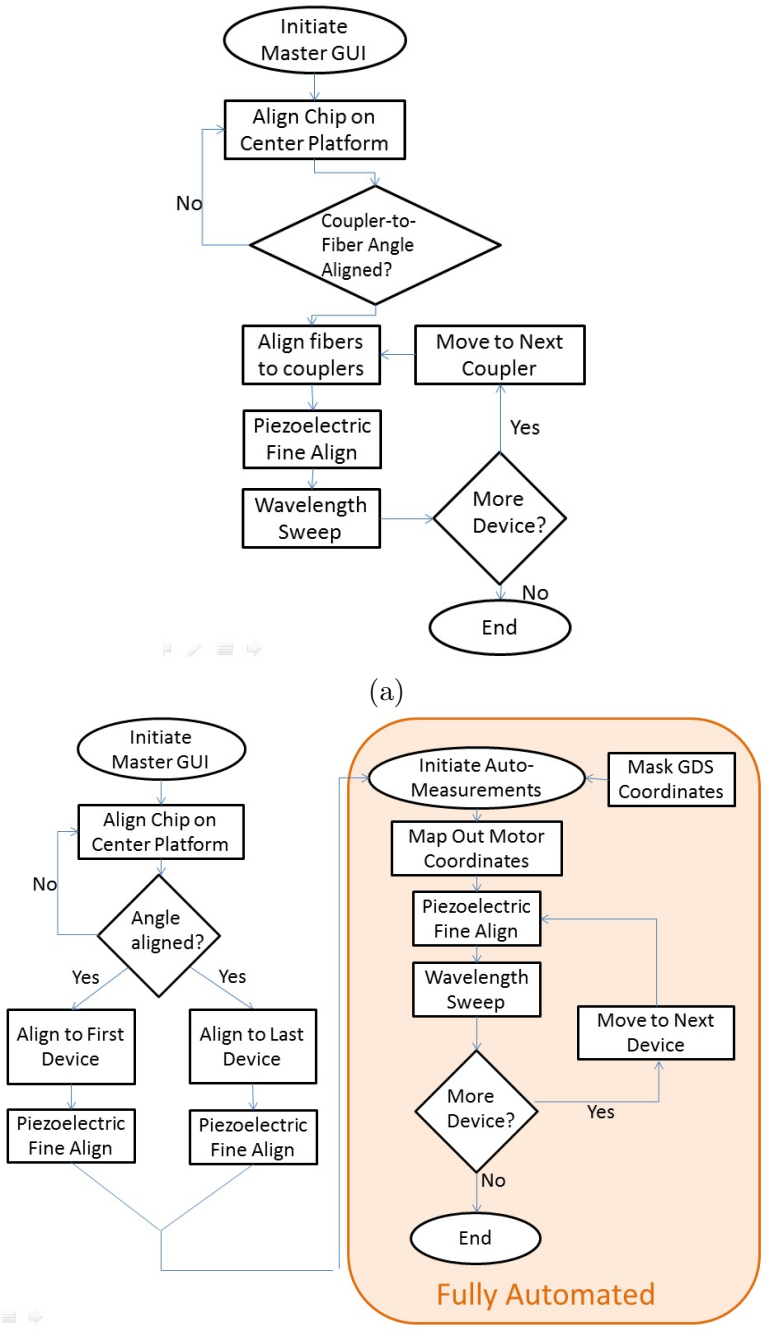


Figure 3.4: (a) Manual Device Measurement Flowchart. (b) Automated Device Measurement Flowchart.

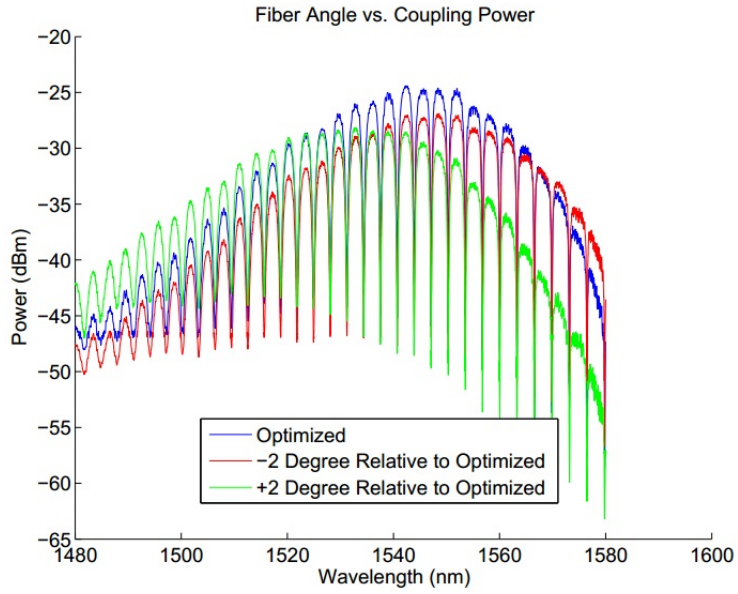
The multi-measurement algorithm requires a GDS mask coordinate Excel file and the first and last device motor coordinates of the input and output fiber. The Excel file contains the coordinates of input and output grating couplers which describe the relative distances between the couplers. After aligning the fibers to the first and last device and record the motor coordinates, the Excel file GDS coordinates are read and converted into matrix form. The first and last device coordinates from the Excel file are matched with the first and last device motor coordinates. Using these points, relative chip rotation angles to the input and output fibers are calculated along with magnitude scaling constants. Using the calculated parameters, the rest of the device GDS coordinates are converted to motor coordinates and thus the travel path of the input and output fiber is mapped out. The fibers move along the matrix coordinates one by one; a wavelength sweep is performed at each of the aligned grating coupler after piezoelectric actuators locate the optimal coupling input and output fiber positions.

3.3 Automated Setup Tests and Measurement Results

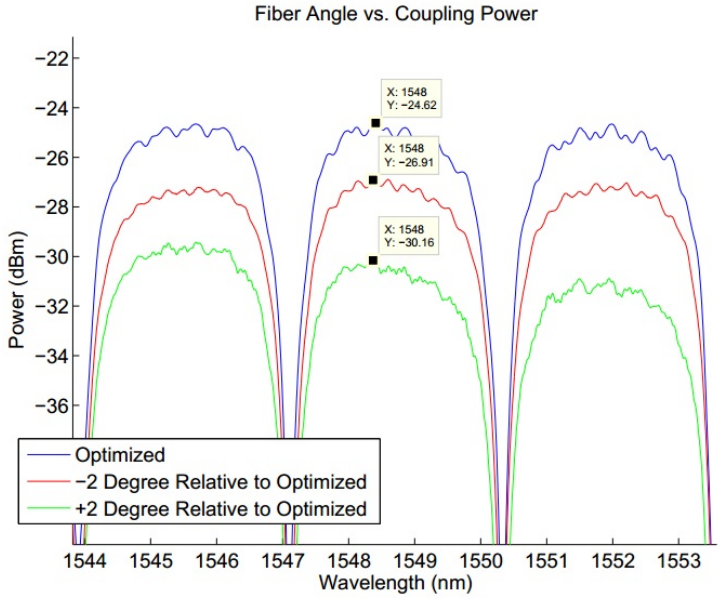
Tests have been conducted to illustrate the stability of the fiber-to-fiber setup. These tests include: fiber angles vs. measurement peaks test, 24 hour alignment test, fiber elevation vs. coupling efficiency test, and laser sweep vs. piezoelectric actuator tracking test. Experimental results of fabricated devices are also illustrated at the end of this section.

3.3.1 Fiber Angles vs. Measurement Peaks

The purpose of this test is to show how coupling fiber angles affect the measurement response. Figure 3.5 shows three measurements where the fiber angle is at optimized position, 2 degrees less than optimized position, and 2 degrees more than optimized position. The maximized coupling power is located at 1548.5 *nm*; to achieve this coupling power, the fiber is adjusted to approximately 12 degrees. The maximum peak shifts relative to the angle variation (see Figure 3.5 (a)). At +2 degree relative to the optimal position, the maximum peak's corresponding wavelength is 1537 *nm*; at -2 degree relative to the optimal position, the maximum peak's corresponding wavelength is 1553.5 *nm*.



(a)



(b)

Figure 3.5: (a) The maximum peak shifts relative to fiber angle. (b) Optimal coupling power can be achieved by adjusting the fiber angle to match the designed grating coupler angle.

At optimal fiber angle, the maximum peak occurs at 1548.5 *nm*, which corresponds to the 1550 *nm* grating coupler used for this ring resonator. The coupling power at 1550 *nm* is -24.62 *dBm*, -26.91 *dBm*, and -30.16 *dBm* for optimal angle, -2 degree from optimal angle, and +2 degree from optimal angle, respectively (see Figure 3.6 (b)). The result of this experiment suggests that fiber angles should be re-adjusted for every chip so the fiber angle to grating coupler relationship is optimal.

3.3.2 24 Hour Alignment Test

The 24 hour alignment test is designed to test the stability of the setup over a long measurement time. The device choice for this test is a ring resonator. The fiber is first fine-aligned to the grating couplers of the ring resonator. The motor actuators are locked at the same position and the piezoelectric actuators are latched in place. Wavelength sweeps are initiated 12 times per hour, with a 5 minute halt between each sweep, over the time span of 24 hours. Ideally, the fibers should be tracking the optimal position continuously when wavelength sweeps are not initialized. In this experiment, the fiber tracking is purposely turned off so the stability of the motor and the position drift of the piezoelectric actuators can be observed. This experiment is carried out with the temperature controller set to 25 ^{o}C.

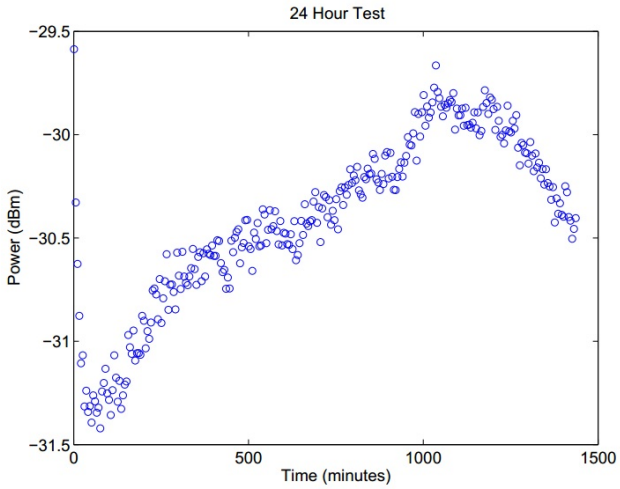


Figure 3.6: 24 Hour Test: Power vs. Time

As the temperatures stabilizes to 25 ^{o}C, a -2 *dBm* drop is observed

from the first wavelength sweeps. As the time progresses through the 24 hour stability test, the power gradually drifts between -31 *dBm* and -29.6 *dBm* (see Figure 3.6). Figure 3.7 documents the change in power every 5 minutes. The maximum coupling power variation is around ± 0.3 *dBm* in a 5 minutes time interval (see Figure 3.7). The experimental results suggest that the setup is relatively stable and thus is suitable for a long duration measurement.

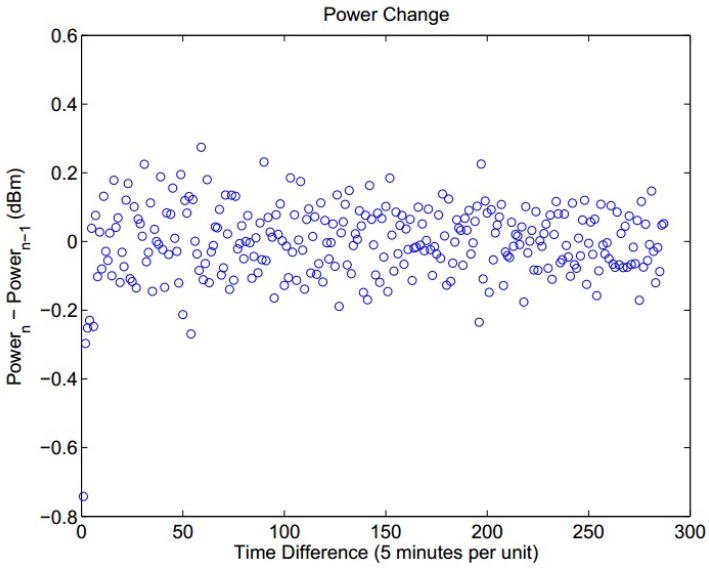


Figure 3.7: Power Change per 5 Minutes

3.3.3 Fiber Elevation vs. Coupling Efficiency

The change in distance between the input fiber and the grating coupler affects the coupling efficiency due to the change in laser spot size. The purpose of this experiment is to document the effect of the fiber-to-chip height on the coupling power. The coupling efficiency is expected to drop as we incrementally move the fiber tip away from the coupler. The fiber elevation experiment starts out by aligning the coupling fibers to the optimal position with an infinitesimally small fiber-to-chip height. A wavelength sweep is performed at each fiber-to-chip elevation as the fiber is moved away gradually at an interval of 4 μm. The final elevation of the fiber is approximately 80 μm above the grating coupler. At each elevation, the fibers

are re-aligned in their X and Y positions. The result is illustrated in Figure 3.8.

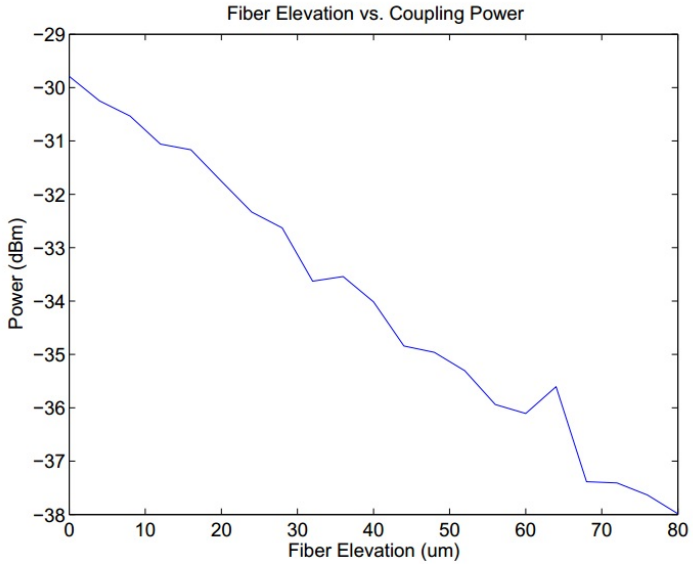


Figure 3.8: Fiber Elevation vs. Coupling Power

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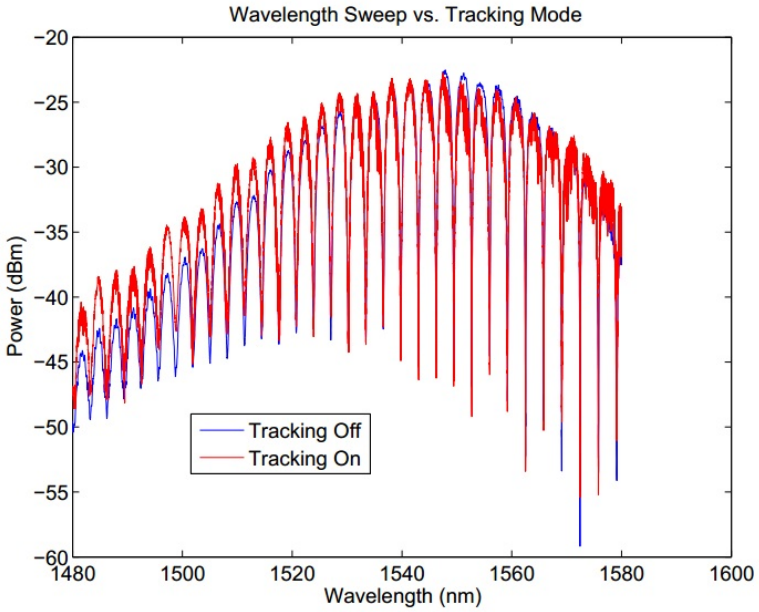
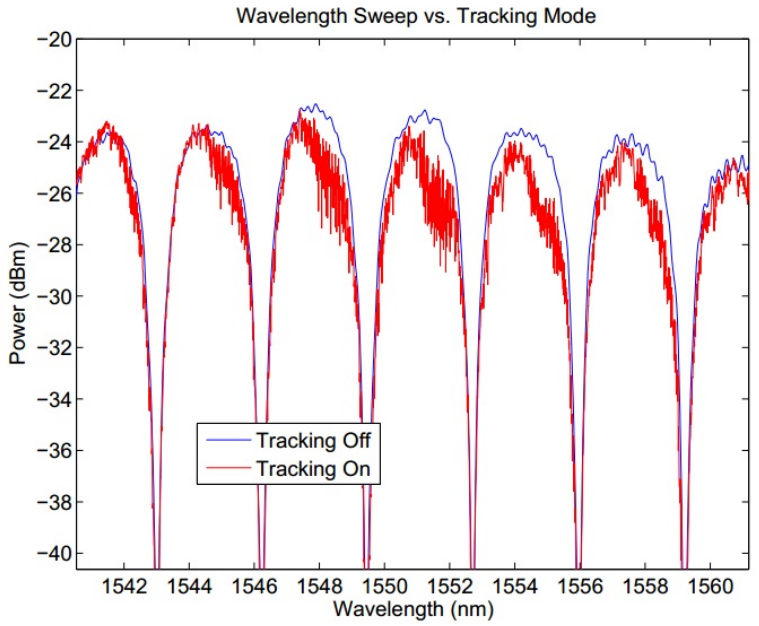
The result suggests that the power decreases as the fiber elevation increases as predicted. Currently, the fiber-to-fiber station is not capable of automatically determining the fiber-to-chip height. Hence in order to avoid damaging the fiber, the height of the fiber is kept at a safe distance away from the chip when the automated measurement algorithm is triggered.

3.3.4 Laser Sweep vs. Piezoelectric Actuator Tracking

With piezoelectric actuation, we can choose to track or latch the fibers during a wavelength sweep. Due to the nature of the grating coupler, the optimal position for every wavelength is slightly different. Hence, tracking during the measurement can provide data sets with less power difference between the highest peak and lowest peak (see Figure 3.9(a)). The purpose of this experiment is to determine the effect of piezoelectric actuator tracking on the measurement response.



(a)



(b)

Figure 3.9: Fiber Tracking vs. Coupling Peaks

Even though less power drop is observed when tracking is used, moving the fiber during an experiment is not desired because the movement from piezoelectric actuation introduces ripple noise to the system (See Figure 3.9 (b)). With tracking off, the power difference between the highest peak and the lowest peak is 21.59 *dBm*; with tracking on, the power difference is 17.30 *dBm*. The ripple introduced to the system by piezoelectric tracking is approximately 0.5 *dBm* at the peaks.

3.3.5 Device Measurement Results

The fiber-to-fiber automated setup is built for research purposes but is also used for graduate and undergraduate courses as well. In the past year, people who took photonic fabrication workshops and courses have been visiting our laboratory for stage demonstrations or to measure their designs. In this section, we show device measurement examples acquired from this setup.

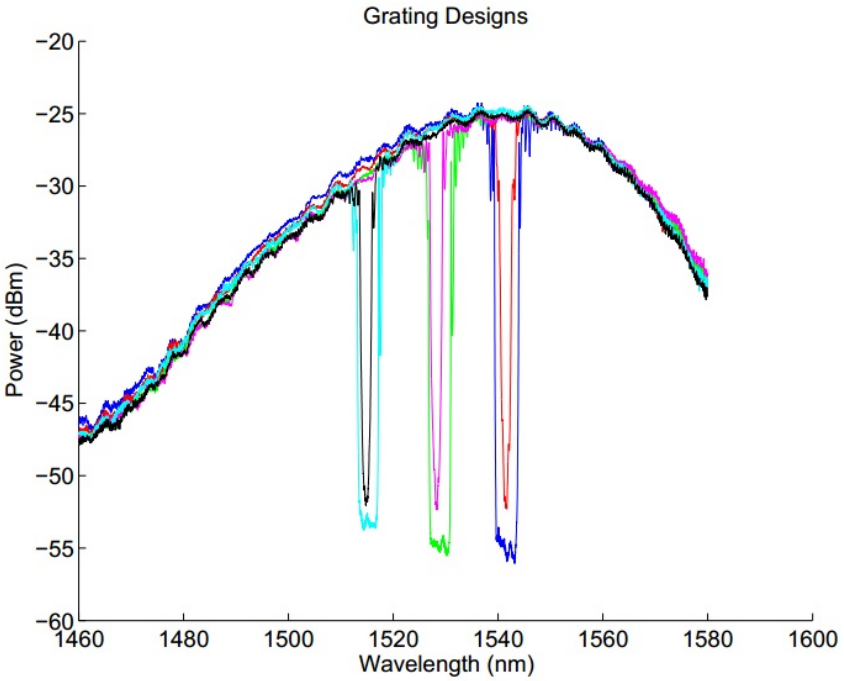


Figure 3.10: These are the measurement results of grating structures designed by Xu Wang (manuscript in preparation).

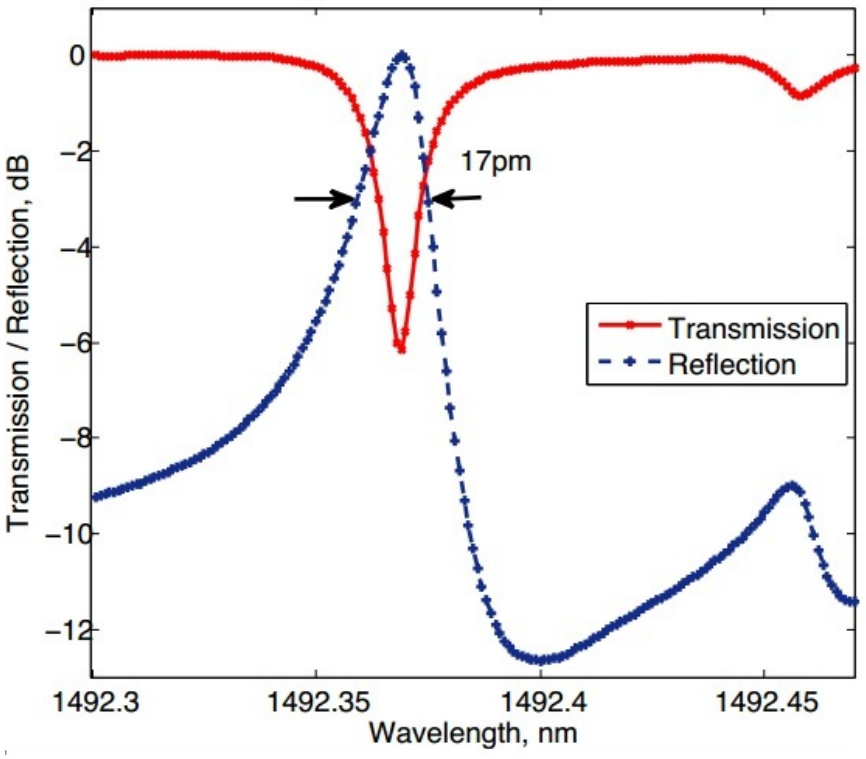


Figure 3.11: This is the transmission and reflection response of a disk resonator designed by Wei Shi [18].

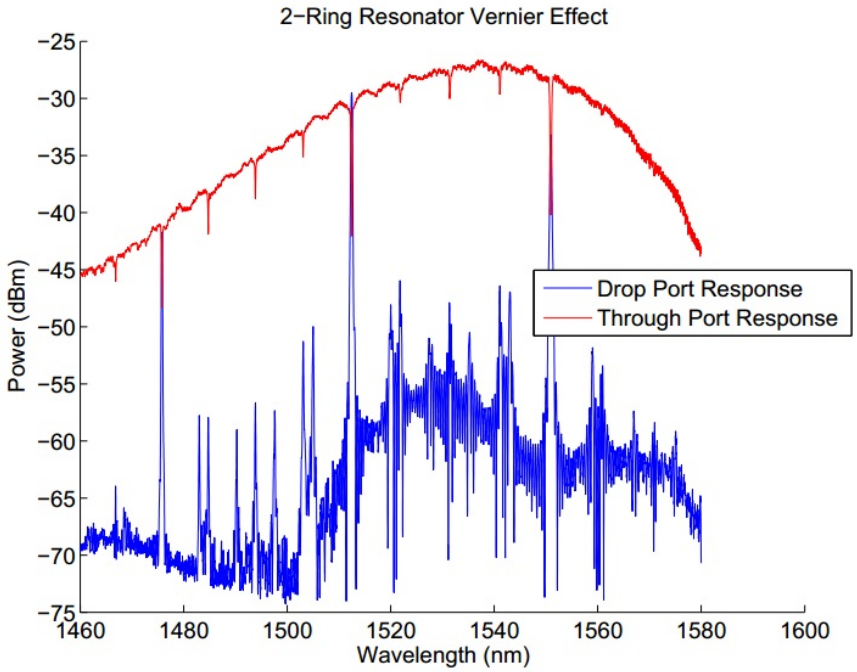


Figure 3.12: These are the measurement results of a 2-ring structure that demonstrates Vernier Effect designed by Robi Boeck (manuscript in preparation).

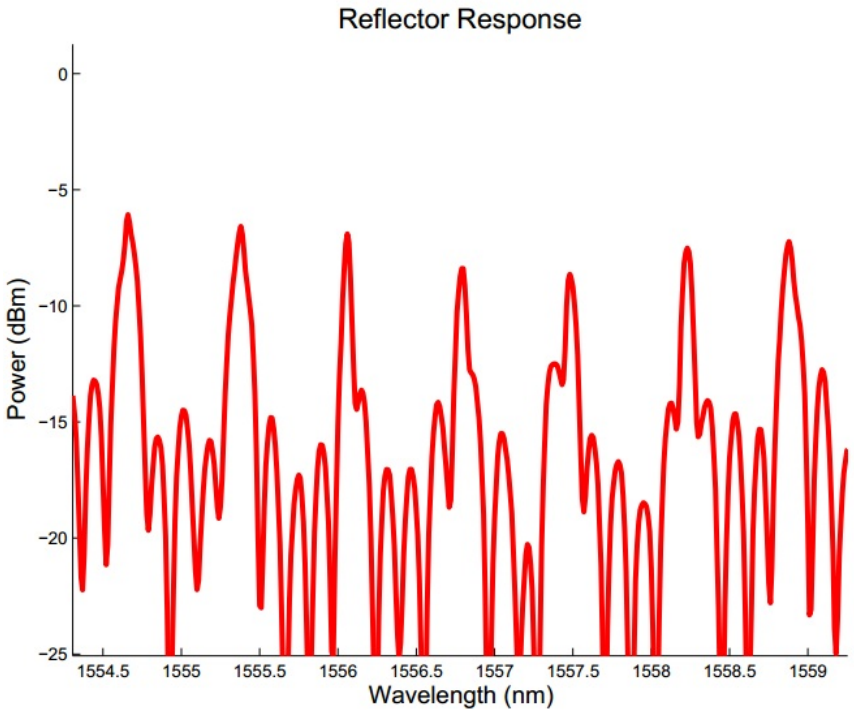


Figure 3.13: This is a measurement of the dumbbell narrow-band reflector designed by Han Yun [5].

Chapter 4

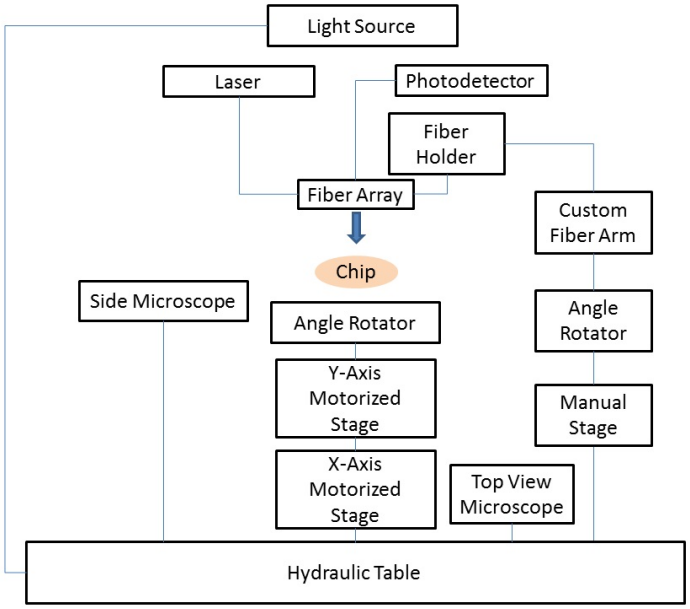
Measurement Setup: Fiber Array Automated Measurement Station

In fiber-to-fiber approach we use two copper fiber mounts to hold the input and output fibers to the left and right of the center stage, whereas in fiber array approach, we use a fiber array ribbon. This setup is inspired by the setup built by the OpSIS group from University of Washington [21]. Based on the performance of the their setup, we believe switching to the fiber array ribbon will greatly increase device coupling power.

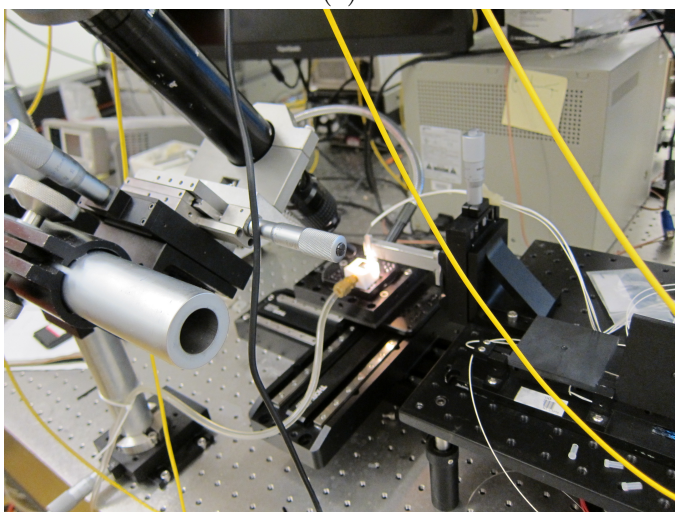
4.1 Station Overview

The chip is placed on top of the platform of an angle rotator that is on top of the Y-axis motorized stage. The Y-axis stage sits on top of the X-axis motorized stage and forms a cross configuration. The fiber array ribbon is held by a custom-made aluminum piece which is suspended on top of the chip platform by an aluminum arm that is attached to an angle rotator. The angle rotator is fixed onto a Z-axis manual actuator that is bolted to a raised platform so the fiber ribbon height can be adjusted accordingly. The ribbon-to-chip image is captured by two microscopes; one microscope shows the top view and is used for alignment purpose; the other microscope is angled from the side to display the height displacement between the fiber array and the chip to prevent crashing the fiber array into the chip during alignment. The light source for the microscopes illuminates the chip platform at an angle from behind the fiber ribbon (see Figure 4.1). The benefit of using the fiber ribbon setup is that only the chip is moving during automated alignment procedure rather than having to move two fibers like in the fiber-to-fiber setup. This makes the alignment process simpler. However, using the fiber array setup also requires the grating couplers to be routed in a standard configuration that corresponds to the fiber array used. In our case, the

grating couplers need to be lined up with a spacing of 127 μm.



(a)



(b)

Figure 4.1: (a) Fiber Array Setup Block Diagram Illustration. (b) Fiber Array Setup.

4.1.1 Station Specification

To improve the automated fiber array setup performance, the following criteria are required:

1. Stage Automation

    - To achieve mask level automated measurement, the stages are required to be automated and have large enough maximum travel to cover the entire chip. The Thorlabs stages used allow only single axis actuation but have a maximum travel of 220 mm. These two stages are set up in an XY configuration and are responsible for both coarse and fine alignment of the fiber array [15].

2. Laser Coupling

    - The laser is coupled in and out of the device via fiber array (fabricated by PLC Connect). Fiber array ribbon is a plastic piece; the fibers are separated 127 μm apart and are glued onto the carved channel cavities. The fibers are polished along with the plastic tip surface of the ribbon. The fiber array ribbon that is currently implemented is a 4-channel fiber array polished to 10° (see Figure 4.3 (a)).

3. Fiber Arm and Holder

    - The fiber array holder is a slotted aluminum piece that uses side screws to hold the fiber array ribbon. The custom-made aluminum arm secures the holder in a similar fashion and is connected to an angle rotator (see Figure 4.2).

4. Angle Adjustments

    - The fiber-grating coupler angle and chip-to-array orientation are important factors that affect the coupling power. An angle rotator is implemented to adjust the incident angle between the fiber array and the grating couplers. Another angle rotator is placed under the chip the grating coupler pair angle can be matched with fiber array angle; this is done by making sure the fiber array ribbon edge is parallel to the chip edge under the microscope.

5. Fiber-to-Chip Height Adjustment

- A manual stage is attached to the fiber arm and holder. This manual stage is installed so the height between the fiber array and the chip can be changed accordingly.

6. Laser Source and Photodetector

   - The same type of laser and photodetector used in fiber-to-fiber automated measurement station is used for the fiber array station (see section 3.1.1).

7. Microscopes and Light Source

   - The side microscope is angled around 10^o and provides the fiber-to-chip height view. The main microscope and its corresponding light source shows the top view of the fiber array and is used as a reference during device alignment. Figure 4.3 shows the top view with and without the fiber array aligned.

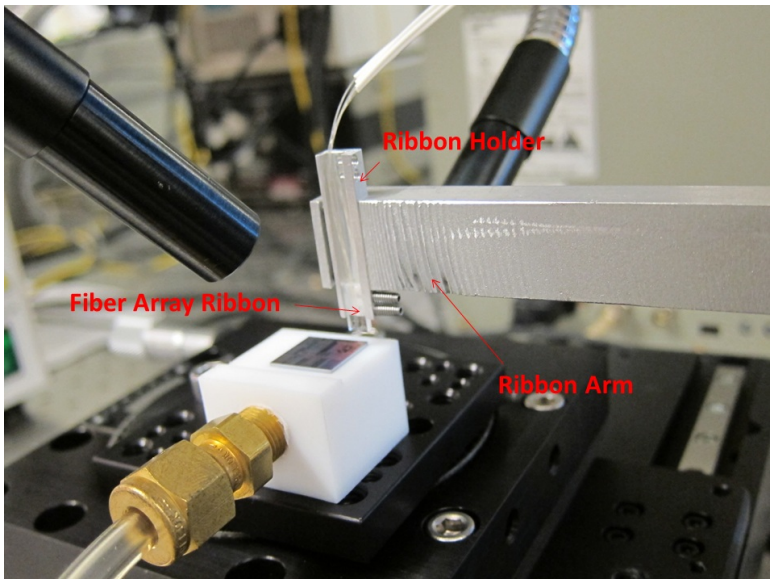
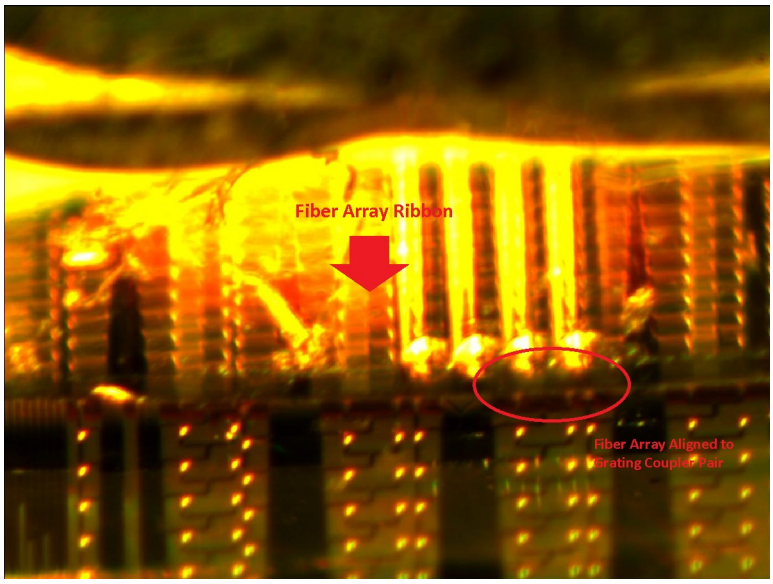
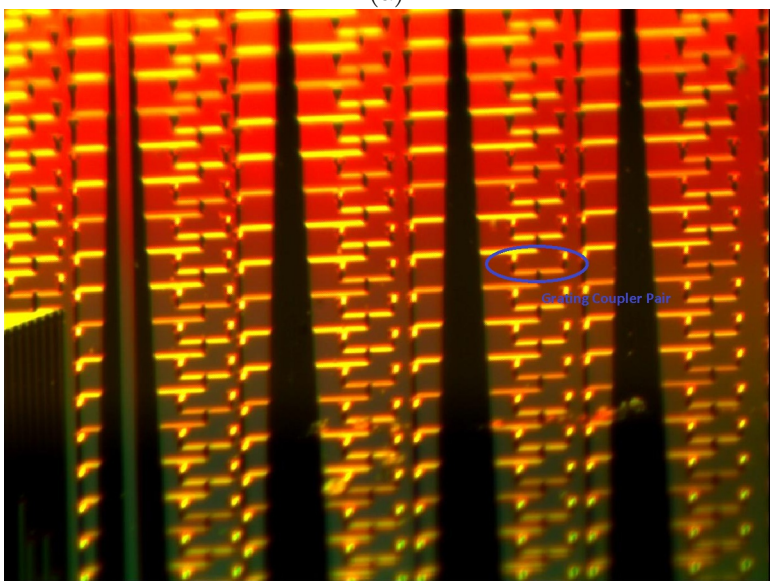


Figure 4.2: Fiber Array Ribbon Holder and Fiber Arm



(a)



(b)

Figure 4.3: (a) Fiber Array Setup Microscope Top View with Fiber Array. (b) Fiber Array Setup Microscope Chip Top View.

4.2 GUI Software

Manual fiber array alignment is not as trivial as fiber-to-fiber alignment. It is difficult to align the fiber arrays under the microscope because the location of the input and output fiber is difficult to identify (see Figure 4.3). To address this issue, several alignment algorithms are implemented to help with the visualization of the current fiber and grating coupler positions. Using these functions, we can locate the desired grating couplers and use the GDS mask coordinates to map all the actual coordinates of the devices and hence perform chip level automated measurements. The GUI is constantly being updated to include new functionalities [20]. It is now more user-friendly and include 1220 *nm* laser controller module. The typical measurement flow for manual and automated device characterization are illustrated in the following flow charts (see Figures 4.4 and 4.5).

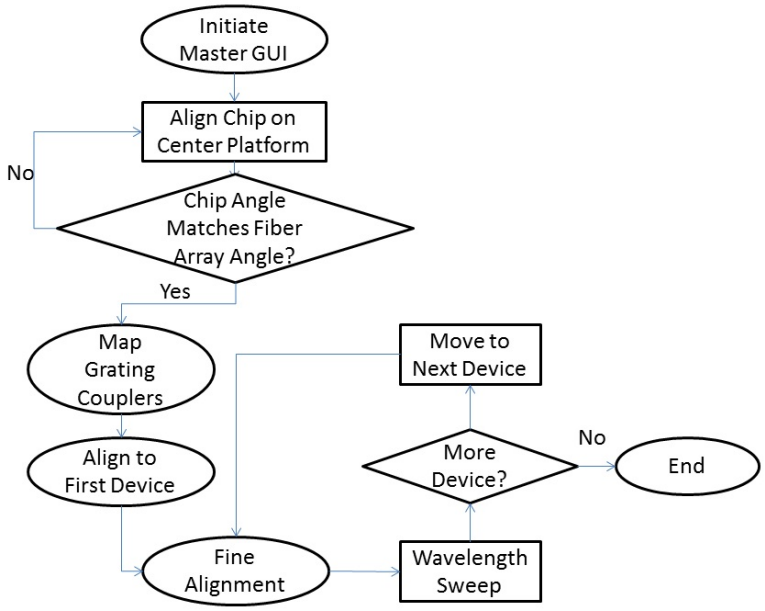


Figure 4.4: Manual Device Measurement Flowchart

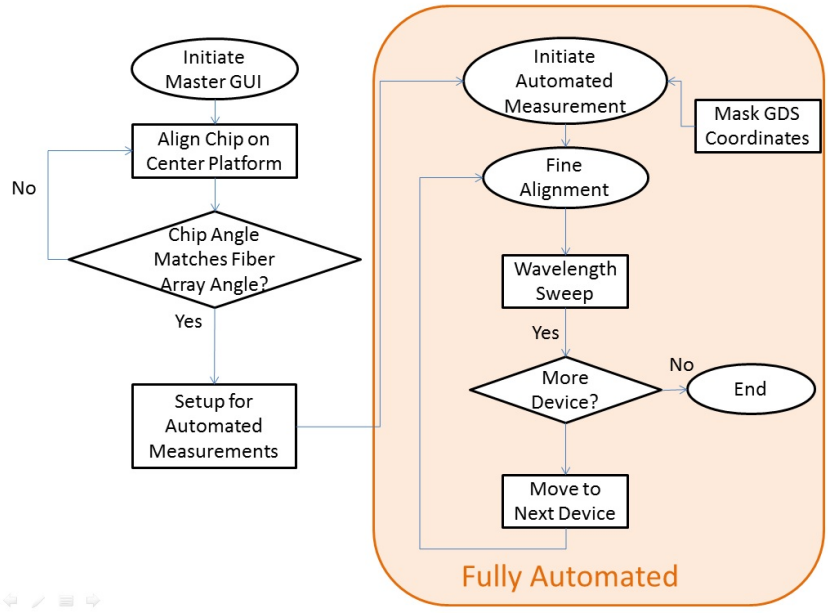
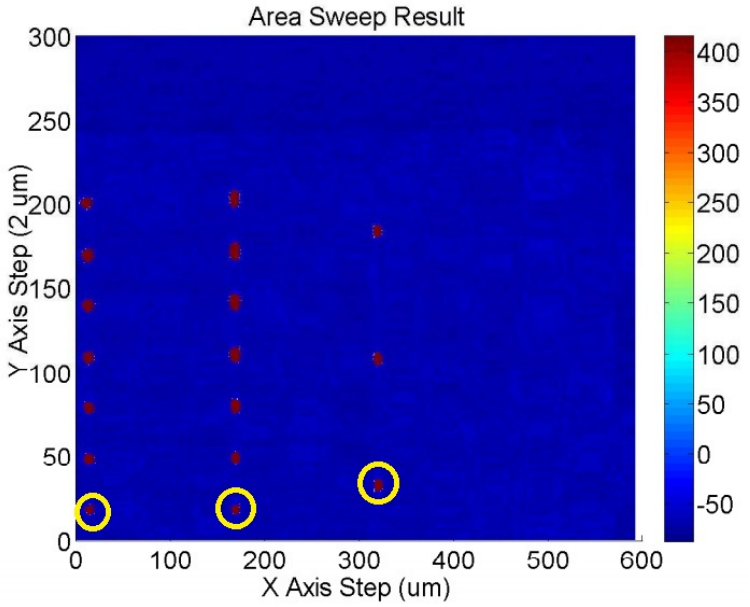


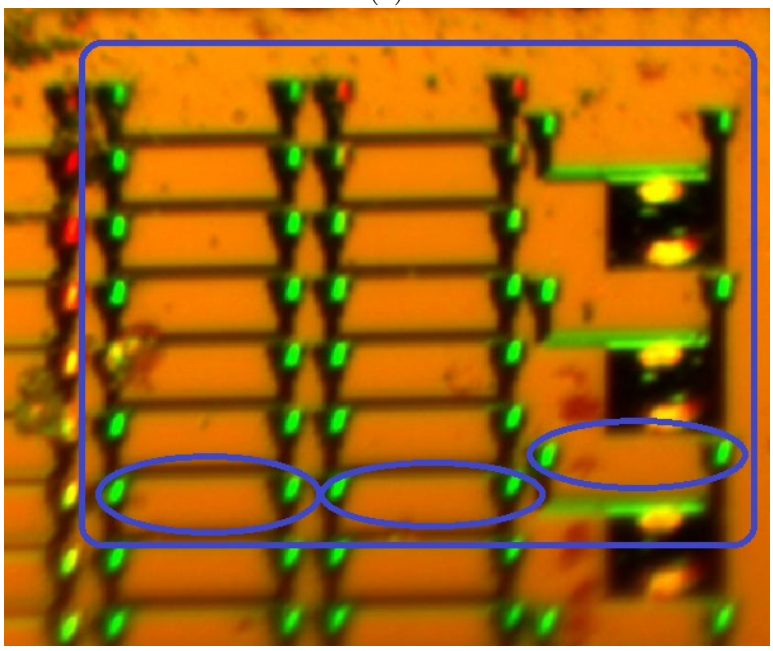
Figure 4.5: Automated Device Measurement Flowchart.

4.2.1 Area Sweeping

Map sweeping function scans a small area in proximity to the current location of the fiber ribbon. The function moves the fiber ribbon in a snake-like fashion and record the power continuously (see Figure 4.7 (b)). The scan window is user defined. A contour plot is generated at the end of the sweep to provide a visual of the relative coupling of the swept area; the color bar is in *dBm* (see Figure 4.6 (a)). Each point of the plot represents a power value collected via power sensor. The corresponding grating coupler microscope image is illustrated in Figure 4.6 (b). The circled coupling peaks in Figure 4.6 (a) correspond to the circled grating coupler pairs in Figure 4.6 (b). The X axis of the plot represents the total data point collected per line; each unit in Y axis represents the Y displacement performed. The red power points in the figure represents the locations of the grating couplers. The flowchart of this program is shown in Figure 4.7 (a).

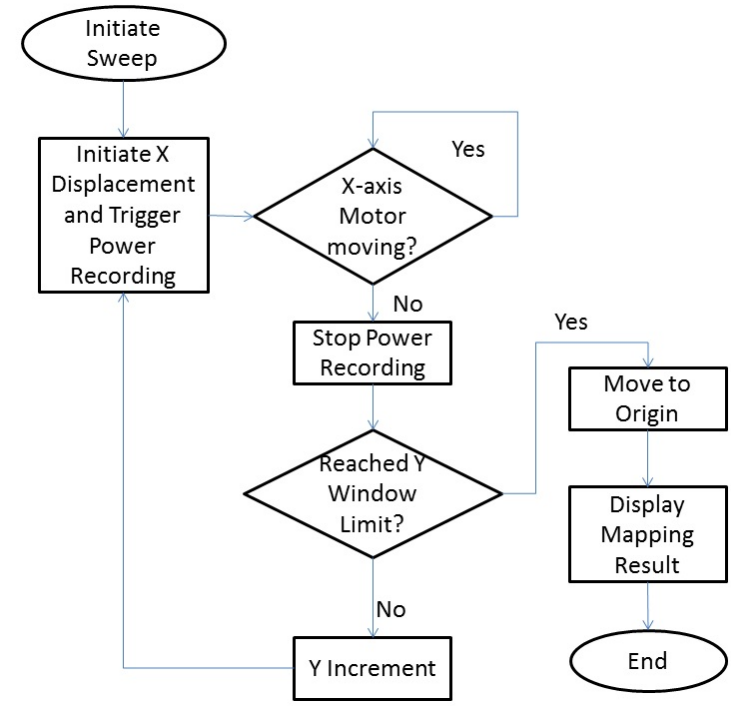


(a)

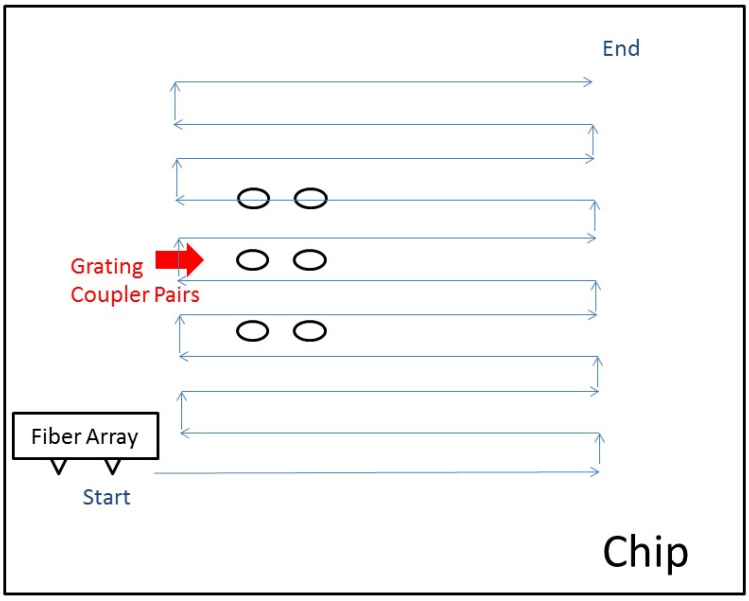


(b)

Figure 4.6: (a) Grating Coupler Intensity Mapping. (b) Corresponding Grating Coupler Microscope Image.



(a)



(b)

Figure 4.7: (a) Area Sweeping Algorithm Flowchart. (b) Fiber Array Travel Pattern.

4.2.2 First Device Alignment and Fine Alignment

Because the exact location of the input fiber cannot be located with the naked eye through the microscope, we implement the first device alignment algorithm for device alignment. After the area sweeping function outputs a intensity map and confirms that working grating couplers are in proximity, this function locates the first working device and performs the fine alignment algorithm. First device alignment uses a similar approach as the map sweeping algorithm. If the recorded power that correspond to the current displacement meets the coupling threshold criteria, the motor is stopped and relocated to the detected coupler. The fine alignment algorithm scans first in the X axis and moves to the optimal X axis coupling position and performs a similar scan in the Y axis; the fine alignment process takes around 10 seconds. After the optimal position of coupling is reached, the motor coordinates are recorded and used for chip level auto-mapping algorithm. The flowcharts that represent the first device alignment and fine alignment algorithm are presented in Figure 4.8 and 4.9 respectively.

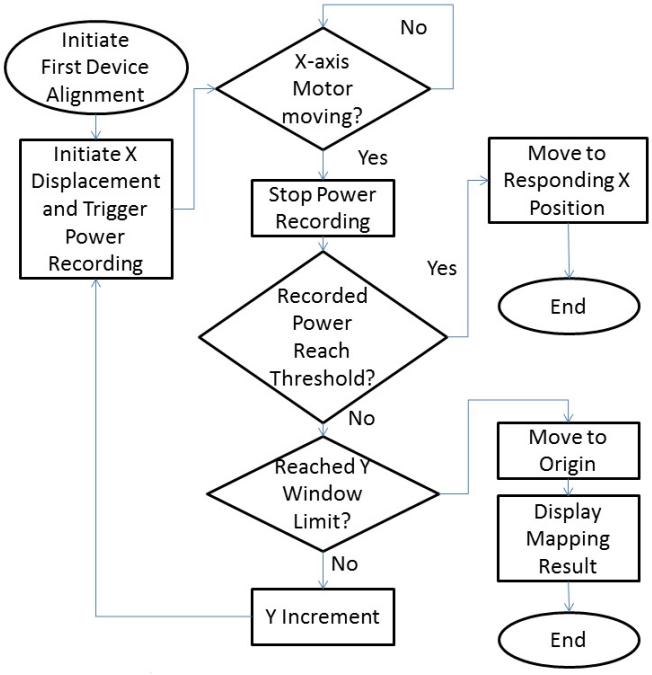


Figure 4.8: First Device Alignment Flowchart

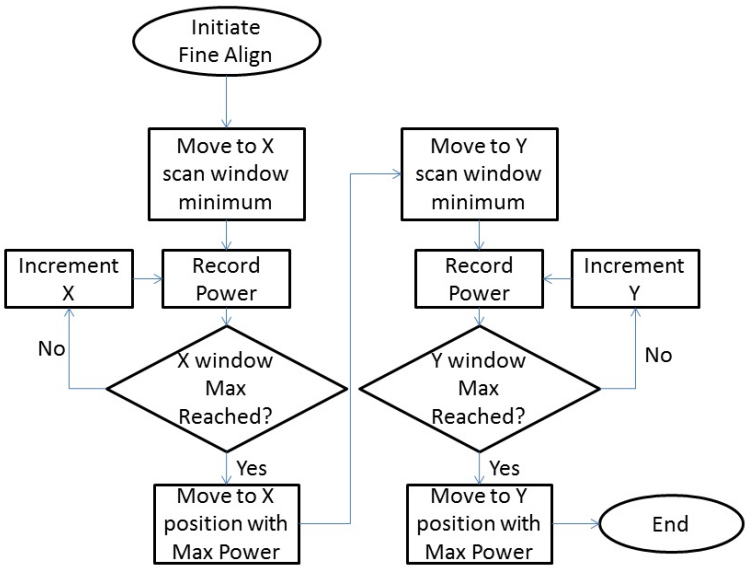


Figure 4.9: Fine Alignment Flowchart

4.2.3 Chip Level Auto-Measuring Algorithm

The chip level auto-mapping algorithm is defined by two functions. The first function takes in motor coordinates and GDS coordinates and outputs chip rotation angle relative to fiber ribbon and magnitude scaling factor. A total of four motor coordinates are required along with their corresponding GDS coordinates. The angle and distance relations between all the input motor coordinates are calculated and compared to the relations of the GDS coordinates. An average value of the angle difference between the coordinates are used to represent the chip rotation angle. The magnitude scaling factor is deduced in the same fashion through cosine law. The calculated rotation angle and scaling factor are applied to three of the input motor coordinates to find the relative fourth motor coordinates. The calculated fourth motor coordinate values are averaged and compared to the inputed fourth motor coordinate. The errors between these values are calculated and if they are within a tolerable range, the function will output the calculated chip rotation angle and magnitude scaling factor. The second function of this auto-mapping algorithm takes in the previous calculated rotation angle and scaling factor and use them to deduce the corresponding motor coordinate matrix. By feeding this function a GDS coordinate array, we can

map all the grating couplers on the chip, and therefore chip level testing can be performed. See Figure 4.10 for the complete flowchart of the chip level auto-mapping algorithm.

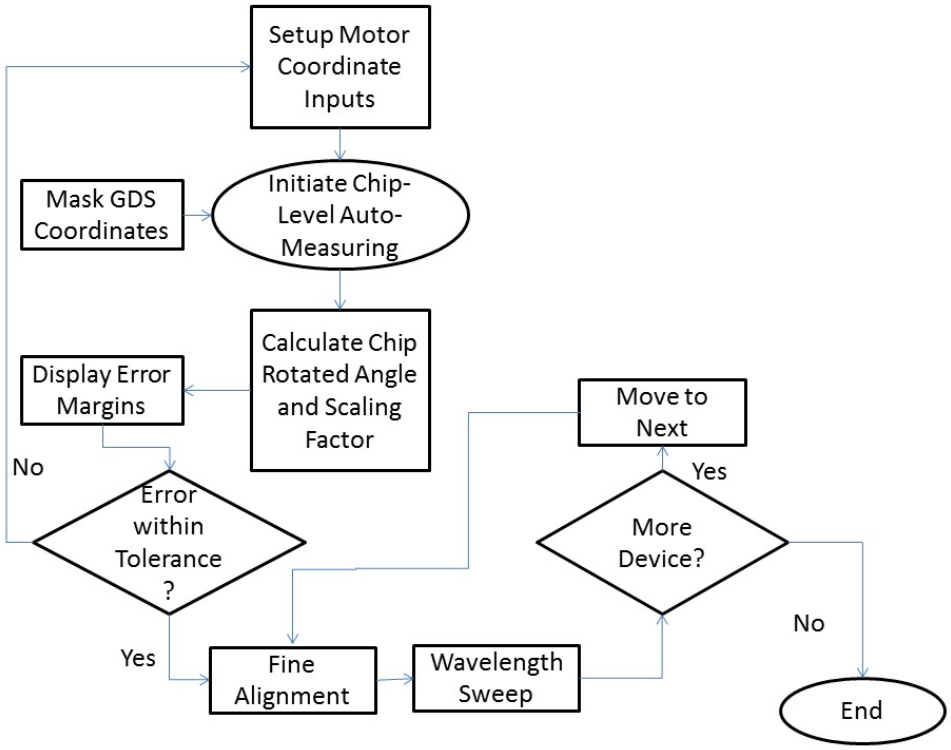


Figure 4.10: Chip Level Auto-Measuring Algorithm

4.3 Automated Setup Tests and Measured Results

Stability tests similar to those listed in the fiber-to-fiber setup section are performed to illustrate the stability of the fiber ribbon setup. These tests include: fiber ribbon angles vs. measurement peaks test, repeated alignment test, and 24 hour alignment test. Device measurement results of several different designs are included at the end of this section.

4.3.1 Repeated Alignment Test

The repeated alignment test is performed to show the performance of the first device alignment and the fine alignment algorithm. First, fine alignment algorithm is triggered to locate the optimal coupling position of a ring resonator. The fiber array is then moved out of optimal position and re-aligned repeatedly. The coordinate of the fiber array is recorded after each re-alignment. By summarizing the change in the optimal coupling location after each re-alignment, we can understand the performance of the alignment algorithms.

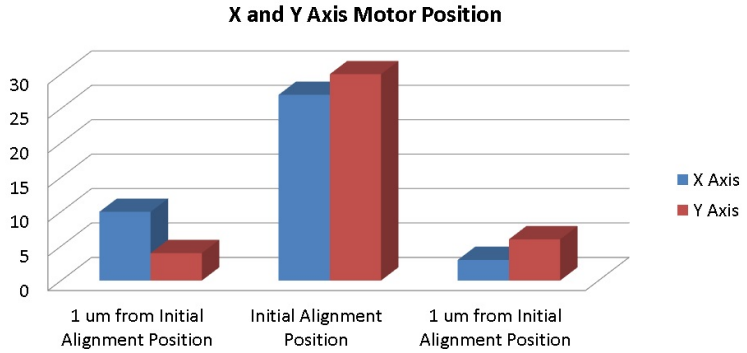


Figure 4.11: Fiber Array Position Summary with 4 mm^2 window.

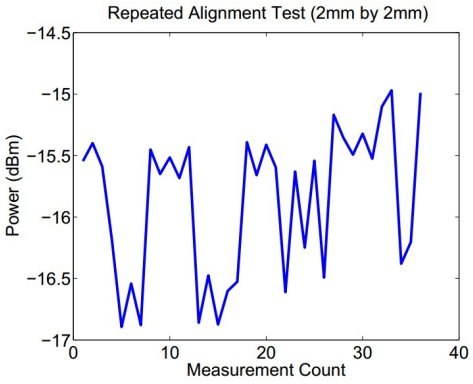


Figure 4.12: Fiber Array Power Summary with 4 mm^2 window.

This test is performed twice with a 2 mm by 2 mm and 10 mm by 10 mm X and Y displacement window. Figures 4.11 and 4.13 correspond to the motor position for the 4 mm^2 window and 100 mm^2 window respectively. And Figures 4.12 and 4.14 correspond to the measurement power after every re-alignment. Each test sequence iterates for 40 times. The experimental result indicates that during fine alignment, the stages have a ± 1 μm variation. This variation is within tolerance range. Overall, the system is stable in terms of device re-alignment and relative motor displacement.

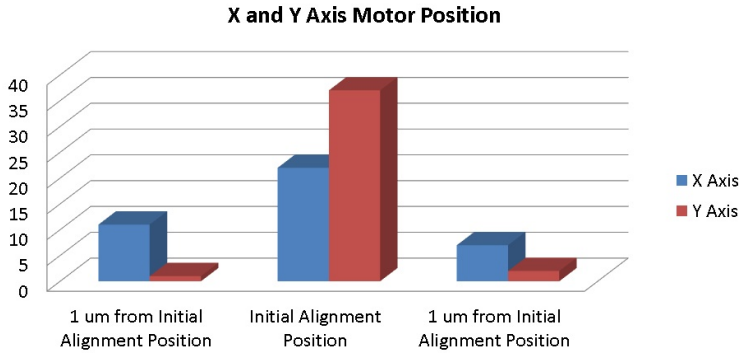


Figure 4.13: Fiber Array Position Summary with 100 mm^2 window.

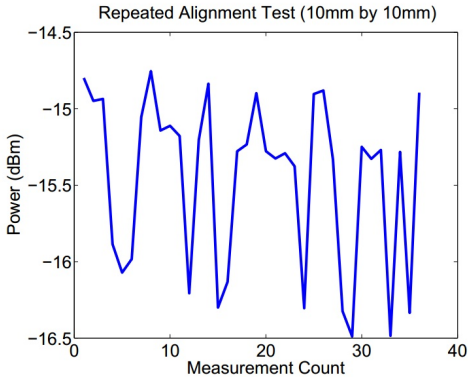


Figure 4.14: Fiber Array Power Summary with 100 mm^2 window.

4.3.2 24 hour alignment test

A ring structure is used for the 24 hour alignment test. This is the same test performed on the fiber-to-fiber automated measurement station (see section 3.3.2). A wavelength sweep is performed every 5 minutes and the maximum value of the sweep is used to plot Figure 4.15. The temperature controller is not available on the fiber array setup.

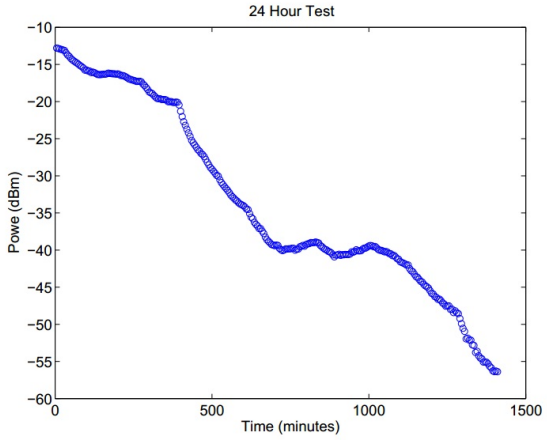


Figure 4.15: 24 Hour Test: Power vs. Time

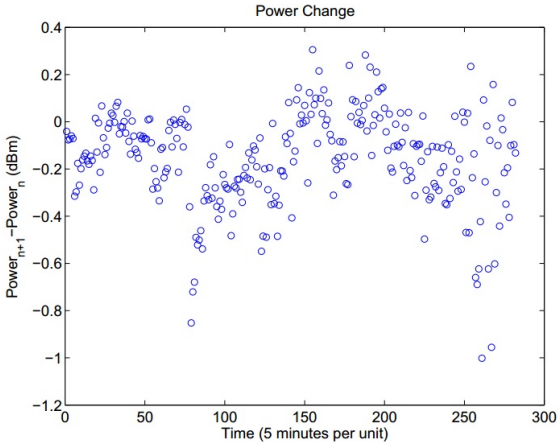


Figure 4.16: Power Change per 5 Minutes

The coupling power drops dramatically over the duration of the experiment. The DDS200 stages used in the fiber array setup appear to be not as stable as the MAX300 stages used in the fiber-to-fiber setup. The total power drop of 43 *dBm* over 24 hours illustrated in Figure 4.15 corresponds to a 3 μm and 2 μm motor movement in Y axis and X axis motorized stage respectively; these values are obtained from comparing the re-aligned motor coordinates (after stage drift) and the motor coordinates before the drift occurs. The power change per 5 minutes illustrated in figure 4.16 shows a maximum drop of 1 *dBm* over the duration of 5 minutes. As a result, fiber array automated measurement station is currently not suitable for long duration single device measurements.

4.3.3 Fiber Array Angles vs. Measurement Peaks

The fiber-to-grating angle test performed on the fiber array setup follows the same concept as illustrated for the fiber-to-fiber setup (see section 3.3.1).

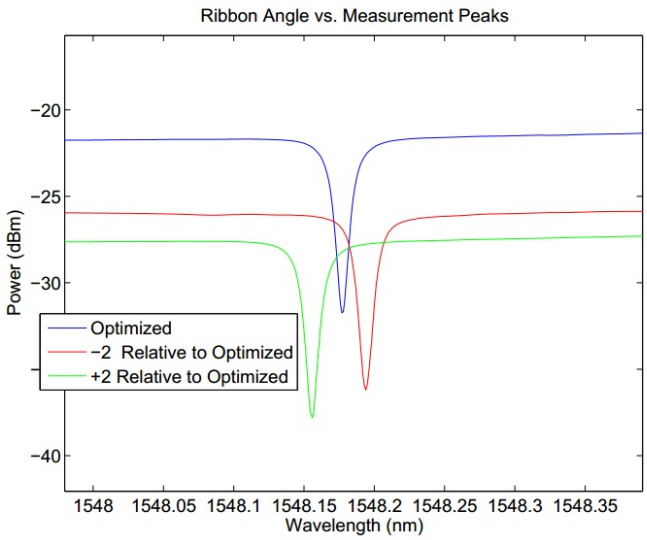


Figure 4.17: Fiber Ribbon Angle vs. Measurement Peaks

At optimal angle, the coupling power is -30.81 *dBm* at center trough wavelength 1548.17 *nm*. With a -2 degree change relative to the optimal angle, the coupling power is -35.95 *dBm* at center trough wavelength 1548.20 *nm*. With a +2 degree change relative to the optimal angle, the coupling

power is -36.33 *dBm* at center trough wavelength 1548.16 *nm* (see Figure 4.17). The power drop when the fiber-to-grating coupler angle is not optimized suggests that re-optimization of the fiber array ribbon angle should be performed each time the device chip is changed.

4.3.4 Device Measurement Results

In this section, device measurement results obtained from the fiber ribbon automated setup are included. These measurements include grating-ring resonators, bio-sensing ring resonators, and grating couplers.

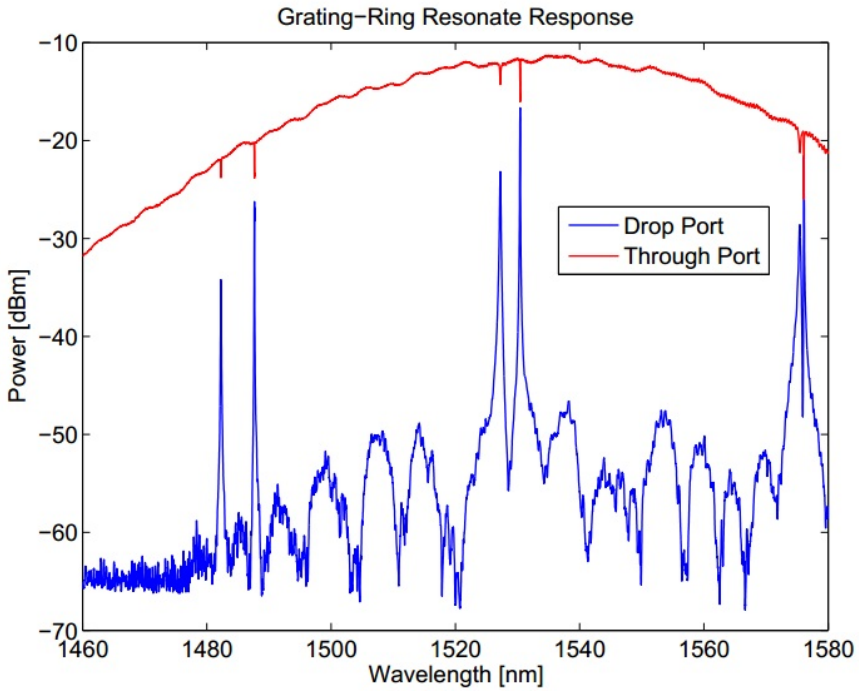


Figure 4.18: These are the through and drop port response of grating-ring resonators designed by Wei Shi (manuscript in preparation) [14].

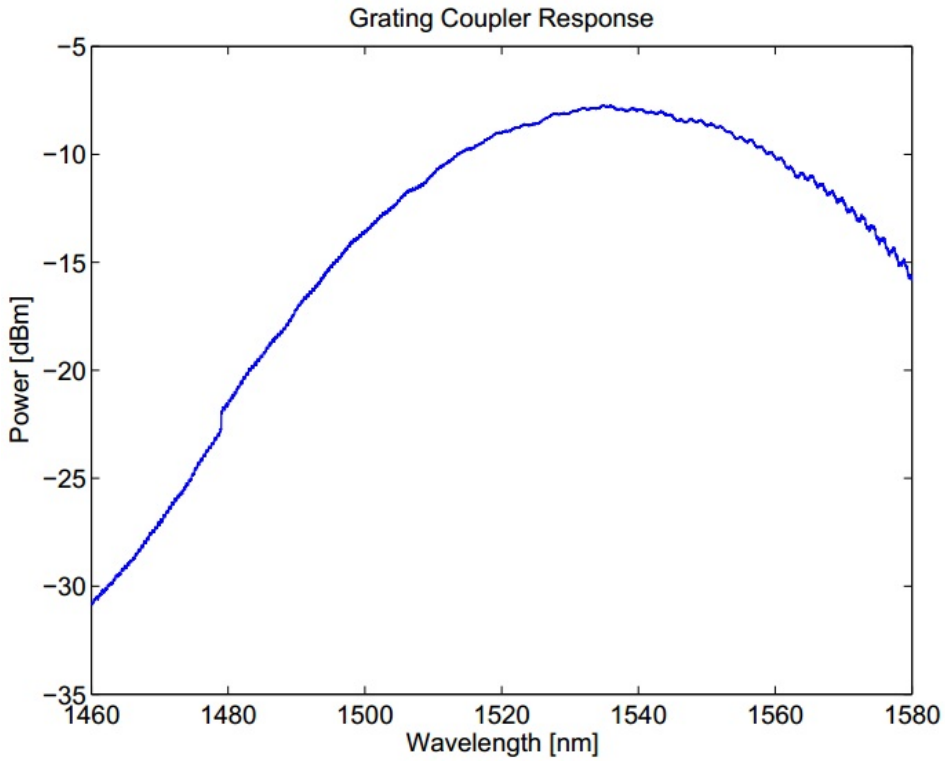


Figure 4.19: This is a measurement of a grating coupler pair designed by Oscar Wang. This design consists of two grating couplers separated 127 μm apart; they are connected together with a straight waveguide. The -7.7 dBm coupling power obtained suggests that the grating couplers have a 3.8 dBm power loss each. This is the highest coupling power value observed with the fiber-to-fiber or fiber ribbon setup [9].

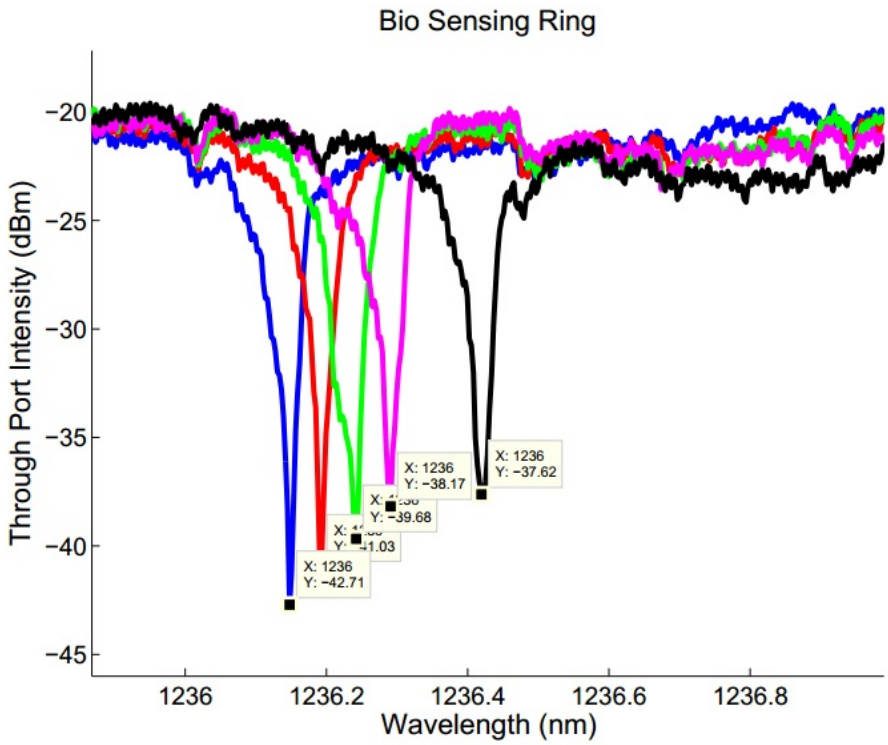


Figure 4.20: These ring resonators are designed to operate at 1220 *nm* by Jonas Flueckiger. A 1220 nm laser is used for this experiment. This plot illustrates the shift observed when the device is exposed to solutions with different $NaCl$ concentrations [20].

Chapter 5

Conclusion

The primary goal of this thesis is to improve the traditional photonic device design flow. With the mask drawing methods introduced, device simulation and layout design can occur simultaneously. The introduced mask design methods, nested PCell approach and hierarchy approach, are capable of generating device structures with different parameter combinations effectively. As a result, simulations can be performed directly on the generated GDS mask files to more accurately predict device performance. Bragg grating designs, for example, benefit from this feature significantly because they require accurate lithography simulation follow by FDTD to accurately predict the device performance. With multiple mask-layout-to-simulation iterations, the physical drawing constraints are kept in check while device performance is being imrpoved. Therefore, situations where optimal device parameters are physically incompatible with fabrication process will not occur. The nested PCell approach and hierarchy approach are both scripted; this makes error fixing trivial compared to traditional manual mask drawing approaches. As silicon photonic research groups evolve from experimenting with simple photonic structures into studying complex devices or systems, having a quality mask design method that improves the design efficiency, reduces design error, and emphasizes the mask re-usability becomes more crucial towards improving their research flow. Hence, the application of this method towards all future photonic masks designs is advised.

To effectively carry out device testing, we introduce the concept of two automated measurement stations, the fiber-to-fiber setup and the fiber array setup. By linking the coupler coordinates in the mask GDS file to the measurement algorithm, the automatic GDS coodinate-driven testing is possible. Switching from manual measurement stations to automated stations provide a big leap in terms of photonic device design efficiency. With traditional manual testing stations, the measurement process requires a tremendous amount of time and effort because it requires ones presence. With the testing procedure fully automated, hours that are required to obtain measurement results can be minimized. As a result, the implementation of automated stations are advised in order to further improve the efficiency of

silicon design flow. The active device measurement is not yet supported. To add the active device measurement capability, we require automated actuation to adjust the height of chip so it can be raised to be in contact with the added probe.

The fiber-to-fiber and fiber array automated measurement stations may serve the same purpose, but they are two very different stations due to their design architecture and parts used. The pros and cons of the fiber-to-fiber and the fiber array setups are illustrated below:

Fiber-to-Fiber Setup Pros:

- Allows multi-device testing
- Supports temperature control
- Allow almost any input/output grating coupler configuration
- Has minimum stage drift overtime
- Easy coupling fiber replacement when damaged
- Easy device alignment
- Supports 1 input and multiple output device configuration

Fiber-to-Fiber Setup Cons:

- Presently Supports only passive device measurement
- Does not support chip-level automated testing due to stage travel limitations
- Multi-device testing limited by the 4 mm stage travel
- High insertion loss; the total insertion loss is typically around -17 dB
- Sensitive to acoustic vibration (introduces noise to the measurement)

Fiber Array Setup Pros:

- Allows multi-device testing
- Allows chip-level testing
- Low insertion loss; the total insertion loss is typically around -7.7 dB
- Fiber array measurements have less ripple noise

- Additional probes can be easily added to support active device measurements

Fiber Array Setup Cons:

- Presently Supports only passive device measurement
- Requires paired input/output couplers
- Temperature control not yet supported
- Not suitable for long measurements due to excessive stage drift overtime
- Fiber array needs to be re-ordered when damaged
- Fiber array is difficult to align manually
- 1 input and multiple output device measurement requires multiple photodetectors and is limited to 3 output channels only for the 4-channel fiber array we purchased

The insertion loss values listed are not inherent. They are the best coupling loss observed with our current setups. Both the grating coupler and the cleaved fiber or polished fiber array contribute to this loss and can be further improved. After installing the fiber-to-fiber and the fiber ribbon setup, experiments that require multiple measurements only require an initial set up time of 10 minutes. This is a large efficiency improvement compared to our outdated manual setup where measuring 30 devices requires one's constant attention of 1 to 2 hours.

By implementing the PCell method, the hierarchy method, and the automated testing stations, the overall efficiency of the silicon photonic design process is improved; the design process is becoming more like CMOS analog design process. Companies, such as Luxtera, have been integrating optic designs into their fabrication platform. Ultimately, the characterized optical components become basic circuit building blocks, like resistors, capacitors, or diodes in CMOS designs, which can be accessed as part of a toolkit for optoelectonic circuit design [26]. IPKISS, developed by the Photonic Research Group of Ghent University and IMEC, is another program that can be used to design photonic components and complex photonic integrated circuits. A designer can directly simulate the defined photonic components in electromagnetic solvers and then integrate them into a photonic circuit for mask

fabrication [28]. To the best of our knowledge, there are no commercial system available for the fiber-to-fiber measurement station introduced. Both OpSIS and Luxtera use fiber array ribbon in their wafer-level automated testing stations. Active device measurement is also available on Luxtera's testing platform. In the near future, we want to improve our mask design process to include schematic driven layout and layout versus schematic verification. Also we want to improve the capability of the current fiber-to-fiber and fiber array measurement stations and meet the requirements for automated active device wafer-level testing.

5.1 Suggestions for Future Work

1. Pyxis Development
   - Categorize GDS and PCell Library components
   - Generate documentations for developed library components
   - Implement Pyxis Auto-routing tool to accelerate Schematic Driven Layout flow and allow system level simulation capability.
   - Implement new Mentor Graphics tools so Layout Versus Schematic (LVS) verification is possible.
2. Fiber-to-Fiber Measurement Station
   - Improve fiber-to-coupler angle adjustment by re-designing fiber arm
   - Implement a height adjustment algorithm to maximize coupling efficiency
   - Further study is required to characterize the motor drift over time
   - Re-configure the station to allow active device measurement
   - Re-design fiber holder to allow the implementation of lensed fibers
3. Fiber Array Measurement Station
   - Chip level automated measurement algorithm needs to be tested more extensively
   - Implement stages that support position feedback to minimize stage drifting over time
   - Implement a temperature controller to allow temperature tuning.
   - Re-configure the station to allow active device measurement

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Appendix A

Taper PCell Script

```
function my_taper3()
{
        local device = $get_device_iobj();
        local length = $get_property_value(device,"length");
        local my_layer = $get_property_value(device,"my_layer");
        local h = $get_property_value(device,"h");
        local h2 = $get_property_value(device,"h2");
        local tl = $get_property_value(device,"tl");
        build_taper(my_layer,length, h, h2, tl);
}
function build_taper(my_layer: string {default="Layer1"}, length :
number {default=3}, h : number {default=1}, h2 : number {default=1},
tl : number {default=100})
{       local se = 3;
        $add_shape([ [0,h2],[1*length/100,h2+h/10],
                                [4*length/100,h2+2*h/10],[9*length/100,h2+3*h/10],
                                [16*length/100,h2+4*h/10],[25*length/100,h2+5*h/10],
                                [36*length/100,h2+6*h/10],[49*length/100,h2+7*h/10],
                                [64*length/100,h2+8*h/10],[81*length/100,h2+9*h/10],
                                [100*length/100,h2+10*h/10],[length,h2] ],se);
        $add_shape([ [0,0],[1*length/100,-h/10],
                                 [4*length/100,2*-h/10],[9*length/100,3*-h/10],
                                 [16*length/100,4*-h/10],[25*length/100,5*-h/10],
                                 [36*length/100,6*-h/10],[49*length/100,7*-h/10],
                                 [64*length/100,8*-h/10],[81*length/100,9*-h/10],
                                 [100*length/100,-10*h/10],[length,0] ],se);
}
function taper_parameters( my_layer: optional string {default =
"Layer1" }, length: optional number {default =3},h: optional number
{default =1}, h2: optional number {default =1}, tl: optional number
{default =100})
{ return [ ["my_layer",my_layer],["length",$g(length)],["h",$g(h)],
```

```
["h2",$g(h2)], ["tl",$g(tl)]  ]; }
```