A STUDY OF TWO WIDEBAND CMOS LC-VCO STRUCTURES

by

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Abstract

Phase-locked loops (PLLs) are widely used in telecommunication, radio, and computer applications. This thesis focuses on the study of wide-band PLLs, as they are a critical building block of many wireless and wireline systems. In particular, wide tuning range, low phase noise, and low power are desirable attributes for multi-standard and multi-band communication systems. One of the most critical components in a PLL is the voltage-controlled oscillator (VCO). In this work, two techniques for implementing a wide-tuning-range LC-VCO are presented. As a proof of concept, the techniques are used to design and layout two 13-GHz LC-VCOs, which are fabricated in a 90-nm CMOS technology and successfully tested. One design (Design A) uses two VCO cores and has an extra source-follower buffer while the other (Design B) uses one VCO core with a bank of switched capacitors. The 90-nm CMOS prototypes operate from a supply of 1.2 V. The Design A prototype has a 28.20% tuning range and a phase noise of –90.98 dBc/Hz at 1 MHz offset from the carrier, while the Design B prototype has a 24.42% tuning range and a phase noise of –94.20 dBc/Hz at 1 MHz offset. This measured performance is comparable with state-of-the-art wide-tuning-range VCOs. The total chip size, excluding pads, is 0.335×0.750 mm^2 and 0.316×0.425 mm^2 for Designs A and B, respectively. It was found that the addition of the source-follower buffer allows the VCO to function at a higher frequency, while the presence of the switched capacitor tends to deteriorate phase noise.

Table of Contents

List of Tables

List of Figures

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Chapter 1: Introduction

This chapter provides the motivation for the design of a wide-tuning-range 13-GHz LC-VCO. Two methods of implementing wide-tuning-range VCOs are explored and comparison of the two designs is made. The two VCO designs are laid out, and measurements were taken upon receiving the fabricated chip. A simple PFD, charge pump, and loop filter are also designed to simulate a closed-loop PLL using a Verilog-A divider. This chapter defines the objectives of this work and briefly outlines the organization of this thesis.

1.1 Motivation

A phase-locked loop (PLL) is a circuit that causes one system to track another; specifically, it is a circuit that synchronizes an output signal and an input signal in frequency as well as in phase. If a phase error builds up, a control mechanism directs the output signal to minimize the phase error with the input signal. The phase of the output signal is actually locked to the phase of the input signal hence a phase-locked loop. This feature of PLLs proves useful in many applications such as radio, computers, telecommunications and other electronic applications [1]. In this work, the implementation of wide-tuning-range PLLs is studied.

The design of PLLs for communication applications has been greatly impacted by the growing demand for multi-standard and multi-band communication systems. The need for higher data rates and lower power consumption are also crucial. This has been achieved in both wireless and wireline applications through implementing a wider bandwidth PLL with techniques to lower noise, power, and fabrication costs. The design of wider-tuning-range PLLs is also important for lowering costs as a larger tuning range is not limited to one but caters to many applications. Another importance of the study of wide-tuning range PLLs is that it is a practical method in dealing with environmental and process variations.

Being a critical building block of the PLL, the VCO performs essential functions in the transmission of and reception of data. For this work, two designs for implementing wide-tuning-range LC-VCOs are presented. These high-frequency VCO designs belong to

the state-of-the-art and are worthwhile to examine. Also, it is often ideal to design higher frequency VCOs and then lower its frequency through the use of a divider in the closed-loop PLL, as higher frequency LC-VCOs are implemented with smaller inductors which occupy smaller area. As a proof of concept, two different 13-GHz VCOs were designed. The VCOs were laid out and fabricated in a 90-nm CMOS technology, and their performance was evaluated by measurements.

1.2 Objectives

The objectives of this work are as follows:

- Investigate the design of a wide-tuning-range LC-VCO with low phase noise and power dissipation.
- Design two wide-tuning-range LC-VCOs with center frequency of approximately 13 GHz using two different approaches and compare their performance.
- Layout, fabricate, and test the designed circuit blocks of the 13-GHz VCOs.

A closed-loop PLL with a simple charge pump, PFD, and loop filter along with a Verilog-A divider were also designed and simulated.

1.3 Outline

The remainder of this thesis is organized as follows. The next chapter provides a review of PLLs based on LC-VCOs. Chapter 3 discusses the theory and design techniques for the particular 13-GHz LC-VCOs implemented. Chapter 4 presents and discusses the simulation results of the LC-VCOs. Chapter 5 details the measurement approach of the fabricated VCO and compares these measurements with simulation results as well as to other's work. Chapter 6 presents the design of a simple charge pump, PFD, and loop filter, and with a Verilog-A divider simulates a closed-loop PLL. Finally, Chapter 7 concludes the thesis and discusses future work.

Chapter 2: Phase-Locked Loops

This chapter introduces PLLs and the circuit blocks they comprise of. It discusses the basic operation of the PLL. Ring Oscillators and LC-VCOs are discussed and reason is given for implementing the LC-VCO for this work. Other's work on the LC-VCO is considered as a brief literature review on it is provided. This chapter also examines wide-band LC-VCOs in particular. Finally, this chapter provides a discussion of the phase noise of LC-VCOs, which is an extremely important characteristic of any VCO and thus a significant factor when designing PLLs.

2.1 Introduction to PLLs

A PLL is a closed-loop feedback system whose output tracks or synchronizes to the input signal in frequency and in phase [2]. In the synchronized, or locked, state the phase error between the oscillator's output signal and the reference signal is zero or extremely small [2]. This property of PLLs has resulted in their wide popularity in many applications. The main reason for this popularity is probably the versatility of PLLs [3]. The first PLL was introduced in 1932 and today, decades later, there are still many people researching this circuit [3].

2.1.1 Blocks of a PLL

A PLL consists of four basic components: a phase frequency detector (PFD), a charge pump (CP), a loop filter (LP), a voltage-controlled oscillator (VCO), and optionally a frequency divider (÷M), as shown in Figure 2.1 below.

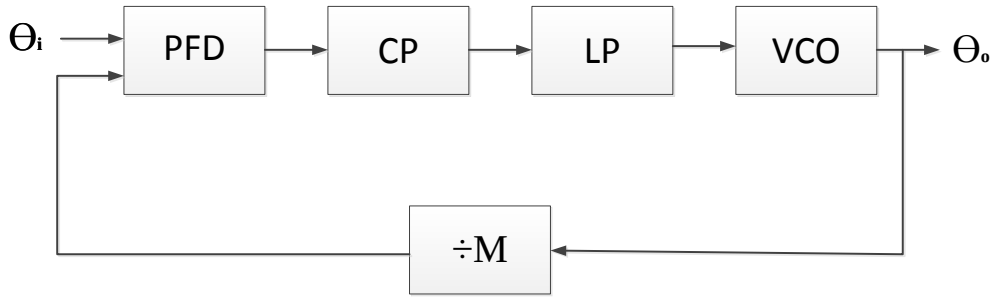


Figure 2.1 Components of a basic Phase-locked Loop

The PFD detects the difference in phase and frequency between the reference clock and feedback clock inputs and generates an "Up" or "Dn" control signal based on whether the feedback frequency is lagging or leading the reference frequency. These "Up" or "Dn" control signals determine whether the VCO needs to operate at a higher or lower frequency, respectively. The PFD outputs these "Up" and "Dn" signals to the charge pump. If the charge pump receives an "Up" signal, current is driven into the loop filter. Conversely, if it receives a "Dn" signal, current is drawn from the loop filter. The loop filter then converts these signals to a control voltage that is used to control the VCO. Based on the control voltage, the VCO oscillates at a higher or lower frequency, which affects the phase and frequency of the feedback clock. If the PFD produces an "Up" signal, then the VCO frequency increases; a "Dn" signal decreases the VCO frequency. The VCO stabilizes once the reference clock and the feedback clock have the same phase and frequency. When the reference clock and the feedback clock are aligned, the PLL is considered locked. The main function of the loop filter is to filter out the phase noise by removing glitches from the charge pump. Finally, a divider may be inserted in the feedback loop to increase the VCO frequency above the input reference frequency [2]. The VCO is the heart of the PLL; thus, the next section is devoted to introducing the options of the types of VCOs one may choose to implement for a PLL. The design of the implemented VCO will be discussed in depth in Chapter 3.

2.1.2 Types of VCOs

The oscillator in a PLL is the most significant block and operates at the highest frequency. The most important specifications of the oscillator are the phase noise, the tuning range, the power consumption, and the cost [1]. Oscillators are generally classified as two types: relaxation oscillators and harmonic oscillators. Relaxation oscillators produce a non-sinusoidal output waveform, such as square or triangular waves, whereas harmonic oscillators have a sinusoidal output waveform. Examples of the relaxation oscillator include the multivibrator and the rotary travelling wave oscillator, but the most common one is the ring oscillator. Examples of the harmonic oscillator include the Hartley oscillator and the

Colpitts oscillator, but the LC-oscillator or the LC-VCO (LC voltage-controlled oscillator) is by far the most popular [4].

The ring oscillator is a commonly used oscillator for integrated PLLs and clock recovery circuits because it is less complex and easy to integrate. It is implemented by cascading a series of odd number of inverters. The ring oscillator provides a wider tuning range compared to a monolithic implementation of an LC-VCO [5]. However, a major drawback of the ring oscillator is that its phase noise is inferior, which impedes its use in high-quality communication systems. This is the reason the LC-VCO is chosen for our application; LC-VCOs exhibit a much better phase noise compared to ring oscillators. The output frequency of the LC-oscillator is determined by the resonance of an inductor and a capacitor. Because both of these elements constitute a passive filter, the phase noise is low [1]. The phase noise of LC-oscillators is typically 20 dB better than that of the ring oscillator [1].

2.2 LC-VCOs

LC-VCOs are superior to other oscillators in the sense that they have good phase noise performance, which is a critical criteria when designing oscillators, and relative ease of design [6]. Due to advantages such as these they are commonly used and have been studied extensively.

2.2.1 Literature Review

LC-VCOs exist in a wide variety of structures, including those with a tail current source, without a tail current source, NMOS-only, PMOS-only, and complementary (both NMOS and PMOS) [7]. Figure 2.2 shows two common structures. Figure 2.2(a) shows a NMOS-only architecture with a tail current source, where V_{bias} is the bias current control for providing a constant tail current in the LC resonator. Figure 2.2(b) shows a complementary architecture with a tail current source.

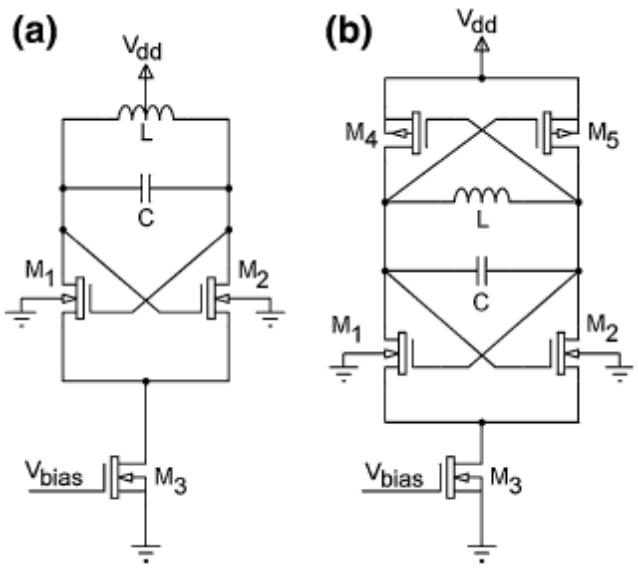


Figure 2.2 LC-VCO structures with a tail current source: (a) NMOS-only (b) complementary [6]

In Figure 2.2(a), an NMOS cross-coupled differential pair (transistors M_1 and M_2) is used to sustain a negative impedance of $(-2/g_m)$ for constant oscillation. It is important to choose the g_m value carefully [8]. Figure 2.3 shows just the NMOS cross-coupled transistors. In Figure 2.3, g_{m1} and g_{m2} are the transconductances of the transistors M_1 and M_2 respectively, and the following relationship holds true [9]:

$$i_{in} = g_{m1}v_{gs1} = -g_{m2}v_{gs2} \tag{2.1}$$

$$\therefore\ R_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{gs2}-v_{gs1}}{i_{in}} = \frac{-1}{g_{m2}} - \frac{1}{g_{m1}} = \frac{-2}{g_m} \tag{2.2}$$

Therefore, to start and keep the oscillation, a negative resistance –R whose magnitude is $2/g_m$ must be present [10]. This will be further discussed in Chapter 3.

The tail current of both the NMOS-only and complementary LC-VCOs in Figure 2.2 flows to the LC-tank and the LC resonator limits the voltage swing across the resonator; this deteriorates the VCO's phase noise. In some cases such as in [11], it has been reported that it may be advantageous to eliminate the tail current source to achieve better phase noise performance. However, the current source has the benefit of supplying a constant current to the cross-coupled differential pair of the LC-tank, making it less sensitive to voltage supply

variations [3]. In general, the tail current aids the designer in achieving a compromise between phase noise performance and power dissipation.

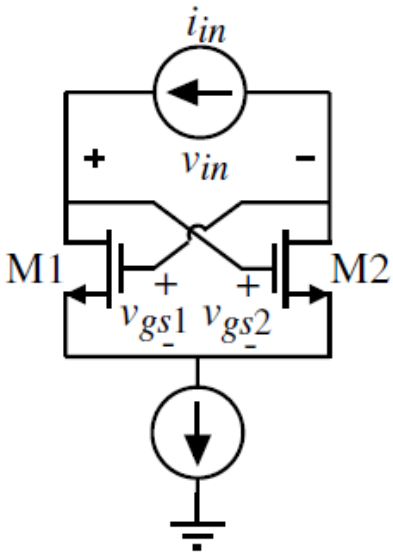


Figure 2.3 NMOS cross-coupled transistors in the configuration to implement a negative resistance [9]

The complementary LC-VCO shown in Figure 2.2(b) is composed of PMOS (M_4 and M_5) and NMOS (M_1 and M_2) transistors stacked in parallel. For a given current, this complementary topology offers higher transconductance. This topology is also symmetrical, which results in faster switching of the cross-coupled pair. Another advantage of using the complementary topology is that it has better phase noise performance [12]. Finally, this structure limits all gate voltages to the supply voltage; this allows for reliable operation within process limits over an extended period of time, such as many years [13]. The main disadvantage to using this configuration is the difficulty in implementing it when the supply voltage is low due to the stacking of transistors. To solve this problem, the tail current source is sometimes removed, such as in [14], thus leaving more voltage headroom for the active devices to operate in the saturation region.

A PMOS-only topology is not shown here but is also used. However, the amplitude for PMOS is smaller and therefore the phase noise worse [1]. Also, since the mobility of holes (μ_p) is lower than that of electrons, PMOS devices have to be twice the size of NMOS devices to achieve a similar performance [15]. Both PMOS- and NMOS-only topologies can provide an output voltage swing greater than the voltage supply with the help of a high tail-

current feed-through. However, the disadvantage to using them is that they also both have worse reliability and power efficiency [16].

2.2.2 Wide-tuning-range LC-VCOs

This thesis focuses on the design of a wide-tuning-range VCO; therefore, it is important to give an overview of the techniques that are commonly used to acquire this wide tuning range. First of all, there are a few design factors that affect the tuning range of all LC-VCOs regardless of what specific technique is employed for wide tuning range; this includes the size of the transistors and the parasitic capacitance of the capacitor and the inductor in the LC-tank. The parasitic parameters of the LC-tank limit the upper frequency band by restricting the upper tuning range [7].

The general problem with LC-VCO design is the tradeoff between the tuning range, phase noise, and power consumption. A typical wide-tuning-range LC-VCO employs the use of a switched capacitor network for coarse tuning and a varactor for fine tuning, such as in [17,18]. As reported in [19], the capacitor network can be made of varactors that can be switched on and off. Another approach for wide-tuning range is to use multiple VCOs with overlapping tuning ranges to cover the entire bandwidth, as in [20]. Alternatively, a wide-tuning-range VCO can be implemented by using switched inductors as in [21] . In general, a mixture of the above techniques is adopted to obtain the desired wide tuning range, which is suitable for the particular technology and design requirements.

2.2.3 Phase Noise of LC-VCOs

Phase noise is a measure of the spectral purity of a signal [1] and is noise that causes variations in the phase of the signal as opposed to fluctuations in the amplitude of a signal [22]. It is an important characteristic of any VCO and thus an important performance metric of PLLs. Phase noise is characterized in the frequency domain and is a key indicator of an oscillator's frequency stability. Phase noise can also be defined as follows:

$$PN = \frac{P_o}{N_o} \tag{2.3}$$

where P_o is the power in the tone at the frequency of oscillation and N_o is the noise power spectral density at some specified offset from the carrier [22]. The main component of oscillator phase noise results from the direct upconversion of white noise and flicker noise (also known as 1/f noise).

Flicker noise is also one of the two main fundamental noise mechanisms for CMOS. The other noise mechanism is thermal noise which is due to the thermal excitation of charge carriers in a conductor. My phase noise simulations indicated the dominance of flicker noise, although thermal noise did occur at times. Flicker noise is a significant noise source in MOS transistors. Flicker noise $V_g^2(f)$ is defined as follows [23]:

$$V_g^2(f) = \frac{K}{WLC_{oxf}} \tag{2.4}$$

where the constant K is dependent on device characteristics and can vary widely for different devices in the same process. The variables W, L, and C_{ox} represent the transistor's width, length, and gate capacitance per unit area, respectively. f is the offset frequency from the center frequency. It is important to note that flicker noise is inversely proportional to the transistor area WL; thus, larger devices have less flicker noise [23].

CMOS transistors generate more flicker noise in comparison to bipolar transistors, which in oscillators is upconverted to $1/f^3$ shaped phase noise close to the carrier. Thus, the $1/f^3$ shaped phase noise is higher in CMOS oscillators and can become an issue. Flicker noise upconversion determines the phase noise at small offset frequencies, where it is suppressed when the oscillator is used in a PLL [1]. It is important to note that flicker noise has large low frequency content [23].

The output of an ideal oscillator is a perfect sinusoidal wave of frequency ω_o, which can be expressed as:

$$\boldsymbol{V_{out}(t) = A \cdot sin(\omega_o t + \theta)} \tag{2.5}$$

where A is the amplitude and θ is a fixed phase reference. In the frequency domain this corresponds to a Dirac impulse at ω_o, $\delta(\omega_o)$. However, with a real oscillator, noise generates fluctuation on the phase and amplitude of the signal, so the output becomes:

$$\boldsymbol{V_{out}(t) = (1 + a(t)) \cdot sin(\omega_o t + \theta(t))} \tag{2.6}$$

Because of the fluctuations on the phase θ(t) and amplitude a(t), the output spectrum is no longer a Dirac impulse, but has sidebands close to the frequency of oscillation, as shown in Figure 2.4. Well-designed, high-quality oscillators are normally very amplitude stable, so a(t) can be considered constant over time. In order to quantify phase noise, the noise power in a unit bandwidth at a certain offset frequency Δω from ω_o is considered and divided by the

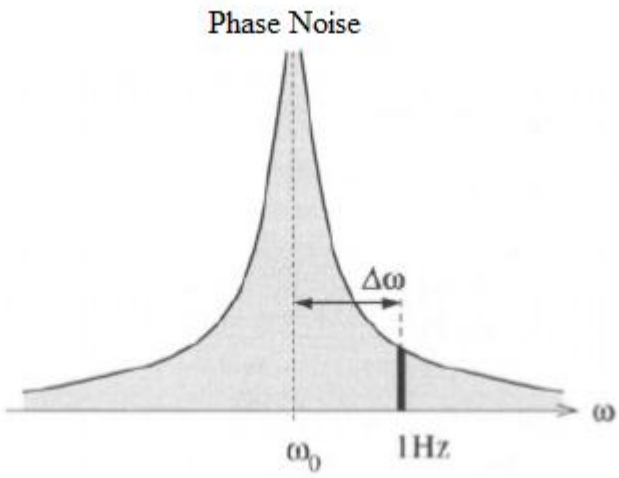


Figure 2.4 The frequency representation of phase noise in an oscillator [1]

carrier power at ω_o. The result is a single sided spectral noise density with units of decibels below the carrier per hertz (dBc/Hz) and is defined as [1]:

$$\mathcal{L}\{\Delta\omega\} = \boldsymbol{10log}\left(\frac{\boldsymbol{noise\ power\ in\ a\ 1\ Hz\ band\ at\ \omega_o+\Delta\omega}}{\boldsymbol{carrier\ power}}\right) \tag{2.7}$$

Figure 2.5 shows the representation of single sideband phase noise.

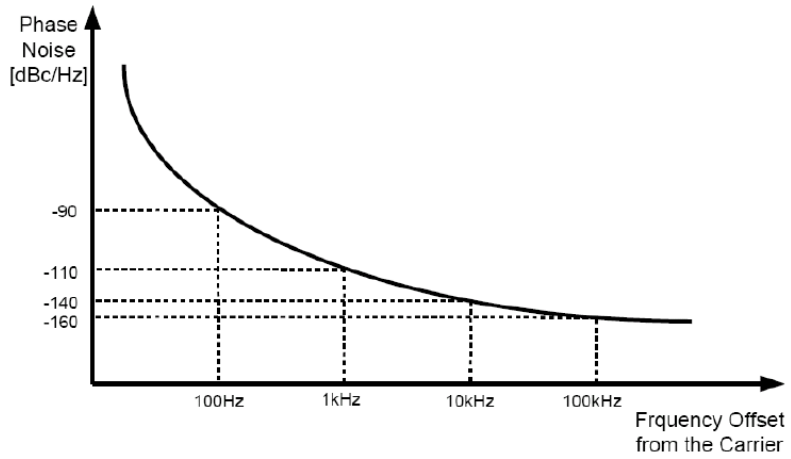


Figure 2.5 Single sideband phase noise representation [24]

Various models have been developed to describe the behavior of phase noise in oscillators. One of the most important models is Leeson's model for oscillator single sideband phase noise, introduced by David B. Leeson in 1966. Leeson proposed the following model [25]:

$$\mathcal{L}\{\Delta\omega\} = \mathbf{10}\,\boldsymbol{log}\left[\frac{\mathbf{2FkT}}{\boldsymbol{P_s}}\cdot\left[\mathbf{1}+\left(\frac{\omega_o}{\mathbf{2}Q_L\,\Delta\omega}\right)^{\mathbf{2}}\right]\cdot\left(\mathbf{1}+\frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{2.8}$$

where $\mathcal{L}$ is the single sideband phase noise density

F is an empirical parameter (often called the "device excess noise number")

P_s is the average power dissipated in the resistive part of the tank

k is Boltzmann's constant, 1.38 x 10^{-23} [J/K]

T is the absolute temperature [K]

ω_o is the oscillation frequency

Q_L is loaded-Q (the effective quality factor of the tank with all loadings accounted for)

$\Delta\omega$ is the frequency offset from the carrier

ω_{1/f^3} is the frequency of the corner between the $1/f^3$ and $1/f^2$ regions as shown in Figure 2.6.

Leeson's model suggests that increasing Q_L, the quality factor of the tank, and signal power reduce phase noise. Additionally, Leeson's model introduces the factor F; it is important to realize that the factor F is an empirical fitting parameter and therefore must be determined

from measurements. This weakens the ability of Leeson's equation to predict the true phase noise. Without knowing exactly what the factor F depends on, it is difficult to identify specific methods of reducing it. Blind application of this model based on pure observation of the equation has resulted in foolish attempts of some designers to use active circuits in order to boost Q_L. Unfortunately, increasing Q_L through this method results in increasing F as well since active devices contribute their own noise; thus, the anticipated phase noise improvements are unsuccessful [26].

Plotting phase noise $\mathcal{L}\{\Delta\omega\}$ for an oscillator (in dBc/Hz) as a function of $\Delta\omega$ on logarithmic scales, regions with different slopes may be observed as shown in Figure 2.6. It is important to note that the curve is approximated by a number of regions, each having a slope of $1/f^x$. At large offset frequencies there is a flat noise floor, and at small offsets there are regions with slopes of $1/f^3$ and $1/f^2$. At very small offset frequencies the spectrum becomes flat again [25].

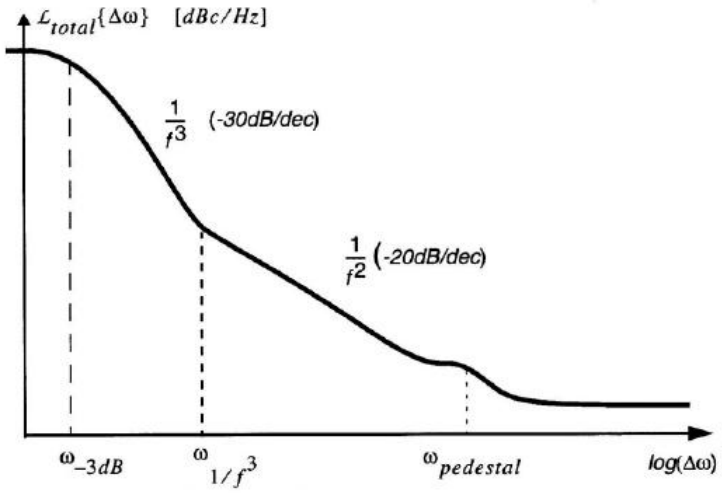


Figure 2.6 The spectrum of the phase noise [25]

Phase noise generated by a VCO is determined by factors such as:

- Q factor of the resonator
- Q factor of the varactor
- Flicker noise
- The active device used for the oscillating transistor

- Power supply noise

The noise contribution made by power supply noise and tuning voltage supply noise can be minimized by choosing carefully the power supplies. Therefore, the phase noise of the VCO is mainly determined by the overall quality factor Q of the circuit [27].

Chapter 3: 13-GHz LC-VCO Design

This chapter discusses the two designs of the 13-GHz LC-VCO. The first one, Design A, is implemented using two VCO cores and the overlapping tuning ranges of the two cores together give overall tuning range. In Design A, a source follower buffer as well as a common-mode logic (CML) buffer are used. The second one, Design B, is implemented using one VCO core and a switched-capacitor. The switched-capacitor can be turned on and off. Design B uses only a CML buffer at the output. Both designs include an on-chip biasing circuitry.

3.1 Design A

This section describes how Design A is implemented. First, steps used to design the LC-VCO cores are discussed. Next, the design of the source follower buffer, common-mode logic stage, as well as the biasing circuitry are examined. Finally, we have a look at the entire VCO with all of these blocks together.

3.1.1 LC-VCO Core

The goal is to achieve an overall tuning range of approximately 30-40 % (calculated as $((f_{max}/f_{min} - 1) * 100\ \%)$. In this design, two VCOs are implemented with an overlapping tuning range. The target center frequency is 13 GHz; however it must initially be designed with a higher center frequency to account for frequency drop after post-layout simulation due to parasitic capacitance. The first VCO was designed to cover the frequency range 15.5 GHz to 20 GHz with a center frequency of 17.75 GHz. The second VCO was designed to cover the frequency range of approximately 12 GHz to 16.5 GHz with a center frequency of 14.25 GHz. Thus, the overall tuning range covered by the two VCOs is 12 GHz to 20 GHz and the center frequency is 16 GHz. The LC-VCO core is designed in the following 4 steps:

Step 1

First of all, it is important to note that the power supply for 90-nm technology is 1.2 V. The design of the VCO starts with the design of the *–Gm* LC-tank, by finding a geometry

that provides a high inductance with the lowest parasitic resistance, while maintaining a sufficient tuning range. The first step is to determine whether complementary (NMOS and PMOS) or xMOS-only (NMOS or PMOS) VCO should be implemented. A complementary VCO, which is commonly used because of its low phase noise characteristics, was not chosen for this design as the power supply is quite low [28]. An NMOS-only LC-tank was implemented, as the speed of NMOS is higher than PMOS. A PMOS current source which has better phase noise performance with reduced flicker noise was used [1]. Figure 3.1 shows the schematic of the LC-VCO core implemented.

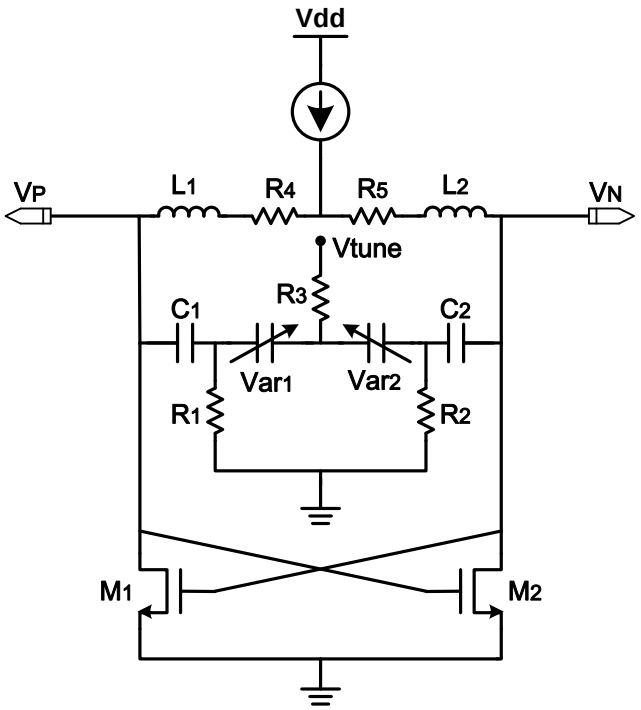


Figure 3.1 Schematic of LC-VCO core implemented

Referring to Figure 3.1, inductors L_1 and L_2 are ideal inductors; the resistors in series with the inductors R_4 and R_5 are the resistances of the inductors. This model of the real inductor is a very simplified model and does not take into consideration the parasitic capacitance and resistance of the inductor but is sufficient for our purposes. To avoid positive bias of varactors Var_1 and Var_2, capacitors C_1 and C_2, and resistors R_1 and R_2 directly bias the varactors to ground avoiding the complex bias circuits [29]. Resistors R_1, R_2 and R_3 shown in Figure 3.1 are for biasing purpose; they are not parasitic resistors.

Adjusting the capacitor and varactor ratio is key to changing or maximizing the tuning range as desired.

Step 2

After determining the geometry of the VCO, the next step is to do initial hand calculations to find the values for the resistors and the varactors of VCO 1 with center frequency 17.75 GHz:

Assuming L = 0.5 nH,

The resonant frequency can be expressed as [30]:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

$$\omega = \frac{1}{\sqrt{LC}}$$

$$C = \frac{1}{\omega^2 L} \approx 160fF$$

$$160fF * 4 = 640fF\ each$$

Refer to Figure 3.2. Let x be the value of the varactor. Assume the value of the capacitor is 600fF (Note: this value will be adjusted during simulation and debugging).

$$\frac{1}{x} + \frac{1}{x} + \frac{1}{600fF} + \frac{1}{600fF} = \frac{1}{160fF} \tag{3.2}$$

$$x \approx 686fF$$

Assuming the inductor's Q factor is 10, which is the worst case scenario, the series resistance Rs (which is equivalent to R_4 and R_5 in Figure 3.1) is [9]:

$$R_S = \frac{\omega L}{Q} = 1.775\pi \approx 5.58\Omega \tag{3.3}$$

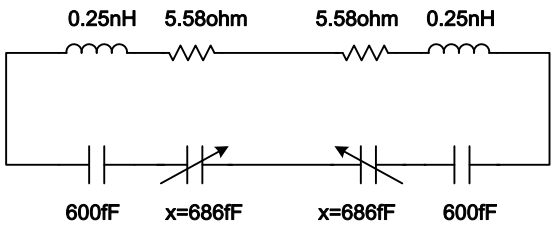


Figure 3.2 Calculated values of the resistors and varactors

Step 3

The next step is to determine the value of $\mu_n C_{ox}$ or K_n. This can be estimated by two different methods. The first method is to use the value of t_{ox} to first calculate $C_{ox.}$ t_{ox} for NMOS is found to be $2.83 * 10^{-9}$ m from the TSMC 90-nmlp model file. Thus from [23],

$$K_n = \mu_n C_{ox} = \mu_n * \frac{K_{ox}\varepsilon_0}{t_{ox}} \tag{3.4}$$

The second method is to perform DC analysis of a transistor and plot its I_{DS} *vs.* V_{GS} curve. By extending the linear portion of this curve to the x-axis, the point where it crosses the x-axis is the approximation of V_{TH}. Using this value of V_{TH} and the coordinates of any point on the I_{DS} vs. V_{GS} curve the value of K_n can be approximated by the squared current-voltage relationship for a MOS transistor in the active region:

$$I_D = \frac{1}{2} K_n \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2 \tag{3.5}$$

The second method should give a closer approximation and is one of the more popular techniques to estimate K_n. The first method particularly will not result in a correct K_n value especially for advanced technology like TSMC 90-nm, because square-law equations are not valid for short-channel transistors. Both of these methods to approximate K_n only provide a general guideline for reference only.

Step 4

Using the K_n value obtained in the previous step, the (W/L) ratio for M_1 and M_2 can be calculated as follows:

According to [9], converting the series impedance of 2L and $2R_s$ into a parallel impedance gives,

$$Y = \frac{1}{2R_s + j\omega 2L} = \frac{0.5}{R_s + j\omega L} * \frac{R_s - j\omega L}{R_s - j\omega L} = \frac{0.5R_s}{R_s^2 + \omega^2 L^2} - j\frac{0.5\omega L}{R_s^2 + \omega^2 L^2} \quad (3.6)$$

The reciprocal of the conductance is the parallel resistance $R_{p,}$ given as

$$R_p = \frac{R_s^2 + \omega^2 L^2}{0.5R_s} \quad (3.7)$$

In order to provide sustained oscillation, a feedback loop is introduced which acts to generate a negative resistance –R, which is shown conceptually in Figure 3.3.

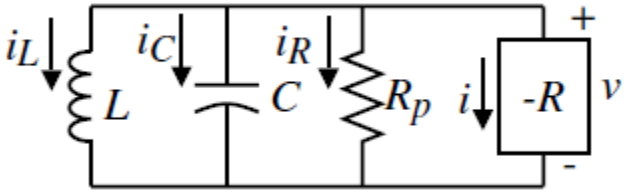


Figure 3.3 Basic RLC oscillator and negative resistance circuit [9]

$$R = -R_p \quad (3.8)$$

From [9], we know that

$$R = -\frac{2}{g_m} \quad (3.9)$$

$$\therefore g_m = -\frac{2}{R} \quad (3.10)$$

Also from [9],

$$V = \frac{2}{\pi} I_{bias} R_p \quad (3.11)$$

We select V to be 1.3V (Note that the output of the NMOS-only topology VCO could be larger than the supply voltage of 1.2V to get better performance [9]). Therefore, the current through each transistor is half of I_{bias}.

Finally, using the following equation from [23], the (W/L) ratio for M_1 and M_2 can be approximated:

$$g_m = \sqrt{2K_n I_D \frac{W}{L}} \tag{3.12}$$

$$\left(\frac{W}{L}\right) = \frac{g_m^2}{2K_n I_D} \tag{3.13}$$

The above four steps were repeated for designing VCO 2 with center frequency 14.25 GHz. For both of these VCO cores these steps are implemented initially to give an estimate of magnitude of components to use; based on these values simulations are performed and sufficient adjustments are made as required.

Figure 3.4 shows the specific LC-tank implemented with design parameters for VCO 1 and VCO 2. As can be seen the design parameter values are different from what was calculated. This is due to the fact that using the calculated parameters, simulation results showed quite a large drop in frequency than what was designed for due to the significant effect of parasitic capacitance at such high frequency. Sufficient adjustments were thus made, resulting in the implemented designs shown in Figure 3.4.

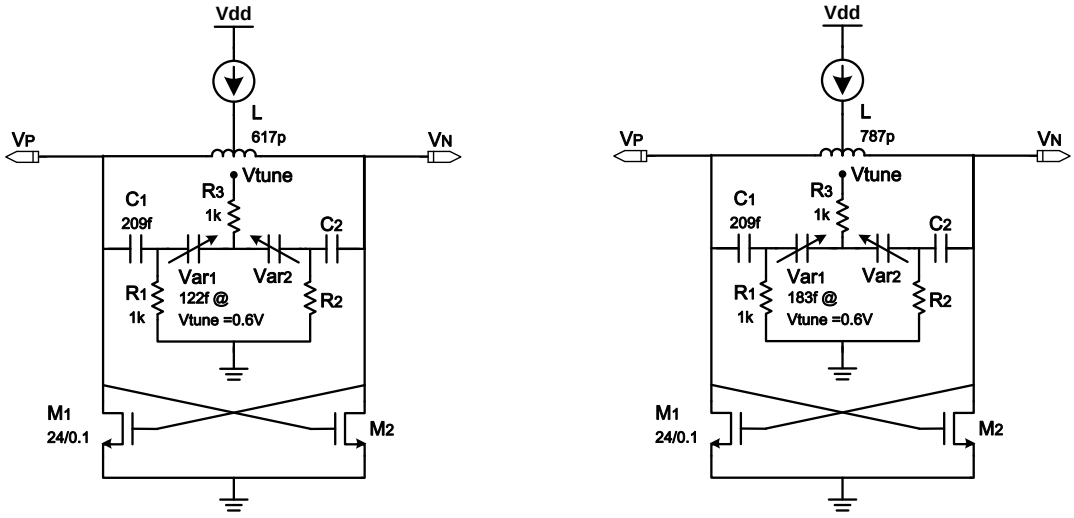


Figure 3.4 LC-VCO schematic with design parameters for a) VCO 1, b) VCO 2

For example, in Figure 3.4 a), using the values of the components indicated in the implemented schematic to calculate the center frequency of VCO 1, the equivalent capacitance is first calculated as:

$$\frac{1}{\frac{1}{209fF}+\frac{1}{209fF}+\frac{1}{122fF}+\frac{1}{122fF}} = 38.52fF \tag{3.14}$$

Thus, the center frequency of VCO 1 is calculated to be:

$$f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(617pH)(38.52fF)}} = 32.65GHz \tag{3.15}$$

This is quite a bit higher than the desired center frequency of 17.75 GHz for VCO 1. Therefore, one can assume that the cross-coupled NMOS capacitors of the LC-tank has significant parasitic capacitance which lowers the center frequency of the VCO.

In general, the capacitance of the varactors is made small compared to the capacitance of the capacitors so the varactors have a larger effect on the total capacitance, which consists of two capacitors and two varactors in series, allowing for a larger frequency range. The varactor cannot be too small as it will result in abnormal behavior of the varactor. As the capacitor to varactor ratio increases, the tuning range of the VCO increases. However, the capacitor to varactor ratio cannot be too large, as simulation indicates that as the ratio increases to a certain degree abnormalities occur. Sufficient adjustments are made to obtain the desired tuning range covered after many simulations. Figure 3.5 shows the Varactor Capacitance vs. V_{tune} for VCO tank 1. At V_{tune} = 0.6 V, the capacitance of the varactor is 122 fF.

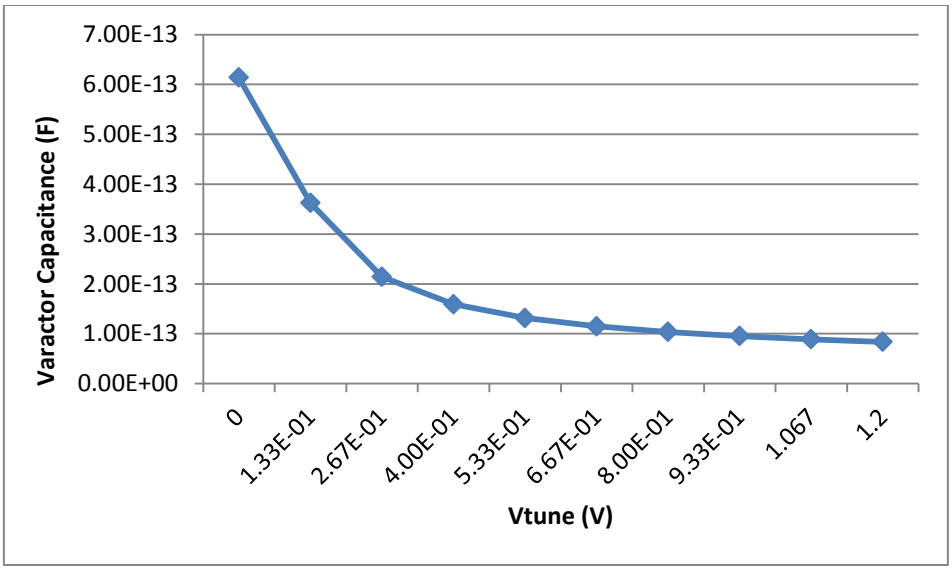


Figure 3.5 Varactor Capacitance vs. Vtune for VCO 1

Figure 3.6 shows the varactor capacitance vs. V_{tune} for VCO tank 2. At V_{tune} = 0.6 V, the capacitance of the varactor is 183 fF.

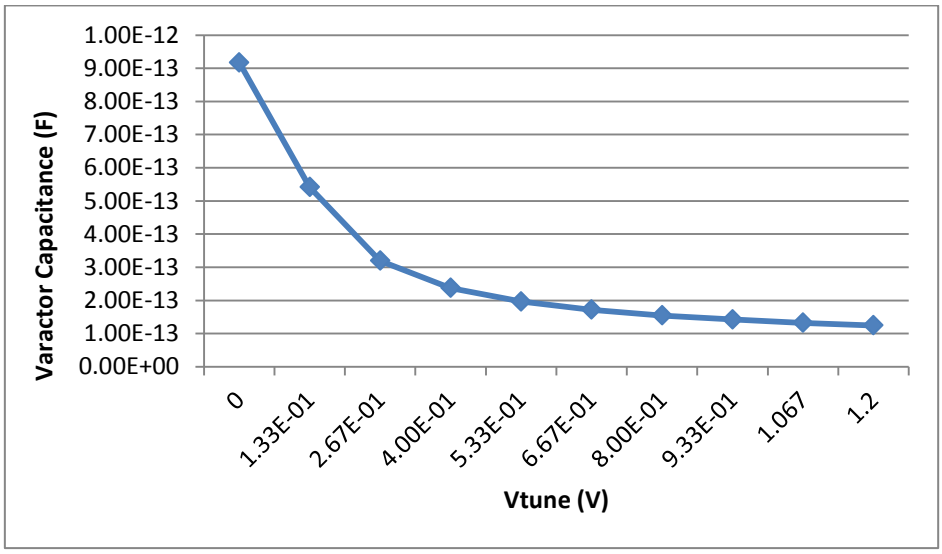


Figure 3.6 Varactor Capacitance vs. V_{tune} for VCO 2

The Q factor of the inductor is found through simulation by the following formula [22]:

$$Q = \frac{|Im(Z_{ind})|}{|Re(Z_{ind})|} \tag{3.16}$$

where Z_{ind} is the impedance of the inductor. For both VCO 1 and VCO 2, the Q factor of their inductor is approximately 12, which is a typical value. In general, the value of the inductor is chosen to be as large as possible for better performance [1]; however, it cannot be too large as a smaller value would result in a larger tuning range since by

$$\omega = \frac{1}{\sqrt{LC}} \tag{3.17}$$

for a fixed ω a smaller L allows for a larger C and thus larger variation in C.

The aspect ratio of the cross-coupled NMOS transistor of the VCO cores varied quite a bit from the calculated value which provided a guideline. This was to be expected since the large effect of the parasitic capacitances present must be considered, especially when the frequency is high. The specific aspect ratio value implemented resulted from satisfaction of the $V_{DS} > (V_{GS} - V_{TH})$ criteria of the transistor during simulation [31].

3.1.2 Source Follower Buffer

The output of the VCO core is connected to the input of the source follower buffer. The source follower buffer has high input impedance, as is shown in [32], and moderate to low output impedance [33]. Its high input impedance means the output load of the VCO core is small so that the VCO can function at a higher frequency. Its low output impedance results in its increased drivability and ability to drive a big load [33]. Also, a source follower is required to connect to the output of the VCO core to isolate the VCO from outside blocks; this can result in the VCO's frequency to be more stable. However, the drawback of the follower buffer is the voltage headroom limitation [33]. Since for the source follower the source is the output node, the transistor becomes dependent on the body effect. The body effect results in the threshold voltage V_{TH} to increase as the output voltage increases [34]. It is important to note that the voltage gain of the source follower is smaller than one.

Figure 3.7 shows the follower buffer implemented for both VCO 1 and VCO 2 with design parameters. The aspect ratio of M_1 and M_2 was designed to guarantee that the VCO would work well, at the desired frequency. The resistors R_1 and R_2 were designed to be as

large as possible but under the condition that transistors M_1 and M_2 were working well, satisfying $V_{DS} > V_{DSAT}$.

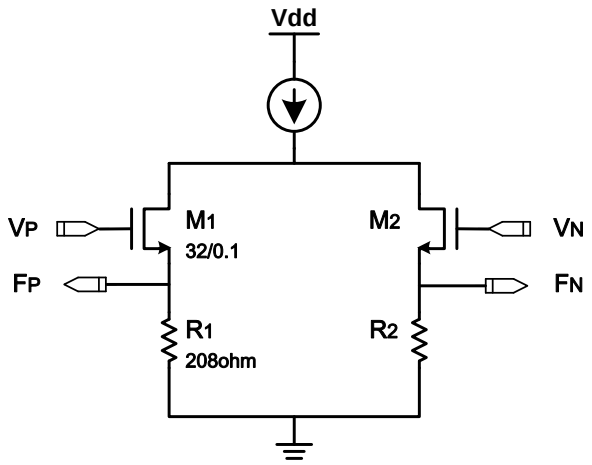


Figure 3.7 Source follower buffer with design parameters

3.1.3 CML Stage

The common-mode logic (CML) stage is connected to the output of the source follower to improve the drivability of the overall VCO. Another reason the CML stage is ideal for this design is because it is a high-speed logic circuit. This fast operation of CML circuits is mainly due to their lower output voltage swing compared to the static CMOS circuits [35]. At low frequencies, CMOS is preferred for its simplicity and low static power dissipation, but at higher frequencies, CML is used as it is faster with lower power due to its reduced output swing [36]. This is clearly illustrated in Figure 3.8 showing Current vs. Frequency for CMOS and CML.

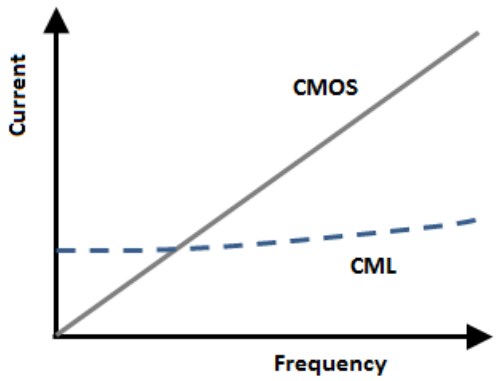


Figure 3.8 Comparison of current vs. frequency for CMOS and CML [36]

The CML stage also functions as a level shifter here depending on the requirements of the next stage's input level, which is required because the output voltage level of the source follower is comparatively low. However, the drawback to using a CML buffer is that it requires a constant static current source; thus, it suffers from dissipating more static power than a CMOS inverter [35]. In general, more current and small R results in higher frequency. This is a trade-off between power and load RC [36].

The implemented design of the CML stage is shown in Figure 3.9. Resistors R_5 and R_6 are pull-up resistors. The logic function is implemented by the logic block connected between the resistors and the current source, which is the differential pair constructed by transistors M_1 and M_2. The operation of the CML buffer is based on the differential pair circuit. Each differential input variable is connected to a differential pair circuit. The value of the input variable controls the flow of current through the two branches [37]. The pull-up resistors were chosen depending on the working frequency and output swing. If the working frequency is increased, the resistance should decrease because they are inversely related. However, the current should increase to ensure sufficient output swing. Conversely, if the working frequency is decreased, the resistance should increase, and the current should decrease to keep the output swing constant. The W and L of transistors M_1 and M_2 were chosen to be as small as possible to reduce the input capacitance and therefore reduce the source follower load, since the input capacitance C_{GS} is proportional to W and L [23] as shown as follows:

$$C_{GS} = \frac{2}{3}WLC_{ox} + WL_{0v}C_{ox} \tag{3.18}$$

However W and L of M_1 and M_2 cannot be too small as the gain of the CML buffer must be taken into consideration as well, since gain of the CML stage is

$$A_v = -g_m R_{5,6} \tag{3.19}$$

and g_m is proportional to the value of W [23] as shown as follows:

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right) V_{eff} \tag{3.20}$$

A crucial part of the design of the CML stage is the AC coupling at its input. This AC coupling block consists of two capacitors and four resistors. As can be seen in Figure 3.9 the values of resistors R_3 and R_4 of the AC coupling are different. These two resistors are for biasing purpose and their values are adjusted accordingly to ensure that M_1 and M_2 are working well to satisfy $V_{DS} > V_{DSAT}$. The values of R_3 and R_4 determine the common-mode level. Resistors R_1 and R_2 must be equal to ensure that the signal is even and has the same amplitude above and below common-mode level. Resistors R_1 and R_2 are designed according to the values of capacitors C_1 and C_2. C_1 and C_2 are designed so their impedance over the frequency range of interest is substantially smaller compared to R_1 and R_2; thus, AC voltage drop across the capacitors is insignificant compared to the voltage drop across the resistors. The AC coupling isolates the DC of the source follower buffer from that of the subsequent blocks.

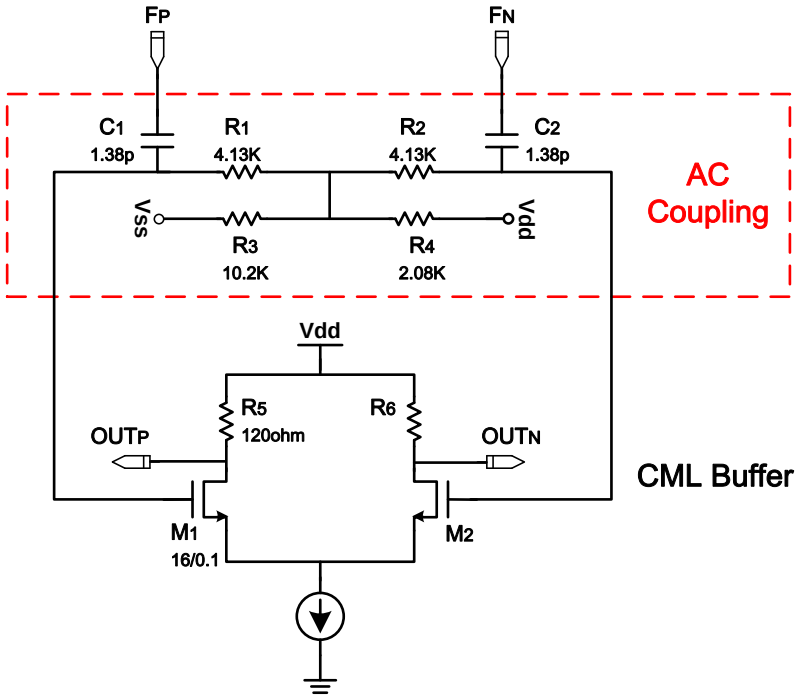


Figure 3.9 Common-mode logic stage with design parameters

3.1.4 Biasing Circuitry

Figure 3.10 shows the schematic with parameters of the constant-g_m with start-up biasing circuit used in the design. The constant-g_m current source consists of transistors M_4, M_2, M_7, and M_8 as well as the resistor R. The startup circuit consists of transistors M_1, M_2, M_3, M_5 and M_6. If all currents in the bias loop are zero, M_2 and M_3 will be off. M_5 and M_6 pull the gate of M_1 high. M_1 will then inject currents into the bias loop, starting up the circuit. Once the loop starts up, M_3 will come on, sinking the current from the cascode M_5 and M_6 and pulling the gate of M_1 low, thus turning it off [23].

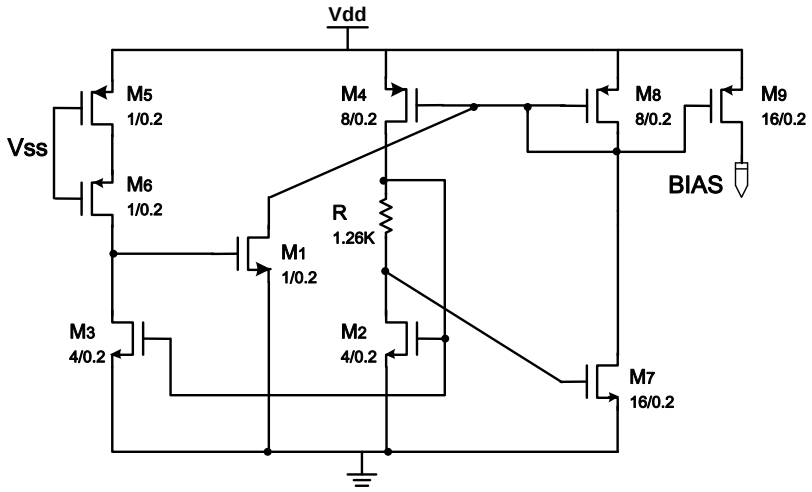


Figure 3.10 Biasing circuitry with design parameters

Figure 3.10 shows that for transistors M_2 and M_7,

$$V_{GS2} = V_{GS7} + I_{D2}R \tag{3.21}$$

Since $V_{effi} = V_{GSi} + V_{TH}$,

$$\therefore V_{eff2} = V_{eff7} + I_{D2}R \tag{3.22}$$

$$\therefore \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} = \sqrt{\frac{2I_{D7}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_7}} + I_{D2}R \tag{3.23}$$

And since $I_{D2} = I_{D7}$,

$$\sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_7}} + I_{D2}R \tag{3.24}$$

$$\frac{2}{\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_2 I_{D2}}}\left[1 - \sqrt{\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_7}}\right] = R \tag{3.25}$$

Recalling that $g_{m2} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_2 I_{D2}}$

$$\therefore g_{m2} = \frac{2\left[1-\sqrt{\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_7}}\right]}{R} \tag{3.26}$$

Therefore, for the special case $\left(\frac{W}{L}\right)_7 = 4\left(\frac{W}{L}\right)_2$, we have $g_{m2} = \frac{1}{R}$.

This is the reason for the name "constant-g_m biasing circuitry." By defining a value for g_{m2}, we can find the suitable value for resistor R [23].

3.1.5 Entire VCO

The overall architecture for this design is depicted in Figure 3.11. The design consists of two VCO cores with overlapping tuning ranges, where only one of the VCO cores (and its source follower buffer) is enabled at a time. Although only two VCOs are used here, in general, one can use more than two VCOs to achieve a wider tuning range. The output of the buffer feeds into a CML stage.

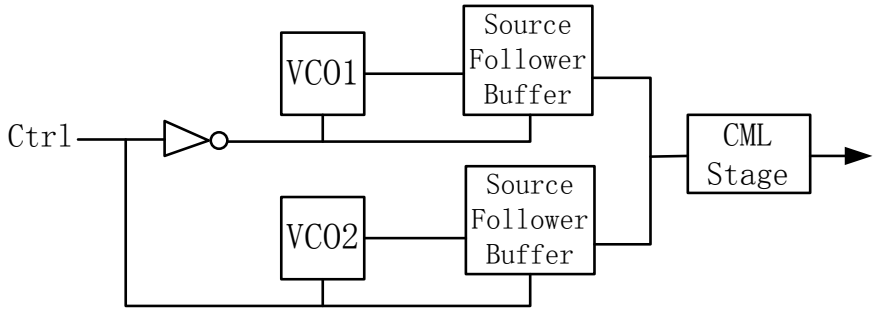


Figure 3.11 Block diagram of Design A architecture

The circuit schematic of one path of this design including the follower buffer and the CML stage is shown in Figure 3.12.

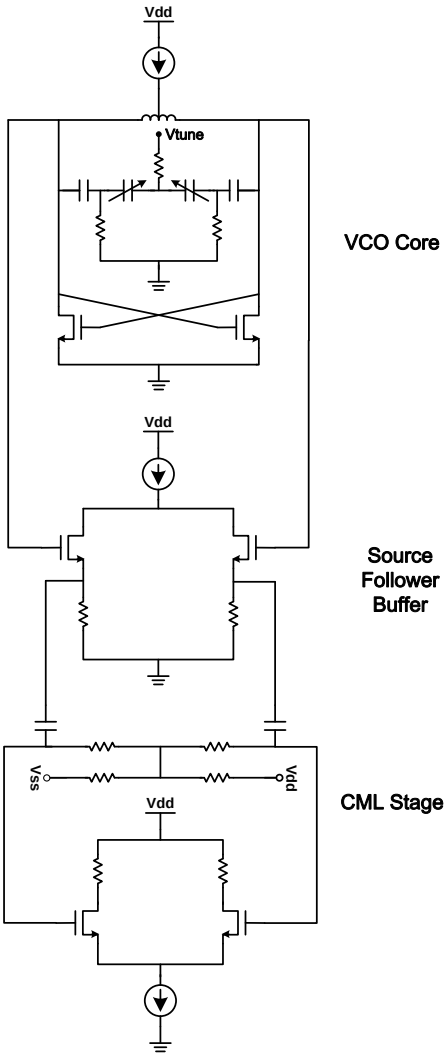


Figure 3.12 Schematic of one path of Design A

3.2 Design B

This section discusses how Design B is implemented. First, the design of the VCO core with the switched capacitor is described. Finally, we have a look at the entire VCO with all circuit blocks together.

3.2.1 LC-VCO Blocks

The initial goal was to achieve an overall tuning range of approximately 30-40 % (calculated as (f_{max}/f_{min} - 1) * 100 %), like for VCO Design A. In this design, one VCO core is implemented with a switched-capacitor. This VCO was designed so that turning the switched-capacitor on and off would result in overlapping tuning range. Initial simulations indicated that the target tuning range was not possible for this design with only one switched-capacitor for a fair comparison, so the goal was altered to maximize tuning range. The target center frequency, like that for Design A, is 13 GHz. The VCO with the switched-capacitor turned off will be designed to cover the frequency range of approximately 14 GHz to 18.5 GHz with a center frequency of 16.25 GHz. The VCO with the switched capacitor turned on will be designed to cover the frequency range of approximately 12.5 GHz to 15.5 GHz with a center frequency of 14 GHz. Thus, the overall tuning range covered is from 12.5 GHz to 18.5 GHz with center frequency 15.5 GHz, which is lower than Design A. Note that the overall tuning range is skewed to allow for frequency drop after post-layout simulation due to parasitic capacitance. The LC-VCO core without the switched-capacitor is identical to VCO 1 in Design A. The tuning range covered when the switched-capacitor is turned off for this design, Design B, is different from the tuning range covered for VCO 1 of Design A partially because the presence of the switched-capacitor introduces extra parasitic capacitance, even when turned off, which lowers the frequency.

The addition of the switched-capacitor provides extra coarse tuning that can be added to the normal fine tuning (ie: the varactors) of the VCO to increase the frequency range. However, the digital logic system that controls the switching of the switched-capacitor must be carefully integrated in the design in order to guarantee stability over the complete tuning range [31]. Also, adding a switched-capacitor to the VCO's LC-tank would in general deteriorate the overall quality factor of the LC-tank and increase the total fixed capacitance of the VCO, which reduces K_{VCO} [31]. The switches must be implemented as MOS transistors, which have series resistance when on, as well as parasitic capacitance to the substrate from their drain and source regions. Therefore, it is expected that the circuit design and layout will have a detrimental influence on the resulting quality factor [31].

Figure 3.13 shows the LC-tank with the switched-capacitor implemented with design parameters.

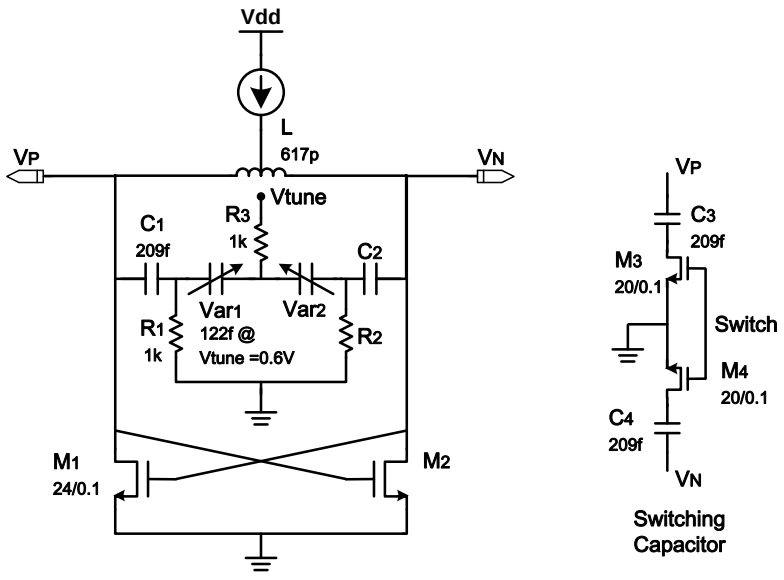


Figure 3.13 LC-VCO with switched-capacitor schematic with design parameters

The switched-capacitor was designed by repeated simulations, meeting the target tuning ranges while ensuring that the $V_{DSAT} < V_{DS}$ for transistors M_3 and M_4. This task was not easy as both switched-capacitor turned off and on had to be considered and sufficient overlapping of tuning range must be guaranteed. The W/L of transistors M3 and M4 should be a relatively large number to minimize their resistance, as resistance is proportional to the inverse of W/L from [23]:

$$R_{total} = R_{\square}\frac{L}{W} \tag{3.27}$$

where $R_{\square}$ is the resistance per square. However, if the transistor size is big, its parasitic capacitor is big as well when the switched-capacitor is off, so considering the trade-off we must debug carefully.

One switched-capacitor is used here to have two modes, for a fair comparison with the two-core Design A. However, it is important to note that in general, an array of switched-capacitors can be used to achieve a larger tuning range. For symmetry, the

switched-capacitor block is implemented using two capacitors and two transistors. The capacitors also act to isolate the switch transistor's DC level from that of the VCO output. The balanced symmetrical design of the switched-capacitor has a common-mode node and allows for better linearity and phase noise performance compared to a switched-capacitor with no common-mode node [31].

The differential outputs of the VCO core V_P and V_N are connected to a CML buffer stage, which is identical to the one described in Design A. Only a CML buffer is implemented with no follower buffer for comparison purposes. Current is supplied to the VCO core and CML stage by a constant-g_m start-up biasing circuitry identical to the one described in Design A.

3.2.2 Entire VCO

The overall architecture for this design is depicted in Figure 3.14. The design consists of one VCO core with a switched-capacitor which can be switched on or off, creating overlapping tuning ranges. The output of the VCO core feeds into a CML stage.

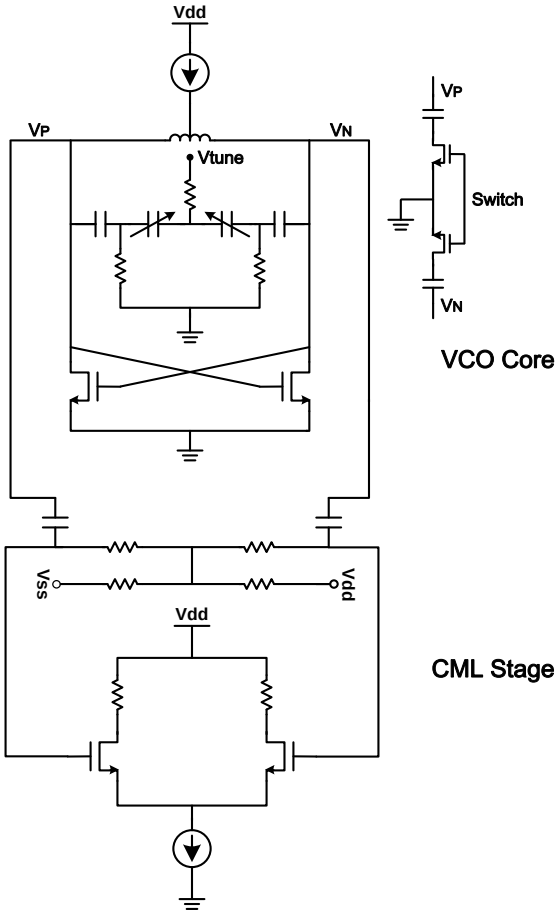


Figure 3.14 Schematic of Design B

It is possible and common to use more switched-capacitors and place them in parallel to the existing switched-capacitor as illustrated in Figure 3.15. Doing so would result in even larger overall tuning range, at the expense of increased phase noise and parasitic capacitance because the Q would be decreased.

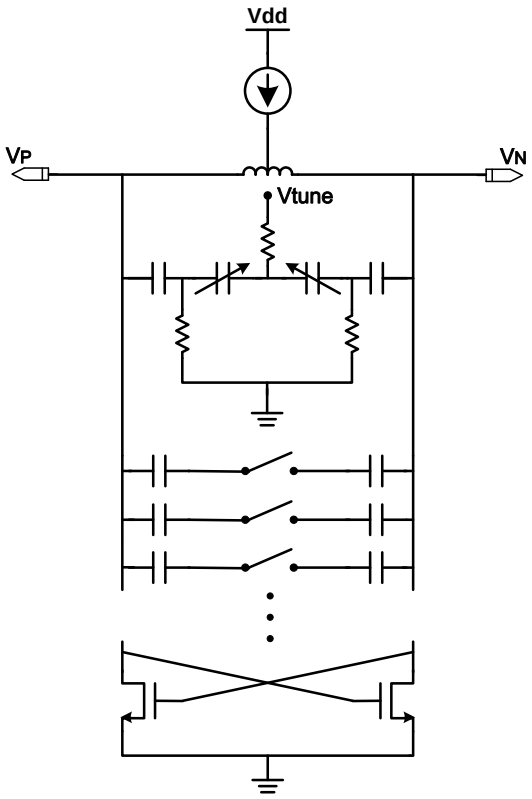


Figure 3.15 Multiple switched-capacitors in parallel

Chapter 4: Simulation Results

This chapter discusses the transient response and amplitude, the tuning range, and finally the phase noise simulation results of the two 13-GHz LC-VCO designs. First, a brief overview of the simulation results without extraction is presented for comparison purposes. Then the post-layout simulation results are discussed.

4.1 13 – GHz VCO Simulation Results

This section presents and briefly discusses the simulated (without extraction) transient response and amplitude, tuning range, and phase noise of the two LC-VCO designs. The purpose of the inclusion of this section is so sufficient comparison can be made to the post-layout simulation results.

4.1.1 Transient Response and Amplitude

For design A, the transient response for the outputs of the VCO core, follower buffer stage, and overall output when VCO 1 is enabled is shown in Figure 4.1. When the oscillation stabilizes the frequency is measured to be approximately 17.24 GHz, which is the center frequency. The differential peak-to-peak amplitude for the VCO core output, source follower buffer stage output, and overall output from the CML stage are 5.42 V, 1.75 V, and 1.09 V respectively.

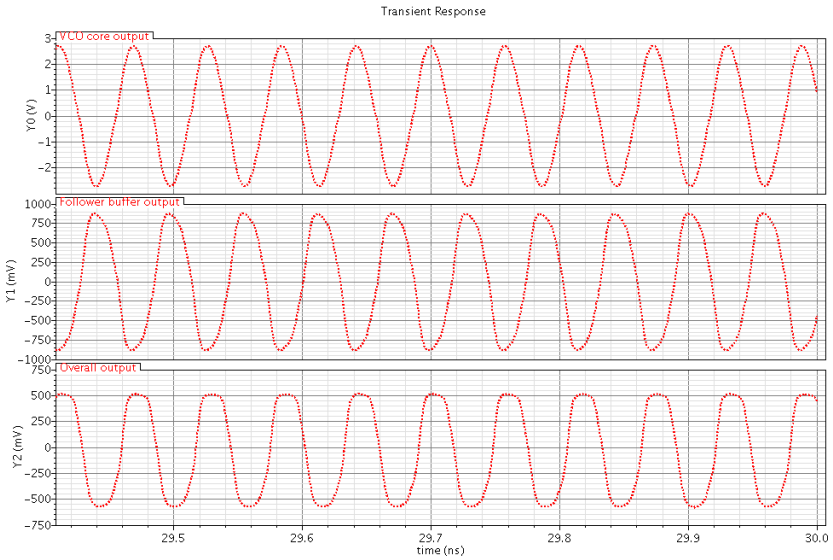


Figure 4.1 Transient response of VCO 1

The transient response for VCO 2 of design A as well as for design B looks similar. Their stabilized frequency and their differential peak-to-peak amplitudes at various stages are summarized in Table 4.1.

Table 4.1 Transient response of Design A and Design B

	Design A			Design B	
	VCO 1	**VCO 2**		**Switched-cap. off**	**Switched-cap. on**
Frequency (GHz)	17.24 GHz	14.08 GHz	**Frequency (GHz)**	15.87 GHz	14.12 GHz
VCO core output amplitude (Vpp)	5.42 V	5.34 V	**VCO core output amplitude (Vpp)**	5.08 V	2.51 V
Source follower buffer stage output amplitude (Vpp)	1.75 V	1.78 V	**OUTP/OUTN (Vpp)**	2.02V	1.82 V
Overall output amplitude from CML stage (Vpp)	1.09 V	1.11 V			

Table 4.1 shows that with the inclusion of the source follower buffer, the overall output amplitude from the CML stage is much lower.

4.1.2 Tuning Range

The overall tuning range covered for both designs is shown in Table 4.2. For Design A, the overall tuning range is obtained by the two overlapping tuning ranges of VCO 1 and

VCO 2. For Design B, the overall tuning range is obtained by the two overlapping tuning ranges obtained when the switched-capacitor is disabled and enabled.

Table 4.2 Tuning range of Design A and Design B

	Design A	Design B
Overall tuning range covered (GHz)	11.11 to 21.31	11.05 to 19.15

4.1.3 Phase Noise

The phase noise for VCO 1 of Design A is shown in Figure 4.2. As indicated, at 1 MHz offset, the phase noise is –89.87 dBc/Hz.

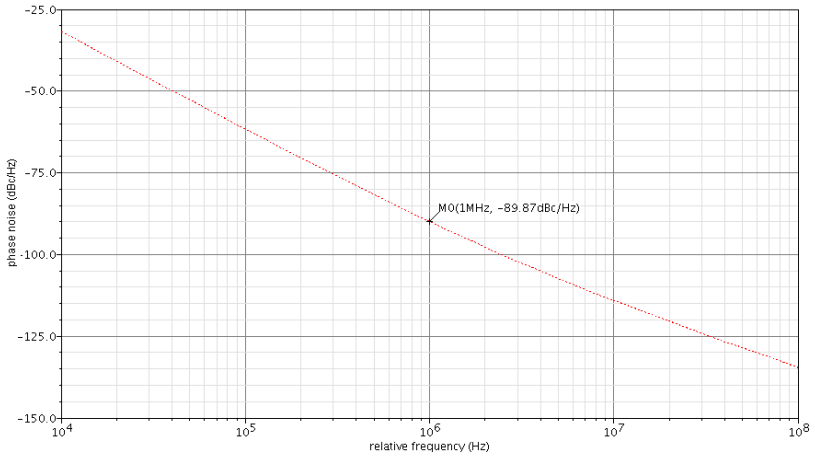


Figure 4.2 Phase noise for VCO 1 of Design A

The phase noise for Design A and Design B at 1 MHz offset is shown in Table 4.3.

Table 4.3 Phase noise at 1 MHz offset for Design A and Design B

	Design A	Design B
Phase Noise in dBc/Hz at 1 MHz	–89.87 dBc/Hz	–90.31 dBc/Hz

4.2 13 – GHz VCO Post-Layout Simulation Results

This section presents and discusses the post-layout simulation results of the transient response and amplitude, tuning range, and phase noise of the two 13-GHz LC-VCO designs. Comparison of these results to simulation results is made, indicating that overall the results match approximately and show the same trend.

4.2.1 Transient Response and Amplitude

For design A, the transient response for the outputs of the VCO core, follower buffer stage, and overall output when VCO 1 is enabled is shown in Figure 4.3.

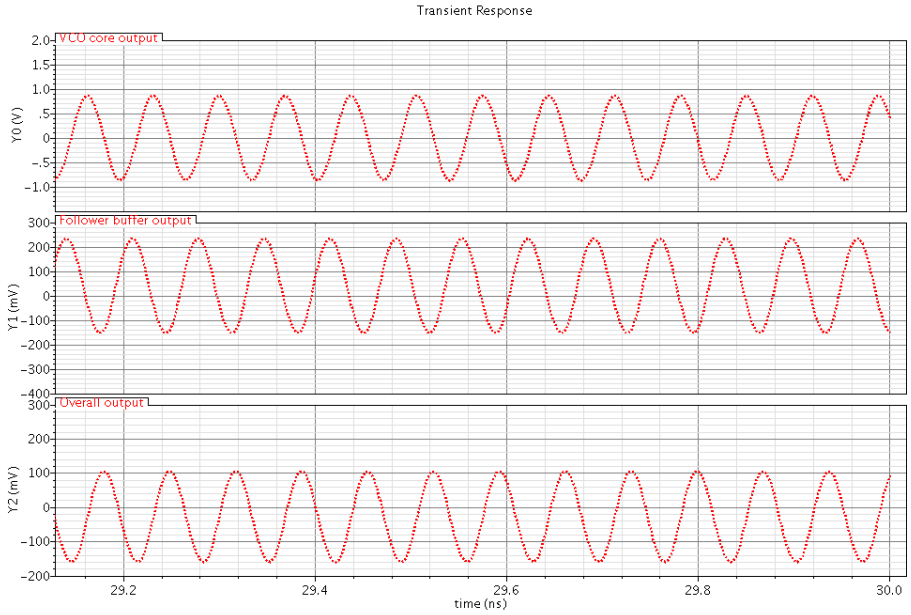


Figure 4.3 Transient response of VCO 1

The frequency when the oscillation stabilizes and the differential peak-to-peak amplitudes for the two designs at various stages are shown in Table 4.4.

Table 4.4 Transient response of Design A and Design B

	Design A			Design B	
	VCO 1	**VCO 2**		**Switched-cap. off**	**Switched-cap. on**
Frequency (GHz)	14.49 GHz	11.76 GHz	**Frequency (GHz)**	12.99 GHz	11.49 GHz
VCO core output amplitude (Vpp)	1.72 V	1.93 V	**VCO core output amplitude (Vpp)**	1.64 V	1.53 V
Source follower buffer stage output amplitude (Vpp)	384.95 mV	497.40 mV	**OUTP/OUTN (Vpp)**	1.29 V	1.22 V
Overall output amplitude from CML stage (Vpp)	264.10 mV	345.70 mV			

Post-layout simulation results of the transient response match the simulation results in that Design A which uses a source follower buffer has a much lower overall output amplitude from the CML stage.

4.2.2 Tuning Range

The overall tuning range obtained for both Design A and Design B are shown in Table 4.5. Corner analysis is performed to observe the sensitivity of the two designs to process variations. The Fast corner FF at –40 ^{o}C and the Slow corner SS at +80 ^{o}C are compared against the Typical case TT at +27 ^{o}C. The center frequency and tuning range, calculated as $(f_{max}/f_{min}–1)\times100$, is also shown in Table 4.5.

Table 4.5 Overall tuning range for Design A and Design B

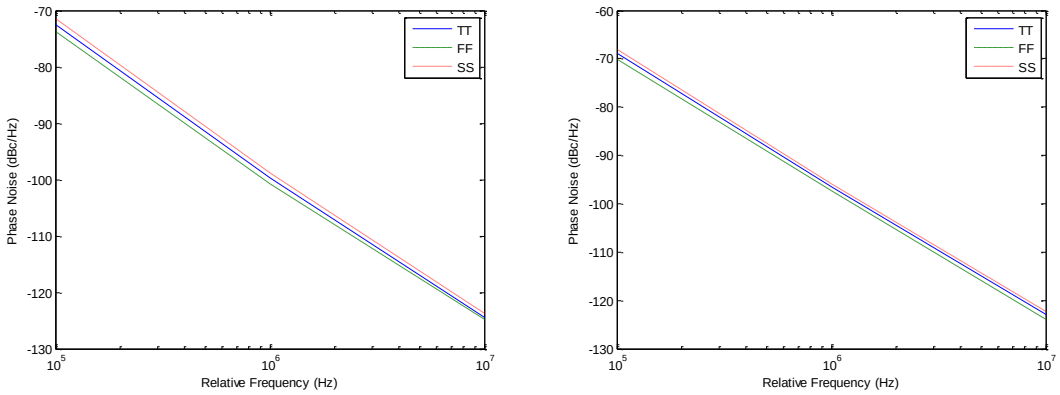
	Process Corner	**Tuning Range (GHz)**	**Center Frequency (GHz)**	**Tuning Range (%)**
Design A	TT	11.87 to 17.02	14.45	43.39
	FF	12.07 to 17.11	14.59	41.76
	SS	11.60 to 16.95	14.28	46.12
Design B	TT	11.18 to 14.40	12.79	28.80
	FF	11.62 to 14.56	13.09	24.30
	SS	10.70 to 14.22	12.46	32.90

Both the results above and the simulated tuning range show the same trend. Design A has a higher and wider tuning range compared to Design B. The reason for this is that

Design B includes the use of a switched-capacitor placed in parallel with the LC-tank; this switched-capacitor has a fixed capacitance which is present even when the switched-capacitor is off. This fixed capacitance placed in parallel with the LC-tank acts to drop the VCO frequency and decrease the tuning range. Tuning ranges at process corners FF and SS are also examined. The results indicate that the designs are both relatively robust to process variations with Design A being slightly better.

4.2.3 Phase Noise

The phase noise performance for both Designs A and B are shown in Figure 4.4. The typical case TT as well as process corners FF and SS are also shown in the same graph. As can be seen, both designs are quite robust to process variations.



a) b)

Figure 4.4 Phase noise performance of a) Design A, b) Design B

The phase noise for the corners at 1 MHz offset is shown in Table 4.6. The % variation is calculated by the following formula:

$$\%\, Variation = \frac{Highest\ Phase\ Noise - Lowest\ Phase\ Noise}{Typical\ Phase\ Noise}\ X\ 100\% \qquad (4.1)$$

Table 4.6 Phase noise for Design A and Design B at 1-MHz offset

	TT	FF	SS	%Variation
Design A	–99.76 dBc/Hz	–100.76 dBc/Hz	–98.83 dBc/Hz	1.93%
Design B	–96.47 dBc/Hz	–97.31 dBc/Hz	–95.85 dBc/Hz	1.51%

For the simulation with no extraction, the phase noise results of Design A and B are very close to one another; one is -89.87 dBc/Hz at 1 MHz offset and another is -90.31 dBc/Hz at 1 MHz offset. For post-layout simulations, Design A is approximately 3 dB better than Design B for all corners. This can be explained by the fact that for Design B, the switched-capacitor is placed in parallel with the LC-tank which decreases the Q of the LC-tank.

Chapter 5: Experimental Method and Measurement Results of 13-GHz VCO

This chapter provides the experimental setup and procedures to test the two 13-GHz VCOs. Also included in this chapter is a discussion of the measurement results. Section 5.1 describes the circuit layout characteristics for both VCO designs. Section 5.2 lists the required equipment and provides a description of test procedures that are feasible with the available equipment, illustrated using schematics. Finally, Section 5.3 provides the VCO measurement results and compares them to the state-of-the-art.

5.1 Circuit Layout Characteristics

Two chips were fabricated in 90-nm CMOS technology. The chip that corresponds to Design A occupies an area of 0.336 x 0.750 mm^2, without pads. The chip includes both VCO cores with their corresponding buffers and biasing circuitry. Figure 5.1 shows the layout of Design A with pad names.

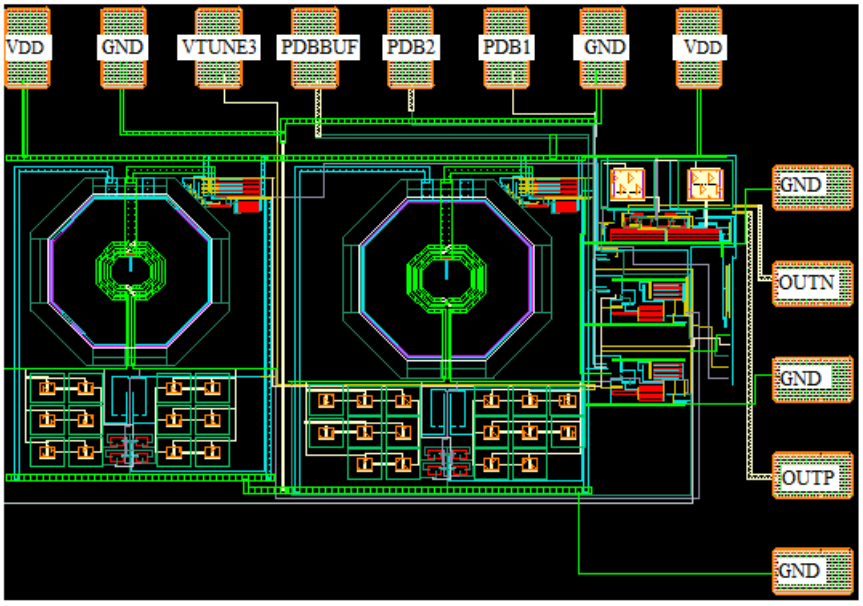


Figure 5.1 Design A layout with pad names

Table 5.1 lists the names of the pads for the layout of Design A and their usages.

Table 5.1 Design A fabricated chip pin functions

Pin Name	Pin Usage
VDD	1.2 V supply
GND	Ground (0 V)
VTUNE3	VCO voltage control for changing VCO frequency, = 0 V to 1.2 V
PDBBUF	Enables CML buffer stage, = 0 V for disable, = 1.2 V for enable
PDB1	Enables VCO core 1 and corresponding follower buffer, = 0 V for disable, = 1.2 V for enable
PDB2	Enables VCO core 2 and corresponding follower buffer, = 0 V for disable, = 1.2 V for enable
OUTP	Differential output
OUTN	Differential output

*Note: PD means Power Down

The chip that corresponds to Design B occupies an area of 0.316 x 0.425 mm^2, without pads. The chip includes VCO core with switched-capacitor, buffer, and biasing circuitry. Figure 5.2 shows the layout of Design B with pad names.

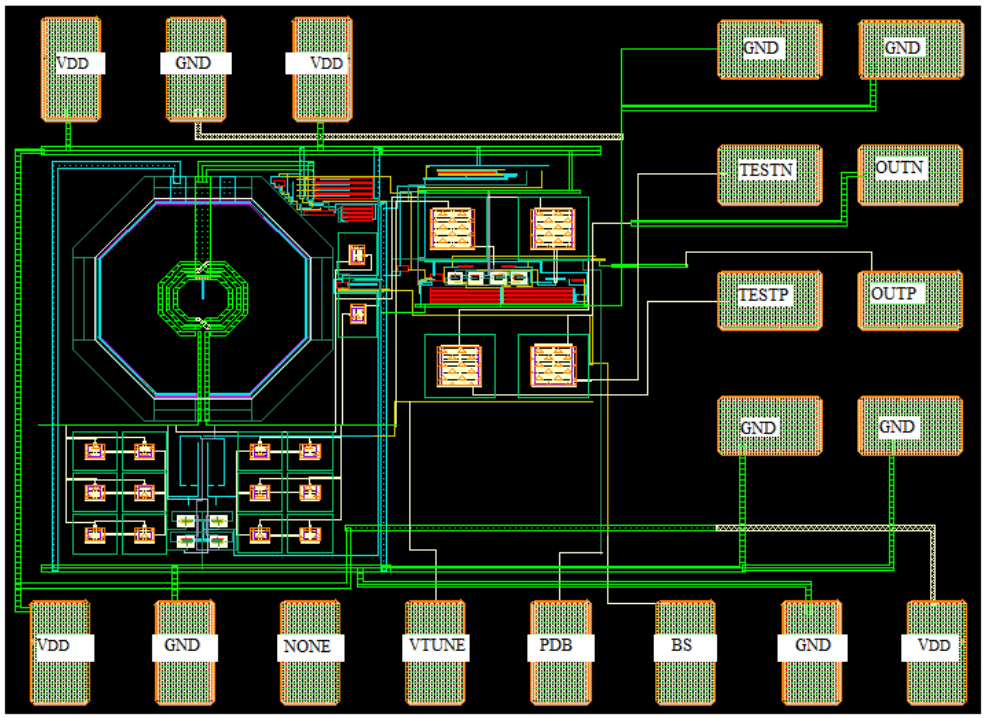


Figure 5.2 Design B layout with pad names

Table 5.2 lists the names of the pads for the layout of Design B and their usages.

Table 5.2 Design B fabricated chip pin functions

Pin Name	Pin Usage
VDD	1.2 V supply
GND	Ground (0 V)
VTUNE	VCO voltage control for changing VCO frequency, = 0 V to 1.2 V
PDB	Enables VCO core and corresponding CML buffer stage, = 0 V for disable, = 1.2 V for enable
BS	Enables switching capacitor, = 0 V for disable, = 1.2 V for enable
TESTP	Differential output with AC coupling to isolate DC condition
TESTN	Differential output with AC coupling to isolate DC condition
OUTP	Differential output
OUTN	Differential output

5.2 Experimental Setup

This section details the test plan for both VCO designs. A list of test equipment required to perform the tests is provided. A description of the tests is also given as well as illustration of the test setup using testbench schematics.

5.2.1 Required Equipment

Table 5.3 lists the required equipment necessary for the characterization of the two VCO designs.

Table 5.3 Test Equipment

Quantity	Equipment
1	RF Probe station
1	PGLLLLGP 500 MHz signal probe
1	GSGSG 40 GHz signal probe
1	GSSG 50 GHz signal probe
1	PGP DC signal probe
1	Shielded Room (Electromagnetic Compatibility Lab - MCLD 132)
1	1.2 V Nickel-metal-hydride battery with battery holder and small circuit to vary vtune using potentiometer
2	DC Power supplies
4	Low-frequency cables
6	SMA (SubMiniature version A) cables
1	N9030A-526 PXA Spectrum Analyzer
2	Multimeters
1	Bias-T (26 GHz)

5.2.2 VCO Characterization

The testbench schematic for Design A characterization is provided in Figure 5.3.

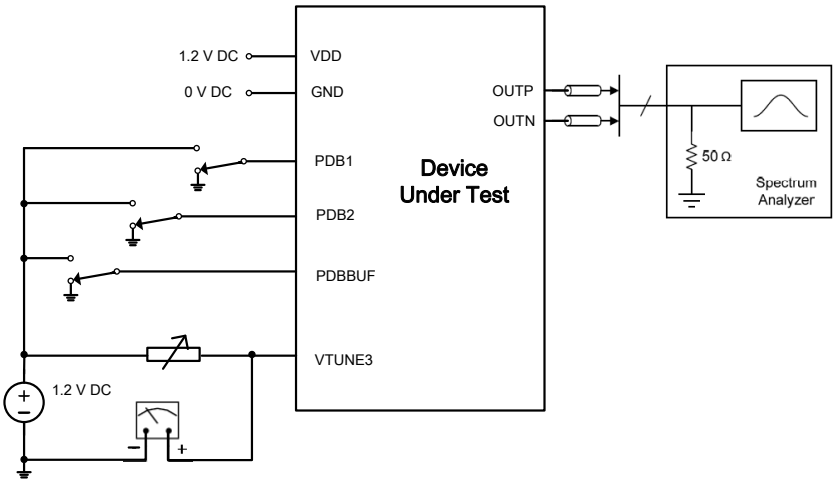


Figure 5.3 Testbench schematic for characterization of Design A

PDBBUF is always switched on, and one VCO with its corresponding follower buffer is enabled at a time by switching on either PDB1 or PDB2. As VTUNE3 is swept, the range of frequencies is measured using the spectrum analyzer. Power consumption is measured via the current drawn using a multimeter. The peak-to-peak voltage is measured using the spectrum analyzer. Finally, the spectrum analyzer is also used to measure phase noise.

The testbench schematic for Design B characterization is provided in Figure 5.4.

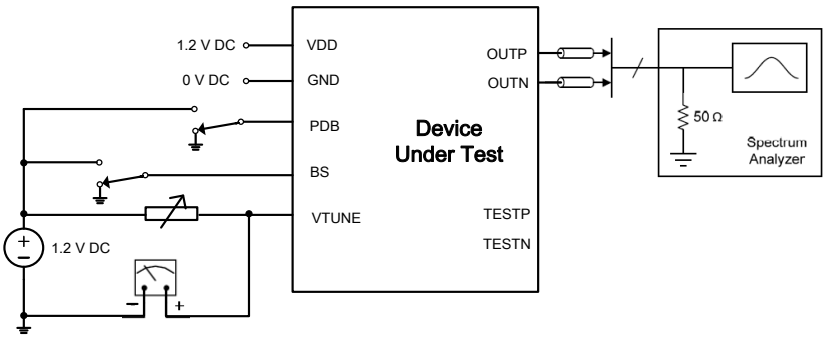


Figure 5.4 Testbench schematic for characterization of Design B

PDB is always switched on, and BS is switched either on or off for enabling and disabling the switched-capacitor. As VTUNE is swept, the range of frequencies is measured using the spectrum analyzer. Like for Design A, power consumption is measured via the current drawn. The peak-to-peak voltage is also measured using the spectrum analyzer. Finally, the spectrum analyzer is used to measure phase noise.

Figure 5.5 shows the initial test setup for VCO characterization where voltage is being supplied by the DC power supplies.

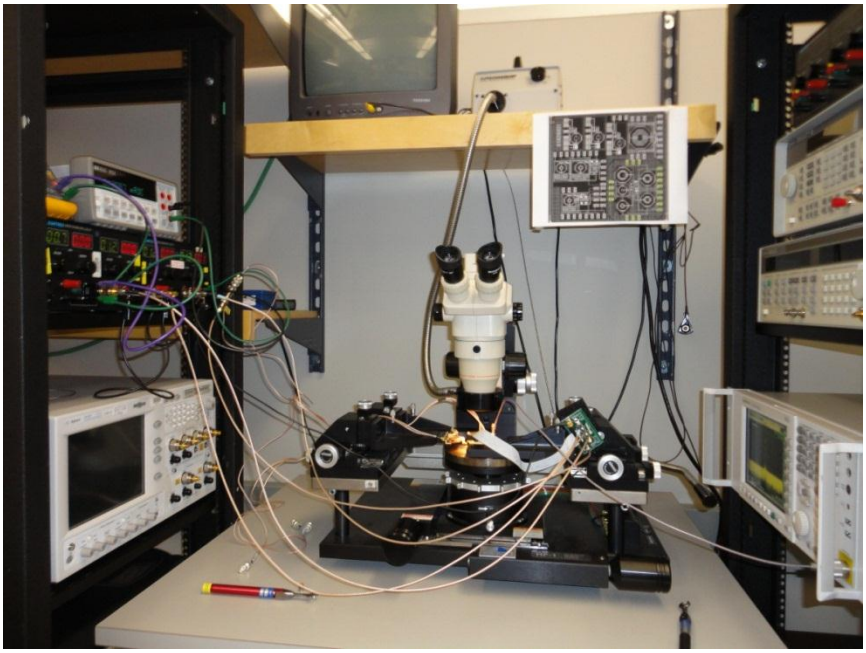
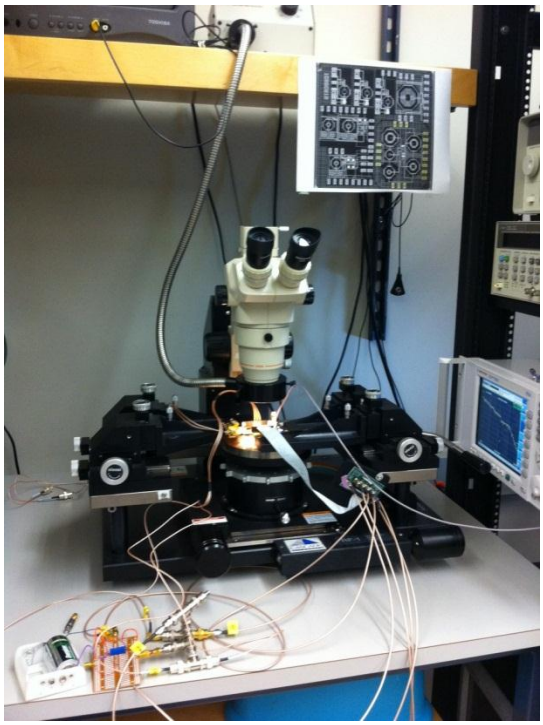


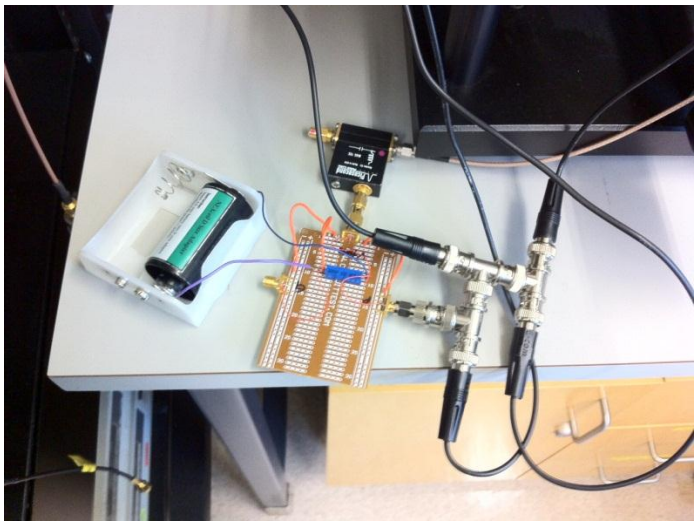
Figure 5.5 Test setup with DC power supplies

To improve phase noise measurements, a 1.2 V battery was used instead of the DC power supplies. To further improve phase noise measurements, the setup was moved to a shielded room to ensure that the electrical settings of the room was not interfering with measurements. A final attempt to improve phase noise was to use a bias-T at V_{tune} with a battery. These setups are shown in Figure 5.6.



a)

b)



c)

Figure 5.6 Test setup with a) battery, b) battery and shielded room, c) battery and bias-T

5.3 Chip Experimental Results

This section discusses the measurement results from the equipment setups described in section 5.2. A micrograph of the fabricated chip with the two VCO designs outlined and annotated is shown in Figure 5.7.

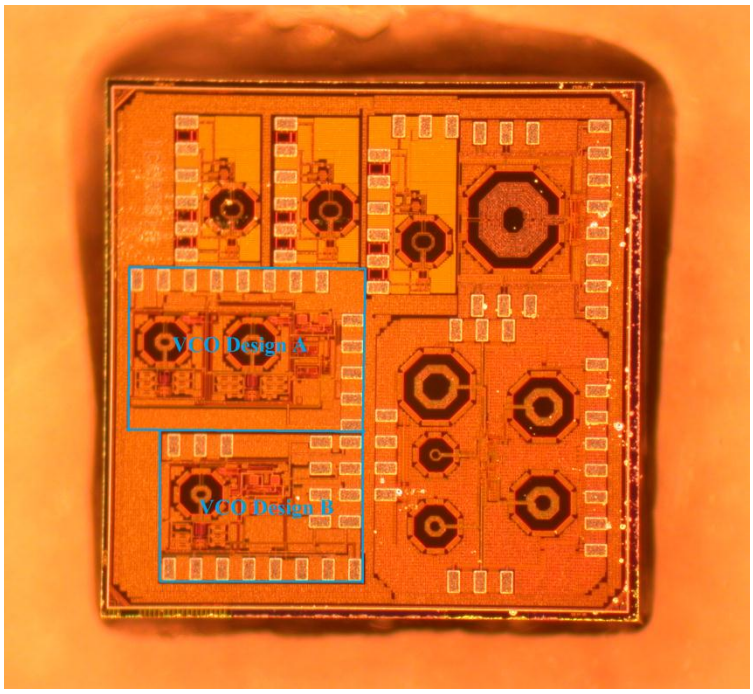


Figure 5.7 Chip micrograph

5.3.1 Measured Amplitude, Power Consumption, and Tuning Range

A sample measurement of the oscillation spectrum of Design B when the switched-capacitor is off measured at V_{tune} = 1.2 V is shown in Figure 5.8. The measured frequency is approximately 13.3 GHz, and the power magnitude of -12.96 dBm corresponds to a peak-to-peak amplitude of 142 mV. The amplitude is smaller than post-layout simulations, however is sufficient to indicate that the VCO is working well. The amplitude is smaller than expected due to the fact that an additional source follower buffer was not used at the output for proper matching to the measuring equipment. This will be further discussed in Chapter 7. It was noted that the measured amplitude of Design A was smaller than that for Design B.

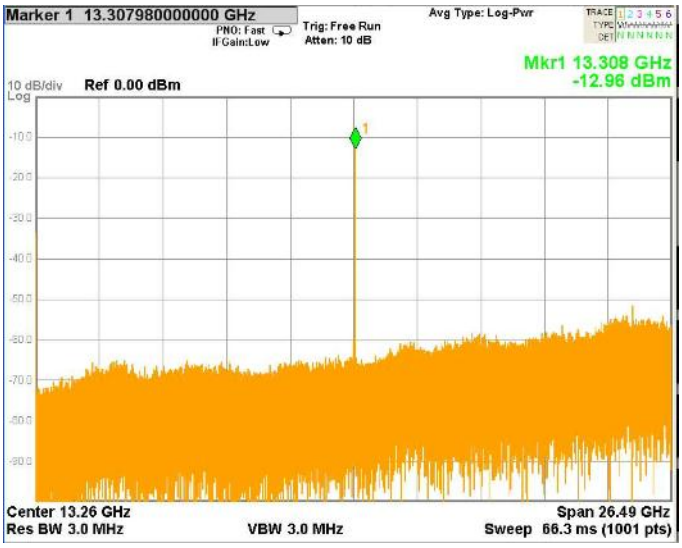


Figure 5.8 Sample measured oscillation spectrum

The total current measured and along with the resulting calculated power consumption of each design is indicated in Table 5.4.

Table 5.4 Measured current and power consumption

		Current	Power Consumption
Design A	VCO 1 Enabled	18.31 mA	21.97 mW
	VCO 2 Enabled	14.56 mA	17.47 mW
Design B	Switched-cap. Disabled	13.50 mA	16.20 mW
	Switched-cap. Enabled	13.13 mA	15.76 mW

The total current and power consumption are lower than the post-layout simulation results. It was noticed that during post-layout simulations the total current varied quite a bit for process corners. Thus, it is believed that process variation of the transistors of the biasing circuitry is the main cause for the difference in simulated and measured current. This problem can be fixed by changing the design of the current source. This will be elaborated in Chapter 7.

The overall tuning range covered for Design A and Design B are indicated in Table 5.5.

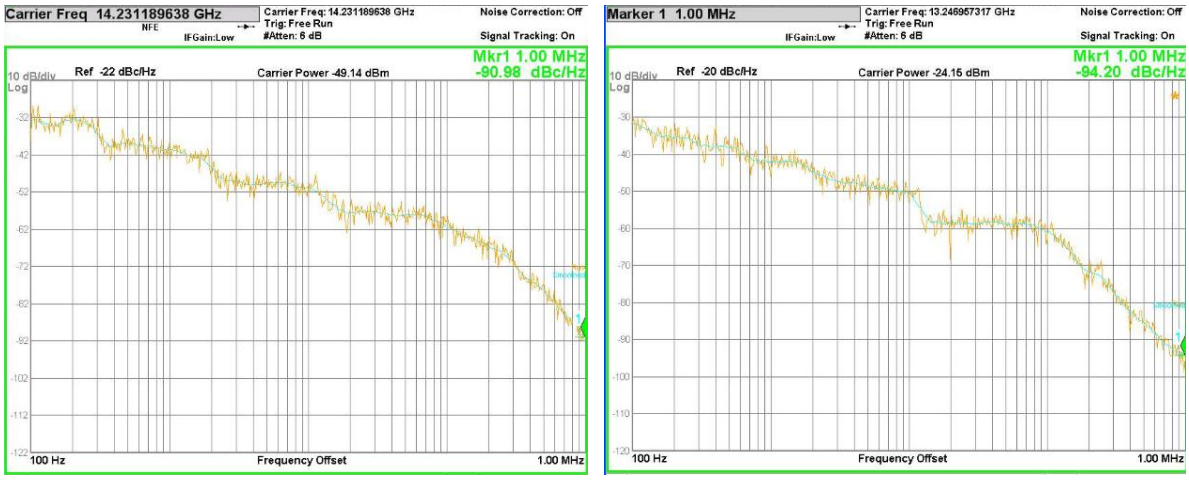
Table 5.5 Measured tuning range

	Tuning Range (GHz)	Centre Frequency (GHz)	Tuning Range (%)
Design A	11.10 – 14.23	12.67	28.20
Design B	10.69 – 13.30	12.00	24.42

The measured tuning range is smaller than post-layout simulations, especially for Design A. One reason is that for the post-layout simulation results, the tuning range corresponds to control voltages of 0 V to 1.2 V, whereas for measurements tuning range can only be measured starting at 0.2 V to 0.3 V. Another obvious reason is the presence of parasitic resistance and capacitance which reduces range.

5.3.2 Measured Phase Noise

Phase noise measurements were improved slightly when using a battery instead of DC power supplies. Testing in the shielded room did not have a noticeable effect on further improving the phase noise. When using a bias-T as part of the equipment setup, the phase noise improved by approximately 2 dB. The measured phase noise for Design A is -90.98 dBc/Hz at 1-MHz offset and that for Design B is -94.20 dBc/Hz at 1-MHz offset both at Vtune = 1.2 V. The measured phase noise for Designs A and B are shown in Figure 5.9.



(a) (b)

Figure 5.9 Measured phase noise of Design (a) A, (b) B

The measured phase noise is worse than post-layout simulations; the main reason for this is the lower measured current compared to the post-layout current. This causes decreased VCO and buffer output amplitude. Phase noise is inversely proportional to VCO output power and amplitude. The measured phase noise of Design A is slightly worse than that of

Design B, contrary to post-layout results; the reason again can be attributed to the lower measured amplitude of Design A compared to post-layout simulations and compared to the lower measured amplitude of Design A compared to Design B. Since as mentioned before the bias current of the designs were lower than expected and due to the fact that Design A has more stages compared to Design B, its final output amplitude was more impacted by the lower bias current.

5.3.3 Comparison of VCO Measurements to Published Works

Table 5.6 summarizes the performance of the two LC-VCO designs and provides a comparison to other published works.

Table 5.6 Performance summary and comparison with published works

Ref.	[38]*	[39]*	[40]*	[41]	[42]*	[43]	**This Work Design A***	**This Work Design B***
CMOS Tech. (nm)	180	130	130	90	180	130	90	90
f_{out} (GHz)	12	15	26.3	5	10	5.2	12.7	12.0
Tuning Range	5.37%	7.48%	26.5%	30%	4.60%	26%	28.20%	24.42%
Phase Noise (dBc/Hz at 1MHz)	-110.8	-112	-92.6	-98.8	-101	-98.5	-90.98	-94.20
P_{diss} (mW)	8.1	33.64	36.5	2.52	9.0	4.2	5.07	5.10
Area (μm^2)	670×672	512×482	1000×1400	350×190	1500×1100	760×850	335×750	316×425
FOM_T (dBc/Hz)	-159.3	-161.1	-160.9	-152.1	-144.5	-148.1	-155.9	-157.0

* Measured results

In Table 5.6, the power dissipation of the VCO core for this work was estimated to be proportional to the simulation results of the power dissipation of the VCO core, since direct measurement of the VCO core's power dissipation could not be measured.

A commonly accepted figure of merit FOM_T [44,45] characterizes the performance of a VCO relative to other VCOs of the same type and considers not only the phase noise but also takes into account the power consumption and the tuning range. FOM_T for the oscillator is given by:

$$\mathrm{FOM_T} = \iint\{\Delta\omega\} - 20 \cdot \log\left[\left(\frac{\omega_o}{\Delta\omega}\right) \cdot \left(\frac{\mathrm{FTR}}{10}\right)\right] + 10 \cdot \log\left(\frac{\mathrm{P_{diss}}}{1\mathrm{mW}}\right) \tag{5.1}$$

where $\Delta\omega$ is the offset from the carrier, ω_o is the nominal oscillation frequency, $\iint\{\Delta\omega\}$ is the phase noise at the specified offset, P_{diss} is the power consumed by the VCO core, and FTR is the frequency tuning range.

As can be seen from Table 5.6, the tuning range of the VCOs designed in this work are good in comparison to that of other state-of-the-art. However, although still comparable to others' work, both phase noise and thus FOM_T have room for improvement.

Chapter 6: Other Blocks of PLL and Closed Loop PLL

This chapter discusses the remaining components of the PLL, namely the phase frequency detector (PFD), charge pump, loop filter, and Verilog-A divider. The combined task of the PFD, charge pump, and loop filter blocks is to provide a stable DC tuning voltage to the VCO based on the frequency and phase difference between the reference frequency and output of the divider so that acquisition of the PLL can be achieved. Section 6.4 provides the closed-loop 13-GHz PLL simulation result.

6.1 Phase Frequency Detector

This section describes the phase frequency detector, a very useful circuit, as it significantly increases the acquisition range and lock speed of PLLs [46]. Section 6.1.1 gives the theory and background information needed to understand this circuit, and Section 6.1.2 discusses the design implemented.

6.1.1 Theory

The phase frequency detector is a sequential phase detector that has a memory function. It can act not only as a phase detector but also as a frequency detector, detecting both phase and frequency difference between two signals and generating an output that represents that difference [47]. The PFD has two outputs, "Up" and "Dn," which open or close the two current sources of the charge pump. When the "Up" signal is high, the charge pump dumps current in the loop filter; this causes a rising voltage at the VCO input, increasing the frequency. The "Dn" signal draws current out of the loop filter impedance and causes a control voltage drop. A third state occurs when none of the signals is active. At this state the output current is zero and the output is a high-impedance node. The fourth state, where both current sources are active, never occurs theoretically [1].

Figure 6.1 (a) shows a simple implementation of a PFD consisting of two edge-triggered, resettable D flipflops with their D inputs tied to logical One. Inputs A and B serve as the clocks of the D flipflops.

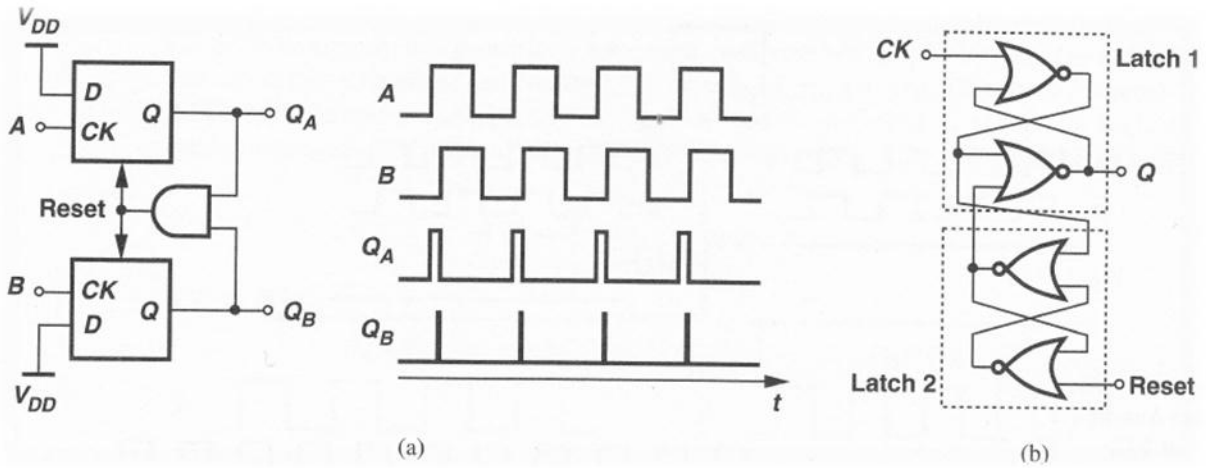


Figure 6.1 (a) Implementation of PFD, (b) Implementation of D flipflop [48]

Suppose the initial condition is $Q_A = Q_B = 0$ and A goes high, then Q_A rises. If this is followed by a rising transition on B then Q_B goes high and the AND gate resets both D flipflops; thus, Q_A and Q_B are both high for a short time. The difference between Q_A and Q_B, however, still represents correctly the input phase or frequency difference. Each D flipflop can be implemented as shown in Figure 6.1 (b) using four NOR gates [48].

When the phase difference, also known as the phase error, is extremely small, there will be problems with the PFD responding to it correctly. Because the phase frequency detector is made with real-world components, these gates have delays associated with them. The delays of the components must match, and if they do not match the delay difference results in dead zone. When dead zone is present in a synthesizer, until the phase difference reaches a certain value, the loop fails to correct the error resulting in the VCO control voltage not being able to change as desired [47]. It is important for PLLs to have dead zone elimination circuitry to ensure that the charge pump always comes on for some amount of time to avoid operating in the dead zone [49]. Eliminating dead zone is important for accurate frequency generation and low phase noise in frequency synthesizer PLLs [50]. A widely adopted method of resolving the dead zone problem easily is by adding a delay in the reset path as shown in Figure 6.2 [1].

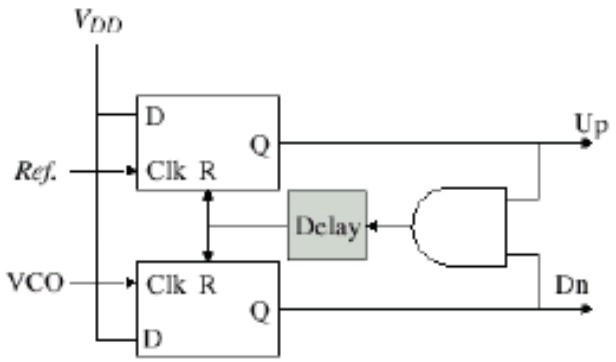


Figure 6.2 Implementation of PFD without a dead zone

6.1.2 Design

To avoid the dead zone problem, an appropriate delay is added in the PFD reset path. However, because of this delay, there will be short pulses on both the "Up" and "Dn" signals, even in the locked state. Therefore, the charge pump will switch on and off, and current spikes will appear on the charge pump output at the reference frequency. If the reset delay in the PFD is too long more noise will be introduced. Thus, careful consideration of the delay length of the PFD is crucial [50].

The amount of delay in the PFD reset path is the key parameter to the dead zone. The appropriate value of the delay was initially chosen by trial and error. Simulations were performed and based on the results sufficient adjustments were made to the delay value to find the suitable value. It was found that a reset delay of approximately 400 ps – 600 ps was sufficient. The design of the PFD is shown in Figure 6.3. The design implemented is the same as that discussed in Section 6.1.1 and shown in Figure 6.2. The inclusion of charge-pump buffers is for increased drivability to the charge pump. There is a buffer included in the reset path to act as a delay.

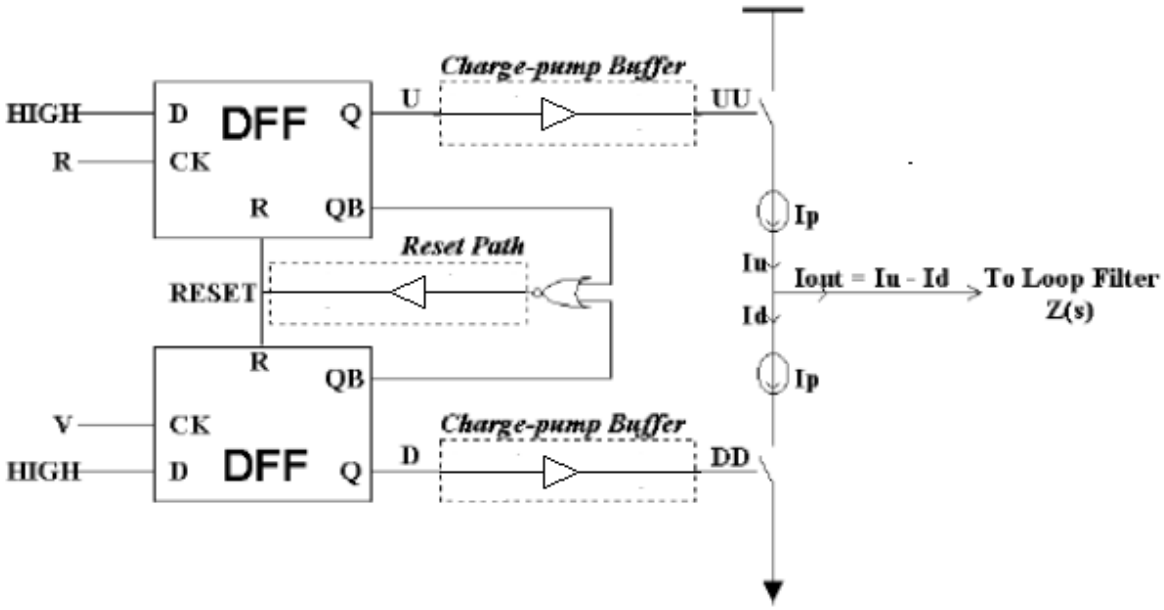


Figure 6.3 Design of the PFD without deadzone and charge pump [50]

6.2 Charge Pump

The charge pump circuit is another key element in a PLL. It is an analog circuit controlled by the phase frequency detector outputs. Section 6.2.1 discusses how the charge pump works, and Section 6.2.2 describes the charge pump implemented.

6.2.1 Theory

The charge pump is a three position electronic switch which is controlled by the three states of the PFD. Its function is to charge and discharge the loop filter according to the outputs of the PFD, so that the phase error is converted to a control voltage to adjust the frequency of the VCO [51]. It in effect transfers the digital signals of "Up" and "Dn" from the PFD to analog signals [52]. A simple model of the charge pump circuit together with a capacitor representing the loop filter is shown in Figure 6.4.

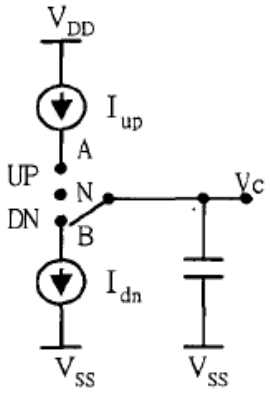


Figure 6.4 A simple model of the charge pump circuit [52]

As shown in Figure 6.4, when the "Up" signal is high, the switch connects to node A and V_c is charged by the upper current source I_{up}. When the "Dn" signal is high, the switch connects to node B and V_c is discharged by the lower current source I_{dn}. If both signals "Up" and "Dn" are low, then the switch maintains at node N and V_c holds the original voltage [52]. The main function of the charge pump is to match the I_{up} and I_{dn} currents. Mismatch between the two results in a net charge deposited onto the loop filter every time a comparison is made [47].

6.2.2 Design

A simple charge pump was designed, the schematic of which is shown in Figure 6.5. As can be seen in Figure 6.5, the "Up" and "Dn" switches of the charge pump are implemented with PMOS (M_2) and NMOS (M_{10}) transistors respectively. Mirror current transistors consist of M_{11}, M_8, M_3, M_4, M_5, M_6, and M_7. Transistors M_9, M_1, and M_0 cascode with the mirror current and increase the mirror current's output impedance. They are also used for matching with the voltage drop across the switches, resulting in the current reference being accurately mirrored to M5 and M7 [47].

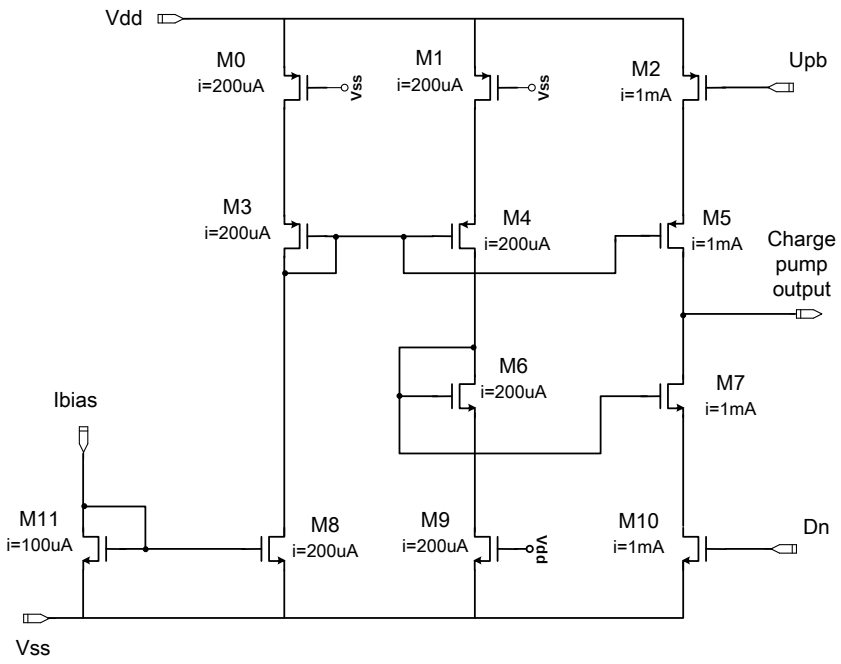


Figure 6.5 Schematic of the implemented charge pump

During debugging, the mirror current transistors' lengths were increased gradually so that the charging and discharging currents flowing through M_2 and M_{10} respectively become as close as possible and match one another. Transistor lengths were increased because as indicated in [23]:

$$R_{total} = R\square\ (L/W) \tag{6.1}$$

or in other words, the total resistance is proportional to L.

Also since

$$\Delta I = \Delta V/\Delta R \tag{6.2}$$

an increase in L will result in a decrease in ΔI; thus, an increase in L will result in smaller current variation and a closer match between charging and discharging currents.

6.3 Loop Filter

The loop filter is often regarded as the circuit in the PLL that is hardest to design. This section introduces the loop filter and discusses how we designed two loop filters, one for loop bandwidth 1 MHz and the other for loop bandwidth 500 kHz.

6.3.1 Theory

VCOs are controlled by voltage and not current. Therefore, we need something to turn the current produced by the charge pump back into a voltage. This is usually accomplished by dumping the charge produced from the charge pump onto a capacitor's terminals. A simple capacitor by itself does not yield a stable loop; therefore, a combination of capacitors and resistors is usually used [53]. Other uses of the loop filter are its ability to remove high frequency (reference frequency) noise of the phase frequency detector and its ability to influence the switching speed of the loop in lock [54]. The proper design of the loop filter is also important for the stability of the PLL loop [55]. Finally, the loop filter is the component most commonly used to control system-level loop dynamics [53].

Loop filters can be classified as either active or passive loop filters. Active loop filters usually consume less area and usually allow for more design flexibility [56]. However passive loop filters are more common because they are relatively simpler, consisting of capacitors and resistors only, have relatively low noise, have unlimited frequency range, and do not consume power [57,54]. In this design, passive loop filters are used.

The design of the loop filter is crucial and determines most of the specifications of the PLL. The circuit component values chosen for the loop filter must be a very carefully balanced compromise between a number of conflicting requirements. Extra poles and zeroes can be introduced in the loop transfer function; these influence the noise and dynamic performance of the loop [31]. In what follows the first-order PLL is first discussed. The PLL performance is improved by extending this first-order loop to higher orders and types. It is important to note that the *order* of the PLL is determined by the highest power of *s* in the denominator of the transfer function. The *type* of the loop is the number of perfect

integrators in the loop; because of the perfect integration in the VCO, every PLL is at least type-I [1].

Generally, the order of the PLL is one higher than the order of the loop filter, as the VCO itself provides a pole. A first-order loop filter for a second-order PLL is shown in Figure 6.6(a). A second-order loop filter is shown in Figure 6.6(b). In Figure 6.6(b), the capacitor C1 is recommended to avoid discrete voltage steps at the VCO control port due to the instantaneous changes in the current output from the charge pump [58]. A low pass filter may be needed for additional rejection of reference sidebands called spurs [58].

(a) (b)

Figure 6.6 (a) First-order loop filter, (b) Second-order loop filter [58]

It is important to discuss the PLL transfer functions here. Figure 6.7 shows the PLL linear model, where K_{VCO} is the gain of the VCO (the frequency vs. voltage tuning ratio), K_ϕ is the phase detector/charge pump constant (the ratio of the current output to the input phase differential), and N is the divider ratio.

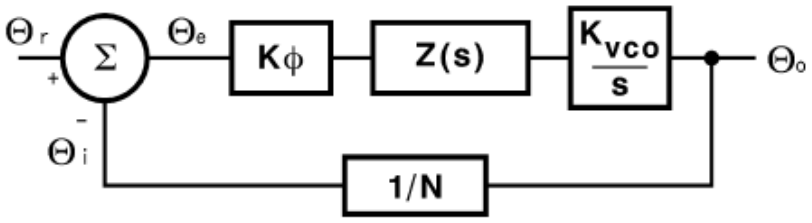


Figure 6.7 PLL linear model [58]

By referring to Figure 6.7, the PLL phase transfer functions are defined as follows [58]:

$$Forward\ loop\ gain = G(s) = \frac{\theta_o}{\theta_e} = \frac{K_\phi Z(s) K_{VCO}}{s} \tag{6.3}$$

$$Reverse\ loop\ gain = H(s) = \frac{\theta_i}{\theta_o} = \frac{1}{N} \tag{6.4}$$

$$Open\ loop\ gain = H(s)G(s) = \frac{\theta_i}{\theta_e} = \frac{K_\emptyset Z(s) K_{VCO}}{Ns} \tag{6.5}$$

$$Closed\ loop\ gain = \frac{\theta_o}{\theta_r} = \frac{G(s)}{[1+H(s)G(s)]} \tag{6.6}$$

The detailed derivation of the basic second-order PLL open loop and closed loop transfer functions are shown in Appendix A. Higher order PLL transfer functions are based on this, however are much more complex.

One method of loop filter design uses the open loop gain bandwidth and phase margin to determine the component values. To ensure loop stability, we must locate the point of minimum phase shift at the unity gain frequency of the open loop response as shown in Figure 6.8. The phase margin ϕ_p is defined as the difference between 180^o and the phase of the open loop transfer function at the frequency ω_p, which corresponds to 0-dB gain. ω_p is also known as the loop bandwidth of the PLL. The phase margin is typically chosen between 30^o and 70^o. It is common to begin a loop filter design with a 45^o phase margin [58]. The phase margin should in general be maximized to ensure loop stability [47].

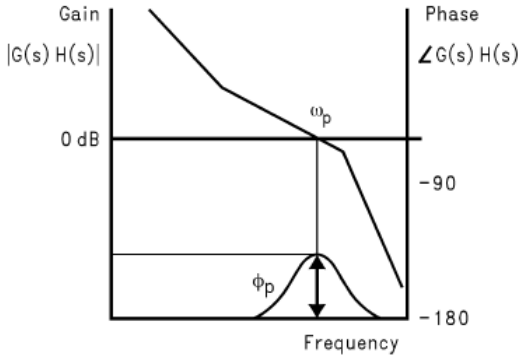


Figure 6.8 Open Loop Response Bode Plot [58]

The impedance of the second-order loop filter shown in Figure 6.6(b) is

$$Z(s) = \left(R_2 + \frac{1}{s*C_2}\right) // \left(\frac{1}{s*C_1}\right) \tag{6.7}$$

which is equal to

$$Z(s) = \frac{s*C_2*R_2+1}{s^2*C_1*C_2*R_2+s*C_1+s*C_2} \quad (6.8)$$

Often times, additional filtering of the reference spurs (i.e., inband noise from reference) is necessary, depending on how narrow the loop filter is. For these applications where performance is key, a series resistor R_3 and a capacitor C_3 can be placed prior to the VCO to provide a low pass pole for more attenuation of unwanted spurs [59], as shown in Figure 6.9. Figure 6.9 shows a third-order loop filter. The additional pole must be lower than the reference frequency in order to significantly attenuate the spurs, but it must be at least 5 times higher than the loop bandwidth, or else the loop will become unstable. As a rule of thumb, C_3 is usually chosen to be smaller than or equal to one-tenth of C_1, and R_3 is chosen to be at least twice the value of R_2 [58].

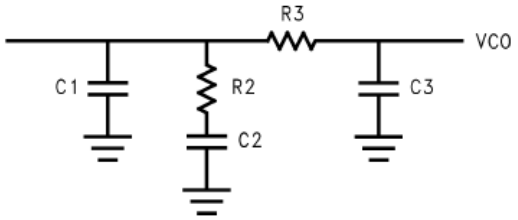


Figure 6.9 Third-order loop filter [58]

6.3.2 Design

A third-order loop filter is designed. As mentioned in section 6.3.1, the third-order loop filter is desirable for its high performance qualities such as its ability to reduce noise caused by the reference and other blocks such as the divider and charge pump. This is very important in frequency synthesizer applications [60]. Loop filter component values are first approximated by a series of calculations as discussed in National Semiconductor's Application Note 1001 [58]. Two loop filters are designed, one for loop bandwidth approximately 1 MHz and another for loop bandwidth approximately 500 KHz. The following equations are used to estimate the values of C_1, C_2, C_3, R_2, and R_3 in the third-order loop filter shown in Figure 6.6 for the two loop bandwidths.

For a bandwidth of about 1MHz, the following values are assumed:

K_{VCO} = 5 GHz/volt

K_ϕ = 1 mA/2πrad

RF_{opt} = 13 GHz

F_{REF} = 100 MHz

N = RF_{opt}/F_{REF} = 130

$\omega_p = 2\pi(1MHz)$

$\phi_p = 45^o = (\pi/4)$ rad

ATTEN = 10 dB

where K_{VCO} is the voltage controlled oscillator tuning voltage constant, the frequency vs. voltage tuning ratio; K_ϕ is the phase detector/charge pump constant, the ratio of the current output to the input phase differential; RF_{opt} is the radio frequency output of the VCO at which the loop filter is optimized; F_{REF} is the frequency of the phase detector inputs, usually equivalent to the RF channel spacing; N is the main divider ratio, equal to RF_{opt}/F_{REF}; ϕ_p is the phase margin; and ATTEN is the attenuation.

$$T1 = \frac{\sec(\phi_p) - \tan(\phi_p)}{\omega_p} \tag{6.9}$$

$$T3 = \sqrt{\frac{10^{\frac{ATTEN}{10}} - 1}{(2\pi F_{REF})^2}} \tag{6.10}$$

$$\omega_c = \frac{tan(\phi_p)\cdot(T1+T3)}{(T1+T3)^2+T1+T3} \cdot \left[\sqrt{1 + \frac{(T1+T3)^2+T1\cdot T3}{\left[tan(\phi_p)\cdot(T1+T3)\right]^2}} - 1\right] \tag{6.11}$$

$$T2 = \frac{1}{\omega_c^2\cdot(T1+T3)} \tag{6.12}$$

Using the above, C1, C2, and R2 can be calculated as:

$$C1 = \frac{T1}{T2} \cdot \frac{K_\Phi \cdot K_{VCO}}{\omega_c^2 \cdot N} \cdot \sqrt{\frac{1+\omega_c^2\cdot T2^2}{(1+\omega_c^2\cdot T1^2)\cdot(1+\omega_c^2\cdot T3^2)}} \tag{6.13}$$

$$C2 = C1 \cdot (\frac{T2}{T1} - 1) \tag{6.14}$$

$$R2 = \frac{T2}{C2} \tag{6.15}$$

If we choose C3 = C1/10 then R3 = T3/C3, and all components of the loop filter are approximated. Sufficient adjustments are made based on simulation results. The component values of the loop filter for a bandwith of 1MHz and for a bandwidth of 0.5MHz are shown in Table 6.1 below.

Table 6.1 Loop filter component values for bandwidths of 1MHz and 0.5MHz

Bandwidth	C1	C2	R2	C3	R3
~1MHz	200pF	2.3nF	250Ω	4.8pF	490Ω
~0.5MHz	860pF	8.6nF	125Ω	9.4pF	250Ω

In order to understand the dynamic behaviour of the PLL, two important factors must be taken into consideration; these are ω_n, the natural frequency of the system, and ζ, the damping factor. ω_n is a measure of bandwidth whereas ζ is a measure of stability. ω_n and ζ are defined by the following equations [46]:

$$\omega_n = \sqrt{\frac{I}{2\pi C_P N} K_{VCO}} \tag{6.16}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{IC_P}{2\pi N} K_{VCO}} \tag{6.17}$$

where K_{VCO} is the frequency vs. voltage tuning ratio of the VCO, N is the divider ratio, I is the charge pump current, C_P is C2 in Table 6.1, and R is R2 in Table 6.1. Equations 6.16 and 6.17 suggest that both ω_n and ζ can be maximized simultaneously by increasing I or K_{VCO}, however increasing C_P increases ζ while decreasing ω_n . In general, ζ can be set independently by the resistor R. Once ω_n and ζ are known, the PLL bandwidth can be approximated using the following equations [53]:

$$Bandwidth \approx 2\zeta\omega_n \qquad for\ \zeta > 1.5 \tag{6.18}$$

$$Bandwidth \approx \left(1 + \zeta\sqrt{2}\right)\omega_n \qquad for\ \zeta < 1.5 \tag{6.19}$$

As equations 6.18 and 6.19 show, bandwidth is usually proportional to ω_n [46]. ω_n and ζ for the two bandwidth examples as well as a more precise estimation of the bandwidths are shown in Table 6.2.

Table 6.2 Natural frequency and damping factor of the PLL

Bandwidth	Natural frequency ω_n	Damping factor ζ
~0.878MHz	2.65 X 10^6 rad/s	0.763
~0.446MHz	1.37 X 10^6 rad/s	0.738

The proper loop bandwidth should be designed depending on the application to minimize the overall phase noise of the PLL [61].

6.4 13 – GHz Closed-loop PLL Simulation Results

Since this work focuses on the design of the VCO, other blocks of the PLL are all very simple designs. The Verilog-A divider used is similar to that described in [62]. Figures 6.10 and 6.12 show the transient responses of the closed loop for bandwidths of approximately 1 MHz and 0.5 MHz respectively. As can be seen in Figure 6.10, the PLL will be locked at approximately 5 μs when the bandwidth is about 1 MHz; however it takes much longer, approximately 16 μs for the PLL to lock when the bandwidth is about 0.5 MHz. This is because settling time is inversely proportional to bandwidth. Figures 6.11 and 6.13 indicate that when the PLL is locked, up and dn of the charge pump are lined up.

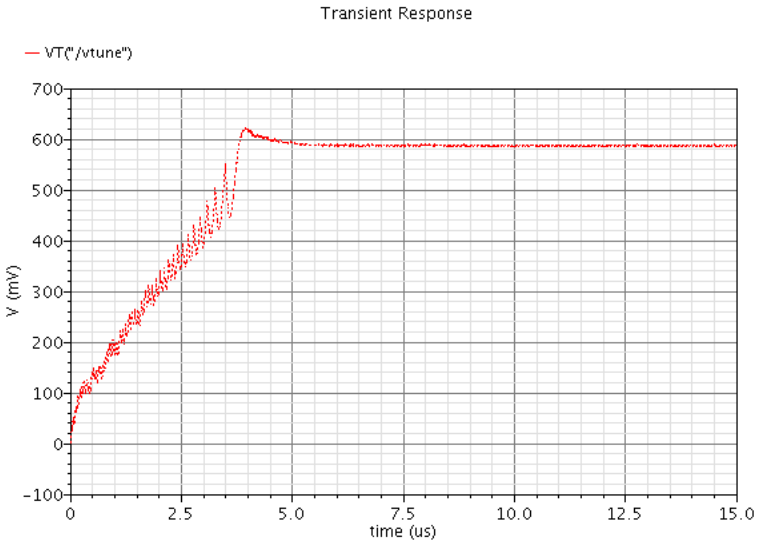


Figure 6.10 Transient response of closed loop PLL for bandwidth 1 MHz

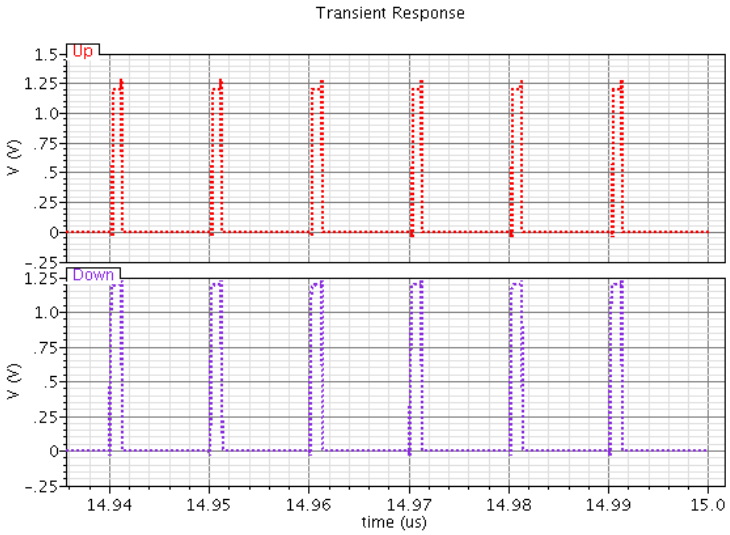


Figure 6.11 Charge pump response for bandwidth 1 MHz

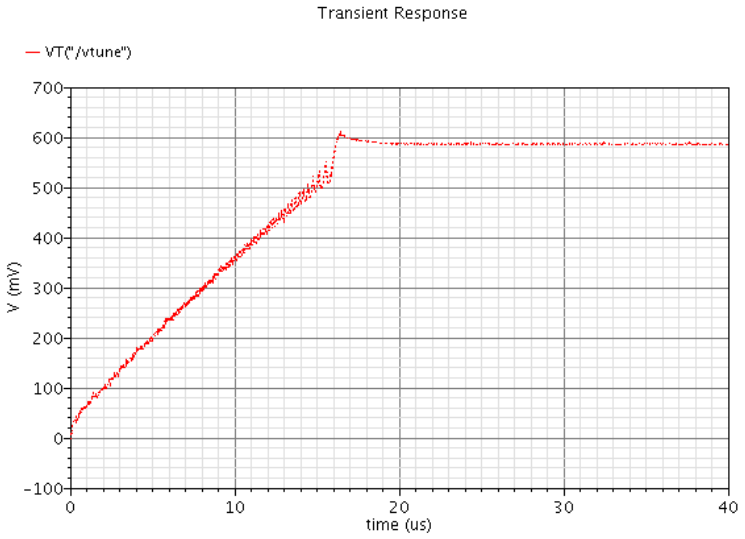


Figure 6.12 Transient response of closed loop PLL for bandwidth 0.5 MHz

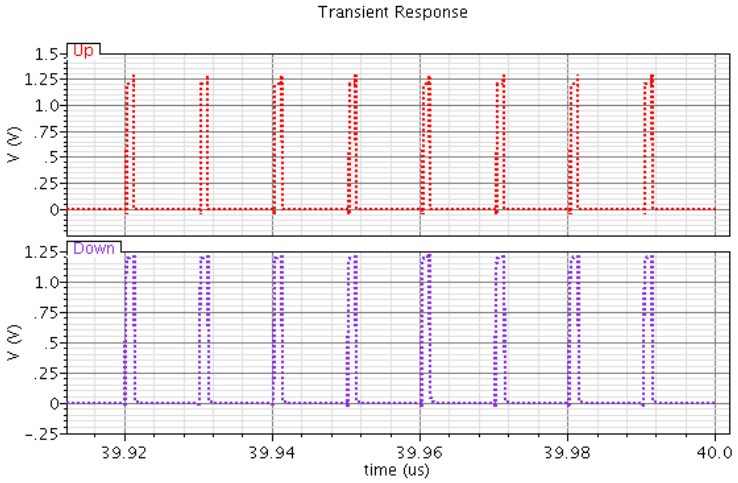


Figure 6.13 Charge pump response for bandwidth 0.5 MHz

Chapter 7: Conclusions

This chapter concludes the thesis. In Section 7.1, the main contributions of this work are briefly reviewed. Section 7.2 examines the problems encountered as well as potential limitations of this work. Finally, this chapter discusses some future work that could improve the current work.

7.1 Achievements

In this work, two wide-tuning-range 13-GHz LC-VCOs were designed. Design A has two VCO cores and incorporates a source follower buffer, whereas Design B uses a switched-capacitor to increase tuning range. The two designs were fabricated in a 90-nm CMOS technology. The total chip size, excluding the pads, is 0.335×0.750 mm^2 and 0.316×0.425 mm^2 for designs A and B, respectively. A review of the measured performance of the two designs is shown in Table 7.1

Table 7.1 Performance of LC-VCOs

Ref.	This Work Design A	This Work Design B
Tech. (nm)	90 CMOS	90 CMOS
f_{out} (GHz)	12.7	12.0
Tuning Range	28.20%	24.42%
Phase Noise (dBc/Hz at 1MHz)	-90.98	-94.20
P_{diss} (mW)	5.07	5.10
FOM_T (dBc/Hz)	-155.9	-157.0

Note that with the addition of the source follower buffer in Design A the oscillation frequency of the overall VCO has increased. The choice of which structure to use would mainly depend on the application. In general, if area is a main concern then Design B would be the more favorable choice. In the context of phase noise, one should pay special attention to the quality factor of the tank as any deterioration in the quality factor would adversely

affect the phase noise performance. In terms of power dissipation, assuming that the VCO cores of both Designs A and B dissipate about the same amount of power, the overall power consumption of the structures would be about the same.

Closed-loop PLL simulations for two loop bandwidths, 1 MHz and 500 kHz, using a simple charge pump, PFD, loop filter, and Verilog-A divider confirm that settling time is inversely proportional to bandwidth.

7.2 Problems and Limitations

There are a couple of problems/limitations to my designs that should be mentioned. Methods of resolving them will be discussed in Section 7.3. These issues are as follows:

a) One of the key limitations of this design is the absence of a source follower buffer at the output for equipment matching purposes. The consequence of this is the relatively low output amplitude.
b) The current was found to be different when comparing simulation results with measured results. The design of the current source could potentially be improved.

7.3 Future Work

To address the issues mentioned in Section 7.2:

a) For proper matching to the equipment and the 50Ω load, we must add a source follower buffer to the output of the CML buffer for both Designs A and B.
b) To improve the design of the current source we could add a programmable current source in parallel to the mirror current to adjust the current when the current changes. Another solution is to inject current from the outside instead of an on-chip current source.

The phase noise could be improved by methods such as:

1. Adding an inductor in the current source to remove upconverted flicker noise.
2. Designing a higher Q inductor.
3. Using high-V_{TH} NMOS which can in general improve the phase noise.

The other components of the PLL can be studied more in depth and improved for a more advanced PLL. Ideally, they should also be laid out and fabricated. Finally, it is well known that as the gate length of the transistors decreases, their operation speed increases [63]. Therefore, it is possible to increase the operation frequency of the designed VCO or PLL using a more advanced technology.

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Appendix

Appendix A: Second Order PLL Transfer Function and Derivation

Figure A.1 below shows the block diagram of the second order PLL.

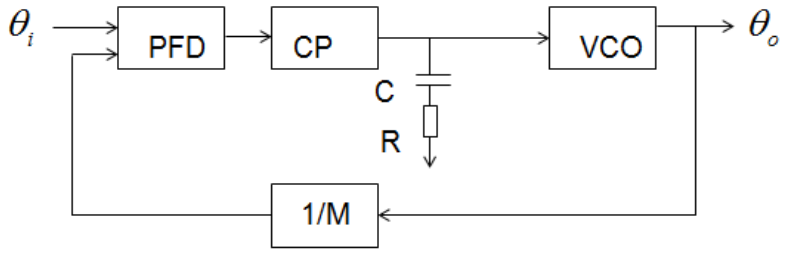

Figure A.1 Block diagram of second order PLL

The open loop and closed loop transfer functions of the above PLL are as follows:

Open Loop: $$H_o(s) = \frac{Ip(R + 1/sc)2\pi K_{voc}}{2\pi s} \qquad G = \frac{1}{M}$$

Closed Loop: $$H(s) = \frac{H_o(s)}{1 + H_o(s)G} = \frac{M(2\zeta\omega_n s + \omega_n^2)}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

The derivation of the closed loop transfer function is shown below:

$$H(s) = \frac{\frac{Ip}{2\pi}(R + \frac{1}{sc})(2\pi\frac{k_{vco}}{s})}{1 + \frac{Ip}{2\pi M}(R + \frac{1}{sc})(2\pi\frac{k_{vco}}{s})}$$

$$= \frac{(\frac{IpRk_{vco}}{sM} + \frac{Ipk_{vco}}{s^2 cM})M}{1 + \frac{IpRk_{vco}}{Ms} + \frac{Ipk_{vco}}{s^2 cM}}$$

$$= M(\frac{\frac{2\zeta\omega_n}{s} + \frac{\omega_n^2}{s^2}}{1 + \frac{2\zeta\omega_n}{s} + \frac{\omega_n^2}{s^2}})$$

$$= M\frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

where $\omega_n = \sqrt{\frac{k_{vco} Ip}{CM}}$

$$\zeta = \frac{R}{2}\sqrt{\frac{k_{vco} IpC}{M}}$$