Design Techniques for High-Temperature
Analog and Mixed-Signal Integrated Circuits

by

Nima Sadeghi

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Abstract

Reliable high-temperature analog and mixed-signal CMOS circuits are required for several applications including aerospace, automotive control, oil field instrumentation, and pulp and paper digesters. In particular, in this work we focus on the design of key building blocks of a miniature sensor interface system that is intended to operate in a pulp and paper digester and collect and record sensory data such as pressure and temperature along its trajectory within the digester. The temperature inside the digester can be as high as 180$^\circ$C.

Design considerations and techniques for implementing these building blocks both at component- and circuit-levels are presented. At the component level, techniques for designing monolithic resistors with a desired temperature coefficient (TC) are proposed, and an analysis on the effects of design parameters such as resistor length, width and the number of fingers on the TC of such multi-finger resistor structures is presented. Furthermore, since the foundry-provided transistor models are typically valid up to 125$^\circ$C, various NMOS and PMOS transistors with different sizes are implemented to study their behaviour at high temperature. Based on our observations, a suitable sizing for transistors is suggested for circuits operating up to 200$^\circ$C. At the circuit-level, several key building blocks such as bias circuits, voltage references and oscillators are designed and proof-of-concept prototypes are implemented in a standard 0.13 µm CMOS process. The operation of the circuits is experimentally validated over the temperature range of interest, namely, 25 to 200$^\circ$C.
Also, a low-complexity resistive and capacitive temperature-compensation techniques for high-temperature relaxation oscillators is proposed. Although the temperature stability of the proposed oscillator (108 ppm/°C) compares favourably with that of state-of-the-art designs, it occupies 0.007 mm$^2$ which is 2.3 × to 114 × smaller than other comparable designs. Also, the proposed circuit operates reliably up to 200°C (as compared to 125°C in other designs).

Although the proposed techniques are only validated using proof-of-concept prototypes in a 0.13 μm CMOS technology, they are general and our preliminary studies on several technologies indicate that the techniques can be implemented in other CMOS technologies as well.
Preface

I, Nima Sadeghi, am the first author and principle contributor of all chapters. All chapters are co-authored with Dr. Shahriar Mirabbasi, who supervised the research and provided technical consultation and editing assistance on the manuscript. The following publications describe the work completed in this thesis. The second journal paper contains material that overlaps with the first conference paper. Chapter 3 is based on the second submitted journal paper which is co-authored by Dr. Iman Sadeghi, who contributed in the programming of the algorithm that is used to optimize the resistor structures. Furthermore, Chapter 5 is based on first submitted journal paper which is co-authored by Alireza Sharif Bakhtiar, who helped with the design and implementation of the oscillator. Professor Chad Bennington who is a co-author on the second conference paper, initiated the research, however, sadly and untimely he passed away on February 14, 2010.

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List of Acronyms

BF  balance factor
BR  balanced resistor
CAD computer-aided design
CMFB common-mode feedback
ESD electrostatic discharge
LF length factor
MEMS micro electro-mechanical systems
MIM metal-insulator-metal
N-TC negative temperature coefficient
NZ-TC near-zero temperature coefficient
P-TC positive temperature coefficient
PTAT proportional to absolute temperature
PSRR power-supply rejection ratio
PVT process, supply voltage, and temperature
SoC system-on-a-chip
SOI silicon-on-insulator
TC temperature coefficient
Z-TC zero temperature coefficient
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To my family,

and

Those who encourage to seek the truth.
An ocean of knowledge is little for a closed-heart man, a drop of knowledge, however, is miracle for a man with open heart to wisdom.

“Anonymous”
Chapter 1

Introduction

1.1 Motivation

Reliable electronic circuits that can operate at high temperature are required for several applications including automotive sensors and electronics, oil field devices, aerospace devices, and multi-phase chemical reactors used in pulp and paper industry. Samples of such applications are shown in Fig 1.1. Our target application for this research is the pulp and paper industry, where there is a need to optimize the digester process operating at temperatures up to 180°C. Such an optimization requires detailed information including time, temperature, and pressure taken from within the digester during its operation.

Figure 1.1: Examples of high-temperature electronic application.
In the context of pulp and paper digesters, our ultimate goal is to have an autonomous flow-following sensor and its interface electronics, referred to as SmartChip, that can be released into the digester, measure and record the required data as it goes through the digester, withstand the harsh conditions (e.g., high temperature), and be retrieved from the reactor for further processing of the recorded data. In order to successfully achieve this goal, the sensor interface requires data acquisition at high temperatures with low power consumption, which introduces new design challenges in terms of temperature stability. The data acquired using the proposed sensor system would facilitate process optimization, with potential increase in digester efficiency of up to 5%. It is worthwhile to mention that in Canada alone, a 1% improvement in digester operation efficiency is worth $80 million/year [1]. Towards achieving this ultimate target, the focus of this research is on the development of design techniques for high-temperature analog and mixed-signal circuits and experimental validation of the proposed techniques.

1.2 High-Temperature Application Specifications

1.2.1 System-on-Chip (SoC) Sensor Interface

Recent research show that high-temperature sensor interface components implemented in standard CMOS processes can operate at temperatures beyond 200 °C [2–9]. These studies have used established technologies such as 0.5-µm bulk CMOS technology with a 5-V supply voltage. Our goal, however, is to build a SmartChip which includes a variety of sensors as well as low-power small-size system-on-chip (SoC) for recording the required data from within a digester. The system has to withstand high temperatures of up to 180 °C for one cycle of digester continuous operation which is in
excess of 8 hours. In the following, we provide more information on the requirements of such design.

1.2.2 Small-Size Requirement

It is envisioned that the SmartChip has a similar size as compared to the real wood chips that are being processed in the digester. The reason is two fold: 1) it is desired that the SmartChips sense the same conditions as the real wood chips and 2) their inclusion in the digester does not disturb the process. Wood chips are typically about (or smaller than) 30 mm × 20 mm × 7 mm [10]. Thus, given that the SmartChip should be packaged with an on-board battery, miniature size of the SmartChip is of paramount importance. Although some electronic components are commercially available that could withstand the harsh environment conditions of digesters, they are typically bulky discrete components and do not satisfy the desired sizing requirement. Furthermore, almost all commercially available high-temperature circuitry use non-CMOS or non-standard CMOS processes which are more expensive than the standard CMOS technologies and they typically use a relatively high supply voltage (5 V or higher). For example, silicon-on-Insulator (SOI) chips which are designed to operate up to 200 °C usually require 5 V and typically consume more than 10 mW per component (and are relatively expensive) [11]. In this application, due to the size restrictions, coin-size batteries are used. The nominal voltage of such batteries is 3 V [1] and thus it is desired to use a technology with a nominal supply of less than 3 V.

1.2.3 Low-Power Requirement

In contrast to previously published results [2–9] a major goal in this design is to minimize the power consumption of the overall SmartChip so that it is able to operate
for more than 8 hours from a small coin-size battery. To minimize the power, while
taking advantage of high level of integration, smaller feature size technologies are more
desirable. Taking the manufacturing cost into account, a 0.13 µm CMOS technology,
is a good compromise for low power, high level of integration and low cost. The
low-power, low-voltage requirements are due to the small size requirements of the
application that demands operation from one or more coin-size batteries. Given that
the nominal voltage of high-temperature coin-size batteries is 3 V [1], and considering
the voltage drop of the regulator, the supply voltage of the design is chosen to be 2.5
V. To extend the operation to beyond 8 hours, we minimize the power consumption
by optimizing the current draw of each block.

1.2.4 System Block Diagram

The SmartChip can be considered as an independent autonomous data acquisition
system for high temperature applications which is composed of three major build-
ing blocks: 1) miniature sensors which are predominantly consist of micro-electro-
mechanical systems (MEMS) and MEMS-based sensors, 2) analog interface circuits,
and 3) digital/mixed-signal blocks, as shown in Fig 1.2.

In this work, we focus on the design, implementation and test of analog interface
blocks of the SmartChip. The MEMS sensors and digital/mixed-signal electronic
blocks are being studied and designed by other members of our team. The analog
interface building blocks of the SmartChip include a bias circuitry, an amplifier, a
voltage reference, and an oscillator.

In this thesis we focus on the analysis and design of the above mentioned building
blocks. To achieve this goal, we study, design, and implement several different size
transistors and different resistor structures to investigate their behaviour and perfor-
mance over the wide temperature range of interest. We propose various architectures for designing temperature-stable resistors. Furthermore, we propose temperature compensation techniques to improve the performance of the building blocks.

Let us first briefly review the effects of (high) temperature on the performance of CMOS electronics and then overview the available and proposed high temperature compensation techniques.

### 1.3 High-Temperature Design Considerations

At high temperature, the circuit blocks shown in Fig. 1.2 present many design challenges that have to be accounted for when implemented in CMOS, including reduced electron/hole mobility, threshold voltages drop, and increased junction leakage currents [12–16]. These issues will be discussed in the following subsections.

![Figure 1.2: SmartChip system block diagram.](image-url)
### 1.3.1 Mobility Variation over Temperature

In silicon material at high temperature, the carrier (electron/hole) mobility is mainly affected by a basic scattering mechanism, called lattice scattering. This means that lattice vibration, while increases with temperature, scatters the charge carrier (electron/hole) [7].

An example of an NMOS channel electron mobility measurement versus temperature reported in [7]) shows that in the temperature range of interest, from room temperature, 27°C (300°K) up to 180°C (453°K), the mobility decreases over temperature. This measured results are fitted to the following simplified model provided by [13].

\[
\mu(T) = \mu(T_0) \left(\frac{T}{T_0}\right)^{-1.5} \quad (1.1)
\]

### 1.3.2 Threshold-Voltage Variation over Temperature

The physical expression for the threshold voltage of a long channel MOS transistor without substrate biasing is given in Equation (1.2) [14].

\[
V_{th} = \phi_{ms} - \frac{Q_{SS}}{C_{OX}} \pm 2\phi_F \pm \gamma_{n,p} \sqrt{2\phi_F} \quad (1.2)
\]

where + sign is for NMOS and - sign is for PMOS devices. Here \(C_{OX}\) is the gate capacitance per unit area, \(\gamma_{n,p}\) is the body-effect constant, \(Q_{SS}\) is the surface-state charge density, \(\phi_F\) is the Fermi potential of the bulk, and \(\phi_{ms}\) is the contact potential difference between the gate and the substrate.

The temperature dependency of the NMOS threshold voltage can be derived by taking the derivative of \(V_{th}\) with respect to temperature as given by [7] as follow:
\[
\frac{\delta V_{th}}{\delta T} = \frac{\phi_{ms}}{T} + \frac{2\phi_F}{T} \frac{\gamma_n}{\sqrt{2\phi_F}} \frac{\delta \phi_F}{\delta T}, \quad (N\text{MOS})
\]

(1.3)

For a typical CMOS process this dependency at room temperature, i.e., 300 °K, results in a value of -3.10 mV/°C for the first term, 2.70 mV/°C for the second term, and -0.4 mV/°C for the last term [7], which show that the threshold voltage of an NMOS transistor decreases when the temperature increases.

On the other hand, the threshold voltage temperature dependency for a PMOS device is given as follow [7]:

\[
\frac{\delta V_{th}}{\delta T} = \frac{\phi_{ms}}{T} - \frac{2\phi_F}{T} - \frac{\gamma_p}{\sqrt{2\phi_F}} \frac{\delta \phi_F}{\delta T} + \frac{1}{T} \left( \frac{E_g}{q} + \frac{3kT}{q} \right), \quad (P\text{MOS})
\]

(1.4)

where \(E_g\) is the energy band of a free electron. For a typical CMOS process this dependency at room temperature, i.e., 300 °K, results in the decreased magnitude of first term which is about -0.5 mV/°C, the negative sign for the second and third terms and an extra added term with a value of about 4.3 mV/°C at 300 °K [17]. As a result for both NMOS and PMOS the absolute value of threshold voltage decreases as temperature increases. Also, we notice that the change of PMOS threshold voltage is a bit more pronounced than that of NMOS.

In general, the absolute value of a MOS threshold voltage decreases as temperature increases. Validated by measurement (and extrapolation of measurement) results as well as analytical equations for threshold voltage, to the first-order of approximation, the temperature dependency of threshold voltage can be expressed as follows [16]:

\[
V_{TH}(T) = p_0 \cdot T + q_0
\]

(1.5)
where \( p_0 \) in \( V/\circ CK \) is a negative value for NMOS transistors and a positive value for PMOS transistors. \( q_0 \) is the threshold voltage of the device at \( 0^\circ K \).

1.3.3 Junction Leakage Current over Temperature

The high temperature variation causes two sources of leakage currents, one is sub-threshold channel leakage current and the other is junction-to-substrate leakage current. The sub-threshold channel leakage current exponentially increased due to decreased threshold voltage and carrier mobility, however, all the building blocks of the SmartChip shown in Fig. 1.2 operate in strong inversion, so we only consider the junction-to-substrate leakage current. This leakage current increases (about 5 orders of magnitude from 25 to 250°C) due to increased intrinsic carrier concentration, \( n_i(T) \) [7].

At room temperature, the leakage current is very small, usually on the order of \( pA \). As temperature rises, two different effects cause the increase of the junction leakage current, drift current and diffusion current as follow:

\[
I_{\text{Leak}} = I_{L,\text{Diffusion}} + I_{L,\text{Drift}} \approx -\frac{qAn_i^2(T)}{N_D} \sqrt{\frac{D_P}{\tau}} - \frac{qAn_i(T)W}{2\tau} V_A
\]

where \( A \) is the area of the \( p - n \) junction, \( V_A \) is the reverse bias voltage, which is negative, \( N_D \) is the \( n - \text{type} \) doping density, \( W \) is the width of the junction depletion region at applied \( V_A \), \( D_P \) is the minority carrier diffusion constant, and \( \tau \) is the minority carrier lifetime. The first term is diffusion current and the second term is drift current.

Drift (generation-recombination) current is due to the thermally generated electron-
hole pairs in the depletion region. This current is proportional to $n_i(T)$, and dominates to temperatures up to 100 – 150°C. It doubles the leakage current for every increase of 10°C based on the formula provided here.

Diffusion current is due to the thermally generated minority carriers away from the junction area. This current is proportional to $n_i^2(T)$ and dominates at higher temperature 150 – 300°C. It, however, quadruples the leakage current for every increase of 10°C.

1.4 High-Temperature Compensation Techniques

The above drawbacks introduce new design challenges. Among the drawbacks, excess leakage current at high temperature causes serious problems [13] such as shifting the operating point in analog circuits, lowering output resistance of high-impedance nodes, being a source of latch up triggering current, or greatly increasing offset among matched devices. It can expedite the loss of charge stored at dynamic nodes or severely reduce circuit performance due to reduced bias current. Depending on the specific requirements, some techniques can be used to decrease the impact of high-temperature leakage currents, including zero temperature coefficient gate biasing, substrate biasing feedback, leakage current feedback cancellation, and constant-$g_m$ biasing [7, 13, 16, 18–20].

For the SmartChip, as explained earlier, to improve battery longevity power consumption must be minimized. However, low DC bias current means increased sensitivity to current variations due to the increased leakage at high temperatures. Therefore, in this work a special attention has been paid to this design trade off. The conventional and proposed temperature compensation techniques are as follows:
1.4.1 Fully Differential Design

In general, single-ended circuits are sensitive to common-mode perturbations such as supply noise or deviations caused by leakage current. A robust circuit architecture that mitigates these common-mode errors is the fully differential structure. Fully differential structures are commonly used in almost all integrated circuit implementations including those for high-temperature designs.

1.4.2 Constant-$g_m$ Biasing Technique

The constant-$g_m$ biasing is a popular technique to implement robust bias circuitry [21] and is also used in high-temperature designs [7] and [8] as a temperature stabilizing technique to mitigate the impact of mobility degradation. In this work, we have modified their proposed circuit and improved the performance of the circuit due to temperature variations which will be discussed in more details later in this thesis.

1.4.3 Proposed Temperature-Stable Resistor Structure

The proposed monolithic structure is a resistor with a desired temperature coefficient (TC) for which no special processing steps are required. Furthermore, it does not require any extra circuitry for temperature compensation that would typically increase the complexity and/or power consumption of the circuit. This technique is based on taking advantage of the temperature behaviour of both contact and core resistors, which are used in on-chip resistors, to control the overall temperature behaviour of the structure.
1.4.4 Proposed Capacitive Compensation Technique

The proposed capacitive compensation technique is a simple feedback-based structure that compensates for the performance degradation of the circuit over a wide temperature range. The proposed approach is presented in the context of an oscillator whose frequency of oscillation is kept stable over a wide range of temperatures by using a varactor which is controlled by the already existing bias voltage in the design and therefore the system only adds a small overhead (due to the addition of the varactor) and does not require any complicated circuitry.

1.5 Summary of Contributions and Thesis Outline

The main objective of this work is to develop design techniques for analog and mixed-signal circuits that have a temperature-stable performance over a wide range of temperature. To validate the proposed techniques, various building blocks of the SmartChip are designed, implemented, and successfully tested over the temperature range of 25 to 200°C. The proof-of-concept circuits are designed in a 0.13 µm CMOS technology. Three chips consisting of various building blocks are designed and fabricated as a proof of concept for the proposed temperature compensation techniques. The design and measurement results are discussed in detail.

In order to mitigate the high temperature impairments, we propose three new techniques which are validated by successful measurement of proof-of-concept designs. These techniques are:

- A modified constant-\(g_m\) bias circuit.
- A monolithic resistor structure that can be designed to have a given TC without
using any extra processing steps during the chip manufacturing.

- A simple capacitive compensation technique using a varactor that is controlled by the variation of a (typically available) bias voltage.

Although the proposed techniques are only validated in a 0.13 \( \mu m \) CMOS technology, they are general and our preliminary studies on several technologies indicate that the techniques can be ported to other CMOS technologies.

The organization of the thesis is as follows. In Chapter 2, we study the behaviour of CMOS transistors at high temperature, and presents the design of bias circuit, amplifier, voltage reference, and a basic concept for implementing resistors with near-zero TC. In Chapter 3, we propose a technique for implementing monolithic resistors with a desired temperature coefficient using standard process steps and analyze the proposed technique. In Chapter 4, we expand the proposed resistor design and provide an analysis of resistor TC sensitivity to length, width, and number of fingers of the proposed multi-finger resistor structure. In Chapter 5, we propose a capacitive temperature compensation technique in the context of a varactor-based temperature compensated oscillator. In Chapter 6, we summarize the research contributions and suggest areas for future work.
Chapter 2

Building Blocks for High Temperature Sensor Interface

The first fabricated chip consists the following designs; different size NMOS and PMOS transistors to study the high temperature behaviour of these devices which is usually not provided by the foundry, two different bias circuits, an amplifier, two different voltage references, and different resistor structures for investigating their temperature behaviour over the temperature range of interest. The die micrograph of the chip is presented in Fig. 2.1.

Since the foundry provided models are not validated at temperatures beyond 125°C, we implemented several different size NMOS and PMOS transistors to study their behaviour at higher temperatures. Comparing the simulation results with measured data, we picked a proper sizing for transistors for which the I-V characteristic of the device matches that of the simulations over a wide range of temperature. The measurements are done for temperatures up to 180°C. In addition a few more building blocks (as mentioned above)

For the high temperature measurement setup, we use a chamber which has a heater for increasing the internal temperature of the closed chamber. We put the chip that is mounted on a test printed-circuit board (PCB) inside the chamber. In order to have access to the pins inside the chamber we use special high temperature wires. To read and control the temperature of the chip, we use a resistance temperature detector (RTD) on top of the chip using thermal paste (for thermal connectivity) and
high temperature tape (for preventing disconnection during measurement). Fig. 2.2 shows this setup before starting a measurement. For measurements, we put the chip inside the chamber, and turn on the heater. The heater has a temperature controller. It turns on and off automatically by comparing the preset target temperature with the temperature of the RTD and adjusts the inside temperature of the chamber. Depending on the number of required measurements, the temperature is kept constant for up to several hours at each target temperature.
2.1 Measure and Validate CMOS Transistor’s Behaviour up to 180°C

Typically, the foundry-provided models for NMOS and PMOS transistors are valid up to 125°C. This is also the case for the 0.13 μm CMOS technology used in this work. Therefore, to investigate the behaviour of transistors at higher temperatures, we have implemented several different size transistors to measure and study their temperature behaviour above 125°C.

2.1.1 Short-Channel Non-idealities versus Large-Size Junction Leakage

Transistor’s length size is a critical parameter in high-temperature design. Assuming a constant aspect ratio, $\frac{W}{L}$, where $W$ is the width and $L$ is the length of the transistor, we compare a minimum-length transistor with a large-length transistor. There is a trade-off between short-channel non-idealities and large size junction leakage at high temperatures. Therefore in high-temperature design it is important to choose a proper transistor length.
2.1.2 Different Length-Size Transistors over Temperature

We have implemented transistors with three different transistor length size. These representative transistors are referred to as a short device ($L = 1.25 \times L_{\text{min}}$), a mid device ($L = 2.5 \times L_{\text{min}}$), and a long device ($L = 12.5 \times L_{\text{min}}$). All these transistors have the same aspect ratio, $\frac{W}{L}$. We measured the $I_D-V_{DS}$ and $I_D-V_{GS}$ characteristics for both NMOS and PMOS transistors for all these different sizes over the temperature range of 25 to 180°C.

2.1.3 CMOS Transistors Simulation and Measurement Results

Figs. 2.3, 2.4, 2.5, and 2.6 compare the simulation and measurement results of $I_D-V_{DS}$ and $I_D-V_{GS}$ of the NMOS transistors with different length sizes at both 125°C and 180°C.

More measurements and simulations at other temperatures have also been performed and the results are showing the same trend. From these representative figures, we notice that the simulation results based on foundry-provided models are in very good agreement with the measurement results for the mid-size transistor ($2.5 \times L_{\text{min}}$).

Thus, we have used the length size of $2.5 \times L_{\text{min}}$ for all the NMOS transistors in this design. The simulation and measurement results for the PMOS transistors also show a similar trend, although for the PMOS transistors the matching between simulation and measurement results (for $I_D-V_{SD}$) improves as the length size of the transistor increases. However, since for a given aspect ratio, the larger the length of the transistor the larger the area occupied by the transistor, to have a reasonable area, we have also chosen the length size of $2.5 \times L_{\text{min}}$ for all the PMOS transistors.

Choosing the proper length size of transistors for high temperature design, in the
Figure 2.3: Simulation and measurement results comparison of $I_D-V_{DS}$ of NMOS transistors at 125°C for $V_{GS} = 1.25$ V and different length sizes with $\frac{W}{L} = 1$.

Figure 2.4: Simulation and measurement results comparison of $I_D-V_{GS}$ of NMOS transistors at 125°C for $V_{DS} = 1.5$ V and different length sizes with $\frac{W}{L} = 1$. 

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Figure 2.5: Simulation and measurement results comparison of $I_D-V_{DS}$ of NMOS transistors at $180^\circ$C for $V_{GS} = 1.25$ V and different length sizes with $\frac{W}{L} = 1$.

Figure 2.6: Simulation and measurement results comparison of $I_D-V_{GS}$ of NMOS transistors at $180^\circ$C for $V_{DS} = 1.5$ V and different length sizes with $\frac{W}{L} = 1$. 
following section, we look at the design of a bias circuit to decrease the impact of high temperature impairments. We explain the design of a proposed constant-$g_m$ bias circuit which is modified for high temperature applications with performance improvement.

2.2 Bias Circuit Design and Implementation

A classic bias circuit for having constant $g_m$ biasing [21] is shown in Fig. 2.7. This structure is ideally independent of supply variation since there is a feedback from the output current, drain current of $M_4$, to sense the reference input, diode-connected $M_3$ [21].

![Generic constant-$g_m$ bias circuit](image)

Figure 2.7: Generic constant-$g_m$ bias circuit.
2.2.1 Temperature Dependency of Constant-\(g_m\) Biasing

Now we want to consider the impact of temperature variation on the output bias current. It can be shown that \(I_B\) in this circuit (assuming long-channel devices and neglecting channel length modulation and the body effect) is given by [21]:

\[
I_B = \frac{2}{\mu_n C_{ox} R_B^2} \left( \sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}} \right)^2. \tag{2.1}
\]

This output current highly depends on temperature because of its dependence to \(\mu_p\), \(C_{ox}\), and \(R_s\).

In the other hand, the transconductance \(g_m\) of devices is a critical parameter affecting gain, bandwidth, and stability of analog circuits including amplifiers. Therefore, it is important to minimize \(g_m\) variations over the desired temperature range of operation. It is well-known that the \(g_m\) of a MOS transistor in saturation region, assuming long-channel devices and neglecting channel length modulation and the body effect, is given by [21]

\[
g_m = \sqrt{2 \mu_n C_{ox}\left(\frac{W}{L}\right) I_D}. \tag{2.2}
\]

Since \(g_m\) is proportional to mobility, and based on Eq. (2.1) the bias current is inversely proportional to the mobility, then the \(g_m\) of any transistor whose bias current is derived from such current is ideally independent of the mobility. From Eqs. 2.1 and 2.2, the \(g_m\) of \(M_2\) is given by

\[
g_{m2} = \frac{2}{R_B} \left( 1 - \frac{1}{\sqrt{K}} \right). \tag{2.3}
\]

where \(K\) is \(\frac{W_2/L_2}{W_1/L_1}\). Thus \(g_{m2}\) to the first order of approximation is independent of the
bias current, and is inversely proportional to $R_B$. Hence, although the bias current would increase due to change in the temperature, $g_m$ would ideally be stable over temperature if the bias resistor, $R_B$, has a zero temperature coefficient (TC). This is the task of the classic constant-$g_m$ bias circuit of Fig. 2.8.

### 2.2.2 Temperature Compensated Constant-$g_m$ Bias

![Bias Circuit Diagram](image)

Figure 2.8: (a) Bias circuit using constant-$g_m$ biasing. (b) our modification; using two resistors in series with negative and positive TC.

Fig. 2.8 presents our fabricated design of the biasing circuit with the proposed temperature compensation technique. In [8], the main core of the circuit of Fig. 2.8. (a) has been used and with acceptable performance has been reported when $R_B$ is implemented using a conventional poly resistor with TC of about $1000 \text{ppm/}^\circ\text{C}$. In
this work, we further improve the performance by using an alternative implementation for this resistor.

First, in the 0.13\(\mu\)m CMOS technology that we are using, a resistor with TC on the order of 100 ppm/°C is available. Using this resistor which is less sensitive to temperature further improves the temperature stability of the circuit. Second and a more important modification is the realization of \(R_B\) using a series combination of two different type of resistors, one with a positive TC and another with a negative TC (the magnitude of their temperature coefficients differ by a factor of two), thus using a proper ratio of resistors we minimize the effective TC of the series combination, as shown in Fig. 2.8(b). Implementing these two modifications, the temperature stability of the circuit has been improved.

We can think of an alternative approach in which we use the same topology shown in Fig. 2.8, but we try to make the bias current constant rather than \(g_m\). If we again consider Eq. 2.1, we notice that \(I_B\) has two temperature dependent parameters; \(\mu_n\) and \(R_B^2\). We know that \(\mu_n\) decreases over temperature as we discussed in previous section on Eq. 1.1, hence to make \(I_B\) constant we can use a biasing resistor, \(R_B\), which has a positive temperature coefficient. We designed and implemented the circuits of both constant-\(g_m\) and constant-\(I_B\) approaches which will be discussed in more details in the following.

2.2.3 Bias Current Comparison of Constant-\(g_m\) and Constant-\(I_B\)

We simulated the circuit shown in Fig. 2.8 to obtain \(I_B\) vs temperature. The bias current \(I_B\) changes from 10.3 \(\mu\)A at room temperature (25°C) and almost linearly increases to 13.05 \(\mu\)A at 125°C. Based on Eq. 2.1, the reason for such linear increase in \(I_B\) for constant-\(g_m\) approach, while we almost keep \(R_B\) value constant using a series
combination of positive and negative TC Resistors, is the $\mu_n$ temperature behaviour which is decreasing as mentioned on Eq. 1.1. In comparison, the same bias current in [7] varies from $\sim 9$ $\mu$A to $14\mu$A for the same temperature range. Both result reported in [7] and our result are based on simulations. In [8], the measured bias current varies from $\sim 15$ $\mu$A to $20\mu$A over the same temperature range.

![Figure 2.9: Comparison of $I_{bias}$ versus temperature between constant-$g_m$ and constant-$I_B$ approaches.](image)

Next, we compare the constant-$g_m$ and constant-$I_B$ approaches. In this simulation we decrease the amount of bias current to achieve a lower power consumption. In the constant-$g_m$ approach, the bias current $I_B$, shown in Fig. 2.9, presents the same characteristic as previous simulation. $I_B$ changes from $6.4$ $\mu$A at room temperature ($25^\circ$C) and almost linearly increases to $8.2$ $\mu$A at $125^\circ$C. The $I_B$ variation over this temperature range in the constant-$g_m$ approach is about $1.8$ $\mu$A. The $g_m$ variation over this temperature range is about $5$ $\mu\Omega^{-1}$ from $82.51$ to $77.55$ $\mu\Omega^{-1}$. The reason
for this minor variation of $g_m$ is due to overall temperature coefficient of $R_1$ and $R_2$ in series which is not absolutely zero.

The other curve in Fig. 2.9, however, illustrates the characteristic of the constant-$I_B$ approach. As we mentioned we use a positive temperature coefficient biasing resistor for $R_B$ to compensate the negative temperature coefficient behaviour of $\mu_n$ in Eq. 2.1. $I_B$ obtain its minimum value of 6.26 $\mu$A at room temperature (25°C) and its maximum value of 6.68 $\mu$A at around 85 – 90°C. This $I_B$ variation over the temperature range of 25 – 125°C in the constant-$I_B$ approach is about 0.42 $\mu$A which is less than 1/4 of that of constant-$g_m$ approach, 1.8 $\mu$A.

The performance summary of bias circuits presented here and in [7] (simulation level) as well as [8] (implementation level) is presented in Table 2.1.

<table>
<thead>
<tr>
<th>Design</th>
<th>Const-$g_m$</th>
<th>Const-$I_B$</th>
<th>[7] (Sim.)</th>
<th>[8] (Mes.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology ($\mu$m)</td>
<td>0.13</td>
<td>0.13</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>$V_{dd}$ (V)</td>
<td>2.5</td>
<td>2.5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>$I_B$ ($\mu$A) from 25 to 125°C</td>
<td>6.4 to 8.2</td>
<td>6.26 to 6.68</td>
<td>9 to 14</td>
<td>15 to 20</td>
</tr>
</tbody>
</table>

Table 2.1: Bias circuit performance comparison.

Both of our constant-$g_m$ and constant-$I_B$ approaches show a lower power consumption as well as a lower temperature variation compared to what reported by [8] and [7]. It should be noted that in the constant-$g_m$ approach, even if we assume that Eq. 2.3 (which is based on simplified quadratic relation between the drain current and gate-source voltage of the transistors,) is valid, the value of $g_m$ will change due to temperature variation. This is due to the fact that $R_B$ changes with temperature. In our design, the value of $g_m$ based on Eq. 2.3 changes from 65.4 to 50.1 $\mu\Omega^{-1}$ when the temperature changes from 25 to 180°C. This variation in $g_m$ for the main part is attributed to variation of $R_B$ due to temperature. Although $R_B$ is a combination
of a NTC resistor in series with a PTC resistor, the overall TC of R is still not neg-
ligible since it is challenging to completely match the TC of NTC and PTC resistor
components over a wide temperature range. This has been our motivation behind
the approach presented in Chapter 3 where we present a technique for designing
monolithic resistors with a desired temperature coefficient over a wide temperature
range.

Using the proposed temperature compensated constant-$g_m$ bias circuit in other
analog blocks of SmartChip, we improve the temperature performance of each indi-
vidual block. In the following section we consider the design and performance of the
proposed high temperature amplifier.

2.3 Amplifier Design and Implementation

Almost all analog blocks shown in Fig. 1.2 have an amplifier including the voltage
reference and the oscillator. Based on the design requirements for different blocks,
different structures will be used. The amplifier open-loop block diagram shown in
Fig. 2.10, consists of a core amplifier, a bias circuit and a switch-capacitor common-
mode feedback. We used the constant $g_m$ bias topology for the bias circuit.

2.3.1 Folded-Cascode Temperature Compensated Design

Since a relatively large-gain amplifier is desired (so that when the gain drops due to
temperature increase [6, 22] it still has sufficient gain) and also it should be capable
of driving capacitive loads (e.g., input capacitance of the ADC), a fully differential
folded-cascode topology [21], shown in Fig. 2.11, with a classic switched-capacitor
common-mode feedback (CMFB) circuit is chosen. This structure has been shown to
operate at high (225 °C) temperatures [6]. It also provides good stability performance and has lower voltage headroom requirement compared to the telescopic structure [21]. For the output stage, however, a two-stage amplifier might perform better in terms of large output swings due to the low voltage limitation. An amplifier with NMOS input pair is chosen to to achieve larger $g_m$ with reasonable device sizes. All amplifier bias voltages are generated using the bias circuit shown in Fig. 2.8.(a).

### 2.3.2 Switched-Capacitor Common Mode Feedback (CMFB)

The CMFB circuit maintains the common-mode output voltage around $\frac{V_{dd}}{2}$ and is shown in Fig. 2.12.(a). Its functionality at high temperature is confirmed in [6]. Here, $V_{p\text{bias}}$, provided from the bias circuit is used in CMFB circuit to adjust $V_{c\text{mfbPbias}}$ for controlling the bias voltage of the $M_{9-10}$ of the amplifier. All the switches in this figure are CMOS transmission gates, shown in Fig. 2.12.(b). The constant $g_m$ biasing circuit is also used to generate $V_{CM} = \frac{V_{dd}}{2} = 1.25 \, V$. As shown in the simulation section the output common-mode voltage will settle to the desired voltage of 1.25 V after about 8 clock cycles.
2.3.3 Amplifier Frequency Response over Temperature

The amplifier is simulated over the temperature range from 25°C to 125°C. At 125°C the bias currents, $I_{REF1}$, $I_{REF2}$ and $I_{REF3}$, shown in Fig. 2.11 are 60, 64, and 124 µA, respectively. Note that the larger the bias currents, the less sensitive the performance of the circuit to the increase of leakage at high temperature. Hence, there is a trade off between power performance and temperature stability. The magnitude frequency response of the amplifier at 25°C (and 125°C) are shown in Fig. 2.13. The open-loop DC gain is 72 dB (69 dB) and the unity gain bandwidth of the amplifier is 4.25 MHz (4.13 MHz). The phase margin is relatively insensitive to temperature and is greater than 86° over the temperature range as shown in Fig. 2.13.
Figure 2.12: Switched-capacitor CMFB.

Figure 2.13: Amplifier frequency response; open-loop gain and phase margin over the temperature range from 25 °C to 125 °C.
In [7], $I_{REF1}$, $I_{REF2}$ and $I_{REF3}$ are chosen as 180, 270, and 450 $\mu$A at 125°C and the simulated open-loop gain of the amplifier is 57 dB.

2.3.4 Amplifier Transient Response at High Temperature

The amplifier transient response at 125°C is shown in Fig. 2.14.

![Amplifier Transient Response](image)

Figure 2.14: Amplifier transient response at 125°C. The CMFB gradually sets the common-mode of the output to the desired value of $V_{dd}/2 = 1.25$ V.

In this figure, 100 Hz input signal is used. The common-mode of the output voltage, at the beginning is close to the ground due to the higher leakage current of NMOS as compared to that of PMOS transistors at 125°C. However, the CMFB circuit gradually sets the common-mode of the output to the desired value of $V_{dd}/2 = 1.25$ V.

Table 2.2 summarizes the performance of the presented amplifier and compares it with that of [8] and [7]. Here, the variations of $I_B$ correspond to the temperature range from 25°C to 125°C, however, based on the measurement results presented in [8], this current continues to increase (approximately) linearly as temperature goes
beyond 125 °C (up to approximately 200 °C). Given the similarity between the structure of the amplifier presented here and that of [8], it is expected that $I_B$ increases to 14.6 μA, $DC_{gain}$ remains above 67 dB, and the amplifier remains functional as temperature increases to 180 °C.

### 2.3.5 Amplifier Performance and Comparison

A performance comparison between the above mentioned amplifier and that of [7] (simulation level) as well as [8] (implementation level) is presented in Table 2.2.

<table>
<thead>
<tr>
<th>Design</th>
<th>This Work</th>
<th>[7] (Sim.)</th>
<th>[8] (Mes.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (μm)</td>
<td>0.13</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>$V_{dd} (V)$</td>
<td>2.5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>$I_{REF3} (μA)$ at 125 °C</td>
<td>124</td>
<td>450</td>
<td>N.A.</td>
</tr>
<tr>
<td>Amp. Power (mW) at 125 °C</td>
<td>0.62</td>
<td>4.5</td>
<td>N.A.</td>
</tr>
<tr>
<td>$I_B (μA)$ from 25 to 125 °C</td>
<td>10.3 to 13.05</td>
<td>9 to 14</td>
<td>15 to 20</td>
</tr>
<tr>
<td>$DC_{gain} (dB)$ at 125 °C</td>
<td>69</td>
<td>57</td>
<td>56</td>
</tr>
</tbody>
</table>

Table 2.2: Amplifier performance comparison.

Notice that the power improves by $\frac{5(V) \cdot 450(μA)}{2.5(V) \cdot 124(μA)}$, which is more than 6 times. The results from [8] shows the same bias current variation as [7] shifted to 15-20 μA for the same temperature variation, however, this results are at implementation level.

This proposed high temperature amplifier is used as one of the building blocks required for the voltage reference which is discussed in the following section.

### 2.4 Voltage Reference Design and Implementation

The voltage reference is responsible to generate a dc voltage that is practically independent of process, supply voltage, and temperature (PVT) variations. A popular
technique to generate an almost constant voltage over a wide temperature range is based on exploiting two different electrical characteristics; negative temperature coefficient (N-TC) voltage and positive temperature coefficient (P-TC) voltage. By adding these two components together with a proper scaling, one can obtain a practically constant voltage reference. This is a fundamental idea behind bandgap voltage references [21]. These voltage references typically rely on the fact that the bipolar base-emitter voltage has a negative TC characteristic, and the difference between the base-emitter voltage of two bipolar transistors, i.e., $\Delta V_{BE}$, with unequal bias currents is proportional to absolute temperature (PTAT).

Several state-of-the-art CMOS voltage reference designs have been presented in the literature in silicon-on-insulator (SOI) [23, 24] as well as bulk CMOS [25–38]. All these bulk CMOS circuits operate below 150°C. This temperature limitation can be attributed to the the extensive leakage current, due to the diffusion of thermally generated minority carriers, that becomes dominant around 150°C [5] and causes performance degradation.

Many state-of-the-art high-temperature voltage references use trimming capability to compensate for the temperature variations by minimizing the temperature sensitivity of the circuit [25–35]. Proper trimming of such voltage references requires calibration (which in turn requires some specific amount of time for each temperature interval). In some applications, e.g., for statistical analysis or data fusion of multiple sensory circuits, the calibration and test time may be too time consuming and/or non-practical to perform on every chip. Thus, in such applications a design without any post-manufacturing trimming [36–38] is preferred.

Fig. 2.15 shows a simplified block diagram of the voltage reference. In this section, we present the design and measurement results of a high temperature bandgap
voltage reference and compare its performance with recent designs. In this design, the proposed folded-cascode amplifier and the modified constant-\(g_m\) bias circuit [39] are used.

![Voltage Reference Block Diagram](image)

**Figure 2.15:** Designed voltage reference block diagram.

### 2.4.1 CMOS Bandgap Reference for High Temperature

Fig. 2.16 shows the schematic diagram of a generic bandgap voltage reference. It consists of a bandgap core circuitry, a high-gain amplifier as well as a bias circuit (not shown in the figure for the purpose of brevity). The opAmp ensures that the voltage at \(X\) is equal to the voltage at \(Y\). So by applying the KVL over the loop of Q1, R1 and Q2 we can find that the voltage of R1 is equal to \(\Delta V_{BE}\). Thus in this branch we add a N-TC voltage, base-emitter voltage of Q2, with a P-TC voltage, R1 voltage.

In order to ensure that the voltage at \(X\) is equal to the voltage at \(Y\) in Fig. 2.16, we need a high open-loop gain opAmp. Therefore one of the important design factors is the temperature behaviour of the operational amplifier, particularly, that of its bias circuit. In this design, the above mentioned folded-cascode amplifier with a
temperature-compensated constant-$g_m$ biasing circuit [39] is used for the operational amplifier shown in Fig. 2.16.

It can be shown [21] that the output voltage is:

$$V_{REF} = V_{BE6} + \frac{R_2}{R_1} V_T \ln n$$

(2.4)

where $V_{REF}$ is the output voltage, $V_{BE6}$ is the base-emitter voltage of $Q_6$, $R_1$ and $R_2$ are resistors shown in Fig. 2.16, and $V_T$ is the thermal voltage, and $n$ is the size ratio of $Q_2$ to $Q_1$. Note that in this equation, the first term has an N-TC while the
second term has a P-TC (or is PTAT). Although the resistors are each temperature dependent, their ratio is a weak function of temperature and therefore, it has a minor impact in the temperature behaviour of the overall system. [21].

For the current mirror circuit shown in Fig. 2.16, PMOS transistors are used to take advantage of their lower leakage current as compared to that of NMOS [5] at high temperatures. As mentioned before, the size of the transistor, in particular its length, is a critical design parameter in high-temperature design as there is a trade-off between short-channel non-idealities and junction leakage at high temperatures. Considering this trade-off and based on our previous discussion, we have used the length size of $2.5 \times L_{\text{min}}$ for all the transistors in this design.

We first present the measurement results of the bias circuit and compare the results for both conventional and the modified resistors. Then we present the measurement results of the voltage reference and compare the performance of the proposed circuit with that of recent non-trimming voltage references.

### 2.4.2 Bandgap Bias Resistor Measurement Results

For the proposed voltage reference, we consider both conventional and modified constant-$g_{m}$ bias circuits shown in Fig. 2.17.

We compare the measurement results of the temperature behaviour of the bias resistor over the temperature range of 25 to 200°C for both conventional and the modified resistor used in this design (Fig. 2.18).

As can be seen from the figure, for the conventional bias resistor, namely, $R_{b\text{-Conventional}}$, the resistance varies from 10.44 kΩ to 15.49 kΩ over the temperature range of 25 to 200°C. However, for the modified resistor (two different types of resistors, one with P-TC and the other one with N-TC, in series), denoted as $R_{b\text{-}}$
Modified, the resistance varies from 8.96 kΩ to 11.71 kΩ. Thus measurement results confirm that the Rb-Modified variation over temperature is smaller than that of a conventional resistor. One can further improve this temperature compensation to achieve a (near) zero TC resistor by using different size or if available different type of resistors for the series resistors, or the technique proposed in [40].

In the following sections, the measurement results of the proposed voltage reference (shown in Fig. 2.16) are presented. Furthermore, we compare the performance
Figure 2.18: Measurement comparison of the bias resistor over the temperature range of 25 to 200 °C for both conventional and the modified resistor used in the constant-\(g_m\) bias circuit.

of the proposed circuit with that of recent non-trimming voltage references.

### 2.4.3 Measured Output Voltage over Temperature

Both simulated (based on the results of Fig. 2.18) and measured results of the output voltage of the proposed circuit over the temperature range of 25 to 200 °C are presented in Fig. 2.19. The power supply is set to the nominal value of 2.5 V. From the measurement results, the \(V_{\text{ref}}\) changes from 1.218 V at 25 °C to 1.182 V at 200 °C, that is, about 36 mV variation. The measured results correspond to a temperature coefficient (TC) of 171 ppm/°C. Note that from Fig. 2.19, the impact of the extra leakage current above 150 °C \[5\] is clear as the measured output voltage drops more rapidly when the temperature goes beyond 150 °C. Also, note that the slope (varia-
Figure 2.19: Simulated and measured output of the proposed voltage reference over the temperature range of 25 to 200°C.

2.4.4 Measured Output for ±20% Supply Variation over Temperature

Fig. 2.20 presents the measured output voltage of the circuit as a function of temperature when the power supply changes by ±20%. For supply voltages above 2.5 V, the output voltage profile versus temperature remains reasonably the same, while, for voltages below 2.5 V, the low supply voltage results in more performance degradation.

2.4.5 Measured Output for Different Temperatures over Supply Voltage

In Fig. 2.21, the graph of measured output voltage versus supply voltage (changing from 2 to 3 V) for different temperatures values is presented.

At room temperature, i.e., 25°C, if $V_{DD}$ changes from 2 to 3 V, the voltage reference output changes about 20 mV. As temperature increases, the output variations
Figure 2.20: Measured output of the proposed voltage reference for different $V_{DD}$ values over the temperature range of 25 to 200℃.

Figure 2.21: Measured output of the proposed voltage reference for different temperature values versus supply voltage.
also increase. At 200°C the output variation increases to 60 mV.

2.4.6 Measured Power-Supply Rejection Ratio over Frequency

Fig. 2.22 presents the measured power-supply rejection ratio (PSRR) of the circuit. This measurement is for the worst case, (high) temperature, under the conditions of a 2.5 V supply, 100 mV signal, and without any filtering capacitor.

Figure 2.22: Measured PSRR of the proposed voltage reference at 180°C using a 2.5 V supply voltage with a 100 mV signal, $V_s$.

At 180°C the PSRR at 10 Hz is −32 dB. The PSRR reaches to −63 dB at 1 kHz. The PSRR is almost constant and is below −60 dB, from 1 kHz up to 1 MHz, and it
increases to $-35$ dB at 10 MHz. In comparison, a recent non-trimming reference [36] (although the temperate of the PSRR test is not indicated), achieves a PSRR of $-41$ dB at 10 Hz and stays relatively constant around $-29$ dB up to 1 MHz and increases to $-10$ dB PSRR at 10 MHz.

2.4.7 Voltage Reference Performance Summary

The proposed voltage reference performance is summarized in Table 2.3. Furthermore, for the purpose of comparison, the performance summary of other state-of-the-art non-trimming designs are also included in the table. Note that [37] is using triple-well technology while [38] is operating in the sub-threshold region, and both are operating over a narrower temperature range than the proposed circuit. In this table, the proposed CMOS voltage reference is the only design that operates up to temperature of 200 °C. As discussed earlier and shown in Fig. 2.19, beyond 150 °C the slope of output voltage variation increases due to the extra leakage current. The relatively large TC of the proposed design can be attributed to operating beyond 150 °C.

<table>
<thead>
<tr>
<th>Voltage Reference</th>
<th>This Work</th>
<th>[36]</th>
<th>[37]</th>
<th>[38]</th>
</tr>
</thead>
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<tr>
<td>CMOS ($\mu$m)</td>
<td>0.13</td>
<td>0.35</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>Area ($mm^2$)</td>
<td>0.015</td>
<td>0.021</td>
<td>0.085</td>
<td>0.024</td>
</tr>
<tr>
<td>$V_{DD}$ (V)</td>
<td>2.5</td>
<td>2</td>
<td>0.95</td>
<td>0.85</td>
</tr>
<tr>
<td>$V_{ref}$ (V)</td>
<td>1.22</td>
<td>0.8</td>
<td>0.75</td>
<td>0.22</td>
</tr>
<tr>
<td>Current ($\mu A$)</td>
<td>357</td>
<td>400</td>
<td>10</td>
<td>4</td>
</tr>
<tr>
<td>Temperature (°C)</td>
<td>25-200</td>
<td>0-80</td>
<td>-45-105</td>
<td>20-120</td>
</tr>
<tr>
<td>TC (ppm/°C)</td>
<td>171</td>
<td>104</td>
<td>131</td>
<td>272</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>2-3</td>
<td>2-3.5</td>
<td>1-3</td>
<td>0.9-2.5</td>
</tr>
<tr>
<td>Line Reg. (%/V)</td>
<td>1.6</td>
<td>0.9</td>
<td>–</td>
<td>0.6</td>
</tr>
<tr>
<td>PSRR (dB)@10 Hz</td>
<td>$-32$</td>
<td>$-41$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PSRR (dB)@1 MHz</td>
<td>$-60$</td>
<td>$-29$</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 2.3: Performance comparison of non-trimming voltage references.
The design and implementation of a high-temperature voltage reference in a standard 0.13 µm CMOS technology is discussed. The voltage reference provides a 1.22 V output from a nominal 2.5 V supply. Measured results show that the circuit provides a line regulation of 1.6 to 5.2 %/V over the temperature range of 25 to 200°C and the supply range of 2 to 3 V. To find the proper size (in particular length) of transistors, the I-V curves of different size transistors over the temperature range of interest 25 to 200°C is measured and it is shown that by choosing a particular length the temperature behaviour of transistors can be well modelled with foundry-provided models. Furthermore, to improve the temperature stability of the biasing circuit, two different types of monolithic resistors with P-TC and N-TC are used in series to minimize the overall TC of the bias resistor in the constant-\(g_m\) biasing circuit of the voltage reference. The circuit achieves a temperature coefficient of 171 ppm/°C over the temperature range of 25 to 200°C. The maximum power consumption is 892 µW and the circuit occupies 0.015 mm².

In the following section we present a novel technique to implement monolithic resistors with Near-Zero Temperature Coefficient (NZ-TC) to improve even more the above temperature compensation technique for a bias resistor.

2.5 Implementing Monolithic Resistors with Near-Zero TC

The technique presented in this work takes into account the temperature behaviour of the contact resistors to obtain a better temperature compensation. We propose to implement an NZ-TC resistor using only one type of resistor with P-TC core resistance and N-TC contact resistance. The validity of the proposed idea is confirmed using measurement results. first we describe the proposed NZ-TC resistor design technique
and then measurement results are presented.

### 2.5.1 The Proposed Design Technique

To minimize the resistance variation of a resistor over temperature, it is desired to implement a resistor with (near) Z-TC using the available resistor structures in any given technology. As discussed, it is advantageous if only one specific type of resistor is used. To do so, in addition to the temperature behaviour of the core resistor, one should also consider the temperature behaviour of its contacts.

Typically, the resistance of every on-chip resistor consists of two physical components: a core resistance, $R_{cor}$, and a contact resistance, $R_{cnt}$. Each physical part has its own resistivity and temperature property. In a typical technology, such as the 0.13 µm CMOS technology used in this work, if $R_{core}$ is a poly resistor it has a P-TC while the $R_{cnt}$ of the contacts has a N-TC. Thus, the overall resistor can potentially take advantage of the opposite TC property of its two components to achieve a temperature-stable behaviour.

Assume the following two resistors: one resistor is made of a long poly resistor with contact areas at each end and another one is a series of several shorter poly resistors with contacts at each end of each poly resistor. The former is referred to as $R_{long}$ while each component of the latter is referred to as $R_{short}$. Without loss of generality, assume $R_{short}$ is a resistor with the minimum-length and minimum-width allowed by the technology.

Note that in a typical resistor, contact resistance is usually (much) smaller than the poly resistance, therefore, one can increase the number of contacts to take advantage of their temperature property without any significant effect on the overall resistance. Since $R_{cor}$ has P-TC and $R_{cnt}$ has N-TC property, we propose to implement an
arbitrary temperature stable resistor, $R_{tot}$, as a series combination of one long resistor, $R_{long}$, with a proper length and $n$ series $R_{short}$ resistors as shown in Fig. 2.23.

![Diagram](image)

Figure 2.23: $R_{tot}$ example; series combination of $n = 5$ $R_{short}$ resistors with a $R_{long}$ having a length of 11.25 times minimum-length.

To compensate the P-TC of $R_{corr}$, one can include more $R_{cnt}$ with N-TC. If the resistance of $R_{long}$ is small, i.e., for a small $R_{long}$, the TC of $R_{cnt}$ in $R_{long}$ would be dominant and a negative TC is obtained. For a larger $R_{long}$ the $R_{corr}$ TC would be dominant and a positive TC is obtained. Note that typically $R_{long}$ has P-TC and single $R_{short}$ has N-TC. The larger the $R_{long}$ the more its positive TC. Therefore, for a given value of $R_{tot}$, one can design a temperature-stable resistor by dividing it into an $R_{long}$ and series combination of $R_{short}$ resistors while choosing an appropriate length for $R_{long}$ and proper number of $R_{short}$ resistors, $n$.

To evaluate this technique, several resistor structures are implemented using different $R_{long}$ lengths and different $n$ for $R_{short}$ structures. Also, different structures of
short and long resistors in series are implemented to confirm the temperature performance improvements of the proposed approach. Measurement results (presented in next section) confirm the validity of the proposed technique.

For all results presented in this section, the variation of the resistance of the resistor under test over the temperature range of 25 to 200°C is measured. Without loss of generality, for all resistor structures, we use the minimum width. Only measurement results are presented in this section since the computer-aided design (CAD) tool simulations ignore the impact of contact resistance and its temperature coefficient. It is, however, possible to develop a new model based on the measured values to improve the fidelity of the simulation results.

First, we present the measurement results of two typical resistors (a stand alone resistor as well as a series combination of two different types of resistors with N-TC and P-TC used in [39]). Then, we present the measurement results of the proposed technique and compare them with those of the above mentioned resistors.

2.5.2 Temperature Stability Comparison of the Proposed Resistor with Two Typical Resistor Designs

The measurements shown in Fig. 2.24 illustrate the temperature stability of the proposed resistor as well as two typical resistors over the temperature range of 25 – 200 °C.

The resistance of the one that consist of only a P-TC resistor, conventional resistor, varies from 10.44 kΩ to 15.49 kΩ over the entire temperature range. The second plot in this figure is for a structure which consists of two different types of resistors one with P-TC and the other one with N-TC to achieve an NZ-TC resistor. Measurement shows that the resistor variation in the second structure is less than that of a single
resistor, however, its resistance change is still relatively large. The resistor varies from 8.96 kΩ to 11.71 kΩ over the entire temperature range of 25 to 200°C. This variation is about 2.74 kΩ (relative change of 30% with respect to its nominal value). The proposed approach, however, provides a resistor with ~2 orders of magnitude less resistance change over the same temperature range.

2.5.3 P-TC Behaviour of Different Lengths $R_{long}$

The measurements presented in Fig. 2.25 provide the variation of two $R_{long}$ resistors with different lengths over the temperature range. One $R_{long}$ has a nominal value of 3.2 kΩ and its length is $11.25 \cdot L_{min}$, while the other one has a nominal value
of 5.6 kΩ and its length is $20 \cdot L_{\text{min}}$. The former varies from 3.178 kΩ to 3.204 kΩ, corresponding to the change of 26 Ω over the temperature range. While the 5.6 kΩ $R_{\text{long}}$ varies from 5.563 kΩ to 5.661 kΩ, corresponding to 98 Ω change over the same temperature range. This difference of resistance changes is due to the different lengths of the resistor, however, both results show the expected P-TC behaviour of $R_{\text{long}}$ resistor.

Figure 2.25: Measured $R_{\text{long}}$ for two different lengths of 11.25 and 20 times minimum length resistors versus temperature.

### 2.5.4 N-TC Behaviour of $R_{\text{short}}$ with Different $n$, Resistors in Series

The measurements presented in Fig. 2.26 provide the variation of four different $R_{\text{short}}$ resistors versus temperature. The resistors are 2.9 kΩ, 5.3 kΩ, 5.9 kΩ, and 8.2 kΩ with $n = 8$, $n = 14$, $n = 15$, and $n = 22$, respectively. The measured results are summarized in Table. 2.4.
Figure 2.26: Measured $R_{\text{short}}$ for four different values for $n = 8$, $n = 14$, $n = 15$, and $n = 22$ versus temperature.

| $R_{\text{short}}$ (kΩ) | $R @ 25 \degree C$ (kΩ) | $R @ 200 \degree C$ (kΩ) | $\Delta R$ (Ω) | $|\Delta R/R|$ |
|--------------------------|--------------------------|--------------------------|----------------|----------------|
| 2.9                      | 2.997                    | 2.913                    | -84           | 2.9 %          |
| 5.3                      | 5.359                    | 5.225                    | -134          | 2.6 %          |
| 5.6                      | 5.693                    | 5.550                    | -143          | 2.6 %          |
| 8.2                      | 8.356                    | 8.138                    | -218          | 2.7 %          |

Table 2.4: Measured results of resistors shown in Fig. 2.26.

The last column of this table shows that all of these $R_{\text{short}}$ resistors provide about the same relative change, i.e., $|\Delta R/R|$, over the temperature range of interest, while they all show an N-TC behaviour. This approximately constant relative change can be attributed to the fixed ratio of core resistance and contact resistance for all of these $R_{\text{short}}$ resistors.
2.5.5 Comparing Temperature Behaviour of a Given $R_{tot}$ with Different $R_{long}$ or $R_{short}$ Implementation

Fig. 2.27 presents the measurement results of $\sim 3$ kΩ resistor using different structures: (1) $R_{long}$ with a length of $11.25 \cdot L_{min}$, and (2) $R_{short}$ with $n = 8$ structures. As can be seen, the $R_{long}$ resistor shows a P-TC and the $R_{short}$ resistor shows a N-TC.

![Figure 2.27: Measured resistance of $\sim 3$ kΩ using $R_{long}$ with a length of $11.25 \cdot L_{min}$ and $n = 8$ $R_{short}$ structures versus temperature.](image)

Fig. 2.28 shows the behaviour of another $R_{long}$ and two other $R_{short}$ structures for resistor valued around 5.6 kΩ. Again the $R_{long}$ resistor shows a P-TC and $R_{short}$ resistors show a N-TC. The two $R_{short}$ structures differ in their value of $n$, 15 versus 14, and hence the one with smaller $n$ has a nominal value of $\sim 5.3$ kΩ. Note that, as expected, both $R_{short}$ resistors show approximately the same N-TC behaviour over
Figure 2.28: Measured resistance of a 5.6 kΩ $R_{long}$ structure and 5.6 kΩ and 5.3 kΩ $R_{short}$ structures versus temperature.

The measured results presented in Fig. 2.29 are for temperature behaviour of three different resistors: (1) $R_{short}$ with $n = 22$, (2) 14 $R_{short}$ in series with $R_{long}$ with length $11.25 \cdot L_{min}$, and (3) 8 $R_{short}$ in series with $R_{long}$ with length $20 \cdot L_{min}$ (refer to Fig. 3.2). In this example, the goal is to implement a temperature-stable resistor with a value of $\sim 8.5$ kΩ.

As a first step, consider the 8.2 kΩ $R_{short}$ structure with $n = 22$ from Table. (2.4). It varies from 8.356 to 8.138 kΩ over the temperature range. The next step is to de-
crease $n$ of $R_{\text{short}}$ structure, which only decrease the resistor value without changing its N-TC characteristic, and then use a $R_{\text{long}}$ resistor with P-TC in series to compensate that N-TC behaviour. Therefore, an $R_{\text{short}}$ with $n = 14$ and an $R_{\text{long}}$ with length of $11.25 \cdot L_{\text{min}}$ in series are chosen. The overall temperature behaviour improved as shown in Fig. 2.29. This result can be further improved by again decreasing the $n$ of $R_{\text{short}}$ and increasing the length of $R_{\text{long}}$. The final resistor structure here consists of an $R_{\text{short}}$ with $n = 8$ in series with an $R_{\text{long}}$ with $20 \cdot L_{\text{min}}$. The resulting resistor varies from $8.560 \, \text{k\Omega}$ to $8.592 \, \text{k\Omega}$ with absolute change of $\sim 32 \, \Omega$ and relative change
of 0.37 % over the temperature range of 25 to 200 °C. The resulting structure provides \(\sim 2\) orders of magnitude better temperature stability as compared to the resistor structure used in [39], shown in Fig. 2.24 (which is based on a series combination of two different types of resistors).

In summary, one can divide a long core resistor, which has a P-TC, into several short core resistors in series. Because each of the short core resistors introduces two more contact resistors with N-TC one can compensate temperature variations (with a couple of trial and error steps). In the above example, we started from a total resistor which has large number of contacts, \(n = 22\), and remove those to smaller \(n = 14\) in one step and again to the final number of \(n = 8\) to achieve a low temperature coefficient.

### 2.5.7 Summary of the Proposed Technique

A technique for implementing temperature-stable integrated resistors is presented. The typical structure of monolithic resistors contains a core resistor that is connected to the circuit interconnects through contacts. Typically, the temperature behaviour of contact resistors is ignored, however, we show that one can take advantage of contact resistors and their temperature dependency. The improvement in temperature behaviour of the proposed structure is due to adjusting the amount of core resistors (with P-TC) and contact resistors (with N-TC) used in the structure to minimize (or stabilize) the overall TC of the resistor. The concept has been confirmed using prototype structures implemented in a 0.13 \(\mu\)m CMOS technology. Without loss of generality, the proposed approach can be used to implement a resistor with a given temperature coefficient.
2.6 Chapter Summary

In this chapter, we measure and validate the model for NMOS / PMOS transistor in high temperature up to 180°C. We propose the design of a modified constant-$g_m$ bias circuit, along with a folded-cascode amplifier. We use this bias circuit and amplifier as a building block of the proposed high-temperature bandgap voltage reference. Furthermore, we study the preliminary technique proposed for implementing resistor with near-zero TC based on the temperature behaviour of resistor contacts.

In the next chapter, we study the above-mentioned behaviour of monolithic resistors in more details and present a mathematical model along with an analysis. Based on the proposed mathematical model, we introduce a resistor structure with identical unit resistors in series to implement any given resistor with desired TC. Based on the proposed technique and as a proof of concept we designed and implemented several resistor structures.
Chapter 3

Monolithic Resistors with a Desired Temperature Coefficient

Temperature-independent resistors, resistors with zero temperature coefficient (Z-TC), improve the reliability of analog and mixed-signal circuits for applications requiring operation over a wide range of temperature. In addition, being able to design a resistor with a known (and desired) TC provides more flexibility in the design of circuits for temperature-concerned applications. There are many analog and mixed-signal integrated circuits that require temperature-independent resistors. Examples include voltage and current references and bias circuits, in particular, constant-$g_m$ biasing in both regular and high-temperature circuits [6–8, 21, 39, 41–43]. Resistors with a known TC can be used for temperature measurement and/or calibration.

There are several approaches available to implement a (near) Z-TC resistor: Some are intended for discrete (off-chip) resistors, or use non-standard materials and/or extra process steps to realize a composite on-chip resistor with Z-TC [44–49]. In addition to these approaches, there are several circuit techniques to implement (near) Z-TC resistors. One technique is to apply an external compensation circuit [50] which requires extra design effort and circuit components. Another circuit technique is based on using two different types of monolithic resistors, negative TC (N-TC) and positive TC (P-TC) resistors [51–56]. By properly combining these resistors in series and/or parallel a (near) Z-TC composite resistor is realized. However, in such resistor structures the effects of contacts on the temperature behaviour of the overall
resistor has not been considered. The effects of contacts become more pronounced as the number of resistors that are being combined increases.

To alleviate the above-mentioned issues, the presented technique is based on implementing a given resistor using a combination of same-type resistors and considering the temperature behaviour of contacts used in sub-resistors. A preliminary concept of such technique is discussed in [40]. In this work, we expand the concept, simplify the design strategy, provide the design methodologies, and verify the proposed techniques using simulations as well as measurements on a wide range of fabricated resistors. Using the proposed model, one can lay out a resistor with a controlled TC by combining several core resistors and adding certain number of contacts (with opposite TC as compared to the core resistors). Thus, a resistor with a desired TC (with negative, nearly zero, or positive value) can be implemented.

In the following sections, we present the proposed monolithic resistor structure and a design strategy on how to implement a resistor with a desired TC. The proposed technique is simple and practical. Without loss of generality, we present the design technique for resistors with near Z-TC, however, the technique can be used to design resistors with a desired TC.

As a proof of concept several resistor structures, based on the proposed technique, in the range of 1 kΩ to 100 kΩ have been simulated and implemented in a 0.13 µm-CMOS technology. These different resistors are designed to show the impact of each model parameter on temperature behaviour of the overall resistor. The simulation and measurement results over the temperature range of 25 to 200°C confirm the validity of the proposed technique. These results will be discussed in the measurement section.
3.1 Monolithic Resistor Structure

Typically, in a monolithic design, it is desirable to implement resistors with a near zero (or with a given) TC using the foundry provided resistor structures available in a given technology. Let us first briefly overview a generic resistor structure that is provided by foundries.

3.1.1 Foundry-Provided Resistor Parameters

A typical resistor structure, e.g., a poly resistor, consists of two physical parts, namely, a core resistor, with the sheet resistance \( R_{\text{core}} \), and two terminal contact resistors, each one denoted as \( R_{\text{cnt}} \). Note that the number of physical contacts in the contact region depends on the technology as well as the shape and area of the contact region, however, without loss of generality, \( R_{\text{cnt}} \) refers to the resistance of the contact region. The total value of the resistor, \( R_{\text{tot}} \), is given by:

\[
R_{\text{tot}} = (R_{\text{core}} \cdot \frac{L}{W}) + (2 \cdot \frac{R_{\text{cnt}}}{W})
\]  

(3.1)

where \( L \) and \( W \) are the length and width of the resistive layer, e.g., poly, in \( \mu \text{m} \). The core resistor, \( R_{\text{core}} \), is in \( \Omega/\), each contact resistor, \( R_{\text{cnt}} \), is in \( \Omega \cdot \mu \text{m} \), and total resistor, \( R_{\text{tot}} \), is in \( \Omega \). A typical minimum value (scaled version) of \( L \) and \( W \) for such resistor, in the technology that we used, are 1.6 \( \mu \text{m} \) and 0.4 \( \mu \text{m} \), respectively. Each resistor component has its own resistivity value and temperature coefficient. These values are provided by the foundry. Please note that to avoid disclosing the values provided by the particular foundry used in this work, the values shown in Table 3.1 are scaled.

As can be seen from the table, \( R_{\text{core}} \) has a P-TC and \( R_{\text{cnt}} \) has an N-TC, therefore,
<table>
<thead>
<tr>
<th>Definition</th>
<th>Constant</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
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<td>Minimum Length</td>
<td>$L_{\text{min}}$</td>
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<td>$\mu$m</td>
</tr>
<tr>
<td>Minimum Width</td>
<td>$W_{\text{min}}$</td>
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<td>$\mu$m</td>
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<td>Core Resistor</td>
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<td>$\Omega/sqr$</td>
</tr>
<tr>
<td>Contact Resistor</td>
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<td>$\Omega \cdot \mu m$</td>
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<td>Contact Resistor-TC</td>
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<td>$R_{\text{core}} \times L_{\text{min}}$</td>
<td>435.2</td>
<td>$\Omega \cdot \mu m$</td>
</tr>
<tr>
<td>$R_{\text{u.cnt}}$ (Unit $R_{\text{cnt}}$)</td>
<td>$2 \times R_{\text{cnt}}$</td>
<td>86.4</td>
<td>$\Omega \cdot \mu m$</td>
</tr>
<tr>
<td>$R_{\text{u.tot}}$ (Unit $R_{\text{tot}}$)</td>
<td>$R_{\text{tot}} \times W_{\text{min}}$</td>
<td>$0.4 \cdot R_{\text{tot}}$</td>
<td>$\Omega \cdot \mu m$</td>
</tr>
</tbody>
</table>

Table 3.1: Example parameters of a specific resistor ($R_{\text{tot}}$) based on core resistance ($R_{\text{core}}$) and contact resistance ($R_{\text{cnt}}$).

by proper choice of areas for the core and contact regions, one can implement a resistor with a given temperature coefficient. This is the fundamental idea behind this work which will be elaborated in more details in this paper.

### 3.1.2 Definitions Used in the Proposed Technique

For the purpose of clarity and brevity of the analysis that will follow, we define three unit resistors. Unit $R_{\text{core}}$: $R_{\text{u.core}} = R_{\text{core}} \times L_{\text{min}}$, Unit $R_{\text{cnt}}$: $R_{\text{u.cnt}} = 2 \times R_{\text{cnt}}$, and Unit $R_{\text{tot}}$: $R_{\text{u.tot}} = R_{\text{tot}} \times W_{\text{min}}$. Note that the factor of 2 is included in $R_{\text{u.cnt}}$ to account for the contacts at both ends of the core region. Also, note that all these defined parameters have the same unit, i.e., $\Omega \cdot \mu m$. The scaled values of these parameters are also listed in Table 3.1. Using these three defined unit resistors, we can rewrite Eq. (4.1) as follows:

$$
\frac{R_{\text{u.tot}}}{W_{\text{min}}} = \frac{R_{\text{u.core}}}{W} + \frac{R_{\text{u.cnt}}}{W}
$$

(3.2)

Furthermore, without loss of generality, we consider the following two configura-
tions for implementing a given resistor, $R_{tot}$: one resistor configuration is based on a long minimum-width core resistor with contact areas at each end, $R_{long}$, and the other one is a series of several minimum-width short core resistors each having two contacts at their two ends, $R_{short}$. The resistance of these configurations based on Eq. (4.1) can be calculated as:

$$R_{long} = (R_{core} \cdot \frac{x \cdot L_{min}}{W_{min}}) + (2 \cdot \frac{R_{cnt}}{W_{min}}) \quad (3.3)$$

$$R_{short} = (R_{core} \cdot \frac{n \cdot y \cdot L_{min}}{W_{min}}) + n \cdot (2 \cdot \frac{R_{cnt}}{W_{min}}) \quad (3.4)$$

where $L_{min}$ and $W_{min}$ are the minimum length and width of the core resistor, $x$ and $y$ are length factors defined as $L/L_{min}$ for $R_{long}$ and $R_{short}$, respectively, and $n$ is the number of series resistors in $R_{short}$. Examples of $R_{long}$ and $R_{short}$ with different values for $x$, $y$, and $n$ are shown in Fig. 3.1.

Note that since $R_{core}$ has a P-TC and $R_{cnt}$ has a N-TC (refer to Table 3.1), essentially by increasing $x$ the effective TC of $R_{long}$ increases. Thus, by proper choice of $x$, one can design a resistor in which core and contact resistors have the same absolute value of TC, however, with opposite signs.

### 3.1.3 Resistor Temperature Coefficient Considerations

Consider a minimum-size resistor with $L_{min}$ and $W_{min}$ and corresponding contacts at each end as shown in Fig. 3.1.(a). From Eq. (3.3) for $x = 1$ (or from Eq. (3.4) for $n = 1$ and $y = 1$) by substituting the corresponding values from Table 3.1, we obtain the ratio of $R_{u,cnt}/R_{u,core}$ which is equal to $86.4 \ \Omega \cdot \mu m / 435.2 \ \Omega \cdot \mu m = 0.199$. Note that for this particular case, the contact resistor is almost a fifth of the core resistor.
(that is, $R_{cnt} \approx 1/6 \times R_{tot}$ and $R_{core} \approx 5/6 \times R_{tot}$). On the other hand, the TC ratio for the $R_{cnt}$ and $R_{core}$, i.e., $TC_{cnt}/TC_{core}$, is $-976/61.6 = -15.84$. Hence, the overall TC of a minimum-size resistor $R_{tot}$ is mainly effected by $R_{cnt}$, i.e., the effect of contact resistor TC on overall TC of the minimum-size resistor is approximately $-15.84 \times 0.199 = -3.15$ times more than that of the TC of the core resistor.

Now, consider the case when $R_{tot}$ is larger than the minimum-size resistor, i.e., $x > 1$ in Eq. (3.3). We want to investigate the temperature behaviour of $R_{tot}$ for different values of $x$. Based on the result of previous paragraph, if $x$ is chosen to be around 3.15, the overall temperature coefficient of the total resistor $R_{tot}$ is proportional to $3.15 \times 5/6 = 2.63$ related to $R_{core}$ and $-15.84 \times 1/6 = -2.64$ related to $R_{cnt}$. Thus, by proper choice of $x$, these two values can ideally cancel out each other to achieve
an $R_{\text{tot}}$ with a (near) zero TC.

Hence, for a given $R_{\text{tot}}$, depending on the value of the length factor, $x$, one can obtain different TCs. In our example, if $x$ is chosen to be around 3.15, a (near) zero-TC resistor will be achieved. For smaller values of $x$ the $R_{\text{cnt}}$ TC would be dominant and a negative overall TC will be obtained, while for larger values of $x$ the $R_{\text{core}}$ TC would be dominant and a positive overall TC will be achieved. To be able to differentiate between $R_{\text{long}}$ and $R_{\text{short}}$, in the following discussions, any long resistor $R_{\text{tot}}$ with sufficiently large $x$ which results in a positive TC resistor is referred to as $R_{\text{long}}$. In our example, if $x > 3.15$ then the resistor is classified as $R_{\text{long}}$. On the other hand, if $x$ is such that the TC of the resistor is negative ($x < 3.15$ for our example) then the resistor is referred as $R_{\text{short}}$. In essence, $R_{\text{long}}$ has P-TC and $R_{\text{short}}$ has N-TC. Based on the notation in Eqs. 3.3 and 3.4, $x$ is exclusively used for the length factor of $R_{\text{long}}$ and $y$ is exclusively used for length factor of $R_{\text{short}}$.

### 3.1.4 Combination of $R_{\text{long}}$ and $R_{\text{short}}$

In order to create an arbitrary value resistor with a given TC, one solution is to use an $R_{\text{short}}$ from Eq. (3.4) in series with an $R_{\text{long}}$ from Eq. 3.3 and choose proper values for $x$, $y$, and $n$ to achieve the desired TC.

Given the structure of $R_{\text{long}}$, by changing $x$ one can adjust the TC of $R_{\text{long}}$ to obtain a desired positive value. Similarly, in an $R_{\text{short}}$, by changing $y$, one can adjust the TC of $R_{\text{short}}$ to obtain a desired negative value. In general, $R_{\text{short}}$ consists of $n$ identical short resistor structures in series. These subcomponents have a fixed TC because of their fixed ratio of core resistor to contact resistor. Thus, by increasing $n$ only the resistance of $R_{\text{short}}$ (i.e., the resistance of the series combination of these $n$ subcomponents) increases while its negative TC stays intact. Therefore, in an
$R_{\text{short}}$ structure, one can set the TC by changing $y$ regardless of $n$ and then set the resistor value by changing $n$ without effecting the previously set TC. These are the basis for the proposed technique for designing a resistor with a desired TC using $R_{\text{long}}$ and $R_{\text{short}}$. As mentioned before, without loss of generality, here, we will focus on implementing (near) zero TC resistors with any given resistance, however, the proposed technique is also applicable to resistors with non-zero TC.

3.2 Analysis and Design of an Arbitrary Resistor with a Given TC

Using Series Combination of $R_{\text{long}}$ and $R_{\text{short}}$

Before explaining the main proposed technique for implementing a given resistor with a desired TC, in this section we present the preliminary procedure of the main technique which is based on designing a series combination of an $R_{\text{long}}$ and an $R_{\text{short}}$. Measured results of a few such series combinations have been previously presented in [40]. Then, we extend this design procedure to a more general and simpler technique for implementing resistors which is the main contribution of this work.

In order to find the proper values for $x$, $y$, and $n$ presented in Eqs. (3.3) and (3.4), we focus on the resistor structures shown in Fig. 3.1. Any arbitrary resistor, $R_{\text{tot}}$, can be realized using a series combination of one $R_{\text{long}}(x)$ and one $R_{\text{short}}(n, y)$, as shown in Fig. 3.1(b) and (c), as follows:

$$R_{\text{tot}} = R_{\text{long}}(x) + R_{\text{short}}(n, y)$$  \hspace{1cm} (3.5)

where both $x$ and $y$ are positive real values and $n$ is a positive integer. Note that $x$ and $y$ are length factors, i.e., $L/L_{\text{min}}$ where $L$ is the length of the structure and $L_{\text{min}}$ is the minimum length allowable in the process.
Considering Eq. (3.5), to simplify the analysis, we assume that \( y \) is equal to 1. This assumption is not restrictive since for compensating the P-TC of \( R_{\text{core}} \) we require to put more \( R_{\text{cnt}} \) with N-TC, thus, one can assume that all \( R_{\text{short}} \) resistor subcomponents are minimum length with two contact regions at each end and then the remaining portion of \( y \) can be included as a part of \( x \). Therefore, one can obtain an \( R_{\text{tot}} \) with \( n \) number of minimum-size unit resistors in series with an \( R_{\text{long}} \) as shown in Fig. 3.2.

\[
L : (x = 9.6)
\]

![Diagram](image)

**Figure 3.2:** \( R_{\text{tot}} \) example; series combination of \( n \) minimum-size unit resistors as \( R_{\text{short}} \) with \( n = 3 \) and \( y = 1 \) with a \( R_{\text{long}} \) with a length factor, \( x = 9.6 \).

Therefore, by substituting Eqs. (3.3) and (3.4) into Eq. 3.5, we have:

\[
R_{\text{tot}} = (n + x) \cdot (R_{\text{core}} \cdot \frac{L_{\text{min}}}{W_{\text{min}}}) + (n + 1) \cdot (2 \cdot \frac{R_{\text{cnt}}}{W_{\text{min}}}). \tag{3.6}
\]

Multiplying both sides of Eq. 3.6 by \( W_{\text{min}} \), we obtain:
\[ R_{\text{tot}} \cdot W_{\text{min}} = (n + x)R_{\text{core}} \cdot L_{\text{min}} + (n + 1)2R_{\text{cnt}}. \] (3.7)

Recall from Table 3.1, a unit resistor \( R_{\text{u.core}} \) denotes a minimum-size unit resistor, i.e., \( R_{\text{core}} \times L_{\text{min}} \). Also, a unit contact resistor \( R_{\text{u.cnt}} \) is denoted by \( 2 \times R_{\text{cnt}} \) (since each unit resistor has two contacts) and a unit total resistor \( R_{\text{u.tot}} \) is defined as \( R_{\text{tot}} \times W_{\text{min}} \). Using these notations, we rewrite Eq. (3.7) as:

\[ R_{\text{u.tot}} = (n + x)R_{\text{u.core}} + (n + 1)R_{\text{u.cnt}}. \] (3.8)

Eq. (3.8) can be rewritten as:

\[ x = -n\left(\frac{R_{\text{u.cnt}}}{R_{\text{u.core}}} + 1\right) + \frac{R_{\text{u.tot}} - R_{\text{u.cnt}}}{R_{\text{u.core}}}. \] (3.9)

This equation relates \( x \) and \( n \) based on the value of the desired resistance. Note that given a technology and the desired value of the resistor that we want to design, the values of \( R_{\text{u.core}}, R_{\text{u.cnt}} \) and \( R_{\text{u.tot}} \) are known and fixed. Thus Eq. (3.9) provides a known relationship between \( x \) and \( n \).

Another relation between \( x \) and \( n \) can be obtained based on the requirement on the temperature coefficient. More specifically, the temperature coefficient of \( R_{\text{u.tot}} \) in Eq. (3.8) is:

\[ (n + x)TC_{\text{core}}R_{\text{u.core}} + (n + 1)TC_{\text{cnt}}R_{\text{u.cnt}}. \] (3.10)

To achieve a (near) zero-TC, we require (note that the desired TC can be a negative, zero, or positive number, however, without loss of generality we have assumed that a (near) zero TC is desirable):
\[(n + x)TC_{\text{core}}R_{u,\text{core}} + (n + 1)TC_{\text{cnt}}R_{u,\text{cnt}} = 0. \tag{3.11}\]

Eq. (3.11) can be rewritten as:

\[
\frac{n + x}{n + 1} = -\frac{TC_{\text{cnt}} \cdot R_{u,\text{cnt}}}{TC_{\text{core}} \cdot R_{u,\text{core}}}. \tag{3.12}\]

Given that the TCs of contact and core resistors have opposite signs, the right-hand side of Eq. 3.12 is positive. We denote this value for which the positive and negative TCs of the resistor components balance each other as the balance factor (BF), i.e.,

\[
\frac{n + x}{n + 1} = \left| \frac{TC_{\text{cnt}} \cdot R_{u,\text{cnt}}}{TC_{\text{core}} \cdot R_{u,\text{core}}} \right| = BF. \tag{3.13}\]

Note that given a technology, BF is a fixed number and can be calculated from the process parameters provided by the foundry (similar to those given in Table 3.1).

Eq. (3.13) can be rewritten as:

\[
x = n \cdot (BF - 1) + BF. \tag{3.14}\]

This equation relates \(x\) and \(n\) for a (near) Z-TC resistor. Thus, Eqs. (3.9) and (3.14) provide a system of two equations two unknowns and can be solved for \(x\) and \(n\).

For example, suppose that we want to design a 15 k\(\Omega\) resistor with a (near) Z-TC. From Table 3.1 we have: \(R_{u,\text{tot}} = 15 \times 0.4 = 6 \, k\Omega \cdot \mu m\) and
Eqs. (3.9) and (3.14) can then be written as:

\[ x = -1.2n + 13.59, \tag{3.16} \]

and

\[ x = 2.15n + 3.15. \tag{3.17} \]

Thus, \( n = 3.17 \) and \( x = 9.97 \). However, since \( n \) is the number of series resistors in \( R_{\text{short}} \), it has to be an integer. Choosing \( n = 3 \) \((n = 4)\), one can recalculate \( x \) from Eq. (3.17) to keep near Z-TC behaviour. For \( n = 3 \) \((n = 4)\), we have \( x = 9.6 \) \((x = 11.75)\), hence introducing an error of \((9.6 - 9.97)/9.97 = -3.7\% \((17.9\%)\) in the value of the resistor, i.e., the designed resistor will be \( R_{\text{tot}} = 14.6 \, \text{k}\Omega \) \((R_{\text{tot}} = 18.2 \, \text{k}\Omega)\) instead of \( 15 \, \text{k}\Omega \). The series combination of \( R_{\text{long}} \) with \( x = 9.6 \) and \( R_{\text{short}} \) with \( n = 3 \) in order to design \( R_{\text{tot}} = 14.6 \, \text{k}\Omega \) is shown in Fig. 3.2.

This is the analysis pertaining to the technique proposed in [40] which we refer to as \( R_{\text{long}} \) and \( R_{\text{short}} \) structure to implement (near) Z-TC resistor (or with a straightforward modification it can be used for designing a resistor with a desired TC). However, as it can be seen from the above example, this approach has two main limitations: (1) since \( n \) has to be integer, the value of the designed resistor will most likely be different from the desired value, (2) \( R_{\text{tot}} \) consists of the resistor structures with different lengths (i.e., \( R_{\text{long}} \) and \( R_{\text{short}} \) components), thus it does not have a structured layout and is also sensitive to process. Therefore, to address these shortcomings, we propose another resistor structure that resolves the aforementioned issues and furthermore
makes the design procedure simpler and more practical. This modified structure is based on using identical resistor components and in the following section, we describe the steps that has led to this structure.

### 3.3 The Proposed Resistor Structure

Consider an $R_{tot}$ shown in Fig. 3.2 (as we know from the previous example, it has been designed to have a (near) Z-TC): the core part of $R_{long}$ can be divided into smaller sizes and added to the resistive core part of $R_{short}$ components, such that all the components ($R_{long}$ and all the resistors in $R_{short}$) have the same length. Due to this re-distribution, the temperature behaviour of $R_{tot}$ should remain the same since it still consists of the same amount of core resistor with P-TC and contact resistor with N-TC. This uniform resistor structure will minimize the impacts of process on the $R_{tot}$. With this rearrangement, any given resistor can be laid out with $N$ uniform resistors (note that $N = n + 1$) with a length of $X/N \times L_{min}$ where $X = x + n \cdot y$ and $x = y$, as shown in Fig. 3.3.

Note that since $R_{tot}$ has a (near) Z-TC consisting of identical resistor units, every resistor unit has to have (near) Z-TC. Thus, intuitively, each of these resistor units has to have a length (i.e., $X/N$) that is exactly equal to BF. In other words, the $R_{tot}$ consists of $N$ resistor units each of length $X/N \times L_{min}$ and having a (near) Z-TC. Therefore, we call this (near) Z-TC resistor unit balanced resistor (BR).

For instance, considering the (near) Z-TC resistor design example shown in Fig. 3.2. The entire length factor of $R_{tot}$ can be calculated as $x = 9.6$ related to $R_{long}$ plus $n \times y = 3 \times 1$ related to $R_{short}$ which is equal to 12.6. Also from Eq. (3.15), we know that for this example $BF = 3.15$. Now it is clear that one can simply divide the
\[ L = \left( \frac{X}{N} \right) \times L_{\text{min}} \]

Figure 3.3: \( R_{\text{tot}} \) example; series combination of \( N \) Balanced Resistors (BRs) with the same length factor of \( X/N \).

entire length factor of 12.6 into 4 units with the same length factor of 3.15 without changing the temperature behaviour of the \( R_{\text{tot}} \). Note that by this division we obtain the same structure as shown in Fig. 3.3 for \( R_{\text{tot}} \) with 4 BRs each has a length factor of 3.15 equal to BF.

With this modified \( R_{\text{tot}} \) model, one can rewrite Eqs. (3.8) and (3.11) as follows:

\[ R_{u,\text{tot}} = X \cdot R_{u,\text{core}} + N \cdot R_{u,\text{cnt}} \] \hspace{1cm} (3.18)

and

\[ X \cdot TC_{\text{core}} \cdot R_{u,\text{core}} + N \cdot TC_{\text{cnt}} \cdot R_{u,\text{cnt}} = 0. \] \hspace{1cm} (3.19)

Given the process parameters, these two equations construct a linear system of
two equations two unknowns that can be solved for $X$ and $N$. They can be rewritten as:

$$X = \frac{R_{u,\text{tot}} - N \cdot R_{u,\text{cnt}}}{R_{u,\text{core}}} \quad (3.20)$$

and

$$X = N \cdot BF \quad (3.21)$$

Now, assume that we want to design the same 15 kΩ resistor discussed in the previous section. After solving for $X$ and $N$ from Eqs. (3.20) and (3.21), we have: $N = 4.12$ and $X = 12.98$. Again, since $N$ is a number of resistor units, it has to be an integer. Thus, for $N = 4$ ($N = 5$), $X$ becomes 12.6 (15.75), hence introducing an error of $(12.6 - 12.98)/12.98 = -2.9\%$ ($21.3\%$) in the value of the resistor. The resistor will be $R_{\text{tot}} = 14.6$ kΩ ($18.2$ kΩ) rather than 15 kΩ. Note that this resistor has the same temperature behaviour as the one designed in the previous section which was based on $R_{\text{long}}$ and $R_{\text{short}}$ combination.

Thus, in this modified structure (as compared to the structure based on $R_{\text{long}}$ and $R_{\text{short}}$), all resistor units are identical and therefore have the same temperature behaviour. Furthermore, this structure with identical unit resistors is more layout friendly. However, with this approach, one still can not design an $R_{\text{tot}}$ with an arbitrary value and there will be some error due to the requirement of $N$ being a positive integer number. In what follows, we address the design problem of how to implement an arbitrary (near) $Z$-TC resistor with minimal (ideally zero) error in its value.
3.3.1 (Near) Z-TC Resistor with an Arbitrary Value Using Parallel / Series-Combinations Algorithm

Let us first find the minimum possible value of balanced resistor available in a given technology. Given that:

\[ BF = \left| \frac{TC_{cnt} \cdot R_{u,cnt}}{TC_{core} \cdot R_{u,core}} \right|, \quad (3.22) \]

from Eqs. (3.20), (3.21) and (3.22), we have:

\[ N = \frac{R_{u,tot}}{(R_{u,cnt} - R_{u,cnt} \cdot \frac{TC_{cnt}}{TC_{core}})}. \quad (3.23) \]

For the process used in this work, substituting \( R_{u,cnt} \) and \( R_{u,cor} \) in kΩ, we obtain \( N = R_{u,tot}/1.46 \) or \( R_{u,tot} = 1.46 \cdot N \). Since \( R_{u,tot} = R_{tot} \cdot W_{min} \), we can derive \( R_{tot} \) as a function of \( N \) for \( W_{min} = 0.4 \mu m \) as follows:

\[ R_{tot} = (1.46/0.4) \times N = 3.65 \times N. \quad (3.24) \]

From Eq. (3.24), one can obtain possible values for structures made of series combination of \( N \) BRs. Table 3.2 shows these values for \( N = 1, \ldots, 10 \).

<table>
<thead>
<tr>
<th>( N )</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{tot} )</td>
<td>3.65</td>
<td>7.30</td>
<td>10.95</td>
<td>14.60</td>
<td>18.25</td>
</tr>
<tr>
<td>( N )</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>( R_{tot} )</td>
<td>21.90</td>
<td>25.55</td>
<td>29.20</td>
<td>32.85</td>
<td>36.50</td>
</tr>
</tbody>
</table>

Table 3.2: Values of \( N \) BRs connected in series in kΩ, for \( W_{min} = 0.4 \mu m \) and \( N = 1, \ldots, 10 \).

If the specific values shown in Table 3.2 can be used in a design, then no additional design step is required. However, if a different value is desired, which is typically the
case, then the following approach can be applied.

Since the minimum BR increment is 3.65 kΩ (for N=1 and near zero-TC), we need a procedure to design a smaller resistor in the range of 0 to 3.65 kΩ so it can be added to any series combination of the BR building blocks listed in Table. 3.2 to cover the full range of resistances. One possibility is to use parallel combination of these BRs to create the smaller residual resistor. There are many different ways to implement such smaller resistor, however, many are ad-hoc methods and will not necessarily result in an optimal configuration (in a sense of number of resistors used). To achieve the optimal configuration with the least number of BRs we can use a dynamic programming algorithm [57] and efficiently find all possible values for such residual resistors with a given error bound (as percentage of BR). Given the specific percentage error of e, the algorithm considers separate intervals of \([p \times e, (p + 1) \times e]\) for all \(0 \leq p \leq 1/e − 1\) and finds a specific series/parallel combination of BRs with minimum number of resistor building blocks whose value is inside each interval. For instance if \(e = 5\%\) there are 20 intervals of the form \([p \times 0.05, (p + 1) \times 0.05]\) with \(0 \leq p \leq 19\), and thus the algorithm finds 20 resistors each located in a different interval, so that, there is one value within each interval. The algorithm is as follows.

In this discussion, \(s, i, j, k, k',\) and \(k''\) are all positive integers.

We define \(R_1(1) = BR\) and for the integer number \(s \geq 2\) we define \(R_s\) as the set of resistors, where each element of the set, \(R_s(k)\), has a value that is less than BR, and each element is implemented using series and/or parallel combination of exactly \(s\) BR resistors. Furthermore, \(R_s\) only includes the resistors which are not in any \(R_j\) where \(j < s\). For example, \(R_2\) is a set of all combinations of 2 BR resistors. Since there are only two possibilities, parallel or series combination of 2 BRs, and the elements of \(R_2\) are required to be smaller than BR, there will be only one element in \(R_2\), whose value
relative to BR is 0.5 (implemented by combining two BR components in parallel).

We compute all possible elements of $R_s$ in a bottom-up scheme (i.e., the elements of $R_s$ are series or parallel combinations of two elements, one from $R_i$ and the other from $R_{s-i}$, where $0 < i \leq s/2$), shown in Fig. 3.4, according to the following formula:

$$R_s(k) = \begin{cases} 
R_i(k') + R_{s-i}(k'') & \forall i : 0 < i \leq s/2 \\
OR & \forall \{k, k', k''\} \geq 0 \\
R_i(k') \parallel R_{s-i}(k'') & \forall i : 0 < i \leq s/2 \\
& \forall \{k, k', k''\} \geq 0
\end{cases}$$

Figure 3.4: $R_s(k)$ is constructed by either series or parallel combination of two elements from previous sets.

In order to avoid any duplication, we use a hash table [57] and store the values that have been already calculated. For example, given a desired precision of 5% again, the proposed algorithm checks different configurations of such BR-based resistors until it
Table 3.3: Algorithm results for computing all possible residual resistor values based on previously constructed resistor combinations with a 5% precision.

finds exactly one resistor for each of the 20 intervals.

Table 3.3 shows the result of the proposed algorithm for computing all 20 residual
resistor values for a 5% precision. Note that some of $R_i$ sets are empty sets. It also provides information on how each resistor has been implemented based on the previously calculated resistors. For example, for designing a 0.42 BR combination, refer to $R_7(2)$, we use a parallel combination of $R_6(3)$ and $R_1(1)$, where $R_6(3)$ is the series combination of $R_4(1)$ and $R_2(1)$. The structure is shown in Fig. 3.5.

![Figure 3.5: Reconstructed $R_7(2)$ by parallel combination of $R_1(1)$ and $R_6(3)$ which in turn have been reconstructed based on Table 3.3. All building block resistors have the same value of a unit BR.](image)

We now provide an example: Assume that we want to design the same 15 kΩ resistor that we discussed earlier. Further assume that the required precision is 5% of BR (i.e., $0.05 \times 3.65 \text{ kΩ} = 182.5 \text{ Ω}$). As a first step, one can chose a closest value smaller than the given $R_{tot}$ from Table 3.2 which is 14.60. By combining 4 BRs in series we obtain 14.60 kΩ. Therefore, we need to find $15 - 14.6 = 0.4 \text{ kΩ}$ residual.
resistor, using the proposed algorithm. 0.4 kΩ is 0.11 of $BR(3.65 \, \text{kΩ})$, hence we can use algorithm results listed in Table 3.3 to find the closes value to 0.11 which is $R_{11}(1) = 0.09$. Therefore, one can implement $R_{tot}$ as a series combination of 4 BRs in series with 11 BRs in parallel. The final value turns out to be $4 \times 3.65 + 0.09 \times 3.65 = 14.93 \, \text{kΩ}$ with an error of $(14.93 - 15)/15 = 0.5\%$ (or approximately 2% of BR which is within the desired 5% precision).

If a higher precision for $R_{tot}$ is desired, then one needs to use the same algorithm to find a larger number of residual resistors. For example, for precision of 1% with respect to BR, 100 residual resistors have to be found. Using the proposed algorithm, one can efficiently find the optimal residual resistor configuration (in a sense of number of BR elements used) for any desired precision. The proposed algorithm provides a technique to design any given resistor with an arbitrary unit resistor. Here, we use this technique to design (near) Z-TC resistors. Without loss of generality, this technique can be extended for designing a resistor with a desired temperature coefficient.

### 3.3.2 Z-TC Resistor with an Arbitrary Value by Changing Resistor Width

The algorithm proposed in the previous subsection is useful when it is desired to keep the width of each resistor block constant (for example, in this paper, we assumed minimum width structures). Note that the temperature behaviour of the proposed resistor which consists of BRs is independent of the $W$ of its components. This is due to the fact that the BF found in Eq. (3.13) depends on both $R_{u.core}$ and $R_{u.cnt}$, while these unit resistors (based on Eq. (3.2)) are independent of the $W$, resistor width. $W$ affects both $R_{u.core}$ and $R_{u.cnt}$ in the same way and since $R_{u.core}$ has P-TC and $R_{u.cnt}$ has N-TC thus temperature-wise the effect of $W$ is canceled out. Although
the temperature behaviour of the proposed resistor structure is independent of its $W$, the value of the resistor is indeed a function of $W$ (refer to Eq. (3.2)). Thus, one can increase (decrease) the width of all BR building blocks to decrease (increase) the value of $R_{tot}$ without changing the TC of the resistor structure. This fact leads us to a simpler design procedure without the need to use the algorithmic design proposed earlier.

### 3.3.3 The Main Proposed Design Procedure

The proposed procedure to implement any arbitrary resistor with (near) Z-TC behaviour is presented here. Note that the procedure is general and can be applied to any TC, however, without loss of generality we are focusing on (near) Z-TC structures. Let us consider the same design example of implementing a 15 kΩ resistor that we discussed earlier. Based on Eq. (3.23), if we use an arbitrary $W = W_{min} + \Delta W$, we can derive:

$$N = \frac{R_{tot} \cdot (W_{min} + \Delta W)}{1.46} \quad (3.25)$$

where in our process $W_{min} = 0.4$. The corresponding resistor structure is shown in Fig. 3.6.

To design and implement a (near) Z-TC $R_{tot}=15$ kΩ, using resistor components with width of $W_{min}$, the raw value for $N$ was calculated to be 4.12. By properly choosing $\Delta W$ one can adjust $N$ to be an integer, e.g., 5 in this case where a new $W$ can be found to be $5 \times 1.46/15 \approx 0.49$ µm. That is, a $\Delta W$ of 0.09 µm is required. As a side note, by increasing the $W$ from 0.4 µm to 0.49 µm, a 14.90 kΩ resistor is achieved. The value of the resistor can be further refined if finer width adjustments
are possible in the technology. Using $W = 0.49 \, \mu m$ introduces an error of about 100 $\Omega$ as compared to the target resistor, $15 \, k\Omega$ which translates to $\sim 0.7\%$ error. Since the fine tuning of the value is achieved by adjusting the width of the building blocks, the number of overall resistor blocks used is generally less than that of the case when the width of all resistor building blocks is fixed (which was the case for the proposed algorithm in Section 3.3.1).

It is worthwhile to mention that instead of increasing the $W$ of all $N$ BRs shown in Fig. 3.6 one can only increase the $W$ of one BR component and keep the rest intact. Such structure is shown in Fig. 3.7.

In summary, the proposed design procedure is as follows: to implement an arbitrary resistor with (near) Z-TC, we would first choose the closest available balanced resistor whose value is larger than the desired resistor (from Eq. (3.24) or from pre-
calculated values shown in Table 3.2). For instance, if the goal is to design a 20 kΩ resistor, we choose 21.90 kΩ structure which consists of $N = 6$ BR components. Then, we increase the width of all, some, or only one of these $N = 6$ BR building blocks to achieve the desired resistance.

Note that the proposed design procedure is general and one can also design and implement a resistor with an arbitrary positive or negative TC value by setting the Eq. (3.19) equal to the desired TC rather than zero. The design strategy is the same as shown in Fig. 3.6, the only difference is to choose different length for the resistor components in series combination, in other words we still use the same structure, but for N-TC the resistor lengths will be less than BF (the resistor components will be $R_{\text{short}}$), and for P-TC the resistor lengths will be more than BF (the resistor components will be $R_{\text{long}}$). The positive and negative TC range of such resistor
is limited by the temperature coefficient of core and contact resistors, $TC_{\text{core}}$ and $TC_{\text{cnt}}$, that are provided by the specific target technology. As a proof-of-concept of the proposed technique, we have designed and implemented several different resistor structures. The simulation and measurement results are provided in the following section.

### 3.4 Simulation and Measurement Results

Based on design technique proposed above, we have simulated and implemented several different resistor structures with Z-TC, N-TC and P-TC. All provided simulation and measurement results in this section are over the temperature range of 25 to $200^\circ$C.

First, we provide the results for a BR of 1, 10, 100 kΩ to prove the validity of the proposed technique. Then, we investigate the role of different width size of a given BR on its temperature behaviour for different number of series resistor components, $N$. In this case, we use yet another BR value, i.e., $\sim$ 8 kΩ. Finally, we compare the temperature behaviour of 10 and 100 kΩ $R_{\text{tot}}$ from different structures: BR, $R_{\text{short}}$ and $R_{\text{long}}$. In this work, all resistors have been designed and implemented using the structure shown in Fig. 3.6.

During the measurements, for each resistor, we applied between 50 to 150 different sample currents and measured the voltage across the resistor for each current at the given temperature. The resistor value for each temperature, has been calculated by fitting a line into measured current/voltage data. The measurements are done on three different test chips and at 25, 75, 125, 175 and 200$^\circ$C.
3.4.1 Temperature Stability of BRs in the Range of 1 to 100 kΩ

The simulation and measurement results presented in Fig. 3.8 provide the temperature stability of three different BRs in a range of 1 to 100 kΩ. Note that there is a good match between the simulation and measurement results. The values of BR structures are arbitrarily chosen to show the validity of the method, however, the performance is not limited to these values. Note that for larger size resistors, e.g., 1 MΩ, one can use a series combination of the above resistors (e.g., 10 100 kΩ BR structure) and achieve the same temperature stability. Also, for smaller size resistors, e.g., 100 Ω for example, one can use a parallel combination of such resistors (e.g., 10 1 kΩ BR structure).

3.4.2 Temperature Stability of an ~8 kΩ Resistor with Different-Width BRs

In this section, we investigate the effect of the width of the resistor components on the temperature behaviour of the proposed BR structure. As expected, the measurements confirm that the temperature stability of the proposed resistor structure is independent of the width of its building blocks.

Fig. 3.9 shows the simulation and measurement results of an ~8 kΩ BR with three different width size. In essence, we designed three BRs with $N = 1, 6, \text{ and } 13$ and for larger number of $N$, we also increased the width so that the total amount of BR structure remains about the same ~8 kΩ.

Comparing the measurements and simulations, there are some errors in the total amount of all three resistors. The one with $N = 1$ introduces a larger error, while the other two ($N = 6 \text{ and } 13$) show about the same error. This extra error can be
attributed to the impact of process variation during the fabrication, since $N = 1$ structure is highly process dependent, while the other two are more robust due to multiple finger structure. Therefore, comparing $N = 6$ with $N = 13$ BR structure, they both provide about the same temperature behaviour over the temperature range of 25 to 200°C. Note that in all cases the value of the resistor is approximately temperature independent (N-TC behaviour).
Figure 3.9: Simulation and measurement results for a $\sim 8$ kΩ BR with different width size ($N = 1, 6$ and 13) over the temperature range of 25 to 200 °C.

### 3.4.3 Comparing 10 kΩ BR, $R_{short}$ and $R_{long}$ Structures

The simulation and measurement results in Fig. 3.10 present the temperature behaviour of a 10 kΩ resistor with three different structures, BR, $R_{short}$ and $R_{long}$. Supporting the proposed technique, both simulation and measurement results confirm that: The $R_{short}$ shows a N-TC behaviour since the TC of contacts is dominant as compared to the core resistor TC, while the BR obtains (near) Z-TC and the $R_{long}$ shows a P-TC behaviour since the core resistor TC is dominant as compared to the TC of contacts. These results are also listed in Table. 3.4.
Figure 3.10: Simulation and measurement results for a 10 kΩ resistor with different structures (BR, $R_{\text{short}}$ and $R_{\text{long}}$) over the temperature range of 25 to 200 °C. Measurements are done on three different test chips, however, the variation at each point is less than 10 Ω and thus are masked by the marker.

<table>
<thead>
<tr>
<th>10 kΩ</th>
<th>$BR$</th>
<th>$R_{\text{short}}$</th>
<th>$R_{\text{long}}$</th>
</tr>
</thead>
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<td>$TC_{\text{sim}}$ ppm/°C</td>
<td>-0.041</td>
<td>-293</td>
<td>+61</td>
</tr>
<tr>
<td>$TC_{\text{mes}}$ ppm/°C</td>
<td>-19.6</td>
<td>-411</td>
<td>+73</td>
</tr>
</tbody>
</table>

Table 3.4: Temperature coefficient of a 10 kΩ resistor with different structures (BR, $R_{\text{short}}$ and $R_{\text{long}}$) over the temperature range of 25 to 200 °C calculated based on both simulation and measurement results.

3.4.4 Comparing 100 kΩ BR, $R_{\text{short}}$ and $R_{\text{long}}$ Structures

The simulation and measurement results shown in Fig. 3.11 present the temperature behaviour of a 100 kΩ resistor again with three different structures, BR, $R_{\text{short}}$ and
Figure 3.11: Simulation and measurement results for a 100 kΩ resistor with different structures (BR, \( R_{\text{short}} \) and \( R_{\text{long}} \)) over the temperature range of 25 to 200 °C. Measurements are done on three different test chips, however, the variation at each point is less than 100 Ω and thus are masked by the marker.

\( R_{\text{long}} \). The simulation results illustrate the same temperature behaviour compared with the results for a 10 kΩ resistor shown in Fig. 3.10. This trend and confirm the validity of the proposed technique for different resistor values. Note that the measurement results show a bend at high temperature (beyond 125°C for all three resistor structures. The bend can be attributed to the temperature behaviour of an electrostatic discharge (ESD) protection block that is embedded in the chip pads. These blocks consist of a reversed-bias diode which introduces an extra leakage current at
high temperature and this extra current reduces the measured resistor value. Therefore, we believe that this bend is due to the limitation in the measurement setup and is not related to the resistor structure.

3.5 Chapter Summary

A technique for implementing monolithic resistors with a desired TC over a wide temperature range is presented. A typical monolithic resistor consists of a core resistive layer terminated with contact layers on each end. In a typical process, there are core resistive layers that have TCs with opposite sign of that of the contacts. The technique is based on taking advantage of resistor contacts that has an opposite TC as compared to the TC of the resistor core itself. By distributing a certain number of contacts across the core resistor, designers can achieve a desired overall TC for monolithic resistors. The main design goal is to find a specific length factor based on the proposed technique for implementing a given resistor $R_{\text{tot}}$ with a desired TC. Finding this length factor, one can use the proposed resistor structure consisting of identical resistor components with the same length factor to implement the $R_{\text{tot}}$. These identical resistors can be chosen to be $R_{\text{long}}$, BR, or $R_{\text{short}}$ depends on desired TC values which are P-TC, (near) Z-TC, or N-TC, respectively. Methodologies for designing such resistors are presented and several resistor structures in a range of 1 kΩ to 100 kΩ have been simulated and implemented in a 0.13 μm CMOS technology. The simulation and measurement results over the temperature range of 25 to 200$^\circ$C confirm the validity of the proposed technique. The technique is general and can be applied to any technology (aside from the 0.13 μm CMOS technology used in this work) in which core and contact components of resistors have opposite TC. In
the next chapter, we expand the analysis and study the design sensitivity to resistor’s length, width, and number of fingers.
Chapter 4

Analysis and Design of Monolithic Resistors:
Effects of Length, Width, and Number of Fingers

We use the proposed technique of previous chapter to implement a resistor with a desired TC and further analyze the effects of length, $L$, and width, $W$, of each finger, and the number of fingers, $N$, on the TC of multi-finger resistor structures with identical fingers that have a desired TC. To verify the results, 41 different resistors in the range of 100 $\Omega$ to 1 M$\Omega$ have been designed and implemented in a 0.13-$\mu$m CMOS technology. The measurement results over the temperature range of 25 to 200°C confirm the validity of the proposed technique.

The organization of this chapter is as follows. Section 4.1 briefly reviews the structure of monolithic resistors for a desired TC. Section 4.2 presents design considerations for multi-finger resistor structures and discusses the effect of $L$, $W$, and $N$ on the TC of the resistor, given the tolerance of the $R_{\text{core}}$ and $R_{\text{cnt}}$. Section 4.3 presents the measurement results and concluding remarks are provided in Section 4.4.

4.1 Generic Structure for Resistors with Desired TC

A typical foundry-provided resistor, e.g., a poly resistor, consists of two physical parts, a core resistor with the sheet resistance of $R_{\text{core}}$, and two terminal contact resistors each with resistance $R_{\text{cnt}}$. The total resistor, $R_{\text{tot}}$, is given by:
\[ R_{\text{tot}} = (R_{\text{core}} \cdot \frac{L}{W}) + (2 \cdot \frac{R_{\text{cnt}}}{W}) \] (4.1)

where \( L \) and \( W \) are the length and width of the core resistive layer in \( \mu m \). The total resistor, \( R_{\text{tot}} \), is in \( \Omega \), core resistor, \( R_{\text{core}} \), is in \( \Omega/ \), and each contact resistor, \( R_{\text{cnt}} \), is in \( \Omega \cdot \mu m \). Each resistor component (\( R_{\text{core}} \) and \( R_{\text{cnt}} \)) has its own temperature coefficient (\( TC_{\text{core}} \) and \( TC_{\text{cnt}} \), respectively, which are provided by the foundry). The resistor structure considered here has components with opposite sign TCs, that is, an \( R_{\text{core}} \) with a P-TC and \( R_{\text{cnt}} \) with an N-TC. Therefore, by proper sizing of the core and contact regions, one can implement a resistor with a given TC.

### 4.1.1 Physical Constraint

As discussed in Chapter 3, we define the following unit resistors. Unit \( R_{\text{core}} \): \( R_{u,\text{core}} = R_{\text{core}} \times L_{\text{min}} \), Unit \( R_{\text{cnt}} \): \( R_{u,\text{cnt}} = 2 \times R_{\text{cnt}} \), and Unit \( R_{\text{tot}} \): \( R_{u,\text{tot}} = R_{\text{tot}} \times W_{\text{min}} \), where \( L_{\text{min}} \) and \( W_{\text{min}} \) are the minimum available length and width of the core resistor, respectively. Based on these defined parameters and using Eq. (4.1), the overall resistance of a multi-finger resistor structure with \( N \) fingers can be rewritten as follows:

\[ R_{\text{tot}} = \frac{R_{u,\text{tot}}}{W_{\text{min}}} = N \cdot LF \cdot \frac{R_{u,\text{core}}}{W} + N \cdot \frac{R_{u,\text{cnt}}}{W} \] (4.2)

where \( LF \) is a length factor equal to \( L/L_{\text{min}} \) and \( L \) is the length of the core of one of the \( N \) identical fingers (Fig. 4.1). This is a generic multi-finger resistor structure which consists of \( N \) identical fingers, connected in series, with the total resistance of \( R_{\text{tot}} \).

Given \( R_{u,\text{core}} \) and \( R_{u,\text{cnt}} \), to design a specific \( R_{\text{tot}} \) with a known \( LF \), one has several choices for \( N \) and \( W \) based on Eq. (4.2). For example, if \( N \) is doubled, \( W \) can be
Figure 4.1: Multi-finger $R_{tot}$ with $N$ $R_{fng}$, identical finger resistors.

doubled to obtain the same $R_{tot}$ with a larger structure. Therefore, designers have a degree of freedom for implementing a given $R_{tot}$ with a known $LF$. We will discuss these different options and will take advantage of the degree of freedom to implement a temperature-stable resistor with a desired TC.

4.1.2 Temperature Constraint

The length factor $LF$ of each finger resistor is determined by desired TC specification. $LF$ in essence controls the ratio between the P-TC of $R_{u.core}$ and the N-TC of $R_{u.cnt}$ to obtain the required overall TC, $TC_{tot}$, of the $R_{tot}$. Including the effect of TC in Eq. (4.2), one can derive Eq. (4.3) which shows the overall temperature characteristic
of the total resistor, $TC_{tot}$, based on positive $TC_{core}$ and negative $TC_{cnt}$.

$$TC_{tot} \cdot R_{tot} = \frac{N}{W} \cdot (LF \cdot TC_{core} \cdot R_{u.core} + TC_{cnt} \cdot R_{u.cnt})$$  \hspace{1cm} (4.3)

This equation can be solved for $LF$ as follows:

$$LF = \frac{W}{N} \cdot \frac{TC_{tot} \cdot R_{tot}}{TC_{core} \cdot R_{u.core}} + \left| \frac{-TC_{cnt} \cdot R_{u.cnt}}{TC_{core} \cdot R_{u.core}} \right|$$  \hspace{1cm} (4.4)

Based on the amount of desired $TC$, $TC_{tot}$, the length factor can take any positive value more than 1 ($LF \geq 1$) to satisfy the technology minimum length requirement. For the case of overall zero temperature coefficient, i.e., $TC_{tot} = 0$, the first term in Eq. (4.4) is zero and the length factor equation is reduced to Eq. (4.5) where the balance factor ($BF$) is the $LF$ of the Z-TC resistor unit.

$$BF = \left| \frac{-TC_{cnt} \cdot R_{u.cnt}}{TC_{core} \cdot R_{u.core}} \right|$$  \hspace{1cm} (4.5)

For $TC_{tot} < 0$, we have $LF < BF$, and for $TC_{tot} > 0$, we have $LF > BF$. Based on these three desired $TC$ regions ($TC_{tot} < 0$, $TC_{tot} = 0$, and $TC_{tot} > 0$) and the corresponding length factors ($LF < BF$, $LF = BF$, and $LF > BF$), we define three resistor structures referred to as $R_{short}$, $BR$, and $R_{long}$, respectively. All these resistors have a similar structure to the one shown in Fig. 4.1, however, they have different length factors. Note that the range of achievable $TC_{tot}$ depends on the values of $TC_{core}$ and $TC_{cnt}$.

To investigate the effects of $L$, $W$, and $N$ on the temperature behaviour of the overall resistor over the temperature range of 25 to 200$^\circ$C, several different resistor structures ($R_{short}$, $BR$, and $R_{long}$) in the range of 100 $\Omega$ to 1 M$\Omega$ have been designed
and implemented in a 0.13 µm-CMOS technology. To avoid disclosing the process-specific parameters provided by the foundry used in this work, the values presented here are scaled. The minimum value (scaled version) of resistor length, $L_{\text{min}}$, for this technology is 1 µm. In this work, we consider $R_{\text{short}}$ structures that are minimum length, $L_{\text{min}}$, and have a length factor $LF = 1$. The $BR$ structures have $LF = 5$ and we also consider two different $R_{\text{long}}$ structures with $LF = 25$ and $LF = 50$.

4.2 Multi-Finger Resistor Design

Consider the above-mentioned physical and temperature constraints. In a given technology, one can calculate $BF$ from Eq. (4.5). Then depending on whether the desired $TC$ is negative or zero or positive, then we know that we have to choose $1 \leq LF < BF$ or $LF = BF$, or $LF > BF$, respectively. Noting that there is a degree of freedom in choosing $W$ and $N$, i.e., as long as as the ratio of $W$ and $N$ remains constant, one can scale them and still obtain the same $R_{\text{tot}}$, we can calculate the $LF$ and $\frac{W}{N}$, based on Eqs. (4.4) and (4.2). We will discuss about how to choose reasonable values for $W$ and $N$, for a given $\frac{W}{N}$ in Section 4.2.2. Next, we will consider the impact of resistor tolerance on the temperature behaviour of the proposed resistor structure.

4.2.1 Impact of Resistor Tolerance

Typically monolithic resistors are fabricated with a specific tolerance. In this work, the 3-sigma tolerance is 15 % for both for $R_{\text{core}}$, $R_{\text{cnt}}$. These resistor component tolerances cause an overall tolerance for $R_{\text{tot}}$. To study the impact of such tolerances on the desired $TC_{\text{tot}}$, we can rewrite Eq. (4.3) as follows:
\[ TC_{tot} = N \cdot \left( LF \cdot TC_{core} \cdot \frac{R_{u,core}}{R_{u,tot}} + TC_{cnt} \cdot \frac{R_{u,cnt}}{R_{u,tot}} \right) \] (4.6)

where only two resistor ratios are effected by such tolerances. By adding corresponding tolerances, these two ratios become \( \frac{\Delta R_{core} + R_{u,core}}{\Delta R_{tot} + R_{u,tot}} \) and \( \frac{\Delta R_{cnt} + R_{u,cnt}}{\Delta R_{tot} + R_{u,tot}} \). Since \( R_{u,cnt} \) is usually small in compare to \( R_{u,core} \), the \( R_{u,tot} \) is roughly equal to \( R_{u,core} \) and the overall tolerance, \( \Delta R_{tot} \), can be assumed to be equal to the core resistor tolerance \( \Delta R_{core} \) based on Eq. (4.2). Therefore, only the last term of Eq. (4.6) is effected by tolerance and becomes \( \frac{\Delta R_{cnt} + R_{u,cnt}}{\Delta R_{core} + R_{u,core}} \). For each specific \( LF \), the desired \( TC_{tot} \) in Eq. (4.6) can be viewed as having one constant term plus a term which varies based on the tolerance of resistor components. To study the impact of such tolerances the Eq. (4.6) can be rewritten as:

\[ \Delta TC_{tot} = A \cdot LF + B \cdot \frac{\Delta R_{cnt} + R_{u,cnt}}{\Delta R_{core} + R_{u,core}} \] (4.7)

where \( A = N \cdot TC_{core} \cdot \frac{R_{u,core}}{R_{u,tot}} \) and \( B = N \cdot TC_{cnt} \cdot W_{min} \). Consider two worst cases, when the maximum tolerance of \( \Delta R_{core} \) and \( \Delta R_{cnt} \) happens with opposite signs, i.e. either \( \Delta R_{cnt} = +15\% R_{cnt} \) and \( \Delta R_{core} = -15\% R_{core} \) or \( \Delta R_{cnt} = -15\% R_{cnt} \) and \( \Delta R_{core} = +15\% R_{core} \), the \( \Delta TC_{tot} \) in Eq. (4.7) equals either one of the following forms respectively:

\[ \Delta TC_{tot1} = A \cdot LF + B \times 1.35 \times \frac{R_{u,cnt}}{R_{u,core}} \] (4.8)

\[ \Delta TC_{tot2} = A \cdot LF + B \times 0.74 \times \frac{R_{u,cnt}}{R_{u,core}} \] (4.9)

The \( TC_{tot1} \) and \( TC_{tot2} \) present the upper bound and lower bound for the desired
Therefore, $TC_{tot}$ can take any value inside this bound based on the tolerances and it is not a fixed desired TC as assumed before. In other words, although based on the proposed above technique we design a specific resistor for a fixed desired TC, the overall $TC_{tot}$ can be any value in a bound around that desired TC. For example for designing a zero-TC resistor, the length factor is equal to $BF$ and can be calculated from Eq. (4.5). Substituting this length factor into Eq. (4.3), the $TC_{tot}$, however, is not zero due to the tolerance of resistor components as explained. Hence for any desired TC we will find a bound rather than a fixed value. Note that by increasing the $LF$, this tolerance bound is decreased because the constant term of $TC_{tot}$ gets larger in compared with the variable terms. We will discuss such an impact of tolerance in measurement results section.

4.2.2 Design and Implementation

In this work, we designed and implemented several different resistor structures (41 resistors with values from 100 Ω to 1 MΩ) with specific values of 100 Ω, 1 kΩ, 10 kΩ, 100 kΩ, and 1 MΩ. For each resistor value, we used different length factors to implement $R_{short}$, $BR$, and $R_{long}$ structures. Also, for each specific resistor value with a specific length factor, we used several options of $N$ and $W$ (e.g., $N = 1$, $N = 5$, and $N = 20$ with a corresponding increased $W$) to study the effects of $N$ and $W$ on the proposed resistor structure. Furthermore, to investigate the length factor sensitivity to $L$, we chose 10 different 10 kΩ $BR$ resistors with a length factor $LF = 5$ with intended errors of ±0.2%, ±0.4%, ±1%, ±2%, and ±10%. A list of these resistors along with their parameters is provided in Table 4.1.

Note that since $L_{min}$ is 1 µm, then $LF = L/1 = L$ for all of these resistor structures.

To analyze the behaviour of these resistor structures, we focus on their geometry and
<table>
<thead>
<tr>
<th></th>
<th>Value</th>
<th>Type</th>
<th>L</th>
<th>N</th>
<th>W (µm)</th>
</tr>
</thead>
<tbody>
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<td>1</td>
<td>100 Ω</td>
<td>R(_{\text{short}})</td>
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<td>1 kΩ</td>
<td>R(_{\text{long}})</td>
<td>25</td>
<td>20</td>
<td>172</td>
</tr>
<tr>
<td>14</td>
<td>10 kΩ</td>
<td>R(_{\text{short}})</td>
<td>1</td>
<td>5</td>
<td>0.2</td>
</tr>
<tr>
<td>15</td>
<td>10 kΩ</td>
<td>R(_{\text{short}})</td>
<td>1</td>
<td>26</td>
<td>1</td>
</tr>
<tr>
<td>16</td>
<td>10 kΩ</td>
<td>BR</td>
<td>5</td>
<td>1</td>
<td>0.2</td>
</tr>
<tr>
<td>17</td>
<td>10 kΩ</td>
<td>BR</td>
<td>5</td>
<td>5</td>
<td>0.9</td>
</tr>
<tr>
<td>18</td>
<td>10 kΩ</td>
<td>BR</td>
<td>5</td>
<td>20</td>
<td>3.7</td>
</tr>
<tr>
<td>19</td>
<td>10 kΩ</td>
<td>R(_{\text{long}})</td>
<td>25</td>
<td>1</td>
<td>0.9</td>
</tr>
<tr>
<td>20</td>
<td>10 kΩ</td>
<td>R(_{\text{long}})</td>
<td>25</td>
<td>5</td>
<td>4.3</td>
</tr>
<tr>
<td>21</td>
<td>10 kΩ</td>
<td>R(_{\text{long}})</td>
<td>25</td>
<td>20</td>
<td>17</td>
</tr>
<tr>
<td>22</td>
<td>100 kΩ</td>
<td>R(_{\text{short}})</td>
<td>1</td>
<td>47</td>
<td>0.2</td>
</tr>
<tr>
<td>23</td>
<td>100 kΩ</td>
<td>R(_{\text{short}})</td>
<td>1</td>
<td>255</td>
<td>1</td>
</tr>
<tr>
<td>24</td>
<td>100 kΩ</td>
<td>BR</td>
<td>5</td>
<td>12</td>
<td>0.25</td>
</tr>
<tr>
<td>25</td>
<td>100 kΩ</td>
<td>BR</td>
<td>5</td>
<td>50</td>
<td>0.94</td>
</tr>
<tr>
<td>26</td>
<td>100 kΩ</td>
<td>R(_{\text{long}})</td>
<td>50</td>
<td>1</td>
<td>0.2</td>
</tr>
<tr>
<td>27</td>
<td>100 kΩ</td>
<td>R(_{\text{long}})</td>
<td>50</td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>28</td>
<td>1 MΩ</td>
<td>R(_{\text{short}})</td>
<td>1</td>
<td>472</td>
<td>0.2</td>
</tr>
<tr>
<td>29</td>
<td>1 MΩ</td>
<td>BR</td>
<td>5</td>
<td>104</td>
<td>0.2</td>
</tr>
<tr>
<td>30</td>
<td>1 MΩ</td>
<td>BR</td>
<td>5</td>
<td>533</td>
<td>1</td>
</tr>
<tr>
<td>31</td>
<td>1 MΩ</td>
<td>R(_{\text{long}})</td>
<td>50</td>
<td>60</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 4.1: List of different designed and implemented resistor structures along with their parameters.
the effects of $N$ and $W$ on resistors with fixed length factors.

![Figure 4.2](image_url)

**Figure 4.2:** Implemented resistors located in the $N-W$ plane. The resistor values are chosen based on the design requirement in the range of 100 $\Omega$ to 1 M$\Omega$ and the resistor lengths are chosen based on temperature requirement represented as $R_{short}$, $BR$, and $R_{long}$.

Fig. 4.2 presents a graph of the above resistors in the $N-W$ plane. Both $N$ and $W$ axes are in logarithmic scale. Note that these resistors, whose value is within the range of 100 $\Omega$ to 1 M$\Omega$, cover a wide range of $10$ to $10^3$ for $N$ and $10^{-1}$ to $10^3$ $\mu$m for $W$. The naming convention used to denote the resistors indicates their geometry and their length factors and is based on the following order of the parameters; resistor, number, value, type, number of fingers, and length size. For the purpose of brevity, $R_{short}$, balance resistor, and $R_{long}$ resistors are denoted by $R_S$, $BR$, and $R_L$, respectively. For example, #18-10kBR20L5 refers to resistor number #18 (as listed in Table 4.1) which is a balanced resistor whose value is 10 k$\Omega$, and has 20 fingers of 5 $\mu$m length each. Note that in the plot of Fig. 4.2, the small-value resistors are located in the upper-left corner, the medium-value resistors are mostly distributed in the center and
the lower-left corner (depending on $N$), and the large-value resistors are located in the lower-right corner.

There are two boundary regions in this plot; one is for resistor structures with $N=1$, another one is for the resistor structures with minimum width, $W_{\text{min}}$. The resistors located close to these two regions in general are highly process dependent. For $N=1$ region, this is because the resistors have only one single finger, rather than a multi-finger structure. For $W_{\text{min}}$ region, a variation in $W$ introduces a large change on the overall resistor value and therefore it is not recommended (even the foundry-provided design kit warns designers not to use such resistors).

Furthermore, two regions for resistors with large physical size (denoted as “Oversize Region” and “Large-Size Region”) are shown in Fig. 4.2. The first one is for small-value resistors (100 Ω) in the upper-left corner with square markers, where $N$ is small and $W$ is large depending on the length of the structure (i.e., $R_{\text{short}}$, $BR$, or $R_{\text{long}}$). For these resistors $W/L > > 1$. The next such region is for large-value resistors (e.g., 1 MΩ) in the lower-right corner with diamond markers where $W$ is small and $N$ is large, depending on the length of the structure. For these resistors $N \times L/W > > 1$.

4.2.3 Design Region for Large-Size Small-Value Resistors (i.e., Oversize Resistors with Large $W$)

Based on the resistor layout consideration provided by the foundry, it is generally a good idea to keep the width of a resistor finger smaller than or at most at about the same size of its length. Let us assume $W/L \leq 2$ is a suitable size for each finger. In our design, since we have only implemented resistors with four different lengths, i.e., $R_{\text{short}}$ $L=1$, $BR$ $L=5$, and $R_{\text{long}}$ $L=25$ and $L=50$, we have included 4 horizontal dashed lines
to indicate $W = 2L$ for each of these length values so that we can quickly verify for each resistor whether it meets our $W/L \leq 2$ condition. For example, consider resistor #3 in Table 4.1 which is presented as #3-100BR5L5 in this plot. As mentioned earlier, the last number in the resistor name indicates that the length of the resistor finger is $5 \, \mu m$. If this resistor in the graph was under the line $W = 2 \times 5$, then it would have met the $W/L \leq 2$ condition. However, #3-100BR5L5 is located above the $W = 2 \times 5$ dashed line and thus does not satisfy our design condition. Note that none of these small-value resistors (100 $\Omega$) satisfy the sizing condition and therefore, their performance is likely not as reliable as the other resistors. We will discuss the temperature behavior of such resistors in the measurement results section. Note that for a resistor with a finger length of $L$ to satisfy the $W/L \leq 2$ condition it should appear below the corresponding $W = 2 \times L$ line. For a given finger length, the region below the corresponding $W = 2 \times L$ is referred to as the “proper region”, while the region above the line is referred to as the “oversize region”.

4.2.4 Design Region for Large-Size Large-Value Resistors (i.e., Resistors with Large $N$

As mentioned above the next large size region on the $N-W$ plane in Fig. 4.2 is for large-value resistors (1 M$\Omega$) where $N \times L/W \gg 1$. In this region typically $W$ is small and $N$ is large. In spite the above-mentioned observation that $LF$ is independent of $N$ and $W$ based on Eq. (4.4), the large number of contacts in a narrow physical resistor structure with a given length size can potentially introduce changes in the temperature behavior of the resistor. This can be attributed to the fact that in practical structures many contacts are used (for redundancy and also for reducing the contact resistance) and each symbolic contact shown in Eq. (4.2) is
indeed a group of several physical contacts. The contact behavior is not modeled in Eq. (4.2) and it becomes more important when the number of contacts in large. In essence, for a given $R_{\text{tot}}$, by doubling both $N$ and $W$ one may not get exactly the same $R_{\text{tot}}$ (which is theoretically expected) unless one made some adjustments to the finger width, $W$. The discrepancy may be due to the number of contacts that do not increase linearly with widening the $W$. As another example, for making 10 times larger resistor, ideally the $W$ needs to decrease 10 times or the $N$ needs to be increased by a factor of 10, or in general, the ratio of $W/N$ has to be $1/10$. Due to the discrete nature of the number of contacts (that is, number of contacts is not linearly proportional to the $W$ due to the foundry design rule limitations), $W$ and $N$ need to be adjusted to achieve the desired resistance value. In conclusion, $LF$ is somehow dependent on $N$ and $W$, particularly when $N$ is large and/or $W$ is small. As an example, let us compare resistors #22 and #28 in Table 4.1 which are shown as #22-100$kR_S47L1$ and #28-1$MR_S472L1$ in Fig. 4.2. For both these structures, $W$ is 0.2 $\mu$m and $L$ is 1 $\mu$m. The number of fingers, $N$, for larger resistor, $N = 472$, is not exactly 10 times that of a smaller resistor, $N = 47$. Note that although the ratio of these two resistors is 10, i.e., 1 M$\Omega$ and 10 k$\Omega$ the $W/N$ ratio is less than $1/10$. We will study the temperature behavior of such large-value resistors in the measurement results section.

Based on the above discussion, we can divide the graph of Fig. 4.2 into six different design regions; two “process dependent regions” for $N=1$ (single-finger resistors) and $W_{\text{min}}$ structures, two regions for resistors with a large physical size, namely “oversize region” and “large-size region” as explained above, a “non-practical region” which indicates that the designs do not follow the layout design rule of $W/L \leq 2$, and the “proper region” for resistors that do not belong to any of the previous regions. In the measurement section, we will discuss the temperature behavior of resistors of each
To make the plot more clear, we use different symbols for each group of resistors with the same value. Each such group consists of different $R_{\text{short}}$, $BR$, and $R_{\text{long}}$ types depending on their length. Also, all $BR$ resistors with the same value and different $N$ are connected with a dashed line to show how the size of these resistors increase based on the number of fingers, $N$. These $BR$ dashed lines starts from either of the “process dependent region” with $N = 1$ or $W_{\text{min}}$ and extend to the region of more practical multi-finger structures with larger $W$. Some of them (for example 1 kΩ $BR$ resistors) even extend to the “non-practical region” where the $W$ is about 10 time larger than $L$ (close to the $R_{\text{long}} L = 2 \times 25$ dashed line). Note that in each group of the same value resistors, $R_{\text{long}}$ and $R_{\text{short}}$ structures are located in top and bottom of the $BR$ solid line, respectively.

In the following section, we present measurement results on these structures and further discuss the temperature behavior of these resistors and their sensitivity to $W$, $N$, and $L$ over the temperature range of 25 to 200°C.

### 4.3 Measurement Results

We have designed and implemented several different resistor structures ($R_{\text{short}}$, $BR$, and $R_{\text{long}}$) with different desired TCs (ideally Z-TC, N-TC and P-TC) in the range of 100 Ω to 1 MΩ, as listed in Table 4.1 and illustrated in Fig. 4.2. A desired TC specifies a certain resistor length, $L$, and length factor, $LF$. Based on the existence of one degree of freedom in choosing the ratio of $N/W$ for a given $R_{\text{tot}}$, we have implemented several options of $N$ and $W$ (e.g., $N = 1$, $N = 5$, and $N = 20$ with a corresponding increased $W$). We present how this degree of freedom can help the
designers to implement a given resistor in a proper region and make its value more stable over the temperature range of interest.

For a given tolerance of the resistor component, we study the temperature sensitivity of resistor structures in different design regions shown in Fig. 4.2 to $L$, $N$, and $W$. Also, we investigate the sensitivity of the length factor $LF$ to $L$ by implementing 10 different 10 kΩ $BR$ resistors with a length factor $LF = 5$ intentionally varied by ±0.2%, ±0.4%, ±1%, ±2%, and ±10%. Due to the existence of resistor tolerance, as explained before, we obtain a desired TC bound rather than a single TC value.

The temperature range of interest in this work is from 25 to 200°C (limited by the test equipment) and the reported measurements are at 25, 75, 125, 175 and 200°C. During the measurements, for each resistor, we applied 100 different sample currents and measured the voltage across the resistor for each current at each given temperature. Fitting a line into measured voltage/current data, we calculate the resistor value for each temperature.

### 4.3.1 Proper and Sensitive Design Regions

Table 4.2 lists the measurement results of the resistors of Table 4.1; The measured value, resistor tolerance and the temperature coefficient over the temperature range of interest are listed in this table. For each resistor, it is indicated whether the resistor is located either in the proper or sensitive design region. Note that all the regions shown in Fig. 4.2, excluding the proper region, are referred to as sensitive region.

Most of the resistors in the sensitive region introduce large tolerance (close to 3-sigma value of 15% provided by foundry). The measured tolerances have direct impact on the desired TC value as we discuss in the following.
<table>
<thead>
<tr>
<th>#</th>
<th>Region</th>
<th>Type-N</th>
<th>Mes.</th>
<th>Tol. (%)</th>
<th>TC (ppm/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Sensitive</td>
<td>$R_{short}$-1</td>
<td>111 Ω</td>
<td>11</td>
<td>-47</td>
</tr>
<tr>
<td>2</td>
<td>Sensitive</td>
<td>$R_{short}$-5</td>
<td>117 Ω</td>
<td>17</td>
<td>-171</td>
</tr>
<tr>
<td>3</td>
<td>Sensitive</td>
<td>BR-5</td>
<td>108 Ω</td>
<td>8</td>
<td>+116</td>
</tr>
<tr>
<td>4</td>
<td>Sensitive</td>
<td>$R_{long}$-1</td>
<td>110 Ω</td>
<td>10</td>
<td>+302</td>
</tr>
<tr>
<td>5</td>
<td>Sensitive</td>
<td>$R_{long}$-5</td>
<td>106 Ω</td>
<td>6</td>
<td>+222</td>
</tr>
<tr>
<td>6</td>
<td>Proper</td>
<td>$R_{short}$-5</td>
<td>1.13 kΩ</td>
<td>13</td>
<td>-296</td>
</tr>
<tr>
<td>7</td>
<td>Proper</td>
<td>$R_{short}$-20</td>
<td>1.16 kΩ</td>
<td>16</td>
<td>-239</td>
</tr>
<tr>
<td>8</td>
<td>Sensitive</td>
<td>BR-1</td>
<td>1.04 kΩ</td>
<td>4</td>
<td>-30</td>
</tr>
<tr>
<td>9</td>
<td>Proper</td>
<td>BR-5</td>
<td>1.04 kΩ</td>
<td>4</td>
<td>+63</td>
</tr>
<tr>
<td>10</td>
<td>Sensitive</td>
<td>BR-20</td>
<td>1.18 kΩ</td>
<td>18</td>
<td>+349</td>
</tr>
<tr>
<td>11</td>
<td>Sensitive</td>
<td>$R_{long}$-1</td>
<td>1.01 kΩ</td>
<td>1</td>
<td>+68</td>
</tr>
<tr>
<td>12</td>
<td>Proper</td>
<td>$R_{long}$-5</td>
<td>1.01 kΩ</td>
<td>1</td>
<td>+73</td>
</tr>
<tr>
<td>13</td>
<td>Sensitive</td>
<td>$R_{long}$-20</td>
<td>1.01 kΩ</td>
<td>1</td>
<td>+94</td>
</tr>
<tr>
<td>14</td>
<td>Sensitive</td>
<td>$R_{short}$-5</td>
<td>11.83 kΩ</td>
<td>18</td>
<td>-453</td>
</tr>
<tr>
<td>15</td>
<td>Proper</td>
<td>$R_{short}$-26</td>
<td>11.29 kΩ</td>
<td>13</td>
<td>-315</td>
</tr>
<tr>
<td>16</td>
<td>Sensitive</td>
<td>BR-1</td>
<td>11.19 kΩ</td>
<td>12</td>
<td>-116</td>
</tr>
<tr>
<td>17</td>
<td>Proper</td>
<td>BR-5</td>
<td>10.56 kΩ</td>
<td>6</td>
<td>-48</td>
</tr>
<tr>
<td>18</td>
<td>Proper</td>
<td>BR-20</td>
<td>10.30 kΩ</td>
<td>3</td>
<td>-28</td>
</tr>
<tr>
<td>19</td>
<td>Sensitive</td>
<td>$R_{long}$-1</td>
<td>10.30 kΩ</td>
<td>3</td>
<td>+63</td>
</tr>
<tr>
<td>20</td>
<td>Proper</td>
<td>$R_{long}$-5</td>
<td>10.10 kΩ</td>
<td>1</td>
<td>+54</td>
</tr>
<tr>
<td>21</td>
<td>Proper</td>
<td>$R_{long}$-20</td>
<td>10.12 kΩ</td>
<td>1</td>
<td>+89</td>
</tr>
<tr>
<td>22</td>
<td>Sensitive</td>
<td>$R_{short}$-47</td>
<td>115 kΩ</td>
<td>15</td>
<td>-452</td>
</tr>
<tr>
<td>23</td>
<td>Proper</td>
<td>$R_{short}$-255</td>
<td>113 kΩ</td>
<td>13</td>
<td>-355</td>
</tr>
<tr>
<td>24</td>
<td>Sensitive</td>
<td>BR-12</td>
<td>107 kΩ</td>
<td>7</td>
<td>-166</td>
</tr>
<tr>
<td>25</td>
<td>Proper</td>
<td>BR-50</td>
<td>104 kΩ</td>
<td>4</td>
<td>-109</td>
</tr>
<tr>
<td>26</td>
<td>Sensitive</td>
<td>$R_{long}$-1</td>
<td>107 kΩ</td>
<td>7</td>
<td>+28</td>
</tr>
<tr>
<td>27</td>
<td>Proper</td>
<td>$R_{long}$-6</td>
<td>102 kΩ</td>
<td>2</td>
<td>+63</td>
</tr>
<tr>
<td>28</td>
<td>Sensitive</td>
<td>$R_{short}$-472</td>
<td>1.17 MΩ</td>
<td>17</td>
<td>-541</td>
</tr>
<tr>
<td>29</td>
<td>Sensitive</td>
<td>BR-104</td>
<td>1.08 MΩ</td>
<td>8</td>
<td>-186</td>
</tr>
<tr>
<td>30</td>
<td>Proper</td>
<td>BR-533</td>
<td>1.04 MΩ</td>
<td>4</td>
<td>-166</td>
</tr>
<tr>
<td>31</td>
<td>Proper</td>
<td>$R_{long}$-60</td>
<td>1.02 MΩ</td>
<td>2</td>
<td>+55</td>
</tr>
</tbody>
</table>

Table 4.2: Measurement results of the implemented resistors over the temperature range of 25 to 200°C.
4.3.2 Sensitivity to $L$ for Different Resistor Values

As discussed earlier, the resistor component tolerances introduce a TC bound around the desired designed $TC_{tot}$. This bound is tighter for large resistor length. This statement is confirmed by the results of Table 4.2 where by increasing the length of the resistor structure (from minimum length of $R_{short}$ up to large length of $R_{long}$), the tolerance is decreased for every specific resistor value, from 100 Ω to 1 MΩ. For instance, several resistors in the range of 1 kΩ to 1 MΩ are chosen, all from proper region, to compare the TC variation for different length resistors. These are the following resistors from Table 4.2: $R_{short}$ (#7, #15, #23, #28), $BR$ (#9, #17, #25, #30), and $R_{long}$ (#12, #20, #27, #31). Fig. 4.3 depicts the measured $TC_{tot}$ of each resistor to compare the sensitivity of the structure to the length.

![Figure 4.3: Measured $TC_{tot}$ of several $R_{short}$, $BR$, and $R_{long}$ in a range of 1 kΩ to 1 MΩ.](image)

Ideally, all resistors with the same length should have had the same $TC_{tot}$. For
example, all $R_{\text{short}}$ even with different value are designed to have the same temperature variation and $TC_{\text{tot}}$. However, as shown in Fig. 4.3 the $TC_{\text{tot}}$ is not constant and decreases as the size of resistor increases. $R_{\text{long}}$ resistors have the smallest TC variation. The $\Delta TC_{\text{tot}}$ is $-302$, $-103$, and $-19 \text{ ppm/°C}$ for $R_{\text{short}}$, $BR$, and $R_{\text{long}}$, respectively.

4.3.3 Sensitivity to $N$ and $W$ for Different Resistor Values

Considering a fixed length for different value resistors, e.g., $BR$ structures shown in Fig. 4.3, we would like to find the effects of $N$ and $W$ on the $\Delta TC_{\text{tot}}$ and the temperature behavior of the proposed resistors. In order to take into account the tolerance impact on the $TC_{\text{tot}}$ in Eq. (4.4), we add $\Delta TC_{\text{tot}}$ and rewrite this equation as follows:

$$LF = \frac{W}{N} \cdot \frac{\Delta TC_{\text{tot}} \cdot R_{\text{tot}}}{TC_{\text{core}} \cdot R_{u,\text{core}}} + \left| \frac{-TC_{\text{cnt}} \cdot R_{u,\text{cnt}}}{TC_{\text{core}} \cdot R_{u,\text{core}}} \right|$$

(4.10)

For a specific $LF$, the first term of Eq. (4.10) depends on the overall tolerance and the second term is a positive constant. To increase the value of such resistor from 1 kΩ to 1 MΩ, one can either increase $N$, or decrease $W$, or a combination of the two. In the absent of contact resistors, by doubling the overall $\frac{W}{N}$ ratio the $R_{\text{tot}}$ is halved. However, as explained earlier, relation between $\frac{W}{N}$ and $R_{\text{tot}}$ is not quite linear (due to the existence of contacts), and hence, the $R_{\text{tot}}$ and $\frac{W}{N}$ can not be canceled out in Eq. (4.10). Thus, $LF$ is a weak function of $\frac{W}{N}$ which effects the overall $\Delta TC_{\text{tot}}$. This behavior is more pronounced for large number of contacts (fingers) $N$ in the large-size large-value design region. That is why for small $N$, the P-TC of core resistor has more contribution on overall $TC_{\text{tot}}$, as compared to large $N$ where contact resistors
contribute to a N-TC and decrease the overall $TC_{tot}$.

### 4.3.4 Sensitivity to $\Delta L$ for a Specific Resistor Value with a Fixed $L$

10 different 10 kΩ $BR$ resistors with a length factor $LF = 5$ with intentional length variation of $\pm 0.2\%$, $\pm 0.4\%$, $\pm 1\%$, $\pm 2\%$, and $\pm 10\%$ are implemented as listed in Table 4.3.

<table>
<thead>
<tr>
<th>#</th>
<th>$\Delta L$</th>
<th>$L(\mu m)$</th>
<th>$W(\mu m)$</th>
<th>Mes.(kΩ)</th>
<th>TC(ppm/℃)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>+10%</td>
<td>5.53</td>
<td>4.01</td>
<td>10.28</td>
<td>-30</td>
</tr>
<tr>
<td>33</td>
<td>+2%</td>
<td>5.13</td>
<td>3.73</td>
<td>10.31</td>
<td>-18</td>
</tr>
<tr>
<td>34</td>
<td>+1%</td>
<td>5.08</td>
<td>3.7</td>
<td>10.31</td>
<td>-15</td>
</tr>
<tr>
<td>35</td>
<td>+0.4%</td>
<td>5.05</td>
<td>3.68</td>
<td>10.29</td>
<td>-11</td>
</tr>
<tr>
<td>36</td>
<td>+0.2%</td>
<td>5.04</td>
<td>3.67</td>
<td>10.31</td>
<td>-15</td>
</tr>
<tr>
<td>37</td>
<td>−0.2%</td>
<td>5.02</td>
<td>3.66</td>
<td>10.30</td>
<td>−14</td>
</tr>
<tr>
<td>38</td>
<td>−0.4%</td>
<td>5.01</td>
<td>3.68</td>
<td>10.29</td>
<td>−28</td>
</tr>
<tr>
<td>39</td>
<td>−1%</td>
<td>4.98</td>
<td>3.64</td>
<td>10.29</td>
<td>−27</td>
</tr>
<tr>
<td>40</td>
<td>−2%</td>
<td>4.93</td>
<td>3.60</td>
<td>10.31</td>
<td>−16</td>
</tr>
<tr>
<td>41</td>
<td>−10%</td>
<td>4.53</td>
<td>3.33</td>
<td>10.34</td>
<td>−19</td>
</tr>
</tbody>
</table>

Table 4.3: Sensitivity to $\Delta L$ for 10 different 10 kΩ $BR$ resistors with $N = 20$, nominal $L = 5 \mu m$, and $\Delta L$ of $\pm 0.2\%$, $\pm 0.4\%$, $\pm 1\%$, $\pm 2\%$, and $\pm 10\%$ over the temperature range of 25 to 200℃.

The $W$ of these resistor are adjusted so that the resistors have about the same value while their temperature behavior stays the same as the $W$ change is the same for both core and contact resistor (refer to Eq. (4.2)).

Note that for $LF = 5$, the intentional variation of 20%, i.e., $\pm 10\%$ introduces the overall measured $TC_{tot}$ variation of less than $-20$ ppm/℃. These results show a weak sensitivity of the proposed design structure to the variation of $L$ for a specific length.
4.3.5 Sensitivity to Different $N$ and $W$ of Multi-Finger Options for a Specific Resistor Value

As discussed earlier, we have one degree of freedom to select from different combination of $N$ and $W$ for multi-finger structures. This helps us to choose structures which are located in the proper region to obtain a better temperature stability rather than using a structure in the sensitive region which is more process dependent as shown in Fig. 4.2. For example, consider three 1 kΩ $BR$ with different $N$ of 1, 5, and 20 (#8, #9, #10 in Table 4.2). The #9 resistor is in the proper region, while the other two, namely, resistors #8 and #10 are in sensitive regions. Note that the measured TC for these two sensitive structures are $-30$ and $+349$ ppm/$^\circ$C which introduce a large TC variation as compared to $+63$ ppm/$^\circ$C, the TC of #9 resistor.

As another example, consider three $BR$ with different $N$ of 1, 5, and 20 with the value of 10 kΩ (#16, #17, #18 in Table 4.2). In this case, only the #16 resistor is in a sensitive region, while the other two, namely, #17 and #18 resistors are in the proper region. Note that the measured TC for these two structures is $-48$ and $-28$ ppm/$^\circ$C, respectively, and they have a smaller $\Delta TC$ as compared with the $\Delta TC$ of any of these two resistors and that of resistor #16 with TC of $-116$ ppm/$^\circ$C. These two examples are for $BR$, we provide two more examples for $R_{long}$ and $R_{short}$ as follows.

Fig. 4.4 compares the temperature behavior of two 10 kΩ $R_{long}$ multi-finger structures with $N = 5$ and $N = 20$ (#20, #21 in Table 4.2) over the temperature range of 25 to 200 $^\circ$C with overall TC of $+54$ and $+89$ ppm/$^\circ$C, respectively.

Fig. 4.5 compares the temperature behavior of two 1 kΩ $R_{short}$ multi-finger structures with $N = 5$ and $N = 20$ (#6, #7 in Table 4.2) over the temperature range of
25 to 200 °C with overall $TC$ of $-296$ and $-239$ ppm/°C respectively.

Considering all these examples, the sensitivity of the temperature behavior to $\frac{W}{N}$ for all $R_{short}$, $BR$, and $R_{long}$ resistors (each having a fixed resistor value and located in the proper region) is small. The reason for such a low sensitivity can be attributed to Eq. (4.10). These overall $TC_{tot}$ variations are reasonably less than what argued above because in this case for a fixed resistor value, both $W$ and $N$ are increased (decreased) proportionally and the ratio of $\frac{W}{N}$ is constant. This is in contrast to the previous scenario where the resistor values were different and $\frac{W}{N}$ ratio is not constant and $W$ and $N$ change in opposite directions (when $W$ increases $N$ decreases).
4.3.6 Large-Valued Resistors at High Temperature

Consider three 100 kΩ resistors, namely, $R_{\text{short}}$, $BR$, and $R_{\text{long}}$ (#23, #25, #27 in Table 4.2) all in the proper region. Fig. 4.6 shows the measured temperature behaviour of these multi-finger resistor structures. Note that for temperature above 175°C the rate of change of resistance versus temperature changes, regardless of their $L$, $W$, and $N$. That is, the resistance decreases. Note that $R_{\text{long}}$ has a small $N$ of 6, while $BR$ and $R_{\text{short}}$ have a relatively large $N$ of 50 and 255, respectively. This behavior is more pronounced for larger size resistor of 1 MΩ (#28, #30, #31 in Table 4.2) as shown in Fig. 4.7.

These drastic decreasing of the linear temperature behavior of such large-value resistors with relatively large $\frac{N \cdot L}{W}$ can be related to the N-TC change of contact
Figure 4.6: Measured temperature behavior of 100 kΩ $R_{\text{short}}$, $BR$, and $R_{\text{long}}$ multi-finger structures over the temperature range of 25 to 200°C.

Figure 4.7: Measured temperature behavior of 1 MΩ $R_{\text{short}}$, $BR$, and $R_{\text{long}}$ multi-finger structures over the temperature range of 25 to 200°C.
resistor, $TC_{\text{cnt}}$, which presents a new more negative TC above 175 °C. This behavior, however, is not considered in the model provided by foundry and might be related to the physical structures of these contacts.

### 4.3.7 Summary of Contributions

The proposed technique is suited for implementing a given resistor with a desired TC. Unlike the other work in the area, we not only consider the impact of the contact resistors but also take advantage of the temperature coefficient of contact resistors to control the overall temperature behavior. For example, the $TC_{\text{core}}$ and $TC_{\text{cnt}}$ in the technology used in this work are on the order of +100 and −1000 ppm/°C, respectively.

A multi-finger resistor structure which can be used as a standard structure for implementing different resistors with different temperature behavior is introduced as shown in Fig. 4.1. Also, several design regions (proper and sensitive) based on the geometry of a resistor structure ($L$, $W$, and $N$) are defined as illustrated in Fig. 4.2.

The measured results prove the validity of the proposed technique and also provide the temperature sensitivity of the design to the geometry of the resistor structure. With the nominal resistor tolerance of 15% (provided by the foundry), we have measured the temperature behavior of several resistors. For example, for a 10 kΩ resistor, we obtained a measured TC ranging from −315 ppm/°C (for $R_{\text{short}}$) to +89 ppm/°C (for $R_{\text{long}}$) with a zero-TC design ($BR$ structure) achieving a TC of −28 ppm/°C. Note that this TC is more than 3 times smaller that the nominal core resistor $TC_{\text{core}}$ for the technology used. Fig. 4.8 presents the measured temperature behavior of $R_{\text{short}}$, $BR$, and $R_{\text{long}}$ (#15, #18, #21 in Table 4.2).

As discussed earlier the resistor tolerance affects the design sensitivity to $L$ and
Figure 4.8: Measured temperature behavior of 10 kΩ $R_{\text{short}}$, $BR$, and $R_{\text{long}}$ multi-finger structures over the temperature range of 25 to 200 °C.

As a result, using resistors with less tolerance can reduce the TC sensitivity of the resistor. Also, for a fixed tolerance, increasing the length of the resistor can effectively reduce the sensitivity of the design. For example, we measured an overall $\Delta T C_{\text{tot}}$ of $-19 \text{ ppm/}^\circ\text{C}$ for a $R_{\text{long}}$ resistor in a range of 1 kΩ to 1 MΩ. For the $BR$ with a length factor of $BF = 5$, however, such $\Delta T C_{\text{tot}}$ is increased to $-103 \text{ ppm/}^\circ\text{C}$. Note that if we use another type of resistor or another CMOS technology in which the $BF$ is increased to 25 (equal to the length factor of the above-mentioned $R_{\text{long}}$), one can obtain the same $\Delta T C_{\text{tot}}$ of $-19 \text{ ppm/}^\circ\text{C}$ for a $BR$ resistor in the range of 1 kΩ to 1 MΩ. This can also be achieved by using another resistor that has a 5 times larger $T C_{\text{cnt}} \cdot R_{u,\text{cnt}}$ term (refer to $BF$ equation given in Eq. (4.5)).

The sensitivity of temperature behavior of the structure to $L$ is low. For example, we showed that for a 10 kΩ structure with $N = 20$ and nominal $L$ of 5 µm, if $L$
changes by 20% the TC variation is $-19 \ ppm/^\circ C$. Also, the measured sensitivity to $\frac{W}{N}$ for a specific resistor value with a multi-finger structure is small, e.g., for two 10 kΩ $BR$ with $N = 5$ (#17 in Table 4.2) and $N = 20$ (#18 in Table 4.2), the overall measured $\Delta TC_{tot}$ is $-20 \ ppm/^\circ C$.

Based on one degree of freedom for choosing $\frac{W}{N}$ of the proposed multi-finger resistor structures, the designers can choose structures that are located in the proper design region shown in Fig. 4.2.

For large-value resistors and for temperature above 175 °C, the TC decreases substantially regardless of the $L$, $W$, and $N$ of the resistor. This can be attributed to the N-TC behavior of contact resistors and may be alleviated by using different materials or types of contacts (e.g., using different type of resistor or different technology).

The technique and analysis presented in this work are general and can be used for any two types of resistors with opposite temperature coefficients, be it monolithic or discrete. Also, if the TCs are not opposite (both are positive or negative), the presented technique can still be used to find the overall TC.

4.4 Chapter Summary

The previous design technique to implement monolithic resistors with a desired TC, over a wide temperature range, by using a core and contact resistors with opposite TC is extended and improved. A standard structure is provided based on a multi-finger resistor structure with finger length, $L$, finger width, $W$, and number of fingers, $N$. Different design regions based on geometry of the structure along with the resistor tolerance provided by foundry are considered for analyzing the sensitivity of the design to $L$, $W$, and $N$. Several resistors are designed and implemented in the range of 100
Ω to 1 MΩ. Techniques to reduce such sensitivities are proposed. The measurement results over the temperature range of 25 to 200 °C confirm the validity of the proposed analysis and design technique.

In the next chapter, we propose a capacitive temperature-compensation technique to implement a high-temperature oscillator and discuss the performance improvement of the oscillator using such technique.
Chapter 5

Resistive and Capacitive Temperature Compensated Oscillator

Reliable high-temperature CMOS oscillators are required for clock and timing signal generation in several analog, mixed-signal, and digital applications including data acquisition for aerospace, automotive control, oil field instrumentation, and pulp and paper industry [58]. Although quartz crystal oscillators are very stable versus temperature and supply voltage variations [59], they can not be integrated in a CMOS system on-a-chip (SoC) and as a result the overall size and cost of the system increases. In general at high temperature, analog circuits implemented in a bulk CMOS process mainly suffer from reduced charge carrier mobility, transistor’s threshold voltage drop, and increased junction-to-substrate leakage current. An alternative technology for high-temperature applications, is silicon-on-insulator (SOI) process due to its low leakage current and temperature-resistant threshold voltage [60], but, SOI is not as low cost as CMOS [61]. There are several CMOS oscillators presented in [62]-[63] that target applications with operating temperature up to 160°C (a relatively large leakage current occurs at higher temperature around 150°C which remarkably degrades the circuit performance [16]). For the purpose of the application considered in this work, namely monitoring environmental variables such as pressure, temperature, conductivity, etc inside a pulp and paper digester, the circuit has to reliably operate up to ~180°C. Therefore, stable operation of circuit blocks well beyond 150°C in a low-cost CMOS process is desired which needs a compensation technique to mitigate
the impact of excessive leakage current at high temperature above 150°C. Using a low-cost CMOS process is also attractive for the purpose of application considered in this work as well as other applications where disposable portable units are desired.

Various temperature compensation techniques have been already presented. These techniques typically require an elaborate circuitry and/or a significant area overhead. For instance, in [64] an integrator-based power averaging feedback (PAF) to compensate the frequency variation of a relaxation oscillator is proposed. The PAF approach minimizes the impact of the comparator-delay variation on output frequency. The frequency variation is further reduced by using a temperature-compensated +4.5 mV/100°C $V_{ref}$ generator, by using a combination of diffused and polysilicon resistors with different sensitivities to temperature. In [65], a Wienbridge oscillator with two gain boosting amplifiers and an amplitude regulator is presented. Applying advanced design techniques for amplitude regulation, in this work the oscillation frequency is mainly a function of the temperature-stable passive RC network. The compensation technique presented in [66] consists of a threshold voltage sensing circuit along with an op-amp buffer stage to create a control voltage which adjusts the replica feedback bias circuit to control the frequency of a ring oscillator. In [67], a constant-$g_m$ bias along with a regulator is used for temperature compensation of a compact two-stage ring oscillator. For timing capacitors, using gate capacitance of CMOS transistors along with constant-$g_m$ biasing minimizes the effect of process and temperature variation on the free running frequency. A supply-regulated ring oscillator with a temperature compensation feedback loop consisting of a frequency-to-voltage converter and a VCO along with a bandgap voltage reference is used in [68] to minimize the frequency sensitivity to supply and temperature variations. The proposed circuit used sub-threshold bias circuits to further reduce the power. Also, [69] introduces a relax-
ation oscillator using only one comparator along with a voltage regulator and a pulse
generator to control charging and discharging of a capacitor for low-power applica-
tions. The scheme utilizes current sharing to reduce power consumption. Another
elegant temperature compensation technique based on electron mobility in a MOS
transistors which uses one-point or two-point trimming is presented in [70]. Employ-
ing a bandgap temperature sensor, the authors use one-point or two-point trimming
to achieve a stable output frequency. In all these designs, typically, the temperature
compensation block occupies a relatively large area as compared with that of the core
oscillator itself and introduces extra design overhead. There are also a few patents
on this topic. For example: in [71] an adjustable external DC voltage and a varac-
tor are used to compensate temperature variation of a crystal oscillator. In [72] a
temperature compensation circuit using a control transistor provides a voltage to the
control terminals of the delay stages which is inversely proportional to the threshold
voltage of the control transistor, [73] is based on an elaborate compensation circuitry
and an external precise resistor. In [74] a compensation technique is presented that
either includes or excludes a current source to compensate for the adverse effects of
temperature on the output frequency.

In this chapter, temperature compensation techniques with low complexity are
presented for relaxation oscillators. The output frequency of relaxation oscillators
directly depends on a resistor-capacitor product. Therefore we proposed two resis-
tive and capacitive compensation techniques. A typical monolithic resistor in CMOS
process has core and contact each having certain TC. The resistive compensation
 technique is based on using a core resistor which has contact with opposite TC. By
changing the number of contacts in a multi-finger resistor structure, we designed and
used a bias resistor with a low TC. The capacitive compensation technique is based
on adjusting the timing capacitance over the temperature range of interest. We pro-
posed how one can use a non-linear capacitance to compensate for high-temperature
junction leakage current which mitigates the frequency drift over temperature. For
this purpose, the oscillator capacitor is divided into a fixed capacitor and a non-linear
variable capacitor (varactor). The leakage current impact is mitigated by controlling
the varactor capacitance using the available bias reference, i.e, no additional circuitry
is required for compensation. Therefore the output frequency is stabilized by em-
ploying a low-TC resistor along with a non-linear varactor. As a proof-of-concept
a 1-MHz relaxation oscillator is implemented in a 0.13-μm standard CMOS process
that operates over the temperature range from 25 to 200°C.

This chapter is organized as follows. In Section II, we overview the adverse effects
of high temperature on CMOS circuit operation. In Section III, the oscillator circuit
topology is presented. The circuit design and associated temperature-compensation
techniques are explained in Section IV. In Section V, measured performance of the pro-
posed oscillator is compared with that of stat-of-the-art designs. Section VI presents
concluding remarks.

5.1 Relaxation-Oscillator Circuit Topology

A generic block diagram of a relaxation oscillator [63] is shown in Fig. 5.1. The
oscillator consists of a bias reference, a timing circuit, a comparator block, and an SR
latch. Using a resistor R, the bias reference circuit generates two correlated references,
a reference voltage and a reference current, namely, $V_{REF}$ and $I_{REF} = V_{REF}/R$.

The simplified timing waveforms of the oscillator are illustrated in Fig. 5.2. Since
the circuit is symmetrical, $(T_1 = T_2 = T_{osc}/2, C_1 = C_2 = C)$, the period of oscillation
is $T_{osc} = T_1 + T_2 = 2T_1 = 2T_2$. The ramp voltage for each capacitor is given by

$$\frac{dV}{dt} = \frac{I_{REF}}{C} \quad (5.1)$$

Assuming that the comparators are ideal and $V_{REF} = R \cdot I_{REF}$, the ramp interval time for each capacitor can be written as

$$\frac{T_{osc}}{2} = \frac{V_{REF} \cdot C}{I_{REF}} = RC \quad (5.2)$$

Eq. (5.2) shows that to the first order of approximation, the oscillation frequency
Figure 5.2: Relaxation-oscillator simplified timing waveforms.

is independent of both reference voltage and reference current and is set by the time constant, RC. Therefore, if the comparator is ideal and assuming the $I_{REF}$ in the bias reference circuit is equal to the $I_{REF}$ in the timing circuit, only a temperature stable resistor and capacitor are required for a stable oscillation.

In the following section, we will discuss how this relaxation oscillator suffers from above-mentioned high-temperature circuit impairments and explain the proposed temperature compensation techniques.
5.2 Oscillator Design and Temperature Compensation Techniques

The bias circuit and timing circuit shown in Fig. 5.3 are typically used in relaxation oscillators.

![Bias Reference and Timing Circuit Diagram](image)

Figure 5.3: Typical bias reference and timing circuit of relaxation-oscillator.

The start-up circuitry ensures proper functionality of the bias reference by driving the circuit out of its zero current state (degenerate state) when the supply is turned on. It consists of a cascade of diode-connected transistors which ensure that when the supply is turned on there will be a non-zero current following through current mirror consisting of $M_1$ and $M_3$. Once the bias reference is properly operational, i.e., $I_{REF}$ flows through $M_3$, the diode-connected transistors in the start-up circuitry will automatically turn off (the operation is similar to classic start-up circuits such as the...
one discussed in [21]. In the nominal operation of the reference circuit, the reference current $I_{REF}$ flows through $R$ and generates the reference voltage $V_{REF}$ to be used as the comparator reference level. This current is also mirrored through $M_3$ and $M_5$ to provide the same $I_{REF}$ for timing circuit to alternately charge capacitors in every other half-cycle of oscillation. Note that to minimize the mismatch in $I_{REF}$ in the bias reference and the timing circuit, one can use a cascode current mirror. To the first order of approximation, $I_{REF}$ can be expressed by

$$I_{REF} = \frac{1}{2} \mu_n(T) C_{ox}(\frac{W}{L})_2(V_{REF} - V_{TH}(T))^2$$

(5.3)

where $(W/L)_2$ is the aspect ratio of $M_2$ and $C_{ox}$ is the gate-oxide capacitance per unit area. From Eqs. (1.1) and (1.5), the temperature dependency of $\mu$ is proportional to $T^{-1.5}$ while that of $V_{TH}$ is proportional to $-T$. Therefore, $I_{REF}$ decreases as temperature increases. Since $V_{REF} = R \cdot I_{REF}$, the $V_{REF}$ is also decreased as temperature increases. Based on Eq. (5.2), the oscillation frequency, however, is defined by RC and is independent of $I_{REF}$ and $V_{REF}$. Note that this claim is valid if we have ideal switches to charge capacitors (i.e., no impairments in transistors $M_7$ and $M_9$). At high temperature, however, these transistors have non-negligible leakage currents, especially diffusion current above 150°C. This leakage current, in turn, decreases the effective $I_{REF}$ in Eq. (5.2) and increases the capacitor charging time, $T_{osc}$, which in essence, decreases the oscillation frequency.

In relaxation oscillator design, the three main temperature-related concerns are as follows. First, the temperature drift of passive components, namely, resistors and capacitors, which directly affect $T_{osc}$ and output frequency based on Eq. (5.2). Given that temperature coefficient of capacitors are usually negligible, the proposed
technique focuses on resistor TC and mitigates its impact on the output frequency. Second, the leakage current of CMOS switches that are used to charge timing capacitors. Such an adverse effect is alleviated by the proposed capacitance compensation technique. Third, the comparator non-idealities and reduced gain at high temperatures which can be attributed to the threshold voltage drop of transistors. We will discuss on how to improve these impairments on the comparator design section. Note that the variation of $I_{REF}$ over temperature has relatively the same impact on the other currents in the relaxation oscillator (which are generated from $I_{REF}$ using current mirrors) and $V_{REF} = R \cdot I_{REF}$ and based on Eq. (5.2), thus the output frequency is ideally independent of $I_{REF}$.

To verify the proposed techniques, two oscillators (uncompensated and compensated) with nominal oscillation frequency of 1 MHz are implemented in a 0.13-µm CMOS process. The uncompensated oscillator (shown in Fig. 5.3) consists of a typical available monolithic resistor with a certain TC and two fixed metal-insulator-metal (MIM) capacitors. Note that TC of the MIM capacitors is very small (on the order of 10 ppm/°C) and is thus neglected in this work.

For the compensated oscillator both resistive and capacitive compensation techniques have been used as shown in Fig. 5.4. The resistive compensation is based on the use of a resistor which has a low TC [40]. The capacitive compensation is based on using an accumulation-mode varactor (nCap) in parallel with the main capacitor which is a fixed capacitor implemented using a metal-insulator-metal capacitor (MIMcap) as shown in Fig. 5.4. The nCap accumulation-mode varactor is a nonlinear capacitor, e.g., an nmos-type device inside an N-well, that is, two n-diffusion regions within an Nwell [75]. To further reduce the chip area, the varactor is placed under the fixed MIMCap. The proposed techniques are discussed in the next two
5.2.1 Resistive Temperature Compensation Technique

A typical multi-finger poly resistor in the 0.13-µm CMOS technology has a core TC that is on the order of 100 ppm/°C. In practice, however, the overall TC of the resistor is different from the core TC due to the effect of the contacts. In the same 0.13-µm CMOS process, the contact TC is on the order of −1000 ppm/°C. The proposed resistive temperature compensation is based on a resistor structure presented in [40] for designing resistors with near-zero TC. The structure adjusts the overall TC of the entire resistor by choosing the proper number of contacts. A typical
multi-finger poly resistor that we have used in the bias reference circuitry of the uncompensated oscillator has an overall TC of $-104 \text{ ppm}/\degree C$. For the compensated oscillator, however, we used a resistor [40] that has an improved TC of $-34 \text{ ppm}/\degree C$.

In the prototype designs, the resistor is 500 kΩ for both uncompensated and compensated oscillators. The number of contacts used in each resistor, however, varies and the uncompensated design contains 1320 contacts, while compensated design contains 440 contacts. For the compensated design, the 500 kΩ resistor is a combination of a total of 454.7 kΩ core resistance and a total of 45.5 kΩ contact resistance. To confirm that the proposed multi-finger resistors have a robust temperature behavior, based on the proposed temperature-stable resistor structure, we have designed and implemented several test resistors with near-zero TCs. Specifically, 10 different 10 kΩ resistors with a core length of 100 µm, a contact number of 40 and an intentional length variation of $\pm 0.2\%$, $\pm 0.4\%$, $\pm 1\%$, $\pm 2\%$, and $\pm 10\%$ are implemented. Despite the fact that the maximum intentional variation of 20%, i.e., $\pm 10\%$, is considered, the overall variation of measured TCs among all these resistors is less than 20 ppm/°C as shown in Fig. 5.5.

Note that if we consider series combination of these 10 resistors (nominal value of 100 kΩ) the worst case variation of the overall temperature coefficient will still be 20 ppm/°C.

This can be explained as follows: Assume the TC of a resistor structure has a variation of $\Delta TC$ with respect to its nominal value (e.g., in this work, the maximum $\Delta TC$ is $\Delta TC_{\text{max}} = 20 \text{ ppm}/\degree C$). The overall TC of a series combination of $n$ such resistor structures can be calculated from the following equation:
Figure 5.5: Different 10 kΩ resistors with a core length of 100 µm, a contact number of 40 and an intentional length variation of ±0.2%, ±0.4%, ±1%, ±2%, and ±10%.

\[ TC_{tot} = \sum_{i=1}^{n} TC_i \cdot R_{i,nom} \sum_{i=1}^{n} R_{i,nom} \]  \hspace{1cm} (5.4)

where \( R_{i,nom} \) \((i = 1, 2, \ldots, n)\) is the nominal resistance of the \(i^{th}\) component of the series combination and \(TC_i\) is the \(TC\) of the \(i^{th}\) component. Given that \(R_{i,nom}\)'s are positive values, the upper bound on the worst-case \(TC_{tot}\) is achieved when all \(TC_i\)'s are at their maximum. That is,

\[ \Delta TC_{tot,max} \leq \sum_{i=1}^{n} \Delta TC_{i,max} \cdot R_{i,nom} \sum_{i=1}^{n} R_{i,nom} \]  \hspace{1cm} (5.5)

Assuming that all \(R_{i,nom}\)'s are chosen to be equal, then, \(\Delta TC_{tot,max} = \frac{\sum_{i=1}^{n} \Delta TC_{i,max}}{n}\).

Now, if we assume that the worst-case \(TC\) variation of all the components is \(\Delta TC_{max}\),
then $\Delta T C_{\text{tot}, \text{max}} \leq \frac{n \cdot \Delta T C_{\text{max}}}{n} = \Delta T C_{\text{max}}$. The measured results confirm the robust temperature behaviour of the proposed resistor structure.

Since the bias resistor of the uncompensated oscillator shows a negative TC, based on Eq. (5.2) it means that by increasing temperature the oscillation frequency also increases as expected from $f_{\text{osc}} = 1/T_{\text{osc}} = 1/(2RC)$. For the compensated oscillator, however, by using a less temperature-sensitive resistor (about 3 times lower TC) we improve the temperature stability of the oscillator. Fig. 5.6 illustrates how the use of low-TC resistor stabilizes the output frequency of the relaxation oscillator. The improvement achieved by using this technique will be discussed in the measurement section.

Figure 5.6: Illustration on how the use of low-TC resistor stabilizes the output frequency of the relaxation oscillator.

As presented in [76], the dangling bond effect of polysilicon resistors typically affects the resistivity of the structure at beyond $200^\circ$C and changes (reduces) the
sheet resistance of the polysilicon. Note that 1) as explained in the introduction, in our case, this design is intended for applications with ambient temperature of up to 180°C and thus for this particular application it is unlikely that the design operates at 200°C even for a short period of time; 2) at high temperatures the leakage current increases which in turn reduces the frequency of operation (as will be discussed in Section V). At the same time as temperature increases to the range where dangling bond effect affects the performance of the circuit, the decrease in the resistor values because of the dangling bond effect tend to increase the frequency of operation and therefore one may be able to take advantage of this frequency increase for frequency compensation.

5.2.2 Capacitive Temperature Compensation Technique

As discussed earlier, we need to consider the leakage current of transistor switches and include its effect in Eq. (5.2). The capacitive compensation is a technique that we propose to achieve this goal. Since by increasing temperature, the switch leakage current is increased non-linearly, with larger variations at high temperature especially above 150°C, one can use a non-linear variable capacitor and control the amount of this capacitor to compensate for the effect of leakage current in Eq. (5.2). Such leakage current decreases the oscillator frequency over temperature, with much stronger impact and faster drop in frequency above 150°C.

Based on Eq. (5.3), the $I_{REF}$ and consequently the $V_{REF}$ decrease by increasing temperature. One can use a varactor in parallel to the timing capacitor of the oscillator and control the overall capacitance by a voltage proportional to $V_{REF}$. In this way, when temperature increases the effective capacitance of the oscillator decreases and thus the reduction in this capacitance, increases the output frequency to compen-
sate for the switches leakage current. Fig. 5.7 illustrates how the proposed capacitive compensation technique stabilizes the output frequency of the relaxation oscillator. The non-linear characteristic of nCap is based on foundry-provided information [77].

![Figure 5.7: Illustration on how the proposed capacitive compensation technique stabilizes the output frequency of the relaxation oscillator.](image)

Since $V_{REF}$ is connected to one of the inputs of the comparator and acts as the comparison reference level, the value of $V_{REF}$ affects the trip point of the comparator, and thus the other input of the comparator (the ramp signal in Fig. 5.2) changes from 0 V to $V_{REF}$. Therefore, we use this input ($V_{ramp}$) of the comparator whose average value is a function of $V_{REF}$, as the control voltage of the nCap variable capacitor. By proper choice of the size of nCap (ratio of the total nCap capacitance to the overall capacitance), this compensation approach improves temperature stability of the relaxation oscillator, especially at high temperature (beyond 150°C).

Let us explain the compensation approach through an example. For the proof-of-concept design presented in Section V, over the temperature range of 25 to 200°C,
$V_{REF}$ (also used as the varactor control voltage) changes from 550 mV to 470 mV. The nominal value of the fixed (MIM) capacitor portion is 220 fF. The varactor (nCap) capacitance is 730 fF when $V_{REF}$ is 550 mV at 25 °C, and it slowly decreases to 700 fF for $V_{REF} = 493$ mV at about 150 °C and rapidly drops to 650 fF when $V_{REF}$ is 470 mV at 200 °C. The ratio of the total varactor capacitance to fixed MIM capacitance can be adjusted through design iteration. Therefore, using this capacitive compensation, one can improve the temperature stability of the oscillator frequency. We will further discuss this in the measurement section.

5.2.3 High Temperature Comparator Design

For both uncompensated and compensated oscillator, we use the same comparator block which is designed for high temperature. For the purpose of clarity and brevity Fig. 5.8 depicts only one of the identical two-stage comparators (the working principle of the second comparator is exactly the same).

In the first gain stage amplifier, since $V_{REF}$ is provided by the bias reference, the same drain current in $M_2$ (i.e. $I_{REF}$) of Fig. 5.4 is mirrored to the comparator reference $M_{12}$. The drain current of $M_{12}$ is mirrored via $M_{13}$ to $M_{11}$.

The common-drain node of $M_{10}$ and $M_{11}$ ($V_{fast1}$) is the output of the first stage. $M_{10}$ gate voltage ($V_{ramp1}$) is reset during half the cycle and is ramping up during the other half. When the gate voltage is less than the gate voltage of $M_{12}$ (i.e. bias reference voltage, $V_{REF}$) the comparator output is high. When $V_{GS10}$ is equal to $V_{REF}$, the comparator trip point has been reached, and the output transits to low.

The gain of this stage is proportional to $g_m$ of $M_{10}$ which can be approximated by
Figure 5.8: Two-stage comparator designed for relaxation oscillator to mitigate the high temperature impairments.

\[ g_m = \frac{2I_{REF}}{V_{REF} - V_{TH}} \]  \hspace{1cm} (5.6)

Since based on Eq. (1.5) and Eq. (5.3), \( V_{TH} \), \( V_{REF} \) and \( I_{REF} \) all decrease as temperature increases, therefore, \( g_m \) and subsequently the gain also decreases as temperature increases. By adding the second gain stage one can mitigate this gain loss to provide a steeper transition in the transfer characteristic of the comparator (closer to ideal comparator). Transistors \( M_{16} - M_{19} \) construct a replica copy of the output stage (transistors \( M_{20} - M_{23} \)) and are used to provide the proper bias for the transistors \( M_{20} \) and \( M_{21} \) to make sure the decision threshold of the comparator is set at \( V_{REF} \) (i.e., the output of the comparator toggles when \( V_{ramp1} \) crosses \( V_{REF} \)). The second
gain stage output feeds the reset input of the latch which will be used to turn on/off switches in the timing circuit shown in Fig. 5.4.

5.2.4 Overall Delay Impact of Comparator and Latch

In the derivation of Eq. (5.2), we have assumed that the delay of the comparator block and that of the SR latch stage are negligible. To study the impact of such delays on the output frequency, one can rewrite Eq. (5.2) to include the overall delay due to the comparator and latch stages, $D_{tot}$, i.e., the $T_{osc} = T_1 + D_{tot} + T_2 + D_{tot} = 2(RC + D_{tot})$. By proper design (sizing of transistors and choice of bias current of the comparator and latch) one can minimize $D_{tot}$. In this work, the comparator and latch are designed such that $D_{tot} < 1/20 \times RC$ to mitigate the dependency of output frequency to $D_{tot}$. Note that $D_{tot}$ varies over temperature due to reduction in the gain of the comparator (caused by threshold voltage drop) and extra delay of SR latch (caused by increased leakage current). We have increased the gain of the comparator by adding a second gain stage. Furthermore, we have designed the latch to have a relatively high short-circuit current to mitigate the impact of leakage current. In the proposed design, the maximum variation of $D_{tot}$, $\Delta D_{tot}$, over the temperature range of interest is less than ±5%. The impact of $\Delta D_{tot}$ on the oscillation period (output frequency) can be found as follows:

$$T_{osc} + \Delta T_{osc} = 2[RC + D_{tot}(1 + \Delta D_{tot})]$$ \hspace{1cm} (5.7)

Since $D_{tot} < 1/20 \times RC$ and $\Delta D_{tot} < \pm5\%$, the maximum $\Delta T_{osc}$ can be calculated using the following steps:
\[ T_{osc} + Max(\Delta T_{osc}) = 2[RC + \frac{1}{20}RC(1 \pm 5\%)] \]  (5.8)

where \( T_{osc} \) is

\[ T_{osc} = 2RC(1 + \frac{1}{20}) = 2RC(1.05) \]  (5.9)

and

\[ Max(\Delta T_{osc}) = 2RC(\pm 0.25\%) \]  (5.10)

and since \( f_{osc} = \frac{1}{T_{osc}} \), then

\[ \frac{\Delta f_{osc}}{f_{osc}} \approx -\frac{\Delta T_{osc}}{T_{osc}} = \frac{0.25\% - (-0.25\%)}{1.05} < 0.5\% \]  (5.11)

Eq. (5.11) shows that in this work the impact of the variation of the overall delay of both comparator and latch circuitry, i.e., \( \Delta D_{tot} \), on the output frequency over the temperature range of interest is less than 0.5\% which is indeed negligible for the target application.

### 5.3 Measurement Results

Both uncompensated and compensated oscillators are designed and fabricated in a 0.13-\( \mu \)m CMOS technology (a chip micrograph is shown in Fig. 5.9). Both oscillators are designed to operate from a coin size battery that after regulation provides a 2.5 V nominal supply. The load of the oscillator is an impedance consisting of parallel combination of a 15 pF capacitor and 1 M\( \Omega \) resistor (typical input impedance of a oscilloscope). The overall compensated oscillator area including the output driver is 80 \( \mu \)m by 90 \( \mu \)m (7200 \( \mu \)m\(^2\)), while the uncompensated oscillator occupies 75 \( \mu \)m
Figure 5.9: Chip micrograph of uncompensated and compensated relaxation-oscillators.

<table>
<thead>
<tr>
<th>Area</th>
<th>Oscillator</th>
<th>Resistor</th>
<th>MIMcap</th>
<th>nCap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uncom.</td>
<td>75×145 µm²</td>
<td>20×90 µm²</td>
<td>25×55 µm²</td>
<td>-</td>
</tr>
<tr>
<td>Comp.</td>
<td>80×90 µm²</td>
<td>20×90 µm²</td>
<td>25×25 µm²</td>
<td>15×20 µm²</td>
</tr>
</tbody>
</table>

by 145 µm (10875 µm²). Note that, the only difference between the uncompensated and the compensated designs is in their capacitors. The uncompensated design has two large MIMcaps with the size of 25 µm by 55 µm each, while the compensated design has two smaller MIMcaps with the size of 25 µm by 25 µm each and two extra varactors (nCaps) of the size 15 µm by 20 µm which have been laid out underneath their corresponding MIMcaps. In the final layout, due to the size reduction of total
capacitors in the compensated version, by rearranging some sub-blocks and slightly extending the width of the overall design (from 75 to 80 µm), we managed to fit the layout of compensated design in a more compact space.

In this section, we present various performance measures of these oscillators. We compare the frequency stability of uncompensated and compensated oscillators over the temperature range of 25 to 200°C. Then we present the frequency stability of the compensated oscillator when the supply voltage varies between 2 to 3 V. Furthermore, simulation studies on the performance of the oscillator in the presence of process variations are presented.

5.3.1 Comparison of the Uncompensated and Compensated Oscillators over Temperature

6 different samples of the two prototype circuits, i.e., uncompensated and compensated 1 MHz oscillators are measured over the temperature range of 25 to 200°C. The measurement results are presented in Fig. 5.10. The error bars on this graph represent the maximum and minimum frequency of oscillation for the 6 samples. In these measurements, the worst-case standard deviation of measured frequencies at each temperature (over the 6 samples repeated three times for each sample) is approximately 1.514 kHz. The measurements are done at 11 different temperature values, namely, 25, 50, 75, 100, 125, 150, 160, 170, 180, 190, and 200°C. At each temperature value, the temperature has been kept constant for 8 hours. At each temperature and for the nominal supply voltage of 2.5 V, we have measured the average frequency of the output waveforms.

At room temperature, i.e., 25°C, the output frequency of both uncompensated and compensated oscillators is around 1.012 MHz. As temperature increases up to
200°C, however, the uncompensated oscillator shows a frequency variation of 9.92% (566 ppm/°C) while the compensated oscillator shows a variation of only 1.88% (108 ppm/°C). The frequency variation of the uncompensated oscillator over temperature is dominated by the bias resistor drift (from 25 to about 150°C) and the leakage current of the charging switches (from 150 to 200°C). In the compensated oscillator we used resistive compensation technique to compensate for the resistor drift as discussed in Fig. 5.6 and capacitive compensation technique to compensate for the leakage current as discussed Fig. 5.7. The combination of both resistive and capacitive compensation techniques can be seen in measured results shown in Fig. 5.10.
5.3.2 Frequency Stability over $V_{dd}$ Variations

Fig. 5.11 presents the measured output frequency of the compensated oscillator when nominal supply (2.5 V) varies by ±20%. Based on measured results, the oscillation frequency is stable over a range of 2 to 3 V and varies by ±1.09%. This frequency stability can be attributed to the robustness of the bias reference circuit shown in Fig. 5.3. This reference circuit is based on bootstrap bias technique and is robust to supply variation. The process corners simulations guarantee operation over this supply voltage range. The simulation results for process corners over the temperature range of −40 to 200 °C are presented in Fig. 5.12. Based on these simulations, the oscillator reliably operates down to −40 °C and lower, however, due to the lack of access to temperature chamber with proper cooling system we were not able to measure the performance below 25 °C.

![Figure 5.11: Measured compensated oscillation frequency versus ±20% supply variation.](image)

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Due to the process spread between the MIMcap and varactor (nCap) as well as other process variations; the value and temperature behaviour of bias resistor, reference voltage ($V_{REF}$, i.e., the varactor control voltage), varactor itself, and the leakage current of the switches may vary. These changes can affect the compensation technique and degrade its performance. The difference between measured results and simulations can be attributed to these spreads. To compensate for the changes, one can use a trimming technique. For example, one possibility is to include additional capacitors (with fixed and variable values) and control switches in parallel to the existing capacitors to change the ratio of the fixed capacitance to the variable capacitance.
5.3.3 Oscillator performance summary and comparison

There are a variety of figures of merit (FoMs) used in the literature in the context of oscillators, however, we were not able to find a commonly used FoM that includes temperature range and area. Therefore, we have included two FoMs: one is frequency to power ratio, $\text{FoM}_1 = 10 \log(f/P)$ that is commonly used in the context of low-power oscillators, e.g., in [69], and the other one is $\text{FoM}_2 = 10 \log \left( \frac{f \cdot \Delta T \cdot L_{\min}^2}{P \cdot TC \cdot A} \right)$ in which $\text{FoM}_1$ is modified to take into account the effects of the temperature range ($\Delta T$), temperature coefficient (TC), area (A), and feature size of the technology ($L_{\min}$).

<table>
<thead>
<tr>
<th>Reference</th>
<th>Tech. (nm)</th>
<th>Area (mm$^2$)</th>
<th>Scaled Area (mm$^2$)</th>
<th>Supply (V)</th>
<th>Power Consumption</th>
<th>Target Frequency</th>
<th>Temperature Range (°C)</th>
<th>TC (ppm/°C)</th>
<th>$\text{FoM}_1$ (dB)</th>
<th>$\text{FoM}_2$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uncom.</td>
<td>130</td>
<td>0.011</td>
<td>0.011</td>
<td>2.5</td>
<td>391 $\mu$W</td>
<td>1 MHz</td>
<td>25 to 200</td>
<td>566</td>
<td>94</td>
<td>152</td>
</tr>
<tr>
<td>Comp.</td>
<td>130</td>
<td>0.007</td>
<td>0.007</td>
<td>2.5</td>
<td>428 $\mu$W</td>
<td>1 MHz</td>
<td>25 to 200</td>
<td>108</td>
<td>93</td>
<td>160</td>
</tr>
<tr>
<td>[62]</td>
<td>90</td>
<td>0.013</td>
<td>0.026</td>
<td>1.0</td>
<td>87 $\mu$W</td>
<td>1.8 GHz</td>
<td>7 to 62</td>
<td>85</td>
<td>133</td>
<td>189</td>
</tr>
<tr>
<td>[76]</td>
<td>90</td>
<td>0.096</td>
<td>0.192</td>
<td>1.0</td>
<td>1.95 mW</td>
<td>2.1 GHz</td>
<td>7 to 62</td>
<td>168</td>
<td>120</td>
<td>164</td>
</tr>
<tr>
<td>[64]$^a$</td>
<td>180</td>
<td>0.04</td>
<td>0.02</td>
<td>1.8</td>
<td>43 $\mu$W</td>
<td>14 MHz</td>
<td>−40 to 125</td>
<td>91</td>
<td>115</td>
<td>177</td>
</tr>
<tr>
<td>[64]$^a$</td>
<td>180</td>
<td>0.04</td>
<td>0.02</td>
<td>1.8</td>
<td>43 $\mu$W</td>
<td>14 MHz</td>
<td>−40 to 125</td>
<td>23</td>
<td>115</td>
<td>183</td>
</tr>
<tr>
<td>[65]</td>
<td>65</td>
<td>0.03</td>
<td>0.12</td>
<td>1.2</td>
<td>66 $\mu$W</td>
<td>6 MHz</td>
<td>0 to 120</td>
<td>86</td>
<td>110</td>
<td>163</td>
</tr>
<tr>
<td>[66]</td>
<td>250</td>
<td>1.6</td>
<td>0.4</td>
<td>2.5</td>
<td>1.5 mW</td>
<td>7 MHz</td>
<td>−40 to 125</td>
<td>315</td>
<td>96</td>
<td>140</td>
</tr>
<tr>
<td>[67]</td>
<td>130</td>
<td>0.016</td>
<td>0.016</td>
<td>3.3</td>
<td>11.2 mW</td>
<td>1.25 GHz</td>
<td>−40 to 125</td>
<td>340</td>
<td>110</td>
<td>168</td>
</tr>
<tr>
<td>[68]</td>
<td>180</td>
<td>0.22</td>
<td>0.11</td>
<td>1.2</td>
<td>80 $\mu$W</td>
<td>10 MHz</td>
<td>−20 to 100</td>
<td>67</td>
<td>111</td>
<td>165</td>
</tr>
<tr>
<td>[69]</td>
<td>350</td>
<td>0.1</td>
<td>0.017</td>
<td>1.0</td>
<td>1.1 mW</td>
<td>3.3 kHz</td>
<td>−20 to 80</td>
<td>260</td>
<td>125</td>
<td>182</td>
</tr>
<tr>
<td>[70]$^b$</td>
<td>65</td>
<td>0.2</td>
<td>0.8</td>
<td>1.2</td>
<td>51 $\mu$W</td>
<td>150 kHz</td>
<td>−55 to 125</td>
<td>300</td>
<td>94</td>
<td>136</td>
</tr>
<tr>
<td>[70]$^c$</td>
<td>65</td>
<td>0.2</td>
<td>0.8</td>
<td>1.2</td>
<td>51 $\mu$W</td>
<td>150 kHz</td>
<td>−55 to 125</td>
<td>55</td>
<td>94</td>
<td>143</td>
</tr>
<tr>
<td>[79]</td>
<td>180</td>
<td>0.525</td>
<td>0.262</td>
<td>1.8</td>
<td>2 mW</td>
<td>625 MHz</td>
<td>0 to 80</td>
<td>550</td>
<td>115</td>
<td>154</td>
</tr>
<tr>
<td>[80]</td>
<td>350</td>
<td>0.162</td>
<td>0.027</td>
<td>3.0</td>
<td>−</td>
<td>1 MHz</td>
<td>0 to 100</td>
<td>333</td>
<td>−</td>
<td>−</td>
</tr>
</tbody>
</table>

$^a$With temperature compensation for $V_{ref}$, $^b$With 1-point trimming, $^c$With 2-point trimming

Table 5.1: Performance comparison

Table. 5.1 presents the performance summary table that includes the measured performance of the uncompensated and compensated oscillator as well as that of several recent works. In this table, the scaled area column gives the simplistic projection
of the oscillator area for each design, had it been implemented in the 0.13-μm CMOS technology. By simplistic, we mean that we simply scale the area according to the feature size ratio. This scaled area represents a relatively fair measure to compare the size of the designs. Note that while the temperature stability of the compensated oscillator compares favourably with state-of-the-art designs, it occupies 0.007 mm² which is 2.3× to 114× smaller than other designs. Also, the proposed circuit operates reliably up to 200°C (as compared to 125°C in other designs).

One of the main contributors to the chip area in such relaxation oscillator is the capacitor which does not scale with the technology feature size. We, however, introduced the simplistic scaled area for the purpose of area comparison among different technologies. Note that comparing either the area or the simplistically scaled area of the oscillators listed in Table. 5.1, the proposed compensated oscillator has the smallest reported area.

5.4 Chapter Summary

Simple resistive and capacitive temperature-compensation techniques for relaxation oscillators are presented. Proof-of-concept prototypes are implemented in a standard 0.13-μm CMOS process and measurement results of 6 sample chips confirm the validity of the proposed technique. Each sample is measured at 11 different temperature values within the range of 25 to 200°C and the measurement are repeated 3 times for each sample chip. Overall, each of the 6 sample chips has been tested for 264 hours, and each chip has been exposed to temperatures equal or greater than 150°C for 144 hours. Measured results of the output frequency show that over the temperature range of interest (25 to 200°C) the uncompensated oscillator achieves a temperature
coefficient of 566 ppm/°C, while the compensated version achieves more than 5 time better frequency stability with a temperature coefficient of 108 ppm/°C. For the supply voltage changes from 2 to 3 V, the frequency variation over the supply voltage is ±1.09 %/V. Although the measurements and duration of the tests performed in this work may not be quite sufficient for assessing the long-term endurance of the chip at high temperatures and more test and data would be useful, however, we believe the results are representative of an acceptable high-temperature performance for many high-temperature applications operating below 200°C. The entire oscillator along with output driver consumes 428 µW of power at supply voltage of 2.5 V while occupying 7200 µm² which is between 2.3× to 114× smaller than the state-of-the-art designs.
Chapter 6

Conclusion

6.1 Research Contributions

At high temperature, electronic circuits face several challenges including extra leakage current, decreased absolute value of CMOS threshold voltage, and decreased carrier mobility. In this work, design techniques for reliable high-temperature operation of analog and mixed-signal building blocks over a wide temperature are presented. The techniques are motivated by the design of a sensor interface that is required to operate over the temperature range of 25 to 200°C. Several proof-of-concept building blocks are implemented in a 0.13 µm CMOS technology.

In order to minimize the adverse effects of high temperature, we have proposed three new techniques and validated them by successful measurement of proof-of-concept designs. These techniques are as follows:

1) A modified constant-$g_m$ bias circuit is presented which has a temperature-stable behaviour over the temperature range of interest.

2) A resistor structure is proposed that has a desired TC and the structure does not require any extra processing step during the chip manufacturing. This technique considers and takes advantage of contact resistance of the core resistor to control the overall temperature behaviour of the proposed multi-finger resistor structure. The analysis of resistor TC sensitivity and its dependance to length, width, and number of fingers of the structure are also provided.
3) A simple capacitive compensation technique is also presented that uses a varactor which is controlled by the variation of a bias voltage which typically already exists in the circuit.

Furthermore, we have implemented several different size NMOS / PMOS transistors and measured their dc behaviour over the temperature range of interest to find the proper sizing of such transistors. The choice of sizing is validated using measured results of several building blocks.

To show the performance of the above-mentioned techniques, several proof-of-concept building blocks are designed and successfully tested. These include:

A high temperature constant-$g_m$ bias circuit along with fully differential folded-cascode amplifier with a dc gain of 69 dB that consumes at most 620 $\mu W$ from a 2.5 V supply over the temperature range of interest.

Then, the amplifier and bias circuit are used to implement a non-trimming 1.22V bandgap voltage reference for high temperature applications. The bandgap has a temperature coefficient of 171 ppm/$^\circ$C over the temperature range of 25 to 200$^\circ$C, and a line regulation of 1.6%/V. It operates from a supply voltage in the range of 2 to 3 V with the maximum power consumption of 892$\mu W$.

Also, a high-temperature 1.02 MHz oscillator with the proposed capacitive temperature compensation technique is presented. It achieves a temperature coefficient of 108 ppm/$^\circ$C over the temperature range of 25 to 200$^\circ$C. The frequency variation is $\pm$ 1.09 %/V when the supply voltage changes from 2 to 3 V. The entire oscillator along with output driver consumes 428 $\mu W$ from a supply voltage of 2.5 V.

Although the proposed techniques are only validated in a 0.13 $\mu m$ CMOS technology, they are general and our preliminary studies on other technologies indicate that the techniques can be ported to other CMOS technologies.
6.2 Future Work

Based on our study on the sensitivity analysis of the proposed monolithic resistor structures, one can further improve the performance of these resistors. For example, the temperature stability can be improved by using resistors with a lower tolerance. Also, for a given resistor tolerance, increasing the length of the resistor can effectively improve the temperature stability. It would be nice if these observations can be confirmed with an extensive experimental results over a large number of sample resistors and in different technologies.

Using the proposed resistors in different building blocks including constant-$g_m$ bias circuits, bandgap voltage references, amplifiers and oscillators and confirm the performance improvement would be another area for future work. Furthermore, the resistors can be used in more complex blocks and/or systems such as filters, I/O blocks, and clock and data recovery circuits.

In relation to the voltage reference, one can further improve the output line regulation at low frequency by minimizing the impact of amplifier input offset. This can be done by either using a low-input-offset amplifier or by increasing $\Delta V_{BE}$ by using stacked transistors.

In connection with the proposed temperature-compensated relaxation oscillator, through simulations we have shown that by using the proposed resistor structure, temperature stability of the oscillator would significantly improve. One should confirm this with experimental measurement and ideally in several processes.
Bibliography


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tor with a temperature compensated feedback loop in 0.18 μm cmos,” in VLSI Circuits, 2009 Symposium on, june 2009, pp. 226 –227.


