A New Radio Frequency Switch-mode Power Amplifier Concept for Wireless Applications

by

Sheikh Nijam Ali

B.Sc., Bangladesh University of Engineering and Technology (BUET), 2009

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF
THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF APPLIED SCIENCE

in

The College of Graduate Studies

(Electrical Engineering)

THE UNIVERSITY OF BRITISH COLUMBIA

(Okanagan)

August 2012

Abstract

Although RF switch-mode power amplifiers (SMPAs) are theoretically attractive with the potential to achieve very high power efficiencies, experimental realizations at high frequencies have yet to yield significantly better efficiency than conventional analog technology. Most SMPA designs are based on class D or class S circuits, and in these circuits, power efficiency is significantly reduced when the switching signal is changed from periodic to non-periodic. In this work, a new SMPA architecture is proposed. Instead of employing reflective out-of-band matching conditions used in class D/S circuits, the switch is matched to a broadband load which creates dissipative out-of-band impedances. The broadband load significantly improves switching conditions especially for non-periodic signals. The broadband load is implemented as a complementary diplexer which separates in-band and out-of-band signal power at the output of the SMPA. An energy recovery loop using out-of-band signal power is proposed to significantly reduce the sensitivity of the overall power efficiency to changes in the peak to average power ratio of the source signal. Experimental and simulation results are shown for the new SMPA architecture.

Table of Contents

List of Tables

List of Figures

List of Acronyms

AC	Alternating Current
ADS	Advanced Design System
BERT	Bit Error Rate Test
CMCD	Current-mode Class D
CW	Continuous Wave
DC	Direct Current
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
HS	Hard Switched
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
MTT-S	Microwave Theory and Techniques Society
PAPR	Peak to Average Power Ratio
PPM	Pulse Position Modulation
PRBS	Pseudo Random Bit Sequence
PSD	Power Spectral Density
RF	Radio Frequency
RMS	Root Mean Square
SDM	Sigma Delta Modulation
SMPA	Switch-mode Power Amplifier
TEM	Transverse Electromagnetic
VMCD	Voltage-mode Class D

Acknowledgements

This thesis would not have been possible without the help and support of my colleagues, friends, and family.

I am heartily thankful to my supervisor, Dr. Thomas Johnson, for both inspiring and teaching me. He has provided constant encouragement, guidance and support throughout my thesis. He has introduced me to the art of scientific research, the beauty of good experimental design, the value of explaining numerical results not only as mathematical constructs, but also through physical interpretation, the subtlety of clear and accessible scientific writing, the rigors of analytical ability and adherence, and the spirit of intellectual integrity.

I am indebted to many of my colleagues for their support throughout the work and writing.

I would like to also thank NSERC for funding this research project, Agilent for providing simulation tools and Cree Inc. for providing a large signal model for the GaN device used in this work.

To my family, who, of all that walk on the earth, are most precious to me,
for their support in every endeavor.

Chapter 1

Introduction

Research in switch-mode power amplifiers (SMPAs) for wireless applications has been active for the last decade. Despite advances in the implementation of radio frequency (RF) switch-mode power amplifiers, realizing high efficiency circuits has been challenging. At the same time, advances in analog based RF power amplifiers has also continued and drain efficiencies in excess of 50% have been reported for modulated signals. If RF switch-mode technology is to provide a compelling alternative to analog techniques, it clearly must have advantages including competitive power efficiency.

Most RF SMPAs have been based on class D circuit topologies. Variations include current mode class D (CMCD) [1], voltage mode class D (VMCD) [2], and class S [3–5] circuit topologies. Class S is similar to class D except diodes are added to protect the switches under non-periodic switching conditions. Performance limitations in these circuits include power loss mechanisms from parasitic capacitance and inductance, power loss in diodes, low power efficiency under back-off conditions, voltage peaking across the switching device including third quadrant device operation, and power loss related to shoot through current. Although further research will undoubtedly continue to bring improvements to RF SMPA's based on class D circuits, it is interesting to consider whether there are other approaches that could be taken to implement switch-mode designs that may lead to more power

efficient designs.

The RF SMPA architecture presented in this work evolved from a reflection on the challenges in realizing RF class D amplifiers that can efficiently amplify non-periodic pulse trains. In theory, the operation of a current mode class D amplifier requires a load network that is a short for all out-of-band frequency components and is matched for in-band frequency components. A VMCD amplifier is the dual of CMCD and requires an open for all out-of-band frequencies. When class D is driven with non-periodic pulse trains such as a bandpass sigma-delta modulated signal, the source signal is encoded in a noise well and quantization noise rises sharply outside the noise well. A significant challenge in class D is to present a narrow-band match at the device plane which shorts the spectrum adjacent to the noise well while simultaneously matching the in-band spectrum. Improper out-of-band termination impedances create dissipation of out-of-band spectra and consequently power efficiency is reduced. The problem becomes particularly acute when the encoded signal has low coding efficiency and most of the spectrum is out-of-band.

Starting with an exclusive focus on creating impedance conditions that minimize power loss in the switch, a purely resistive load that is broadband is beneficial. Under these conditions, the switch is either on, off, or transitions between states. On and off state losses are similar to class D, however, the relationship between device current and device voltage during transitions is now consistent and predictable for any pulse waveform. In other words, current and voltage are orthogonal for *any* pulse train and transition losses are predictable. The key point is that the phase of the current and voltage is controlled unlike a class D amplifier which has uncontrolled phase relationships when switched with non-periodic signals.

Although low device dissipation in the switch is obtained with a broadband match, the obvious disadvantage is that out-of-band power is now delivered to the load. The question then is: can we mitigate the loss of power efficiency created by power in the out-of-band spectrum? It is this question along with the goal of improving the power efficiency of RF SMPAs that motivates this research.

In the following sections of this chapter, background on switch-mode power amplifiers along with a literature review are given. The research objectives are then presented and the chapter concludes with a summary of contributions.

1.1 Background on RF Switch-mode Power Amplifiers

A high level block diagram of the RF switch-mode power amplifier architecture is shown in Figure 1.1. An analog input signal called the source signal is encoded and converted into a two level binary digital signal. The source signal can be a periodic (CW) signal or a non-periodic (modulated) signal. Depending on the type of encoder used, the output pulse train is also periodic for unmodulated carrier signals and non-periodic for modulated signals. However, regardless of the source signal type, all the information is encoded by the timing of level transitions in the binary amplitude pulse train. A periodic signal has a pulse sequence that repeats while a non-periodic sequence has pulse widths that continuously change depending on the amplitude and phase of the source signal. If the analog input signal is a periodic signal, then after encoding, the signal will be a pure square wave signal which means it is also a periodic signal. On the other hand,

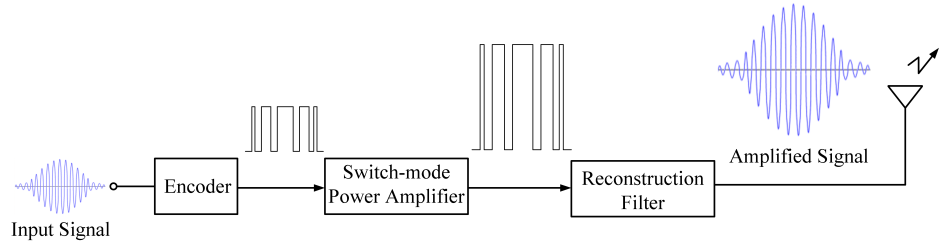

Figure 1.1: Basic block diagram of a RF switch-mode power amplifier system (only non-periodic signals are shown).

if the analog input signal is a non-periodic signal (modulated), then after encoding it will be a square wave signal with different pulse widths which means it is a non-periodic signal. After encoding, a switch-mode power amplifier amplifies the encoded signal. Finally, a reconstruction filter extracts the original analog signal from the amplified version so that it can be transmitted through the antenna.

Therefore a RF switch-mode power amplifier is a type of electronic amplifier used to convert a low-power RF signal into a larger signal of significant power, typically for driving the antenna of a transmitter. Design objectives for a power amplifier include:

- high efficiency (low device dissipation);
- high output power;
- good return loss at the input and output;
- high gain.

In a switch-mode power amplifier the power device is designed to operated as a binary switch defined by an on state and an off state. It is either fully on or fully off. Ideally zero time is spent transitioning between two

states. Figure 1.2 shows the ideal switching waveforms across the device. The current and voltage waveforms are orthogonal which means that no power is dissipated in the device and the amplifier is ideally 100% efficient.

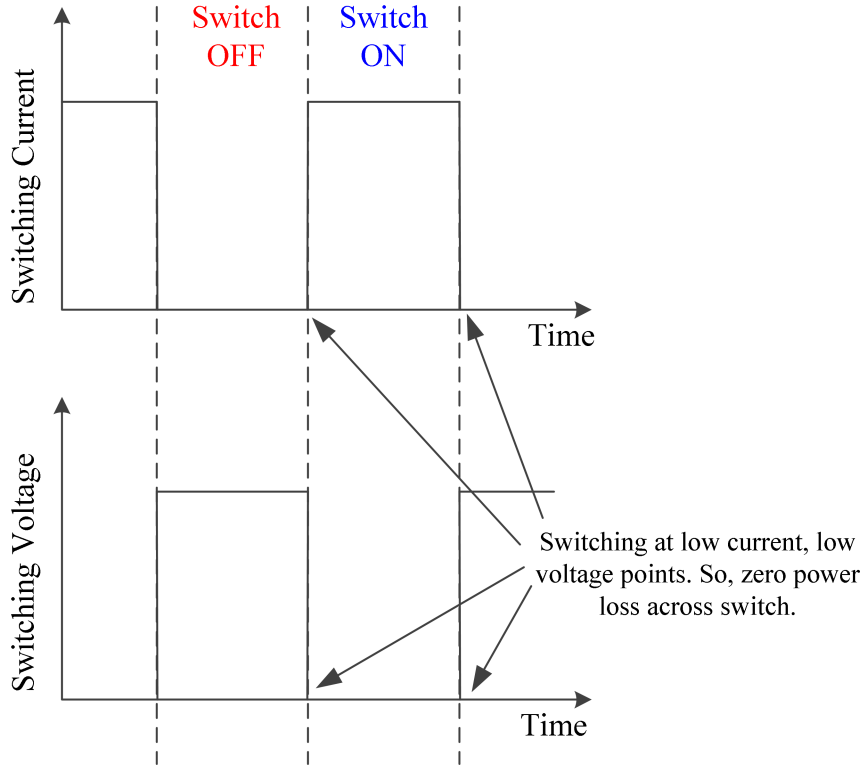

Figure 1.2: Switching characteristics of the RF switch-mode power amplifier.

1.1.1 Class D Switch-mode Power Amplifier

A class D power amplifier employs a pair of active devices operating in a push-pull mode with a tuned output circuit. The active devices are driven to act as a two-pole switch that creates a rectangular voltage waveform called voltage switching or a rectangular current waveform called current switching. The output circuit is tuned to the switching frequency and harmonic

components are attenuated resulting in a purely sinusoidal signal delivered to the load. In theory, a class D amplifier should not dissipate any power in the harmonic components and the amplifier should have very high efficiency. Let us now consider the basic principles, circuit schematics, and voltage-current waveforms corresponding to the different types of class D power amplifiers.

Voltage Mode Class D power amplifier (VMCD)

Figure 1.3 shows the simplified circuit diagram of a voltage mode class D (VMCD) power amplifier. Two transistors (Q_1 and Q_2) are driven 180 degrees out-of-phase. A series LC filter, consisting of components L_0 and C_0, is employed with a resonant frequency set to the center frequency of the signal. Providing the filter has sufficient selectivity, the VMCD amplifier is matched for in-band frequencies and open for all out-of-band frequencies. Ideal drain voltage and drain current waveforms are shown in Figure 1.4. The voltage across the transistors is a square wave (switched) while the current is a half-wave rectified sine wave. The push pull action of Q_1 and Q_2 will combine to create a load current that is a full-wave sine wave. The conditions shown in this figure correspond to a periodic switching signal with a 50% duty cycle. Implementation challenges in practical class D circuits at high frequencies include the design of a high side driver for Q_1 and high Q output filters to provide an effective open at harmonic or out-of-band frequencies.

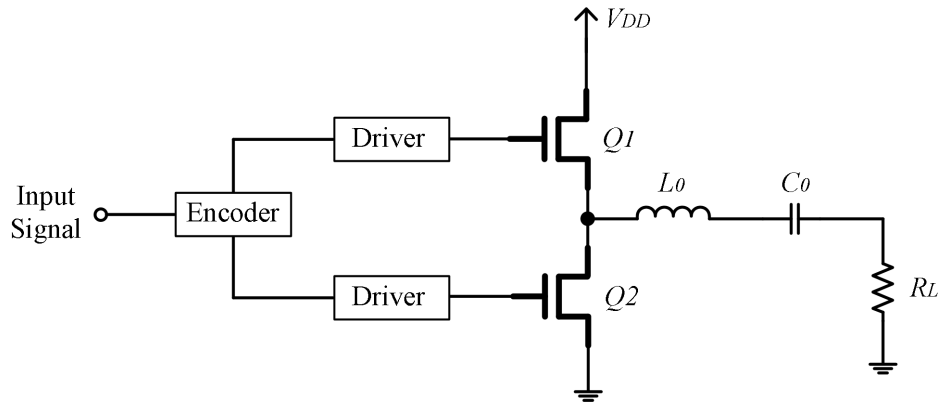

Figure 1.3: Circuit diagram of a voltage mode class D (VMCD) power amplifier.

Current Mode Class D power amplifier (CMCD)

Figure 1.5 shows the simplified circuit diagram of a current mode class D (CMCD) power amplifier. In this case, drain bias is provided by current sources instead of voltage sources which are used in VMCD, and the two switching transistors (Q_1 and Q_2) control the current instead of the voltage. There is a parallel-connected filter with a resonant frequency set to the center frequency. Therefore, the operation of the CMCD amplifier requires a load network that is a short for all out-of-band frequency components and is matched for in-band frequency components. Figure 1.6 shows the ideal current and voltage waveforms of the transistors. There is no voltage across the transistors at each switching time. Hence, ideally, the efficiency is 100%.

Periodic vs Non-periodic Switching Condition in Class D

Under periodic switching conditions with a 50% duty cycle, the switch-mode class D (CMCD or VMCD) circuit design is configured to generate

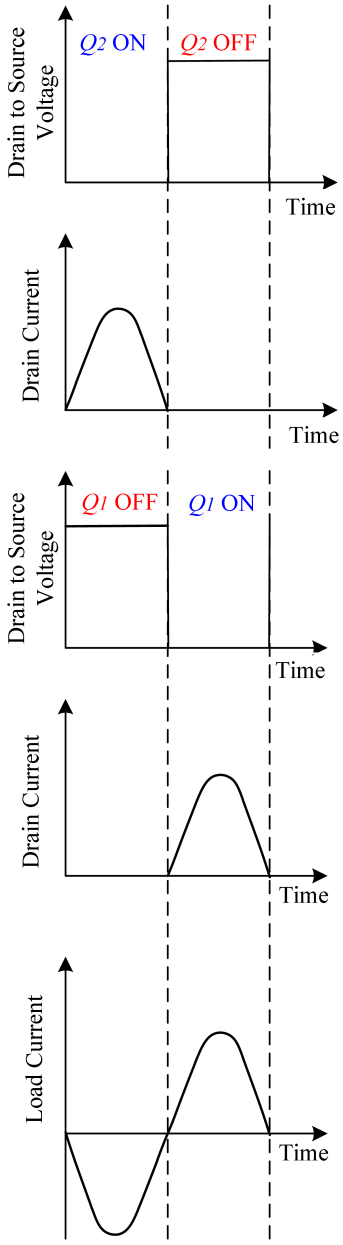

Figure 1.4: Voltage and current waveforms of a voltage mode class D (VMCD) power amplifier.

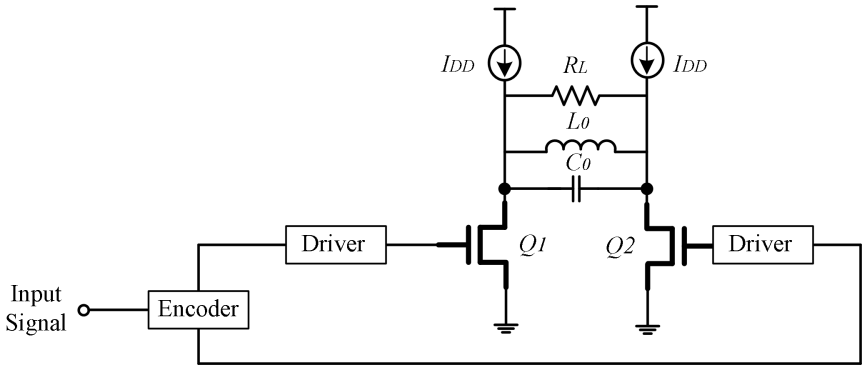

Figure 1.5: Circuit diagram of a current mode class D (CMCD) power amplifier.

zero voltage or zero current switching, a condition that minimizes switching losses. On the other hand, non-periodic switching conditions destroy the zero voltage or current switching conditions. For non-periodic switching, the relationship between the voltage across the switching device and the current through the device is arbitrary. These arbitrary switching conditions lead to significantly higher switching losses. In addition, for non-periodic pulse trains, the source signal is encoded in a noise well and the quantization noise rises sharply outside the noise well. An example of an encoded pulse train signal is shown in Figure 1.7.

It is very challenging to construct a narrow-band match at the device plane which shorts the spectrum adjacent to the noise well while simultaneously matching the in-band spectrum. Improper out-of-band termination impedances create dissipation of out-of-band spectra which can reduce power efficiency significantly. This out-of-band mismatch problem becomes severe when the encoded signal has low coding efficiency. Wireless communication source signals have large amplitude variation which means that the average power in the encoded spectrum is much lower than peak power. As signal

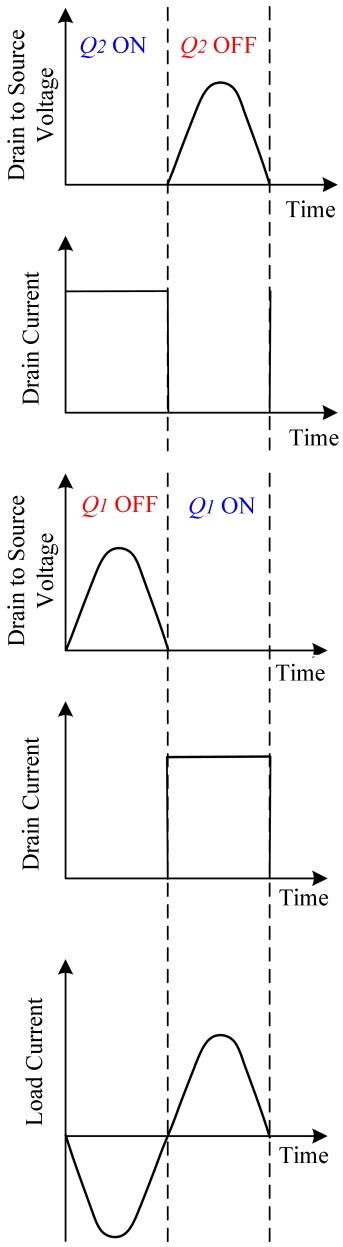

Figure 1.6: Voltage and current waveforms of a current mode class D (CMCD) power amplifier.

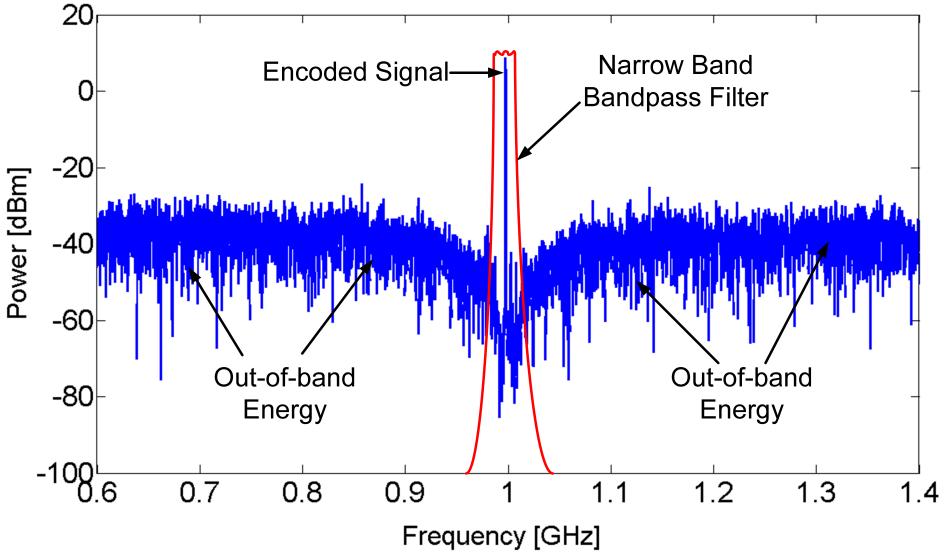

Figure 1.7: Power spectral density of a 1 GHz pulse encoded signal. An overlay of a narrow-band bandpass reconstruction filter is also shown.

power is backed-off relative to peak power, coding efficiency is low and consequently power efficiency can degrade significantly. The reduction in power efficiency under non-periodic switching conditions is a major limitation of class D power amplifiers especially in very high frequency applications.

1.1.2 Class S Switch-mode Power Amplifier

Class S is similar to class D except diodes are added to protect the switches under non-periodic switching conditions. Figure 1.8 shows a voltage mode class S power amplifier. Two diodes (D_1 and D_2) are added across the two transistors (Q_1 and Q_2) to protect the switches from voltage peaking and third quadrant transistor operation. However, diode losses can reduce the overall power efficiency significantly. The working principles of the current mode (CM) and voltage mode (VM) class S are similar to CMCD and VMCD

respectively.

Therefore, in a summary, the limitations of the class D and class S switch-mode power amplifiers are:

- simultaneous in-band and out-of-band match is required;
- low power efficiency under wide back-off conditions;
- voltage peaking across the switching device including third quadrant device operation;
- power loss in protection diodes;
- power loss related to shoot through current;
- implementation challenges with output baluns and high swing drivers;
- two devices are required.

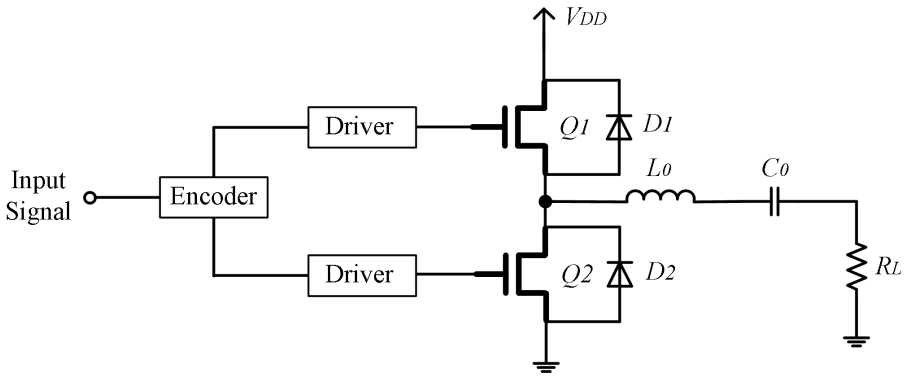

Figure 1.8: Circuit diagram of a voltage mode class S power amplifier.

Table 1.1: Some recent experimental results for periodic switching (CW)

Frequency	Drain Efficiency	Power	Topology	Year	Author
420 MHz	59%	19 W	CM class S	2010	[3]
400 MHz	64%	7 W	VM class S	2011	[4]
800 MHz	74%	62 W	Class E	2010	[7]
550-1100 MHz	74%	10.5 W	Class F	2010	[8]
3.27 GHz	71%	5 W	Inverse class F	2009	[9]
1 GHz	83%	10 W	Inverse class F	2009	[10]
2.3-2.7 GHz	60-68%	10 W	Class J	2011	[11]
850 MHz	73%	81 W	HS class AB	2011	[6]

1.2 Literature Review

Table 1.1 shows some recent experimental results based on periodic switching. The peak drain efficiencies range from 60% to 80%. The circuits span a wide range of frequencies from 400 MHz to 2.7 GHz over a wide range of output power from 5 W to 81 W. Different topologies are used and drain efficiency is quite high because the reported results correspond to 50% duty cycle periodic switching.

For wireless applications, we have to consider a modulated source signal, which after encoding, creates non-periodic pulse trains. The results for encoded pulse trains (non-periodic switching) are tabulated in Table 1.2. Many of the recent results are from Wentzel et al. [3–5] where the drain efficiency is around 40% for a frequency 450 MHz. In this work, a class S topology is used with a fourth order bandpass sigma-delta modulator for the source encoder. Other work by Johnson et al. [6] uses a hard switched (HS) class AB amplifier with a fourth order noise shaped asynchronous encoder. A power efficiency of 30% is reported at a power of 20 W for a modulated IS-95A CDMA source signal.

From these two tables, it is very apparent that if a non-periodic pulse

Table 1.2: Some recent experimental results for non-periodic switching with pulse encoded signals.

Frequency	Drain Efficiency	Power	Topology	Year	Author
420 MHz	34%	8.7 W	CM class S	2010	[3]
400 MHz	38%	3.4 W	VM class S	2011	[4]
850 MHz	30%	20.4 W	HS class AB	2011	[6]
450 MHz	60%	1 W	VM class S	2011	[5]
450 MHz	25%	6 dB Back off.	VM class S	2011	[5]

signal is used to drive a switch-mode power amplifier, drain efficiency drops significantly. In other words, although SMPAs have theoretically very high power efficiency, experimental prototypes demonstrating high efficiency have not yet been realized at high frequencies. Another important observation for the results shown in Table 1.2 is the reduction in power as output power is reduced (backed-off) from peak power. Results from Wentzel et al. [5] show 60% peak drain efficiency at 450 MHz, while under 6 dB back-off the drain efficiency drops to 25%. Since many common wireless communication signals have peak to average ratios of 6 to 10 dB, this means the average efficiency for modulated signals will be low. Therefore, research into improving the power efficiency under back-off conditions is required to enable commercial deployment of SMPA technology for wireless applications.

1.3 Motivation and Research Objectives

Class D and Class S circuit topologies have not yielded competitive power efficiency relative to analog power amplifier designs and research is still required to realize a practical high efficiency SMPA for wireless applications. In this research, a new RF SMPA architecture is presented which is motivated by the following objectives:

- to improve the power efficiency of RF switch-mode design under non-periodic switching conditions;
- to obtain high power efficiency over a wide back-off range (e.g. 10 dB back-off), because existing switch-mode RF power amplifier designs have low power efficiency under back-off conditions;
- to address implementation challenges with RF switch-mode circuits employing class D or class S circuit topologies; these topologies may require high side switch drivers, protection diodes, and baluns.

1.4 Contributions

The SMPA concept in this work focuses on implementing a broadband output match across a single switch. A diagram of the overall proposed SMPA amplifier is shown in Figure 1.9. A modulated source signal $s(t)$ is first encoded into a pulse train $p(t)$ that has two amplitude levels which control the state of the power switch Q_1. The pulse train is amplified by a wide-band driver circuit with a low output impedance to drive the gate of Q_1. Since the gate is primarily capacitive, the driver sources or sinks charge to switch the device. The output network at the drain node consists of a broadband DC bias feed and a broadband output network. Because the load is broadband, the switch voltage and current waveforms are orthogonal and device dissipation is low. The load consists of a complementary diplexer which has a bandpass filter branch for reconstructing the source signal across the output load and a bandstop branch for capturing out-of-band energy. Unlike reflective filters or split band diplexers, the common input port of a complementary diplexer is matched at all frequencies including the transition

bands. The impedance presented by the diplexer input port at node C in Figure 1.9 is approximately equivalent to a broadband 50 Ω load.

The design of the encoder has important implications on the overall power efficiency of the SMPA. Since the power switch can only replicate two amplitude states, a source signal with amplitude variation must be encoded into a binary amplitude pulse train, amplified, and then recovered at the output after the reconstruction filter. Therefore, the encoder can also be thought of as a way to linearize the hard switched amplifier; it provides a means of reducing the distortion which would otherwise be very severe if the source were to directly drive the gate of the switch. The cost of linearizing the amplifier with a pulse encoder is an expansion in the bandwidth of the source signal. When the source envelope is quantized to two levels, bandwidth expansion is very large.

A figure of merit which is useful for characterizing encoder designs for SMPA applications is to measure the ratio of the in-band signal power to the total power in the pulse train $p(t)$. This measure is called coding efficiency. The coding efficiency of an encoder for a modulated source signal depends on the peak coding efficiency and the peak to average power ratio (PAPR) of the signal. For a source signal with a PAPR of 6 dB, the typical coding efficiency of a bandpass sigma-delta modulator is about 15% which means that 85% of the power is out-of-band. Class D and S amplifier designs ideally do not generate any power in the out of band signal but in practice this is very difficult to achieve.

Since out-of-band power is always generated by source encoders, a design is proposed that will recycle out-of-band power from the output of the bandstop diplexer port. If the energy recycling was 100% efficient, this would lead to a SMPA design that would have constant power efficiency

independent of the source PAPR. Obviously, 100% conversion efficiency will not be achieved in practice and an analysis of power efficiency assuming 75% conversion efficiency is shown in chapter 6. Even modest conversion efficiency can dramatically improve power efficiency for high PAPR sources, something that is difficult to achieve in class D or class S circuits.

1.5 Thesis Outline

Chapter 2: Power Amplifier Design

In Chapter 2, three different switch-mode power amplifier circuit designs are presented. The main goal of this chapter is to describe the design and implementation of these circuits.

Chapter 3: Complementary Diplexer

In Chapter 3, the theory and implementation of a complementary diplexer is presented. The complementary diplexer is a key component in the proposed SMPA architecture.

Chapter 4: Results

In Chapter 4, simulation and experimental results for the three different SMPA circuit designs are described. The chapter concludes with a comparison of measured results for the different circuits.

Chapter 5: Pulse Encoded Responses

In Chapter 5, simulated results are presented for the amplification of encoded pulse trains using sigma-delta and pulse-position modulated signals. Encoded pulse trains are generated in Matlab and used to predict the power efficiency of the RF SMPA using circuit simulation models.

Chapter 6: Energy Recovery

In Chapter 6, background and possibilities to rectify out-of-band energy are presented. Simulation results for the RF SMPA are shown assuming a RF to DC conversion efficiency of 75% could be obtained from these circuits.

Chapter 7: Conclusion

A summary of the main conclusions is presented as well as recommendations for future research works.

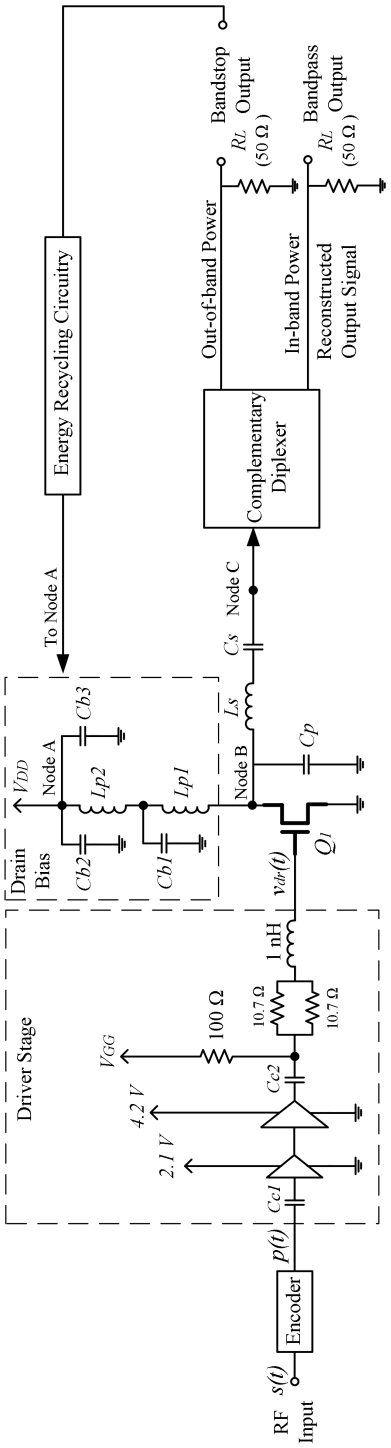

Figure 1.9: Circuit diagram of the proposed RF switch-mode power amplifier.

Chapter 2

Switch-mode Power Amplifier Design

In this chapter three switch-mode power amplifier (SMPA) designs are presented. The designs are called Design 1, Design 2, and Design 3, and become progressively more complicated. A 10 W GaN power device is used as the power switch. The purpose of stepping through each design is to evaluate design trade-offs.

In Design 1, the switching device is directly coupled to a 50 Ω load without any matching circuit. In other words, the load line for the switching device is 50 Ω. The motivation for Design 1 is to avoid introducing any bandwidth limitations in the output matching network, and in this case, a 50 Ω transmission line is all that is used. The output network also includes a DC bias network for supplying power to the drain of the switching device. Therefore, the bandwidth of the output network is primarily limited by the drain bias network. A two stage bias network is used to obtain a broadband output.

In Design 2, the output device capacitance is included in the design of the output network. The DC drain bias inductor is tuned to resonate with the output device capacitance to form a low Q output. As in Design 1, the device is also presented with a 50 Ω load line to avoid introducing any

further bandwidth restrictions created by matching networks.

In Design 3, an output matching network is added to Design 2 to transform the 50 Ω load to an optimum load impedance of 33.3 Ω for the switching device. A multistage matching network is used to implement broadband impedance transformations.

Simulated and experimental results for the different designs are presented in later chapters and the purpose of this chapter is to present the design methodology used for implementing the output stage of the SMPA.

2.1 Design 1: Broadband RF SMPA with a 50 Ω Load

2.1.1 Design Considerations

Figure 2.1 shows the circuit diagram of a broadband RF switch-mode power amplifier (SMPA) with a 50 Ω load. The design is called Design 1, a term which is used throughout this work. The term "broadband load" means that the output network including the drain biasing network (L_p) is broadband for a certain range of frequencies. In this work, circuits have bandwidths that range from two to five harmonics. In Design 1, the output device capacitance C_p is neglected and later, in Design 2 and Design 3, the capacitance is integrated into the output network design.

In Design 1, the load is a 50 Ω impedance which is directly coupled to the switching device through a DC blocking capacitor C_s and a series inductance L_s. The series inductor is used to adjust the relative phase of the current and voltage waveforms across the switching device at node B. The drain bias V_{DD} is provided through a drain bias circuit. Theoretically, the bias network

can be modeled by a large inductor L_p with a bypass capacitor C_b as shown in Figure 2.1. However, in practice it is difficult to realize a broadband bias network with a single inductor because parasitic capacitance in the inductor will lead to resonances which limits bandwidth. Therefore, a multistage bias network is needed in the design and will be described later.

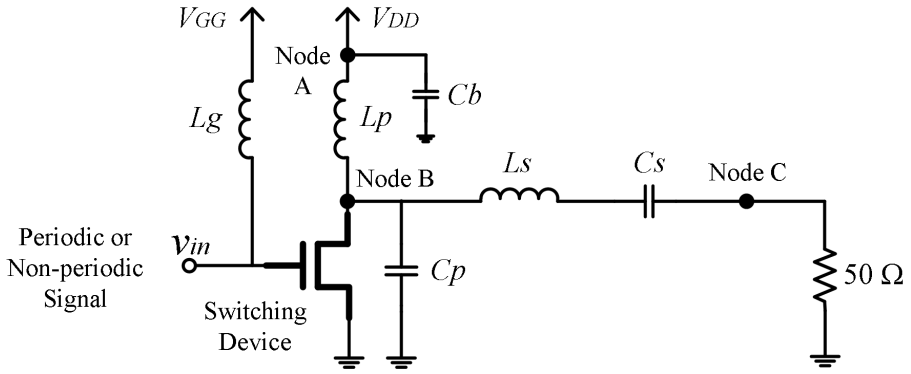

Figure 2.1: Circuit diagram of the broadband RF switch-mode power amplifier with a 50 Ω load (Design 1).

2.1.2 The RF Switch

For this work, a 10 W GaN (CGH40010) high electron mobility transistor (HEMT) from Cree Inc. is used as the switching device. The CGH40010 is a wideband unmatched power device. Cree also provides a large signal non-linear device model that is used for circuit modeling. As mentioned earlier, the effect of the output capacitance, C_p, is neglected in Design 1 and a discussion about the characteristics of C_p is deferred to section 2.2.2.

Figure 2.2 shows the drain-source characteristics of the CGH40010 for different values of gate-source voltage. The GaN device is a depletion mode device and consequently the device is on when $V_{gs} = 0$ and the device is off at the pinch-off voltage, approximately -3.3 V. From the data sheet of

the Cree device, the maximum breakdown voltage of this device is 84 V and the maximum drain current is approximately 2.9 A at a gate-source voltage of 1 V. The knee voltage, V_k, is approximately 5 V. The nominal operating gate voltage ranges from -5 V to +1 V and the maximum operating junction temperature is 225 °C.

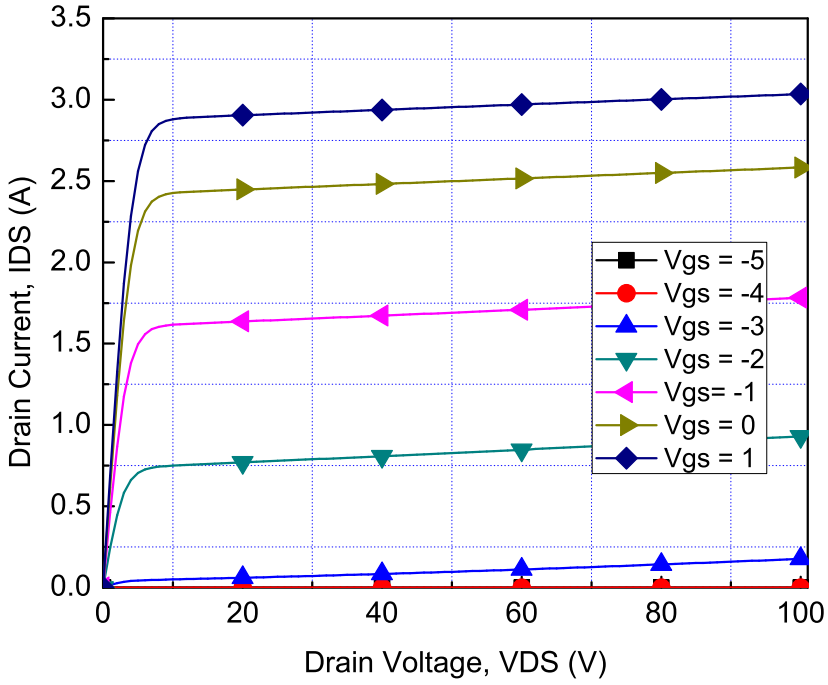

Figure 2.2: Drain-source characteristics of the 10 W GaN HEMT Cree device.

2.1.3 Output Network Design

Figure 2.3 shows the equivalent output network of Design 1. Two port symbols are added to the output circuit which relate to physical coaxial connectors used to measure the frequency response of the network. The ports are connected to 50 Ω terminations and used for measuring the S-

parameters of the network.

Since the objective is to have a broadband output network from node B to node C in Figure 2.3, a broadband drain bias network is required. It is difficult to obtain a large bandwidth bias network using a single inductor. Therefore a two stage network is used to improve the realization of a high bandwidth bias network. The biasing network consists of two LC filter stages. Each stage acts as a lowpass filter. The first stage consists of L_{p1} and C_{b1} and has a higher cut-off frequency relative to the second stage consisting of L_{p2} and C_{b2}. C_{b1} and C_{b2} are ceramic bypass capacitors, while C_{b3} is a large tantalum capacitor from AVX which is used to improve the low frequency bypass response of the second filter stage. L_{p1} and L_{p2} are chip inductors from Coilcraft.

The series inductor L_s is implemented with a transmission line on the circuit board and the value is selected to adjust the relative phase of the current and voltage across the switching device to minimize device dissipation. C_s is the DC blocking capacitance which is also from AVX.

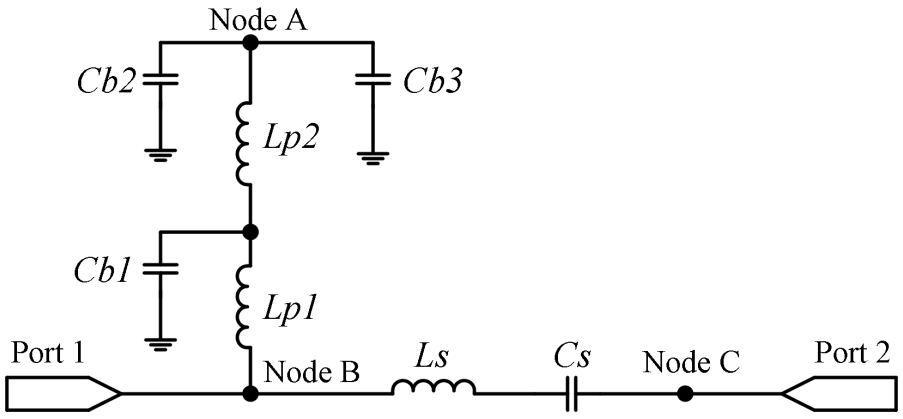

Figure 2.3: Equivalent output network for frequency response measurements of Design 1.

Table 2.1: Experimental circuit component values of output matching network for Design 1.

Components	Values
L_{p1}	33 nH
L_{p2}	82 nH
C_{b1}	100 pF
C_{b2}	100 pF
C_{b3}	0.33 μH
L_s	2.5 nH
C_s	33 pF

Once the circuit topology was defined, initial component values were calculated and a circuit simulation was done to verify and optimize the design. All circuit simulations use Agilent Technologies Advanced Design System (ADS) circuit simulation tools. Models for passive and active components were obtained from vendors, and distributed matching structures use models in ADS. Final component values which are used in Design 1 are given in Table 2.1. Simulation results for the output network are discussed next.

Figure 2.4 shows the S-parameter, $|S22|$, at port 2 in terms of return loss in dB.[1] The dotted line is the simulation result and the solid line is the measured result. The frequency span shown corresponds to the frequency range of the network analyzer available for measurements; in this case, measurements can be made from 100 kHz to 1.5 GHz. In this figure, the experimental trace follows the pattern of the simulated trace and both are close to each other.

A -15 dB reference line in Figure 2.4 is used to evaluate the output match. Return loss is approximately -26 dB from 0.2 GHz to 0.4 GHz and then it

[1]Note that return loss is usually defined as a positive term. The definition of return loss is $RL = -20\ log|S22|$. Here, data are shown from the network analyzer where S22 is measured.

starts to increase slowly as the frequency increases. Another noticeable characteristic is that there is a sudden dip and rise at low frequencies. The low frequency characteristics are dominated by the large tantulum bypass capacitor and the low impedance of the bias inductors. Therefore, the lowest frequency range that can be efficiently amplified is expected to be about 200 MHz.

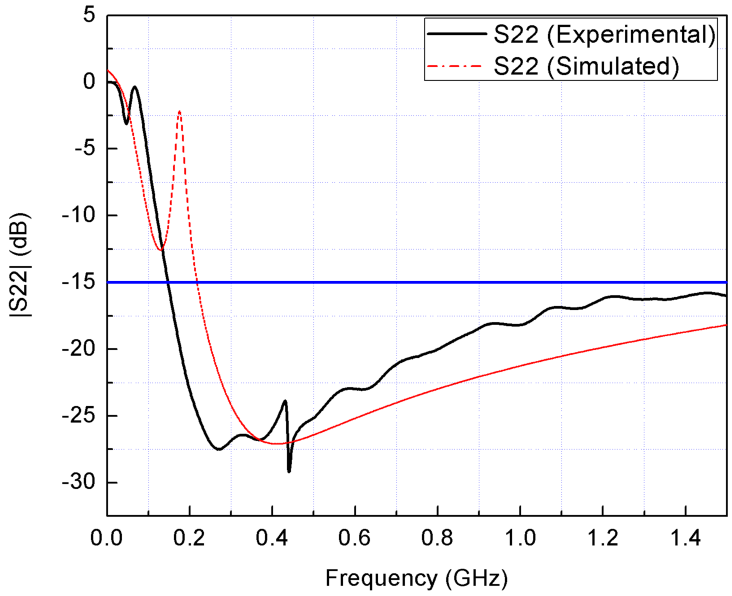

Figure 2.4: Output reflection coefficient $|S22|$ at port 2 of Figure 2.3.

The insertion loss of the output network is shown in Figure 2.5. Both simulation and experimental results show that insertion loss is very low (0.2 dB) from 0.2 GHz to 1.5 GHz. As mentioned, the network analyzer is limited to an upper frequency of 1.5 GHz and simulation results are shown in Figure 2.6 for an extended frequency range up to 10 GHz. The output network has sufficient bandwidth for five harmonics assuming a fundamental frequency of 1 GHz.

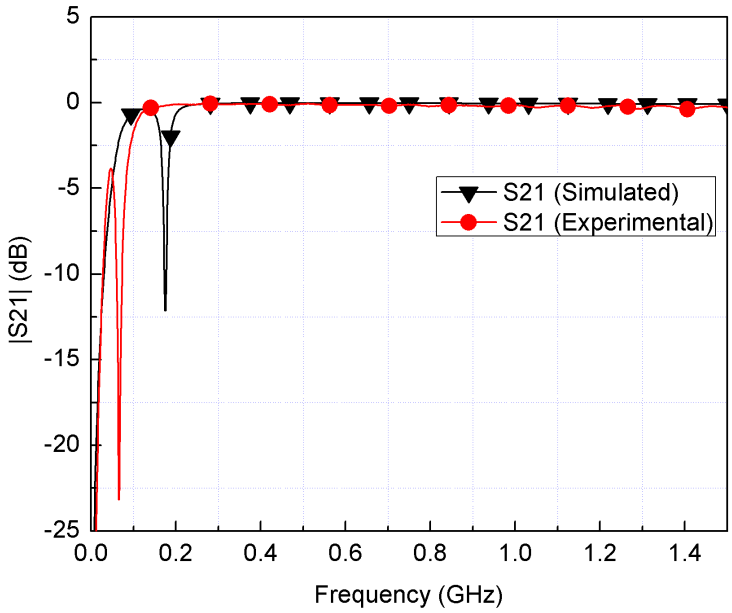

Figure 2.5: Simulated and experimental results for the insertion loss of the output network for Design 1.

A photograph of the experimental output circuit for Design 1 is shown in Figure 2.7. The design is fabricated on a Rogers R4350 substrate; the dielectric thickness is 60 mil and the copper conductor thickness is 1.5 mil.[2]

[2] 1 mil is 0.001 inches or 25.4 microns.

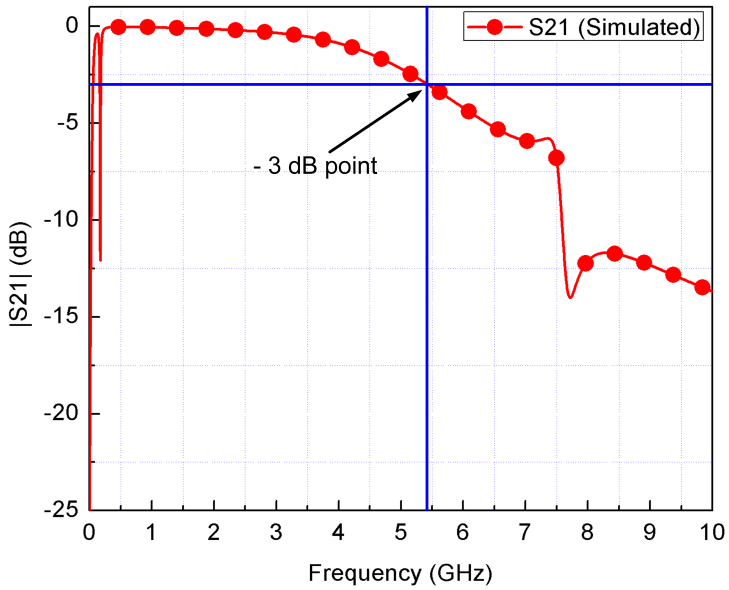

Figure 2.6: Simulated results for the insertion loss of the output network for Design 1 over an extended frequency range up to 10 GHz.

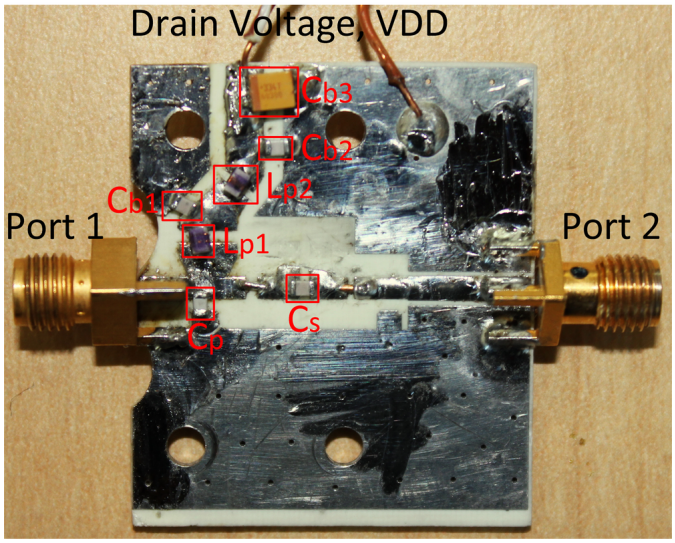

Figure 2.7: Picture of the output network for Design 1.

2.2 Design 2: Tuned Broadband RF SMPA with a 50 Ω Load

2.2.1 Design Considerations

Figure 2.8 shows Design 2, a tuned broadband RF switch-mode power amplifier (SMPA) with a 50 Ω load. The circuit diagram is similar to Design 1 except the value of the drain bias inductor L_p is selected to resonate with the output capacitance of the device. Therefore, in this design it is necessary to estimate the output capacitance of the 10 W HEMT GaN Cree device.

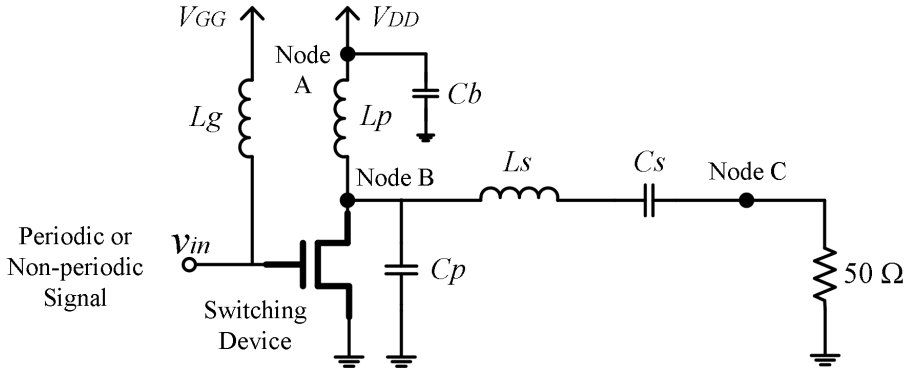

Figure 2.8: Circuit diagram of the tuned broadband RF switch-mode power amplifier (Design 2).

2.2.2 Determination of the Output Capacitance of the Cree Device

The measurement of the effective output capacitance of the device is very crucial in the amplifier design because it helps to choose the right value of other circuit components. The effective output capacitance is non-linear

and the effective value of C_p depends on the amplitudes of the switching voltages and currents in the device. Since the output capacitance is non-linear, analysis is very difficult and our goal here is to estimate an effective output capacitance from the device model that can be used in the design.

Figure 2.9 shows the circuit diagram for a simulation test bench used to measure output capacitance at different bias conditions. The gate voltage V_{GG} is varied from +1 V to -5 V with a step of 1 V and drain voltage from +8 V to +80 V. A simplified circuit diagram of the output admittance network looking into port 1 is also shown in Figure 2.10.

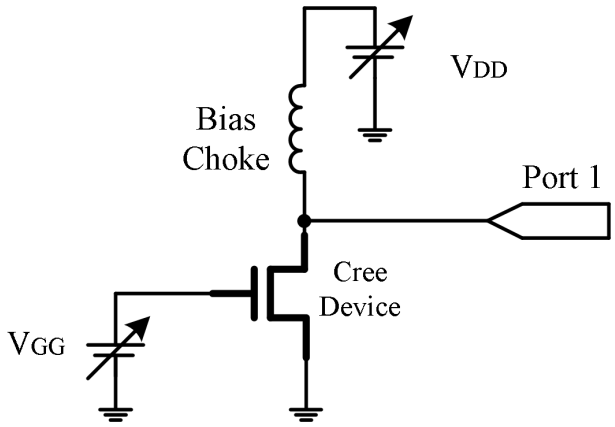

Figure 2.9: Circuit diagram to determine output capacitance.

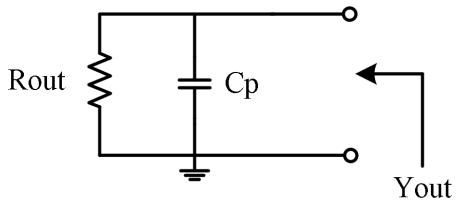

Figure 2.10: Simplified circuit model of the output admittance network of the Cree device looking into port 1.

Figure 2.11 shows the input reflection coefficient ($S11$) at port 1 for a

1 GHz frequency on a Smith chart with an admittance chart. Here, we are only showing the results of $S11$ for a particular case of gate and drain bias conditions; V_{GG} is -1 V and the V_{DD} is +30 V. From this figure, the value of the normalized output admittance $\overline{y_{out}}$ is (0.336+j0.510) at 1 GHz where the normalizing impedance is 50 Ω. An over-bar is used to denote normalized quantities. The input admittance can be separated into real and imaginary parts that correspond to conductance and susceptance:

$$\overline{y_{out}} = \overline{g_{out}} + j\overline{b_{out}}. \tag{2.1}$$

The susceptance can then be equated to find the effective capacitance

$$\begin{aligned} \overline{b_{out}} &= 50\omega_c C_p \\ C_p &= \frac{\overline{b_{out}}}{50\omega_c} \end{aligned} \tag{2.2}$$

where $\omega_c = 2\pi f$ is the frequency of the measurement. For the measurement in Figure 2.11, f_c = 1 GHz, $\overline{b_{out}}$ = 0.511, and the output capacitance C_p is calculated to be 1.62 pF. In a similar way the value of the C_p for different switching conditions can be determined. The extracted model values for C_p are summarized in Figure 2.12. As the data show, the capacitance characteristics are highly nonlinear and the data is now used to calculate an effective output capacitance.

In Design 2, the drain-source voltage varies from 0 V to 60 V while the gate-source voltage varies from 0 V to -4 V. Note that a 0 V gate voltage means the device is in the on state and -4 V means the device is in the off state. Using data from Figure 2.12, C_p is 2.3 pF in the on state and 1.45 pF in the off state. The average of these two values is approximately 1.9 pF

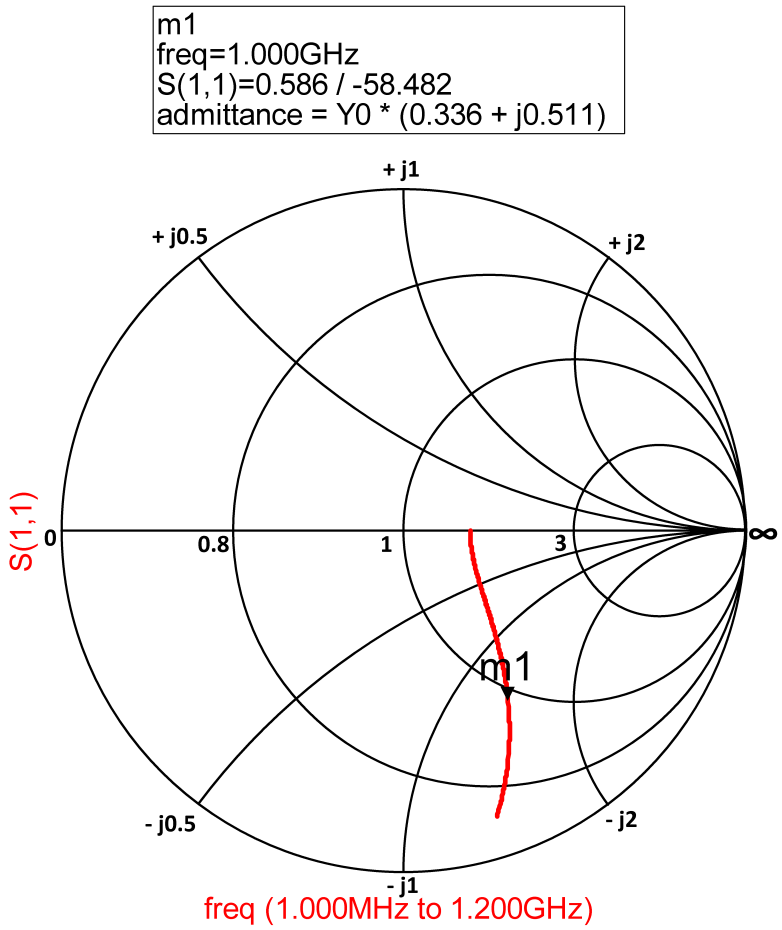

Figure 2.11: Small signal output admittance for a bias of V_{GG} = -1 V and the V_{DD} = +30 V .

which is the estimated effective output capacitance of the Cree device.

2.2.3 Output Network Design

Figure 2.13 shows the equivalent circuit for the output network in Design 2. In Design 2, the output capacitance C_p, is tuned with the drain bias inductor L_{p1} at a frequency of 1 GHz. The second inductor L_{p2} is used to

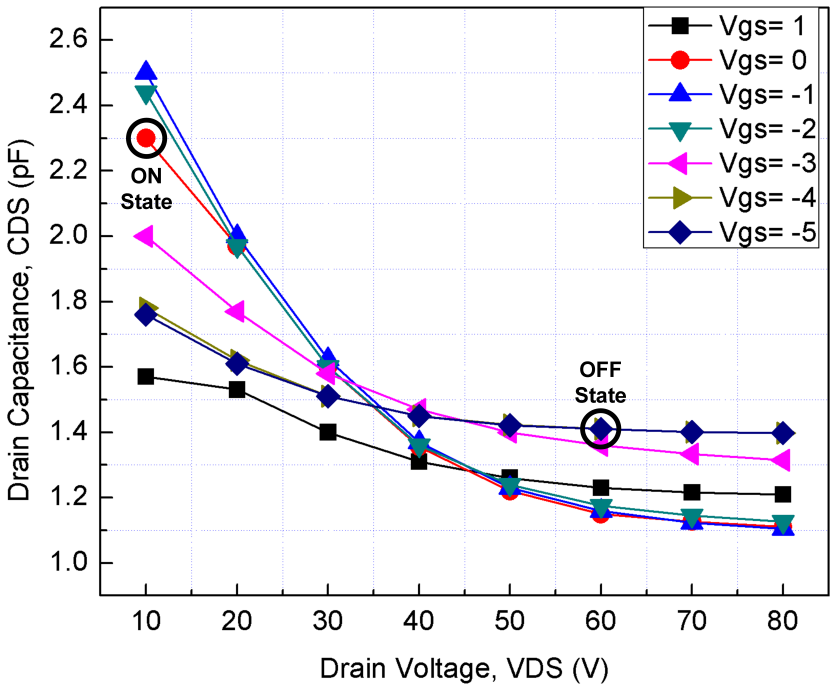

Figure 2.12: Extracted output capacitance, C_p, for the Cree device for different gate and drain voltages at a frequency of 1 GHz.

enhance the low frequency characteristics and a final value for this inductor is determined using simulation.

An initial value for L_{p1} is calculated using basic equations for a parallel resonant circuit. Therefore,

$$C_p = \frac{Q}{\omega_c R_{50}}$$
$$L_{p1} = \frac{R_{50}}{\omega_c Q} \tag{2.3}$$

where R_{50} is the 50 Ω load, Q is the loaded quality factor, and $\omega_c = 2\pi f_c$ where f_c is the center frequency. A value of 2 pF is used for C_p which was the closest value of a fixed capacitor value to model C_p in experiments to verify

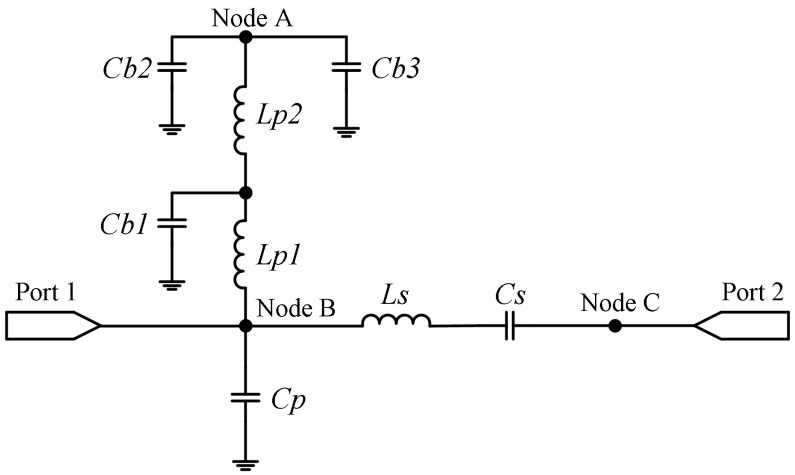

Figure 2.13: Equivalent output network for frequency response measurements of the tuned broadband SMPA (Design 2).

the operation of the output circuit. Using equation (2.3), the value of L_{p1} is 12.68 nH and Q is 0.628. The closest possible inductor value from Coilcraft is 12 nH and it is chosen for the final output network design. Note that the value of the quality factor is low which supports the broadband load theory and it is expected to pass harmonic power to the output terminal. The value of the other components in the output network are given in Table 2.2.

Table 2.2: Experimental circuit component values of output matching network for Design 2.

Components	Values
L_{p1}	12 nH
L_{p2}	82 nH
C_p	2 pF
C_{b1}	100 pF
C_{b2}	100 pF
C_{b3}	0.33 μH
L_s	2.2 nH
C_s	33 pF

Figure 2.14 shows both experimental and simulated results for $|S22|$ to evaluate the output match at port 2. The two data sets are similar and the dip in $|S22|$ at 1 GHz frequency shows that the circuit is matched at this frequency. A -15 dB reference line is shown in this figure. For the frequency range of 0.9 GHz to 1.1 GHz, the return loss is below -15 dB. The output match is therefore narrower than Design 1 and shows that the tuned output network has come at the expense of a reduction in bandwidth. Performance is expected to be good in a frequency range near 1 GHz and fall off as the frequency moves away from 1 GHz.

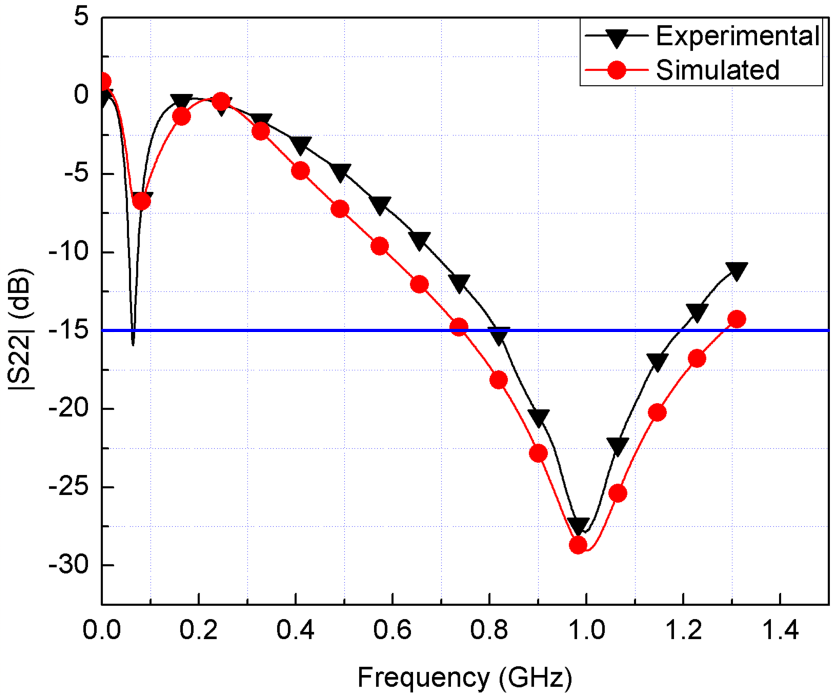

Figure 2.14: Output reflection coefficient $|S22|$ at port 2 of Figure 2.13.

Next, Figure 2.15 shows the experimental and simulated results for insertion loss ($S21$). Both curves are very close to each other and insertion

loss is about 0.2 dB for frequencies above 0.5 GHz. From this figure it is hard to make any conclusion about the upper frequency limit of the output matching network because we are restricted to 1.5 GHz. As the experimental and simulated results are similar, the simulation model is used to extend the frequency sweep. Figure 2.16 shows the extended simulation results for $S21$ up to a frequency of 6 GHz. Based on simulation results, the estimated -3 dB bandwidth is approximately 2.4 GHz. If the center frequency is 1 GHz, then it is expected that harmonic power will include the second harmonic and approximately 40% of the third harmonic. A photograph of the implemented output circuit is shown in Figure 2.17.

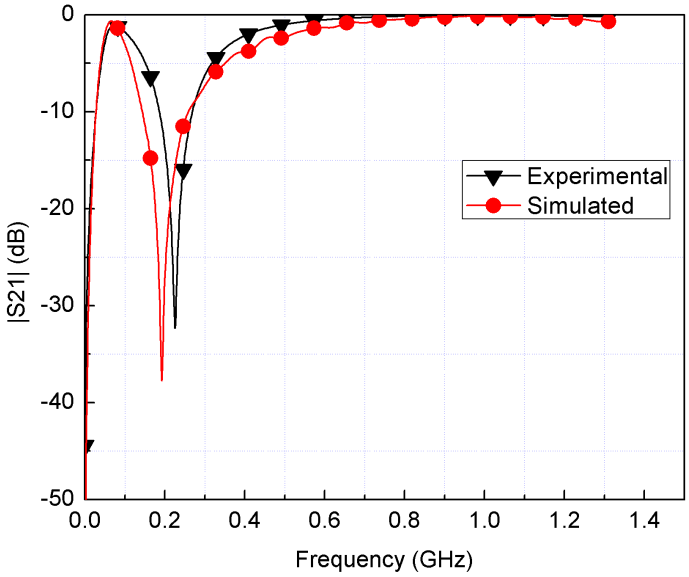

Figure 2.15: Simulated and experimental measurements of insertion loss $|S21|$ for Design 2 up to 1.5 GHz.

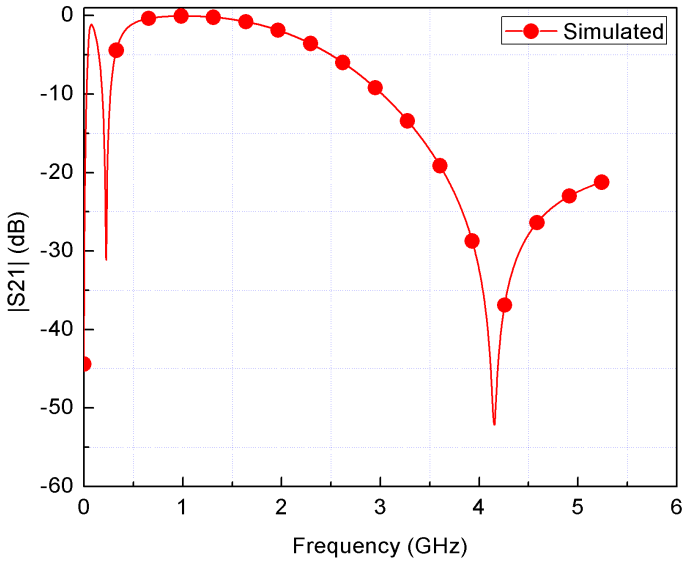

Figure 2.16: Simulated insertion loss $|S21|$ of the output network of the Design 2 up to 10 GHz.

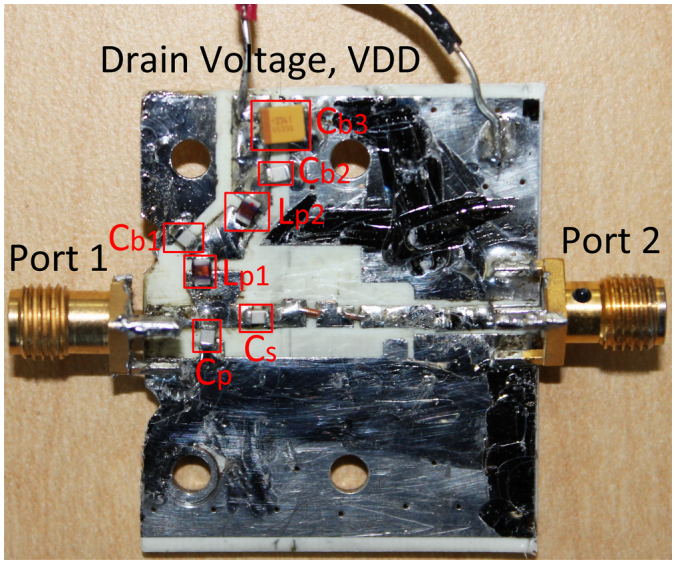

Figure 2.17: Picture of the output network for Design 2.

2.3 Design 3: Broadband RF SMPA with an Optimum Load, R_{opt}

2.3.1 Design Considerations

Calculating R_{opt}

In Design 3, the device is matched to a load impedance called R_{opt} that is not equal to 50 Ω. R_{opt} is selected to maximize the power delivered by the switch to the load and is determined from a load line analysis of the device. An equivalent model for Design 3 is shown in Figure 2.18 where the output load is now replaced by R_{opt}.

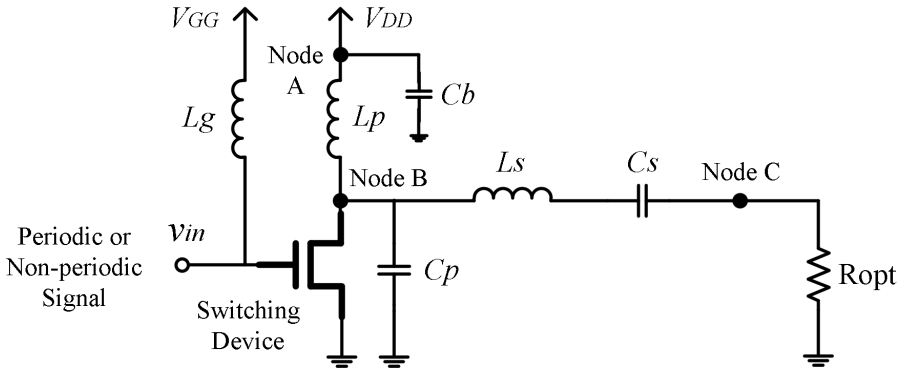

Figure 2.18: Simplified circuit diagram of the Design 3 with an optimum load R_{opt}.

The ideal load line for the device is shown in Figure 2.19. The optimum load line is found from the slope of the line which passes through (V_k, I_{max}) and (V_{max}, 0). The bias point or quiescent point is indicated by Q on the load line. The optimum load, R_{opt} can be determined from the value of the maximum available drain voltage and current for a 50% duty cycle input source. The optimum load resistance is

$$R_{opt} = \frac{(V_{max} - V_k)}{I_{max}} \tag{2.4}$$

and the corresponding drain bias voltage is

$$\begin{aligned} V_{DD} &= \frac{(V_{max} - V_k)}{2} + V_k \\ &= \frac{(V_{max} + V_k)}{2} \end{aligned} \tag{2.5}$$

where V_k is the knee voltage, V_{max} is the maximum drain-source voltage across the switch and I_{max} is the maximum drain-source current through the switch. From the drain-source characteristics of the 10 W Cree GaN device in Figure 2.2, the selected values for calculating the optimum load are: $V_{max} = 65$ V, $I_{max} = 2.3$ A and $V_k = 5$ V. After substituting these values in equation (2.4), the value of the optimum load is 25.6 Ω.

Matching Network Design

Since a 50 Ω output impedance is required to interface with the diplexer, a matching network is required to transform R_{opt} to 50 Ω. Figure 2.20 shows the basic block diagram of the impedance transformation from R_{opt} to 50 Ω. There are several ways to do this impedance transformation using either lumped components or distributed transmission line components. For example a stepped transmission line could be used or a multistage lumped element circuit could be used. How the network is implemented has a significant effect on the loss in the network, the size of the layout, and the bandwidth of the network. In this work, a transmission line design synthesizing an equivalent multistage L-match network is used. A model of the matching network is shown in Figure 2.21.

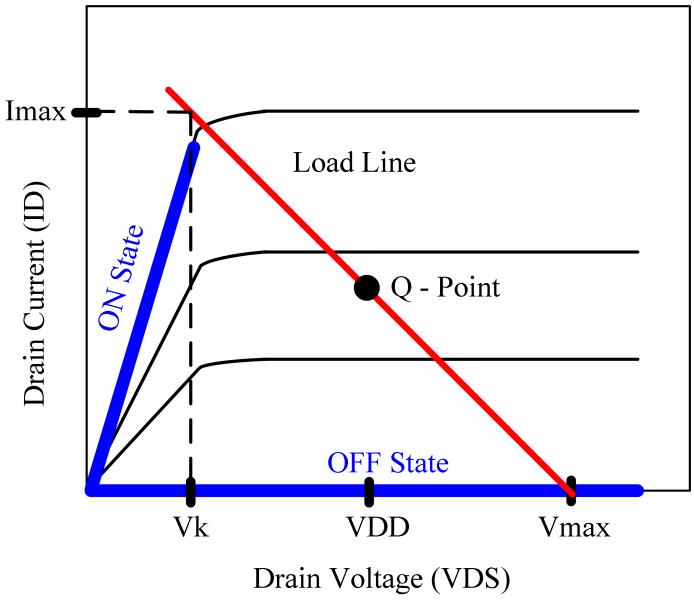

Figure 2.19: Ideal switching characteristics of a RF switch-mode power amplifier.

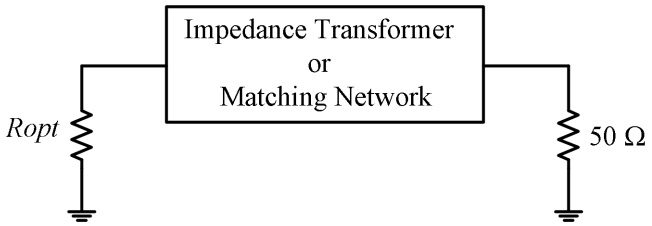

Figure 2.20: Block diagram of the impedance transformation from R_{opt} to a 50 Ω load.

2.3.2 Output Network Design

Figure 2.22 shows the circuit diagram for Design 3 with a multistage matching network. At node C, the load is R_{opt} and then it is transformed to 50 Ω at node D. Using the values of the optimum load and the output capacitance of the device, the value of L_{p1} can be calculated using equation (2.3). For a frequency of 1 GHz L_{p1} is 12.68 nH. It is same value as

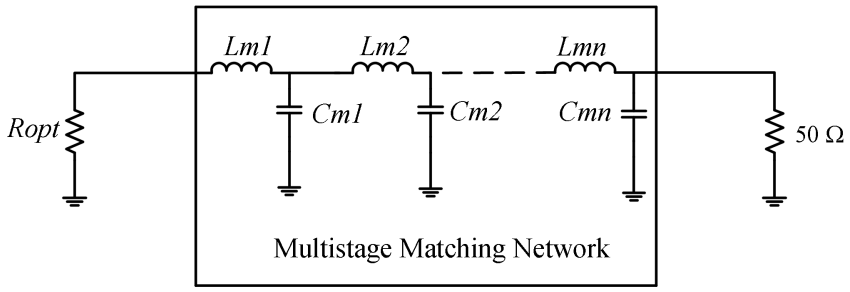

Figure 2.21: Multistage matching network to transform R_{opt} to a 50 Ω load.

Design 2 because the center frequency is same; only the quality factor is changed and has a value of 0.3125 in Design 3.

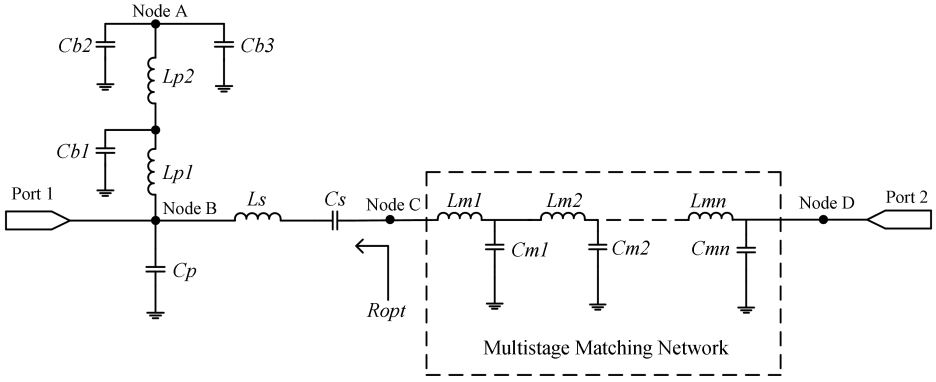

Figure 2.22: Equivalent output network for frequency response measurements of the optimum broadband RF switch-mode power amplifier (Design 3).

The calculated values were used for initial component values in the simulator. The simulator was then used to explore power and efficiency trade-offs in the design. The best value for the R_{opt} was found to be 33.3 Ω for maximum drain efficiency condition, a value 1.3 times larger than the calculated value. The value of the other components in the output network are summarized in Table 2.3.

Table 2.3: Experimental circuit component values of output matching network for Design 3.

Components	Values
L_{p1}	12 nH
L_{p2}	82 nH
C_p	2 pF
C_{b1}	100 pF
C_{b2}	100 pF
C_{b3}	0.33 μH
L_s	2.2 nH
C_s	33 pF
R_{opt}	33.3 Ω

The next step is to convert R_{opt} to a 50 Ω load. A three stage L-match design based on binomial transformer intermediate impedances is used in Design 3. The design details are described in the next section.

2.3.3 Multi-stage L-match Circuit

A multi-stage match is implemented based on impedances determined from a binomial stepped transmission line design. A binomial transformer transforms a real source impedance to an output load impedance in N steps using a series of quarter wave transformers. The number of sections determines the bandwidth of the match and bandwidth improves as more sections are added. The disadvantage of adding more sections is that the physical space of the matching network becomes large. To keep the output match network compact, the binomial transformer is converted to an equivalent L-match circuit. The intermediate impedance levels in the L-match circuit are calculated using binomial transformer design equations.

The passband response of a binomial matching transformer is optimum in the sense that, for a given number of sections, the response is as flat as

possible near the design frequency. Thus, such a response is also known as maximally flat. If Z_n is defined as the characteristic impedance of the n^{th} section, then [12],

$$\begin{aligned} \ln(Z_{n+1}) &= \ln(Z_n) + 2^{-N} {C_n}^N \ln\left(\frac{Z_L}{Z_{opt}}\right) \\ \text{or, } Z_{n+1} &= \exp\left[\ln(Z_n) + 2^{-N} {C_n}^N \ln\left(\frac{Z_L}{Z_{opt}}\right)\right] \end{aligned} \tag{2.6}$$

where ${C_n}^N$ is the binomial coefficient and Z_L and Z_{opt} are the load and source impedance respectively.

From equation (2.6), the characteristic impedances for a three stage network ($N = 3$) are:

$$\begin{aligned} Z_1 &= \exp\left[\ln(Z_0) + 2^{-N} {C_n}^N \ln\left(\frac{Z_L}{Z_{opt}}\right)\right] \\ Z_2 &= \exp\left[\ln(Z_1) + 2^{-N} {C_n}^N \ln\left(\frac{Z_L}{Z_{opt}}\right)\right] \\ Z_3 &= \exp\left[\ln(Z_2) + 2^{-N} {C_n}^N \ln\left(\frac{Z_L}{Z_{opt}}\right)\right]. \end{aligned} \tag{2.7}$$

Here, Z_0 is Z_{opt} because this is the impedance of the zero section and Z_L is 50 Ω. After substituting these values in equation (2.7), the value of the three transformer impedances are:

$$\begin{aligned} Z_1 &= 35\ \Omega \\ Z_2 &= 40.8\ \Omega \\ Z_3 &= 47.5\ \Omega. \end{aligned} \tag{2.8}$$

Figure 2.23 shows the circuit diagram of the three stage binomial transformer. Z_1, Z_2 and Z_3 are the characteristic impedances of each section and

R_{IM1} and R_{IM2} are the accumulated intermediate impedances seen looking towards the source. It is necessary to know the intermediate impedances to convert this network into a LC ladder network. For a binomial multistage match, the impedance of the n^{th} stage is equal to the geometric mean of the preceding and following stage. Thus,

$$Z_n = \sqrt{Z_{n-1}Z_{n+1}} \tag{2.9}$$

and for this design case, the three expressions are [13],

$$\begin{aligned} Z_1 &= \sqrt{R_{opt}R_{IM1}} \\ Z_2 &= \sqrt{R_{IM1}R_{IM2}} \\ Z_3 &= \sqrt{R_{IM2}R_L}. \end{aligned} \tag{2.10}$$

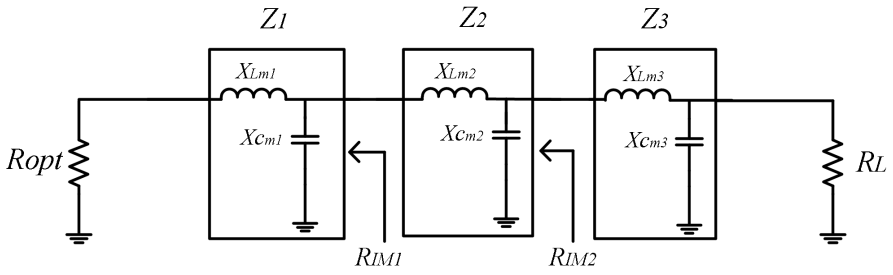

Figure 2.23: Three stage binomial transformer.

After using the three characteristic impedance values from equation (2.8) in equation (2.10), the values of the intermediate impedances are [13]

$$\begin{aligned} R_{IM1} &= 36.79\ \Omega \\ R_{IM2} &= 45.13\ \Omega. \end{aligned} \tag{2.11}$$

Next, each characteristic impedance block is converted into a $L-$match network. The impedance transformation ratios are

$$\begin{aligned} m_1 &= \frac{R_{IM1}}{R_L} \\ m_2 &= \frac{R_{IM2}}{R_{IM1}} \\ m_3 &= \frac{R_L}{R_{IM2}}. \end{aligned} \tag{2.12}$$

The corresponding values for the equivalent L-match cascade are:

$$\begin{aligned} X_{Cm1} &= \frac{R_{IM1}}{\sqrt{(m_1-1)}} \\ X_{Cm2} &= \frac{R_{IM2}}{\sqrt{(m_2-1)}} \\ X_{Cm3} &= \frac{R_L}{\sqrt{(m_3-1)}}; \end{aligned} \tag{2.13}$$

$$\begin{aligned} X_{Lm1} &= R_L\sqrt{(m_1-1)} \\ X_{Lm2} &= R_{IM2}\sqrt{(m_2-1)} \\ X_{Lm3} &= R_L\sqrt{(m_3-1)}. \end{aligned} \tag{2.14}$$

After calculating the reactance values using the equations above, the capacitor and inductor values can be determined as follows:

$$\begin{aligned} C_{m1} &= \frac{1}{2\pi f X_{Cm1}} \\ C_{m2} &= \frac{1}{2\pi f X_{Cm2}} \\ C_{m3} &= \frac{1}{2\pi f X_{Cm3}}; \end{aligned} \tag{2.15}$$

$$\begin{aligned} L_{m1} &= \frac{X_{Lm1}}{2\pi f} \\ L_{m2} &= \frac{X_{Lm2}}{2\pi f} \\ L_{m3} &= \frac{X_{Lm3}}{2\pi f}. \end{aligned} \tag{2.16}$$

The values are tabulated in Table 2.4. The values are small and difficult to implement with off the shelf lumped components. Additionally, the voltages across these components can be large at high power and dissipation can be a problem. For these reasons, the lumped element values are implemented by equivalent transmission line structures.

Table 2.4: Capacitor and inductor values for the matching circuit.

Components	Values
C_{m1}	1.412 pF
C_{m2}	1.673 pF
C_{m3}	1.041 pF
L_{m1}	1.733 nH
L_{m2}	2.785 nH
L_{m3}	2.351 nH

In the ADS circuit simulator, the dimensions of the transmission lines in the matching network are optimized. The final dimensions of the transmission lines are given in Table 2.5 for a Rogers 4350 subtrate. The substrate properties are summarized in Table 2.6.

Simulation and experimental results were made to characterize the output network response. Figure 2.24 shows return loss measured at the output port. In making these measurements, port 1 is terminated with 50 Ω because the network analyzer has port impedances of 50 Ω. Therefore, the measurements do not directly correspond to the conditions in the circuit when the device is driving the input port. However, the correlation between

Table 2.5: Transmission line dimensions for the output matching circuit in Design 3.

Components	Width (mil)	Length (mil)
C_{m1}	350	680
C_{m2}	150	379
C_{m3}	150	540
L_{m1}	45	410
L_{m2}	40	270
L_{m3}	35	220

Table 2.6: Substrate process parameters.

Parameters	Values
Substrate Thickness	60 mil
Dielectric Constant, ε_r	3.48
Dissipation Factor, δ	0.0031
Copper Thickness	1.4 mil

model and measurements is a useful comparison and the results are similar. Measurements of insertion loss are shown in Figures 2.25 and Figure 2.26. Similar to the measurements in the other designs, an extended frequency range simulation is used to estimate bandwidth. From Figure 2.26, the estimated -3 dB bandwidth is about 1.8 GHz. For a center frequency of 1 GHz it is expected that up to 80% of second harmonic power will pass through to the output. Beyond the second harmonic, no significant output power is expected and the data shows that the bandwidth of Design 3 is even narrower than Design 2. A photograph of the complete SMPA with the output match is shown in Figure 2.27. Unlike the photos for Designs 1 and 2, this photo includes the driver and Cree power device. The driver stage is described in more detail in the next section.

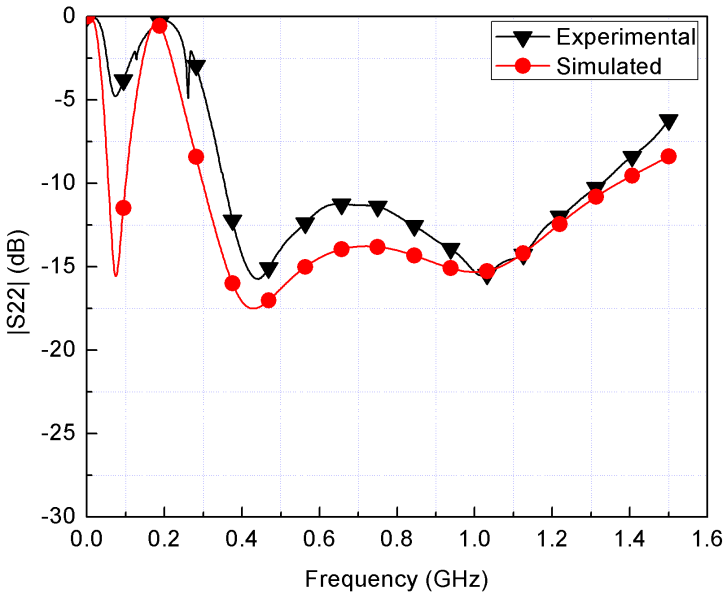

Figure 2.24: Output reflection coefficient $|S22|$ at port 2 of Figure 2.22.

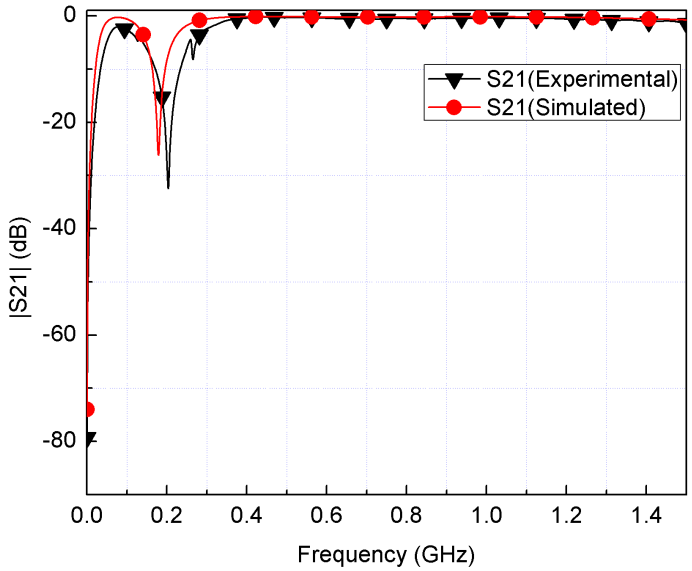

Figure 2.25: Simulated and experimental results for insertion loss $|S21|$ of the output network for the Design 3.

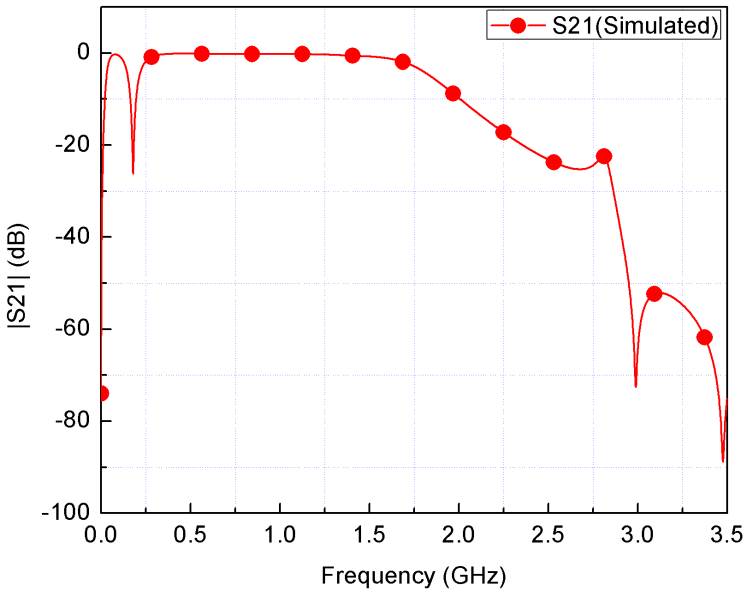

Figure 2.26: Simulated insertion loss $|S21|$ of the output network for Design 3.

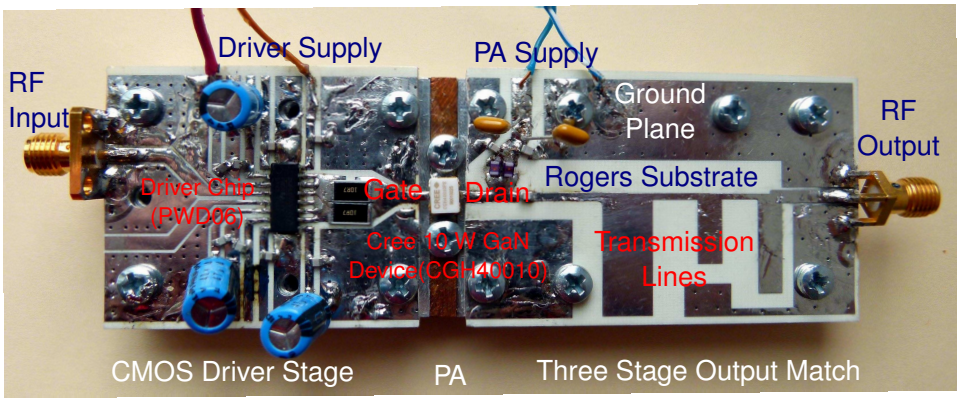

Figure 2.27: Picture of the experimental prototype of Design 3 with a driver board and a 10 W GaN Cree device.

2.4 Driver for the Final Stage of the SMPA

A driver is required to switch the gate of the power device. The driver needs to have a low impedance high current output to generate fast switching transitions. In this design, a PWD06 CMOS driver from PWRF Inc. is used. The nominal specifications for this driver chip are given in Table 2.7.

Table 2.7: Nominal parameters of the PWD06 driver chip.

Parameters	Values
RF Input Frequency Range	30 - 3000 MHz
RF Input Level	0 dBm
RF Input Return Loss at 1 GHz	-14 dB
Insertion Delay	550 ps
Instantaneous Bandwidth	$>$ 2.5 GHz
Nominal Output Resistance	1.6 Ω
Nominal Output Voltage	Max. 4.2 V

The driver has an output impedance of 1.6 Ω with a small signal gain of approximately 35 dB. Sinusoidal input signals are clipped to generate square wave output pulse trains. The input and output terminals of the driver are AC coupled through capacitors. The driver also has a 100 Ω resistor connected to the output terminal which can be used to supply a DC bias to the gate. A gate bias of -2.5 V is used and the driver has a 4 V output swing.

The driver to gate interface must be carefully designed to minimize parasitic inductance. In this design, the parasitic inductance is estimated to be about 1 nH. A series damping resistor 5.35 Ω (combination of two parallel 10.7 Ω resistors) is placed between the driver output and gate. The

resistance was selected to maximize the drain efficiency of the power switch stage.

The pin diagram of the PWD06 driver chip is shown in Figure 2.28 and the description of the pins are tabulated in Table 2.8. A simplified circuit diagram of the chip is shown in Figure 2.29 and the description of the nominal circuit parameters are tabulated in Table 2.7.

A picture of the implemented driver board is shown in Figure 2.30. The circuit board is a Rogers R4350B substrate - the same substrate used for the output network. The properties of this substrate were given earlier in Table 2.6. The measured driver response for a 1 GHz sine wave input signal with an input power of 0 dBm is shown in Figure 2.31. The response is measured with a 50 Ω load and captured on a high speed oscilloscope (Tektronix model DP070804B). The output is a square wave signal and shows that the driver amplifies and clips the sinusoidal signal to generate an output pulse train which controls the state of the power switch. The driver output for another test signal is shown in Figure 2.32. The input signal in this case is a pseudo-random bit sequence (PRBS) from a pattern generator. The PRBS test pattern in non-periodic and used to evaluate the performance of the SMPA. In Chapter 4, both test signals will be used to measure the performance of the RF SMPA designs.

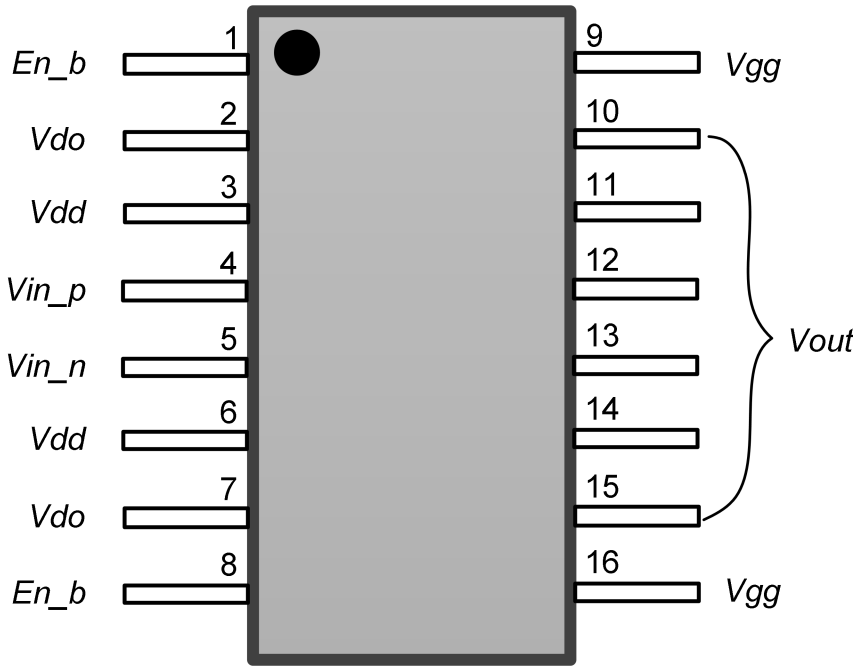

Figure 2.28: Pin diagram of the PWD06 driver chip.

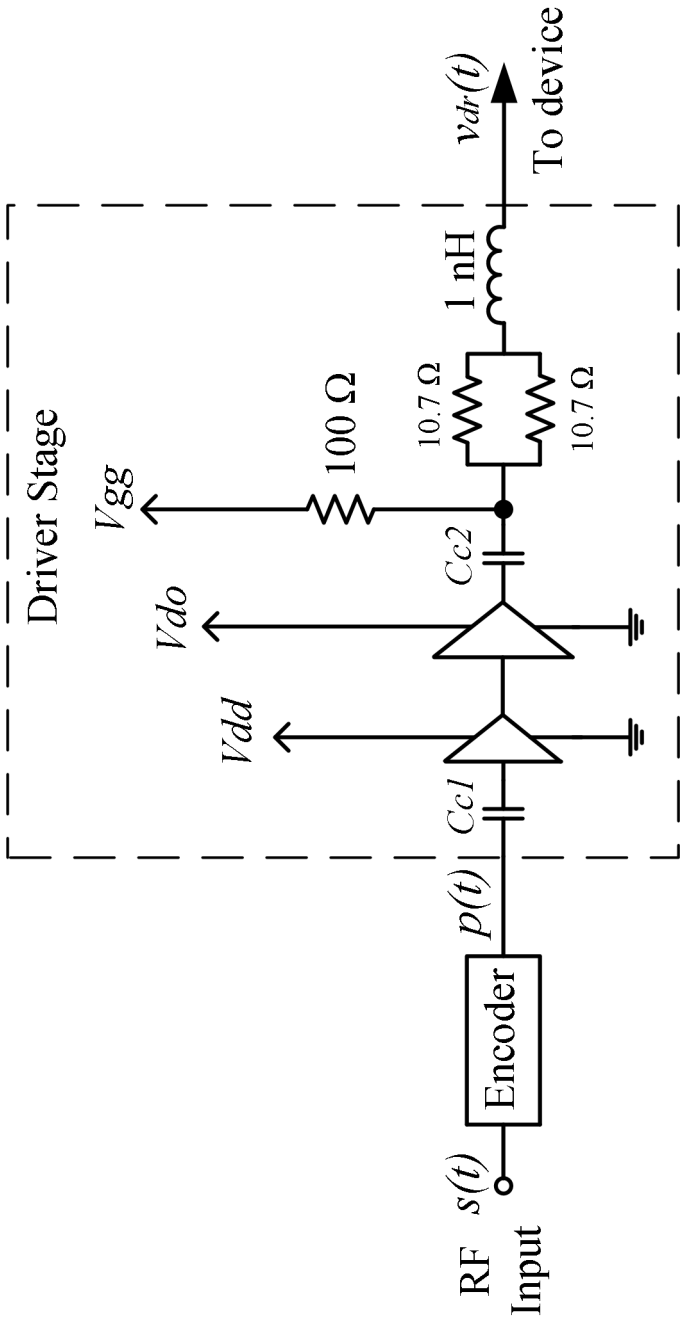

Figure 2.29: Internal circuit diagram of the driver board.

Table 2.8: Description of the pins of the PWD06 driver chip.

Pin	Mnemonic	Description	Nominal value
1, 8	En_b	Active low enable, or active high disable	-
2, 7	V_{do}	Output stage supply voltage	4.1 V
3, 6	V_{dd}	Internal circuits supply voltage	2.1 V
4	V_{in_p}	50 Ω differential terminated input, positive side	-
5	V_{in_n}	50 Ω differential terminated input, negative side	-
9, 16	V_{gg}	DC bias voltage input pin for routing bias to next stage gate input, Resistively connected to V_{out}	-2.5 V
10, 11, 12, 13, 14, 15	V_{out}	Driver outputs	-
Backside metal	GND	Ground	-

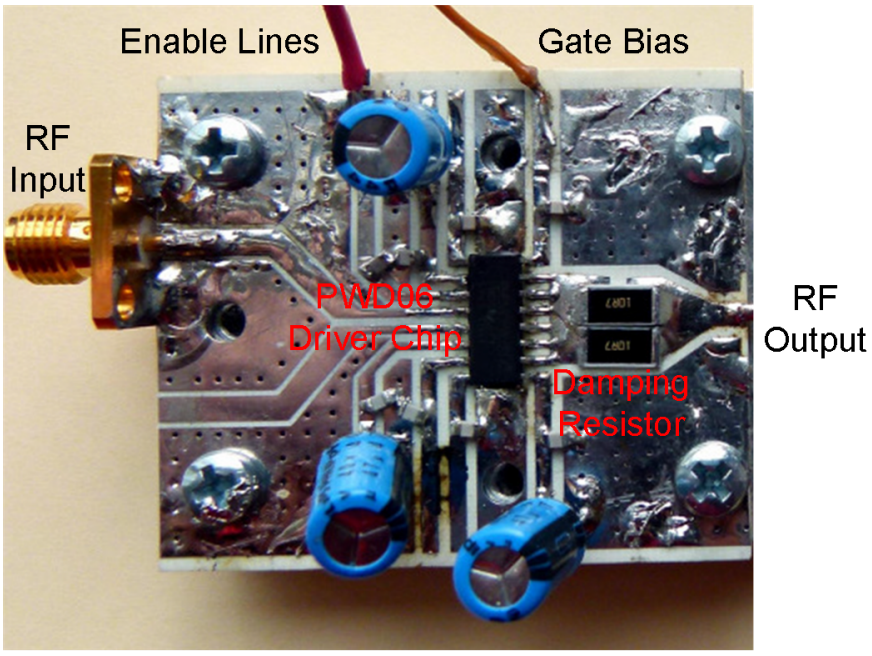

Figure 2.30: Picture of the driver board.

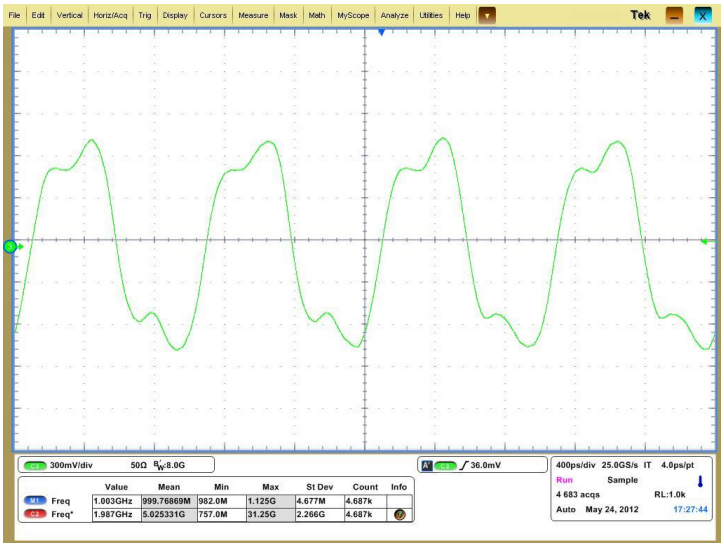

Figure 2.31: Measured driver response for a 1 GHz CW input signal across a 50 Ω load.

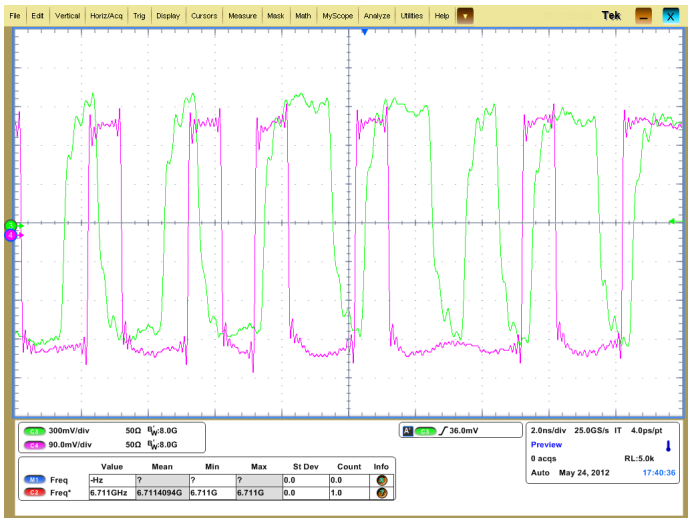

Figure 2.32: Measured driver output wave shape at 1 GHz frequency for PRBS excitation across a 50 Ω load (red line indicates the driver input and green line indicates driver output).

Chapter 3

Complementary Diplexer

An integral part of the proposed SMPA architecture is an output diplexer to separate in-band and out-of-band components of the amplified pulse train. The diplexer design has the additional constraint that the input impedance is constant over the entire bandwidth of the spectrum. In other words, the diplexer is equivalent to the 50 Ω load which was assumed in the previous chapter. A special diplexer called the complementary diplexer has the property that the input port is matched for all frequencies. The purpose of this chapter is to explain the theory of complementary diplexers and describe the implementation of an experimental prototype used in the SMPA.

3.1 Background

A diplexer is a single input two output filter bank that splits a common input frequency band into two distinct output bands. In terms of network theory, a diplexer is a three port network where each port is terminated in an impedance. A block diagram of an ideal diplexer is shown in Figure 3.1. It consists of two parallel connected resistively terminated lossless filters, one of which is a lowpass and the other is a highpass. Network equations in terms of Y-parameters for the diplexer are given below:

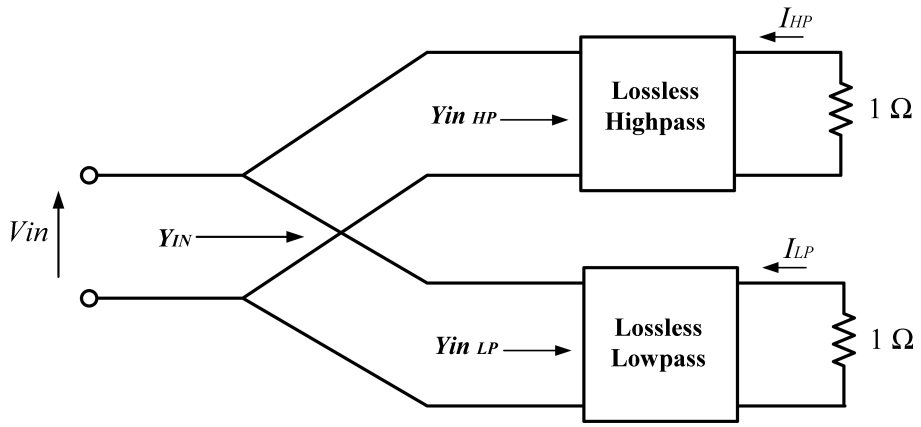

Figure 3.1: Basic block diagram of a diplexer.

$$\begin{aligned} Y_{in} &= Y_{inLP} + Y_{inHP} \\ &= \mathrm{Re}[Y_{inLP}] + j\mathrm{Im}[Y_{inLP}] + \mathrm{Re}[Y_{inHP}] + j\mathrm{Im}[Y_{inHP}] \end{aligned} \tag{3.1}$$

$$|Y_{12HP}|^2 = \left|\frac{I_{HP}}{V_{in}}\right|^2 \tag{3.2}$$

$$|Y_{12LP}|^2 = \left|\frac{I_{LP}}{V_{in}}\right|^2. \tag{3.3}$$

In these equations, Y_{inLP} and Y_{inHP} are the input admittances of the lowpass and highpass sections respectively, V_{in} is the voltage across the input port, and I_{HP} and I_{LP} are terminal currents at the output ports. Also, without loss of generality, all terminal impedances are normalized to 1 Ω; terminal impedances can be scaled after a canonic prototype design is made.

3.2 Singly and Doubly Terminated Filters

In a doubly terminated filter, both the input and output ports are matched over the passband region of the filter. Out-of-band, the stop band impedance of the filter is unmatched and approaches either a short circuit or open circuit impedance depending on the design of the filter. In a doubly terminated filter, if a signal generator is used to sweep the frequency response of the filter, one would see that the voltage across the input terminals of the filter depends on frequency. If the frequency of the source is within the passband of the filter where the impedance of the source and filter are matched, the amplitude would be half the open circuit amplitude of the source. On the other hand, if the frequency is changed to the stop band of the filter, then the input voltage increases to the open circuit source voltage assuming the stop band impedance is an open circuit. Conversely, the voltage would collapse to zero if the stop band impedance is a short circuit. In other words, in a doubly terminated filter, the input terminal voltage depends on frequency and is simply another way of stating that the input impedance varies with frequency.

In a singly terminated filter, the input port impedance is constant and independent of frequency. A singly terminated filter design is distinctly different from a doubly terminated filter design. The input impedance is constant and filter prototypes are designed for an ideal voltage source or an ideal current source. As shown next, singly terminated filter prototypes are required to implement a complementary diplexer.

3.3 Complementary Diplexer

A complementary diplexer is a special diplexer which has two filter branches that sum to give an input impedance that is independent of frequency [14, 15]. Since the input impedance of a complementary diplexer is independent of frequency, each filter branch must be designed as a singly terminated filter. Therefore the filter design for a complementary diplexer begins with two singly terminated networks connected in shunt at the input terminal.

If the parallel connection of the filter networks shown in Figure 3.1 provides a constant admittance independent of frequency, then the sum of the lowpass and highpass input admittances must equal a constant. Using a normalized impedance of 1 Ω, the complementary condition then requires

$$Y_{in} = Y_{inLP} + Y_{inHP} = 1. \tag{3.4}$$

Consequently, the necessary condition is that the sum of the real parts of the input admittances must be constant and the reactive parts must be equal and of opposite sign. Thus,

$$\mathrm{Re}[Y_{inLP}] + \mathrm{Re}[Y_{inHP}] = 1 \tag{3.5}$$

$$\mathrm{Im}[Y_{inLP}] + \mathrm{Im}[Y_{inHP}] = 0. \tag{3.6}$$

For lossless networks terminated in a unit resistance

$$\mathrm{Re}[Y_{in}] = |Y_{12}|^2 \tag{3.7}$$

where Y_{12} is the ratio of output current to input voltage. Therefore, equation (3.4) to (3.7) requires that

$$|Y_{12}|^2{}_{LP} + |Y_{12}|^2{}_{HP} = 1. \tag{3.8}$$

At this point, we have an equation that links the transfer admittance of the lowpass and highpass filters. Stated another way, the frequency response of the two filter branches are coupled and the synthesis requires finding realizable functions for the filter branches. Fortunately, the maximally flat filter function can be manipulated to satisfy the complementary constraint. Other filters based on Chebyshev prototypes can be synthesized assuming the constant impedance condition is relaxed and satisfies a minimum return loss specification. An example of a lumped element Chebyshev filter diplexer is shown in the next section followed by a Butterworth filter diplexer design implemented with transmission line structures.

3.4 Lumped Element Complementary Diplexer Design

Lumped element filter prototypes are used as the first step in the synthesis of distributed filter designs. The lumped element values for the complementary filter branches are obtained from standard filter design tables for singly terminated filter networks. In the design procedure described below, it is assumed that the input terminal is connected to a voltage source. Therefore each filter branch is designed with a singly terminated network with zero source resistance.

The input impedance of the diplexer is ideally independent of frequency.

However, in practice a small variation in impedance is usually acceptable provided the impedance variation is small. We usually quantify the acceptable match in terms of a minimum return loss specification. For example, in a Chebyshev filter design, the in-band ripple is directly related to the minimum acceptable return loss. The same concept can be extended to the design of a diplexer where the input port impedance can vary providing it does not exceed a minimum return loss specification.

For the SMPA design, a diplexer with complementary bandpass and bandstop filter branches is required. The bandpass filter branch is a reconstruction filter and the attenuation characteristics must match the noise shaping characteristics in the encoder such that the output signal has an out-of-band noise spectrum that meets the spectral requirements of the transmitter. The diplexer design specifications are summarized below:

- center frequency of bandpass and bandstop filter branches: 1 GHz;
- -3 dB bandwidth of reconstruction filter: 50 MHz;
- out of band attenuation to create a flat noise spectrum assuming a fourth order noise shaping filter is used in the encoder. This corresponds to a two section low pass filter which is transformed into a fourth order (two resonator) bandpass filter;
- minimum input return loss of 20 dB for matched output ports;
- operating bandwidth: DC to 5 GHz.

Based on these specifications, a 0.5 dB ripple 5^{th} order Chebyshev filter response is selected. Normalized lowpass filter values for a singly terminated 0.5 dB ripple Chebyshev are given in Table 3.1. The table assumes the filter

Table 3.1: Normalized 0.5 dB Chebyshev element values for $R_s = 0$ or ∞.

Order	C_1	L_2	C_3	L_4	C_5	L_6	C_7
1	1.00000						
2	1.36144	1.01565					
3	1.57200	1.51790	0.93182				
4	1.45345	1.91162	1.53945	0.92395			
5	1.62994	1.73996	1.92168	1.51377	0.90343		
6	1.46994	1,99084	1.79019	1.93593	1.51606	0.90305	
7	1.64643	1.77716	2.03065	1.78918	1.92388	1.50337	0.89478
$R_s = 0$	L_1'	C_2'	L_3'	C_4'	L_5'	C_6'	L_7'

is terminated in a 1 Ω load and the filter cut-off frequency is 1 rad/s. Filter scaling and transformation functions can be used to convert these values to lowpass, highpass, bandpass, or bandstop filters. Since the prototype is consistent with the complementary condition, a lowpass/highpass or bandstop/bandpass diplexer can be obtained. The design steps for a n^{th} order lowpass/highpass complementary diplexer are summarized below:

- choose the normalized element values for order n with the desired filter prototype for a singly terminated network with $R_s = 0$;
- select the required transition frequency (cut-off frequency);
- scale the prototype lowpass values from $\omega_0 = 1$ rad/s, $R_0 = 1$ Ω to the desired values: multiply prototype inductor values by $R_0\omega_0$ and multiply prototype capacitor values by $1/(R_0\omega_0)$;
- exchange inductor and capacitors in the lowpass prototype to construct a highpass prototype;
- scale the prototype highpass values for the same cut-off frequency ω_0 and the required terminal impedance.

As an example, consider a lowpass/highpass complementary diplexer with a transition frequency of 1 GHz. The output port impedances are 50 Ω

and a 0.5 dB Chebyshev response is required. Using the above procedure gives the diplexer design shown in Figure 3.2. The design is verified in an ADS simulation and the simulation results are shown in Figure 3.3. From Figure 3.3 it is very clear that the - 3 dB cross-over frequency or center frequency is exactly 1 GHz. The input impedance is also very constant and $|S11|$ is no greater than -25 dB. The simulation results therefore confirm that the diplexer is indeed a complementary diplexer.

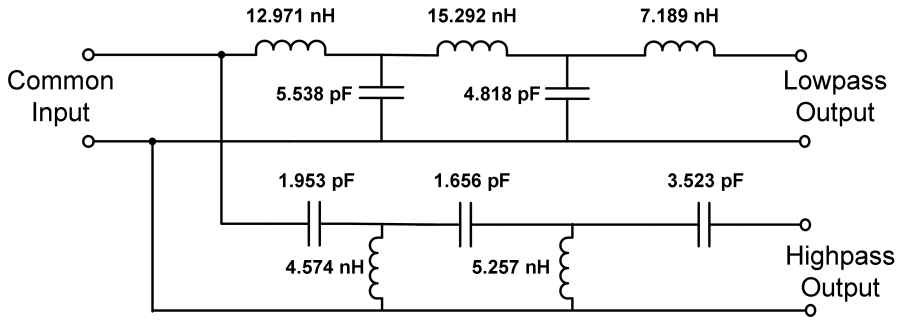

Figure 3.2: Circuit diagram of a lumped element 5^{th} order 0.5 dB ripple 1 GHz Chebyshev lowpass/highpass complementary diplexer.

A bandpass/bandstop diplexer can also be designed in a similar way from a lowpass/highpass filter type. First, the normalized lowpass filter values must be frequency and impedance scaled, then transformed into bandpass and bandstop sections. Figure 3.4 and Figure 3.5 shows the conversion procedure from a lowpass filter section to a bandpass section and a highpass filter section to a bandstop filter section. The formulas used to convert

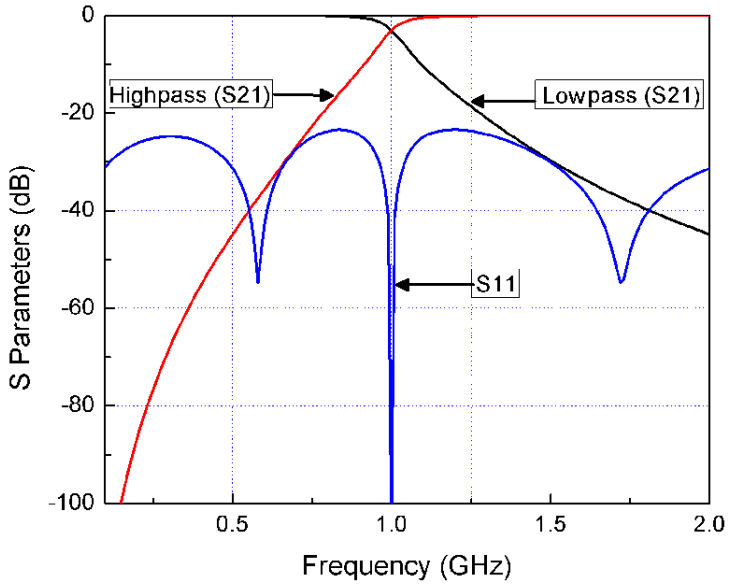

Figure 3.3: Simulation results of a 5^{th} order 0.5 dB ripple 1 GHz Chebyshev lowpass/highpass complementary diplexer.

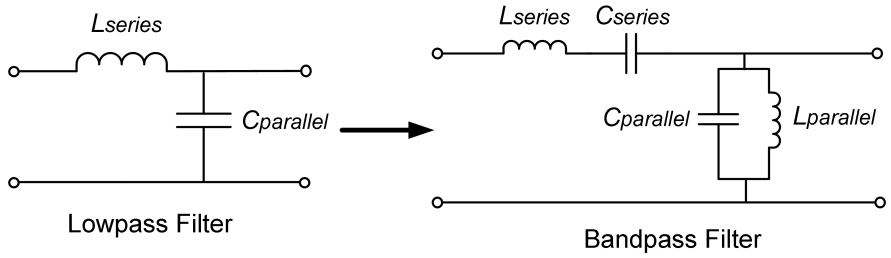

Figure 3.4: Circuit diagram showing the conversion procedure from a lowpass filter to a bandpass filter.

lowpass filter into a bandpass filter are given below:

$$C_{Series} = \frac{F_U - F_L}{2\pi F_U F_L R X} \tag{3.9}$$

$$L_{Series} = \frac{RX}{2\pi(F_U - F_L)} \tag{3.10}$$

$$C_{Parallel} = \frac{X}{2\pi(F_U - F_L)R} \tag{3.11}$$

$$L_{Parallel} = \frac{(F_U - F_L)R}{2\pi F_U F_L X} \tag{3.12}$$

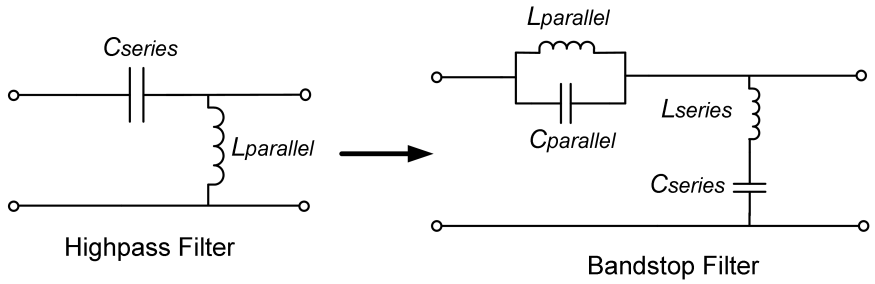

Figure 3.5: Circuit diagram showing the conversion procedure from a highpass filter to a bandstop filter.

Here, the series and parallel subscripts indicate which circuit element is being considered. In the equations, X is the normalized lowpass element value, F_U is the upper cutoff frequency, F_L is the lower cutoff frequency, and R is the termination resistance. The same value of X must be used for transforming a lowpass component into an inductor/capacitor pair. This is because each branch in the lowpass filter is transformed to either a series or parallel resonant circuit.

Similarly, formulas for converting highpass prototype values into a bandstop filter are:

$$C_{Series} = \frac{1}{2\pi(F_U - F_L)RX} \tag{3.13}$$

$$L_{Series} = \frac{(F_U - F_L)RX}{2\pi F_U F_L} \tag{3.14}$$

$$C_{Parallel} = \frac{(F_U - F_L)X}{2\pi F_U F_L R} \tag{3.15}$$

$$L_{Parallel} = \frac{R}{2\pi(F_U - F_L)X} \tag{3.16}$$

By using these transformations a 5^{th} order 0.5 dB ripple 1 GHz Chebyshev bandpass/bandstop complementary diplexer with a 2% bandwidth is

designed. The circuit diagram and simulated results are shown in Figure 3.6 and 3.7 respectively. Again, the simulation results clearly show the complementary attenuation characteristics of the bandpass and bandstop filter branches as well as a constant input impedance at the input terminal of the diplexer.

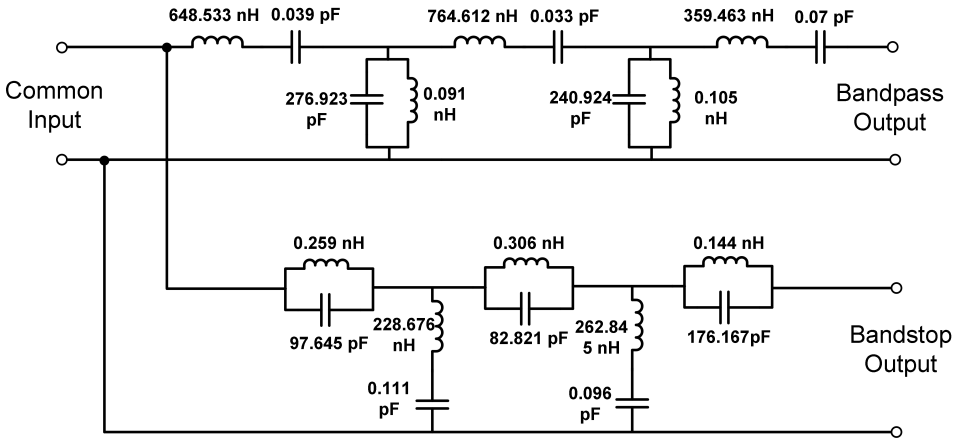

Figure 3.6: Circuit diagram of a 5^{th} order 0.5 dB ripple 1 GHz Chebyshev bandpass/bandstop complementary diplexer with 2% bandwidth.

3.5 Distributed Element Complementary Diplexer Design

Original work on the implementation of complementary diplexers using transmission line structures was first published by Wenzel in 1968 [16]. In terms of transmission line structures, design is simplified if the transmission lines satisfy the transverse electromagnetic (TEM) propagation conditions. Therefore designs using coaxial structures or stripline are preferred. A stripline design is implemented in this research project because it can be easily fabricated using circuit board techniques.

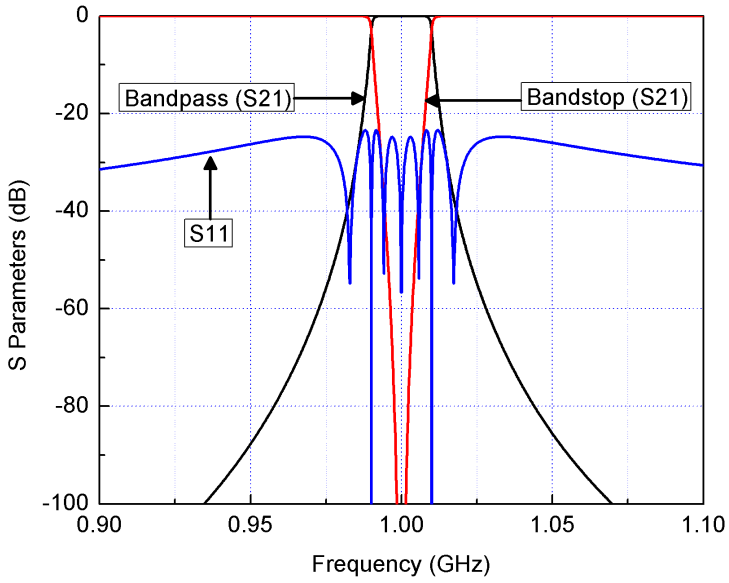

Figure 3.7: Simulation results of a 5^{th} order 0.5 dB ripple 1 GHz Chebyshev bandpass/bandstop complementary diplexer with 2% bandwidth.

The constraints imposed by the complementary condition make the design of a TEM diplexer more complicated than doubly terminated single branch TEM filters. Also, relatively few papers are available that describe complementary diplexer implementations; diplexer implementations with two distinct bandpass filter branches are much more common. Therefore, a more extensive description of the conversion of a lumped element design to a TEM design is presented. The final complementary diplexer is implemented in stripline using coupled resonator sections.

Lumped element filters can be implemented in distributed TEM structures by first mapping the inductors and capacitors to equivalent short circuit and open circuit transmission lines. The mapping function is called

Richard's transformation [12] and is given by

$$S = j\Omega = j \tan \frac{\pi\omega}{2\omega_0}. \tag{3.17}$$

An important difference between lumped element and distributed element filters obtained through the transformation is that the distributed structure has a periodic frequency response which is related to the length of the transmission line. This means that a lumped element lowpass filter can be transformed directly to a transmission line bandstop filter and a highpass filter can be transformed to a transmission line bandpass filter. For example, Figure 3.8 [17] shows how a lumped component highpass filter prototype is mapped into a distributed element bandpass filter using Richard's transformation.

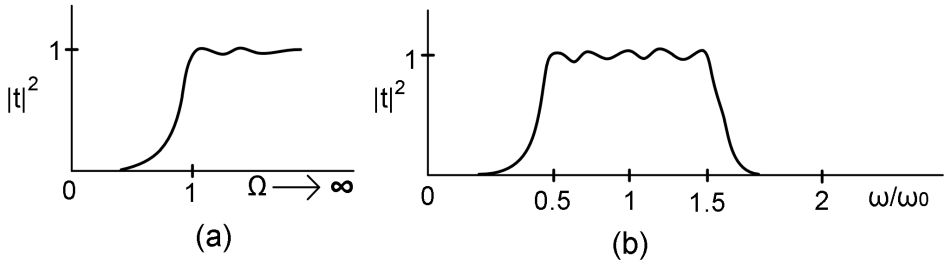

Figure 3.8: Mapping properties of the transformation $\Omega = \tan \frac{\pi\omega}{2\omega_0}$ (a) Prototype lumped element highpass (b) Corresponding distributed element bandpass.

Although Richard's transformation provides a way to map lumped element filters to distributed element filters, the resulting structures are usually difficult to implement because series elements map to series stubs. Fabricating series stubs is much more difficult than shunt stubs. Therefore, it is desirable to continue transforming the distributed circuit into a more convenient form. Kuroda's identities [12] are very useful for making these

transformations and it enables the synthesis of filter structures that consist of entirely shunt stubs.

The implementation of TEM filters can be carried to structures other than shunt stubs and often coupled transmission lines are preferred. For a pair of coupled lines there are ten different possible configurations that can be synthesized using only open and short terminations on the four port device [14]. Models for coupled lines can be found in many different references and a coupled line diplexer implementation is used in this work which is modeled on Wenzel's original paper [16].

But in the case of TEM distributed components, the diplexer design procedure is not straight forward. The main problem is related to the common input connection between two complementary filter branches. For example, in the case of doubly terminated parallel coupled narrow-band bandpass filters, we could obtain reasonable impedance levels by adding a redundant unit element of Z_0 to both the source terminal and load terminal. The addition of redundant elements does not change the transfer amplitude, it only alters the transfer phase. But, in case of singly terminated filter design, which is the key condition for complementary diplexers, we cannot apply a redundant unit element at the source terminal. A unit element can be placed at the common input terminal, but it cannot be shifted past the junction because this would then mean that the filter branches are no longer singly terminated. Therefore standard techniques to transform lumped element filters into distributed element filters cannot be applied at the source end of a singly terminated filter.

As a way around this problem, Wenzel proposes the addition of a coupled line to maintain the complementary impedance condition [16]. The coupled line shown in Figure 3.9(a) has four physical ports and the struc-

ture is equivalent to a three port network shown in Figure 3.9(b). Port 1 is the common input, port 2 the complementary bandstop port, port 3 is the bandpass port and port 4 is open circuited. The three port network satisfies the necessary conditions for the common input terminal. The unit element $Z_0 = 1$ has not been moved beyond the junction. The coupled line structure also adds a degree of freedom in the design by creating a transformer to change impedance levels in the bandpass filter branch where the turns ratio n can be equated to the even and odd mode impedance of the coupled line. Design equations for a coupled line complementary diplexer are summarized next.

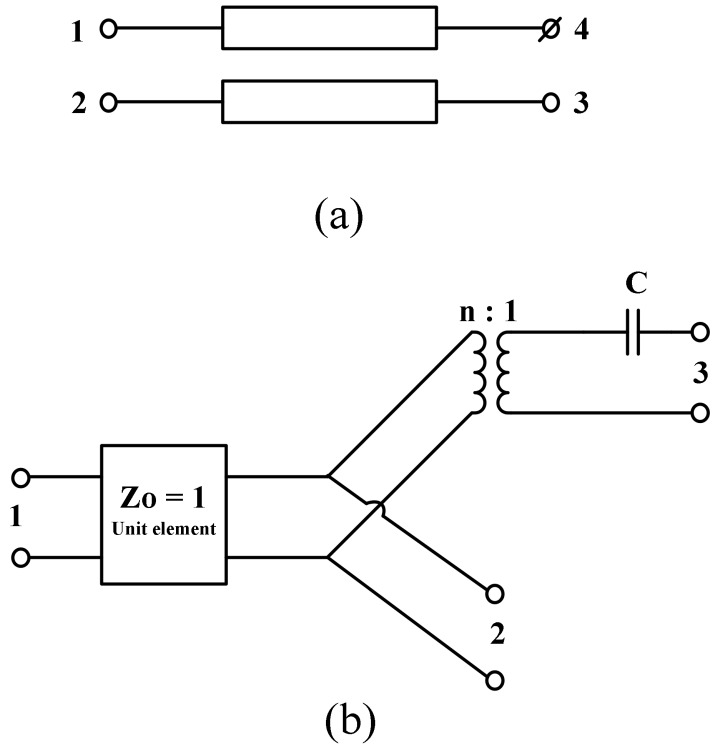

Figure 3.9: Parallel connection for bandpass/bandstop complementary diplexer (a) Physical realization (b) Equivalent circuit.

The transfer function for a complementary diplexer satisfies the following equation [17]

$$|Y_{12}|^2 = \frac{1}{1 + |\rho|^2/|t|^2} \tag{3.18}$$

where ρ is the input reflection coefficient and t is the transmission coefficient. For a Butterworth filter, the attenuation characteristic of the corresponding functions for $|\rho|^2/|t|^2$ are

$$\text{HP:} \quad \frac{|\rho|^2}{|t|^2} = \left(\frac{S_c}{S}\right)^{2M} \left(\sqrt{\frac{1 - S_c^2}{1 - S^2}}\right)^{2N} \tag{3.19}$$

$$\text{LP:} \quad \frac{|\rho|^2}{|t|^2} = \left(\frac{S_c}{S}\right)^{2M} \left(\frac{S}{S_c}\sqrt{\frac{1 - S_c^2}{1 - S^2}}\right)^{2N} \tag{3.20}$$

where HP denotes highpass and LP denotes lowpass. In these equations, S is a complex frequency variable that is given by Richard's transformation

$$S = j \tan\theta \tag{3.21}$$

where θ is a normalized frequency that depends on the physical length of the transmission line. The complex frequency S_c corresponds to the cut-off frequency of the lowpass/highpass filters. The variable M corresponds to the number of LC element pairs in the lowpass prototype, and N is the number of redundant unit elements Z_o introduced into the transformation of the design from lumped elements to distributed elements using Kuroda's transformations. So, for a two-section ($n = 2$) filter pair, the number of LC element pairs in the lowpass filter is $M = 1$ and the number of unit elements added to the transformation is $(n - 1) = N = 1$. Substituting these values into equations (3.18) and (3.19), the transfer function of the highpass filter

section is

$$\begin{aligned} |Y_{12}|^2_{HP} &= \frac{1}{1+\left(\frac{S_c}{S}\right)^2\left(\frac{1-S_c^2}{1-S^2}\right)} \\ &= \frac{-S^2(1-S^2)}{-S^2(1-S^2)+k^2} \end{aligned} \tag{3.22}$$

where

$$k^2 = -S_c^2(1-S_c^2) = \tan^2\theta_c \sec^2\theta_c. \tag{3.23}$$

The next step is to find the transfer admittance function, Y_{12HP}. It can be obtained from equation (3.22) by factoring the denominator and re-arranging the left half plane poles. Thus,

$$\begin{aligned} |Y_{12}|^2_{HP} &= Y_{12}(S)Y_{12}(-S) \\ &= \left[\frac{S\sqrt{(1-S^2)}}{S^2+\sqrt{(1+2k)}S+k}\right]\left[\frac{-S\sqrt{(1-S^2)}}{S^2-\sqrt{(1+2k)}S+k}\right]. \end{aligned} \tag{3.24}$$

Then, by applying the Brune-Gewertz procedure [18], we can get $Y_{in_{HP}}$ from $Y_{12_{HP}}$ as

$$Y_{in_{HP}} = \frac{S^2+\frac{1+k}{\sqrt{1+2k}}S}{S^2+(\sqrt{1+2k})S+k}. \tag{3.25}$$

Here, the network has one LC element pair in the lowpass prototype and one unit element is added in the transformation from lumped elements to distributed elements. So, the network can be synthesized by one application of Richard's theorem. The effect of adding a redundant unit element can be removed using a simple pole removal procedure given in [17] which leads to a more efficient distributed structure without redundant unit elements. The

synthesized non-redundant network is shown in Figure 3.10(a) where

$$C_o = \frac{1+k}{k\sqrt{1+2k}} \tag{3.26}$$

$$Z = \frac{\sqrt{1+2k}}{1+k} \tag{3.27}$$

$$R = \frac{1+2k}{(1+k)^2} \tag{3.28}$$

Note that in the non-redundant network form the terminal impedance is R and not unity.

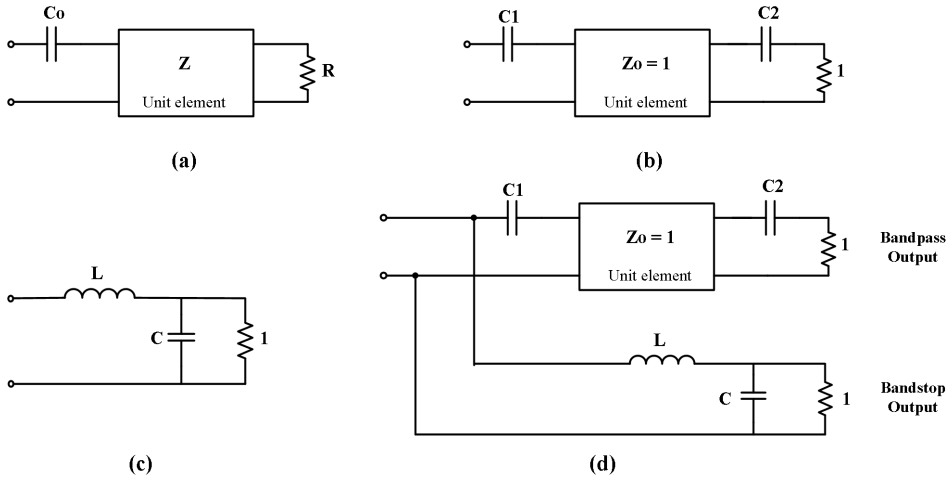

Figure 3.10: (a) Equivalent circuit for a non-redundant singly terminated bandpass filter section. (b) Bandpass filter with the addition of a redundant unit element to restore the terminal impedance to unity. (c) Singly terminated lumped element lowpass (distributed element bandstop) filter. (d) Equivalent circuit of the final diplexer with no redundant unit elements.

It is clear from equation (3.28) that in a non-redundant form the load resistance for the parallel coupled filter would no longer be unity. Unity impedance can be restored by adding a redundant capacitor and then using Kuroda's identity [12] to transform back to unity load impedance. This step

is shown in Figure 3.10(b).

Substituting the value of $Y_{in_{HP}}$ from equation (3.24) into (3.4), we can get an expression for the complementary lowpass filter from the highpass filter function. Therefore:

$$Y_{in_{LP}} = 1 - Y_{in_{HP}} = \frac{\frac{k}{\sqrt{(1+2k)}S+k}}{S^2 + \sqrt{(1+2k)}S + k}. \tag{3.29}$$

As $|Y_{12LP}|^2$ has all its zeros at $S = j\infty$, the corresponding network is a two-section LC ladder which can be synthesized by two pole removals [17] and the synthesized lowpass configuration is shown in Figure 3.10(c) where

$$L = \frac{\sqrt{1+2k}}{k} \tag{3.30}$$

$$C = \frac{1}{\sqrt{1+2k}}. \tag{3.31}$$

The lowpass section can be combined with the highpass section to form a complementary diplexer with the equivalent circuit shown in Figure 3.10(d). Figure 3.11 shows the final practical equivalent circuit diagram with redundant unit elements and two ideal transformers with arbitrary turns ratio of n.

A disadvantage of the final equivalent circuit in Figure 3.11 is that the turns ratio n requires coupled line structures with unequal widths. An implementation with equal strip widths is preferred and additional transformations are applied to achieve this goal. The procedure is again based on Wenzel's work where he defines an elastance matrix, a matrix composed of the inverse of coupled line capacitances. The elastance matrix can be scaled to maintain the terminal impedances while equalizing internal filter impedances so equal width parallel coupled lines can be implemented. The

reader is referred to Wenzel's paper [16] for details and a summary of the scaling procedure is given in Appendix A.

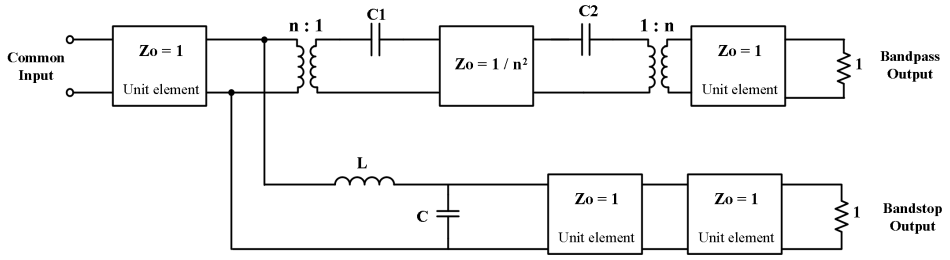

Figure 3.11: Practical diplexer equivalent circuit.

A two-section diplexer with a center frequency of 1 GHz and a relative bandwidth of 5.75% is designed. The design is shown in Figure 3.12. Each unit element has an electrical length of $\theta_c = 87.1$ degrees, very close to a quarter wavelength. Convenient dimensions for equal width strips were obtained for bandpass filter sections using elastance matrix scaling techniques with $n_2 = 0.248$ and $n_3 = 0.3446$. Kuroda's identity can then be used to obtain the redundant bandstop configuration shown in Figure 3.12(b). The final S-plane equivalent circuits for both the bandpass and bandstop filters are shown in Figure 3.12(c).

The corresponding physical realization of the bandpass [14] and bandstop filters with coupled line sections are obtained using the technique shown in Figure 3.13. Coupled lines with equal strip widths are used for both filters. The width of the strips and the gap spacing are calculated from the even and odd mode impedances of the coupled line. The impedances are related to the equivalent circuit values for L and C shown in Figure 3.12 using the

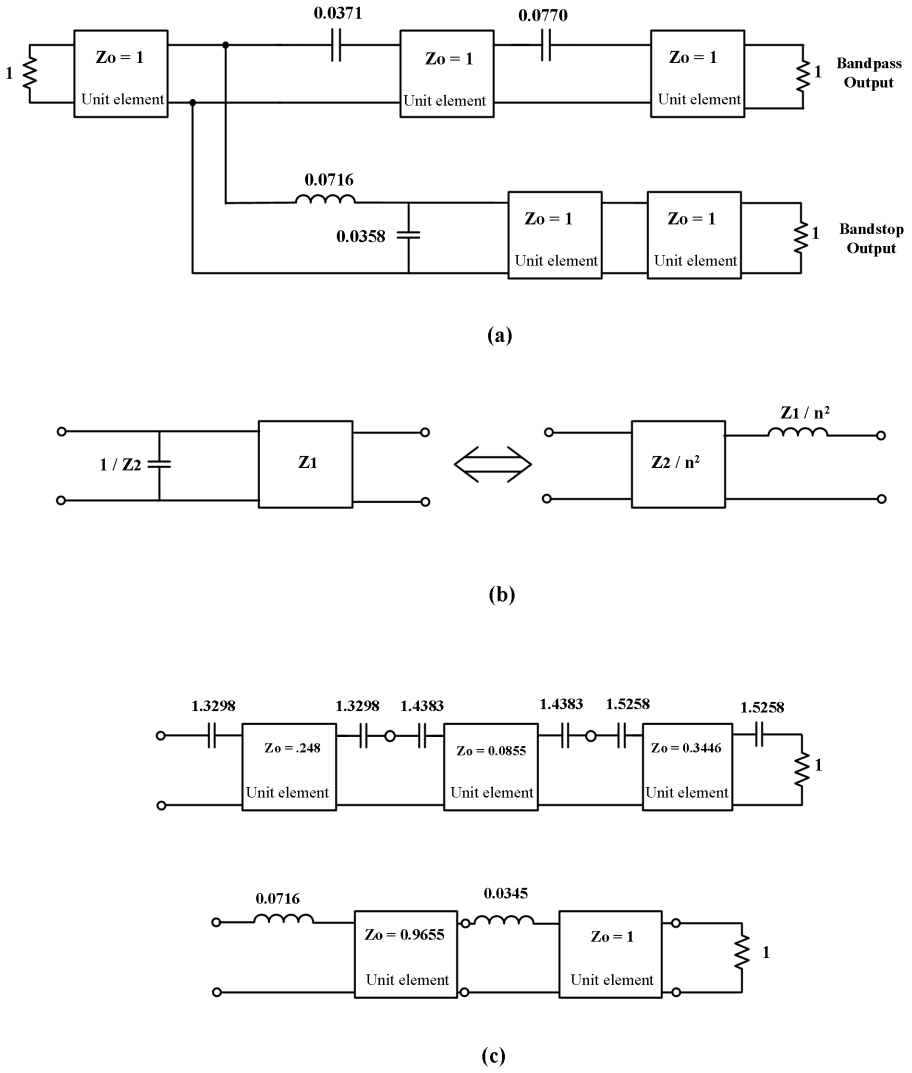

Figure 3.12: Design of a two-section complementary diplexer for a center frequency of 1 GHz and 5.75% bandwidth. (a) Equivalent circuit for a two-section diplexer. (b) One of the Kuroda's identity. (c) S- plane equivalent circuit filter branches.

following equations:

$$Z_{0o(bandpass)} = \frac{1}{C} \tag{3.32}$$

$$Z_{0e(bandpass)} = 2(Z_0 + \frac{1}{C}) - Z_{0o(bandpass)}. \tag{3.33}$$

$$Z_{0o(bandstop)} = L + Z_0 - \sqrt{(L + Z_0 + Z_a)L} \quad (3.34)$$

$$Z_{0e(bandstop)} = L + Z_0 + \sqrt{(L + Z_0 + Z_a)L} \quad (3.35)$$

$$Z_a < \frac{Z_0(Z_0 + L)}{L}. \quad (3.36)$$

The physical realization of the bandstop filter contains one more parameter, Z_a, and this is a free parameter in the design. Convenient dimensions of Z_a can be determined to facilitate the implementation using a quarter wave transmission line. Note that each bandstop resonator can be tuned over a 5 to 10 percent frequency range by changing the length of this quarter wave transmission line. This allows simple alignment of the diplexing filter. Figure 3.13(c) shows the complete physical realization of the stripline bandpass/bandstop complementary diplexer.

A photograph of the prototyped stripline bandpass/bandstop diplexer is shown in Figure 3.14. The even and odd mode impedances for each coupled line section as well as the physical dimensions of the traces are tabulated in Table 3.2 and Table 3.3, respectively. The diplexer was fabricated on a Rogers R4350 1.5 mil substrate and the substrate parameters are given in Table 3.4.

The design was simulated in ADS. First a schematic with distributed transmission line models was used to verify the initial design, then the design was optimized in Agilent's electromagnetic simulator called Momentum. The simulation results for both the schematic and electromagnetic models are shown in Figure 3.15 and Figure 3.16 respectively. Both simulation models are in close agreement with each other which shows that the distributed transmission line models in the schematic are accurate.

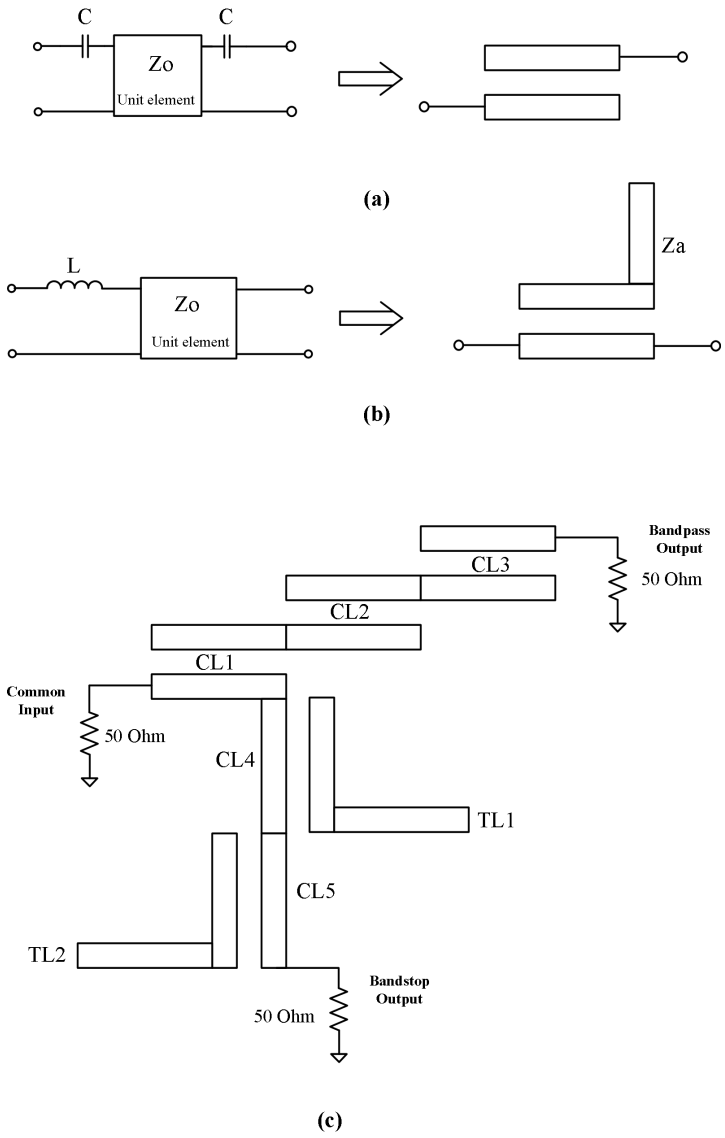

Figure 3.13: (a) Bandpass section equivalent circuit for equal strip width coupled lines. (b)Bandstop section equivalent circuit for equal strip width coupled lines. (c) Complete physical realization of the stripline complementary diplexer (not drawn to scale).

Measurement results for the diplexer are shown in Figure 3.17. The experimental results deviate from the simulated results primarily in terms of the insertion loss and return loss of the bandpass filter. The difference was tracked down to a fabrication fault where the traces on the board were over etched by 2 mil. As shown in Table 3.3, the coupling gap for CL3 is 7 mil and the gap for CL1 is 15.4 mil. An over etch of 2 mils is a significant error especially for narrow gap spacing and this increased the insertion loss of the filter. The impact of over etching the board was verified by re-simulating the design in Momentum with a 2 mil etching error. The results are shown in Figure 3.18 and confirm the increase in insertion loss. A different board vendor is recommended for future spins of the diplexer design. A summary of modeled and measured results for the complementary diplexer is given in Table 3.5.

Table 3.2: Complementary Diplexer design parameters (even and odd mode impedances).

Filter Type	Coupled Line	Even Mode (Ω)	Odd Mode (Ω)
Bandpass	CL1	62.4	37.60
	CL2	43.31	34.76
	CL3	67.23	32.77
Bandstop	CL4	70.96	32.75
	CL5	64.98	38.47

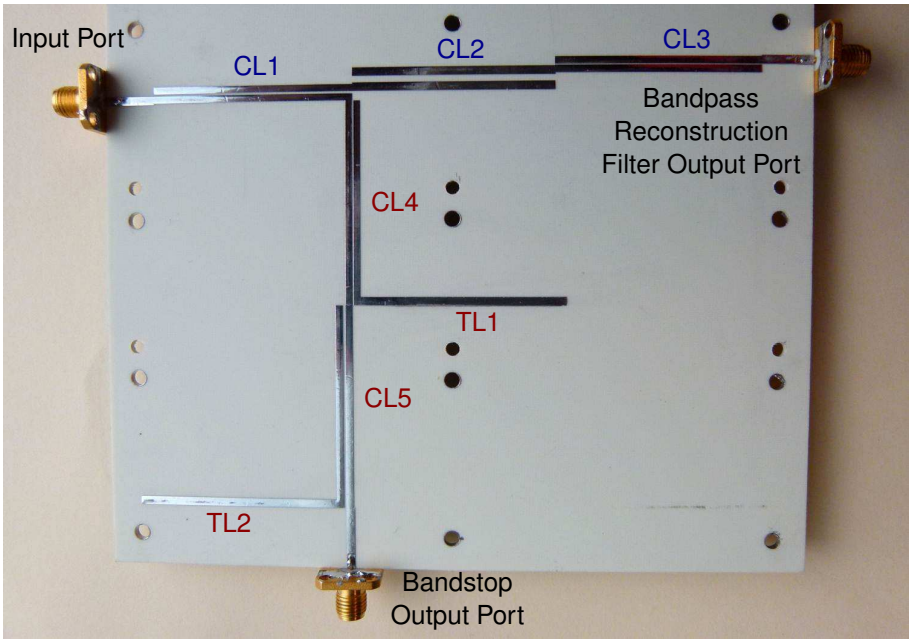

Figure 3.14: Photograph of the stripline complementary diplexer.

Table 3.3: Diplexer design parameters (physical dimensions).

Filter Type	Coupled Line	Length (mil)	Width (mil)	Gap (mil)
Bandpass	CL1	1571.8	55.9	15.4
	CL2	1559.8	67.3	48.4
	CL3	1571.8	58.6	7.0
Bandstop	CL4	1585.1	55.1	7.1
	CL5	1598.8	58.6	16.7
	TL1	1590.1	65.8	-
	TL2	1590.1	65.8	-

Table 3.4: Substrate process parameters.

Parameters	Values
Substrate Thickness	60 mil
Dielectric Constant, ε_r	3.48
Dissipation Factor, δ	0.0031
Copper Thickness	1.4 mil

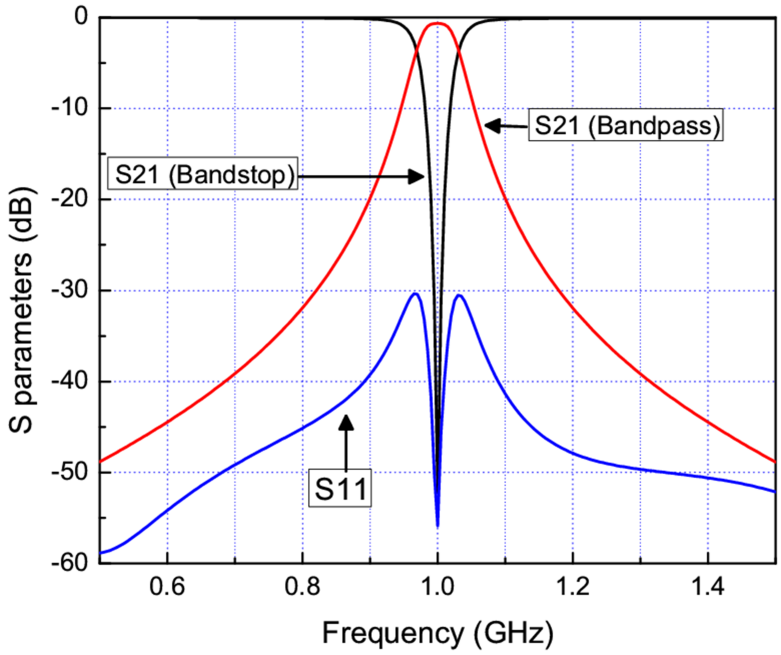

Figure 3.15: Simulated results for the complementary diplexer using schematic models.

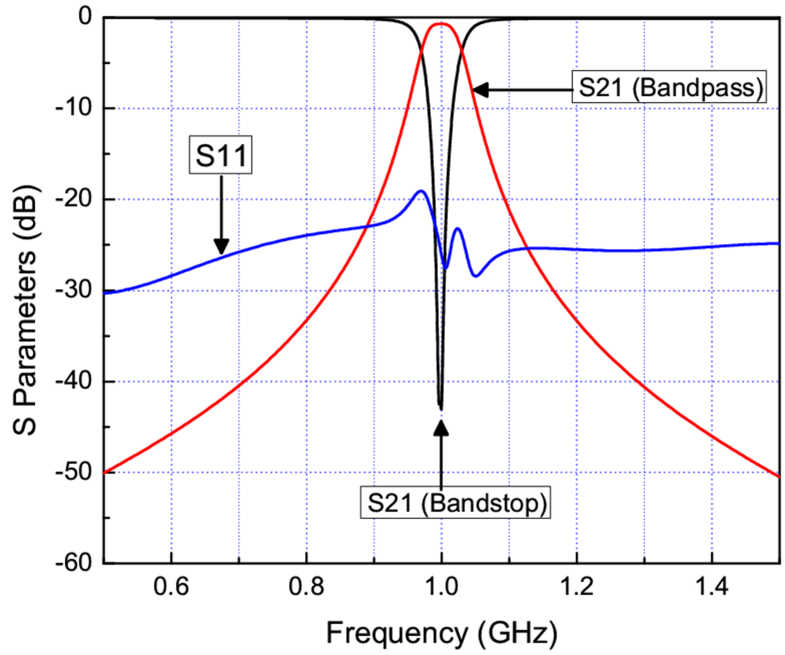

Figure 3.16: Simulated results for the complementary diplexer using an electromagnetic simulator (Momentum).

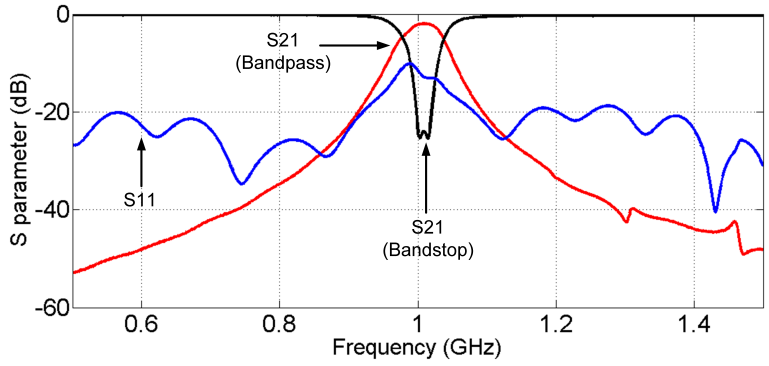

Figure 3.17: Measured results for the complementary diplexer.

Table 3.5: Summary of simulation and measured results for the complementary diplexer.

Parameters	Schematic	Momentum	Experiment	Momentum (with 2 mil over etch)
Center frequency (MHz)	1000	1003	1010	1004
Relative -3 dB Bandwidth (MHz)	57.5	60	65	61
Insertion loss (dB)	-0.653	-0.702	-2.1	-1.0
Maximum Return loss (dB)	-30.3	-19.1	-10.0	-15.0

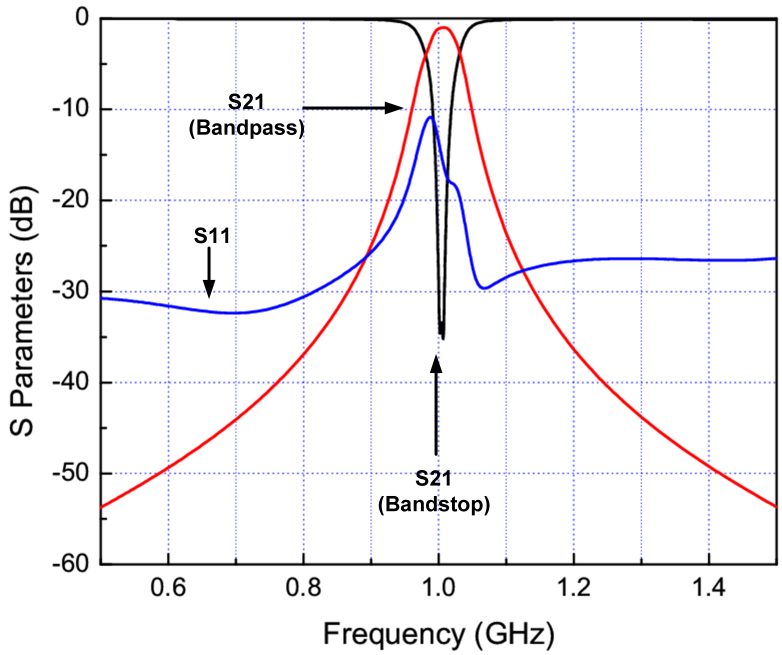

Figure 3.18: Simulated results for the complementary diplexer using Momentum and assuming a 2 mil over etch.

Chapter 4

Results

In chapters 2 and 3, the design of the power amplifier switching circuit and the output diplexer were described. In this chapter, simulation and experimental results for these design are presented.

The chapter begins with a description of the source signals which are used for evaluating the the SMPA designs. In the remaining sections of the chapter, experimental results are shown for each of the three power amplifier designs using different source signal waveforms. Finally, a concluding section presents a comparison of the different designs and summarizes the conclusions from experimental measurements.

4.1 Input Signal Types

Before going to the main results, the types of source signals used to evaluate the SMPA performance are described. Three types of source signals were used for measurements:

- a sinusoidal or continuous wave (CW) signal for 50% duty cycle tests;
- periodic pulse trains with 25%, 50% and 75% duty cycles generated by a Xilinx Vertex-II FPGA (field programmable gate array) development board;

- pseudo-random (non-periodic) bit patterns generated by a Centellax TG1B1-A 10 G PRBS test pattern generator.

4.1.1 Periodic 50% Duty Cycle Test Signal

A 50% duty cycle periodic test signal is generated by applying a sinusoidal input signal to the driver input. The driver has 35 dB of gain and a 0 dBm sinusoidal input signal is clipped to a square wave output signal. Examples of the sinusoidal source signal and the driver output signal for a frequency of 1 GHz are shown in Figures 4.1 and 4.2.

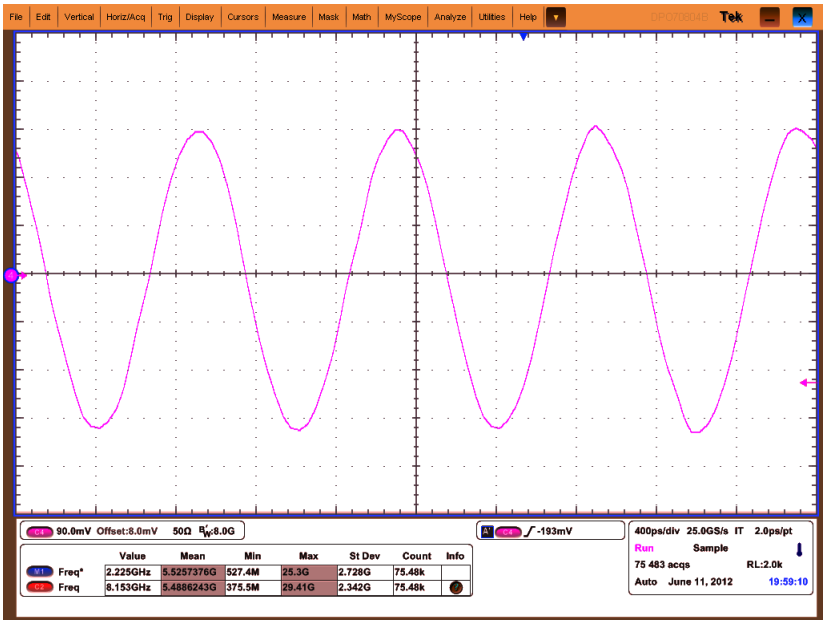

Figure 4.1: A 0 dBm 1 GHz sinusoidal source signal measured with a high speed oscilloscope.

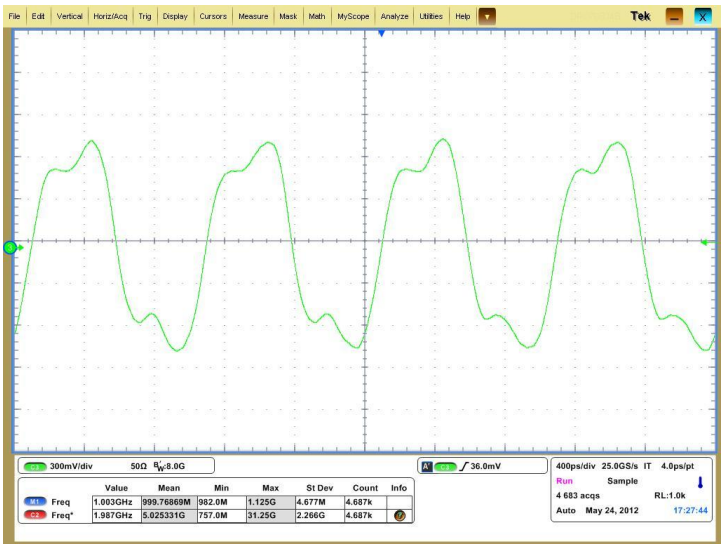

Figure 4.2: Measured driver response for a 1 GHz CW input signal across a 50 Ω load.

4.1.2 Periodic Test Signals with Variable Duty Cycle

Variable duty cycle pulse trains were synthesized using a Xilinx XUP Virtex-II development system. Standard code is available for this platform to read a 40 bit pattern from memory out a Rocket I/O port which is clocked at 1.5 GHz. Since each bit is clocked at 1.5 GHz, a periodic 40 bit sequence generated would be much too low in frequency to evaluate the SMPA designs. The low frequency response of the SMPA is limited by the bandwidth of the drain bias circuit, and for the designs described in Chapter 2, frequencies above 200 MHz are useful. Therefore, the Xilinx platform was configured to output a four bit pattern which was used to synthesize 25%, 50%, and 75% pulse trains at a frequency of 375 MHz. An eight bit sequence generating an alternating 25% then 75% duty cycle pattern was also generated. The purpose of this waveform is to have a

varying duty cycle that is more representative of non-periodic pulse trains. Measured waveforms at the output of the Xilinx development board are shown in Figure 4.3 to Figure 4.6.

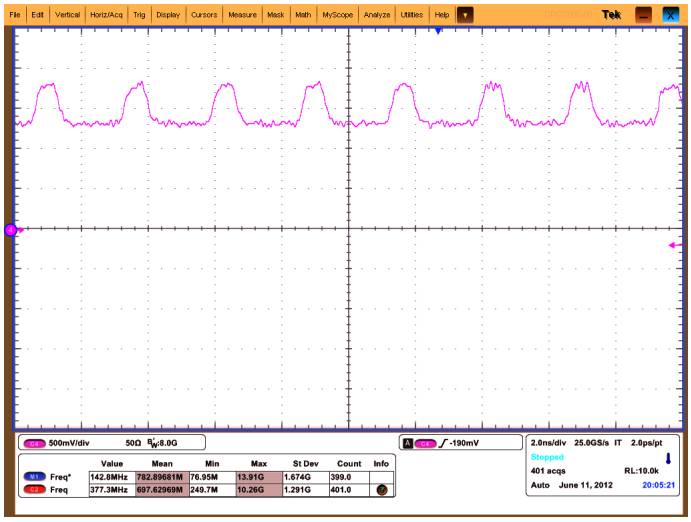

Figure 4.3: Periodic pulse train with a 25% duty cycle at a frequency of 375 MHz.

4.1.3 Pseudo-random (Non-periodic) Test Signals

Given that one of the primary goals of this research was to improve the power efficiency of SMPAs under non-periodic switching conditions, it was important to make measurements with non-periodic signals. Unfortunately, a high speed arbitrary waveform generator was not available to enable testing with encoded pulse trains using sigma-delta modulation or pulse position modulation. However, a high speed pseudo-random bit sequence (PRBS) pattern generator was available and measurements were made using this waveform. The PRBS generator was a Centellax TG1B1-A 10 G bit error rate test (BERT) set which could generate data at rates from 0.5 to

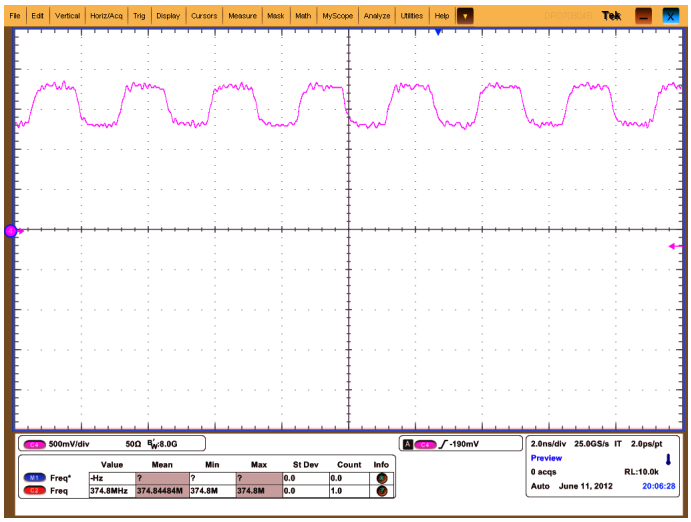

Figure 4.4: Periodic pulse train with a 50% duty cycle at a frequency of 375 MHz.

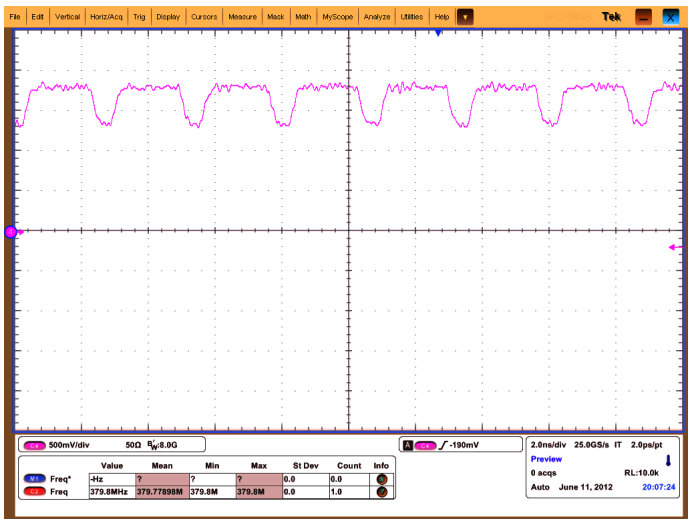

Figure 4.5: Periodic pulse train with a 75% duty cycle at a frequency of 375 MHz.

12.5 Gb/s. Patterns with sequence lengths of 2^7 bits to 2^{32} bits could be generated. A 1 Gb/s was close the the highest frequency that the driver

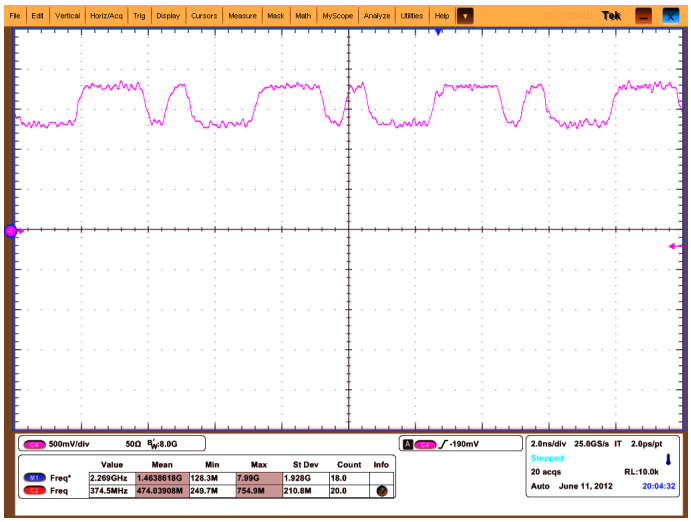

Figure 4.6: Periodic pulse train with a combination of 25% and 75% duty cycle at a frequency of 375 MHz.

could amplify in the SMPA.

A significant limitation of using PRBS patterns is that the spectral power is concentrated at low frequencies and was not matched with the bandwidth of the drain bias circuit in the SMPA. As shown in Chapter 2, the drain bias circuit had a low frequency bandwidth around 200 MHz, while the PRBS has spectral power down to DC as shown by the spectrum analyzer plot in Figure 4.8. PRBS patterns are baseband pulses and used in data communication applications while the SMPA has a bandpass response with low frequency limits created by DC coupling capacitors and the drain bias circuit. As shown in Figure 4.8, the power spectrum has a $\sin(x)/x$ envelope created by the square pulses. Clearly the energy in the low frequency range below 200 MHz is reduced as the clock rate of the PRBS pattern is increased and testing with different clock rates were made. Despite the low frequency limitation of the PRBS signal, it provides useful insight into the operation

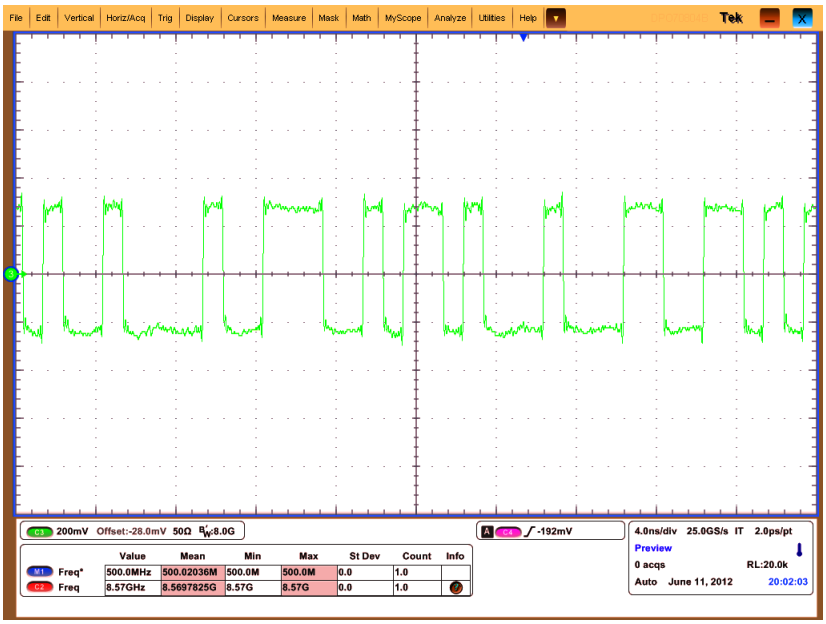

Figure 4.7: A pseudo-random bit sequence (PRBS) generated by a Centallax TG1B1-A 10G bit error rate test unit. The clock frequency is 1 GHz.

of the SMPA and test results are presented for each of the SMPA designs.

4.2 Results for Design 1

4.2.1 SMPA performance with a 50% duty cycle periodic test signal

Design 1 is first characterized using a sinusoidal source signal. As described earlier, the driver clips the sine wave and generates a square wave gate drive signal. The gate signal switches the power device in the SMPA and the current and voltage waveforms across the switch are expected to follow the gate drive signal. An example of the output waveform measured at node C (see Fig.1.9, page 18) is shown in Figure 4.9. The measurement

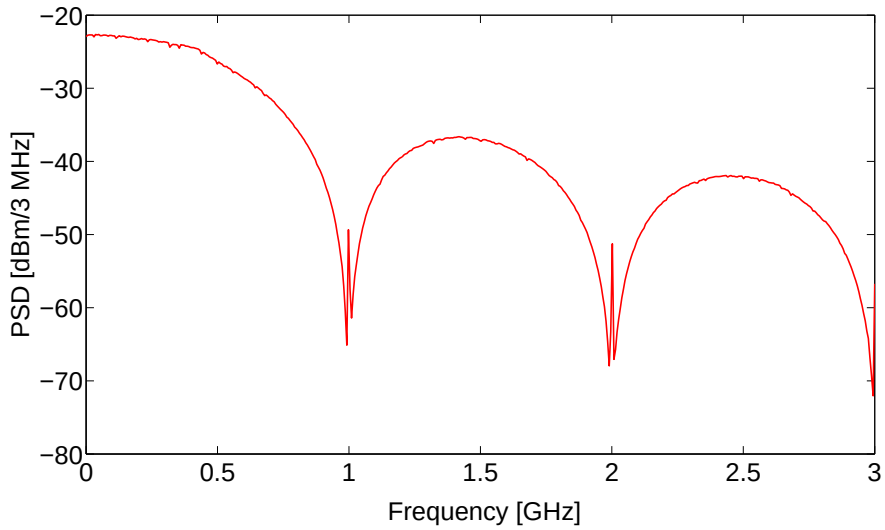

Figure 4.8: Measured power spectral density (PDS) of the PRBS generator at 1 GHz frequency.

is made by connecting a 40 dB power attenuator in series with the SMPA output at node C and then connecting the output signal to a high speed oscilloscope, Tektronix model DP070804B. The measured waveform shows a switched periodic signal with good bandwidth at a switching frequency of 1 GHz. For comparison, simulated results are shown in Figure 4.10 for a drain supply voltage of 25 V, the same supply voltage for the measured waveform shown in Figure 4.9.

Power efficiency is the primary metric which is used to evaluate the performance of the SMPA. A commonly reported efficiency is called drain efficiency which is defined as the ratio of the output load power over the total drain supply power. Drain efficiency is given by

$$\eta = \frac{P_{out}}{P_{in}}. \ 100\% \tag{4.1}$$

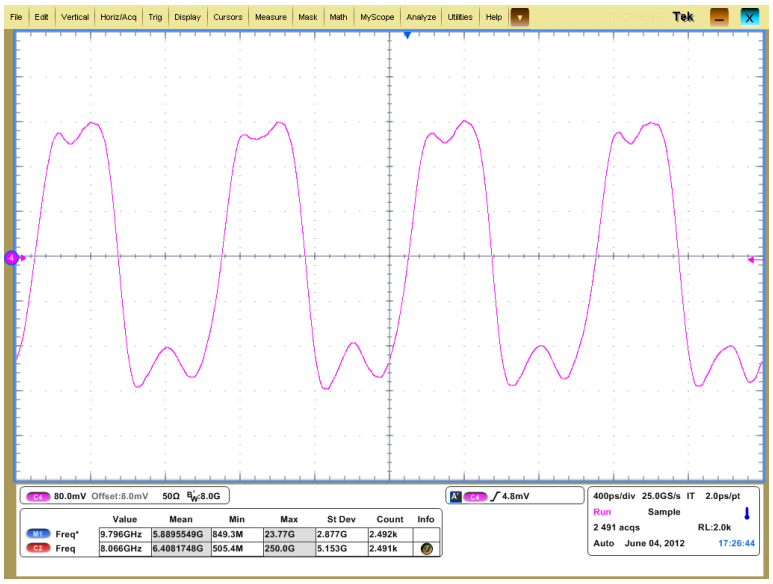

Figure 4.9: Measured output voltage waveform at node C in Design 1 for a 1 GHz CW input signal. The drain voltage is 25 V.

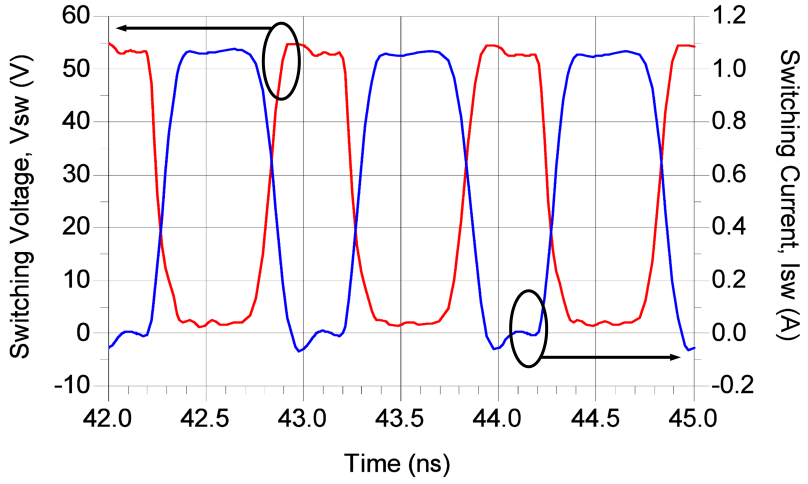

Figure 4.10: Simulated switching voltage and current waveforms at node B for a 1 GHz CW input signal.

where

$$P_{in} = V_{DD} I_{DC} \tag{4.2}$$

and

$$P_{out} = \frac{V_L I_L}{2}. \tag{4.3}$$

In these equations V_{DD} is the drain bias voltage, I_{DC} is the drain bias current, V_L is the peak load voltage, and I_L is the peak load current. For the measurement shown in Figure 4.9, the load power at node C is 10.4 W and the drain supply power is 15.5 W. Therefore, 3.9 W is dissipated in the switch and the drain efficiency is approximately 67%.

Since there is no amplitude control in a SMPA other than changing duty cycle or using encoded pulse trains, the output power is related to the drain supply voltage. As a way to effect a change in load power with a 50% duty cycle test signal, the drain supply voltage is varied. This method is used in all the results shown because encoded test signals were not available for experimental work. Later, in chapter 5, simulation results are presented using the SMPA model to show examples of the performance using encoded pulse trains.

A comparison of measured and simulated results of drain efficiency versus drain supply voltage at a frequency of 1 GHz is shown in Figure 4.11. For these results, load power was measured using a Gigatronics 8541 power meter with a broadband true RMS power head, model 80330A, connected to the output of the SMPA at node C through a 40 dB power attenuator. The simulated drain efficiency curve is quite flat over the entire drain voltage range while the experimental drain efficiency curve starts to drop at high output power. The main reason for the deviation between the simulated and experimental results at high power is because the dissipation in the DC

blocking capacitor (C_s) starts to become significant. Power loss is evident and the capacitor gets warm at high output power. Very high Q capacitors could reduce dissipative losses at high power. Simulated and measured results are similar and the average efficiency is approximately 65%.

The same drain efficiency data shown in Figure 4.11 as a function of load power is shown in Figure 4.12. Measurements of drain efficiency versus output power are much more useful for comparison with other power amplifier circuits. As shown in Figure 4.12, power efficiency is relatively constant up to a power of 40 dBm (10 W) which is the rated power of the device as given by the Cree. Above 40 dBm, power efficiency drops as the device is driven deep into compression.

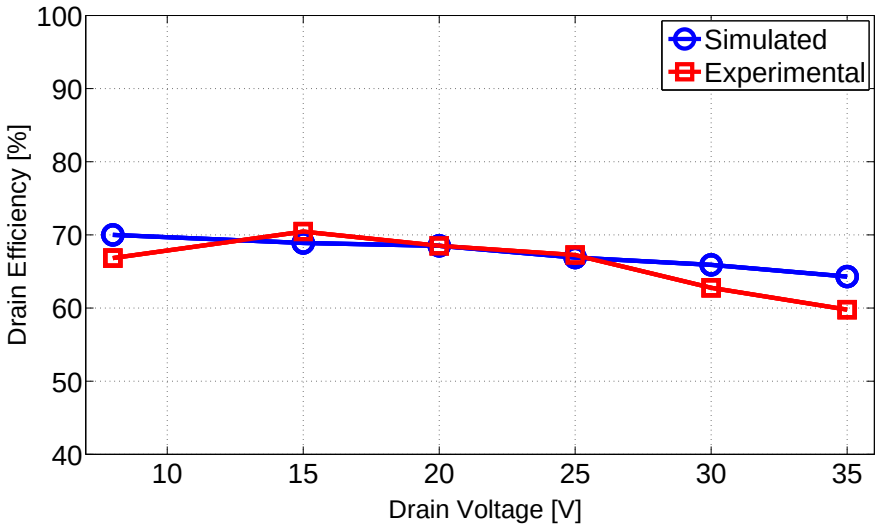

Figure 4.11: Drain efficiency versus drain voltage for a CW source signal at 1 GHz. Measured and simulated data are shown.

Next, the drain efficiency for different frequencies are compared over a frequency range from 375 MHz to 1.1 GHz. Frequency in the context of these measurements refers to the fundamental frequency of a periodic square

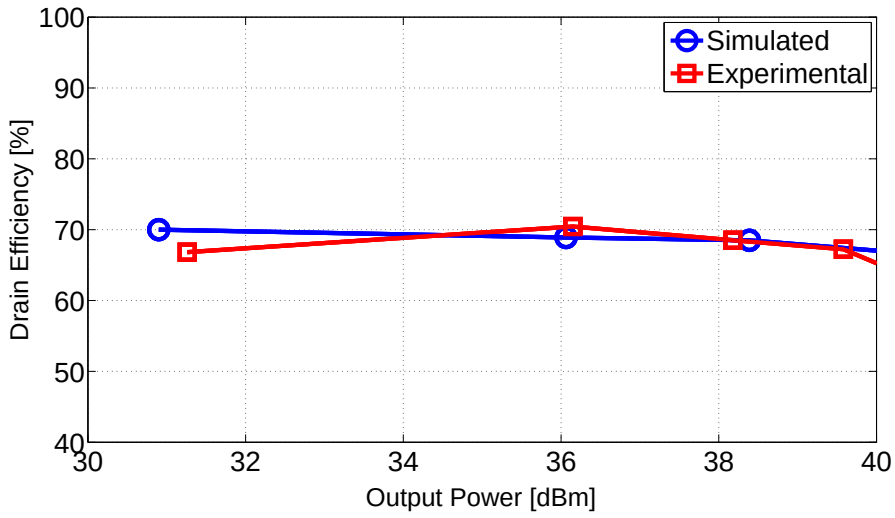

Figure 4.12: Drain efficiency versus output power for a CW source signal at 1 GHz. Measured and simulated data are shown.

wave signal with a duty cycle of 50%. Figure 4.13 shows the measurement results for Design 1. The purpose of this test was to measure the power efficiency over a broad frequency range to evaluate the bandwidth of the driver. At 375 MHz, the average efficiency is approximately 75% while at 1.1 GHz the average efficiency is approximately 55%. For other frequency ranges between 375 MHz and 1.1 GHz, the power efficiency is in the range of 67%. The broad frequency range over which power efficiency is relatively constant is consistent with the broadband design methodology that was used for Design 1. Figure 4.14 shows the same drain efficiency measurements versus output power. Power efficiency is approximately 68% over a range of output power from 30 dBm to 40 dBm.

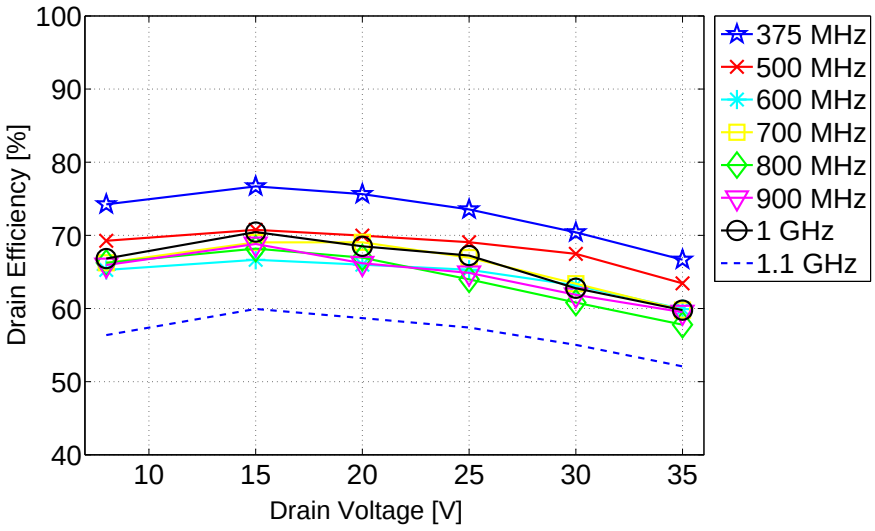

Figure 4.13: Comparison of the measured drain efficiency versus drain voltage for different CW frequencies.

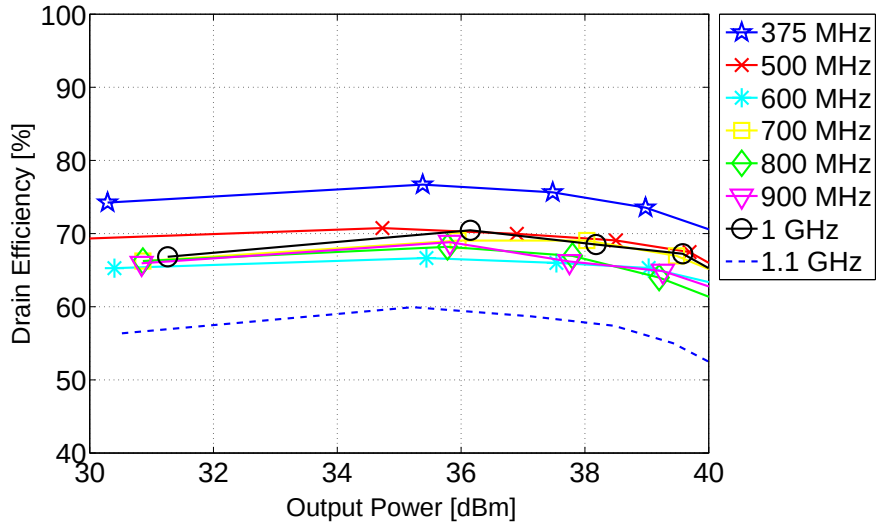

Figure 4.14: Comparison of the measured drain efficiency versus output power for different CW frequencies.

4.3 SMPA performance with periodic switching signals

The next experiments which are discussed use periodic pulse trains generated from the Xilinx FPGA development board described earlier in section 4.1.2. Measurement results are summarized in Figures 4.15 and 4.16.

In Figure 4.15, an example of the input waveform from the FPGA board is shown together with the output waveform measured at node C through a 40 dB power attenuator. The alternating 25/75% duty cycle test pattern is shown. Unlike the output signal at 1 GHz shown earlier in Figure 4.6, a low frequency wander (decrease in amplitude) is evident on the slopes of the long pulses. Since this signal pattern is generated by 8 bit sequences at a clock rate of 1.5 GHz, the period of the waveform is 187.5 MHz. The low frequency content in the signal is impacted by the low frequency response of the drain bias circuit and there is a noticeable shift in bias point over the duration of the pulse. A 'stiffer' broadband drain bias would reduce the wander; however, as long as the zero-crossings are not shifted too much, minimal distortion is expected. Clearly, the spectrum of the pulse train and the bandwidth of the bias network need to be matched; this is an area that is recommended for future research.

In Figure 4.16, a comparison of drain efficiency versus output power is shown for four different periodic pulse trains. The measured input and output waveforms for the 25/75% signal are shown in Fig. 4.15. Note that output power is changed by adjusting the drain supply voltage similar to the measurements made with a sinusoidal source. An important observation in this data set is that the characteristics for the 50% duty cycle square wave and the alternating 25/75% duty cycle square are nearly identical. Both

signals spend an equal amount of time in the on or off state, so conduction (IR) losses in the switch are approximately the same. Although switch timing is much more variable in the 25/75% signal, power efficiency is similar to a 50% duty cycle square wave. This result is expected and consistent with the design approach to implement a broadband match and desensitize power efficiency relative to changes in the pulse pattern. The measurements also clearly show that a 75% duty cycle signal results in lower power efficiency than a 25% duty cycle signal. In the former case, the switch is on for 75% of the time, while the switch is only on for 25% of the time in 25% duty cycle signal. Conduction losses in the power switch are reduced for a reduction in duty cycle and the measurements show that power efficiency is higher for a low duty cycle waveform.

4.4 SMPA performance with Pseudo-random bit sequences

Test results so far have been shown for Design 1 using periodic test patterns and results are now shown for random PRBS signals using the Centallax test set. As shown earlier in section 4.1.3, PRBS signals have significant low frequency energy that falls outside the bandwidth of the drain bias. The low frequency energy in the signal creates wander in the amplified pulse train at the drain of the power switch as shown in Figure 4.17. The measurement results are confirmed by simulation models as shown by the simulated output waveform shown in Figure 4.18. Similar to the experimental results, the low frequency wander is evident. To confirm that the bandwidth of the drain bias circuit causes the wander, a plot of the simulated gate signal is shown in Figure 4.19. The waveform has no baseline wander and the ringing

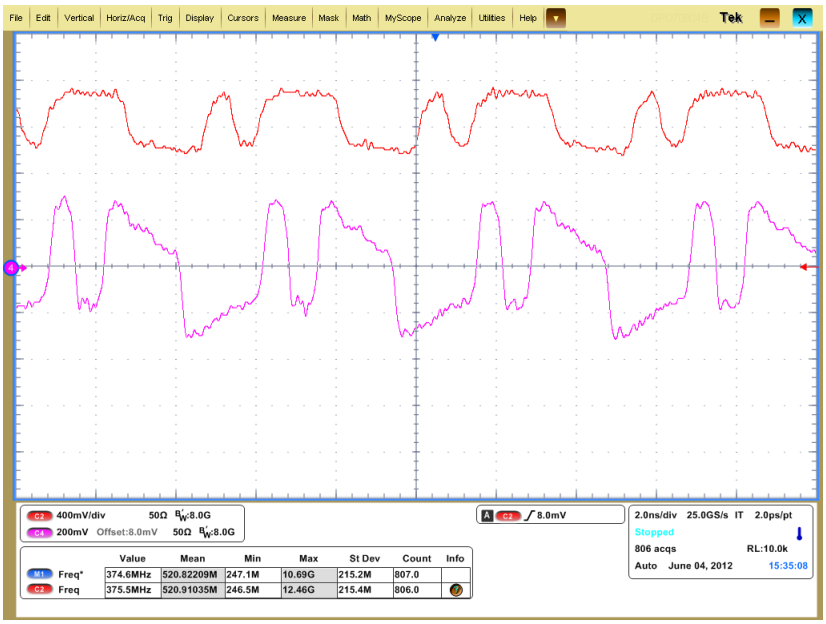

Figure 4.15: Measured waveforms for a 375 MHz input signal with alternating 25% and 75% duty cycle pulses. The top trace is the input signal from the FPGA board and the bottom signal is the output waveform at node C in the SMPA.

is caused by gate and lead inductance. A similar measurement of the gate signal is not available as it is very difficult to measure this waveform in the circuit.

Next, Figures 4.20 and Figure 4.21 show a comparison of simulated and experimental results for a 1 GHz PRBS signal. Over a broad range of drain supply voltages from 8 V to 35 V, drain efficiency is relatively constant in the range of 65%. A comparison of these results with Figure 4.11 for a sinusoidal source signal shows that power efficiency is similar. Design 1 has a broadband output match and therefore drain efficiency is expected to be relatively insensitive to the type of switching waveform.

Since the PRBS pattern has low frequency energy that falls outside the

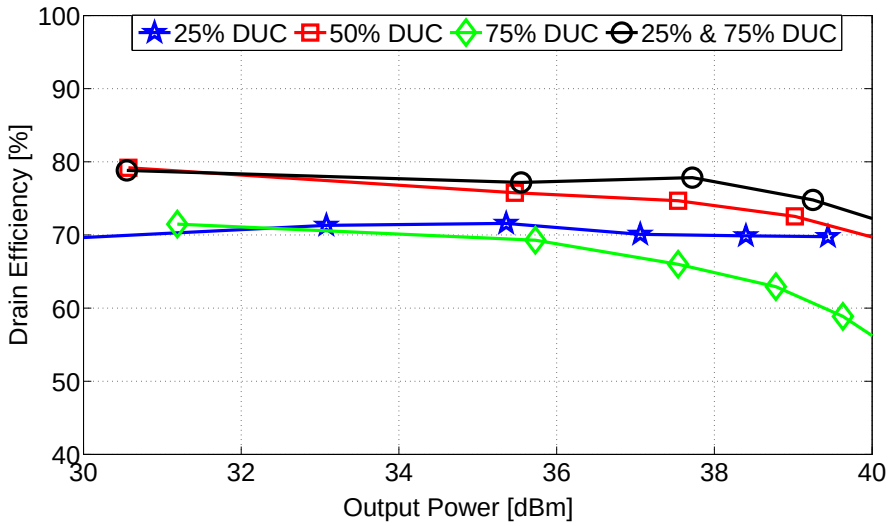

Figure 4.16: Drain efficiency versus output power at 375 MHz for different duty cycles (DUC means duty cycle).

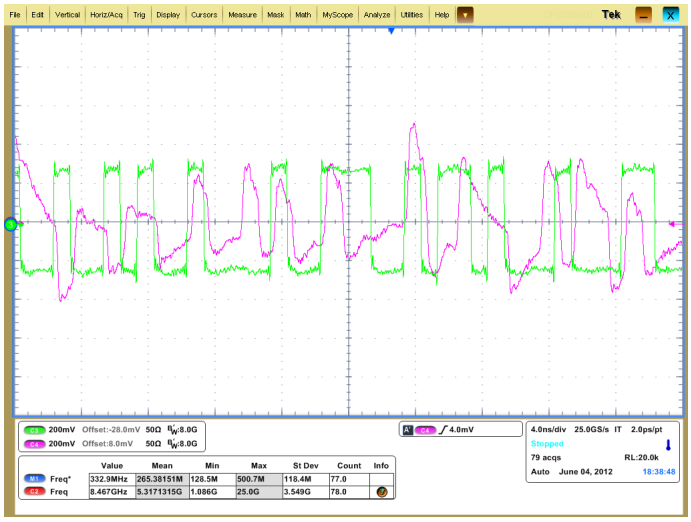

Figure 4.17: Measured output voltage waveform at node C for a 1 GHz PRBS input signal.

bandwidth of the drain bias circuit, it is expected that as the data rate is reduced, the drain efficiency will decrease. Measurements of drain efficiency

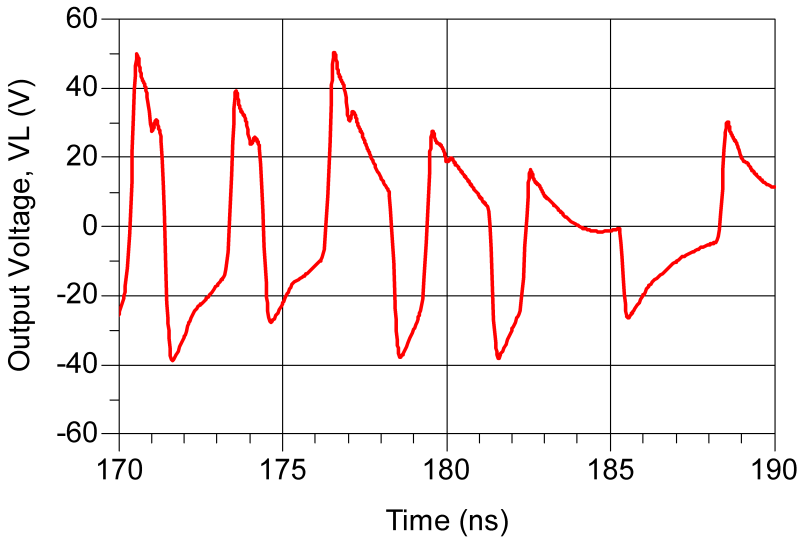

Figure 4.18: Simulated output voltage waveform at node C for a 1 GHz PRBS input signal.

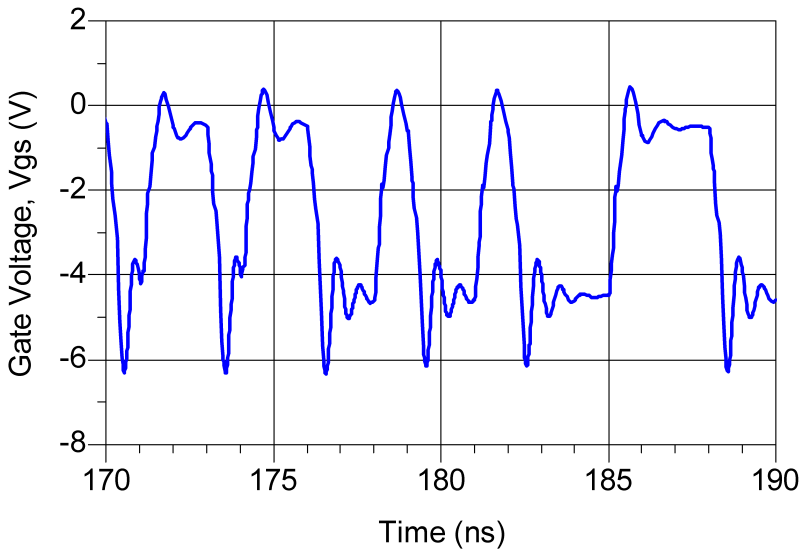

Figure 4.19: Simulated gate voltage waveform for a 1 GHz PRBS input signal.

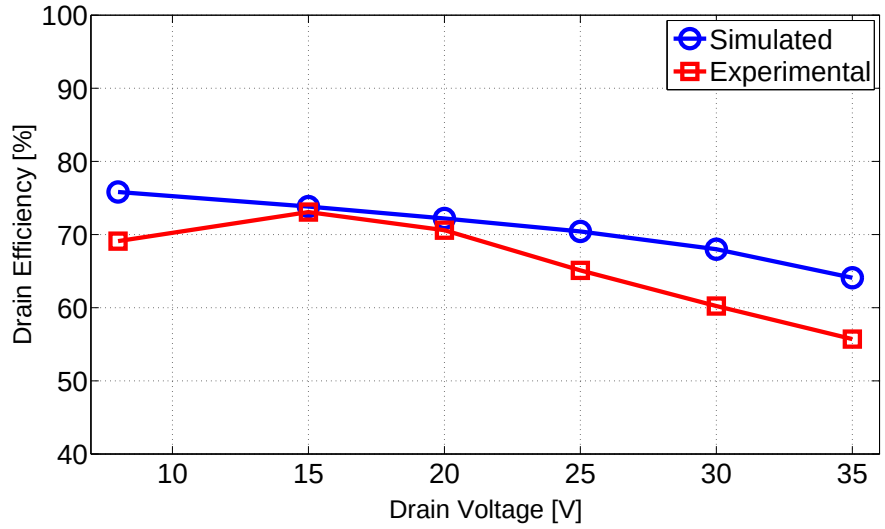

Figure 4.20: Drain efficiency versus drain voltage for a PRBS source signal at 1 GHz. Measured and simulated data are shown.

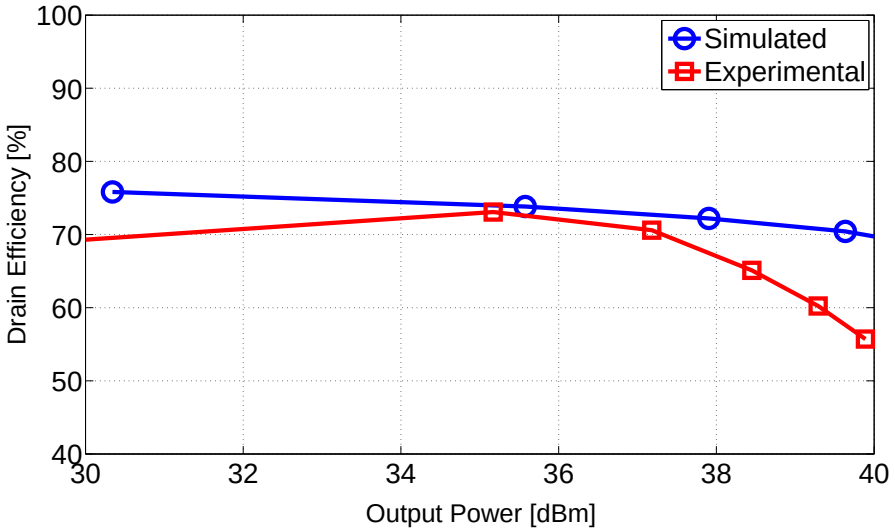

Figure 4.21: Drain efficiency versus output power for a PRBS source signal at 1 GHz. Measured and simulated data are shown.

for different data rates are shown in Figures 4.22 and 4.23. Both figures show that drain efficiency reduces as the data rate is reduced from 1 Gb/s to 375 Mb/s.

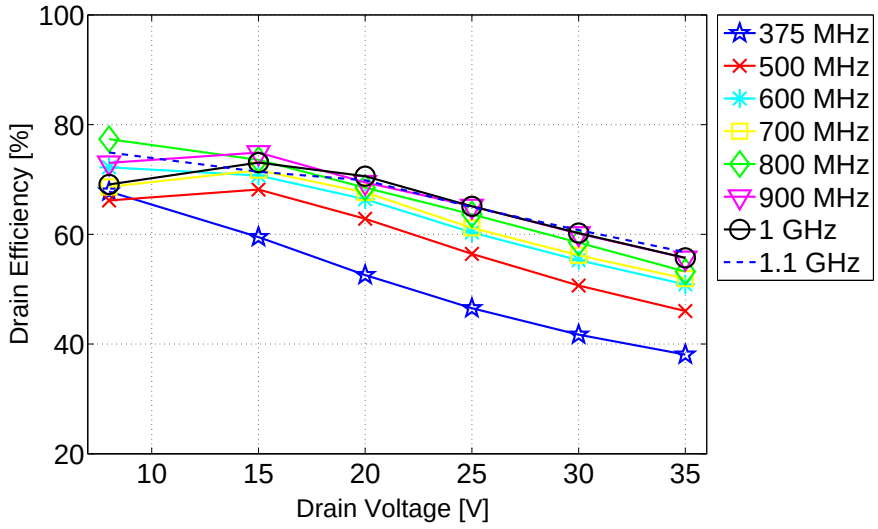

Figure 4.22: Measured drain efficiency versus drain voltage for different PRBS data rates.

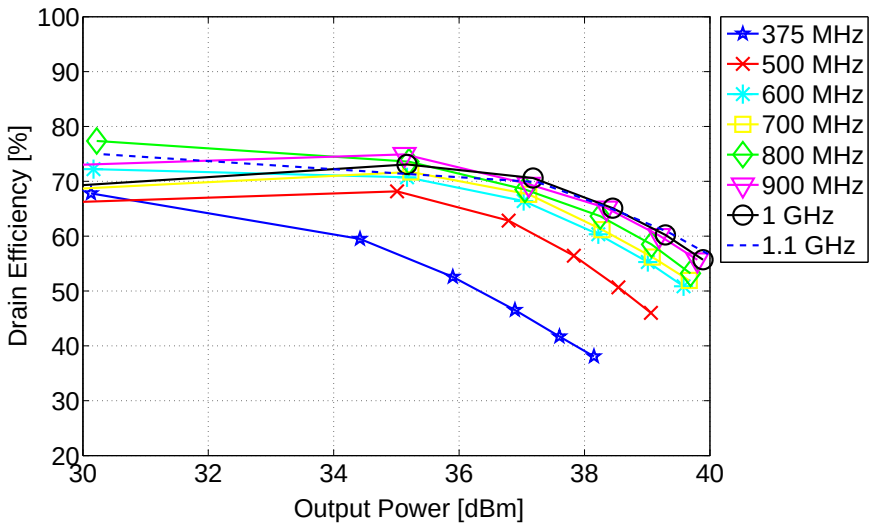

Figure 4.23: Measured drain efficiency versus output power for different PRBS data rates.

4.5 Results for Design 2

As described in chapter 2, Design 2 is a modification of Design 1 where the bias inductor L_{p1} is selected to resonant with the effective output capacitance of the device. The resonant output circuit decreases the bandwidth of the output stage of the SMPA. A comparison of the bandwidth between the different designs is shown in Figure 4.37 (see section 4.7.1) and the bandwidth of Design 2 is approximately 2.4 GHz compared to a bandwidth of 5.4 GHz for Design 1. The tuned output stage boosts drain efficiency for source signals with significant spectral energy within the bandwidth of the tuned output stage. Conversely, drain efficiency is reduced for source signals with spectral energy that falls outside the bandwidth of the output stage. Experimental results confirm these hypotheses and are discussed next.

4.5.1 SMPA performance with sinusoidal source signals

The tuned output stage in Design 2 limits the bandwidth of the load signal measured at node C. This is shown in Figure 4.24 and the waveform, ideally a 50% duty cycle pulse train, now has harmonic roll-off. However, the benefit of the tuned stage is shown by drain efficiency plots in Figures 4.25 and 4.26. Drain efficiency and output power peak at a frequency of 1 GHz which is where the tuned output stage was designed to resonate. A drain efficiency of 72% is measured at an output power of 10 W (40 dBm) which corresponds to a drain supply voltage of 31 V. Both figures also show that similar performance is measured at 900 MHz, and that further decreases in the source frequency reduce drain efficiency. Also, drain efficiency starts to decrease from a maximum at 1 GHz as the frequency is increased. The upper frequency limit is a combination of the bandwidth limitations in the driver as well as the tuned output stage. A comparison between simulated and measured results is shown in Figure 4.27 as a function of drain supply voltage. The simulation model and experimental results match quite well and validate the simulation model.

4.5.2 SMPA performance with Pseudo-random bit sequences (PRBS)

Experimental results for a PRBS test pattern are shown in Figure 4.28. Since the bandwidth of Design 2 is less than Design 1, power efficiency is lower because the spectrum of the PRBS pulse train is wide. Drain efficiency peaks for patterns with data rates near 1 Gb/s and corresponds to a compromise between low frequency cutoff in the drain bias circuit and high frequency cutoff in the output circuit. A comparison of simulated and

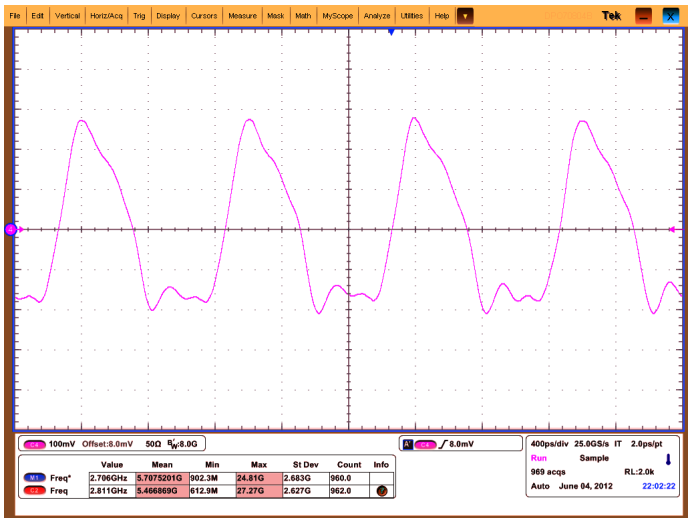

Figure 4.24: Measured output voltage waveform at node C for a 1 GHz CW input signal.

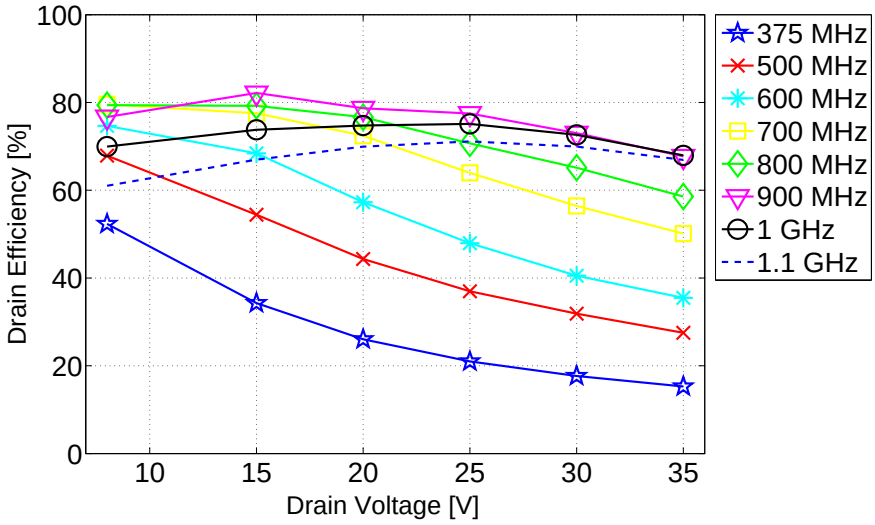

Figure 4.25: Comparison of the measured drain efficiency versus drain voltage for different CW frequencies.

experimental results is shown in Figure 4.29. The simulation results over estimate efficiency by 5-10% depending on the supply voltage.

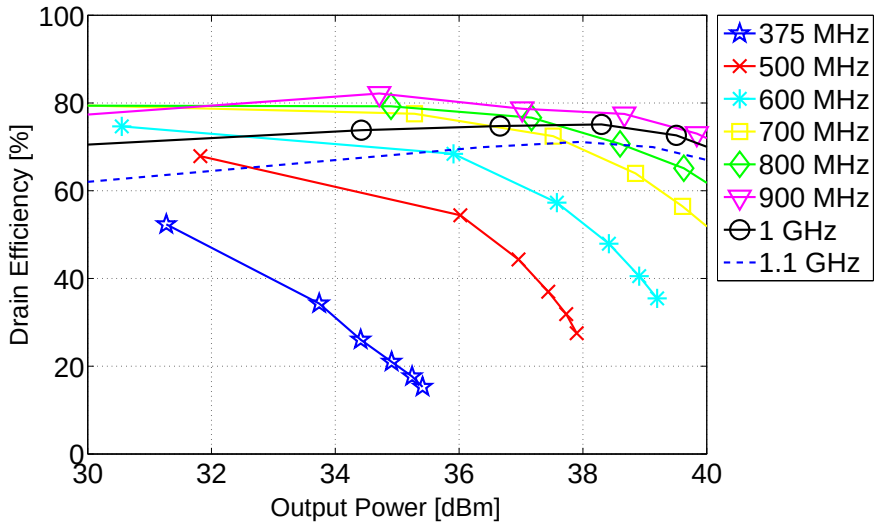

Figure 4.26: Comparison of the measured drain efficiency versus output power for different CW frequencies.

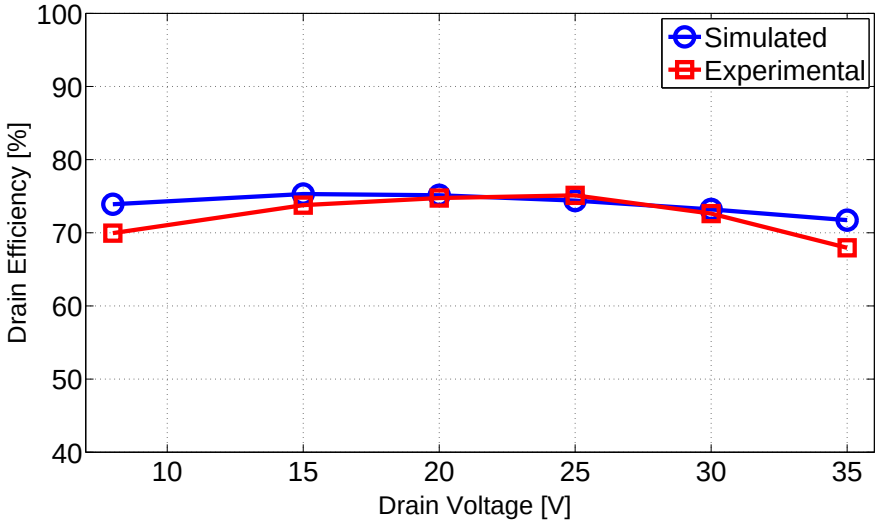

Figure 4.27: Drain efficiency versus drain voltage for a CW source signal at 1 GHz. Measured and simulated data are shown.

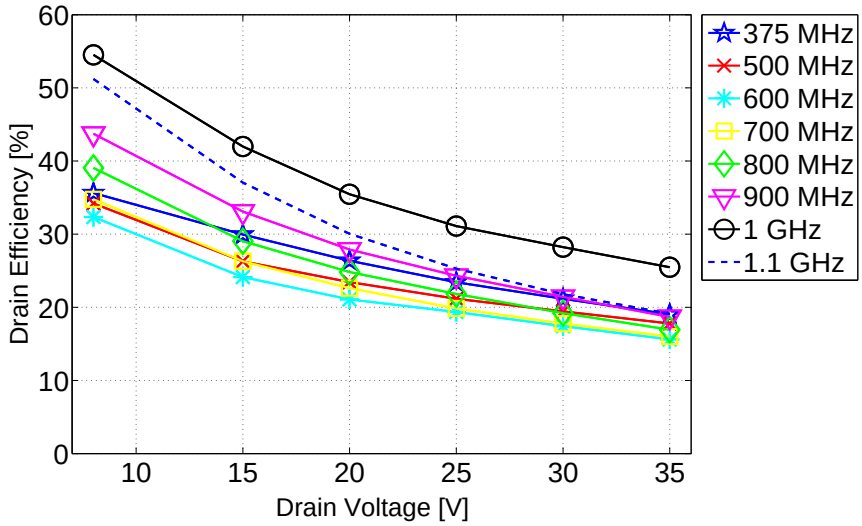

Figure 4.28: Measured drain efficiency versus drain voltage for different PRBS data rates.

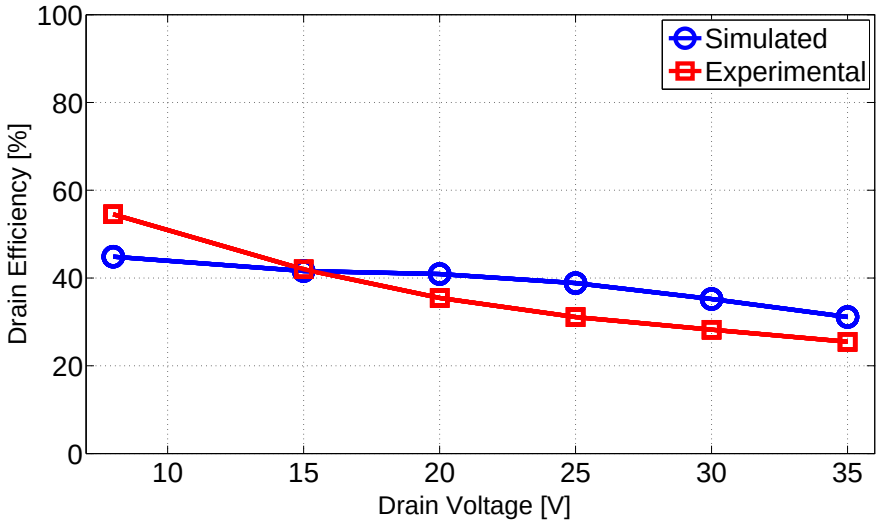

Figure 4.29: Comparison of simulated and experimental results for Design 2 using a PRBS source signal at 1 GHz.

4.6 Results for Design 3

In Design 3, an output matching circuit is implemented to transform 50 Ω to an optimum load impedance of 33.3 Ω. The purpose of transforming the load impedance is to improve the utilization of the device and increase the power delivered to the load. However, the matching circuit also limits the bandwidth of the output circuit and the bandwidth of Design 3 is narrower than Design 2. Experimental results with sinusoidal and PRBS test patterns are presented next.

4.6.1 SMPA performance with a sinusoidal source signal

Figure 4.30 shows the output signal at node C for a 1 GHz sinusoidal input signal. The drain supply voltage is 25 V. Compared to Designs 1 and 2, the waveform is nearly sinusoidal and the limitations in bandwidth are evident. The bandwidth of the output circuit is 1.8 GHz, and harmonics are significantly attenuated.

Drain efficiency versus supply voltage and output power are shown in Figures 4.31 and 4.32 respectively. Overall, drain efficiency for Design 3 is slightly better than Design 2 for all frequencies which shows that the improvement in output match has increased the output power. With respect to Figure 4.32, the average drain efficiency is approximately 67% which is the best performance for a frequency of 1 GHz frequency.

A comparison between the simulated and experimental results for a frequency of 1 GHz is shown in Figure 4.33.

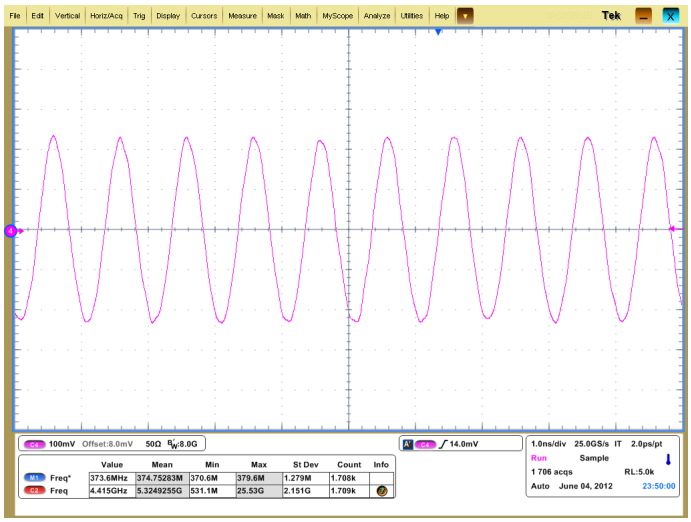

Figure 4.30: Measured output voltage waveform at 1 GHz frequency for CW excitation.

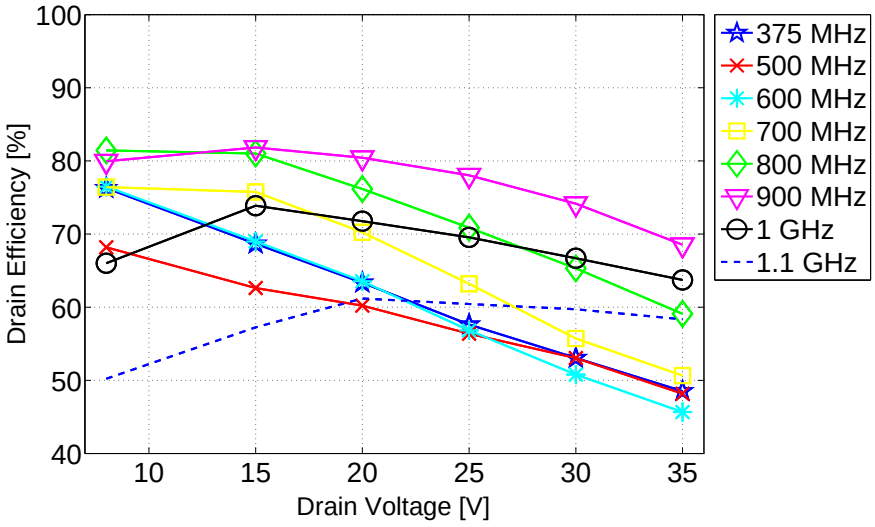

Figure 4.31: Comparison of the measured drain efficiency versus drain voltage for different CW frequencies.

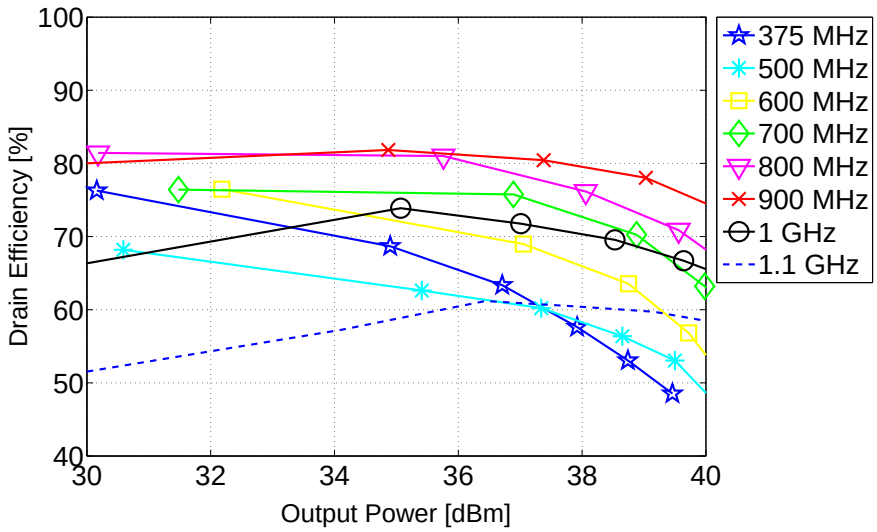

Figure 4.32: Comparison of the measured drain efficiency versus output power for different CW frequencies.

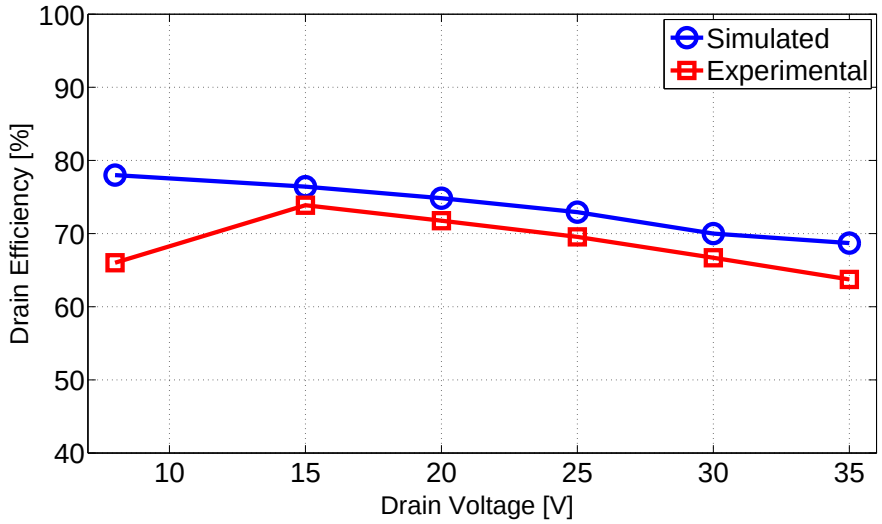

Figure 4.33: Drain efficiency versus drain voltage for a CW source signal at 1 GHz. Measured and simulated data are shown.

4.6.2 SMPA performance with Pseudo-random bit sequences (PRBS)

Experimental results for Design 3 with a PRBS test pattern are shown in Figures 4.34 and 4.35. The average drain efficiency is around 45% from 375 MHz to 1.1 GHz frequency range for the entire voltage span. All the drain efficiency traces follow a similar pattern: at low output power, the drain efficiency is high and drain efficiency then decreases as output power increases.

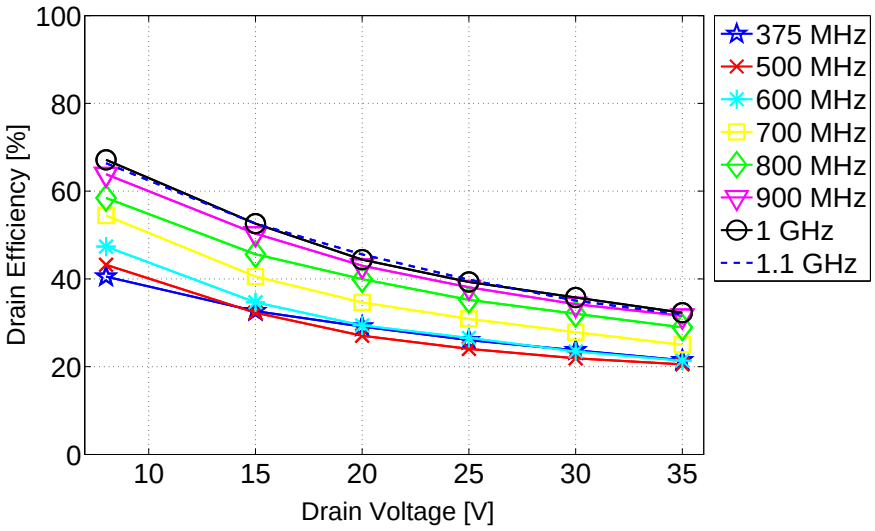

Figure 4.34: Comparison of the measured drain efficiency versus drain voltage for PRBS pulse trains.

Figure 4.36 shows a comparison between simulated and experimental drain efficiency for a frequency of 1 GHz. The average drain efficiency predicted by the simulation model is around 60% while experimental results are lower around 45%.

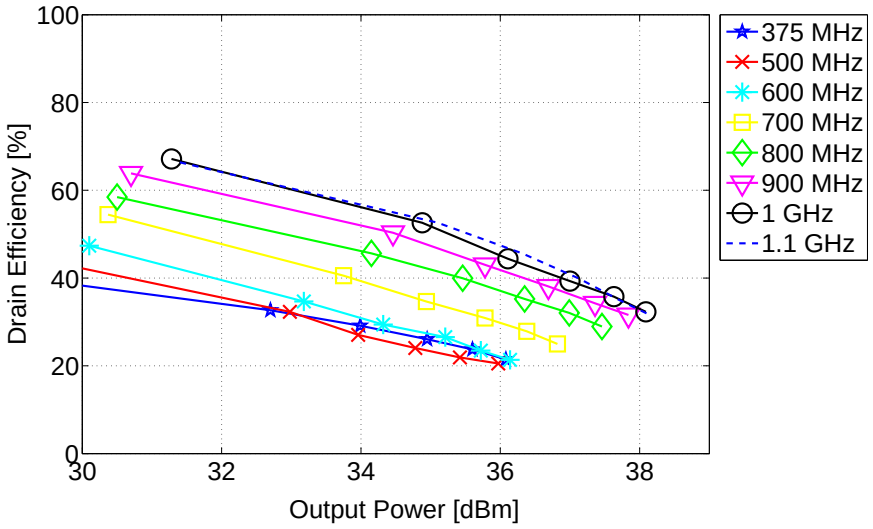

Figure 4.35: Comparison of the measured drain efficiency versus output power for PRBS pulse trains.

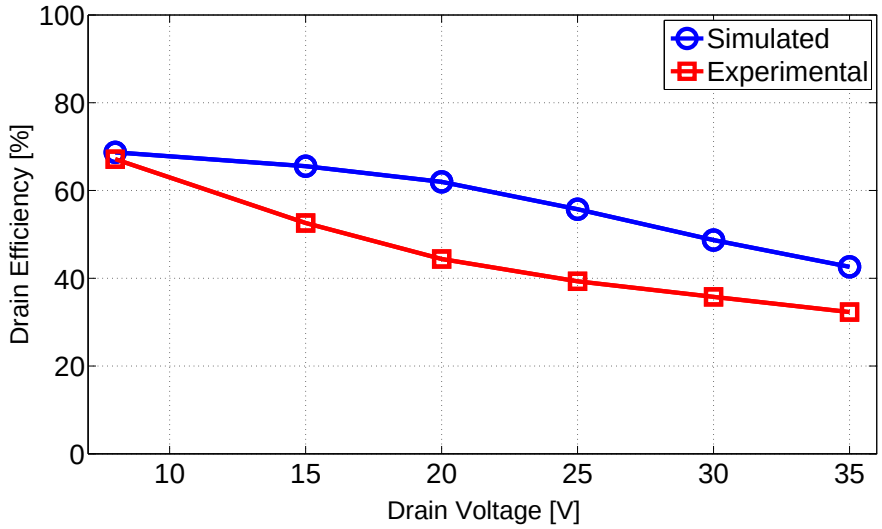

Figure 4.36: Drain efficiency versus drain voltage for a PRBS source signal at 1 GHz. Measured and simulated data are shown.

4.7 Design Comparison Summary

A summary of the three designs is presented in the following sections. The purpose of the summary is to highlight the trade-offs in the different designs and draw conclusions from the experimental results.

4.7.1 Bandwidth Comparison

The objective in Design 1 was to maximize the bandwidth of the SMPA by implementing a simple output network that consists of a broadband drain bias circuit and an AC coupled output to a 50 Ω transmission line. In Design 2, the objective was to demonstrate that power efficiency could be improved by tuning the output bias circuit to resonant with the output capacitance of the switch. The resonate circuit compromised bandwidth to gain efficiency. In Design 3, the objective was to improve the utilization of the power device by implementing a matching network to transform 50 Ω to the optimum load match of 33.3 Ω. The matching circuit that was implemented had a bandwidth that was narrower than both Designs 1 and 2. The frequency response for each of the SMPA output networks is shown in Figure 4.37 and a summary of the bandwidth for each design is tabulated in Table 4.1. Simulation results are shown because the network analyzer which was available had an upper frequency limit of 1.5 GHz while a much larger frequency span could be generated in the simulator.

Table 4.1: Bandwidth comparison for SMPA designs.

Design	-3 dB Bandwidth (GHz)
Design 1	5.4
Design 2	2.4
Design 3	1.8

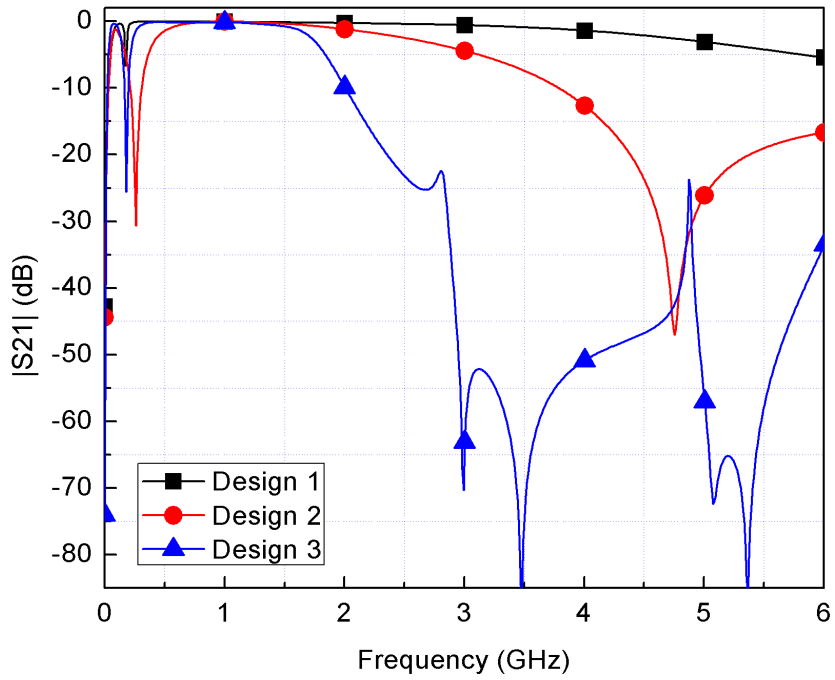

Figure 4.37: Output network bandwidth comparison for the three SMPA designs.

The simulated results for the bandwidth of each design are consistent with measurements of the output waveform at node C. If a comparison of Figures 4.9, 4.24 and 4.30 are made in Figure 4.37, it is clear that the output network becomes progressively narrower. In Design 1, the output was very broadband and a square wave signal with good harmonic content is observed while in Design 3, the output is nearly sinusoidal.

4.7.2 Comparison of Results for Sinusoidal Source Signals

A comparison of the output power versus the drain supply voltage for all three designs is shown in Figure 4.38. The power corresponds to measurements made at node C at a frequency of 1 GHz. Design 1 has the

largest output signal bandwidth and the output power spectrum is therefore broader than Design 2 and 3. Since the measured power at node C is the total power in the spectrum, Design 1 has the highest output power. Design 2 and Design 3 are very similar with slightly less power. The tuned output stage in Design 2 increases the efficiency of the SMPA for signals within the bandwidth of the SMPA but attenuates harmonic power. The net effect in Design 2 is an output power which is slightly less than in Design 1. Design 3 has an even narrower bandwidth than Design 2 but the device match is improved to increase the output power delivered by the device. The bandwidth reduction which reduces harmonic power combined with the change in match to R_{opt} provides similar power characteristics compared to Design 2.

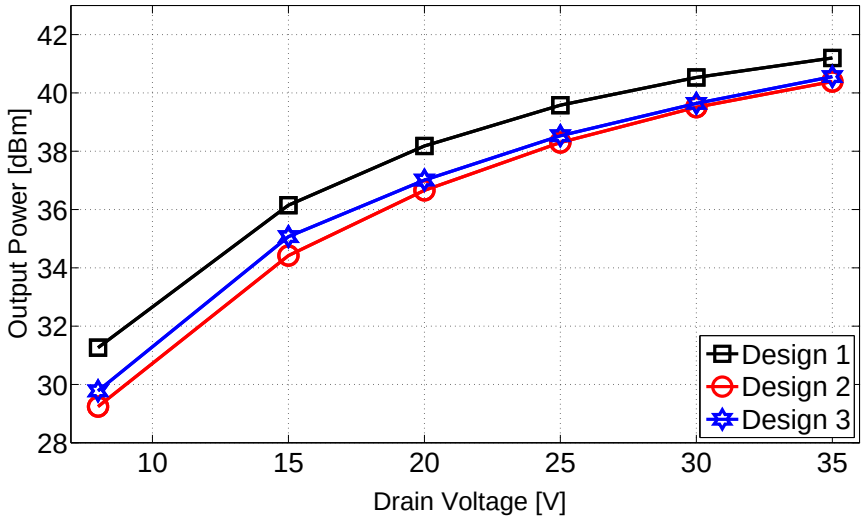

Figure 4.38: Comparison of measured output power for SMPA designs at 1 GHz with a CW signal.

The corresponding power efficiency characteristics for the three different designs are shown in Figure 4.39. Design 2 has the best drain efficiency

characteristic which reduces loss associated with the output capacitance of the device because a resonant tank is employed in the match. Design 3 also exploits the concept of a tuned output stage combined with an optimum match. However, the trade-off between bandwidth and power in Design 3 resulted in lower efficiency than Design 2. Design 1 has the lowest power efficiency but the highest output power. Design 1 did not compensate for the output capacitance of the device. Therefore, switching losses associated with the charging and discharging add to losses in the switch. In a resonant design, like Design 2, the losses are reduced because energy is exchanged between the output capacitance C_p and the drain bias inductor L_{p1} rather than being dissipated in the switch.

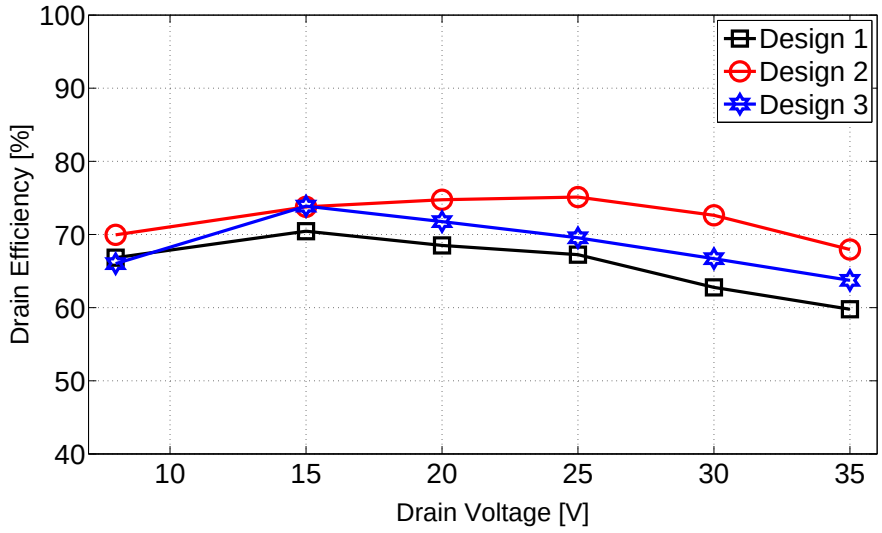

Figure 4.39: Comparison of measured drain efficiency for three different design at 1 GHz CW frequency.

4.8 Comparison of Results for PRBS Bit Sequences

A comparison of the three designs with PRBS bit sequences is shown in Figures 4.40 and 4.41. The measurements correspond to a data rate of 1 Gb/s. The PRBS spectrum is broadband and therefore the output power at node C is expected to be the highest for Design 1 since it has the largest bandwidth. This is confirmed by results shown in Figure 4.40 (output power vs drain supply voltage). The results for Design 2 and 3 are more difficult to predict in terms of conceptual arguments since Design 2 has more bandwidth than Design 3 while Design 3 is matched to deliver more power than Design 2. The experimental results show that Design 3 has slightly more power than Design 2; however both Design 2 and 3 have less power than Design 1 which shows that the output bandwidth of the SMPA is important for maximizing output power. Drain efficiency for the PRBS test pattern follows the same trend as output power. That is, the drain efficiency of Design 1 is the best, followed by Design 3, and then Design 2.

4.8.1 Conclusions

Several conclusions can be made from the experimental work and these lead to recommendations for future research activities. First, Design 1 shows that a broadband output stage has the advantage of reducing the sensitivity of drain efficiency to different switching waveforms. Power efficiency results at a frequency of 1 GHz ranged from 57% to 73% for sinusoidal, periodic and PRBS test signals for the entire voltage span. Secondly, Designs 2 and 3 showed that a tuned and optimally matched output network have merits but the design implementations reduced bandwidth which offset some of the

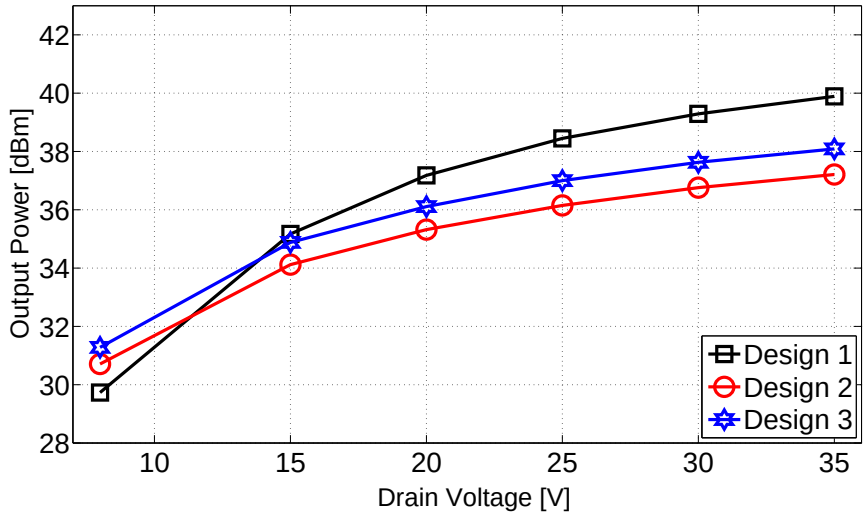

Figure 4.40: Comparison of measured output power for SMPA designs with a 1 Gb/s PRBS signal.

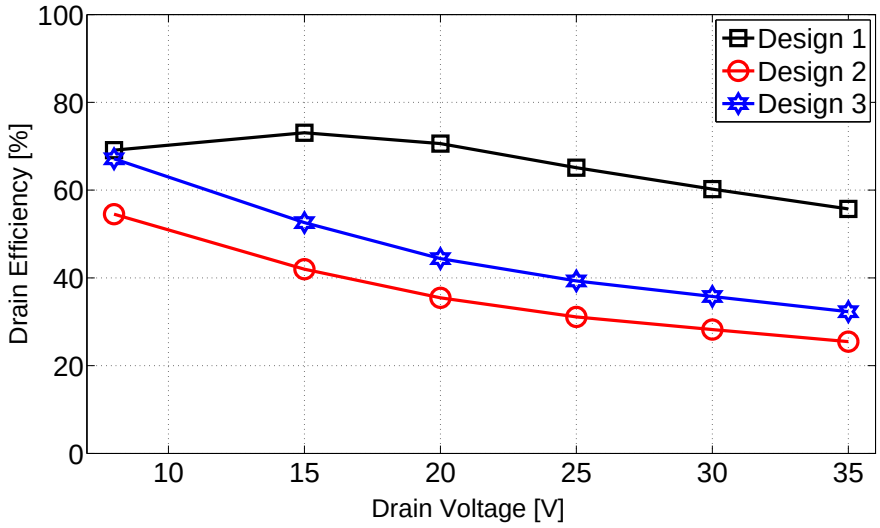

Figure 4.41: Comparison of measured drain efficiency for SMPA designs with a 1 Gb/s PRBS signal.

gains made by these circuit changes. In future work, it is recommended that the trade-offs between bandwidth, tuning and optimum power match be explored more thoroughly. For example, rather than implementing a cascade of L-match circuits with distributed elements, it is proposed that a design with a stepped impedance series transmission line be investigated. Also, specially designed spiral inductors and high Q DC blocking capacitors with high capacitance can be used to improve the bandwidth of the drain bias circuit.

4.9 Results for Design 1 with a Complementary Diplexer

So far all the measurements results which have been discussed were made at node C. A broadband attenuator was connected to node C and measurements with a power meter, oscilloscope or spectrum analyzer were then made. Measurements with the diplexer load are now presented.

As shown in Figure 4.42, a complementary diplexer is used in the SMPA architecture to provide in-band and out-of-band signal separation while simultaneously presenting a fixed broadband load to the output of the amplifier. In effect, the design concept is that the diplexer is equivalent to a broadband load and the replacement of the output attenuator with the diplexer should not change the performance of the SMPA. Since Design 1 has the largest output bandwidth, it is used for tests with the diplexer.

Figure 4.43 shows the drain efficiency of the complementary diplexer referred to node C in Figure 4.42. The total power at the bandpass and bandstop terminals were measured. The insertion loss of each diplexer filter branch was also measured. For the bandpass filter the insertion loss is

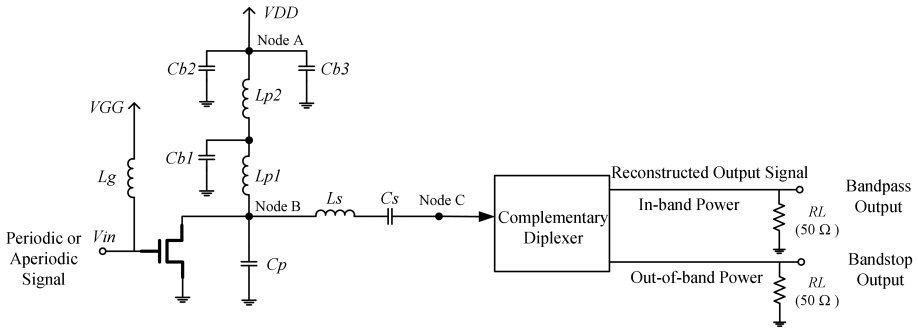

Figure 4.42: Circuit diagram of the Design 1 SMPA with a complementary diplexer.

approximately 2.18 dB and for the bandstop filter the insertion loss is approximately 0.3 dB. The output power and the insertion loss measurements are then combined to determine what the total power in the system is at node C. The power at node C is then used to calculate the drain efficiency of the SMPA which is compared to the drain efficiency measured with an attenuator instead of the diplexer. As shown in Figure 4.44 the sum of the diplexer output power normalized for insertion loss is nearly identical to the power efficiency measured with an attenuator. This shows that the complementary diplexer presents a load impedance to the SMPA that is nearly identical to a broadband load. In the next two chapters, additional results which extend the evaluation of the SMPA with the diplexer are presented.

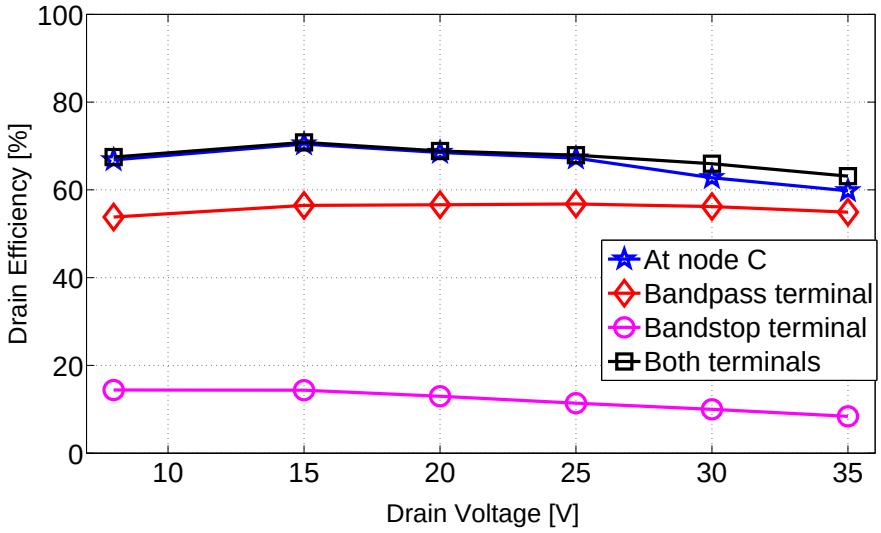

Figure 4.43: Drain efficiency for Design 1 with complementary bandpass/bandstop diplexer.

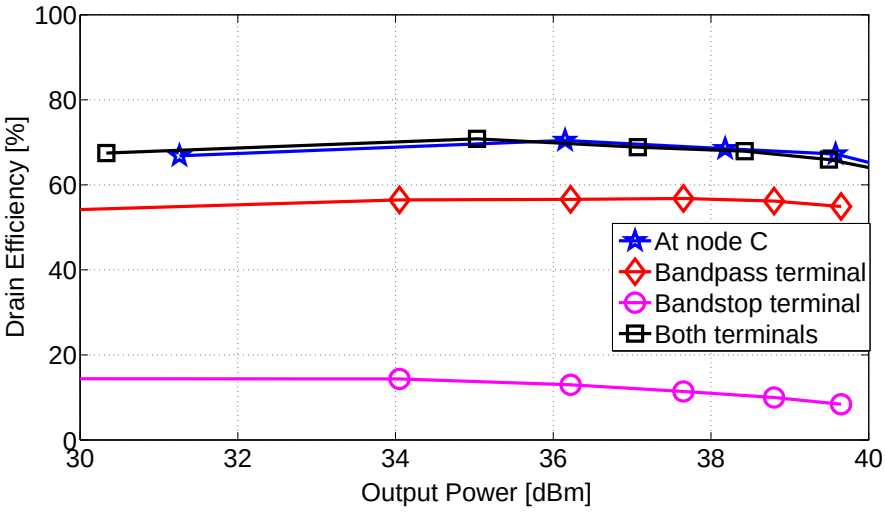

Figure 4.44: Output power versus drain efficiency for Design 1 with a complementary diplexer.

Chapter 5

Pulse Encoded Responses

One of the primary motivations for this research work is to design a RF switch-mode power amplifier architecture that can efficiently amplify encoded pulse trains. A switch-mode power amplifier operates in a highly nonlinear mode and amplitude variation in a modulated source signal will experience severe distortion if the source signal is directly applied to the input of the switch-mode amplifier. Linearity can be significantly improved if the source signal is first encoded into a pulse train which can be efficiently amplified, and then recovered at the output of the amplifier. The class of possible encoders that are compatible with RF switch-mode amplifiers are constrained by signal reconstruction. In most SMPAs a bandpass filter is used for signal reconstruction. In this design, the bandpass filter is integrated.

Most research in RF switch-mode power amplifiers has focused on using bandpass sigma-delta modulation (SDM) as a source encoder. Sigma-delta modulation uses a clocked quantizer to generate a two level encoded pulse train that can be amplified. Since the quantizer is clocked, the timing of zero-crossings in the pulse train are constrained by the clock period. The constrained timing can limit the phase which can be encoded at the peak amplitude of the source signal. Other encoding methods are possible which improve coding efficiency at peak amplitude. One of these methods is called

noise shaped pulse position modulation, a design similar to SDM, except that the clocked quantizer is replaced by a pulse generator which can be triggered asynchronously.

A high speed arbitrary waveform generator was not available during this research project which limited experimental testing to periodic pulse trains and PRBS pulse trains as described earlier in chapter 4. In this chapter, simulation models for the RF switch-mode power amplifier are used to predict the performance of the amplifier with encoded pulse trains. Matlab was used to generate encoded pulse trains which were saved as input files and then used in circuit simulations using ADS. The results of these circuit simulations are described next.

5.1 Generation of Pulse Encoded Signals

5.1.1 Sigma-delta Modulation (SDM)

Bandpass sigma-delta modulation (SDM) [19] has been used by many researchers as a source encoder. In a bandpass SDM encoder, a one bit clocked quantizer is enclosed in a negative feedback loop with a noise shaping filter as shown in Figure 5.1. The quantizer is gated by an external clock

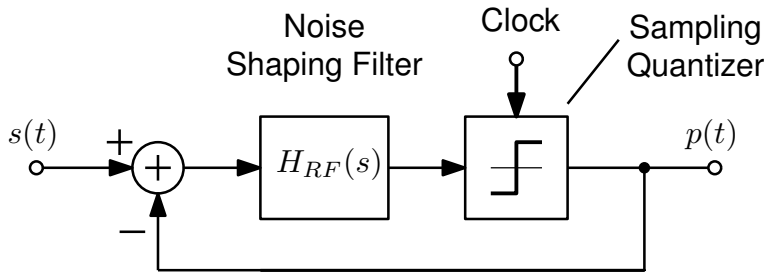

Figure 5.1: Block diagram of a sigma-delta modulator (SDM).

signal and in this work the clock frequency is 3.4 times the carrier frequency (f_c) of the source signal. The clocked quantizer constrains the timing of level crossings in the output pulse train to be synchronous with clock transitions. An example of a sinusoidal input signal and the corresponding SDM encoded signal is shown in Figure 5.2. The thick black line is the pulse encoded signal and the timing of level crossings is synchronous with the clock.

A fourth order spread zero noise shaping transfer function is used in this SDM design. The transfer function of the noise shaping filter is

$$H_{RF}(s) = \frac{\sum_{n=0}^{3} b_n s^n}{\sum_{n=0}^{4} a_n s^n} \tag{5.1}$$

and the values of the coefficients are given in Table 5.1. The encoder designs were implemented in Simulink and output pulse trains were saved as waveform files. The waveforms were then used in ADS to characterize the drain efficiency of the SMPA under different modulator drive levels.

Figure 5.3 shows the output power spectrum of the sigma-delta modulated signal with an overlay of the diplexer frequency response. The center frequency is 1 GHz and bandwidth is 20 MHz. The SDM spectrum has a significant amount of out-of-band power created by the quantization process in the encoder and therefore the complementary diplexer is needed to ex-

Table 5.1: Noise shaping filter coefficient values for $H_{RF}(s)$.

n	b_n	a_n
0	$7.3874\ X\ 10^{37}$	$1.5584\ X\ 10^{39}$
1	$2.0201\ X\ 10^{27}$	$8.6858\ X\ 10^{26}$
2	$1.8850\ X\ 10^{18}$	$7.8962\ X\ 10^{19}$
3	$2.6147\ X\ 10^{7}$	$2.2\ X\ 10^{7}$
4	0	1

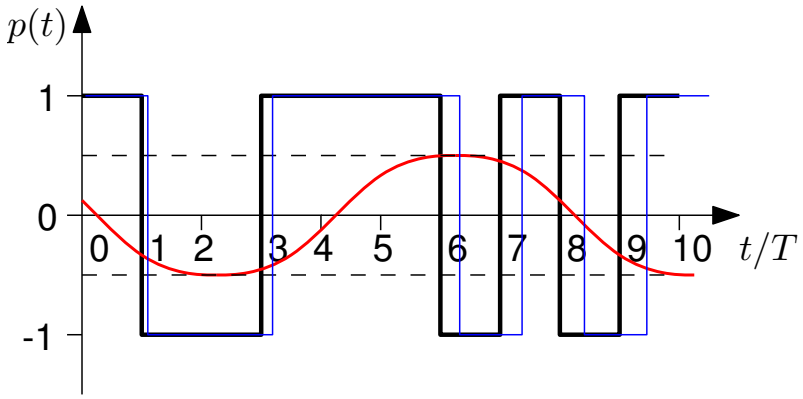

Figure 5.2: Timing diagram of the pulse encoded signals. Black (thick) line shows the sigma-delta pulse trains and blue (thin) line shows the pulse position pulse trains.

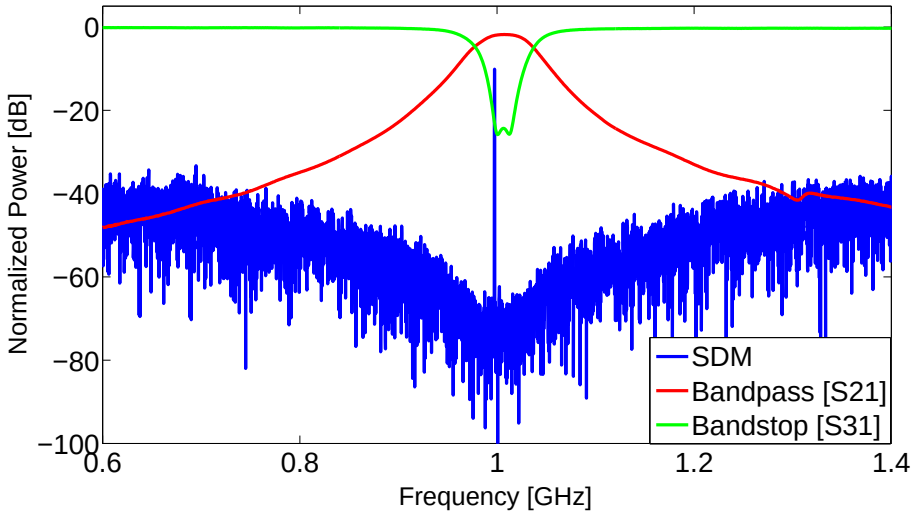

Figure 5.3: Output power spectrum of sigma-delta modulator with diplexer.

tract that out-of-band power through the bandstop output terminal which will help to enhance the overall power efficiency of the SMPA.

5.1.2 Noise-shaped Pulse Position Modulation (PPM)

Another encoder which has better coding efficiency, especially, at large source amplitude levels, is called noise shaped pulse position modulation (PPM) [20]. Noise shaped PPM is a variation of bandpass SDM where the clocked quantizer is replaced with an asynchronous pulse generator; see Figure 5.4 for a block diagram. In this encoder, a pulse generator instead of a clocked quantizer is enclosed in a negative feedback loop. The pulse encoder generates a pulse of duration $T_p = 1/(2f_c)$ whenever the input to the pulse encoder has a zero-crossing; the pulse duration T_p is set to be equal to half the carrier period of the source signal. This type of encoder generates a pulse train similar to pulse position modulation (PPM) and is called a noise shaped PPM encoder [6]. Figure 5.2 shows the waveform for a PPM encoded signal. For this encoder, pulse edges are not constrained and level crossings are asynchronous. The PPM encoder is also implemented in Matlab using the same noise transfer function in equation 5.1.

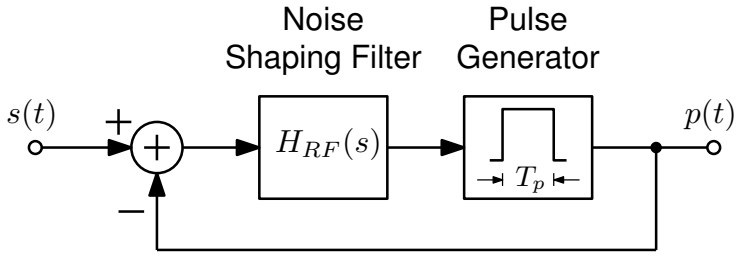

Figure 5.4: Block diagram of a pulse position modulator (PPM).

Figure 5.5 shows the output power spectrum of the PPM pulse train with an overlay of the diplexer frequency responses. The center frequency is 1 GHz the same as the SDM encoder.

In the following section, simulation results with encoders are shown ref-

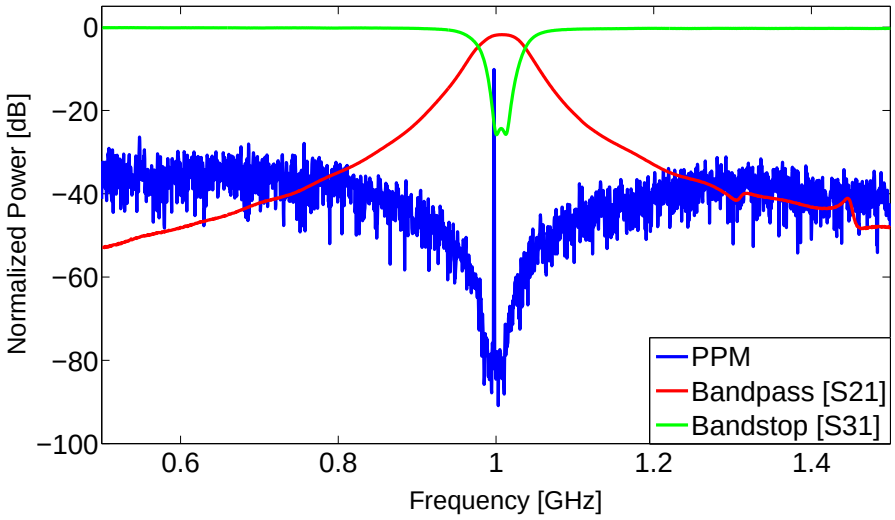

Figure 5.5: Output power spectrum of pulse position modulated signal with diplexer.

erenced to a full scale amplitude of 1 V. For sinusoidal input signals, SDM encoders saturate at full scale while PPM encoders can generate peak amplitude levels which exceed full scale. The peak source signal amplitude for a PPM encoder is $4/\pi \approx 1.27$ V and corresponds to a 50% duty cycle square wave output pulse train. On the other hand, synchronous timing of level crossings in a SDM pulse train means that the encoder cannot always converge to a 50% duty cycle square wave at peak amplitude. Therefore, the asynchronous PPM encoder is more efficient for power amplifier applications and this impact will be evident in the results.

5.2 Results for Pulse Encoded Signals

To validate the proposed topology and investigate the SMPA performance for pulse encoded signals, Design 1 is driven with sigma-delta and

pulse position modulated signals. Figure 5.6 shows the simulated drain efficiency for SDM and PPM signals. Simulated and experimental results are also shown for a sinusoidal (50% duty cycle) switching signal. Drain efficiency for all these results is measured at node C (see Figure 1.9), and the results show that power efficiency does not depend significantly on whether the pulse train is periodic or non-periodic. Periodic switching (both simulated and measured) is about 5% more efficient than non-periodic switching with SDM or PPM encoded pulse trains. This is a very important result as one of the design objectives of this research was to reduce the sensitivity of power efficiency in a SMPA to the type of switching signal.

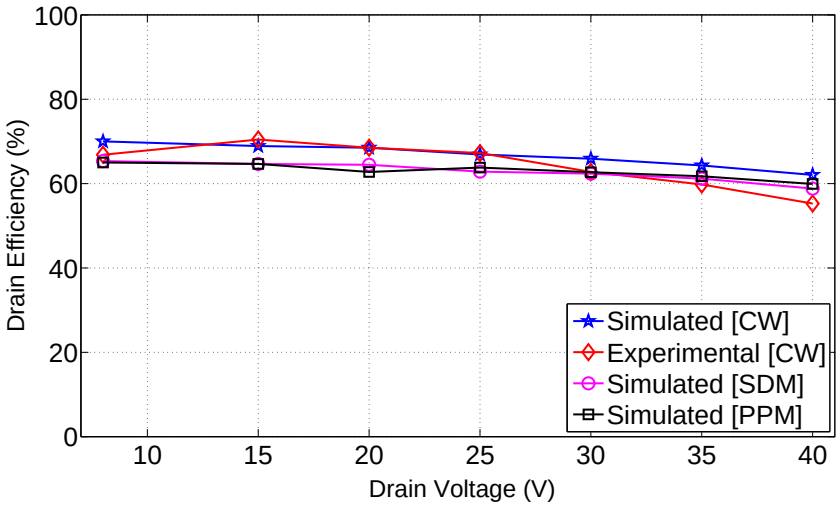

Figure 5.6: Drain efficiency for Design 1 for SDM, PPM and sinusoidal signals.

In Figure 5.7, power efficiency is plotted as a function of the amplitude of the source signal for SDM and PPM encoders. The input source signal is a sine wave with a peak amplitude that is measured relative to 1 V, the quantized (full scale) amplitude level of the output pulse train. Three

different power efficiency values are calculated at each drive level. First, the drain power efficiency of the broadband signal generated at node C (see Figure 1.9) is calculated. The broadband signal consists of both in-band (bandpass) and out-of-band (bandstop) signal components that have been amplified by the SMPA. The second and third drain efficiency curves separate the in-band and out-of-band signal components. The bandpass signal power corresponds to the amplitude of the encoded source signal and decreases as the source amplitude decreases. On the other hand, out-of-band power increases as the source level decreases. The sum of the in-band and out-of-band power is equal to the total power in the pulse train at node C. The summed power is constant while the relative power between in-band and out-of-band signals varies with source amplitude. The results can also be interpreted in terms of coding efficiency which can be calculated from the ratio of the in-band to broadband power.

The timing of level crossings in an SDM encoder are constrained by the clock signal which gates the quantizer. The constraint on the timing of level crossings limits the peak coding efficiency relative to the PPM encoder. The difference in peak coding efficiency is seen for modulator drive levels above 1.1. In the SDM encoder, the output power saturates at an input level of 1.1, while the PPM encoder saturates at a drive level of 1.27 ($4/\pi$). The latter amplitude corresponds to the amplitude of the fundamental frequency component in a 50% duty cycle square wave signal. Below a modulator drive level of 1.1, the in-band signal power of the two modulators are similar. At very low drive levels below 0.6, the out-of-band power and broadband power of the SDM fall below the PPM encoder. The difference is related to the bandwidth of the encoded spectrum relative to the bandwidth of the SMPA. The power spectral density of the PPM encoder is concentrated closer to

the noise well than in the SDM encoder. For modulated signals, it is very desirable to maintain high power efficiency under back-off conditions and it is this objective that leads to the addition of an energy recovery loop which is discussed in the next chapter.

Figure 5.8 shows output power versus modulator drive for both SDM and PPM signals. The total output power at node C is constant for both SDM and PPM encoding. This is expected since the SMPA has a broadband output match that is designed to amplify both in-band and out-of-band spectrum. Two other sets of curves are shown on the graph which separate the in-band and out-of-band power measured at the bandpass and bandstop output terminals of the diplexer. The power is normalized to account for the insertion loss of the diplexer and enable comparison with the total power measured at node C. When the input signal amplitude is high, in-band power is high and out-of-band power is low. Conversely, when the input signal amplitude is low most of the power is in the out-of-band spectrum. The overall efficiency of the SMPA would be improved significantly at low input amplitude if the out-of-band energy could be recycled. An analysis of the efficiency boost which could be obtained with energy recycling is covered in the next chapter.

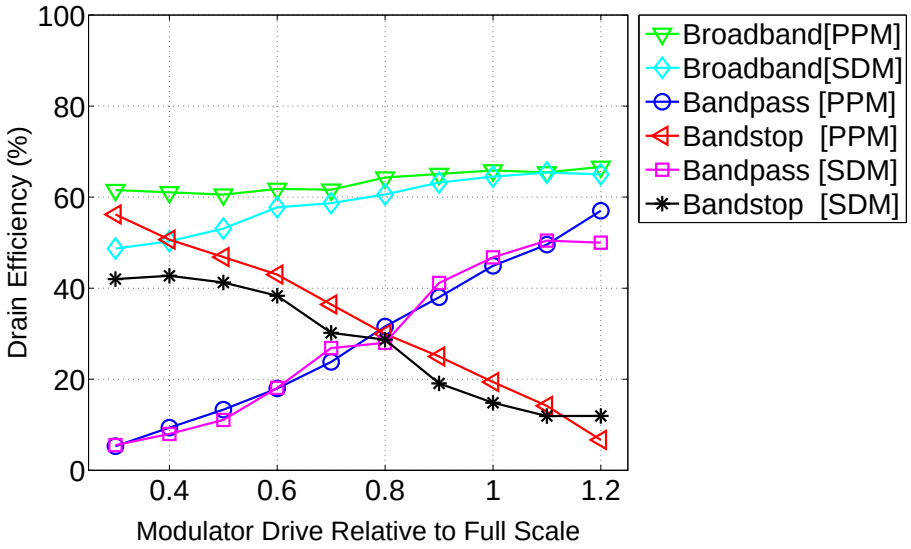

Figure 5.7: Drain efficiency as a function of modulator drive level for SDM and PPM encoders.

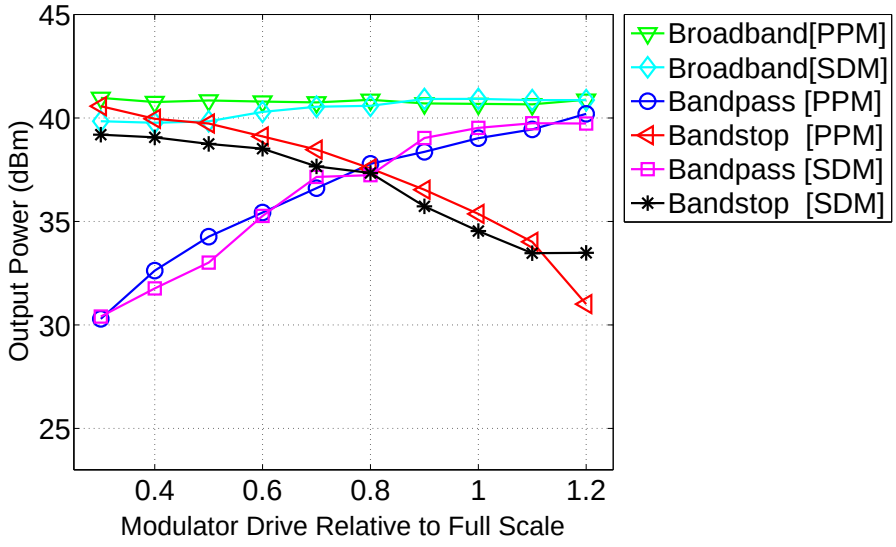

Figure 5.8: Output power as a function of modulator drive level for SDM and PPM encoders.

Chapter 6

Energy Recycling

An important part of the proposed architecture is the energy recycling circuit. A block diagram of the energy recycling concept is shown in Figure 6.1. Out-of-band energy is rectified and converted to DC power which supplements the drain supply for the SMPA. The recovered energy boosts power efficiency especially under low amplitude signal conditions when out-of-band energy is significant.

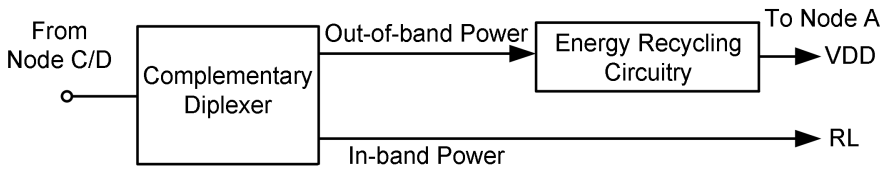

Figure 6.1: Block diagram of the proposed energy recycling circuitry.

6.1 RF to DC Energy Conversion Circuits

RF to DC power conversion has recently been the focus of new research motivated by applications such as energy harvesting for wireless sensors and wireless power transfer. The history of RF to DC power conversion goes back much farther and the pioneering work of Brown [21] focused on high power RF to DC conversion to power a remotely powered helicopter. In all these applications, the research was focused on both an efficient antenna to

receive RF power and the conversion of RF power to DC; hence, the name rectenna is frequently used for integrated antenna and rectification systems.

Experimental results of RF to DC conversion efficiencies in the range of 75–90% have been reported [22–24]. The RF to DC conversion efficiency depends on many factors including device characteristics, frequency, power, load impedance, and bandwidth. Most work has focused on using diode rectifiers but new work is also investigating synchronous RF rectifier circuits [25]. Based on the progress in RF to DC conversion, the possibility of adding an RF energy recovery loop to harvest out-of-band energy is proposed as a way to significantly enhance the power efficiency of the SMPA under back-off conditions.

6.2 Power Efficiency Analysis of SMPA with Energy Recovery

With reference to Figure 6.2, the projected drain efficiency measured at the bandpass output (reconstructed signal) is shown as a function of the amplitude of the source signal $s(t)$. Data are shown for both bandpass SDM and noise shaped PPM. These figures are generated by using the SMPA model of Design 1 with the addition of an energy recovery loop providing a 75% return of out-of-band power to the drain supply. All results are normalized for the insertion loss of the diplexer and data are shown for a 12 dB back-off range relative to peak power.

Without energy recovery, the power efficiency drops as the source level decreases and the SMPA efficiency characteristics are similar to a linear power amplifier. This type of efficiency characteristic is typical of other SMPA designs based on class D or class S circuits. The reduction in power

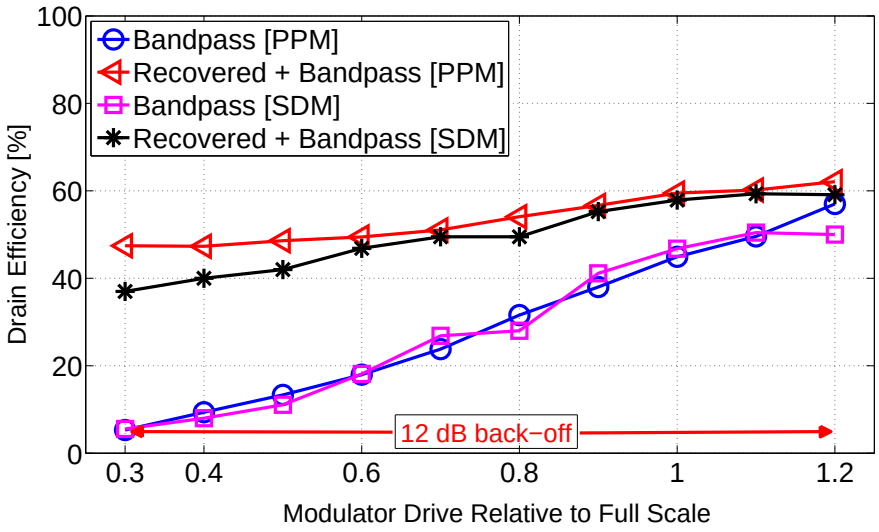

Figure 6.2: Drain efficiency for Design 1 assuming 75% out-of-band energy is recovered.

efficiency with signal level is caused by fixed power losses which burdens power efficiency, especially at low amplitude. If energy recovery is added to the SMPA, there is a significant enhancement in power efficiency especially at large back-offs from peak power. A power amplifier with constant power efficiency that is independent of back-off is highly desirable for modulated source signals with high peak to average power ratios (PAPR). Another important observation is that energy recovery desensitizes the SMPA to the coding efficiency of the encoder. For a 6 dB back-off range (0.6 to 1.2), the SDM and PPM efficiency characteristics are similar while at 12 dB the SDM encoder has a power efficiency of 38% compared to the PPM encoder with an efficiency of 49%.

Implementations of the RF to DC recovery circuit will be investigated in future work. It is also interesting to note that the insertion loss in the bandstop filter branch of the diplexer is much less than the bandpass filter

branch because the bandstop filter is essentially a transmission line with resonators coupled to the through line. This is advantageous to the efficiency of the energy recovery loop especially given that most of the encoder power for modulated signals with high PAPR is out-of-band.

One of the challenges with SMPAs is the large amount of out-of-band power generated by the encoder when a source signal is quantized to binary amplitude levels. Although significant out-of-band power is generated, the advantage of the encoded pulse train is that the amplifying device can be continuously operated at peak power where efficiency is the highest. This is another way of explaining why the power efficiency measured at node C is approximately constant as shown earlier in Chapter 5, Figure 5.8. Assuming peak power can be efficiently encoded, the device utilization is not compromised by the addition of out-of-band power because peak power signals are encoded very efficiently with a small portion of power falling out-of-band. The addition of energy recovery, especially for low amplitude input signals, provides a way to maintain peak power efficiency under back-off conditions thereby exploiting the out-of-band spectrum which is generated by the encoder.

Chapter 7

Conclusion

This chapter concludes the thesis by comparing the contributions made by this work to the original objectives of the project. Potential future work that can be done based on this proposed SMPA architecture is then discussed.

7.1 Evaluation of Thesis Objectives and Contributions

A new RF switch-mode amplifier circuit topology has been proposed which is motivated by the implementation challenges associated with the efficient amplification of non-periodic (encoded) pulse trains. The circuit hard switches a single power device which avoids the need to use baluns, output transformers, high side drivers or protection diodes which may be required in class D and class S circuits topologies. The amplifier design uses a broadband output match coupled to a complementary diplexer to minimize the power dissipation in the switching device. Providing a broadband output match is achieved that matches the bandwidth of the encoded pulse train spectrum, power efficiency is then comparable with periodic switching using a 50% duty cycle square wave. Finally, an energy recovery loop exploiting the amplified out-of-band spectrum is proposed as a way to boost power

efficiency especially under back-off conditions where the coding efficiency of the encoder is usually very low.

Experimental prototypes of the SMPA were constructed to validate several of the concepts proposed in the new design. The driver, power switch, output match, and complementary diplexer were built. Three different output networks for the SMPA were implemented to explore design trade-offs. Design 1 employed a direct match to 50 Ω with a broadband bias network. The bandwidth of the output network in Design 1 was the largest compared to Designs 2 and 3, and Design 1 showed the most robust power efficiency characteristics in terms of periodic and non-periodic switching. In Design 2, the bias network inductor was selected to resonate with the output capacitance of the power device. This provided a boost in power efficiency for narrow-band signals relative to Design 1, but the bandwidth of the output network is narrower. Design 3 went one step further and included an output match which transformed the 50 Ω load to 33.3 Ω which corresponds to the best power match. Similar to Design 2, the trade-off in the output network relative to Design 1 is a reduction in bandwidth. Although Design 1 was robust, there are benefits to integrating the output device capacitance into the output match as well as implementing optimum impedance matches at the output of the device. Future research into the design of output networks that simultaneously satisfy bandwidth and optimum match conditions is recommended.

The introduction of the complementary diplexer into switch-mode power amplifiers is a new concept which provides a way to achieve a high bandwidth output stage yet simultaneously implement a narrow-band signal reconstruction filter. One of the challenges in class D and S circuits is the disruptive effect that a narrow-band output filter has on the power efficiency of the

amplifier. All reported research has shown designs which use reflective out-of-band filters where the objective has been to prevent the dissipation of power in the out-of-band spectrum [3–5]. This is difficult to achieve in experimental work because the out-of-band impedance presented to the switching device is usually uncontrolled and dissipation of out-of-band spectrum still occurs. The complementary diplexer improves the realizability of SMPA circuits by presenting a constant impedance to the switch. There are many new research opportunities that could extend this work including the integration of the complementary diplexers into other SMPA circuit topologies as well as compact structures for implementing complementary diplexers.

The disadvantage of employing a broadband output matche in the SMPA is that out-of-band power is significant. The power could be dumped through the bandstop diplexing port to a load, or, as proposed in this work, it provides an opportunity to enhance power efficiency by returning out-of-band power back to the drain supply. Simulation results were shown for an energy recovery loop assuming a RF to DC conversion efficiency of 75%. Assuming this circuitry can be realized, it provides a way to significantly enhance power efficiency especially under back-off conditions.

7.2 Future Work

Future research into energy recovery circuits is recommended. Research on this topic could include the optimization of the encoder to spectrally shape the out-of-band spectrum to enhance the efficiency of energy recovery. The optimization of Design 3 with a broadband output match and a low loss diplexer is also recommended for future research work.

Bibliography

[1] H. Kobayashi, J. Hinrichs, and P. Asbeck, "Current-mode class-D power amplifiers for high-efficiency RF applications," *IEEE Trans. Microwave Theory Tech.*, vol. 49, no. 12, pp. 2480–2485, Dec. 2001.

[2] T.-P. Hung, J. Rode, L. E. Larson, and P. M. Asbeck, "Design of H-bridge class-D power amplifiers for digital pulse modulation transmitter," *IEEE Trans. Microwave Theory Tech.*, vol. 55, no. 12, pp. 2845–2855, Dec. 2007.

[3] A. Wentzel, C. Meliani, and W. Heinrich, "RF class S power amplifiers: State-of-the-art results and potential," *IEEE MTT-S Symp. Dig.*, pp. 812–815, May 2010.

[4] ——, "A voltage mode class-S power amplifier for the 450 MHz band," *Int. Journal of Micro. And Wireless Tech.*, pp. 315–318, 2011.

[5] ——, "Optimized coding scheme for class-S amplifiers," in *41st European Microwave Integrated Circuits Conference (EuMIC)*, Oct. 2011, pp. 329–332.

[6] T. Johnson, K. Mekechuk, and D. Kelly, "Noise shaped pulse position modulation for RF switch-mode power amplifiers," in *41st European Microwave Integrated Circuits Conference (EuMIC)*, Oct. 2011, pp. 320–323.

[7] V. Carrubba, J. Lees, J. Benedikt, P. Tasker, and S. Cripps, "A novel highly efficient broadband continuous class-F RFPA delivering 74 percent average efficiency for an octave bandwidth," in *IEEE MTT-S Symp. Dig.*, Jun. 2011, pp. 1–4.

[8] D. Wu and S. Boumaiza, "Comprehensive first-pass design methodology for high efficiency mode power amplifier [TC contests]," *IEEE Microwave Magazine*, vol. 11, no. 1, pp. 116–121, Feb. 2010.

[9] M. Helaoui and F. Ghannouchi, "Optimizing losses in distributed multiharmonic matching networks applied to the design of an RF GaN power amplifier with higher than 80 percent power-added efficiency," *IEEE Trans. Microwave Theory Tech.*, vol. 57, no. 2, pp. 314–322, Feb. 2009.

[10] L. Cabria, P. Cabral, J. Pedro, and J. Garcia, "A class E power amplifier design for drain modulation under a high PAPR WiMAX signal," in *IEEE International Microwave Workshop Series on RF Front-ends for Software Defined and Cognitive Radio Solutions IMWS*, Feb. 2010, pp. 1–4.

[11] N. Tuffy, A. Zhu, and T. Brazil, "Class-J RF power amplifier with wideband harmonic suppression," in *IEEE MTT-S Symp. Dig.*, Jun. 2011, pp. 1–4.

[12] D. M. Pozar, *Microwave Engineering.* New York: John Wiley and Sons. Inc., 2006.

[13] S. C. Cripps, *RF Power Amplifiers for Wireless Communications.* Boston-London: Artech House Inc., 1999.

[14] R. J. Wenzel, "Exact design of TEM microwave networks using quarter-wave lines," *IEEE Trans. Microwave Theory Tech.*, vol. 12, pp. 94–111, Jan. 1964.

[15] ——, "Application of exact synthesis methods to multichannel filter design," *IEEE Trans. Microwave Theory Tech.*, vol. 13, pp. 5–15, Jan. 1965.

[16] ——, "Printed-circuit complementary filters for narrow bandwidth multiplexers," *IEEE Trans. Microwave Theory Tech.*, vol. 16, no. 3, pp. 147 – 157, Mar. 1968.

[17] M. C. Horton and R. J. Wenzel, "General theory and design of optimum quarter-wave TEM filters," *IEEE Trans. Microwave Theory Tech.*, vol. 13, pp. 326–327, May 1965.

[18] E. A. Guillemin, *Synthesis of Passive Networks.* New York: John Wiley and Sons. Inc., 1957.

[19] T. Johnson and S. Stapleton, "RF class-D amplification with bandpass sigma-delta modulator drive signals," *IEEE Trans. Circuits Syst.*, vol. 53, no. 12, pp. 2507–2520, Dec. 2006.

[20] T. Johnson, K. Mekechuk, D. Kelly, and J. Lu, "Asynchronous modulator for linearization and switch-mode RF power amplifier applications," in *IEEE RFIC Symposium*, Boston, MA, Jun. 7–9, 2009, pp. 185–188.

[21] W. C. Brown, "The history of power transmission by radio waves," *IEEE Trans. Microwave Theory Tech.*, vol. 32, pp. 1230–1242, Sep. 1984.

[22] W. C. Brown, "Electronic and mechanical improvement of the receiving terminal of a free-space microwave power transmission system," *NASA STI/Recon Technical Report N*, vol. 77, p. 31613, Aug. 1977.

[23] J. McSpadden, L. Fan, and K. Chang, "Design and experiments of a high-conversion-efficiency 5.8-GHz rectenna," *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 12, pp. 2053–2060, Dec. 1998.

[24] M. Roberg, E. Falkenstein, and Z. Popovic, "High-efficiency harmonically-terminated rectifier for wireless powering applications," in *IEEE MTT-S Symp. Dig.*, Jun. 17–22, 2012, pp. –.

[25] M. N. Ruiz, R. Marante, and J. A. Garcia, "A class E synchronous rectifier based on an E-pHEMT device for wireless powering applications," in *IEEE MTT-S Symp. Dig.*, Montréal, Canada, Jun. 17–22, 2012, pp. –.

[26] R. J. Wenzel, "Theoritical and practicla aplications of capacitance matrix transformations of TEM network dresign," *IEEE Trans. Microwave Theory Tech.*, vol. 14, pp. 635–647, Dec. 1966.

Appendix A

Coupled Line Impedance Scaling

A design procedure is given which will provide a systematic way to scale unequal strip widths into equal line widths in a parallel-coupled singly terminated design. The design procedure is based on the use of an elastance (reciprocal capacitance) matrix transformation and is described below.

Consider the parallel-coupled equivalent circuit of Figure 3.10(b) and then the redundant network can be obtained by adding unit elements which is shown in Figure A.1(a). The elastance matrix transformation needs each unit element as a shunt elastance elastance, $S = Z_{ue}$, and each series capacitor as a series elastance, $S_i = 1/C_i$. For elastance matrix, the main diagonal elements can be found by summing all elastances in each circuit loop and off-diagonal elements is equal to the negative of the elastance mutual to each loop [18], [26].

Figure A.1(b) shows the elastance network of the S-plane network of

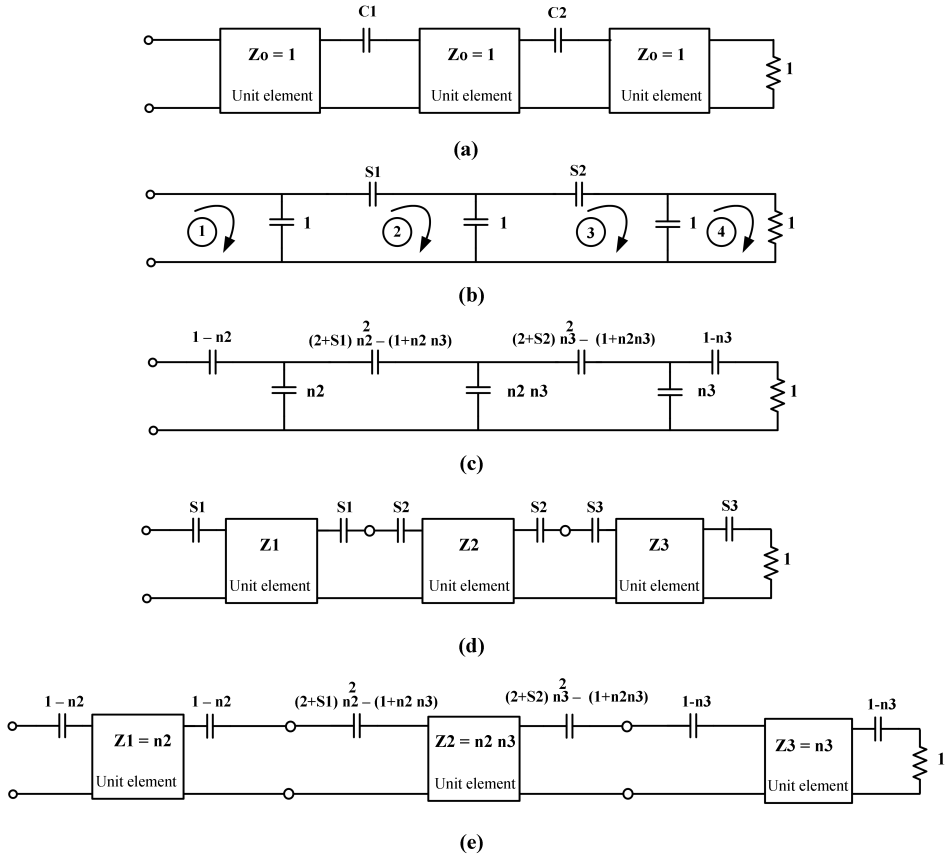

Figure A.1: Equal strip width design by use of an elastance matrix transformation (a) Parallel coupled equivalent circuit with two redundant unit elements. (b) Elastance equivalent network for (a). (c) Elastance network for arbitrary n_2 and n_3. (d) S-plane equivalent circuit for equal strip width realization. (e) Equal strip width realization with specific element values.

Figure A.1(a) and the corresponding 4x4 elastance matrix is given below

$$\begin{bmatrix} 1 & -1 & 0 & 0 \\ -1 & (2+S_1) & -1 & 0 \\ 0 & -1 & (2+S_2) & -1 \\ 0 & 0 & -1 & 1 \end{bmatrix}. \tag{A.1}$$

Next, if we multiply this elastance matrix with a row vector $[n_1\ n_2\ n_3\ n_4]$ and a column vector $[n_1\ n_2\ n_3\ n_4]$ we get the following matrix

$$\begin{bmatrix} n_1^2 & -n_1n_2 & 0 & 0 \\ -n_1n_2 & (2+S_1)n_2^2 & -n_2n_3 & 0 \\ 0 & -n_2n_3 & (2+S_2)n_3^2 & -n_3n_4 \\ 0 & 0 & -n_3n_4 & n_4^2 \end{bmatrix}. \tag{A.2}$$

Equivalent transmission properties and termination impedances are obtained if the input and output loop impedances are unchanged and this requires $n_1 = n_4 = 1$ in matrix (A.2) [26], [18]. Therefore, n_1 and $n_4 = 1$ are fixed while n_2 and n_3 can be used to scale the matrix (A.2). The scaled to matrix is then

$$\begin{bmatrix} 1 & -n_2 & 0 & 0 \\ -n_2 & (2+S_1)n_2^2 & -n_2n_3 & 0 \\ 0 & -n_2n_3 & (2+S_2)n_3^2 & -n_3 \\ 0 & 0 & -n_3 & 1 \end{bmatrix}. \tag{A.3}$$

Figure A.1(c) shows the implementation of matrix (A.1) in terms of arbitrary parameter n_2 and n_3 and the desire S-plane equivalent circuit is shown in Figure A.1(d). For equal strip widths in a parallel-coupled realization, the series capacitors on both sides of each unit element must be identical [14] and applying this constraint gives the final equivalent of Figure A.1(e). So, the relationship between the two capacitances in coupled line section of Figure A.1(e) is,

$$(2+S_1)n_2^2 - (n_2n_3+1) = (2+S_2)n_3^2 - (n_2n_3+1). \tag{A.4}$$

Solving for n_2 in terms of n_3 gives

$$n_2^2 = \frac{(2 + S_1)}{(2 + S_2)} n_3^2. \tag{A.5}$$

So, we can choose either n_2, or n_3 and then calculate the other value from equation (A.5).