DIGITAL CONTROL TECHNIQUES FOR POWER QUALITY IMPROVEMENTS IN POWER FACTOR CORRECTION APPLICATIONS

by

Colin William Clark

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Abstract

The prevalence of standards and recommended practices to meet harmonic current limits has gained, and continues to gain, momentum over recent years. To meet these requirements, power electronic rectification devices are necessitated along with their specialized control techniques. A popular power electronic circuit to obtain low-harmonic input current is the boost power factor correction (PFC) converter, and with the advent of digital control, powerful control techniques to meet these harmonic current limits are possible.

The first contribution is a detailed guide to the conversion of an analog IC-controlled boost PFC converter to a digitally controlled equivalent. Design of the voltage and current sensing networks, compensator, overview of the critical interrupt service routines, and the control implementation in a digital signal processor (DSP) is presented. The existing boost PFC converter modified for digital control is successful, and provides a flexible prototyping test bench for further use.

The second contribution is a novel DSP-based discontinuous conduction mode (DCM) detection method for application to the boost PFC converter. The proposed detection method is computationally simple, and requires little or no modification to existing digitally controlled boost PFC converters using DSPs with on-board comparators. An experimental boost PFC converter verifies the effectiveness of the proposed detection method over traditional zero current detection and DCM detection techniques, enabling advanced control techniques for power quality improvements.

The final contribution is a new adaptive mixed conduction mode (MCM) control technique for the boost PFC converter. This MCM control technique applies the proposed DSP-based DCM detection method to realize higher power factor and decreased total harmonic distortion (THD) over a commercially available analog controller and a conventional digital controller. Using a boost PFC

converter operating in MCM with the proposed adaptive control method, THD improvements of up to 4.55% at light loads and power factor improvements of up to 17.4% are provided over the analog and conventional digital controller.

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List of Symbols

a_n	n_{th} numerator coefficient of 2P2Z transfer function
b_n	n^{th} denominator coefficient of 2P2Z transfer function
C	Capacitor
C_i^{CCM}	CCM current compensator
C_i^{DCM}	DCM current compensator
$CMPA$	Counter compare A register
$CMPB$	Counter compare B register
C_n	Combined parasitic capacitances of switch and output diode
C_v	Voltage compensator
d	Duty cycle
D	Diode
DCM_{flag}	Discontinuous conduction mode flag
DCM_{imm}	Discontinuous conduction mode immediate value flag
D_{DC}	DC duty cycle
d_n	n^{th} duty cycle
$e[k-n]$	n^{th} previously computed error for 2P2Z controller
f_c	Cutoff frequency
f_{line}	AC line frequency
f_{samp}	Sampling frequency
f_{sw}	Switching frequency
G_{delay}	Delays transfer function
G_i^{CCM}	CCM control-to-output boost PFC transfer function
G_i^{DCM}	DCM control-to-output boost PFC transfer function
i_{ac}	AC line current
i_D	Diode current
i_L	Inductor current
I_L	Average inductor current
$I_{n,rms}$	n^{th} RMS current component
i_{pk}	Peak ac input current
i_Q	Switch current

i_{ref}	Inner current loop reference current
I_{rms}	Fundamental RMS current
i_{sense}	Scaled inductor current
K_{ac}	AC input voltage sensor gain
K_{ADC}	Analog-to-digital converter gain
k_{avg}	Exponential moving average weighting factor
K_{crit}	Critical boundary condition
K_{DPWM}	DPWM gain
K_i	Current sense amplifier gain
K_s	Current sensing network gain
K_v	Output voltage sensor gain
k	Discrete-time sample
L	Inductor
P_{out}	Output power
Q	Switch
R_e	Emulated resistance
R_L	Load resistance
R_s	Current sense resistor
R_{ZCD}	Zero-current detection current limiting resistor
S	Apparent power
s	Laplace complex variable
t	Time
TBCTR	Time-base counter register
TBPRD	Time-base period register
T_{DCM}	DCM resonant period
T_i^{CCM}	CCM open-loop gain
T_i^{DCM}	DCM open-loop gain
T_{off}	Off period
T_{on}	On period
T_s	Sampling period
T_{sw}	Switching period
$u[k-n]$	n^{th} previously computed duty cycle for 2P2Z controller

v_-	Comparator negative terminal input
v_+	Comparator positive terminal input
v_{ac}	AC line voltage
v_{acL}	Scaled AC live line voltage
v_{acN}	Scaled AC neutral line voltage
v_{aux}	Auxiliary inductor winding voltage
v_c	Outer voltage loop control signal
V_{CC}	Auxiliary supply voltage
V_{DC}	DC output voltage of DC-DC converter
v_{err}	Outer voltage loop error
v_L	Inductor voltage
V_M	Peak input voltage
v_{min}	Minimum rms ac line voltage
V_o	Output voltage
v_o	Scaled output voltage
v_{rec}	Rectified input voltage
v_{recadc}	Scaled rectified input voltage
v_{recavg}	Average value of rectified input voltage
V_{ref}	Reference voltage setpoint
V_{rms}	Fundamental RMS voltage
$V_{TH\ ZCD}$	Zero-current detection threshold voltage
y	Comparator output
z	Discrete-time complex variable
ZCD_{flag}	Zero current detection flag
η	Efficiency
θ_1	Fundamental voltage phase
κ	DCM average current correction factor
φ_1	Fundamental current phase
ω_n	Parasitic resonant frequency

List of Abbreviations

2P2Z	Two pole two zero
AC	Alternating current
ADC	Analog-to-digital converter
ASIC	Application-specific integrated circuit
BCM	Boundary conduction mode
CCM	Continuous conduction mode
Comp	Comparator
DAC	Digital-to-analog converter
DC	Direct current
DCM	Discontinuous conduction mode
DPWM	Digital pulse width modulation
DSP	Digital signal processor
EMI	Electromagnetic interference
FPGA	Field-programmable gate array
IC	Integrated circuit
IIR	Infinite impulse response
ISR	Interrupt service routine
MCM	Mixed conduction mode
PF	Power factor
PFC	Power factor correction
PI	Proportional-integral
PWM	Pulse-width modulation
RC	Resistor-capacitor
RMS	Root Mean Square
SEPIC	Single-ended primary-inductance converter
SOC	Start-of-conversion
THD	Total harmonic distortion
ZCD	Zero current detection

List of SI Units and Prefixes

p	Pico (10^{-12})
n	Nano (10^{-9})
μ	Micro (10^{-6})
m	Milli (10^{-3})
k	Kilo (10^{3})
M	Mega (10^{6})
A	Amperes
F	Farads
H	Henries
Hz	Hertz
s	Seconds
V	Volts
W	Watts
°	Degrees
Ω	Ohms

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For Hyunjoo

1 Introduction

The rising popularity of switched-mode power supplies to meet efficiency and performance objectives has been met with the development of industry regulations and recommended practices for power quality assurance [1]-[7]. An undesirable side effect to the conversion of electrical energy is the generation of harmonic content caused by non-linear loads; high-speed power electronic switching, capacitive, and inductive loading can lead to significant negative power quality implications for the utility grid [5]-[7]. Excessive heating by eddy currents from high harmonic current content can lead to premature failure of transformers. Additionally, harmful resonance interactions between equipment are possible. Furthermore, the power-supplying capacity of the electrical utility grid is reduced by excessive harmonic content, contributing to increased maintenance costs and downtime.

International standards created by the International Electrotechnical Commission such as the IEC-1000-3-2, and later adopted to regional standards as EN-61000-3-2, were created to regulate the amount of permissible harmonic content generated by electrical devices connected to the electrical grid [1]. These standards impose strict harmonic limits depending on the associated classification of the electrical device, where the classification of the device is dictated by its maximum power level. Class D devices, with their harmonic limits shown in Table 1.1, are devices that have an active power greater or equal to 600 W and meet a specific wave shape criterion.

Table 1.1 IEC-1000-3-2 harmonic limits for Class D equipment [1]

Harmonic order (n)	**Maximum permissible harmonic current per watt (mA/W)**	**Maximum permissible harmonic current (A)**
2	-	1.08
3	3.40	2.30
4	-	0.43
5		1.44
6	-	0.30
7	0.77	0.77
$8 \leq n \leq 40$ (even harmonics only)	-	1.84/n
9	0.50	0.40
11	0.35	0.33
13	0.30	0.21
$15 \leq n \leq 39$ (odd harmonics only)	3.85/n	2.25/n

Furthermore, compliance with energy performance standards such as ENERGY STAR's 80 PLUS program imposes strict limits on the minimum efficiency and power factor requirements of computer power supplies [3]. Future standards are becoming even more stringent, further encouraging advancements in energy conversion techniques.

Traditional methods of power conversion using passive components have significant difficulty, or impossibility, in meeting these standards. As such, the application of advanced switched-mode power electronic techniques through power electronic devices is necessitated. Not only do power electronic conversion techniques permit improved power quality, but also allow efficiency and transient response improvements over their passive counterparts [8].

The application of digital control devices, such as field-programmable gate arrays (FPGAs), digital signal processors (DSPs), and application-specific integrated circuits (ASIC) for power electronics control has been met with significant interest over the past decade [9]. Declining costs, faster devices, and the introduction of feature-packed digital controllers provide incentive for designers to employ digital control methods. In comparison to their analog-controlled counterparts, advantages such as reduced sensitivity to environmental variations, reduced parametric drift of passive components, and tuning simplicity make the migration of control from the analog domain to the digital domain an attractive option. Most importantly, however, digital controllers offer performance advantages that would be otherwise impossible to achieve through analog control techniques.

1.1 Power Quality

Power quality is an important concept in the design and analysis of AC-DC converters, and is the primary motivation behind this thesis. In this section, an overview of total harmonic distortion (THD) and power factor (PF) is presented. In addition, the relationship between THD and power factor, as well as the negative effects of low power factor on the power system, are shown.

1.1.1 Total Harmonic Distortion

THD is defined as the ratio of the non-fundamental rms values to the rms fundamental component. The total harmonic distortion for current is given by

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{I_{1,rms}}. \tag{1-1}$$

Requirements and regulations for the line voltage THD are strict, and a voltage THD of only 10% can cause problematic interactions with sensitive loads [5]. Since the power system supply voltage is generally well regulated and has minimum distortion, it is a reasonable to assume the input voltage is

perfectly sinusoidal to simplify analytical techniques. Input current THD, however, can easily exceed 100% depending on the load and converter used.

1.1.2 Power Factor

The ratio of real power P to the magnitude of apparent power S is defined as power factor. Real power contributes to actual work through the transfer of energy. A heater, for instance, generates heat purely through real power. Apparent power is a scalar quantity and is the product of the rms current I_{rms} and rms voltage V_{rms}, as given in (1-2). If load is purely resistive and consumes all transferred energy, its apparent power is equal to its real power. If, however, apparent power is not equal to the real power, there exist energy storage devices, such as capacitors and inductors, storing and releasing energy during the energy conversion process. If such a case, a byproduct is incomplete net energy transfer to the load.

$$S = I_{rms}V_{rms} \tag{1-2}$$

Power factor provides a dimensionless measure of useable energy efficiency, with values constrained between one and zero. This relationship is shown in equation (1-3). When the sinusoidal source voltage is perfectly in-phase with the sinusoidal source current, as in Figure 1.1, the power factor is unity.

$$\text{PF} = \frac{P}{S} \tag{1-3}$$

With unity power factor, the current drawn from the source is minimized and the load appears purely resistive from the input source, thereby enabling maximum power transfer capability. Practically, unless the load is purely resistive, unity power factor is impossible, but power factors exceeding 0.99 are achievable. If a normally non-sinusoidal load, such as a computer power supply, is controlled to draw a sinusoidal load current, this control method is called power factor correction (PFC).

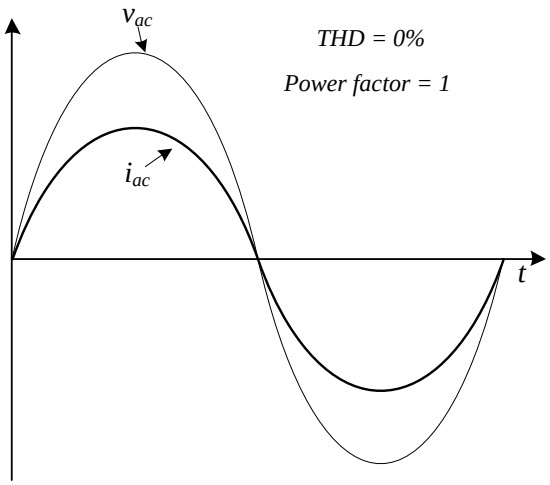


Figure 1.1 Ideal input current and voltage with unity power factor and no current distortion

There is a direct relationship between total harmonic distortion and power factor: a term called the displacement factor that relates the fundamental current phase φ_1, to the fundamental voltage phase θ_1, is defined by equation (1-4). In addition to the displacement factor, a term called the distortion factor, which relates the fundamental rms current to the total rms current, is defined by equation (1-5).

$$\text{displacement factor} = \cos(\varphi_1 - \theta_1) \tag{1-4}$$

$$\text{distortion factor} = \frac{I_{1,rms}}{I_{rms}} \tag{1-5}$$

The definition of power factor is the product of the displacement and distortion factor (1-6), and with no DC current component, as given by (1-7).

$$\text{PF} = (\text{distortion factor})(\text{displacement factor}) \tag{1-6}$$

$$\mathrm{PF} = \left(\frac{1}{\sqrt{1 + (\mathrm{THD})^2}}\right)\cos(\varphi_1 - \theta_1) \tag{1-7}$$

1.1.3 Numerical Example of the Importance of Power Factor

To illustrate the detrimental effects of poor power factor when using an uncontrolled rectifier, Table 1.2 shows the maximum real power that can be supplied to an electrical load for AC-DC rectifier power factors of 0.55 and 0.99. In Figure 1.2, a typical scheme for utility grid-tied rectification is shown. The power system AC supply provides the AC-DC rectifier with a sinusoidal voltage, where the AC-DC converter supplies its slowly regulated output voltage V_o to a high-bandwidth DC-DC converter. The DC-DC converter removes a majority of the ripple from V_o allowing a tightly-regulated voltage for the load.

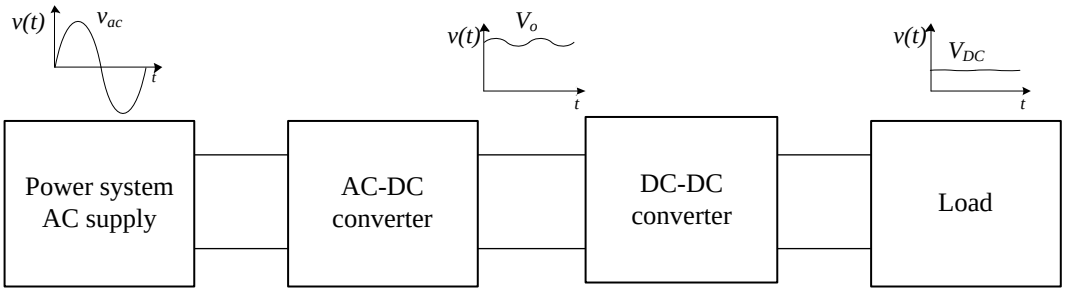


Figure 1.2 Block diagram of typical AC-DC rectification process.

As can be seen from Table 1.2, for the same input and load parameters, the maximum real power that can be supplied to the load with near-unity power factor correction is 71% greater than that of the rectifier with a power factor of 0.55. Clearly, the benefit of high power factor is of direct interest to the consumer if he or she is concerned with drawing as much real power as possible.

Table 1.2 Effect of power factor on line current and maximum power

AC Voltage	Derated Maximum Steady-State Breaker Current (15 A)	AC-DC Rectifier Power Factor	Rectifier Efficiency	Maximum Available Power
120 V	12 A	0.55	98%	776 W
120 V	12 A	0.99	98%	1325 W

1.2 Research Motivation

The objective of this thesis is to realize improvements in power quality for the AC-DC boost PFC converter by introducing a novel digital zero-current detection technique. This digital method realizes improvements over existing techniques, and is subsequently applicable to the control of the boost PFC converter, enabling enhanced power quality for boost PFC converters operating in mixed conduction mode.

1.3 Thesis Organization

This thesis is organized into five chapters. In Chapter 1, the importance and need for power quality is introduced, establishing the basis of motivation for this thesis. Chapter 2 provides a detailed literature review of uncontrolled rectifiers and a controlled rectifier topology, the boost PFC converter, along with its digital control techniques allowing realization of high-quality input current and PFC. Additionally, the differences and control implications of the continuous conduction mode and discontinuous conduction mode in the boost PFC converter is emphasized, and a highlight of existing control limitations is presented.

In Chapter 3, a detailed analysis of the implementation and design of a digital average current mode controller for the CCM boost PFC converter is presented. A 650 W boost PFC converter controlled by an analog integrated circuit is modified for digital operation and the design of the sensing and interfacing circuits is covered. Furthermore, the compensator design and implementation in a digital signal processor

are shown. Finally, the digital controller is experimentally validated showing the feasibility and success of converting an existing boost PFC converter for digital operation.

In Chapter 4, a new DSP-based discontinuous conduction mode detection (DCM) technique is proposed and its design, logic, and operation explained. The detection technique is validated with an experimental boost PFC converter and results are presented, demonstrating the effectiveness and its suitability for replacement of traditional zero-current detection circuits.

In Chapter 5, the proposed DSP-based DCM detection technique is applied to realize an adaptive controller capable of realizing improved control of the boost PFC converter in mixed conduction mode. The design of the DCM compensator is presented, along with experimental validation showing the improvements to harmonic distortion and power factor over conventional digital and analog control techniques.

Chapter 6 summarizes the contributions of this thesis and provides possible areas of future work and improvement for applications of digital control for power factor correction.

2 Literature Review

This chapter provides a detailed review of the fundamental operation and dynamic characteristics of the most popular power electronics topology used for AC-DC rectification, the boost PFC converter, as well as highlighting the limitations of conventional rectifiers. Existing digital control techniques used for active power factor correction under mixed conduction mode operation is also reviewed, with their benefits and limitations explained. Furthermore, the most common methods to detect zero inductor current are presented, along with their advantages and disadvantages. This chapter serves in establishing further motivation for the need of improvements in the realization of power quality by improving on the shortcomings of existing control methods.

2.1 Passive AC-DC Conversion Topologies

The objective of this section is to provide a concise summary of the methodologies and problems associated with uncontrolled passive AC-DC rectification circuits. The performances of the basic uncontrolled full-wave rectifiers are presented and their limitations in terms of THD and power factor are shown.

2.1.1 Uncontrolled Full-wave Rectifier with Capacitive Filtering

The uncontrolled rectifier shown in Figure 2.1 is one of the basic circuits used as a means of providing AC-DC rectification [8].The uncontrolled full-wave rectifier is an effective and inexpensive circuit to provide a DC voltage from an AC source. It has a low component count and no need for a complicated control circuit.

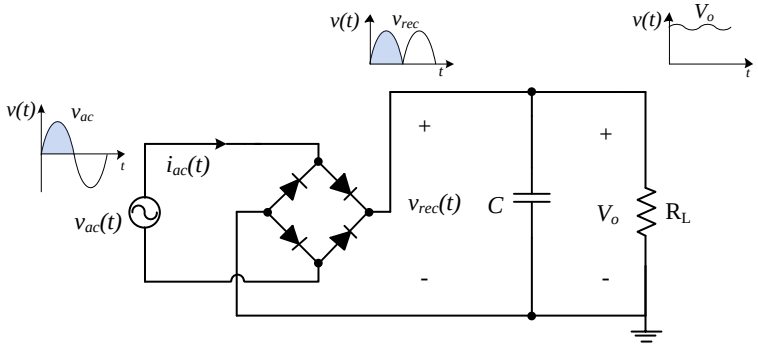


Figure 2.1 Uncontrolled full-wave rectifier.

The input voltage v_{ac} is fed into an uncontrolled full-wave rectifier diode bridge for rectification to DC form. A large filter capacitor is added after the input diode bridge to minimize the output voltage ripple, resulting in a DC voltage V_o. During the times when V_o is greater than v_{ac}, the diodes are reverse-biased and do not conduct. During this mode of operation, the rectifier functions as a peak detector. When V_o is less than v_{ac}, the forwardly-biased diodes conduct, leading to very high peak and rms currents as the filter capacitor is charged. THD levels in the input current i_{ac} are high, leading to a poor power factor as shown in Figure 2.2 (a), where i_{ac} is nearly pulsed in shape.

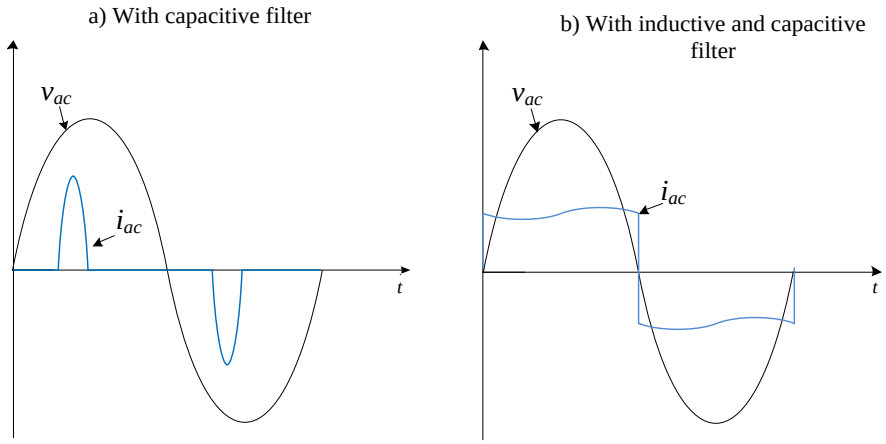


Figure 2.2 Line voltage v_{ac} and distorted line current i_{ac} of uncontrolled full-wave rectifier with: a) capacitive filter and b) inductive and capacitive filter.

2.1.2 Uncontrolled Full-wave Rectifier with Capacitive and Inductive Filtering

A modification to this topology exists with the addition of a large filter inductor immediately following the diode bridge, as illustrated in Figure 2.3. This large inductor forces the input current to be continuous over the half-line cycle without large current peaking, as is the case of uncontrolled rectifier with capacitive filter. The waveforms for this converter are shown in Figure 2.2 (b). Although the input current is continuous, the power factor and THD are again unacceptable in meeting the EN-61000-3-2 standards. Furthermore, due to the low line frequency AC input, the physical size of the inductor is made impractically large and expensive for many applications.

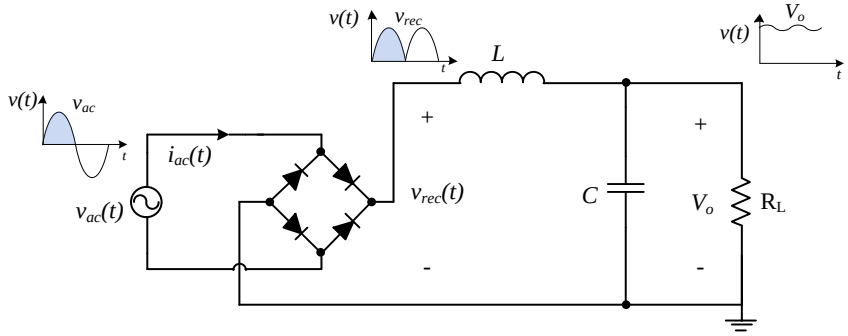


Figure 2.3 Uncontrolled full-wave rectifier with inductive filter.

Generally, the uncontrolled full-wave rectifier is not suitable for power levels exceeding 50 W due to the low power factor, high harmonic currents and significant reduction in maximum available power deliverable to its load. Other passive filtering techniques are possible but suffer from inflexibility when load and input conditions change, large volume and size, as well as high cost [6]. Significant benefits can be realized through active power factor correction by allowing considerably greater real output power.

2.2 Boost PFC Converter

The boost PFC converter is the most popular circuit used for active power factor correction, and is illustrated in Figure 2.4. This circuit has been extensively studied and its control and performance characteristics are widely known [10]-[17]. The primary advantages of the boost PFC converter include its low cost and complexity. In its simplest form, only one active switch and only one diode are required for operation. One advantage of the boost PFC converter is high switching frequencies, allowing a reduction in the physical size of capacitors and inductors. Switching frequencies are approximately three orders of magnitude larger than the line frequency i.e. in the range of 60 kHz versus the 60 Hz line frequency. Additionally, as the ac line input voltage is always coupled to the output ground, the input voltage and input current sensing is facilitated [19].

Essentially, the PFC boost converter is a boost converter from the DC-DC converter family preceded by a rectifier bridge. The input voltage is rectified, processed, and fed to the subsequent stage, or load. The sinusoidal ac line voltage v_{ac} is given by,

$$v_{ac}(t) = V_M \sin(2\pi f_{line} t), \tag{2-1}$$

with a peak component of V_M and with a frequency of f_{line}. v_{ac} is fed through the bridge rectifier generating the rectified voltage v_{rec}.

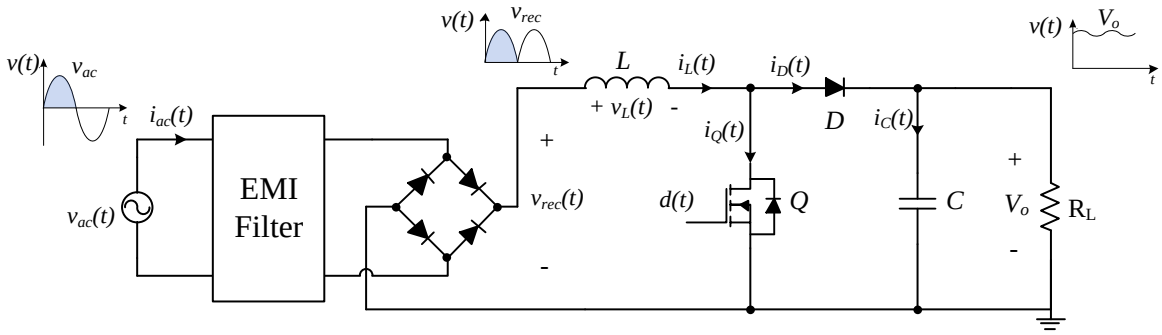


Figure 2.4 Boost PFC converter. DC-DC boost stage is preceded by bridge rectifier, allowing AC-DC rectification and PFC through modulation of switch *Q*.

Since the rectified voltage has an instantaneous value dependent on its frequency-time product, a variable duty cycle is needed to maintain the output voltage V_o. For a constant output voltage V_o, the required duty cycle d of the boost PFC converter is given by

$$d(t) = 1 - \frac{\sqrt{2} v_{ac}(t)}{V_o}. \tag{2-2}$$

The objective of power factor correction is to have a sinusoidal input current i_{ac}, in-phase with the input voltage and free of harmonics. This objective is accomplished by control of the inductor current i_L. Without additional modification, the control law of (2-2) is inadequate in providing direct sinusoidal control over the shape of the input current. Power factor correction control techniques are described in Sections 2.2 and 2.3 to compensate for this limitation.

2.2.1 Operation of the PFC Boost Converter

During an input voltage positive half-cycle with switch *Q* closed and diode *D* reverse-biased, current flows through the rectifier bridge, through the inductor *L*, through switch *Q*, and finally returning to the ac source through the rectifier bridge. This current flow is illustrated in Figure 2.5.The duration of the period where *Q* is closed, T_{on}, is a product of the duty cycle *d* and switching period T_{sw}. Energy is stored in *L* during this time, and capacitor *C* discharges, supplying energy to the load.

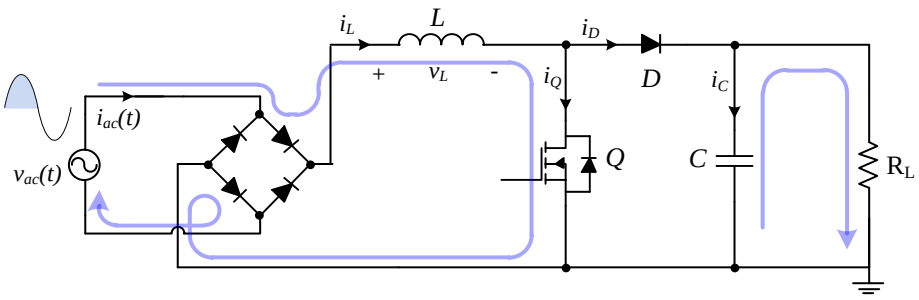


Figure 2.5 Positive line input half-cycle operation of the PFC boost converter with switch *Q* closed. Inductor *L* is storing energy and output capacitor *C* is discharging energy to load.

In the same half-cycle, but now with *Q* open corresponding to period T_{off}, current continues to flow through the rectifier bridge and through *L*; however, now that *Q* is open, the inductor is supplying energy to the load and charging *C* at a voltage greater than the input line voltage. The current returns to the source via the rectifier bridge. The process is illustrated in Figure 2.6.

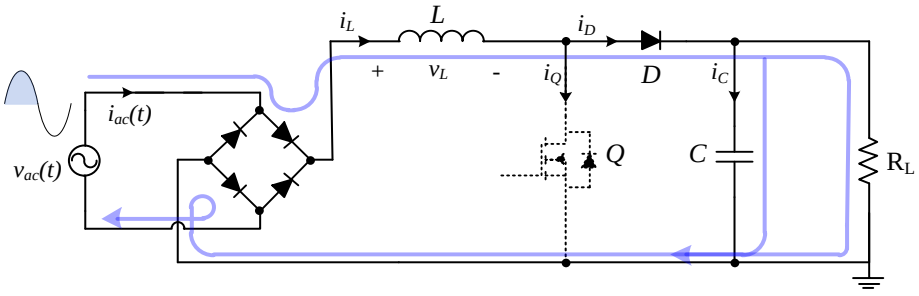


Figure 2.6 Positive line input half-cycle operation of the PFC boost converter with switch *Q* closed. Inductor *L* is storing energy and output capacitor *C* is discharging energy to load.

Detailed waveforms for the positive half-cycle operation are shown in Figure 2.7. It is worth noting that during a negative half-cycle, the converter operation is identical, with the exception of current flow through the rectifier bridge.

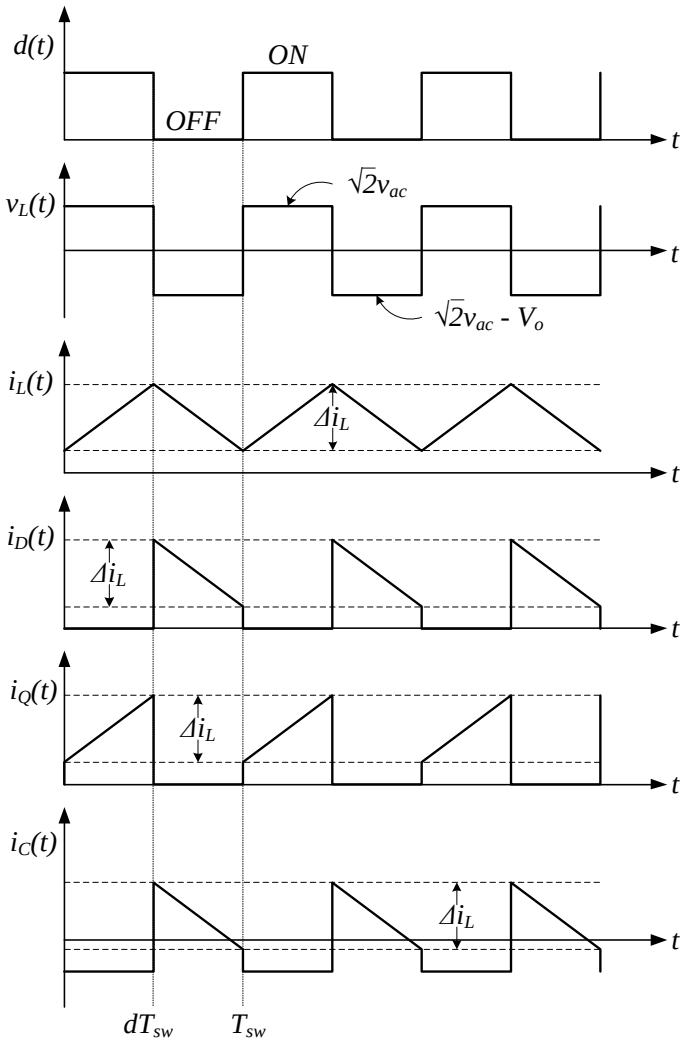


Figure 2.7 Waveforms of boost converter during positive line input half-cycle

2.2.2 Power Factor Correction with the Boost PFC Converter

With proper control of switch *Q*, the input current i_{ac} can be made sinusoidal and in-phase with input voltage v_{ac} [10]. Instead of controlling the duty cycle to achieve a constant V_o, the duty cycle should be

controlled to give an average inductor current I_L that is linearly proportional to the input voltage. Intrinsically, it is desirable to control not the immediate inductor current, but to control I_L over a single switching period. An EMI filter effectively removes the switching ripple from i_L, as seen in Figure 2.8, such that the input to the boost PFC converter sees only the power-factor-corrected line current i_{ac}.

Assuming unity power factor, the boost PFC converter can be considered as a lossless resistor R_e [8]. This matches the definition of power factor, as the PFC circuit should appear as an emulated resistance where all power is supplied to its load, and no power is consumed during the intermediate conversion stage. Thus, the following relationship can be defined:

$$R_e = \frac{v_{ac}(t)}{i_{ac}(t)}. \tag{2-3}$$

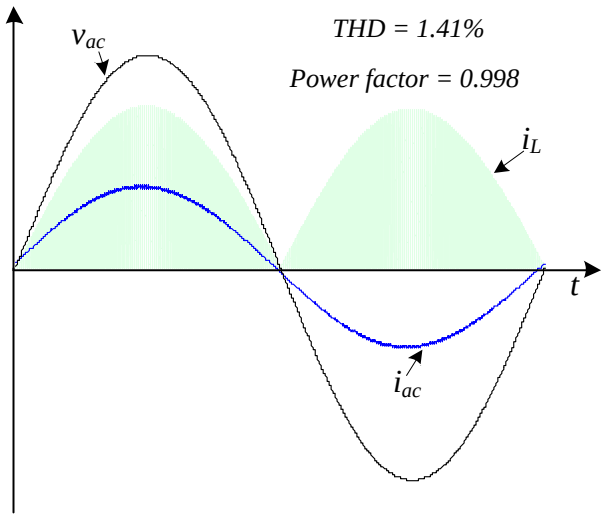


Figure 2.8 Illustration of power factor correction and effect of EMI filtering circuit on line current i_{ac}, representing averaged inductor current I_L over a switching period.

2.2.3 Types of Inductor Current Modes

There are three separate modes of operation for the boost PFC converter, where each mode is determined by the behavior of the inductor current during a single switching cycle, and with each mode having significantly different dynamic considerations. The modes are continuous conduction mode (CCM), boundary conduction mode (BCM), and discontinuous conduction mode (DCM). Each mode is presented in detail in the following sub-sections.

2.2.4 Continuous Conduction Mode

When the boost converter inductor current i_L remains above zero for the entire switching period T_{sw}, the boost PFC converter is said to be operating in continuous conduction mode (CCM). This mode of operation is illustrated in Figure 2.9. Continuous conduction mode is common for power levels exceeding 300 W, as component stresses are minimized and the design of the EMI filter is simplified [14]. Operation in CCM is satisfied if the boost PFC converter obeys the following relationship:

$$R_e < \frac{2L}{T_{sw}(1-\frac{v_{rec}}{V_o})}. \tag{2-4}$$

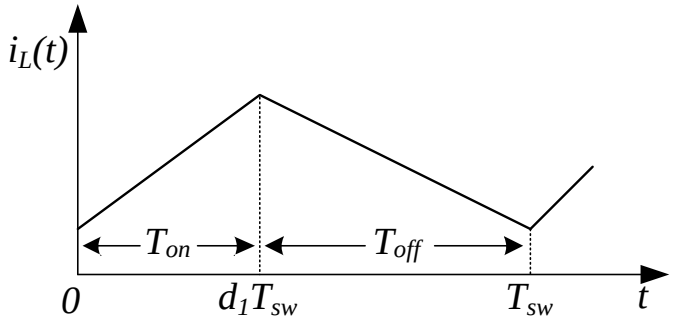


Figure 2.9 Boost PFC inductor current waveform in continuous conduction mode.

A disadvantage of the CCM boost PFC converter is the need for a more complicated PFC controller when compared to BCM and DCM control.

2.2.5 Boundary Conduction Mode

If i_L reaches zero during T_{off} but does not remain at zero for the remaining portion of T_{sw}, the boost PFC converter is said to be operating in boundary conduction mode (BCM). Boundary conduction mode is common for power levels less than 300 W since diode reverse recovery losses are drastically reduced or eliminated due to zero-current switching [8]. The disadvantage of this mode is the increased device stress and the need for a variable switching frequency, which can complicate the design of the EMI filter [19]. Operation in BCM is satisfied if the boost PFC converter obeys the following relationship:

$$R_e = \frac{2L}{T_{on}}. \tag{2-5}$$

The operation over a single switching period is shown in Figure 2.10. As in CCM, the inductor current i_L increases in a linear fashion during the energy storage period d_1T_{sw}. As energy transfers to the load during the T_{off} period, the current reaches zero and the switch Q is immediately turned on at this point, giving the variable switching period T_{sw}.

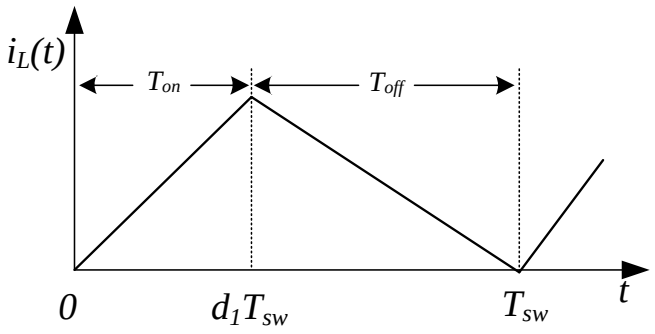


Figure 2.10 Boost PFC inductor current waveform in boundary conduction mode

An inherent advantage of the BCM boost PFC converter is a simple PFC controller scheme. Since Q should be turned on the moment the inductor current reaches zero, only an outer voltage control loop and a zero-current detection circuit are needed to realize PFC [8].

2.2.6 Discontinuous Conduction Mode

If i_L reaches zero and remains, ideally, at zero for the remaining duration of the switching period, the boost PFC is said to be operating in discontinuous conduction mode (DCM). DCM waveforms are illustrated in Figure 2.11. Operation, as in BCM operation, is generally reserved for low power levels due to increased peak currents and greater filtering requirements [8]. The advantage of this mode is that it does not necessarily require variable switching frequencies, thereby simplifying the design of the EMI filter. An important phenomenon is present with the boost PFC converter in DCM mode: at period d_2T_{sw}, the inductor current reaches zero, and oscillates at a frequency given by

$$\omega_n = \frac{1}{\sqrt{LC_n}}. \tag{2-6}$$

The oscillation is a result of the parasitic capacitances, C_n from the switch and output diode, leading to a resonant interaction with the boost inductor L [24]. This period is referred to as the DCM period T_{DCM}, and has important sensing considerations, as will be highlighted in Chapter 4.

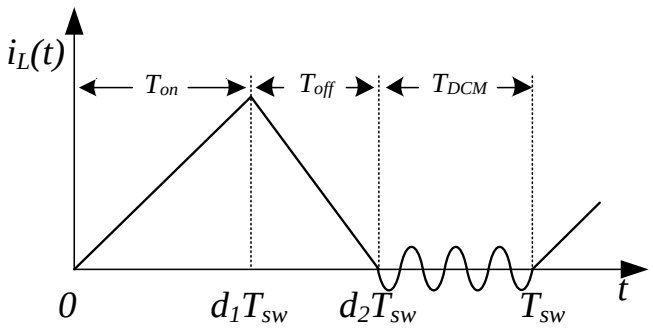


Figure 2.11 Boost PFC inductor current waveform in discontinuous conduction mode.

The boost PFC will operate in DCM if its emulated resistance follows the relationship

$$R_e > \frac{2L}{T_{sw}\left(1 - \frac{V_M}{v_o}\right)}. \tag{2-7}$$

2.2.7 Small-signal Models for the CCM and DCM Boost PFC Converters

To characterize the dynamic properties of the boost PFC converter under CCM and DCM operation, it is necessary to know the effects of duty cycle d on inductor current i_L. Although the boost PFC does not have a static quiescent operating point due to the low frequency input voltage, a linearized plant model can be found applying averaging techniques [8][51].With averaging, the control-to-output transfer function of the boost PFC converter is given by

$$G_i^{CCM}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}(s)} = \frac{V_o}{sL}. \tag{2-8}$$

Similarly, the control-to-output transfer function of the DCM boost PFC converter was derived in [23], and is given by

$$G_i^{DCM}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}(s)} = \frac{\frac{2V_o}{L}}{s + \frac{2f_s(V_o - V_M)}{dV_M}}. \tag{2-9}$$

By comparing equations (2-8) and (2-9), it is evident that there are significant dynamic differences between the CCM and DCM boost PFC converters. Frequency responses for DCM and CCM boost PFC converters (L = 200 µH, f_s = 130 kHz, V_o = 390 V, d = 0.1297, V_M = 340 V) are shown in Figure 2.12, further exemplifying this difference.

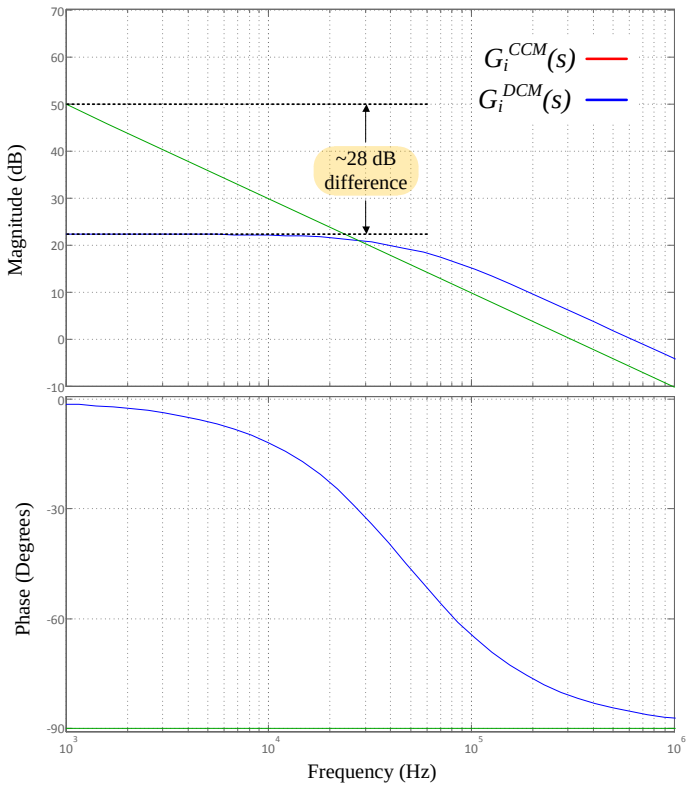


Figure 2.12 Open-loop DCM and CCM control-to-output frequency responses for the boost PFC converter (L = 200 µH, f_s = 130 kHz, V_o = 390 V, D = 0.1297, V_M = 340 V).

2.2.8 Mixed Conduction Mode

When the boost PFC converter operates in both CCM and DCM during a single line cycle, it is said that the boost PFC is operating in the mixed conduction mode (MCM). Waveforms are provided in Figure 2.13. In power factor correction applications, a boost PFC converter designed for CCM operation will exhibit DCM operation near the zero crossings of the input voltage and/or at low output power. Furthermore, as most boost PFC converters are designed for a universal input voltage range (85 – 264 V), the lower input currents at higher voltages will increase the portion of time spent in DCM. Previously shown, the small-signal characteristics of the CCM boost PFC and DCM boost PFC converters are vastly different. If a boost PFC converter designed for CCM operates in DCM, the converter may exhibit

instability, greater THD, and poor power factor [22][23]. If a boost PFC converter designed for general CCM operation employs a DCM control technique during its periods in DCM, otherwise known as MCM, improvements in THD and power factor will be achieved. Therefore, a converter that operates in MCM must be designed with CCM and DCM control considerations if good power quality is desired.

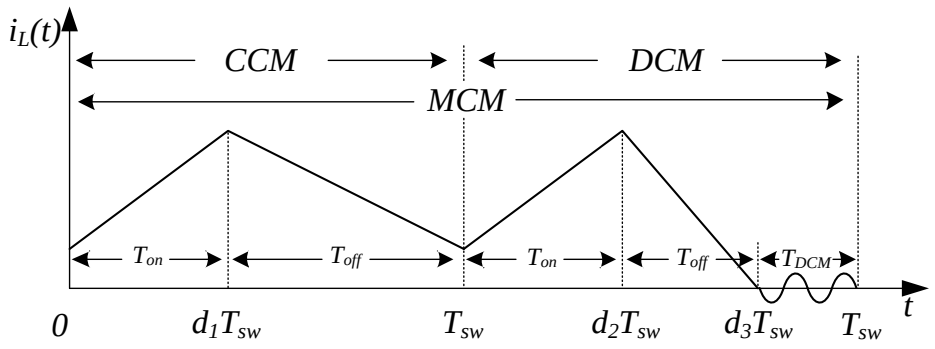


Figure 2.13 Illustration of boost PFC inductor current operating in both CCM and DCM, corresponding to mixed conduction mode (MCM) operation.

2.3 Review of Boost PFC Digital Control Techniques

Achieving low THD and high power factor requires the application of control theory to the boost PFC converter. A number of control methods have been developed and applied to the boost PFC to realize performance improvements and/or simplification of the controller design. Although some control methods give primary importance to the outer voltage loop for improved output voltage transient response [20][21], most research has focused on the inner current loop, allowing direct improvements in THD and power factor [22]-[48].

This section provides a review of the most popular digital control methods used with the boost PFC converter under MCM operation.

2.3.1 Average Current Mode Control

Average current mode control is one of the most popular methods for achieving low distortion and high power factor in boost PFC converters [28]. Its high-level system diagram when applied to the boost PFC converter is shown in Figure 2.14. Several commercially available integrated circuit (IC) control chips employ average current mode control as the control architecture [29][30].

The principle of average current mode control is to control the average inductor current I_L to be proportional to the rectified input voltage. The inductor current is sensed through a current sense series resistor, and the resulting voltage drop across the resistor is amplified and sensed by digital device. Input and output voltages are sensed as well, typically by simple voltage divider networks. By separating the control architecture into two separate loops, a high-bandwidth inner current loop and low-bandwidth outer voltage loop, both PFC and output voltage regulation is obtained.

The bandwidth of the inner current loop is commonly selected to be $1/10^{th}$ to $1/6^{th}$ the switching frequency e.g. 6 - 10 kHz for a 60 kHz switching frequency, and the outer voltage loop's bandwidth is restricted to a range typically less than 20 Hz [18]. The presence of a second harmonic component in the instantaneous output power (2-10) requires a low-bandwidth controller to avoid introducing harmonics into the line current.

$$p(t) = \frac{v_{ac}^2}{R_e v_c(t)}(1 - cos(2\omega t)) \tag{2-10}$$

The advantages of digital average current mode control are good dynamic performance allowing low harmonic distortion, robustness, and simplicity. Additionally, digital average current mode control can be applied to other topologies, such as the buck converter, SEPIC, buck-boost, among others [8]. The disadvantages of digital average current mode control are demanding computational requirements at higher converter switching frequencies; however, with the introduction of more affordable and faster

microprocessors, DSPs, and field-programmable gate arrays (FPGAs), this computational requirement is of less importance today than in previous years.

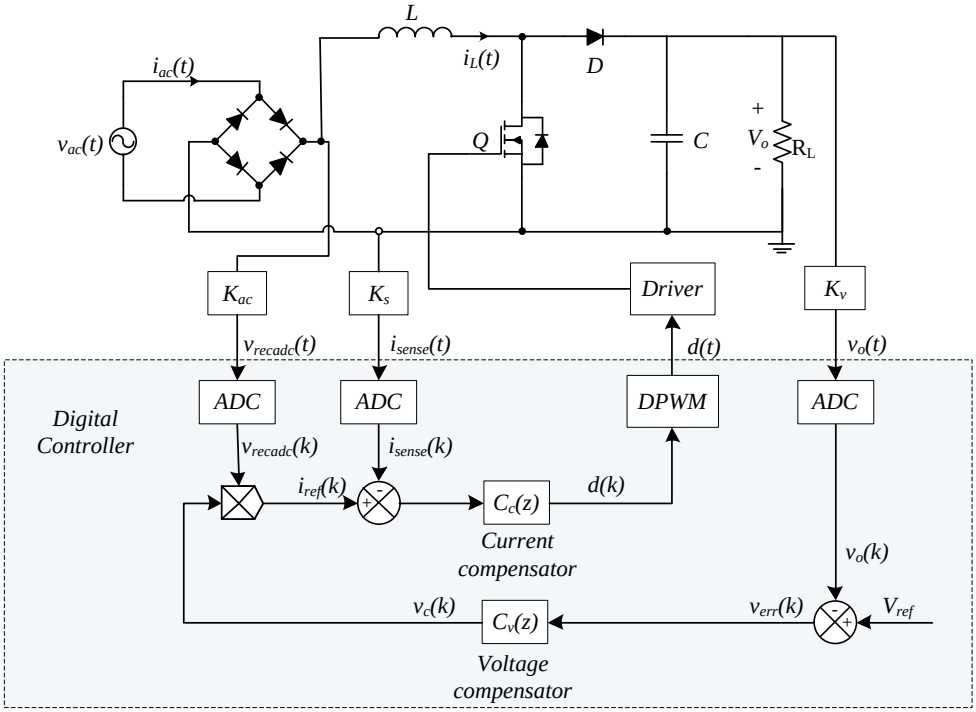


Figure 2.14 Digital implementation of average current mode control for boost PFC converter.

2.3.2 Average Current Mode Control with Voltage Feedforward

A modification to average current mode control is obtained by including the line voltage in the control loops, referred to as input voltage feedforward [8][24],[28]-[43]. The boost PFC converter and average current mode control with voltage feedforward is shown in Figure 2.15. Any disturbances in the line voltage are immediately compensated, providing the output voltage V_o with greater immunity to ac line variations. Several modifications exist [28]-[43], however, the simplest digital implementation is to compute the average of the rectified input voltage v_{rec} and incorporate it into the calculation of the control variable. A disadvantage is the need for a division operation, which may command many instruction cycles on a digital device [55].

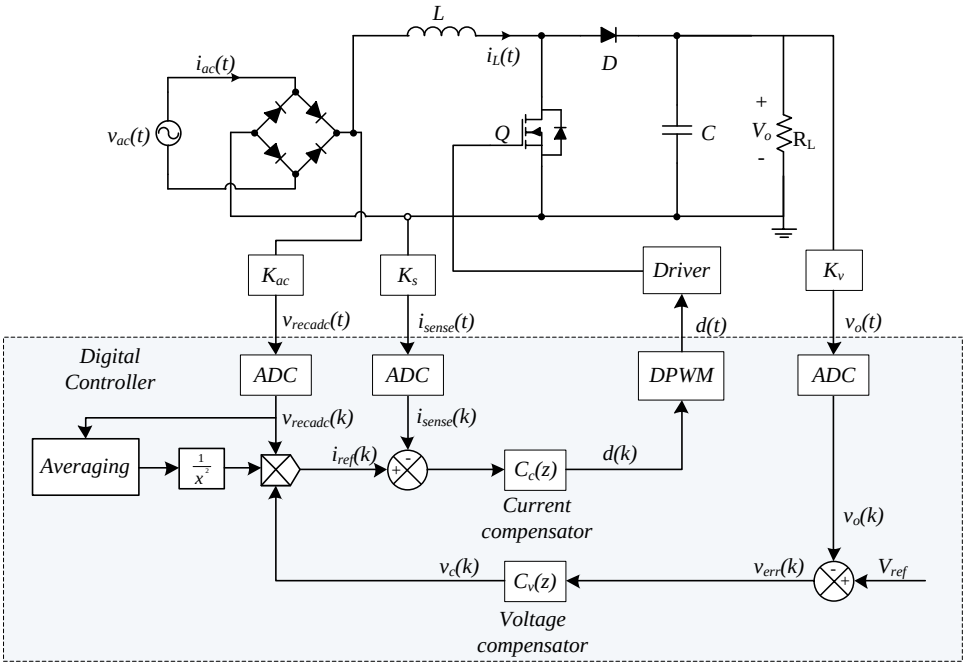


Figure 2.15 Voltage feedforward added to digital average current mode control for boost PFC converter to compensate for variations in line voltage v_{ac}.

2.3.3 Average Current Sampling

An inherent advantage of digital control is the ability to sense the average inductor current by sampling in the middle of the rising or falling inductor current slope [35][38]. Through geometrical symmetry, the sensed current in CCM is approximately equal to the average current, and this avoids the need for low-pass averaging circuit or further processing to extract the average inductor current. The sampling principle is illustrated in Figure 2.16. In DCM, however, the average inductor current is no longer given by sampling in the middle of the rising or falling inductor current slope, and other methods must be used to extract or sample the average inductor current [36][42].

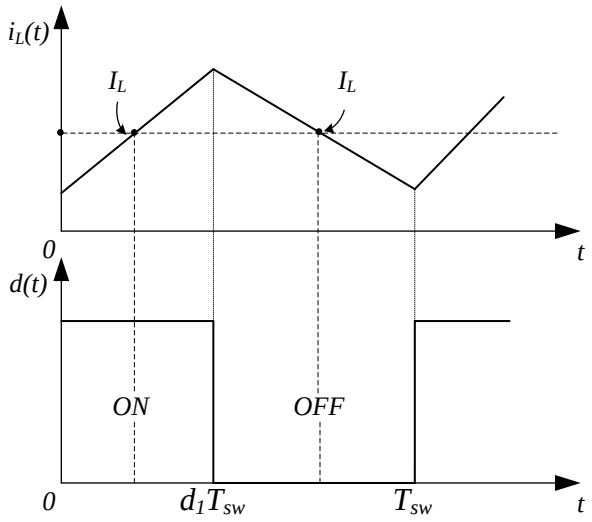


Figure 2.16 Illustration of digital sampling points on middle of rising or falling inductor current slope i_L, giving inherent average inductor current I_L in CCM operation.

2.3.4 DCM Detection Methods and Mixed Conduction Mode Techniques

Employing auxiliary analog circuits to monitor the boost inductor voltage is a widespread method for detecting zero current [33][48][50]. Among the most popular methods is through the sensing of the instantaneous inductor voltage v_L [33][50]. Using a second inductor, coupled with the boost PFC inductor as an auxiliary winding, zero current can be inferred when the potential difference across the auxiliary inductor v_{aux} becomes zero. A significant disadvantage of this method is the need for an auxiliary winding on the boost inductor, as well as additional passive components, leading to increased size and cost. If the leakage inductance is high, a passive RC snubbing circuit is required to limit potentially damaging inductive spiking. Furthermore, replacing existing windings with multi-winding inductors is impractical if the power stage design, analysis, and layout is already complete.

A method employed by a commercial IC for detection of zero current and control of a BCM boost PFC converter [33] is shown in Figure 2.17. The series resistor R_{ZCD} limits the current to the comparator logic, while capacitor C_{ZCD} provides increased noise immunity. A threshold for zero-current detection is

provided by the positive input to the comparator by $V_{TH\ ZCD}$, while clamping circuitry for positive and negative voltages is also employed. Additionally, analog THD optimization circuitry is used to obtain added performance advantages at the cost of increased complexity. Evidentially, the increased component count and complexity of the analog zero-current detection logic further drive the need for a simpler and more efficient detection method.

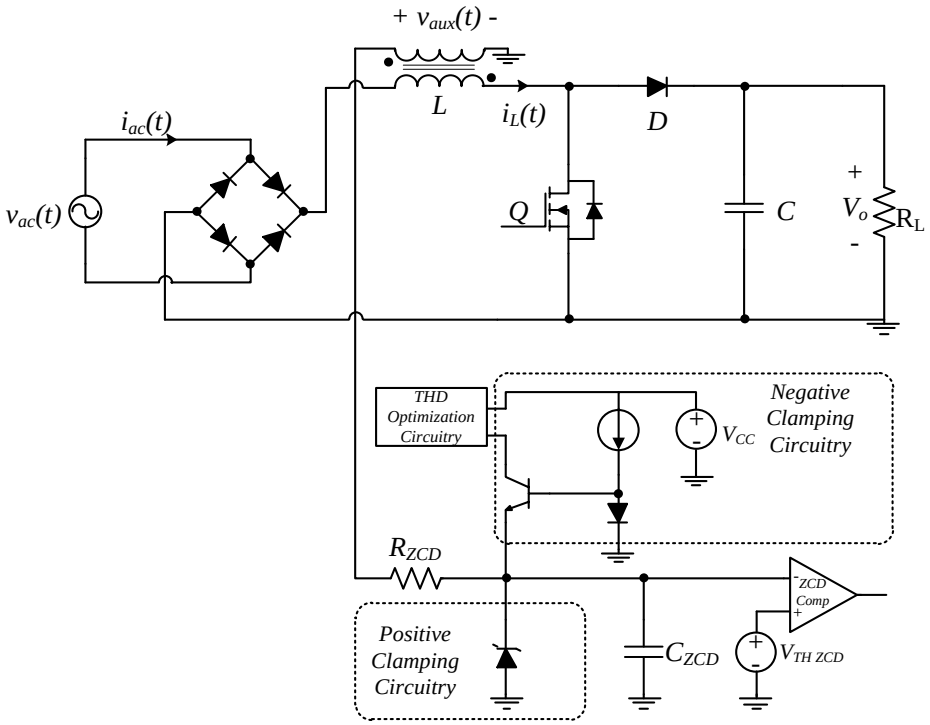


Figure 2.17 Secondary winding applied to boost PFC converter for zero current detection as given in [33]. Additionally clamping circuitry for improved noise immunity is shown.

An alternative option for zero-current detection is to sample continuously the sensed inductor current until zero current is reached. With the majority of boost PFC converters switching in the range of 20-130 kHz, extremely fast analog-to-digital converter (ADC) sampling rates are needed; the processing and cost requirements make this method practically unreasonable.

By determining when the load current reaches a specified value, as proposed in [48], DCM operation is detected and the digital control law is adjusted. Sensing the load current, however, results in efficiency penalties as well as the need for two external comparators and a logical AND gate.

Numerical detection of the DCM boundary is also possible, but with increased sensitivity to passive component tolerances. A DSP-based DCM detection method is presented in [45], which decides the mode of operation based on a comparison of inductor current samples in both the T_{off} and T_{on} periods. From the symmetry of the CCM and BCM current waveforms, if the two samples are approximately equal during a single switching period, the converter is operating in CCM or BCM. If, however, the current sample during the T_{on} period is greater by a configured amount than the sample during the T_{off} period, DCM operation is presumed. Although this method removes the need for an on-board comparator, there are some important disadvantages. Firstly, the inductor current slew rate is a function of the inductance of the converter, and since the inductance of the boost converter does not remain constant during an entire line cycle [46], the slew rate is variable requiring a larger sample comparison interval. Consequently, the detection logic may exhibit increased inaccuracy at certain periods of the line cycle, resulting in a misdetection of the DCM region. Furthermore, as two inductor current samples are required in a single period, there is a need for increased ADC processing requirements. Moreover, around when v_{ac} reaches zero, the duty cycle approaches 100% and the period T_{off} becomes small, allowing possible corruption of the sampled signal by switching noise.

In [25], a DSP provides DCM detection and appropriate MCM control depending on the detected mode. A critical boundary condition K_{crit} is defined as

$$K_{crit} = D_{DC}(1 - D_{DC})^2 , \tag{2-11}$$

where D_{DC} is the computed DC duty cycle of the switch. To determine the type of inductor operation, K_{crit} is compared to another term K (2-12) , whose value is dependent on the boost inductance L, switching period $T_{sw,}$ and load resistance $R_{L.}$

$$K = \frac{2L}{T_{sw}R_L}, \tag{2-12}$$

If $K_{crit} > K$, the converter is operating in DCM, and CCM when $K_{crit} < K$. If $K_{crit} = K$, the converter is operating in BCM. This detection mode has immediate disadvantages due to the requirement of prior knowledge of the boost inductance, output and input voltages, as well as inductor current. Furthermore, the division operations for computation of D_{DC}, R_L, and K are computationally intensive and therefore limit the maximum possible switching frequency. Unfortunately, no THD or power factor experimental number validations are provided to demonstrate the effectiveness of the proposed method. Rather, transient responses of input current and output voltage to step changes in output power are given.

In [39] and [40], an auto-tuning approach is presented for MCM control. To compensate for tolerances in the boost inductance, an FPGA is used to monitor and inject perturbations into the control loops, allowing a more accurate numerical computation of the DCM boundary. Analysis of the injected perturbations provides an estimate of the actual inductance and output capacitance, where the inductance is used to determine the mode of operation. When equation (2-13) is equal to the rectified line voltage, the DCM boundary has been detected.

$$v_{rec} = \left(1 - \frac{2L}{T_{sw}}\left(\frac{v_c}{V_M^2 K_{ac}}\right)\right)V_o. \tag{2-13}$$

Following the determination of the operating mode, either an automatically tuned CCM or DCM proportional-integral (PI) compensator is applied to realize improvements in power quality with system identification methods. Results demonstrate excellent THD and power factor, with the disadvantage of

significantly increased computational requirements. Observing (2-13), the boundary detection condition is computationally demanding due to the multiple division and multiplication operations. Furthermore, the control technique has added complexity from the system identification auto-tuning. Finally, an additionally disadvantage of this method is the need for an auxiliary signal injection circuit.

Feedforward control for MCM converters was proposed in [23] and [37], and later adapted for predictive control [30]-[32] in [41]. The proposed feedforward control from [23] requires the comparison and selection of two separate feedforward actions, either the DCM or CCM duty cycle, to determine the appropriate control method. Upon computation of the two feedforward terms, the selection of the minimum term provides applicable control for either CCM or DCM, thereby decreasing THD and increasing power factor. The feedforward duty cycle is summed with the duty cycle output of the current compensator, giving a final duty cycle applicable to PFC control of the boost PFC converter. The predictive control modification proposed in [41] decreases the number of cycles required for computation of the control law, increasing the maximum possible switching speed. A drawback of these feedforward control methods is the need for two separate feedforward term computations, even though only one is summed to the final duty cycle. Furthermore, the DCM duty cycle feedforward term requires both division and square root operations, increasing the number of instruction cycles.

The average current of the DCM inductor current waveform is not represented solely by its midpoint-sampled value, and without the true average inductor current, average current mode control in DCM employs an erroneous average inductor current. A correction factor κ was proposed in [36], which modifies the sensed current through knowledge of R_e, v_{rec}, V_o, L, and T_{sw}. The expression for the correction factor is given in (2-14). Good performance in THD and power factor over its uncorrected version for the MCM boost PFC converter was observed.

$$\kappa = \sqrt{\frac{2L}{T_{sw}R_e}\left(\frac{V_o}{V_o - v_{rec}}\right)} \tag{2-14}$$

The authors in [42] approach the control of the MCM boost converter by using an auxiliary winding and voltage comparator to measure the DCM period T_{DCM}. With a modification of the current correction factor κ, proposed in [36], the authors simplify the computation of κ by utilizing T_{DCM} to compensate for the midpoint-sampled inductor current slope in DCM operation. The modified expression for κ is given in (2-15). Additionally, more accurate average inductor current in the DCM period detection is provided over (2-14), as (2-15) eliminates the errors introduced by tolerance variability of L. With knowledge of the true average current, adaptive and predictive control techniques are used to realize efficiency and harmonic improvements over traditional average current mode control.

$$\kappa = 1 - \frac{T_{DCM}}{T_{sw}} \tag{2-15}$$

2.4 Summary

This section presented an overview of circuits and control techniques to rectify an AC voltage into a DC voltage. The limitations of passive AC-DC rectifiers, giving high THD and low power factor contributing to poor power quality, was shown and further motivated the necessity of power electronic devices to realize high power quality through power factor correction. Specifically, the boost PFC converter topology was presented along with its operation and most common control technique, average current mode control.

The various modes of inductor current operating during a single switching cycle leading to substantially different control dynamics was explained. At higher power, continuous conduction mode (CCM) is preferred due over discontinuous conduction mode (DCM) due to its reduced component stress. DCM operation is preferred for lower powers as elimination of reverse recovery losses is possible. In PFC

applications, the boost PFC converter operates in both DCM and CCM during a single line cycle, which is known as mixed conduction mode (MCM). MCM boost PFC converters will display increased harmonic distortion and poorer power factor if not properly compensated.

An investigation into existing MCM control methods and zero current detection methods was provided, specifically highlighting their shortcomings and advantages. Digital MCM control methods allow for increased flexibility in the design and performance of boost PFC converters. Present zero current detection methods, such as the one in [33] employ expensive auxiliary circuits to detect the point of zero inductor current during a switching period, and fail to make optimal use of the digital computational resources. Other detection methods, such as the ones proposed in [25] and [45], are computationally demanding and sensitive to component tolerances. MCM control techniques such as the ones in [39] and [41], suffer from demanding computational requirements.

Using a boost PFC converter modified for digital operation, detailed in Chapter 3, Chapter 4 presents a new DSP-based DCM detection method to alleviate the aforementioned zero current detection problems. Chapter 5 provides a new digital adaptive control method to realize lower THD and higher power factor for the MCM boost PFC converter by expanding upon the research completed in Chapters 3 and 4.

3 Digital Design Considerations for the Modification of an Analog IC-controlled Boost PFC Converter

3.1 Overview

A designer may wish to experiment with digital control to evaluate the performance advantages over traditional analog control techniques. It can be costly to re-design an existing product for digital control evaluation; hence, there is an interest to realize a digitally controlled prototype with minimal modification to the existing power electronic device. The purpose of this chapter is to provide a detailed guide to not only the software aspect, but to outline and describe some practical requirements of analog interfacing requirements, digital control, and other digital design aspects, when converting an analog IC-controlled boost PFC converter to a digitally controlled equivalent.

The control of power electronics in the continuous domain, or analog domain, makes use of passive and active components such as resistors, capacitors, and operational amplifiers to achieve the desired control objectives [51]. With these analog components, it is possible to construct an analog filter allowing shaping of the desired closed-loop response of the power electronic device. Digital controllers, on the other hand, operate in the discrete domain under the similar frequency-shaping principles, but in place of the passive and active components of the analog domain, a digital filter is used to shape the frequency response of the power electronic device. This digital controller, or filter, must be implemented using digital arithmetic and memory with finite sampling and computation rates; thus, several important factors emerge when converting a boost PFC converter to a digitally controlled equivalent.

Section 3.2 provides a detailed guide of the analog signal sensing, along with practical requirements to achieve high-quality control variable sensing for the boost PFC converter using a Texas Instruments TMS320F28035 DSP [53]. A detailed guide to the selection of component values for the input and output voltage sensing networks, as well as the current sense amplifier network for interfacing to the analog-to-

digital (ADC) converters is presented. In Section 3.3, the design of the digital compensator for the CCM boost PFC converted is presented, along with simulation results verifying its current-tracking ability. Section 3.4 provides the high-level system diagram of a boost PFC converter with digital average current mode control with voltage feedforward. The digital filter structure of the voltage and current compensators is presented, with provisions made for implementation of digital voltage feedforward. As well, the main interrupt service routine is presented with its operational fundamentals. Finally, Section 3.5 presents experimental results showing the successful digital conversion of the modified boost PFC converter, along with a summary in Section 3.6.

3.2 Analog-to-digital Interfacing Sensor Design

This section provides an overview of the design requirements of the input voltage, output voltage, and current sensors for the boost PFC converter. The input and output voltage sensing networks and the inductor current active sensing network for the boost PFC converter are shown in Figure 3.1.

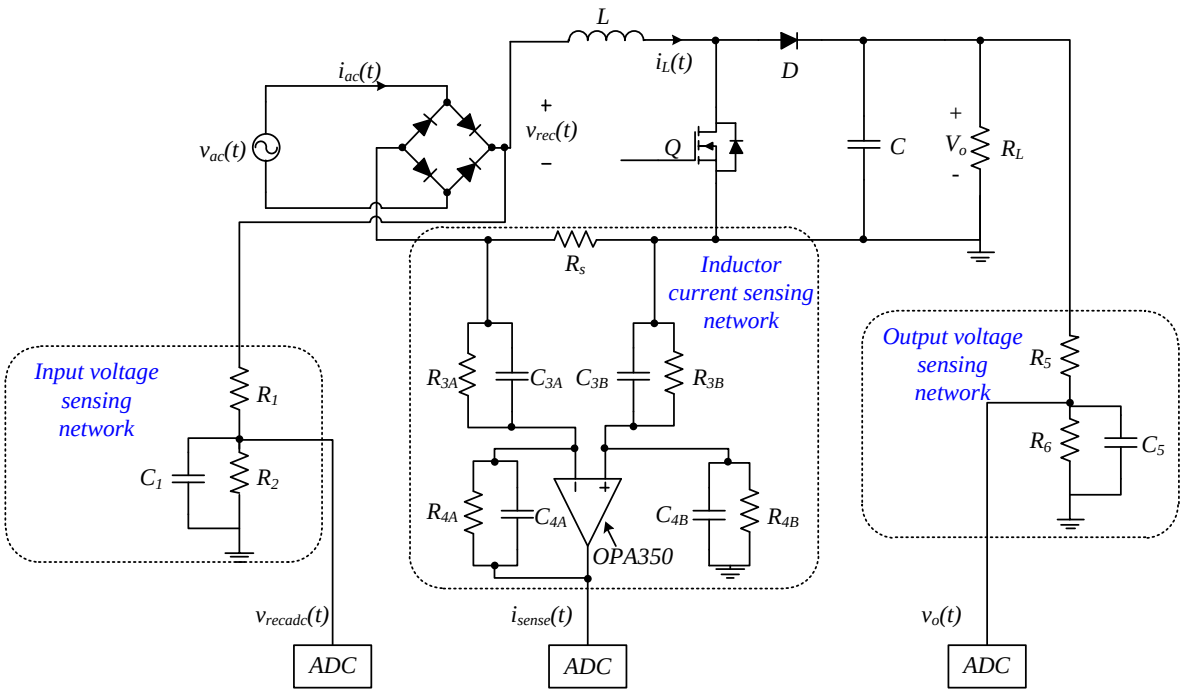


Figure 3.1 Boost PFC converter with analog-to-digital sensing circuitry.

3.2.1 Input Voltage Sensing Design

Given that the rectified input voltage v_{rec} exceeds the typical 0 – 3.3 V range of the ADC considerably, e.g. a maximum v_{rec} of 373 V for a universal input boost PFC converter, it must be scaled down. A voltage divider (Figure 3.1), is a suitable and simple circuit for this task and its DC gain is given by

$$\frac{v_{recadc}}{v_{rec}} = \frac{R_2}{R_1 + R_2}. \tag{3-1}$$

The resistances R_1 and R_2 are selected to give a scaled voltage v_{recadc} equal to the largest measurable voltage at the ADC pin when the maximum expected input voltage is applied to the boost PFC. Although the modified boost PFC converter is designed for universal rms input voltage range of 85-264 V, the input voltage sensor is designed for a maximum rms input voltage of 325 V, or peak input voltage of 460 V.

Such a margin is necessary to allow for overvoltage protection, thereby preventing saturation or damage to the ADC. Since the TMS320F28035 ADCs can sense a maximum full-scale voltage of 3.3 V, values R_1 = 1.12 MΩ and R_2 = 8.090 kΩ are selected to meet this 460 V maximum voltage requirement.

With the maximum sampling frequency of the DSP at 4.6 MHz, the output of the voltage divider networks must attenuate any frequency components greater than half the sampling rate, as governed by the Nyquist Sampling Theorem [49]. In other words, a low pass filter must be used to ensure no frequency components greater than 2.3 MHz are fed to the ADC. The capacitor C_1 is used in parallel with R_2 for this anti-aliasing criterion. The modified boost PFC converter used a capacitance C_1 = 1 nF to achieve a cutoff frequency f_c of

$$f_c = \frac{1}{2\pi C_1 R_2} = \frac{1}{2\pi(1 \cdot 10^{-9}\ \text{F})(8.090 \cdot 10^{3}\Omega)} = 19.7\ \text{kHz}, \tag{3-2}$$

which is well under the sampling rate, but also much greater than twice the bandwidth of the nominally 60 Hz input.

In its simplest form, only the rectified input voltage v_{rec} following the diode bridge requires sensing and sampling. However, due to the presence of an EMI filter before the boost PFC converter, input voltage sensing is accomplished through two voltage dividers with the voltage rectification done in software. This structure is shown at a high-level in Figure 3.1. If the rectified voltage is sensed directly from the output side of the voltage divider, there is considerable DC offset due to capacitive effects, with more prominence at higher line voltages. If accurate zero-crossing detection is required at a later stage, this offset could introduce significant error into the calculation; therefore, this is the reason two identical voltage dividers with software rectification was employed. The disadvantage of this method is the need

for twice the number of passive components and an additional ADC. Nevertheless, higher quality input voltage reproduction is the benefit, possibly allowing greater control performance.

3.2.2 Output Voltage Sensing Design

In a manner nearly identical to the input voltage sensing, the output voltage divider is designed accordingly to sense the output voltage of the boost PFC converter. Generally, boost PFC converters are designed for an output voltage range of 380-400 V [8], with 390 V being the nominal output voltage for the modified boost PFC converter. Allowing suitable margin to protect the ADC and converter from output overvoltage conditions due to transients or device failure, the divider resistances R_5 and R_6 in Figure 3.1 are selected to attenuate the output voltage to the quantity v_o, which has a maximum voltage equal to that of the full-scale input voltage of the ADC. For a full-scale reading of 3.3 V on the ADC converter, resistances R_5 = 1.569 MΩ and R_6 = 10 kΩ are selected for a maximum measurable DC output voltage of 521 V. The output voltage divider gain is given by (3-3).

$$\frac{v_o}{V_o} = \frac{R_6}{R_5 + R_6}. \tag{3-3}$$

Capacitor C_4 is selected as 1 nF, thereby providing the needed anti-aliasing property. The cutoff frequency f_c is

$$f_c = \frac{1}{2\pi C_5 R_6} = \frac{1}{2\pi(1 \cdot 10^{-9}\ \text{F})(10 \cdot 10^{3}\Omega)} = 15.9\ \text{kHz}. \tag{3-4}$$

3.2.3 Inductor Current Sensing Design

The sensing of the inductor current is arguably the most important sensed value for the boost PFC converter. Power factor correction demands an ideally sinusoidal and in-phase input current with the input voltage, so the inductor current must be reproduced as accurately, yet practically, as possible. High

tolerance passive and active components should be employed when sensing the inductor current to ensure this objective.

Current is sensed by measuring the voltage drop across a low-resistance series resistor. Through Ohm's law, the voltage drop can be converted into a corresponding current, provided an accurate resistive value is known. With the modified boost PFC converter, and for a minimally evasive modification, the series resistance in Figure 3.1 is considered fixed at R_s = 20 mΩ, and is therefore a known design factor for the current sensing circuitry. Typically, sensing resistances are on the order of milliohms to minimize power losses [60].

If there is no overcurrent condition, the peak input current i_{pk} in a boost PFC converter is given by

$$i_{pk} = \frac{\sqrt{2}P_{out}}{\eta v_{min}}. \tag{3-5}$$

Where P_{out} is the maximum output power, η the efficiency, and v_{min} the minimum rms ac input voltage. With P_{out} = 650 W, v_{min} = 85 V, and assuming a worst-case efficiency of 88 %, the peak current in the modified boost PFC converter is given by (3-6).

$$\begin{aligned} i_{ac_{pk}} &= \frac{\sqrt{2}P_{out}}{\eta v_{min}} = \frac{\sqrt{2}(650\text{ W})}{(0.88)(85\text{ V})} \\ &= 12.3\text{ A}. \end{aligned} \tag{3-6}$$

Practically, the inductor will have current ripple and additional margin is needed to avoid saturating the full-scale reading of the ADC. Likewise, overcurrent conditions require consideration, and thus the maximum current is assumed greater than 12.3 A. For the modified boost PFC converter, the maximum peak input current, including safety margins, is assumed as 18 A.

Accurate amplification of the R_s voltage drop is accomplished through a single-supply low-pass differential-mode active filter configuration, as shown in Figure 3.1. The gain of the amplifier K_i is given by (3-7).

$$K_i = \frac{i_{sense}}{i_L} = \frac{R_{4A}}{R_{3A}} = \frac{R_{4B}}{R_{3B}} \tag{3-7}$$

With the maximum current and sense resistance R_s known, resistances R_{4A}, R_{4B}, R_{3A}, and R_{3B} in Figure 3.1 are selected to provide a 3.3 V full-scale reading at the ADC input pin. As a direct consequence of this equality, providing high common-mode rejection requires the resistors pairs matched with 1% part tolerance or better [59]. Resistances of $R_{4A} = R_{4B} = 908\ \Omega$, and $R_{3A} = R_{3B} = 98.6\ \Omega$ are selected. The overall gain K_s of the current-sensing network is given by

$$K_s = K_i R_s. \tag{3-8}$$

Similar to the voltage sensors, low-pass filtering is required for anti-aliasing, in addition for noise filtering and attenuation of the high-frequency switching components. Capacitors C_{4A} and C_{4B} are matched and selected as 220 pF for the modified boost PFC converter; therefore, the cutoff frequency f_c is given by (3-9), satisfying the Nyquist Sampling Theorem.

$$\begin{aligned} f_c &= \frac{1}{2\pi R_{4A/4B} C_{4A/4B}} = \frac{1}{2\pi(908\ \Omega)(220 \cdot 10^{-9}\ \text{F})} \\ &= 796\ \text{kHz}. \end{aligned} \tag{3-9}$$

Ideally, the current sense amplifier should be located in close proximity to the current sense resistor, or the input may be overburdened by noise and voltage drops. Additionally, if opportunity permits, four-terminal sensing is recommended. A Texas Instruments OPA350 operational amplifier is used for the current amplifier due to its high performance characteristics and low-offset voltage [61]. The designed current sensor is shown in Figure 3.2.

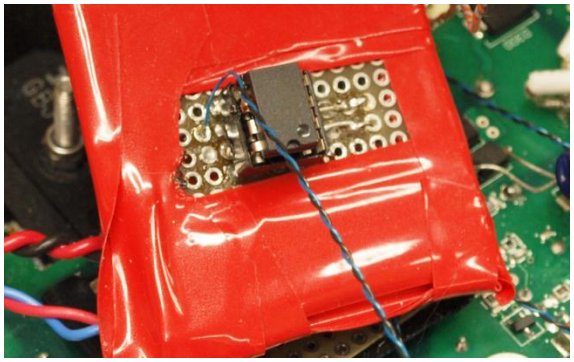


Figure 3.2 Current sense amplifier designed for modified boost PFC converter.

3.3 Current Compensator Design in CCM

Introduced in Chapter 2, the linearized small-signal model of the CCM boost PFC control-to-output transfer function is given by

$$G_i^{CCM}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}(s)} = \frac{V_o}{sL}. \tag{3-10}$$

Characterizing the response of the open-loop boost PFC converter requires writing the loop gain T_i^{CCM} of the system, graphically represented by the system block of Figure 3.3 and mathematically written as (3-11).

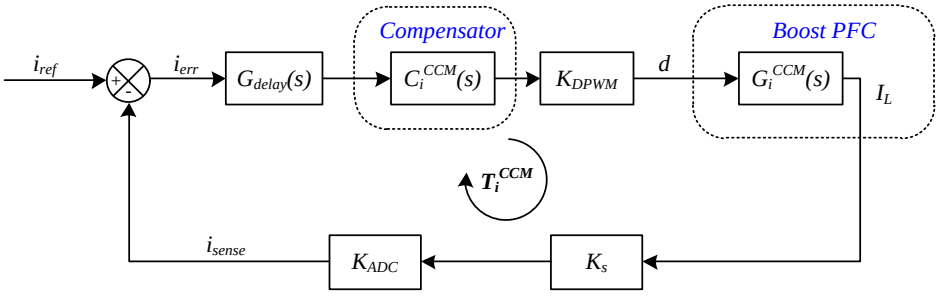


Figure 3.3 System block diagram of CCM boost PFC converter.

The system consists of the sensor gain products, as well as the transfer function products of the boost PFC converter inductor current and current compensator. The gains are: ADC gain K_{ADC}, current sensor

network gain K_s, boost PFC CCM inductor current power stage transfer function G_i^{CCM}, and the CCM current compensator transfer function C_i^{CCM}. Additionally, a delay term $G_{delay}(s)$ is incorporated to account for the computation and ADC sampling delays, and is considered as half the single sampling period delay T_s.

$$T_i^{CCM}(s) = G_i^{CCM}(s)C_i^{CCM}(s)K_sK_{ADC}G_{delay}(s) \tag{3-11}$$

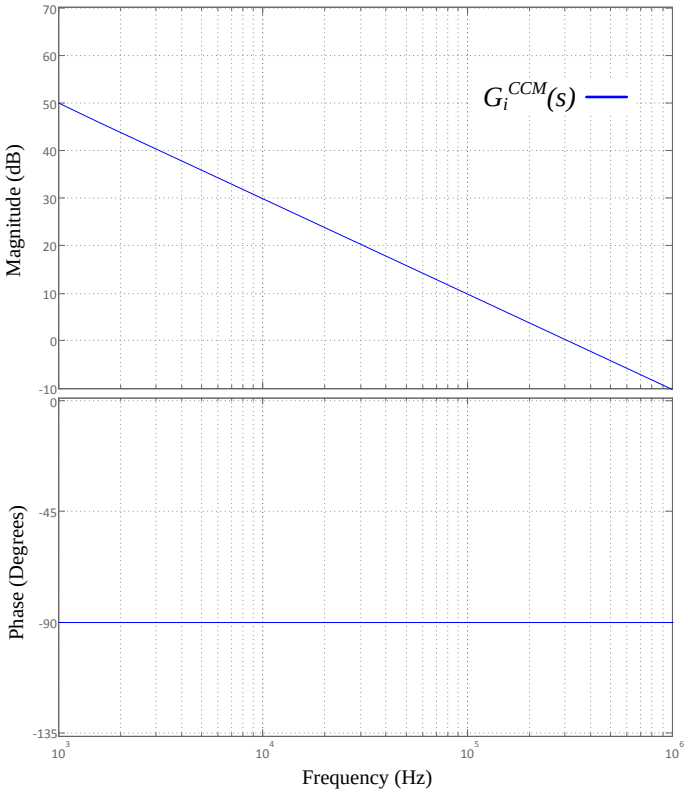


Figure 3.4 Control-to-output frequency response of CCM boost PFC converter (L = 200 µH, f_s = 130 kHz, and V_o = 390 V).

The control-to-output open-loop frequency response is plotted in Figure 3.4 for the boost PFC converter values L = 200 µH, f_s = 130 kHz, and V_o = 390 V. Clearly, the system is of single-pole nature,

with large low-frequency gain and a 90-degree phase lag due to the single-pole response. The system is adequately compensated by proportional-integral (PI) control [8]. The inner current loop is a fast loop with a bandwidth generally selected to be within 1/10th to 1/6th the switching frequency f_s [18]. With f_s = 130 kHz, this translates to a range of 13 kHz to 21.6 kHz.

The CCM current compensator is designed in MATLAB to achieve the desired response characteristics, and the designed continuous-time transfer function of the PI compensator is given by (3-12).

$$C_i^{CCM}(s) = \frac{0.904(s + 2.03 \cdot 10^4)}{s} \tag{3-12}$$

Since (3-12) is in the continuous frequency domain, the compensator must be converted to a discrete format, as a continuous-domain compensator cannot be implemented in a digital device without conversion to a discrete format. The Bilinear Transformation [49] is used to transform the controller into a discrete equivalent, through the following transformation:

$$s = \frac{1}{T_s}\left[\frac{z-1}{z+1}\right]. \tag{3-13}$$

Where *s* and *z* are complex numbers in the continuous and discrete frequency-domains, respectively. The sample rate of the controller is given by T_s, and selected as 130 kHz.

Following discretization of the CCM compensator with the Bilinear Transformation (3-14), the loop gain T_i^{CCM} gives a crossover frequency of 15 kHz and a phase margin of 40 degrees. The frequency response is shown graphically in Figure 3.5.

$$C_i^{CCM}(z) = \frac{0.9742z - 0.8331}{z - 1} \tag{3-14}$$

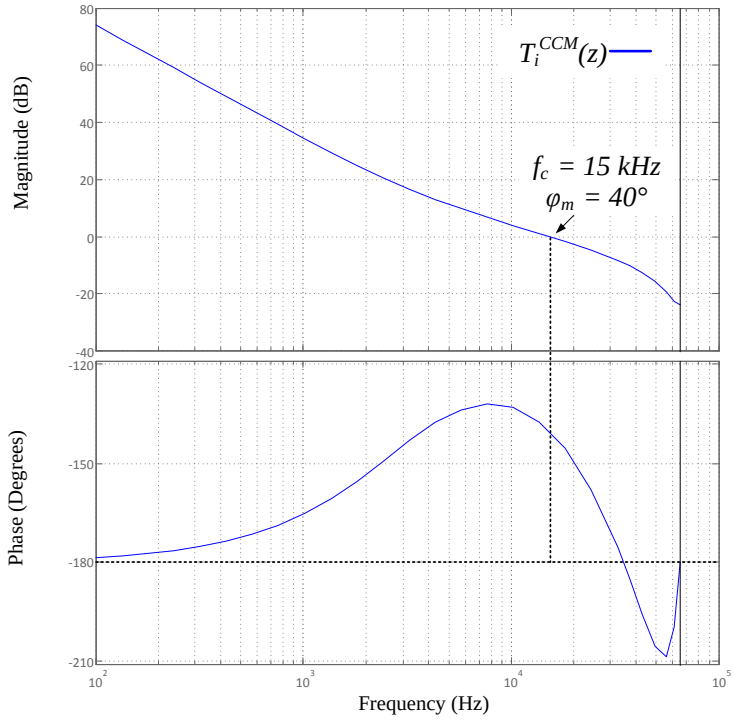


Figure 3.5 Compensated CCM boost PFC current loop T_i^{CCM} in z-domain. Crossover frequency f_c and phase margin φ_m are highlighted (L = 200 µH, f_s = 130 kHz, V_o = 390 V, d = 0.1297, V_M = 340 V).

Simulation is performed through PSIM, a power electronics simulation package [62], verifying the good current-tracking performance of the controller (Figure 3.6).

On the experimental prototype, the current compensator coefficients obtained from MATLAB are implemented in the DSP, but tuned manually in real-time to achieve performance improvements on the non-ideal experimental prototype. Slight tuning is required to account for the non-idealities unaccounted for in the small-signal model.

Due to the much lower bandwidth of the outer voltage loop compared to the inner current loop, the voltage compensator can be tuned in real-time on the DSP. Real-time tuning provides immediate feedback for this slow loop, and performance changes can be quickly seen. The voltage loop should be

tuned to provide an acceptable output voltage regulation and transient response dictated by the application, but should not have such a high bandwidth as to degrade the input current harmonics.

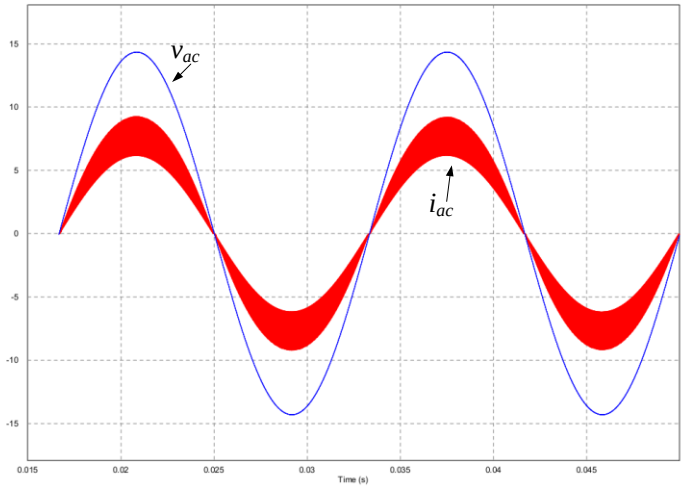


Figure 3.6 Simulation results showing power factor corrected input current i_{ac} sinusoidal and in-phase with line voltage v_{ac}. Compensation is provided by designed CCM proportional-integral compensator.

3.4 Digital Average Current Mode with Voltage Feedforward Controller Implementation with the TMS320F28035 DSP

This section provides an overview of the digital control software architecture and design considerations for the modified boost PFC digital controller when using the Texas Instruments TMS320F28035 DSP. A brief outline of the interrupt service routines (ISRs) and loop architecture is provided for the digital implementation of average current mode control with voltage feedforward.

3.4.1 Digital Average Current Mode Control with Voltage Feedforward

The digital implementation of average current mode control with voltage feedforward is shown in Figure 3.7. As described in Chapter 2, voltage feedforward eliminates the closed-loop response dependency on the line voltage v_{ac}, thereby allowing a constant output power in spite of line voltage disturbances. Additionally, as previously mentioned in Section 3.2.1, input voltage rectification is

performed in software due to DC offset voltages present after the bridge rectifier. Rectification is done at the beginning on the main interrupt and coded in assembler for maximum execution speed.

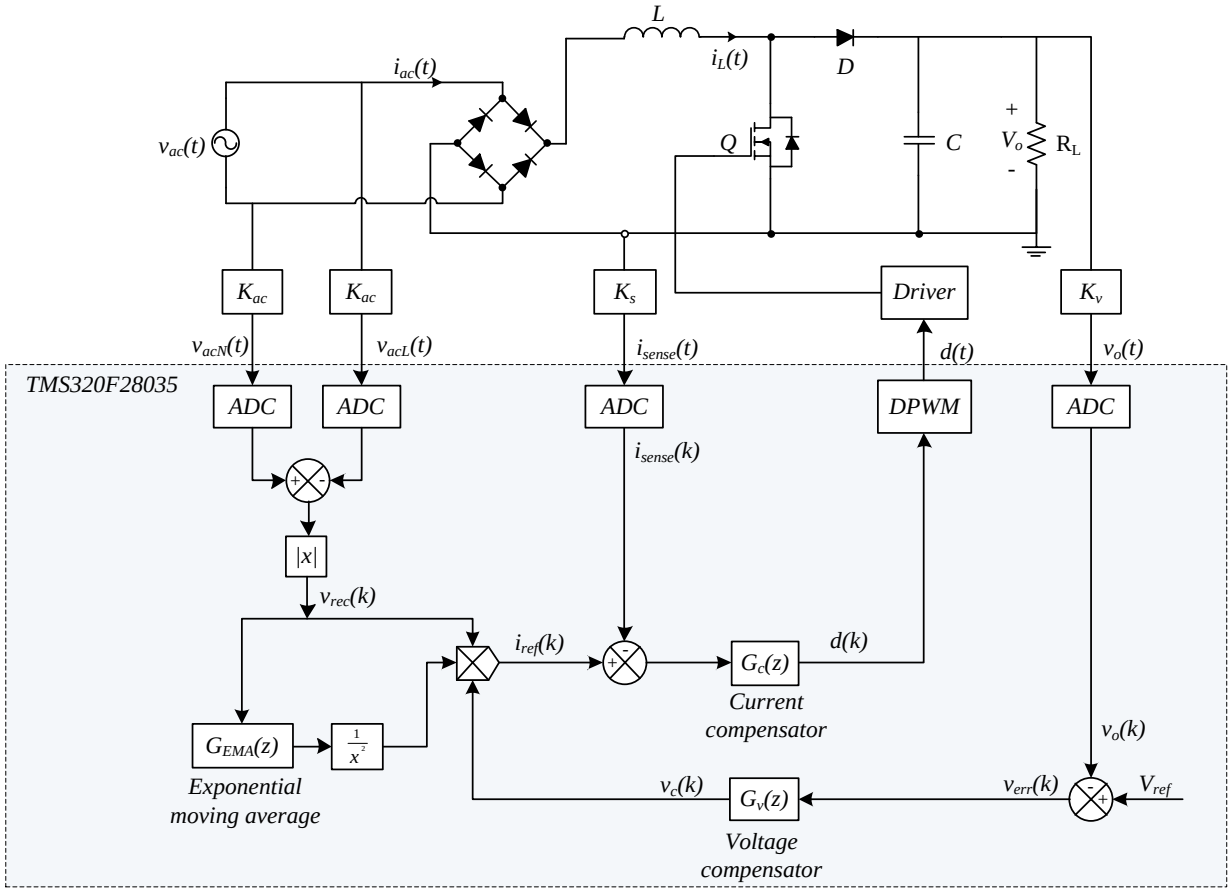


Figure 3.7 High-level structure of implemented version of digital average current mode control with input voltage feedforward

3.4.2 Digital Exponential Moving Average Filter

Voltage feedforward requires the average value v_{recavg} of the rectified input voltage v_{rec}. An infinite impulse response (IIR) filter forms the structure of an exponential moving average filter, and is implemented digitally in the DSP to give v_{recavg} [52]. The filter is shown in Figure 3.8 along with its discrete frequency-domain transfer function in (3-15). The advantages of this filter is a reduction of

memory use and computational requirements when compared to a standard averaging filter, ultimately allowing faster processing speeds.

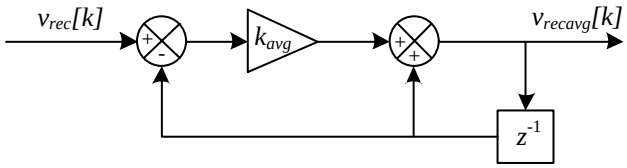


Figure 3.8 Exponential moving average IIR filter providing average input voltage v_{recavg}[k] from rectified input voltage v_{rec}[k].

$$\frac{v_{recavg}(z)}{v_{rec}(z)} = \frac{k_{avg}}{1-(1-k_{avg})z^{-1}} \tag{3-15}$$

The coefficient k_{avg} provides the exponential weighting factor, and is selected according to the desired cutoff frequency f_c, and sampling frequency f_{samp}, in this case 5 Hz and 130 kHz, respectively. Mathematically, its value is selected by evaluating (3-16):

$$\begin{aligned} k_{avg} &= \frac{2\pi f_c}{f_{samp}} = \frac{2\pi \cdot 5\ Hz}{130 \cdot 10^3\ Hz} \\ &= 0.0002417. \end{aligned} \tag{3-16}$$

3.4.3 Current and Voltage Compensators

Considering the generic two pole and two zero (2P2Z) discrete controller discrete transfer function (3-17), where z^{-n} represents a unit delay of n sample periods [52], if the coefficients of each delay term are represented by their corresponding a_n and b_n terms, a difference equation can be written by cross-multiplying and arranging, giving (3-18). Term u[k] represents the controller output, in this instance the duty cycle d, and $u[k - n]$ the duty cycle from the previous switching period n. The same concept applies for the error terms $e[k - n]$, which represent the previous voltage or current error from present or past n

computations. Hence, the digital controller of (3-14) can be implemented in a digital device through simple arithmetic operations and a small number of data storage registers.

$$\frac{U[z]}{E[z]} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 - a_1 z^{-1} - a_2 z^{-2}} \tag{3-17}$$

$$u[k] = b_0 e[k] + b_1 e[k-1] + b_2 e[k-2] + a_1 u[k-1] + a_2 u[k-2] \tag{3-18}$$

In Figure 3.9, the Direct Form I of the IIR 2P2Z controller is shown. This structure is flexible in that it can be used for both the current and voltage compensators, allowing simplicity of the controller implementations. If increased controller complexity is required, the 2P2Z controller is easily extendable to an even greater number of poles and zeros, at the disadvantage of decreased computation speed and increased memory requirements.

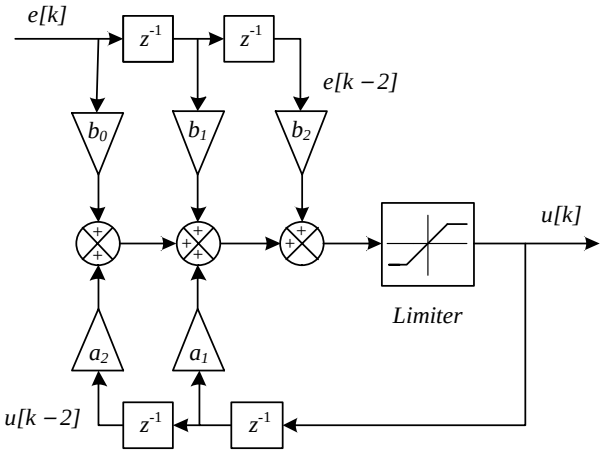


Figure 3.9 Structure of IIR digital two-pole two-zero compensators. Output is limited to prevent duty cycle from exceeding 100%.

3.4.4 Interrupts and Sampling

The DSP contains dedicated PWM counters allowing facilitated generation of the continuous-time duty cycle from its discrete reference value [56]. A register named *TBCTR* is configured to run in a count-

up-count-down triangular pattern, where a register called *TBPRD* sets the maximum counter value, set to 231 for a 130 kHz switching frequency. Upon the event where *TBCTR* equals *TBPRD*, the *TBCTR* begins counting down until it reaches a value of zero. Registers *CMPA* and *CMPB* dictate the points at which the duty cycle transitions from high-to-low and low-to-high, respectively. Figure 3.10 illustrates the DSP internal generation of the PWM signal and sampling during two consecutive switching cycles.

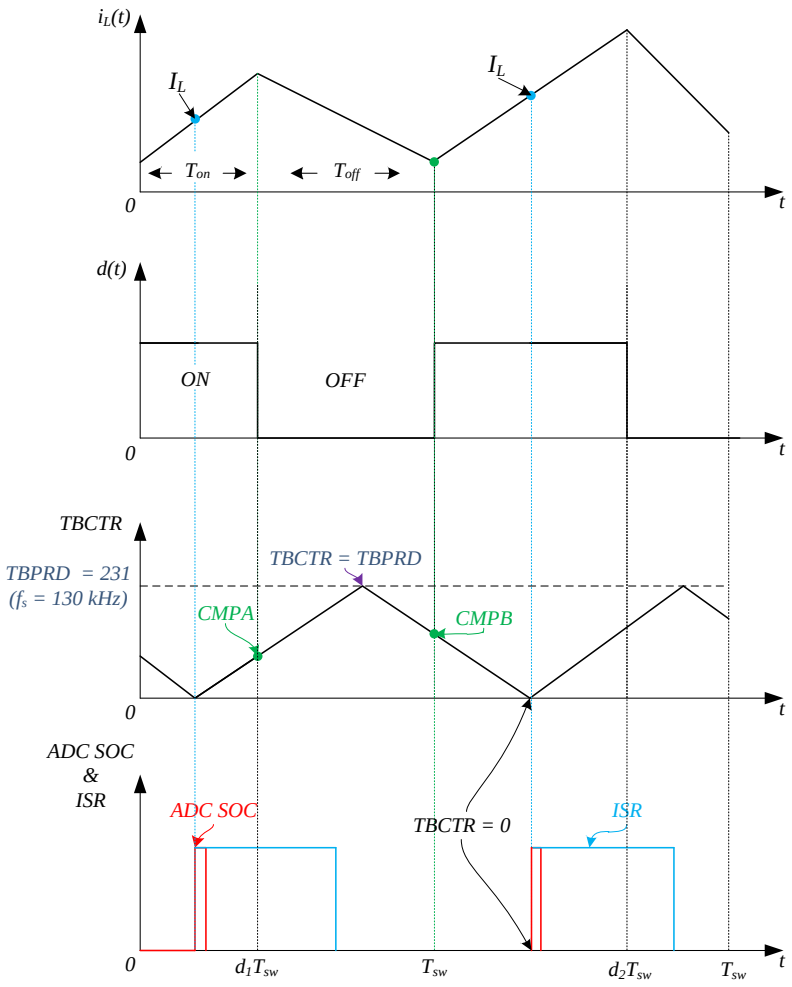


Figure 3.10 Waveforms of DSP internal PWM counter for duty cycle generation, sampling, and interrupt triggering.

This PWM generation process is important for a number of reasons. Upon reaching a *TBCTR* value of zero, an event is triggered signaling the start-of-conversion (SOC) of the ADC modules. Since the

TBCTR = 0 event corresponds with the middle of the duty-cycle *ON* period, sampling of the input voltages v_{acN}, v_{acL}, v_o, and i_{sense} are likely free of switching noise. Furthermore, as explained in Chapter 2, sampling in the middle of the inductor current rising slope, or at *TBCTR = 0*, gives the average inductor current in CCM operation.

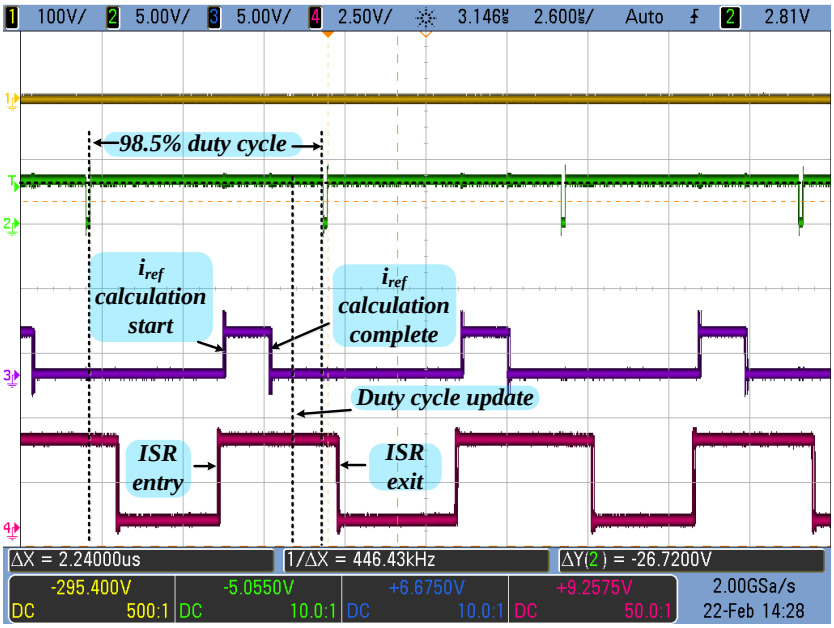


Figure 3.11 Interrupt entry and exit points showing execution speed of compensation ISRs.

Immediately following the conversion of all four sampled quantities, the ADC module initiates entry into an ISR. This ISR is written in assembler allowing minimum servicing time and thus maximum execution rate. As the current loop is time-critical, the next duty cycle must be generated in the same switching period as the sampled values for real-time control. With a 60 MHz clock, there are approximately 462 cycles (T_s = 7.7 μs) to sample, compute, and update the duty cycle for the next switching period. During the worst-case scenario of a 100% duty cycle, there are only 231 cycles available to update duty cycle as a result of the midpoint value sampling. Figure 3.11 provides a visual indication of the ISR entry and exit points. Although the ISR exit point is after the end of the switching

period, the performance is unaffected as the current command waveform indicates that the needed duty cycle is computed before the end of the switching period.

3.5 Experimental Results and Discussion

This section presents the experimental results of the digital conversion and control of the modified boost PFC converter, confirming successful modification of a boost PFC converter previously controlled by an analog IC. The boost PFC converter (L = 200 µH, C = 300 µF, f_s = 130 kHz, V_o = 390 V) is designed for a maximum output power of 650 W and a universal input range (85-264 V).

Waveforms showing the modified converter achieving PFC at an output power P_{out} = 150 W and input voltage v_{ac} = 100 V, as well as 390 V output voltage V_o regulation, are presented in Figure 3.12. The 120 Hz 6.6 V peak-to-peak ripple, due to the second harmonic component in the output power expression (2-10), is clearly visible on V_o.

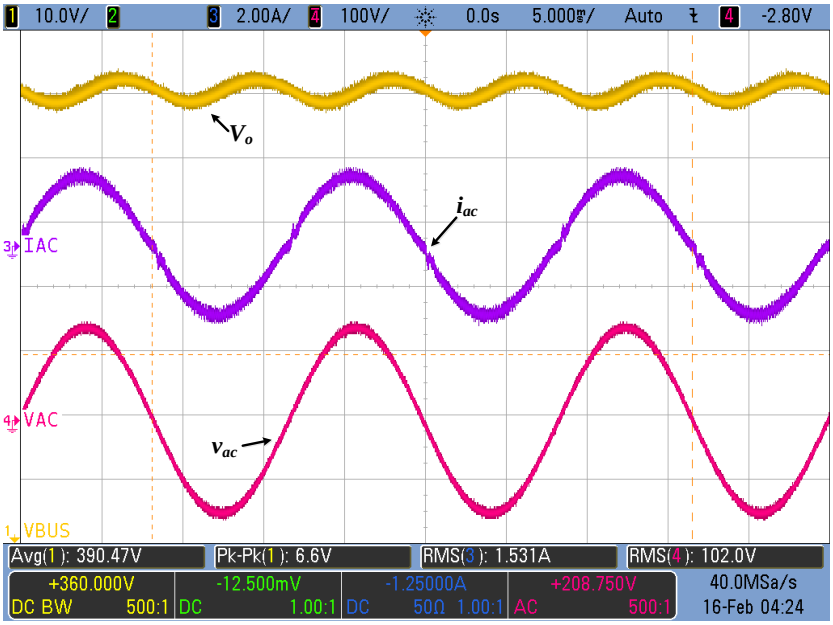


Figure 3.12 Waveform captures showing input voltage v_{ac}, power-factor-corrected input current i_{ac}, and regulated output voltage V_o of modified boost PFC converter with digital control. (P_{out} = 150W, v_{ac} = 100 V, f_{line} = 60 Hz, L = 200 µH, C = 300 µF, f_s = 130 kHz, V_o = 390 V).

Transient performance to a step change in output power P_{out} = 325 W to 650 W is shown in Figure 3.13, verifying voltage loop compensation. In Figure 3.14, waveform captures of the soft-start feature of the digital controller shows a controlled rise in output voltage and gradual increase in input current. Device stresses are therefore minimized on initial startup.

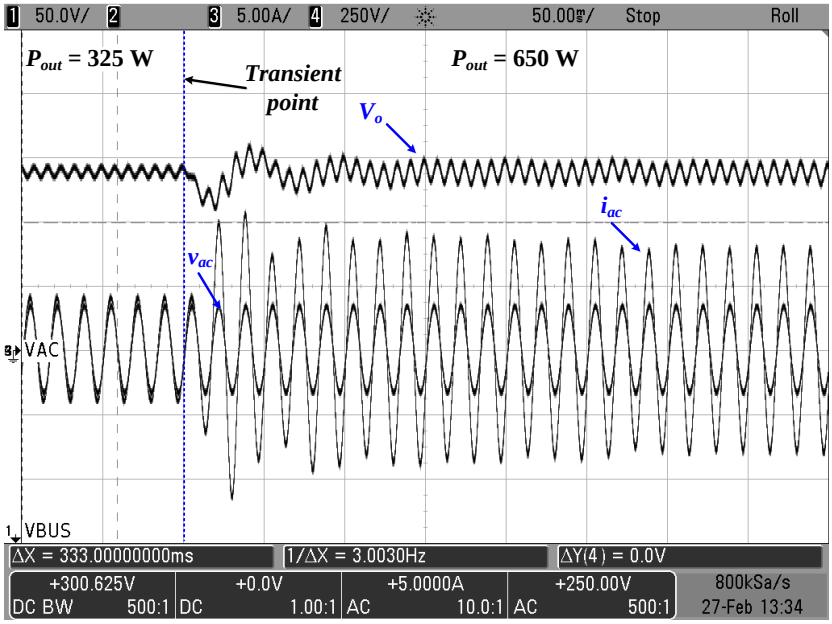


Figure 3.13 Voltage transient waveform capture of step load of P_{out} = 325 W to P_{out} = 650 W for modified boost PFC converter with digital control (Input voltage v_{ac} = 120 V).

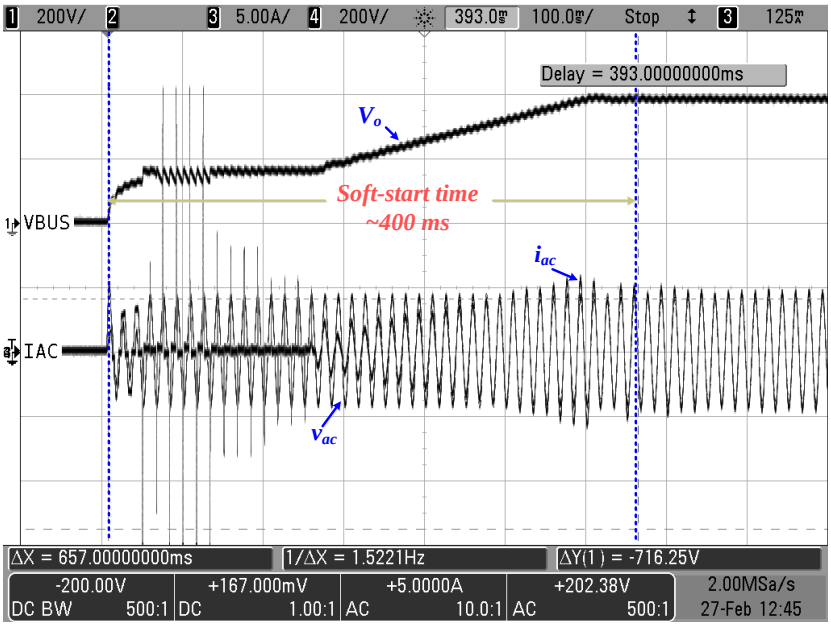


Figure 3.14 Waveform capture of modified boost PFC converter with digital control from an input voltage of v_{ac} = 0 V to v_{ac} = 120 V with output power P_{out} = 325 W. Soft-start time is approximately 400 ms.

3.6 Summary

A modified boost PFC converter was adapted from its analog-controller version for digital implementation using a Texas Instruments TMS320F28035 DSP. A detailed explanation of the required sensing circuits and their designs presented. Modeling and control of the CCM boost PFC current loop to achieve sinusoidal input current under digital average current mode control with voltage feedforward was described, along with simulation results demonstrating its performance. An overview of the DSP software was provided, emphasizing the structure of the 2P2Z digital compensator and exponential moving average filters. Furthermore, a description of the ISR and its operation was provided. Experimental results show the success of modifying the existing boost PFC converter for digital control. The current controller provided a sinusoidal and low-harmonic input current, with the output voltage controller providing a regulated output voltage. Additionally, features such as soft-start and overvoltage protection were

demonstrated, and further experimentation with the digital control framework and modified boost PFC converter for advanced control design is possible, as will be shown in Chapters 4 and 5.

4 DSP-based DCM Detection for Boost PFC Converters

4.1 Overview

This section presents a novel zero current detection (ZCD) method to resolve the cost and computational requirements associated with existing DCM and MCM control techniques. The proposed implementation makes use of high-speed on-board comparators present on many modern digital signal processors to provide a cost-effective ZCD detection solution, while avoiding or improving on existing detection methods. With additional logic to prevent spurious events or noise from erroneously selecting the incorrect mode of operation, DCM operation is also identifiable. Moreover, a reduction of hardware and cost requirements is possible by eliminating the need for auxiliary zero-current detection circuits. Finally, this novel DCM detection method allows rapid prototyping of MCM control techniques to existing digitally controlled boost PFC converters, as few software changes, and minimal, if any, hardware changes are required.

Section 4.2 provides an overview of DSP on-board peripherals, specifically on-board comparators and their functional behaviour. Section 4.3 describes the requirements, implementation, and practical considerations of the proposed ZCD logic. Detailed theoretical operation is presented, and the challenges of ZCD are highlighted. Section 4.4 provides experimental results validating the qualification logic and proposed detection method with a modified PFC boost converter. Finally, Section 4.5 summarizes the contributions of the proposed DSP-based detection method.

4.2 DSP High-speed Comparators

Peripherals such as integrated pulse-width modulation modules, on-board digital-to-analog (DAC) converters, communication modules, etc. are finding greater presence in today's digital controllers [57][58]. Among these peripherals is the on-board high-speed comparator, which, as will be demonstrated, allows for greater flexibility and application of innovative control solutions.

The comparator (Figure 4.1) is two-input terminal analog device whose output y is a logical high when the positive terminal input v_+ is greater or equal than the negative terminal v_-. If v_- is greater than v_+, the output is logical low.

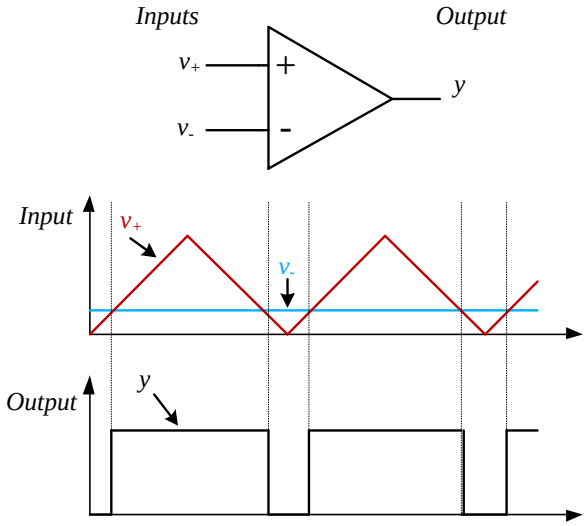


Figure 4.1 Analog comparator with inputs v_+ and v_-. Output y is a logical high if $v_+ \geq v_-$, and a logical low otherwise.

It is highly desirable to use available on-board peripheral resources efficiently on a digital device to minimize complexity and cost. As explained in Chapter 2, existing zero-current detection methods may sometimes employ auxiliary circuits or hardware, leading to increased volume, cost, and complexity. By using the on-board comparators present on many modern DSPs, it is possible to reduce hardware and

software intricacy when detecting zero current. The proposed detection method is described in the next section.

4.3 DSP-based DCM Detection Design Considerations

The simplified system view of the internal high-speed comparator of the TMS320F28035 DSP is shown in Figure 4.2. The input to the positive terminal of the comparator is the scaled inductor current i_{sense}, which has been sensed and amplified by the current-sense network.

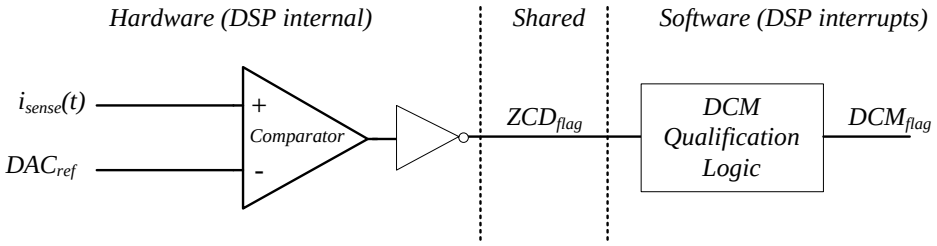


Figure 4.2 DSP (TMS320F28035) hardware comparator and DCM software qualification logic.

Internal to the DSP, the negative terminal of the comparator is connected to a 10-bit DAC whose analog reference voltage DAC_{ref} can be programmed to the required setpoint [54]. Ideally, this reference voltage would be set to zero volts, corresponding to the current-sense amplifier's output for zero inductor current. Practically, however, the effects of amplifier offset voltage, noise, and other non-ideal effects lead to a non-zero output voltage from the current-sense amplifier when the inductor current reaches zero. DAC_{ref} should therefore be configured with a slight voltage offset to ensure adequate detection and noise immunity margins. The programmability of the DAC allows the ideal offset voltage to be set experimentally and with relative ease. Furthermore, to match the definition of a zero-current condition corresponding to logical high ZCD_{flag}, the comparator's output should be inverted before passing to the later stages. This is accomplished internally in hardware, and therefore no significant delay is added to the comparator's output.

Additionally, as shown and described in Chapter 2, the inductor current will resonate due to the inductance and parasitic diode/switch capacitances in the DCM period, possibly indicating a false DCM/CCM transition. It is therefore of interest to minimize susceptibility to false DCM/CCM transition events and spurious events such as switching noise and electromagnetic interference (EMI); thus, a reasonably accurate determination of the ZCD_{flag} validity is required for proper detection of DCM entrance and exit points. By employing specific interrupts generated by their own specific events, a software solution can realize this qualification logic and is proposed in the next section.

4.3.1 Interrupt and Software Detection Logic

This section provides a detailed description of the operation and procedure for detecting zero current using three separate interrupts. Multiple interrupts generated on individually specific conditions dictate the detected mode of operation i.e. operation in CCM or DCM, while also providing robustness to spurious events. Figure 4.3 provides an overview of the interrupt triggered by a hardware ZCD_{flag} and associated qualification action. In Figure 4.4, the second interrupt allowing detection of DCM to CCM operation is shown. Finally, Figure 4.5 shows the third interrupt used for re-enabling additional interrupts. The interrupts and accompanying actions are described in the following paragraphs in more detail.

At the moment of zero-current detection, the output of the comparator is forced high, corresponding to a raised zero-current condition flag ZCD_{flag}. ZCD_{flag} is assigned the immediate output value of the comparator, and is routed to the DSP via a general input/output (GPIO) pin. This GPIO pin is configured in software and hardware to serve as an external interrupt upon a low-to-high transition.

Following entry into the interrupt triggered by the low-to-high transition of the ZCD_{flag}, DCM_{imm} and DCM_{flag} are set, provided the switching period is in T_{off}. If set, external ZCD_{flag} interrupts are disabled for the remainder of T_{sw} and into the next T_{on} period. ZCD_{flag} interrupts will be re-enabled with an additional interrupt upon entry in T_{off}. Consequently, most spurious events, noise, and DCM oscillation will not

trigger the DCM_{flag} successively in a single switching cycle once it has been triggered prior. Such an implementation also results in increased processing headroom due to minimum spent servicing the interrupt.

At the start of a new switching period during T_{on}, a new interrupt is generated to confirm the presence of sustained DCM operation. If DCM_{imm} was set during the most recent past switching period, the DCM_{flag} remains high and indicates continued DCM operation. At this time, appropriate action can be taken to ensure a proper control technique is applied for the DCM mode of operation. If, however, the DCM_{imm} was not triggered during the most recent past switching period, the DCM_{flag} is cleared, indicating the transition from DCM to CCM operation.

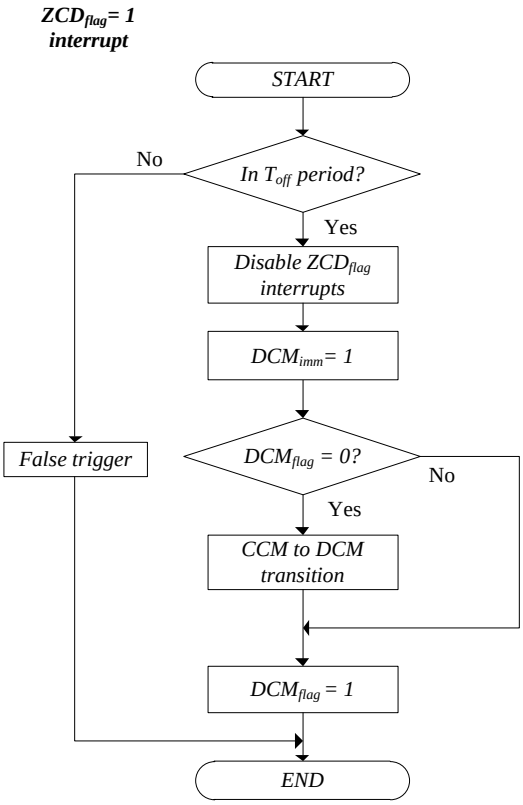


Figure 4.3 Software flowchart illustrating ZCD_{flag} =1 interrupt and associated qualification logic.

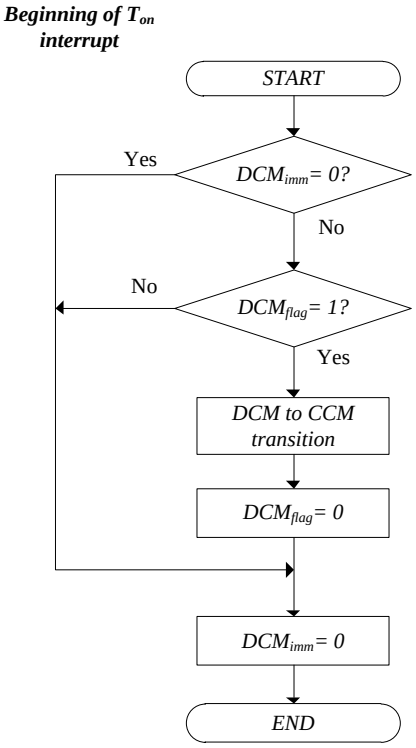


Figure 4.4 Software flowchart illustrating interrupt generated at beginning of T_{on} providing detection of DCM-to-CCM operation.

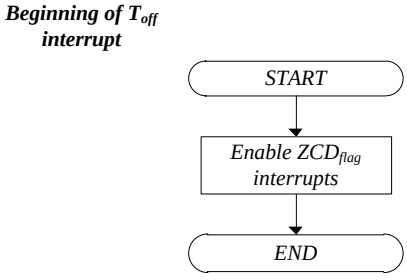


Figure 4.5 Software flowchart illustrating interrupt generated at beginning of $T_{off,}$ thereby allowing future ZCD_{flag} interrupts.

4.3.2 Theoretical Operational of DCM Detection Logic

The theoretical operational scenario presented in Figure 4.6 provides waveforms of the proposed detection and ensuing qualification logic for five hypothetical periods, T_1 – T_5, during a single half-line cycle. The operation is as follows: During T_1, the converter is operating in CCM, hence ZCD_{flag} and DCM_{flag} remain at a logical low. During period T_2 and at moment d_3T_{sw}, the inductor current reaches zero and ZCD_{flag} is triggered high. Subsequently, DCM_{flag} is set high in succession with DCM_{imm}, indicating the transition into DCM operation. Interrupts sourced from a ZCD_{flag} event are disabled at this point, and now additional zero-current events, such as DCM current oscillation, do not expend redundant DSP processing.

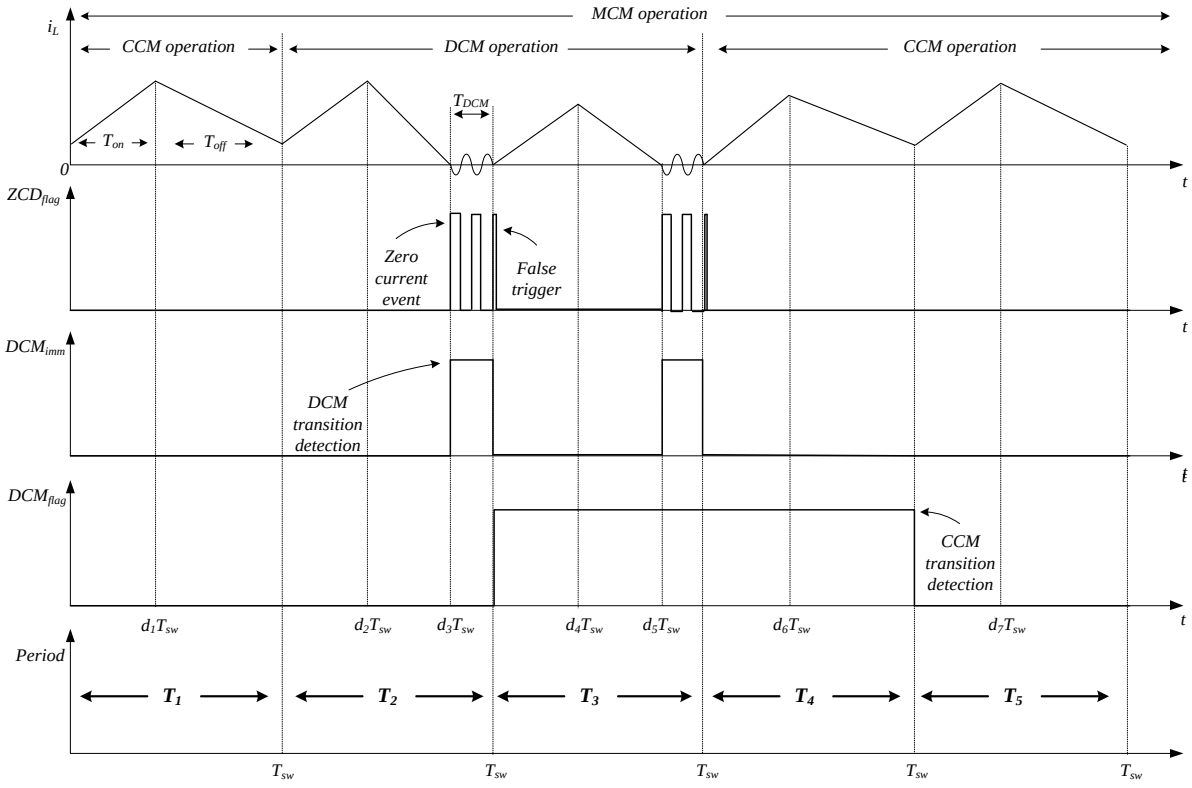


Figure 4.6 Theoretical waveforms illustrating proposed DSP-based detection and qualification logic in response to MCM operation. Detection logic signals ZCD_{flag} DCM_{flag}, and DCM_{imm} are shown with their responses to inductor current i_L.

With DCM operation detected upon entering the switching period of T_3, DCM_{imm} is reset low allowing the DSP to decide if the DCM_{flag} should be cleared or left as-is during the next switching cycle. At d_5T_{sw}, the DCM_{imm} flag is set in accordance with the zero current condition and DCM_{flag} remains unchanged. In period T_4, however, no zero current events are detected during the switching period, and thus no DCM_{imm} flag is set. The boost PFC converter has transitioned DCM operation to CCM operation, and DCM_{flag} is cleared at the beginning of period T_5.

4.4 Experimental Results and Discussion

Initial experimental results present the detection logic applied to a boost converter with constant input voltage V_o and load with output power P_{out} to demonstrate the effectiveness of the qualification logic under CCM and DCM operation. Lastly, the proposed DCM detection logic is experimentally verified under pure DCM as well as MCM operation with a sinusoidal input voltage v_{ac}. A universal input (85-264 V) 650 W boost PFC converter with specifications: L = 200 µH, C = 300 µF, f_s = 130 kHz, and V_o = 390 V was modified for fully digital operation from its previously analog IC-controlled version, and implemented on a Texas Instruments TMS320F28035 DSP. The experimental configuration is shown in Figure 4.7.

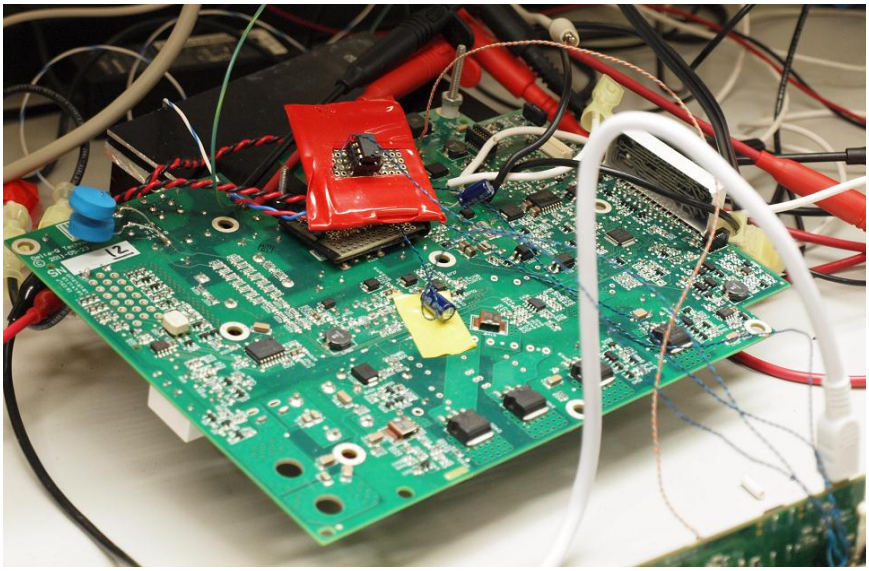


Figure 4.7 Experimental setup and boost PFC prototype modified for digital operation.

The 10-bit DAC internal inverting terminal was empirically determined to trigger at ~29 mV with a sensed inductor current of 0 A. Internal to the DSP, this corresponds to an internal DAC reference of 9 (decimal). As explained in Section 4.3, noise and the current sense offset voltages make a reference of 0 V impractical, and thus, a finite offset must be selected to compensate for these non-idealities.

4.4.1 Qualification Logic Experimental Results

The proposed DCM detection and qualification logic for DCM operation and CCM operation are shown in Figure 4.8 and Figure 4.9, respectively. Approximately, where the inductor current becomes zero (Figure 4.8), ZCD_{flag} is set high and falls low once the next switching period begins. As observed, DCM_{flag} remains high due to the proposed qualification logic preventing additional zero-current events (i.e. DCM oscillation) from triggering redundant interrupts; hence, DCM operation is identified.

In accordance with the proposed DCM detection logic, during sustained CCM operation (Figure 4.9), ZCD_{flag} is toggled but DCM_{flag} remains low due to the halting of ZCD_{flag} interrupts during T_{on} periods. There is a finite delay on the rise and fall of the ZCD_{flag} due to the presence of 35 mV hysteresis internal

to the comparator. Although this hysteresis can be disabled, it is advantageous in that it aids in preventing false triggering due to noise.

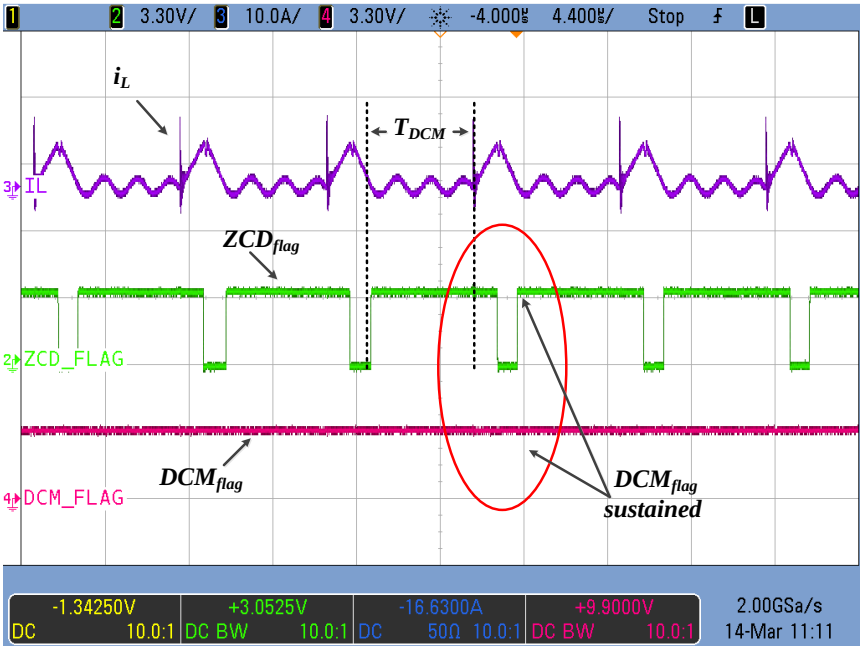


Figure 4.8 Experimental waveform capture of DCM_{flag} and ZCD_{flag} detection qualification validity over multiple switching cycles with inductor current i_L exhibiting fully DCM operation.

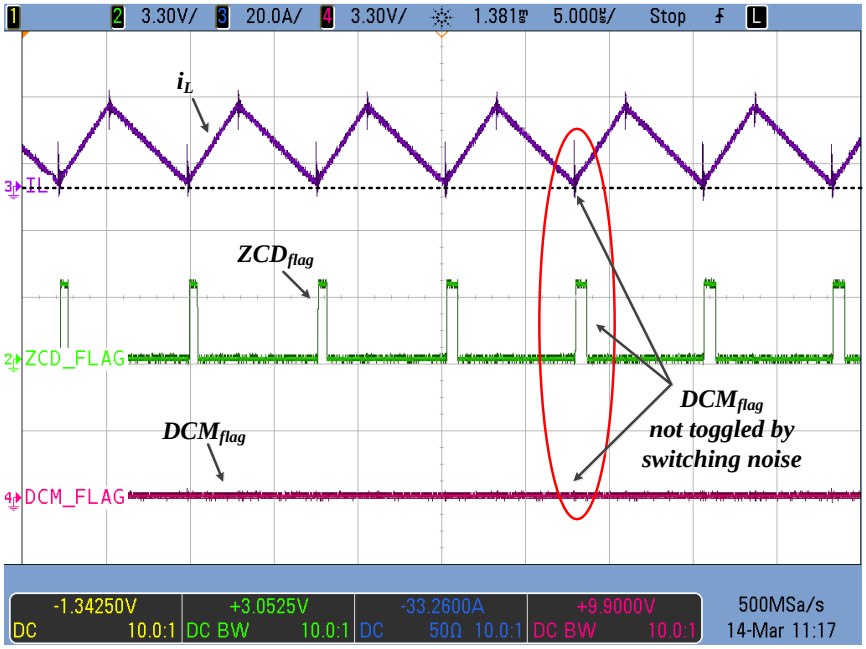


Figure 4.9 Experimental waveform capture of DCM_{flag} and ZCD_{flag} detection qualification rejected toggling from inductor current i_L switching noise during CCM operation.

4.4.2 DCM Detection Applied to Boost PFC Prototype Experimental Results

To demonstrate the feasibility of the proposed DSP-based DCM detection logic for the entire 60 Hz ac line period in PFC applications, the detection logic under various conditions is tested and results presented.

In Figure 4.10 at an output power loading of P_{out} = 49 W, where pure DCM operation over the entire line cycle is observable, the DCM_{flag} successfully specifies constant DCM operation over the entire line cycle. There are no false triggers leading to a change in the reported mode of operation.

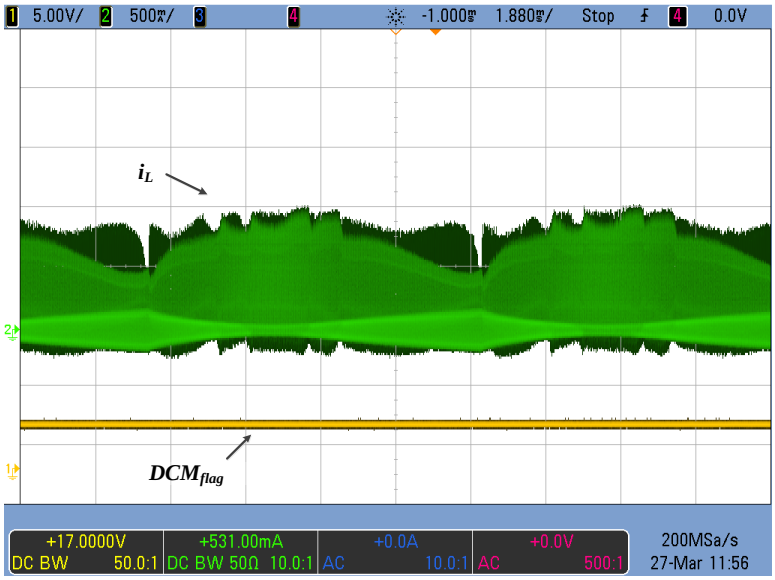


Figure 4.10 Experimental waveform capture of DCM_{flag} validity with inductor current i_L exhibiting fully DCM operation over a line cycle (P_{out} = 49 W, v_{ac} = 120 V, f_{line} = 60 Hz).

Figure 4.11 presents the waveform captures during MCM with an output power of P_{out} = 98 W. Generally, the majority of the line cycle proper detection of DCM operation and CCM operation is specified; however, it can be noted that there is some false DCM_{flag} triggering around the DCM entry and exit points. The high switching frequency of the converter (f_s = 130 kHz) and finite processing speed of the DSP gives a reduced window to service interrupts. Subsequently, during some moments approaching the DCM and CCM transition, rapid interrupt events may be incorrectly serviced or missed entirely. Practically, this phenomenon can be mitigated by selecting a slower switching speed, e.g. 70 kHz, at the expense of larger passive components.

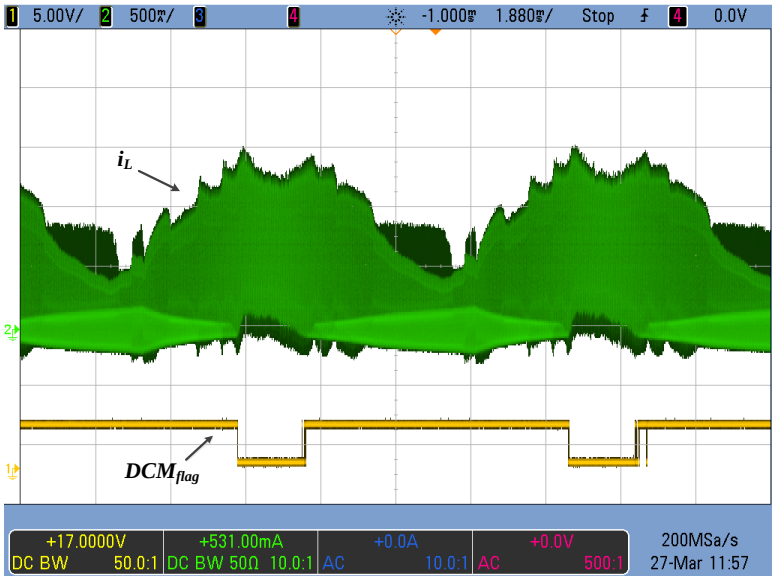


Figure 4.11 Experimental waveform capture of DCM_{flag} validity with inductor current i_L showing MCM operation over a line cycle (P_{out} = 98 W, v_{ac} = 120 V, f_{line} = 60 Hz).

In Figure 4.12, the increased susceptibility of the current sense amplifier to noise and voltage offsets at light currents is demonstrated through a clearing of DCM_{flag} six switching cycles early as the converter transitions into CCM operation. The miniscule error represents 0.28% of switching cycles during the entire 60 Hz ac line cycle.

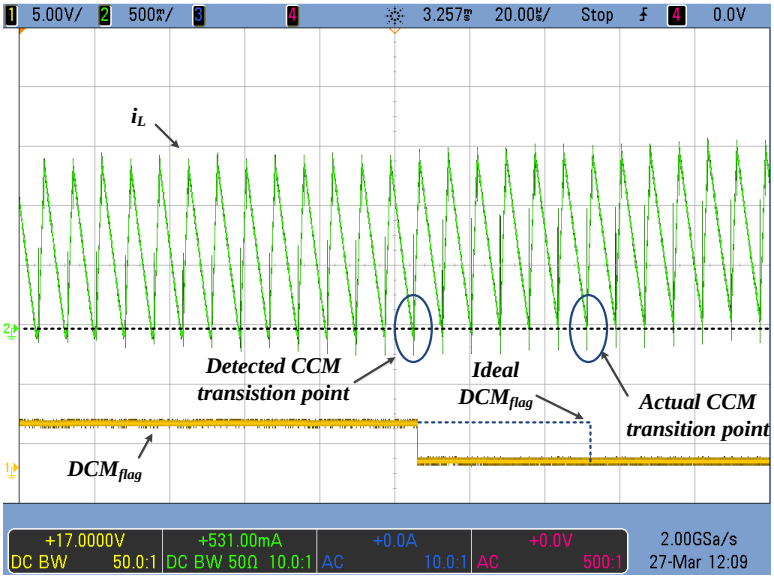


Figure 4.12 Experimental waveform capture of DCM_{flag} detection accuracy with inductor current i_L transitioning from DCM to CCM operation (P_{out} = 98 W, v_{ac} = 120 V, f_{line} = 60 Hz).

4.5 Summary

The experimental results demonstrated success of the proposed DCM detection over the majority of the ac line cycles for all test conditions. As such, the proposed DSP-based detection logic is a suitable alternative to costly auxiliary detection circuits and is therefore an attractive digital replacement for zero-current detection when a DSP with on-board comparators is available. The detection method is computationally simple, uses minimal resources, and allows for accurate detection of zero-current and DCM operation. Furthermore, the integration of the zero-current detection with a DSP opens new possibilities for adaptive digital control techniques, as will be presented in Chapter 5.

5 Adaptive Control of the Boost PFC Converter Operating in Mixed Conduction Mode

5.1 Overview

With the increasing importance of power quality, there has been gaining interest in the control of boost PFC converters operating in both CCM and DCM during a half-line cycle, or otherwise known as MCM [8][24], and [28]-[43]. The respective small-signal characteristics of the boost PFC converter in CCM or DCM have significantly different control requirements depending on the mode of operation, and if a compensator designed for CCM operation is forced to compensate for DCM operation, the converter will exhibit increased harmonic current distortion and reduced power factor due to the improperly compensated dynamics.

Extending the work presented in Chapter 3 and Chapter 4, this chapter introduces an adaptive digital control method for the boost PFC converter under MCM operation. Specifically, the DSP-based DCM detection logic of Chapter 4 is applied to determine the inductor current state such that the average current mode current compensator can be adjusted for either CCM or DCM operation.

The design of the DCM current compensator and modifications to the DSP software are covered in Section 5.2 and 5.3, respectively. As well, detailed experimental results demonstrating the benefits to power quality and harmonic distortion are presented in Section 5.4, followed by a summary in Section 5.5.

5.2 Current Compensator Design in DCM

As shown in Chapter 2, the linearized small-signal model of the DCM boost PFC converter's control-to-output transfer function is given by:

$$G_i^{DCM}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}(s)} = \frac{\frac{2V_o}{L}}{s + \frac{2f_s(V_o - V_M)}{DV_M}}. \tag{5-1}$$

Similarly, the loop gain of the DCM boost PFC is written in (5-2), where C_i^{DCM} is the DCM current loop compensator.

$$T_i^{DCM}(s) = G_i^{DCM}(s)C_i^{DCM}(s)K_sK_{ADC}G_{delay}(s) \tag{5-2}$$

The control-to-output frequency response of the DCM and CCM boost PFC converter is shown in Figure 5.1 for an input voltage of v_{ac} = 240 V. Upon observation, it is evident that the low-frequency gain of the DCM loop is much lower than that of the CCM loop; consequently, the DCM compensator must have an altered set of gains to ensure proper tracking of the reference current in order to account for this difference.

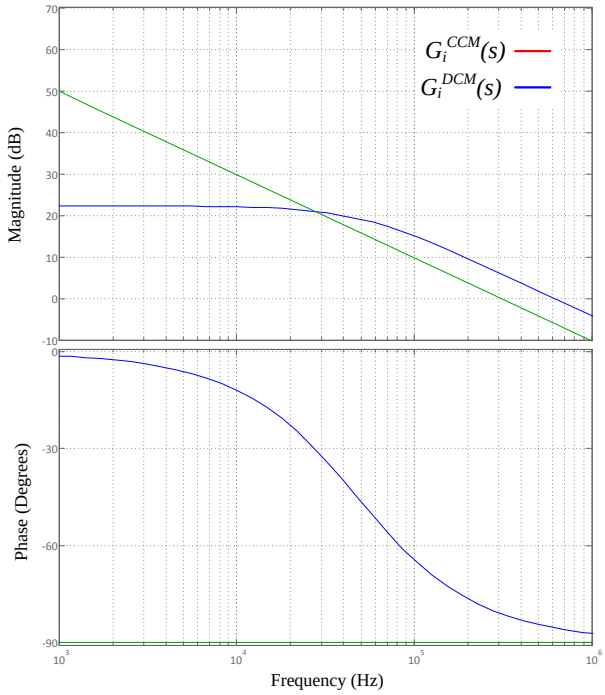


Figure 5.1 Open-loop DCM and CCM control-to-output frequency responses for boost PFC converter (L = 200 µH, f_s = 130 kHz, V_o = 390 V, d = 0.1297, V_M = 340 V).

In the same fashion that the CCM current compensator was designed in Chapter 3, the DCM current compensator is designed in MATLAB to achieve the desired response characteristics. Following discretization of the DCM compensator using the Bilinear Transformation and a sampling rate of T_s of 130 kHz, the current compensator (5-3) gives a loop gain T_i^{DCM} with crossover frequency 15 kHz and a phase margin of 44 degrees.

$$C_i^{DCM}(z) = \frac{0.7403z + 0.3737}{z - 1} \tag{5-3}$$

To highlight the undesirable effect of applying CCM compensation to the boost PFC when it is under DCM operation, the loop gain T_i^{DCM} with the CCM compensator is shown in Figure 5.2. When the CCM compensator is applied to the DCM boost PFC converter, the crossover frequency is reduced and phase margin increases to 2.8 kHz and 121 degrees, respectively. With this reduced performance, the CCM

compensator is unable to track the reference current due to its slow performance when used under DCM operation, thereby contributing to the undesirable traits of greater THD and poorer power factor.

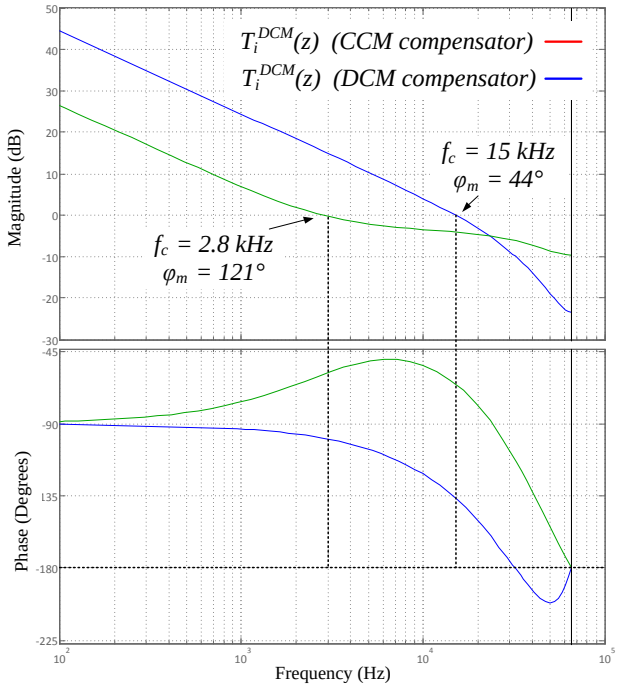


Figure 5.2 Compensated DCM loop gains T_i^{DCM} with both CCM and DCM current compensation schemes. Crossover frequency f_c and phase margin φ_m are highlighted (L = 200 µH, f_s = 130 kHz, V_o = 390 V, d = 0.1297, V_M = 340 V).

5.3 Adaptive MCM Control of the Boost PFC Converter Using DSP-based DCM Detection Logic

With separate compensators designed for CCM and DCM operation, it is possible to use the DSP-based DCM detection logic proposed in Chapter 4 to determine the compensation scheme applicable during each switching period. Depending on whether the boost PFC converter is operating in CCM or DCM, the appropriate DCM or CCM compensator is applied, thereby realizing MCM control. The proposed adaptive control method is illustrated in Figure 5.3, providing a high-level overview of the architecture when applied to a digitally controlled boost PFC converter. The logic is simple in that the

compensator structure remains identical in software, and only the compensator coefficients require modification once CCM or DCM operation is determined.

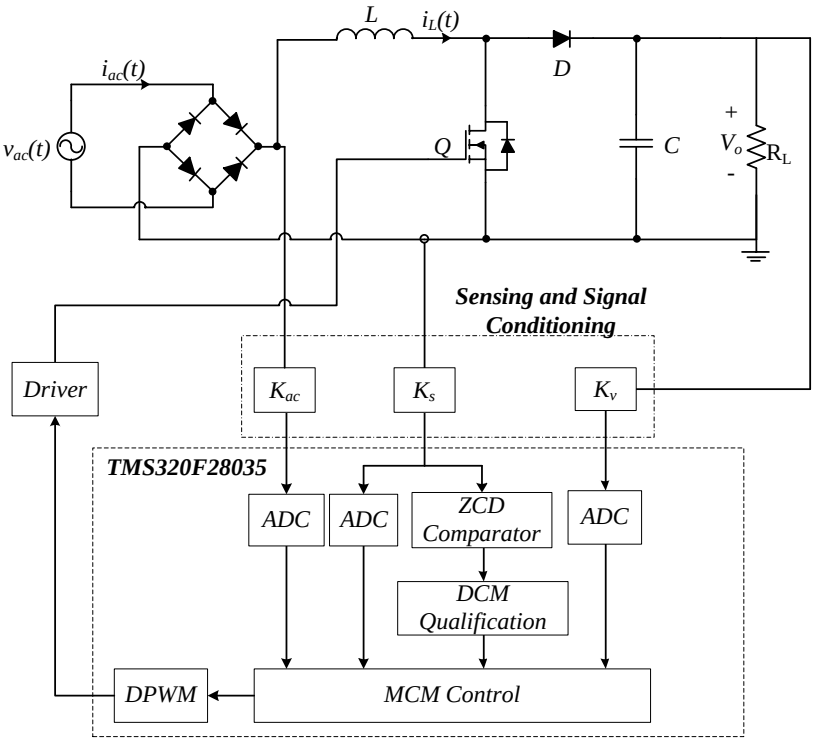


Figure 5.3 Boost PFC converter with high-level digital representation of adaptive MCM control using DSP-based DCM detection logic.

If the DCM_{flag} is set during the immediate switching cycle, the DSP will use the DCM compensator coefficients in the subsequent switching cycles until CCM operation is detected. Inherently, due to the minimum time of one switching cycle necessary to update the duty cycle for the next switching period, the DCM compensator will be delayed during each of its first initializations by an additional switching cycle. Similarly, the same principle of operation applies when the DCM_{flag} is cleared, thus indicating CCM operation. When DCM_{flag} is cleared, the compensator will be updated to use the CCM compensator coefficients until the DCM_{flag} is set again. It is also worth noting that the DCM detection logic is modified

to prevent the coefficients from being unnecessarily updated each switching cycle if the mode of operation has not changed.

5.4 Experimental Results and Discussion

To demonstrate the feasibility of the proposed control method, hereby referred to as the Proposed Controller, a modified digitally controlled boost PFC converter is selected as the test prototype. The boost PFC converter with specifications: L = 200 µH, C = 300 µF, f_s = 130 kHz, and V_o = 390 V is designed for a maximum output power of 650 W and a universal input range (85-264 V). The proposed control method is benchmarked against an Infineon ICE3PCS02G CCM controller IC on an unmodified boost PFC converter, hereby referred to as the Analog Controller, which employs average current mode control with a digital outer voltage loop. Additionally, the Proposed Digital Controller is also benchmarked against the digital average current mode control with a CCM controller only, designed in Chapter 3. This control scheme will be referred to as the Conventional Digital Controller. Total harmonic distortion (THD) and power factor measurements are taken from a Yokogawa WT230 power meter, and a Chroma 61605 programmable AC source is used as the input source.

Power factor and THD measurements are experimentally recorded with output powers P_{out} of 49 W to 650 W. Input voltages v_{ac} of 120 V and 240 V are used to simulate typical low and high line conditions.

5.4.1 Experimental Results for v_{ac} = 120 V

Total harmonic distortion and power factor experimental results of the Analog, Conventional Digital, and Proposed Digital Controllers at v_{ac} = 120 V are summarized numerically in Table 5.1 and graphically in Figure 5.4 and Figure 5.5.

Table 5.1 Summary of experimental power factor and THD measurements for various output power for each of the Analog, Conventional Digital, and Proposed Digital Controllers (v_{ac} = 120 V, f_{line} = *60* Hz)

P_{out} [W]	Analog Controller		Conventional Digital Controller		Proposed Digital Controller	
	Power factor	THD [%]	Power factor	THD [%]	Power Factor	THD [%]
49	0.9521	17.71	0.9741	15.89	0.9830	13.16
98	0.9854	4.70	0.9752	6.81	0.9893	4.07
195	0.9955	4.11	0.9949	3.28	0.9967	3.27
260	0.9976	3.66	0.9971	2.42	0.9978	2.41
325	0.9982	3.41	0.9982	1.98	0.9985	1.92
390	0.9985	3.17	0.9988	1.66	0.9990	1.56
455	0.9987	3.11	0.9991	1.43	0.9993	1.31
520	0.9988	3.02	0.9994	1.26	0.9995	1.12
585	0.9990	2.82	0.9995	1.13	0.9996	1.03
650	0.9990	2.87	0.9995	1.04	0.9998	0.94

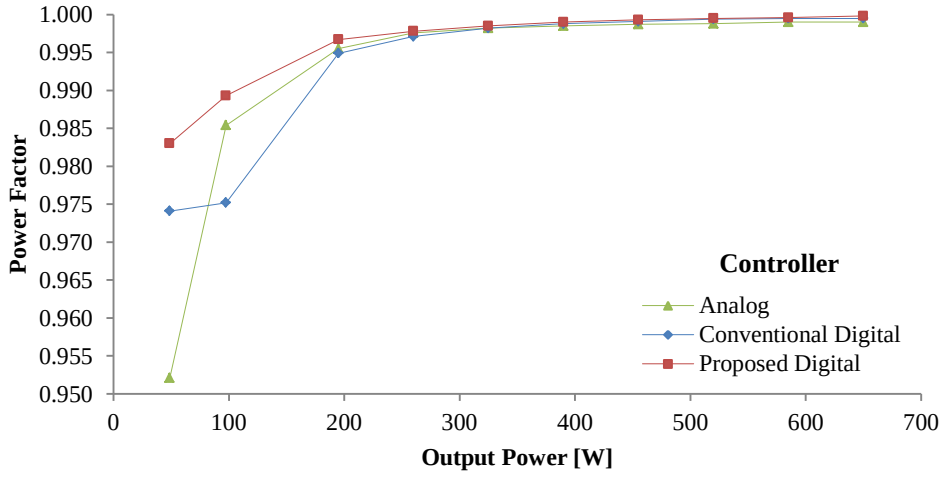


Figure 5.4 Power factor experimental results for the Analog, Conventional Digital, and Proposed Digital Controllers with output powers P_{out} of 49 W to 650 W at v_{ac} = 120 V.

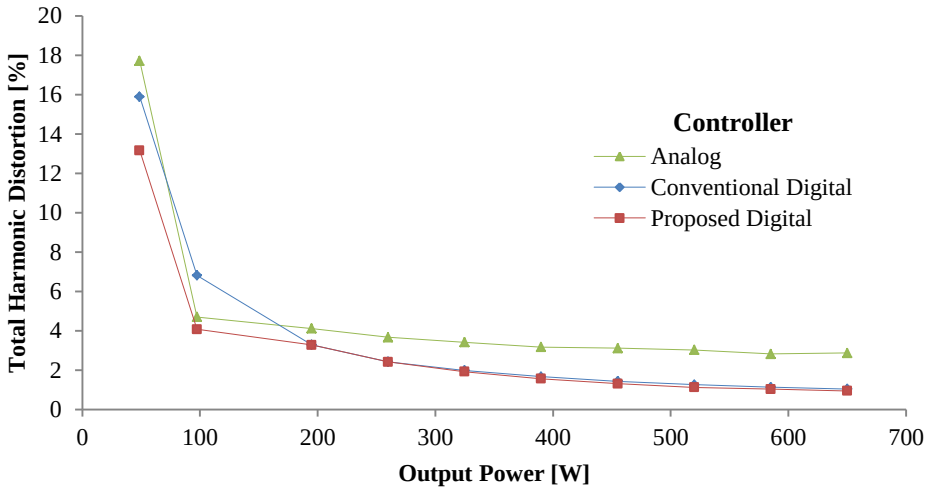
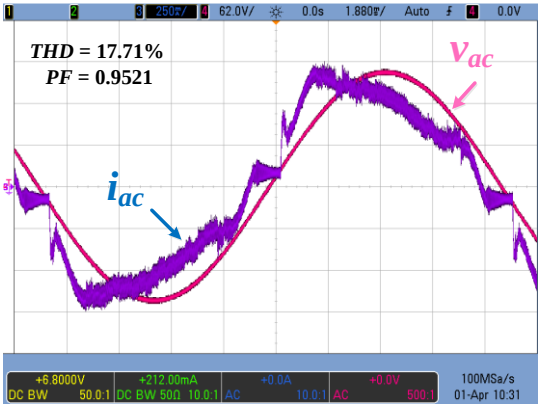


Figure 5.5 Total harmonic distortion experimental results for the Analog, Conventional Digital, and Proposed Digital Controllers with output powers P_{out} of 49 W to 650 W at v_{ac} = 120 V.

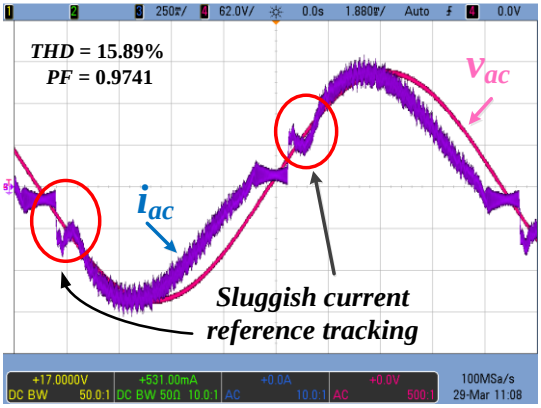
The superior performance of the Proposed Digital Controller is evident when compared with the Analog and Conventional Digital Controllers. It is worth noting that the Proposed Digital Controller always displays greater power factor and less THD than the Analog Controller at all power levels. Additionally, the Proposed Digital Controller also provides equivalent or greater power factor, and less THD when compared to the Conventional Digital Controller, at all output power levels.

Observing Figure 5.6, the Analog Controller in Figure 5.6 (a) provides the most distorted current and poorest power factor of all controllers for an output power of 49 W. The Conventional Digital Controller in Figure 5.6 (b) shows poor current-tracking ability near the zero crossings of the line current, resulting in greater THD and a lower power factor than the Proposed Digital Controller of Figure 5.6 (c). The Proposed Digital Controller displays the highest quality input current of all controllers due to its ability to better track the reference current as the converter operates in DCM. The Proposed Digital Controller realizes power factor improvements of 3.14% over the Analog Controller at the lightest output power, and THD improvements of 26%, or a 4.5% absolute difference.

a) Analog Controller



b) Conventional Digital Controller



c) Proposed Digital Controller

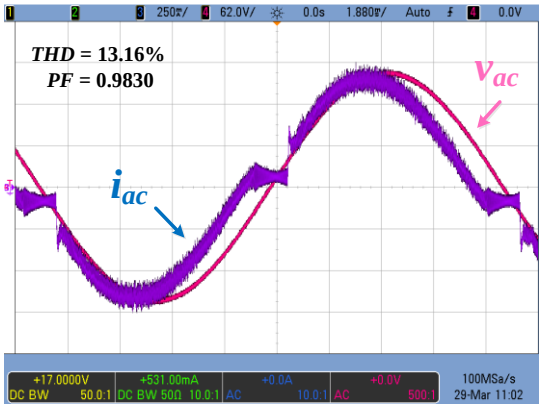
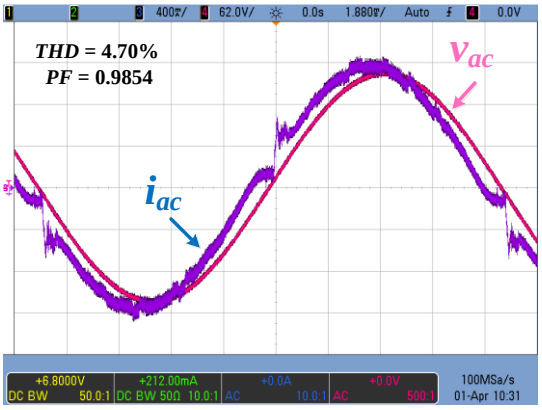


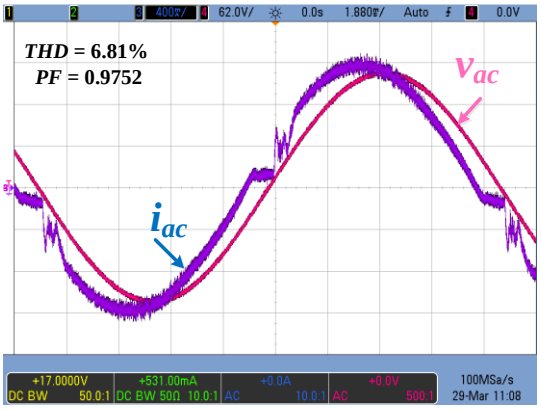
Figure 5.6 Experimental waveform captures of line current i_{ac} and line voltage v_{ac} with different controller configurations. DCM operation over the entire line cycle is observed. (P_{out} = 49 W, v_{ac} = 120 V, f_{line} = 60 Hz).

Figure 5.7 (c) illustrates the smoother line current of the Proposed Digital Controller and better power factor, in contrast to the other waveforms in Figures 5.7 (a)-(b) at P_{out} = 98 W. As the power level increases further, the boost PFC converters begins to operate in CCM for the majority of the ac half-line cycle, the DCM compensator in the Proposed Digital Controller is applied less frequently, as expected. The DCM_{flag}, however, is still triggered in brief moments near the zero-crossing of the ac line voltage, accounting for minor improvements to THD over the other controllers.

a) Analog Controller



b) Conventional Digital Controller



c) Proposed Digital Controller

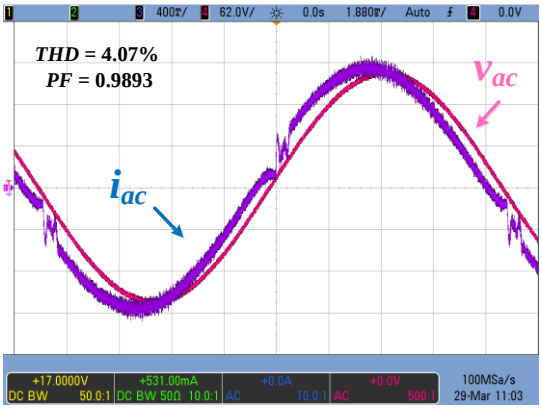
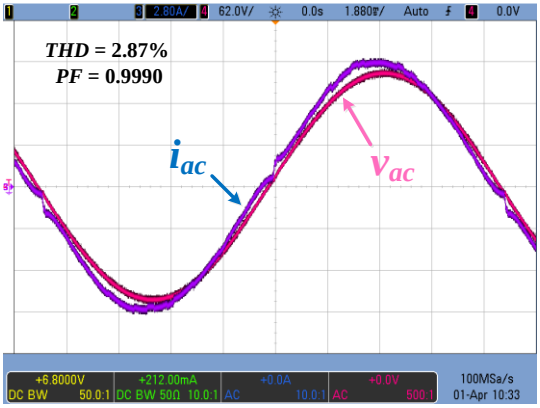


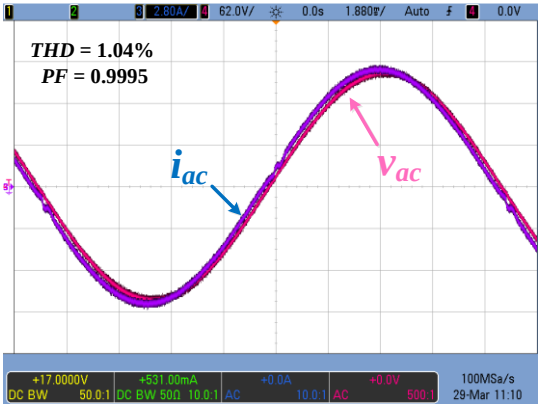
Figure 5.7 Experimental waveform captures of line current i_{ac} and line voltage v_{ac} with different controller configurations. MCM operation over the line cycle is observed. (P_{out} = 98 W, v_{ac} = 120 V, f_{line} = 60 Hz).

In Figure 5.8, waveform captures are provided for P_{out} = 650 W for sustained CCM operation. The high-quality and low-distortion line current waveforms of the both digital controllers are visible. The Proposed Digital Controller displays the highest quality current, due to the DCM compensator application in the brief DCM periods near the zero crossings of the ac line voltage.

a) Analog Controller



b) Conventional Digital Controller



c) Proposed Digital Controller

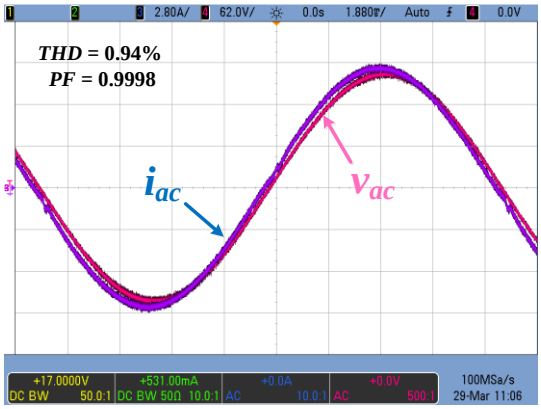


Figure 5.8 Experimental waveform captures of line current i_{ac} and line voltage v_{ac} with different controller configurations. CCM operation over the line cycle is observed. (P_{out} = 650 W, v_{ac} = 120 V, f_{line} = 60 Hz).

5.4.2 Experimental Results for v_{ac} = 240 V

The experimental results providing total harmonic distortion and power factor of the Analog, Conventional Digital, and Proposed Digital Controllers at v_{ac} = 240 V are summarized numerically in Table 5.2 and graphically in Figure 5.9 and Figure 5.10.

Table 5.2 Summary of experimental power factor and THD measurements for various output power for each of the Analog, Conventional Digital, and Proposed Digital Controllers (v_{ac} = 240 V, f_{line} = 60 Hz)

P_{out} [W]	Analog Controller		Conventional Digital Controller		Proposed Digital Controller	
	Power factor	THD [%]	Power factor	THD [%]	Power Factor	THD [%]
49	0.6845	43.01	0.8032	42.54	0.8034	42.84
98	0.8244	25.97	0.8904	36.09	0.8960	34.14
195	0.9529	15.95	0.9541	21.42	0.9653	18.27
260	0.9759	8.73	0.9701	14.33	0.9789	11.02
325	0.9841	4.97	0.9797	11.65	0.9844	8.76
390	0.9878	4.06	0.9761	8.46	0.9845	6.54
455	0.9903	3.71	0.9812	5.86	0.9835	5.48
520	0.9921	3.15	0.9855	4.63	0.9855	4.50
585	0.9933	2.85	0.9885	3.83	0.9885	3.75
650	0.9942	2.79	0.9909	3.29	0.9909	3.17

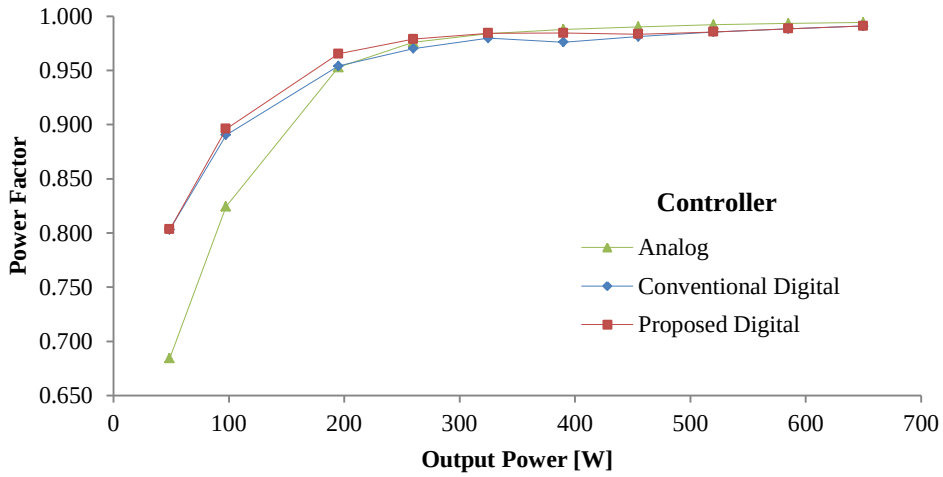


Figure 5.9 Power factor experimental results for the Analog, Conventional Digital, and Proposed Digital Controllers with output powers P_{out} of 49 W to 650 W at v_{ac} = 240 V

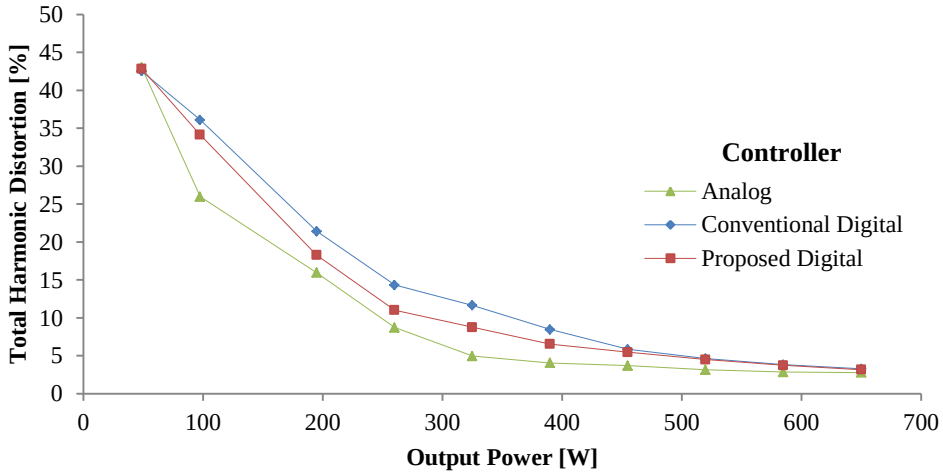


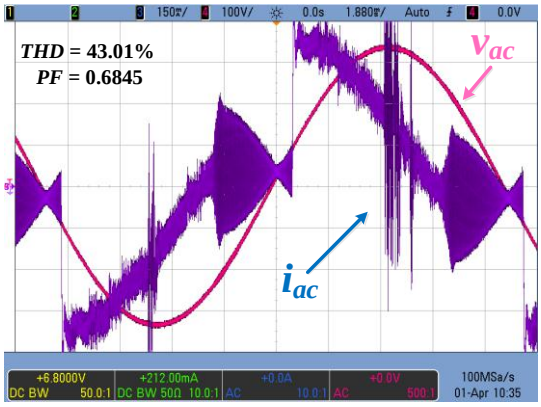
Figure 5.10 Total harmonic distortion experimental results for the Analog, Conventional Digital, and Proposed Digital Controllers with output powers P_{out} of 49 W to 650 W at v_{ac} = 240 V.

The Proposed Digital Controller displays the greatest power factor of all controllers from output powers 49 W to 325 W, but its total harmonic distortion is not lower than the Analog Controller due to poor current sensing accuracy with smaller input current, as dictated by the 240 V operating condition. To its benefit, the Analog Controller IC is physically mounted in close proximity to the sense resistor, thereby mitigating the aforementioned disadvantages.

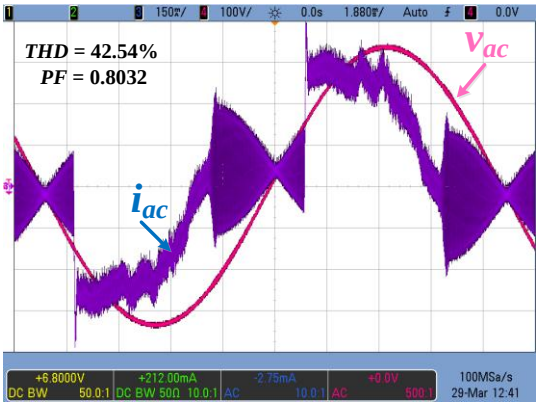
In comparison with only the Conventional Digital Controller, however, the Proposed Digital Controller exhibits noticeable improvements in THD and power factor from power levels of P_{out} = 195 W to 390 W. At P_{out} = 260 W, the THD of the Proposed Digital Controller is reduced by 3.31% over the Conventional Digital controller.

In pure DCM operation at P_{out} = 49 W, all controllers display significant harmonic distortion, as visible in Figure 5.11. The Digital Controllers, though, provide significantly greater power factors than that Analog Controller at lower input powers of P_{out} = 49 – 98 W.

a) Analog Controller



b) Conventional Digital Controller



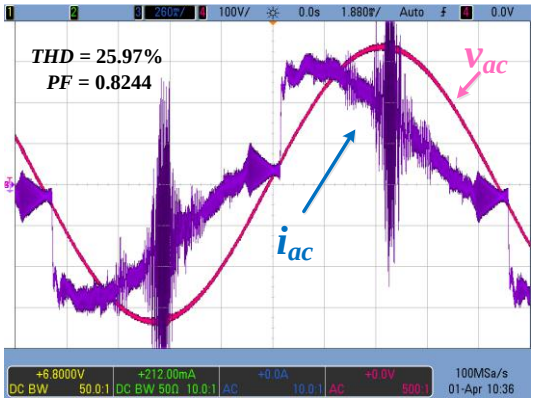
c) Proposed Digital Controller

Figure 5.11 Experimental waveform captures of line current i_{ac} and line voltage v_{ac} with different controller configurations. DCM operation over the entire line cycle is observed. (P_{out} = 49 W, v_{ac} = 240 V, f_{line} = 60 Hz).

Figure 5.12 provides experimental waveform captures for all controllers under MCM operation at an output power level of 98 W. The Analog Controller in Figure 5.12 (a) provides the most graduated reference current tracking of all controllers, although there are short bursts of current-loop instability near the peaks of the input voltage. Observing the intervals near the zero crossings of the input voltage, line

current oscillation is more pronounced with the Conventional Digital Controller in Figure 5.12 (b) and the Proposed Digital Controller from Figure 5.12 (c), leading to an overall greater THD. The Proposed Digital Controller, however, shows a less aggressive line current, and provides a slightly greater power factor and lower THD over the Conventional Digital Controller.

a) Analog Controller



b) Conventional Digital Controller

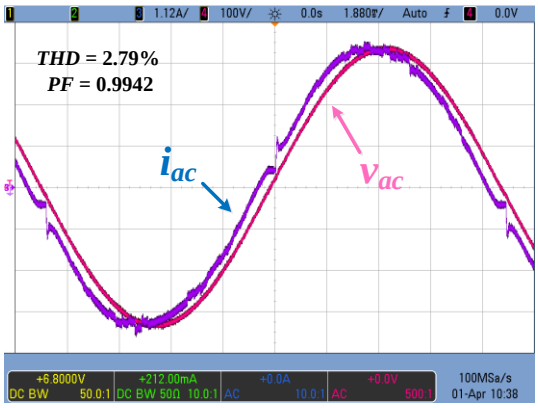
c) Proposed Digital Controller

Figure 5.12 Experimental waveform captures of line current i_{ac} and line voltage v_{ac} with different controller configurations. MCM operation over the line cycle is observed. (P_{out} = 98 W, v_{ac} = 240 V, f_{line} = 60 Hz).

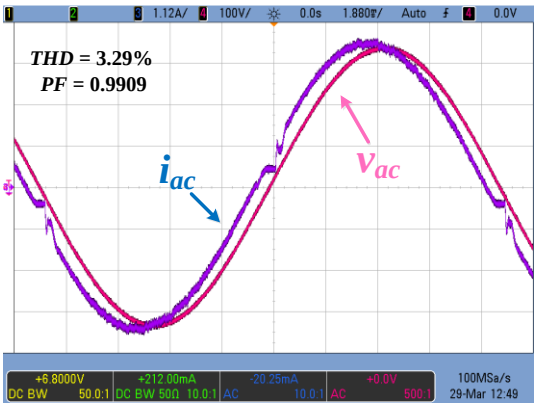
In CCM operation at a full load of 650 W, the waveform captures of Figure 5.13 show the similar performance of all controllers. The input current with the Analog Controller, Figure 5.13 (a), however, is less distorted near the input voltage zero crossings, although appears more distorted than the

Conventional Digital Controller, Figure 5.13 (b), and Proposed Digital Controller, Figure 5.13 (c), during the remaining periods. Additionally, the input current in Figure 5.13 (a) is slightly more in-phase with the input voltage, contributing to a greater power factor. Performance of the Conventional Digital Controller and Proposed Digital Controller is nearly identical at full load.

a) Analog Controller



b) Conventional Digital Controller



c) Proposed Digital Controller

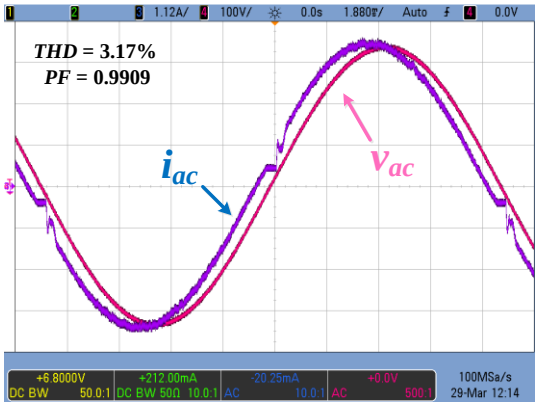


Figure 5.13 Experimental waveform captures of line current i_{ac} and line voltage v_{ac} with different controller configurations. CCM operation over the line cycle is observed. (P_{out} = 650 W, v_{ac} = 240 V, f_{line} = 60 Hz).

It is worth noting that a significant concern is the fidelity of the current sense amplifier output. As the current sense amplifier is located off-board and at a considerably greater distance compared to traditional current sensing techniques, it has a greater susceptibility to EMI and other sources of noise.

These current sense waveforms are presented in Figure 5.14 and Figure 5.15. Furthermore, the small but substantial voltage drop across the sense lines results in a detrimental contribution to current sense distortion. Lower voltage drops over the sense resistor, corresponding to lower input currents, result in reduced performance, as the current sense amplifier cannot faithfully amplify the sensed inductor current. With a four-terminal sensing, shortened distances, and with on printed circuit board (PCB) design, improvements to the current sense amplifier are realizable; however, for the modified prototype implementing this sensing method is impossible, but can be incorporated easily into later PCB redesigns.

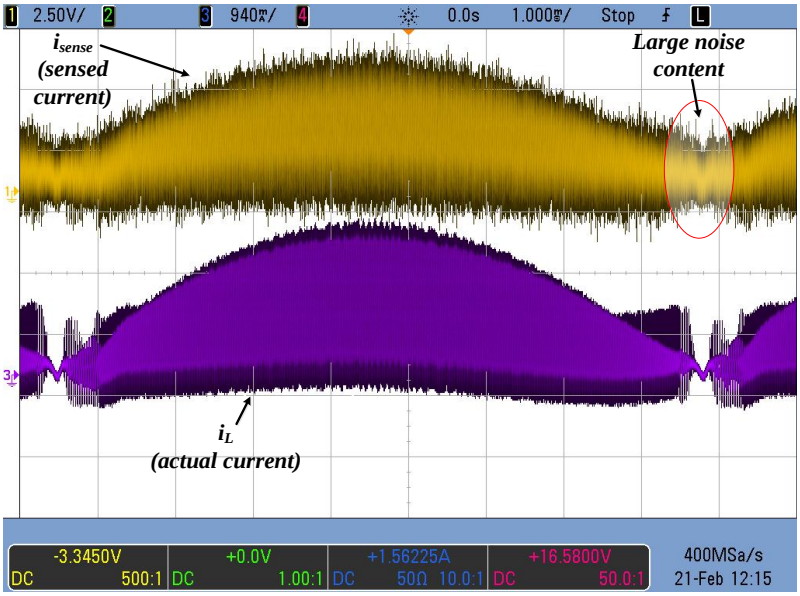


Figure 5.14 Waveform capture demonstrating effect of noise on sensed inductor current i_{sense} when compared to actual inductor current i_L.

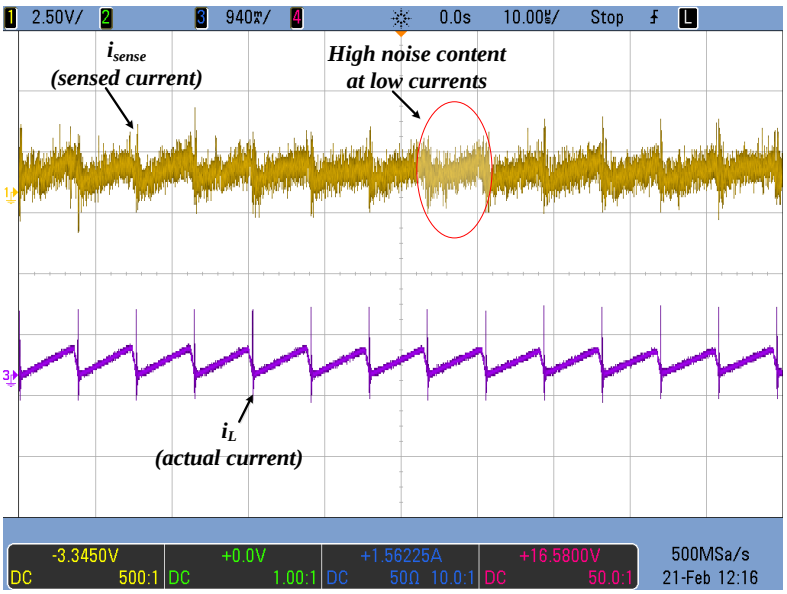


Figure 5.15 Zoomed-in waveform capture demonstrates high noise on sensed inductor current i_{sense} during low output powers and input current, leading to poor average current sensing.

5.5 Summary

Depending on the output power and input voltage, the boost PFC converter will operate in CCM, DCM, or MCM over the entire ac half-line cycle. If the boost PFC converter is operated in DCM with a CCM comparator, compensation is inadequate leading to poor reference current tracking, and thus poor THD and power factor.

The contribution of this thesis chapter was the application of a DSP-based DCM detection logic proposed earlier in Chapter 4 to an MCM boost PFC converter for detection and compensation of DCM operation. Following the detection of the mode, either a CCM or DCM compensator was applied for power quality improvements. Design of the DCM current compensator and modification to the proposed DSP-based detection logic to realize an adaptive control method was covered.

A boost PFC converter controlled by an analog IC, and a modified boost PFC converter with both conventional and the proposed adaptive digital controller, were benchmarked against one another.

Experimental performance data was compared and the Proposed Digital Controller realized a maximum improvement in power factor of 3.25% and a THD improvement of 4.55% over the Analog Controller, at v_{ac} = 120V and P_{out} = 49 W. Moreover, the Proposed Digital Controlled displayed superior THD and power factor performance over the Analog Controller and Conventional Digital Controller for all powers at v_{ac} = 120 V. Performance improvements over the Conventional Digital Controller were seen at a higher line voltage of v_{ac} = 240 V, but poor current sensing at low in output power resulted in no THD improvement when the Proposed Digital Controller was compared with the Analog Controller. There were, however, improvements of up to 17.4% in power factor with the Conventional Digital Controller at low input powers.

Overall, the Proposed Digital Controller employing DSP-based DCM detection logic for adaptive control techniques displayed improved THD and power factor performance at low line voltages. It was proposed that improvements at higher line voltages are possible by placing the current-sense amplifier closer to the sense resistor, thereby reducing the sensed inductor current susceptibility to noise and voltage drops. The control method is simple to implement, and shows performance advantages over the Conventional Digital Controller through a simple software modification and application of a DSP on-board comparator.

6 Conclusions and Future Work

6.1 Conclusions

The growing demand and necessity of high-quality input current for electronic devices has been met with stringent standards such as the EN-61000-3-2, which limit harmonic current content, and the ENERGY STAR program. As a contribution to this developing area of power electronic, this thesis contributed control techniques enabling improvements in power quality. They are summarized in the following sections.

6.1.1 Digital Design Considerations for the Modification of an Analog IC-controlled Boost PFC Converter

With the absence of literature describing the complete modification of a boost PFC converter controlled by an analog IC for digital operation, Chapter 3 provides a detailed overview into the necessary design and modification considerations when converting such a boost PFC converter. This chapter describes the design requirements of the analog-interfacing circuitry, the selection of the DSP, the design of the current loop compensator, and an overview of the software requirements and performance. Experimental results demonstrate the success of modification and allow future and rapid prototyping of additional digital control techniques.

6.1.2 DSP-based DCM Detection for Boost PFC Converters

In Chapter 4, the second contribution of this thesis provides a novel DSP-based DCM detection logic. This detection logic is suitable for detecting zero current in the boost PFC converter in a simple and effective manner. Consequently, this detection technique can be applied for detection of the DCM operation intervals. The proposed logic enables simplification and cost-reduction over existing DCM and zero-current detection methods, while taking full advantage of existing on-board comparators found on many DSP devices. This method is computationally simple, and features additional logic to filter and

ignore erroneous or spurious events. Experimental results of the detection logic applied to a modified boost PFC converter provide evidence of effectiveness of this proposed method.

6.1.3 Adaptive Control of the Boost PFC Converter Operating in Mixed Conduction Mode

The final contribution of this thesis is the application of the proposed DSP-based DCM detection logic to a boost PFC converter operating in both the continuous and discontinuous conduction modes. The DCM current compensator design and the trivial modifications to the software for adaptive MCM control are shown. The DSP-based detection logic is used to select the appropriate compensator for the detected mode of operation. The MCM control technique is applied to a boost PFC converter, and is benchmarked against a conventional digital average current mode control technique and a commercially available PFC control IC. Experimental results show the proposed MCM control technique demonstrates improved performance over both the analog IC controller and conventional digital controller at an input voltage of 120 V. A discussion of the fidelity limitations of the off-board current sensing circuitry and its impact on power quality is also presented.

6.2 Future Work

This section provides possible recommendations to expand on the work done in this thesis.

6.2.1 Improved Current Sensing Accuracy

As the modified boost PFC converter has off-board sensing circuitry, it is subjected to additional noise and voltage drops when compared to sensing circuitry located on-board and in close proximity to the sensing nodes. With a higher quality reproduction of the inductor current, the sensed current would better represent the average current near light loading and the zero crossings of the input voltage. Consequently, it may be possible to realize THD and power factor improvements over the analog IC

controller at all input voltage levels and loads. A redesigned printed circuit board layout would be required in this case.

6.2.2 Experimentation with Reduced Switching Frequencies

Although the modified design required a switching frequency of 130 kHz, which is demanding for PFC control with today's DSPs, a reduction of the switching frequency to a lower value such as 20 kHz or 50 kHz may result in improved THD and power factor with the proposed MCM control. Occasionally, due to the single-threaded architecture of the DSP, some zero-current events may be missed or falsely detected leading to the application of the CCM compensator in DCM mode or vice-versa. With a reduced switching speed, the DSP would have more time to service the zero-current events, and therefore provide potentially greater power quality.

6.2.3 Estimation of the Discontinuous Conduction Interval in DCM Operation

Further research into the accurate detection of the discontinuous conduction interval length may allow further improvements in power quality during DCM operation. As explained in Chapter 2, the discontinuous conduction interval length can be used to compute a current correction factor κ, allowing correct computation of the average current when sampled at the midpoint of the inductor slope in DCM operation. With proper average current, average current mode can be applied to realize potential improvements in power quality over the uncorrected average current mode control method.

References

[1] Limits for Harmonic Current Emissions (Equipment Input Current < 16A per Phase), IEC 1000-3-2 Int. Std., 2001.

[2] Agilent, “Agilent AN 1273 Compliance Testing to the IEC 1000-3-2 (EN 61000-3-2) and IEC 1000-3-3 (EN 61000-3-3) Standards Application Note,” AN 1273, 2000

[3] 80 PLUS, [Online]: Available: http://www.plugloadsolutions.com/

[4] “IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems," IEEE Std 519-1992 , vol.,e no., pp.0_1, 1993

[5] W. M. Grady, S. Santoso, "Understanding Power System Harmonics," *Power Engineering Review, IEEE* , vol.21, no.11, pp.8-11, Nov. 2001

[6] R. Redl, "Electromagnetic environmental impact of power electronics equipment", *Proc. IEEE*, vol. 89, pp.926 -938 2001

[7] W. E. Reid,"Power quality issues-standards and guidelines," *Industry Applications, IEEE Transactions on*, vol. 32, pp. 625-632, 1996.

[8] R. W. Erickson, D. Maksimovic, *Fundamentals of Power Electronics.* Secaucus, NJ, USA: Kluwer Academic Publishers, 2001.

[9] D. Maksimovic, R. Zane and R. Erickson, "Impact of digital control in power electronics," in *Power Semiconductor Devices and ICs, 2004. Proceedings. ISPSD '04. the 16th International Symposium on,* 2004, pp. 13-22.

[10] D. M. Mitchell, “AC-DC converter having an improved power factor,” U.S. Patent 4 412 277, Oct. 25, 1983.

[11] S.D. Freeland, *Input-current shaping for single-phase AC-DC power converters.* Dissertation (Ph.D.), California Institute of Technology.

[12] H.Wei, I. Batarseh, "Comparison of basic converter topologies for power factor correction," in *Southeastcon '98. Proceedings. IEEE,* 1998, pp. 348-353.

[13] O. Garcia, J. A. Cobos, R. Prieto, P. Alou and J. Uceda, "Single phase power factor correction: a survey," *Power Electronics, IEEE Transactions on,* vol. 18, pp. 749-755, 2003

[14] R. Martinez and P. N. Enjeti, "A high performance single phase AC to DC rectifier with input power factor correction," *IEEE Trans. Power Electron.,* vol. 11, no. 2, pp. 311–317, Mar. 1996

[15] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *Industrial Electronics, IEEE Transactions on,* vol. 50, pp. 962-981, 2003.

[16] M. Madigan, R. Erickson and E. Ismail, "Integrated high quality rectifier-regulators," *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE* , vol., no., pp.1043-1051 vol.2, 29 Jun-3 Jul 1992.

[17] T. Nussbaumer, K. Raggl and J. W. Kolar, "Design Guidelines for Interleaved Single-Phase Boost PFC Circuits," *Industrial Electronics, IEEE Transactions on,* vol. 56, pp. 2559-2573, 2009.

[18] C. Zhou and M. M. Jovanovic, "Design Trade-off in continuous current mode controlled boost power factor correction circuits," Virginia Power Electronics Seminar, 1992, pp.57-68

[19] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.,* vol. 23, no. 3, pp. 1381–1390, May 2008.

[20] A. Prodic, J. Chen, D. Maksimovic, and R. W. Erickson, "Self-tuning ´digitally controlled low-harmonic rectifier having fast dynamic response*," IEEE Trans. Power Electron*., vol. 18, no. 1, pp. 420–428, Jan.2003.

[21] S. Buso, P. Mattavelli, L. Rossetto, and G. Spiazzi, "Simple digital control improving dynamic performance of power factor preregulators," *IEEE Trans. Power Electron*., vol. 13, no. 5, pp. 814–423, Sep.1998.

[22] J. Sun, "On the zero-crossing distortion in single-phase PFC converters," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 685-692, 2004.

[23] K. De Gusseme, D. M. Van de Sype, A. P. M. Van den Bossche and J. A. Melkebeek, "Digitally controlled boost power-factor-correction converters operating in both continuous and discontinuous conduction mode," *Industrial Electronics, IEEE Transactions on,* vol. 52, pp. 88-97, 2005.

[24] K. De Gusseme, D. M. Van de Sype, A. P. M. Van den Bossche and J. A. Melkebeek, "Input-Current Distortion of CCM Boost PFC Converters Operated in DCM," *Industrial Electronics, IEEE Transactions on,* vol. 54, pp. 858-865, 2007.

[25] T. Hwang; S. Park; , "Seamless boost converter control in critical boundary condition for fuel cell power conditioning system," *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE* , vol., no., pp.3641-3648, 17-22 Sept. 2011

[26] F. Tahami, B. Gholami and H. M. Ahmadian, "Modeling of the boost power factor correction rectifier in mixed conduction mode using PWA approximation," in *Industrial Electronics, 2008. ISIE 2008. IEEE International Symposium on,* 2008, pp. 190-195.

[27] B. Abdi, A. H. Ranjbar, J. Milimonfared and G. B. Gharehpetian, "Reliability comparison of boost PFC converter in DCM and CCM operating modes," in *Power Electronics, Electrical Drives, Automation and Motion, 2008. SPEEDAM 2008. International Symposium on,* 2008, pp. 939-943.

[28] L. Dixon, "Average current mode control of switching power supplies," in Proc. Unitrode Power Supply Design Sem., 1990

[29] P. C. Todd, "UC3854 Controlled Power Factor Correction Circuit Design," Unitrode Application Note, 1998.

[30] J. Chen, A. Prodic, R. W. Erickson and D. Maksimovic, "Predictive digital current programmed control," *Power Electronics, IEEE Transactions on,* vol. 18, pp. 411-419, 2003.

[31] W. Zhang, G. Feng, Y. Liu and Bin Wu, "A direct duty cycle calculation algorithm for digital power factor correction (PFC) implementation," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual,* 2004, pp. 2326-2332 Vol.3.

[32] W. Zhang, G. Feng, Y. Liu, B. Wu, "A digital power factor correction (PFC) control strategy optimized for DSP," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 1474-1485, 2004.

[33] Fairchild Semiconductor. "FAN7930 Critical Conduction Mode PFC Controller," FAN7930, Apr. 2010.

[34] K. De Gusseme, W. R. Ryckaert, D. M. Van de Sype, J. A. Gijselen and J. A. Melkebeek, "A boost PFC converter with programmable harmonic resistance," in *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE,* 2005, pp. 1621-1627 Vol. 3

[35] D. M. Van de Sype, K. De Gusseme, A. P. Van den Bossche and J. A. A. Melkebeek, "A sampling algorithm for digitally controlled boost PFC converters," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 649-657, 2004.

[36] K. De Gusseme, D. M. V. de Sype, A. P. Van den Bossche and J. A. Melkebeek, "Sample correction for digitally controlled boost PFC converters operating in both CCM and DCM," in *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE,* 2003, pp. 389-395 vol.1.

[37] D. M. van de Sype et al., "Duty-ratio feedforward for digitally controlled boost PFC converters," in *Proc. IEEE Applied Power Electron. Conf.* 2003, pp. 396–402.

[38] J. Zhou, Z. Lu, Z. Lin, Y. Ren, Z. Qian, and Y. Wang, "Novel sampling algorithm for DSP controlled 2kW PFC converter", *IEEE Trans. Power Electron.,* vol. 16, pp.217 -222 2001

[39] S. Moon, L. Corradini and D. Maksimović, "Accurate mode boundary detection in digitally controlled boost power factor correction rectifiers," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE,* 2010, pp. 1212-1217.

[40] S. Moon, L. Corradini and D. Maksimović, "Autotuning of Digitally Controlled Boost Power Factor Correction Rectifiers," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 3006-3018, 2011.

[41] L. Roggia, F. Beltrame, J. E. Baggio and J. R. Pinheiro, "Digital control system applied to a PFC boost converter operating in mixed conduction mode," in *Power Electronics Conference, 2009. COBEP '09. Brazilian,* 2009, pp. 698-704.

[42] F. Chen "Digital Control Techniques for Efficiency Improvements in Single-Phase Boost Power Factor Correction Rectifiers.", PhD Thesis, University of Colorado, United States, 2010.

[43] F. Chen and D. Maksimović, "Digital Control for Improved Efficiency and Reduced Harmonic Distortion Over Wide Load Range in Boost PFC Rectifiers," *Power Electronics, IEEE Transactions on,* vol. 25, pp. 2683-2692, 2010.

[44] C. Ku, D. Chen and S. Lin, "A new control scheme for boost PFC converters for both CCM and DCM operations," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE,* 2011, pp. 1334-1338.

[45] Y. Uno, "Power Factor Correction Converter," U.S Patent 2011/211377 A1, May 13, 2011.

[46] S. F. Lim and A. M. Khambadkone, "A Simple Digital DCM Control Scheme for Boost PFC Operating in Both CCM and DCM," *Industry Applications, IEEE Transactions on,* vol. 47, pp. 1802-1812, 2011.

[47] X. Zhang and J. W. Spencer, "Analysis of Boost PFC Converters Operating in the Discontinuous Conduction Mode," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 3621-3628, 2011.

[48] C. Liou, H. Chieh and W. Liou, "Design and implementation of a boost power factor correction stage operated in mixed-conduction mode," in *Electric Information and Control Engineering (ICEICE), 2011 International Conference on,* 2011, pp. 2069-2072.

[49] M. S. Fadali, A. Visioli. *Digital Control Engineering: Analysis and Design.* Burlington, MA, USA: Academic Press, 2009.

[50] Texas Instruments. ” Transition Mode PFC Controller,” SLUS515F, Mar. 2009.

[51] Kaźmierkowski, M.P., Krishnan, R., *Control in Power Electronics: Selected Problems.* Academic Press, 2002.

[52] Texas Instruments. “C28x Digital Power Library: Module User’s Guide,” DPLib, v. 3.2, Mar. 2011.

[53] Texas Instruments. “TMS320F20835 Datasheet,” SPRS584G, Mar. 2012.

[54] Texas Instruments.“TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide,” SPRUGE5F, Dec. 2011.

[55] Texas Instruments. ” TMS320C28x DSP CPU and Instruction Set Reference Guide (Rev. E),” SPRU430E, Jan. 2009.

[56] Texas Instruments. ”TMS320x2802x, 2803x Piccolo Enhanced Pulse Width Modulator (ePWM) Module UG (Rev. E),” SPRUGE5F, Mar. 2011.

[57] Texas Instruments. “C2000 Microcontrollers Brochure (Rev. L),” SPRB176L, 2011.

[58] Microchip. “dsPIC30F1010/202X Data Sheet,” DS70178C, 2006.

[59] H. Sino. “High-Side Current Sensing: Difference Amplifier vs. Current-Sense Amplifier,” Analog Dialogue 42-01, Jan 2008.

[60] B. Mammano. “Current Sensing Solutions for Power Supply Designers,” Unitrode Power Supply Seminar, Seminar 1200 Topic 1. 2001.

[61] Texas Instruments. “OPA350 Data Sheet,” SBOS099C, Jan. 2005.

[62] Powersim, “PSIM User Manual,” www.powersimtech.com.

Appendices

Appendix A: PSIM Simulation Schematic

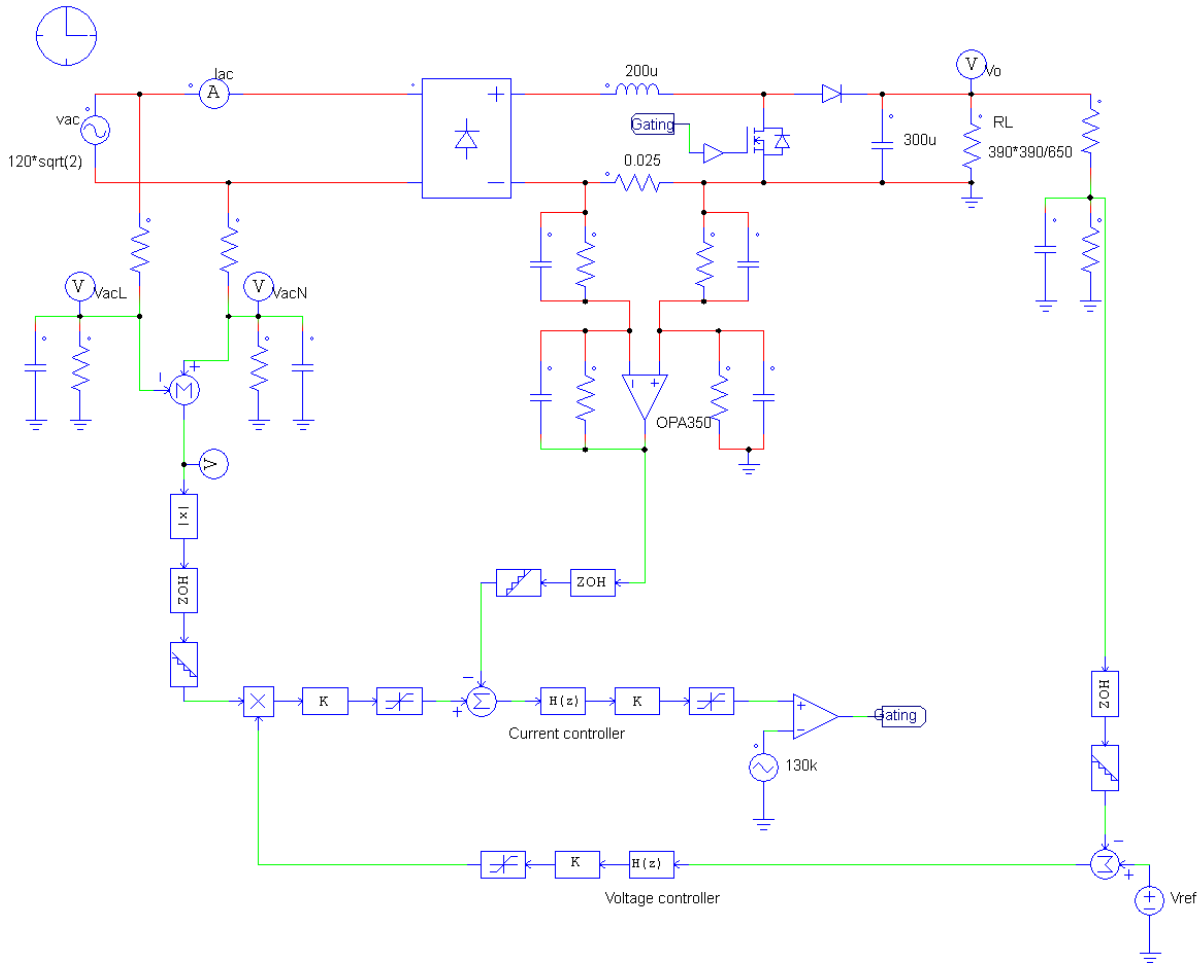


Figure A.1 PSIM simulation schematic for digital average current mode control.