A PREDICTIVE ANALOG DEAD-TIME CONTROL CIRCUIT FOR A HIGH EFFICIENCY SYNCHRONOUS BUCK CONVERTER

by

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Abstract

The synchronous buck DC-DC power converter is the most common switching converter circuit used to step down a DC input voltage to a low logic level DC output voltage in computer applications. The synchronous buck converter has two power MOSFET switches that turn on in a complementary fashion. However, to avoid high input current spikes, a short duration of dead-time (i.e. a time interval when neither switch is on) is required. During dead-time intervals, the buck converter synchronous MOSFET internal body diode conducts the high inductor current, leading to high losses. To minimize this loss, a dead-time controller circuit is required to minimize the dead-time.

The majority of existing predictive dead-time controllers are digital. These dead-time controllers have problems caused by their discrete output including dithering in steady state and reduced accuracy. Furthermore, existing dead-time controllers are limited to buck converter switching frequencies of 300kHz. Therefore, for operation at switching frequencies above 300kHz, dead-time controllers need to be faster and should operate without dithering.

A one-step predictive dead-time control circuit for the synchronous buck converter is proposed in this thesis. It consists of a novel dead-time detection circuit and an analog optimization circuit. The detection circuit utilizes an integrated dead-time detection diode, which can be manufactured on the same die as the synchronous MOSFET in the buck converter. This results in an accurate detection signal indicating body diode conduction of the synchronous MOSFET. The dead-time optimization circuit is an analog circuit, which eliminates the shortcomings of digital control.

The proposed circuit is verified using PSIM simulation software. In comparison to the adaptive dead-time control using a TPS2832 MOSFET gate driver with minimal of 15ns dead-

time, the proposed dead-time control circuit reduces the body diode conduction time of the synchronous MOSFET to 2ns at 10A half load, 12V input, 1.2V output and 500kHz switching frequency. As a result, the efficiency of the buck converter is increased from 89.2% to 90.8%.

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List of Symbols

b	MOSFET body terminal
C	Capacitor of the power stage filter
C_1	Capacitor in the detection circuit
C_2	Capacitor in the PWM signal processing circuit
C_3	Capacitor in the detection signal processing circuit
C_{ctr}	Control capacitor
C_{min}	Minimal capacitance to limit the output voltage ripple
D	Duty cycle
d	MOSFET drain terminal
$D(n)$	Moving average duty cycle
$d(n)$	Current duty cycle
$D[5:1]$	5-digits output of the finite state machine
D_{body}	Body diode of the synchronous MOSFET
D_{det}	Dead-time detection diode
D_{syn}	Synchronous diode
DT	Dead-time
$DT0$	Initial dead-time value
DW	Dead-time width
e	the base of natural logarithm
$E_{ff}(n)$	Buck converter efficiency at current switching cycle
$E_{ff}(n-1)$	Buck converter efficiency at previous switching cycle
f_s	Switching frequency
g	MOSFET gate terminal
g_1	Gate signal for the power MOSFET
g_2	Gate signal for the synchronous MOSFET
I_B	Input bias current of a comparator
i_{C1}	Capacitor C_1 current
i_{C2}	Capacitor C_2 current
i_{C3}	Capacitor C_3 current

I_d	Drain current of MOSFETs
i_{Dbody}	Body diode current of the synchronous MOSFET
i_{Ddet}	Detection diode current
I_{det}	Drain-source current of the detection MOSFET
I_{ds}	Drain-source current of MOSFETs
i_{in}	Input current of the buck converter
I_{in_avr}	Average input current of the buck converter
I_{in_c}	Input current of a comparator
I_L	Inductor current
I_{load}	Load current of the buck converter
I_{Load}	Average load current
I_{Q2}	Drain-source current of the synchronous MOSFET
i_{R2}	Resistor R_2 current
i_{R3}	Resistor R_3 current
i_{R4}	Resistor R_4 current
i_{R5}	Resistor R_5 current
K	Magnification parameter of the voltage amplifier
$K_{rip}\%$	Output voltage peak-to-peak ripple
L	Inductor of the power stage filter
L_{cri}	The critical inductance that ensures continuous current mode
O_{reg}	Flip-flop output
P_{in}	Average input power of the buck converter
p_{in}	Input power of the buck converter
P_{ls}	Power loss at the buck converter
P_{ls1}	Power loss of the buck converter with the proposed dead-time controller
P_{ls2}	Power loss of the buck converter with the benchmark circuit
P_{out}	Average output power of the buck converter
p_{out}	Output power of the buck converter
Q_1	Power MOSFET of the buck converter
Q_2	Synchronous MOSFET of the buck converter
Q_3	MOSFET in the PWM signal processing circuit
Q_4	Charging up MOSFET in the detection signal processing circuit

Q_5	Discharging MOSFET in the detection signal processing circuit
Q_{det}	Dead-time detection MOSFET
Q_g	Gate charge of a MOSFET
R_1	Resistor in the detection circuit
R_2	Charging up resistor in the PWM signal processing circuit
R_3	Discharging resistor in the PWM signal processing circuit
R_4	Charging up resistor in the detection signal processing circuit
R_5	Discharging resistor in the detection signal processing circuit
R_L	Equivalent load resistance
R_{on}	On resistance of MOSFETs
s	MOSFET source terminal
SiO_2	Silicon dioxide
t	Time variable
T	Switching period
t_1	Objective rising time of v_{C2}
t_2	Experimental rising time of v_{C2} at the proposed circuit
t_3	Experimental falling time of v_{C2} at the proposed circuit
t_4	Objective time to charge up C_3 in each switching cycle
t_5	Experimental time starting to charge up C_3 at proposed circuit
t_6	Delay generated by the optimization circuit for the rising edge of the PWM pulse
t_7	Delay caused by the optimization circuit at the trailing edge of the PWM pulse
t_{bc_r}	Body diode conduction time at the rising edge
t_{bc_t}	Body diode conduction time at the trailing edge
t_{con}	Detected body diode conduction time, output of the detection circuit
t_{con_org}	Original body diode conduction time
t_d	Time delay generated by dead-time controllers
$t_d(n)$	Dead-time for the current switching cycle
$t_d(n-1)$	Dead-time of the previous switching cycle
t_{d1}	Time delay at the rising edge of the PWM pulse
t_{d2}	Time delay at the trailing edge of the PWM pulse
t_{do}	Optimal dead-time
t_{off}	Switch off time of a MOSFET

t_{on}	Switch on time of a MOSFET
t_{pd}	Propagation delay of logic gates
t_{Q4_on}	Duration of the MOSFET Q_4 being turned on
t_{rr}	Reverse recovery time of a diode
V_1	Voltage source for the detection circuit
V_2	Voltage source for signal shifting
v_a	Voltage signal at point a in the adjustment circuit
v_b	Voltage signal at point b in the adjustment circuit
v_c	Voltage signal at point c in the adjustment circuit
v_{C1}	Voltage across the capacitor C_1 in the detection circuit
v_{C2}	Voltage across the capacitor C_2 in the PWM signal processing circuit
V_{C2_h}	High voltage value of v_{C2}
V_{C2_l}	Low voltage value of v_{C2}
v_{C3}	Voltage across the capacitor C_3 in the detection signal processing circuit
V_{C3_h}	High voltage value of v_{C3}
V_{C3_l}	Low voltage value of v_{C3}
v_{Ddet}	Anode voltage of the detection diode
v_{det}	Dead-time detection signal voltage
v_{det_r}	Detection signal voltage for the rising edge of the PWM pulse
v_{det_t}	Detection signal voltage for the trailing edge of the PWM pulse
V_{dmax}	Maximal value of the dead-time detection voltage
V_{dmin}	Minimal value of the dead-time detection voltage
V_{ds}	Drain-source voltage of MOSFETs
$V_{F\text{-}body}$	Forward voltage of the synchronous MOSFET body diode
$V_{F\text{-}det}$	Forward voltage of the detection diode
v_{g1}	MOSFET Q_1 gate signal
v_{g2}	MOSFET Q_2 gate signal
V_{gs}	Gate-source voltage of MOSFETs
V_{gs2}	Gate-source voltage of the synchronous MOSFET
V_{high}	Voltage value of logic high
v_{in}	Input voltage of the buck converter
V_{in}	Average input voltage of the buck converter

V_{logic}	Analog voltage level of a logic gate
V_{out}	Average output voltage of the buck converter
v_{out}	Output voltage of the buck converter
V_{out_rms}	Root-mean-square of the buck converter output voltage
v_{pwm}	Output of a PWM controller
v_{pwm_i}	Inverted output of a PWM controller
v_{R2}	Voltage across the resistor R_2
v_{R3}	Voltage across the resistor R_3
v_{R4}	Voltage across the resistor R_4
v_{R5}	Voltage across the resistor R_5
V_{S1}	Voltage source for the control circuit
V_{th}	Threshold voltage of MOSFETs
v_x	Voltage at the junction point of the power MOSFET and the synchronous device
α	Low pass filter factor; between 0 and 1
ΔE_{ff}	Efficiency improvement
$\Delta P\%$	Power loss reduction percentage
ΔP_{ls}	Power loss reduction by the proposed circuit
Δt_d	Dead-time step
$\Delta V_{out\text{-}pp}/V_{out}$	Peak-to-peak output voltage ripple
η	Power efficiency of buck converters
τ_1	Time constant of the detection circuit
τ_2	Time constant of the rising transient at the PWM signal processing circuit
τ_3	Time constant of the falling transient at the PWM signal processing circuit
τ_4	Time constant of the rising transient at the detection signal processing circuit
τ_5	Time constant of the falling transient at the detection signal processing circuit

List of Abbreviations and SI Units

A	Amperes
C	Coulombs
DC	Direct Current
DPWM	Digital Pulse Width Modulation
F	Farads
FSM	Finite State Machine
H	Henries
Hz	Hertz
IC	Integrated Chips
k	Kilo (10^3)
M	Mega (10^6)
m	Milli (10^{-3})
MEPT	Maximum Efficiency Point Tracking
MOSFET	Metal Oxide Silicon Field Effect Transistor
n	Nano (10^{-9})
n-type	Negative-type
PID	Proportion-integral-derivative
p-type	Positive-type
s	Seconds
V	Volts
W	Watts
μ	Micro (10^{-6})
Ω	Ohms

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To my parents

Chapter 1

Introduction

1.1 Introduction of Dead-time in Synchronous Buck Converters

A buck converter is a step down DC to DC conversion circuit. Figure 1.1 is the simplest and most widely used DC-DC converter topology. It is a switching mode power supply, with a frequency generally ranging from 50kHz to 1MHz. It is often used in modern low voltage DC power supplies, such as battery-supplied electronics, point of load converters and microprocessor power supplies.

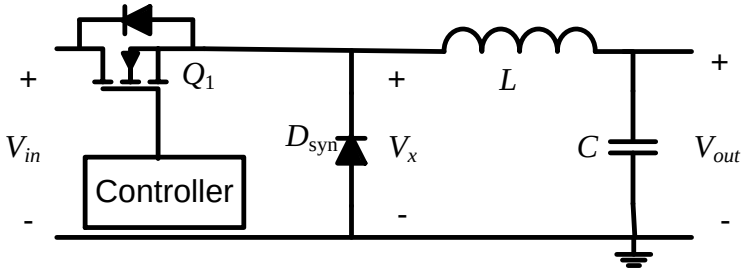

Figure 1.1 The buck converter

A synchronous buck converter uses a power MOSFET to replace the rectifier diode in order to achieve higher efficiency, because for low output voltage applications, a MOSFET exhibits lower conduction loss than a diode. Figure 1.2 illustrates the circuit of a synchronous buck converter, and Figure 1.3 shows its ideal gate-to-source driving waveforms. Q_1 is called the control switch while Q_2 is called the rectifier switch or synchronous rectifier. Ideally, Q_1 and Q_2 are turned on in a complementary fashion such that at $t=DT$, Q_2 is turned on while Q_1 is turned off simultaneously, and vice versa at $t=0$ or T.

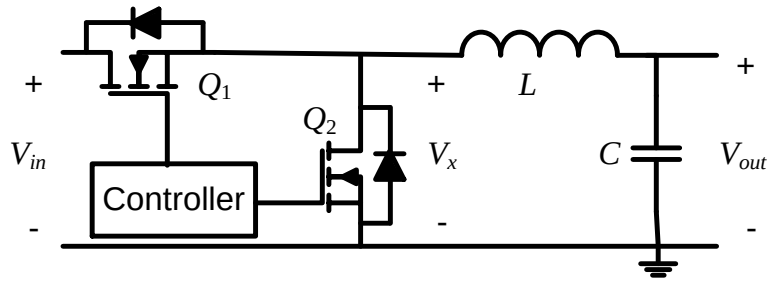

Figure 1.2 The synchronous buck converter

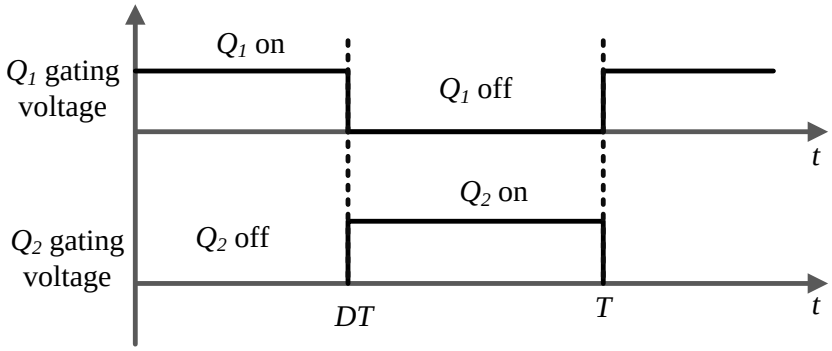

Figure 1.3 Ideal Q_1 and Q_2 gate signal waveforms

Due to the non-zero turn-on and turn-off time of power MOSFETs, a dead-time needs to be inserted into the transition intervals, as shown in Figure 1.4. Without dead-time, it is possible that Q_2 will turn-on when Q_1 is not totally off, resulting in a shoot through current from the source through Q_1 and Q_2 to ground, leading to reliability problems and excessive power loss. Alternately, if the dead-time is longer than required such that Q_2 is not turned-on when Q_1 has been off, the body diode of Q_2 is forced on, providing a continuous path for the inductor current. Generally, a body diode has greater conduction loss than a MOSFET channel. As a result, excessive dead-time results in a lower efficiency for the converter.

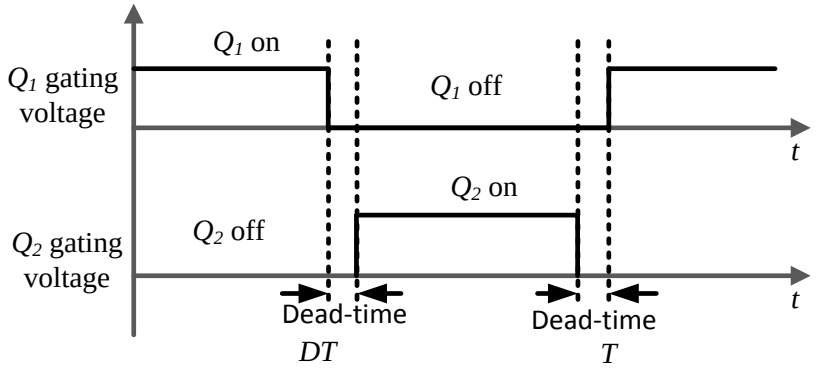

Figure 1.4 Waveforms of Q_1 and Q_2 gate signals with dead-time

1.2 Research Motivation and Objectives

High efficiency is a requirement for the buck converter and all power converters. Their ability to achieve high efficiency (e.g. typically > 85%) is one of the reasons that buck converters are so widely used in power conversion. Therefore, much research has been done to increase efficiency. One method is to reduce the body diode conduction of the synchronous MOSFET in the buck converter.

Buck converters typically switch at frequencies between 200kHz and 500kHz. High switching frequencies result in better performance and design characteristics in many aspects, including a fast transient response, a smaller inductor, and a smaller capacitor. However, frequency dependent losses including switching loss, gate loss and body diode conduction loss increases with frequency. High switching loss and gate loss are not easily addressed; however, fast dead-time control circuits can minimize dead-time related conduction loss in order to achieve high efficiency.

The objective of this thesis is to propose a dead-time control circuit that reduces dead-time to a minimum value in comparison to benchmark circuits used presently in industry. A dead-time control circuit requires dead-time detection and dead-time optimization circuits, which are

discussed in the following subsections.

1.2.1 Dead-time Detection Circuit

The dead-time detection circuit needs to be sensitive. Otherwise it is impossible for the control circuit to achieve a small dead-time if the detector cannot even sense body diode conduction. Moreover, the detection circuit should be able to generate an output signal that precisely tells the body diode conduction time. Without doubt, it is beneficial if the circuit can be made denser.

1.2.2 Dead-time Optimization Circuit

Dead-time optimization circuits can be either analog or digital. However, most dead-time controllers are digital since it is relatively simple to insert dead-time to the PWM pulses. An important objective for the circuit is high speed so that the processing time is much less than the switching period which can be very small for high frequencies. Finally, since the timing of the pulses is critical for proper efficient converter operation, the optimization circuit should synchronize the gate signals for the two MOSFETs.

Chapter 2

Literature Review

2.1 Overview

In this chapter, the MOSFET semiconductor device is briefly introduced, and then a review of dead-time control circuits is presented. The advantages and shortcomings of the existing circuits are compared and summarized, thereby establishing the technical modification for the work presented in the remainder of the thesis.

2.2 Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

Among semiconductor devices, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are the most widely used switching devices in low power and high frequency power conversion applications, due to desirable characteristics including, low on-state voltage drop, low gate drive currents, high current handling capability, and low cost. In this section, the basic structure and models of operation of power MOSFETs is introduced.

2.2.1 Structure of MOSFETs

MOSFETs are semiconductor devices with four terminals including the drain, source, gate, and body. The semiconductor material used for the source and drain terminals in MOSFETs are categorized as n-type or p-type. For n-type MOSFETs, n-type source and drain are added to the body of p-type silicon substrates. A layer of insulative material, silicon dioxide (SiO_2), is then manufactured on top of the substrates. Figure 2.1 illustrates the circuit symbol and device structure of an n-type MOSFET.

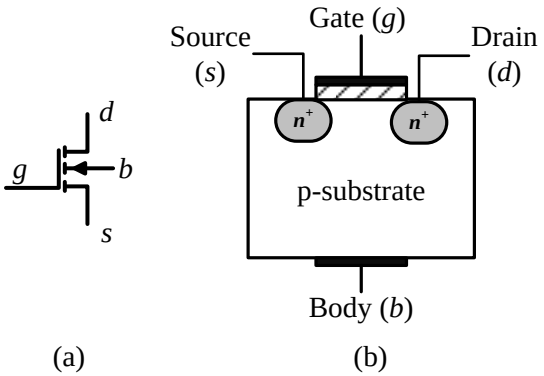

Figure 2.1 n-type MOSFET (a) circuit symbol and (b) device structure

For power MOSFETs, the body terminal is connected to the source, so the device effectively becomes a three-terminal device. Figure 2.2 illustrates the three-pin symbol of an n-type MOSFET.

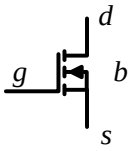

Figure 2.2 Circuit symbol of a three-pin n-type MOSFET

An intrinsic p-n junction exists between the p^+ body region and the implanted n^+ region, as shown in Figure 2.3 (a). This p-n junction is called the body diode in power MOSFETs. Figure 2.3 (b) illustrates the circuit symbol of a power MOSFET with a body diode.

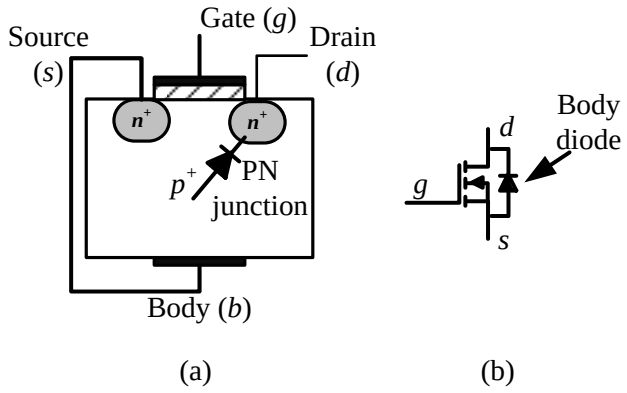

Figure 2.3 (a) The physical origin of the body diode and, (b) circuit symbol of power MOSFET with body diode

2.2.2 MOSFET Mode of Operation

This subsection presents the modes of operation for a MOSFET. When a positive voltage source, V_{gs}, is applied between the gate and source terminals, as shown in Figure 2.4, the gate, the insulative silicon oxide and the base create a capacitive region. The positive voltage draws negative particles to the top of the p-substrate, thus forming a conductive electric channel. Current flows in this channel if another voltage source is present across the drain and source terminals.

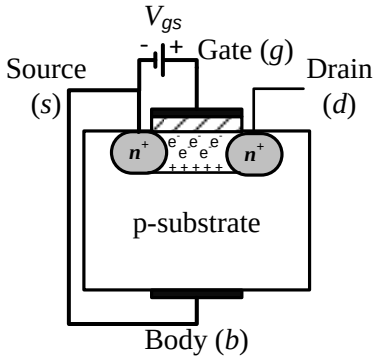

Figure 2.4 The conductive channel between drain and source terminals when a positive V_{gs} is applied between the gate and source terminals

As a first order approximation, MOSFETs have three operation modes depending on the

magnitude of the applied voltages.

1) Cutoff mode

This mode occurs when $V_{gs} < V_{th}$, where V_{th} is the threshold of the device. That is, the gate-source voltage is too small to enable the formation of the conductive channel. This mode is the "off" mode, since the device cannot conduct current.

2) Triode mode

When $V_{gs} > V_{th}$, but $V_{ds} < V_{gs} - V_{th}$, the MOSFET device works like a resistor. The magnitude of the current, I_{ds} is linearly related to V_{ds} for a given value of V_{gs}.

3) Saturation mode

The device is called saturated when $V_{gs} > V_{th}$, and $V_{ds} > V_{gs} - V_{th}$. The value of I_{ds} is controlled by V_{gs} and is independent of V_{ds}.

The resistance between the drain and source terminals in the triode mode is called the on resistance, which is an important parameter in every MOSFET datasheet. The on resistance of a power MOSFET usually lies in the milliohm range, so it is typically ignored, except for use in loss calculations.

Due to high drain current and low drain voltage, power MOSFETs are intended to operate in the triode mode (low resistance) in the on state, and in the cutoff mode (very high resistance) in the off state.

2.3 Dead-time Control Review

Dead-time control techniques can be divided into three types - fixed dead-time control, adaptive dead-time control, and predictive dead-time control [1].

With fixed dead-time, a constant uncontrolled dead-time is added to the gate signal for the

synchronous MOSFET. The fixed dead-time must be long enough to avoid over shoot in any conditions, regardless of changes in temperature, load, and the type of MOSFET device. Therefore, to avoid any chance of shoot through, the dead-time is usually much longer than that needed in most situations, resulting in excessive body diode conduction.

Adaptive dead-time control, however, is able to adjust the dead-time according to the current conditions in the circuit. An example of an adaptive dead-time control circuit is shown in Figure 2.5 [1]. With this technique, there is a feedback loop, which acts to detect body diode conduction. As a result, this method can only decrease body diode conduction rather than eliminate it.

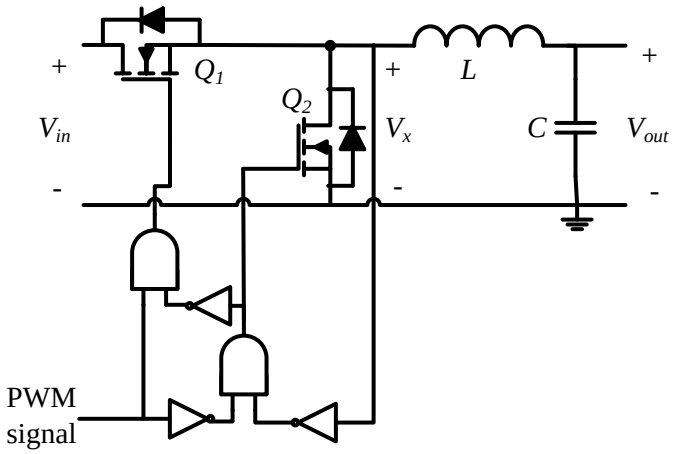

Figure 2.5 An adaptive dead-time control circuit [1]

The third type of dead-time control is predictive dead-time control, which uses information of the previous switching cycle to determine the dead-time needed in the current cycle. Depending on the numbers of cycles needed for the buck converter to reach steady state, predictive dead-time control can be further categorized into unit bit delay adjustment and one step adjustment.

2.4 Review of Dead-time Detection

2.4.1 Maximum Efficiency Point Tracking

A method named "Maximum Efficiency Point Tracking" (MEPT) was proposed in [2]. This method was originally used in solar arrays, and later extended to the field of dead-time control. Figure 2.6 shows the efficiency curve of a buck converter in a certain dead-time range. $t_d(n)$ represents dead-time values at current switching cycle, and $E_{ff}(n)$ is the corresponding efficiency. Similarly, the previous step dead-time is $t_d(n-1)$ and the efficiency $E_{ff}(n-1)$. ΔE_{ff} and Δt_d are given by (2.1) and (2.2).

$$\Delta E_{ff} = E_{ff}(n) - E_{ff}(n-1) \tag{2.1}$$

$$\Delta t_d = t_d(n) - t_d(n-1) \tag{2.2}$$

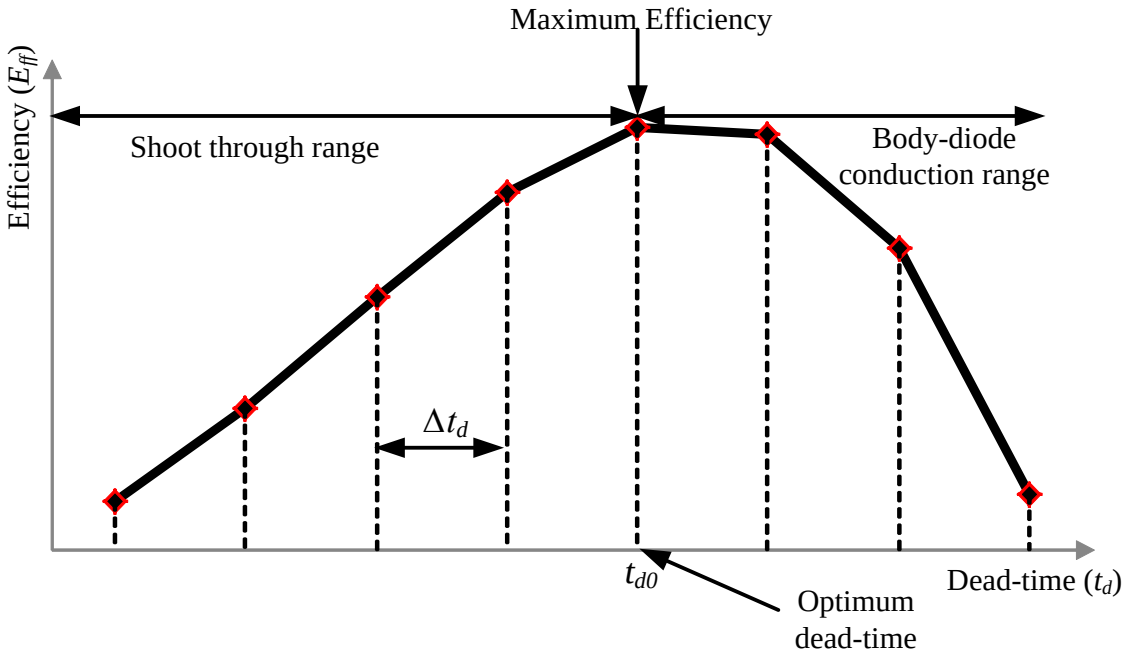

Figure 2.6 A curve of efficiency versus dead-time

If ΔE_{ff} and Δt_d have the same sign, that is both being positive or negative, dead-time for the

coming switching cycle is that of last switching cycle plus one step dead-time value, Δt_d; otherwise, the dead-time is decreased by one step. The dead-time controller starts with a fixed worse-case dead-time, which ensures safety operating at all conditions. The dead-time is then modified step by step until the maximum efficiency is found.

One advantage of this method is that the algorithm is simple. The input current is sensed and used instead of maximum efficiency, since the lowest input current corresponds to the highest efficiency, if the output voltage is regulated. Therefore, an extra sensor is not needed because the input current is usually monitored for safety reasons. Another advantage is that the controller will adapt to the optimum dead-time if the load or input voltage changes. Disadvantages include long transient times and limited accuracy, depending on the step size of the dead-time. Since dead-time is changed step by step rather than continuously, there is a high chance that the actual optimum dead-time exists between two stepped dead-time values.

2.4.2 Sensorless Optimization of Dead-time

Another digital algorithm of dead-time control named sensorless optimization is proposed in [3]. The block diagram of this dead-time controller is provided in Figure 2.7. The PID controller adjusts the duty cycle to regulate the output voltage of the buck converter. In steady state, the optimum dead-time value produces the lowest duty cycle value. The output of the PID compensator is utilized to find the optimum dead-time. The dead-time optimizer starts with a fixed maximum dead-time value, which ensures safe operation of the buck converter under all conditions. Next, the dead-time is decreased step by step until it reaches the dead-time value which yields the lowest duty cycle. To avoid sudden changes, a moving average duty cycle, *D(n)*, is used in the algorithm rather than the current duty cycle, *d(n)*. The moving average duty cycle, given by (2.3), functions as a low pass filter.

$$D(n) = (1-\alpha)D(n-1) + \alpha d(n) \tag{2.3}$$

where α is a factor between 0 and 1and $D(n)$ is equal to $d(n)$ in steady state.

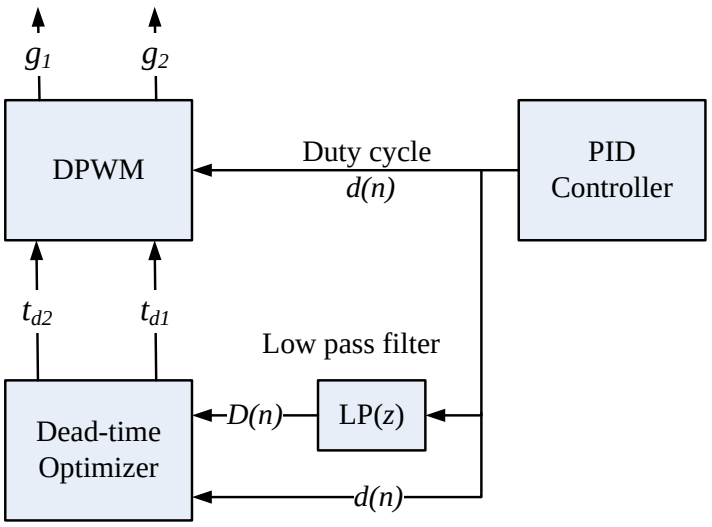

Figure 2.7 Block diagram for sensorless optimization of dead-times

There are several similarities between this sensorless dead-time optimizer and the previous MEPT algorithm. First, no extra sensor is needed to detect dead-time. In both algorithms, detection signals are generated from parameters which already exist in the voltage regulation loop. Second, both dead-time controllers start from a preset maximum value and are decreased step by step until the optimum value is found. For these reasons, the two algorithms are similar such that they share the same advantages and disadvantages.

2.4.3 Logic Gate Used as a Detector

A NOR gate and a comparator are used to detect the body diode conduction of MOSFET Q_2 in [1]. The circuit is provided in Figure 2.8. Waveforms of the NOR gate output, comparator output, Q_2 drain-to-source voltage, V_x, and gate-to-source voltage, V_{gs2}, are provided in Figure 2.9. Only when both V_{gs2} and V_x are low will the NOR gate output be high. Therefore, the presence of a high NOR gate output illustrates body diode conduction and therefore excess dead-

time. The dead-time in the controller is decreased by one step size for the next switching cycle until the high pulse of the NOR gate output is eliminated. When the NOR gate output remains low, a one-step size delay is added to the dead-time for the next switching cycle. As a result, a two-step dead-time size dithering occurs in steady state. The NOR gate is used to detect the body diode conduction before Q_2 turns on; while the comparator is used to detect body diode conduction after Q_2 turns off. This leads to complications in the control circuit and in addition, it takes several switching cycles to eliminate body diode conduction.

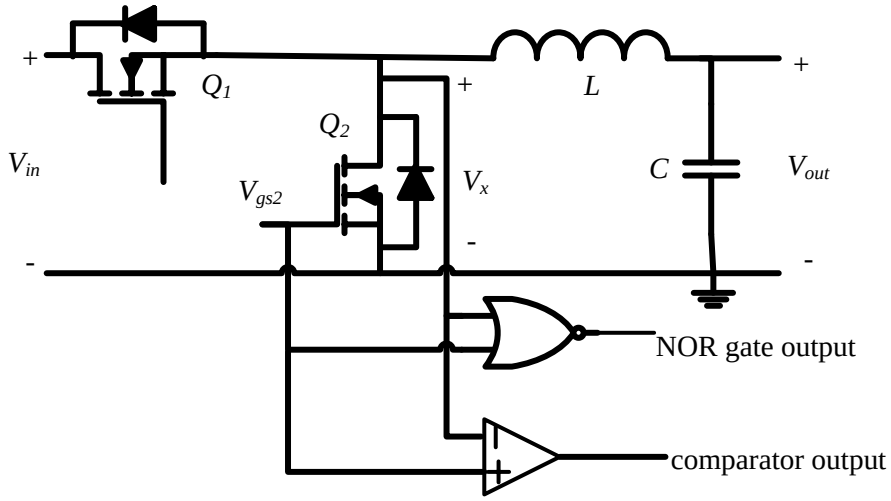

Figure 2.8 A NOR gate is utilized to detect body diode conduction in [1]

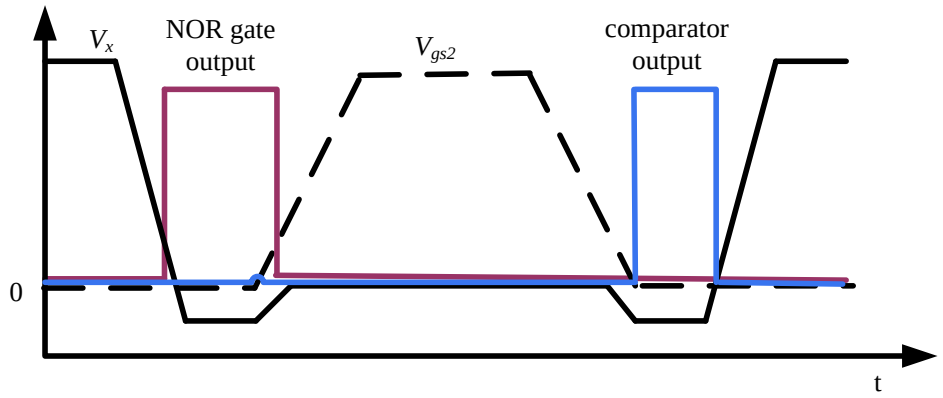

Figure 2.9 Voltage waveforms of the switch node voltage, V_x, Q_2 gate signal, V_{gs2}, and the NOR gate output

2.4.4 One-step Dead-time Correction

To avoid these shortcomings, an improved method, called "one-step digital dead-time correction" was proposed in [4]. A block diagram of this method is provided in Figure 2.10. The comparator in [1] is eliminated and the NOR gate is used to detect body diode conduction during the turn on and turn off transition intervals. This simplifies the circuit and improves its performance, since the NOR gate is faster than the comparator. After dead-time detection is achieved with the NOR gate, a pulse width measurement is implemented to measure the width of the NOR gate output pulse, *DW*. In the next switching cycle, *DW* is subtracted from the dead-time, *DT*. Theoretically, the body diode conduction can be eliminated in the next switching cycle rather than in several switching cycles, so "one-step correction" can be achieved. However, as in [1], a step-size dead-time value, *DT0*, is added when the output of the NOR gate remains low. Therefore, the dithering at the two-step size window remains as in [1].

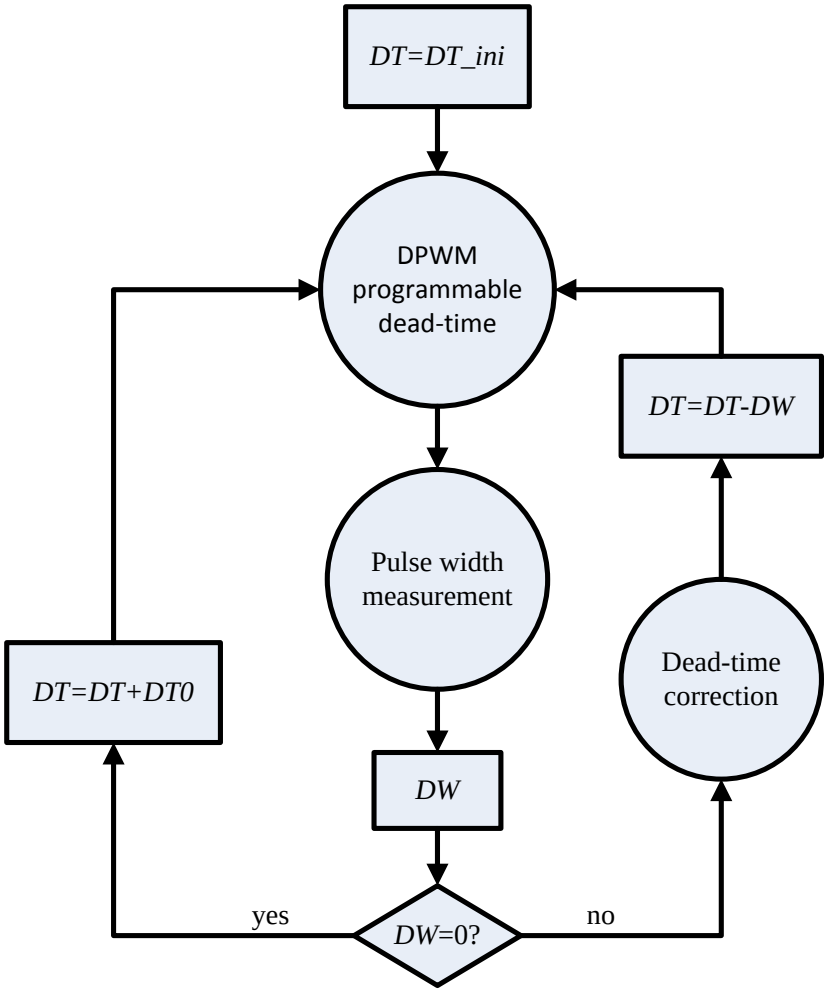

Figure 2.10 Block diagram for the digital one-step dead-time correction

2.4.5 Detecting MOSFET Q_{det}

Dynamic dead-time control is introduced in [5]. Instead of a NOR gate, or a comparator, a detecting MOSFET, Q_{det}, is used. This MOSFET can be fabricated on the same die as the synchronous rectifier MOSFET Q_2, as illustrated in Figure 2.11. The dynamic dead-time control circuit with the buck converter is illustrated in Figure 2.12. When the body diode of Q_2 is on, V_x is slightly negative (e.g. -0.7V). In addition, since Q_{det} is in parallel with Q_2, its body diode is also forced on. Therefore, when the body diode of Q_2 is on, the voltage across C_1 decreases. The time

that C_1 voltage stays low reflects the body diode conduction time of Q_2. The finite state machine (FSM) controls a binary-weighted capacitor, which in turn adjusts the dead-time in the dead-time adjustor (DTA). If the output of the RS flip-flop, O_{reg}, is '1', the dead-time will be reduced in the next switching cycle; while if O_{reg} is '0', the FSM output, *D[5:1]*, is increased, and therefore the next switching cycle dead-time is increased.

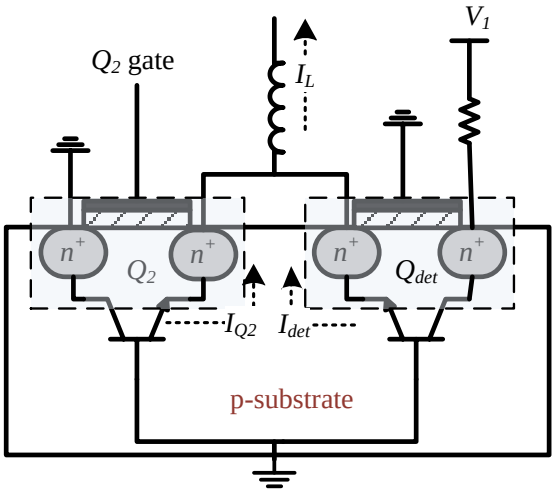

Figure 2.11 The detection MOSFET is implemented on the same die as Q_2 and the body diodes of the two MOSFETs conduct simultaneously

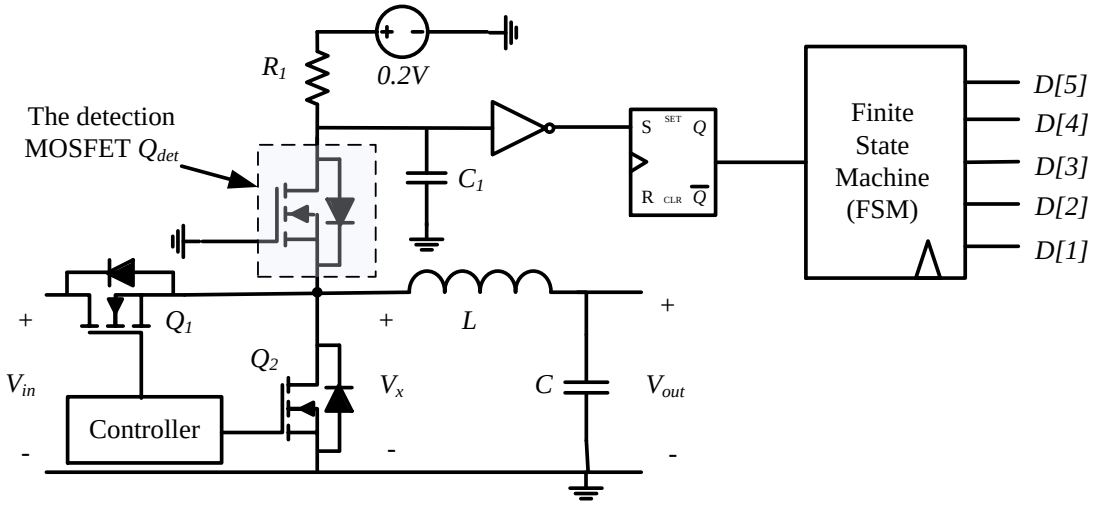

Figure 2.12 The detection MOSFET, Q_{det}, with the dynamic dead-time controller

This dynamic dead-time control is similar to other digital controllers in many aspects except for the body diode conduction detection circuit, which has the built-in detecting MOSFET, unique from other detecting methods. This built-in detector is able to make the integrated control circuit denser than a separate discrete circuit. In addition, it reduces the influence of parasitic electric parameters between the sensor and the Q_2 body diode, eliminating the wire between them. As a result, this sensor can be more accurate than the methods in [1]-[4]. Furthermore, this analog detecting technique is also suitable for an analog controller and thus the disadvantages of digital controllers can be eliminated.

2.4.6 Adaptive Timing Control with Phase Detector

In [9], dead-time control is achieved without the need for a sophisticated digital signal processor. The control circuit presented in [9] is provided in Figure 2.13. The two comparators and the phase detector generate pulses at the "UP" output to increase the next switching cycle dead-time, or pulses at the "DN" output to reduce the dead-time. This control loop only optimizes the dead-time when the synchronous MOSFET Q_2 is turned on. A symmetric dead-time control loop is required for the buck converter when Q_1 is turned on and Q_2 is turned off, because the control loop in Figure 2.13 only optimizes the dead-time interval before Q_2 turns on.

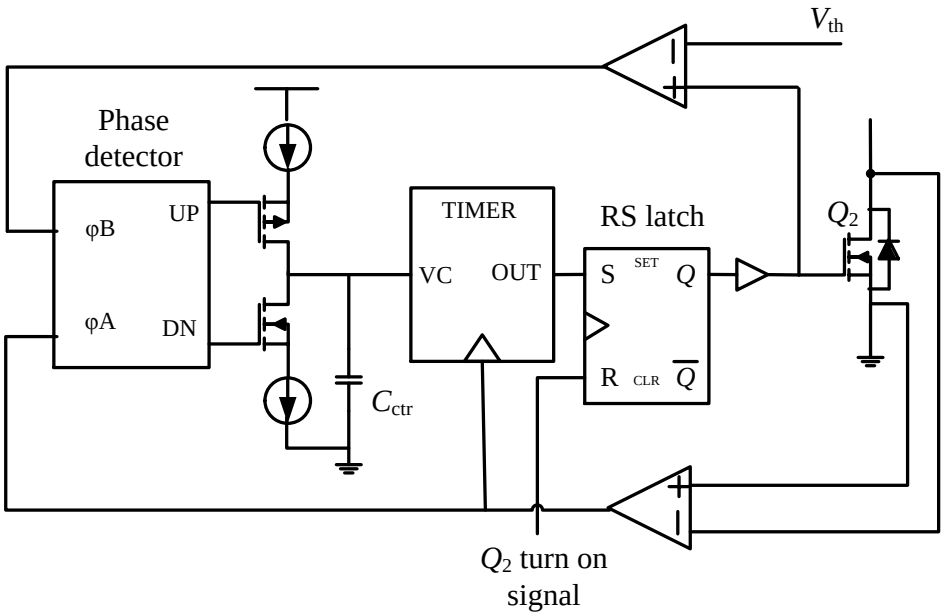

Figure 2.13 A dead-time control loop which does not require a digital processor

This dead-time control circuit overcomes those shortcomings brought in by digital processors, since the dead-time is adjusted continuously rather than step by step. Moreover, the two-step size window dithering in steady state in digital controllers is also eliminated.

2.5 Summary

Body diode conduction detection and dead-time optimization circuits have been reviewed. The work is summarized as follows. Body diode detection methods differ in three ways. Some algorithms use parameters already monitored by the buck converter output voltage controller, such as input current or output voltage [2], [3]. Others use discrete components, like a NOR gate or a comparator, to detect body diode conduction directly [1], [4]. Finally a built-in detecting MOSFET, which is implemented on the same die of the synchronous MOSFET Q_2, is recently proposed to detect dead-time [5].

Unit bit dead-time optimization algorithms have been presented in [1]-[3], and [5]. These

methods work quite similarly despite the different dead-time detection algorithms used. However, if the dead-time for the last switching cycle is too long, it is reduced by one unit bit for the following cycle. A preset maximum dead-time value is stored in the controller and the iterative process stops when the optimum value is found. The number of switching cycles needed to reach steady state, and the accuracy of the optimum dead-time, depend on the size of the unit bit.

In contrast with unit bit dead-time adjustment, the one step adjustment algorithm attempts to reach steady state in one switching cycle [4]. The duration of body diode conduction of the last switching cycle is measured first and then the dead-time for the next switching cycle is set as that of last switching cycle minus body diode conduction time. This algorithm results in a short transient time.

In the chapters that follow, a novel analog body diode detection circuit is proposed in Chapter 3, followed by a novel analog dead-time optimization circuit in Chapter 4. The proposed circuits are combined and PSIM simulation results are used to verify and benchmark the contributions in Chapter 5. The conclusions are presented in Chapter 6.

Chapter 3

Proposed Body Diode Detection Circuit

3.1 Overview

A sensitive detection circuit is critical for dead-time control circuits. In Chapter 2, it was noted that a comparator, or a NOR gate, is a relatively simple way to detect body diode conduction among all the other discussed methods. However, a built-in detector can achieve better performance than discrete devices, because for today's devices that operate at high frequencies, a properly integrated detector can minimize parasitic elements. Therefore, in this chapter, an integrated dead-time detection diode is proposed and the detection circuit operation discussed.

This chapter is organized in the following manner. The dead-time detection circuit is introduced in Section 3.2, followed by a description of an adjustment circuit. The adjustment circuit used to convert the detected non-regular waveform to a pulse waveform is introduced in Section 3.3. In Section 3.4, the detection diode implementation is explained. A design procedure with circuit parameters used is then presented in Section 3.5. Finally, a design example and simulation results are presented in Section 3.6.

3.2 Dead-time Detection Circuit

The proposed dead-time detection circuit for the synchronous buck converter is provided in Figure 3.1. A detection diode, D_{det}, and an auxiliary circuit, consisting of a resistor, R_1, comparator, C_1, and a low DC voltage source, V_1 (e.g. 0.1V), are used to detect the conduction of the Q_2 body diode.

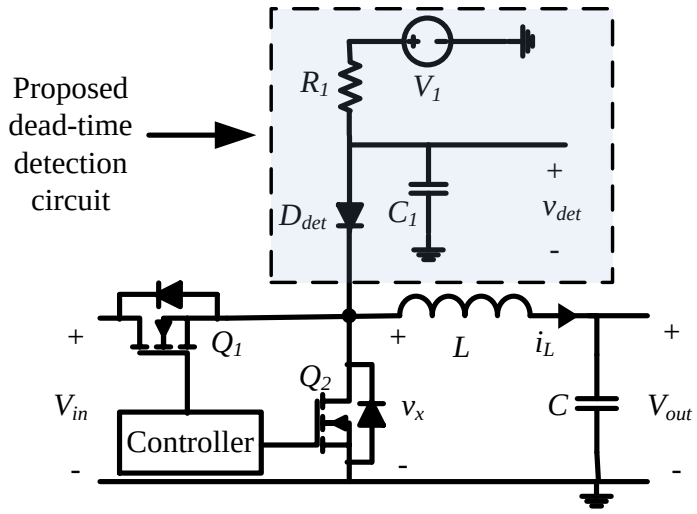

Figure 3.1 Proposed dead-time detection circuit for the synchronous buck converter

In order to illustrate the circuit operation, the output voltage of the capacitor C_1 is analyzed under three different operating conditions of the buck converter:

1) The power MOSFET Q_1 is on while the synchronous MOSFET Q_2 is off.

Switch node voltage v_x in Figure 3.1 is equal to the input voltage V_{in}, which is 12V in the design example of this thesis. V_1 is a small value voltage source, having a value under 0.2V. As a result, a reverse voltage is formed over the diode D_{det} and D_{det} is therefore biased off. The output voltage signal v_{det} is the voltage across capacitor C_1 and is equal to V_1 during this time.

2) The power MOSFET Q_1 is off while the synchronous MOSFET Q_2 is on.

The inductor current flows through MOSFET Q_2 during this time, so voltage v_x is negative and the absolute value of v_x is the product of the current through Q_2 and the on-state resistance of Q_2. Usually, the on-state resistance of a power MOSFET is quite small, ranging from several milliohms to several hundred milliohms depending on the type of the MOSFET. As a result, v_x is usually greater than -0.5V during this time. For the components and circuit operating conditions in this thesis, v_x is approximately -0.1V when Q_2 is on. Thus, diode D_{det} is biased off and the v_{det} is

equal to V_1.

3) The power MOSFET Q_1 is off and the synchronous MOSFET Q_2 is also off.

A prerequisite to use this dead-time detector is that the buck converter is operating in continuous mode (i.e. $i_L > 0$). Since neither switch is on, the body diode of MOSFET Q_2 is forced on to provide a path for the inductor current. As a result v_x drops to a negative value, which is the voltage drop over the p-n junction of Q_2, and is approximately equal to -0.7V for silicon MOSFETs. Since the voltage source, V_1, is positive, a voltage drop, which exceeds 0.7V, is applied to D_{det}, and thus, it is biased on. Therefore, capacitor C_1 is discharged and the output voltage, v_{det}, drops.

A summary of the states of D_{det} during the three operation states of the buck converter is provided in Table 3.1. Figure 3.2 provides the waveforms of the voltage signal v_{det}, along with the gate signals for MOSFETs Q_1 and Q_2. The time interval of signal v_{det} being low represents the period when the body diode of the synchronous MOSFET Q_2 is conducting. In other words, it is this period of time that is desired to be eliminated in order to increase the efficiency. Although v_{det} contains the information of the unwanted dead-time, its waveform is not ideal as a detection signal for the controller. A pulse signal would be preferred, and for this reason, a second circuit is added to adjust the direct detection signal. This adjustment circuit is described in the following subsection.

Table 3.1 Operation condition summary for v_x and D_{det} state

	v_x	Detection diode, D_{det}
Q_1 on, Q_2 off	V_{in} (12V)	Off
Q_1 off, Q_2 on	$-i_L R_{on}$ ($\geq$ -0.1V)	Off
Q_1 off, Q_2 off	-0.7V	On

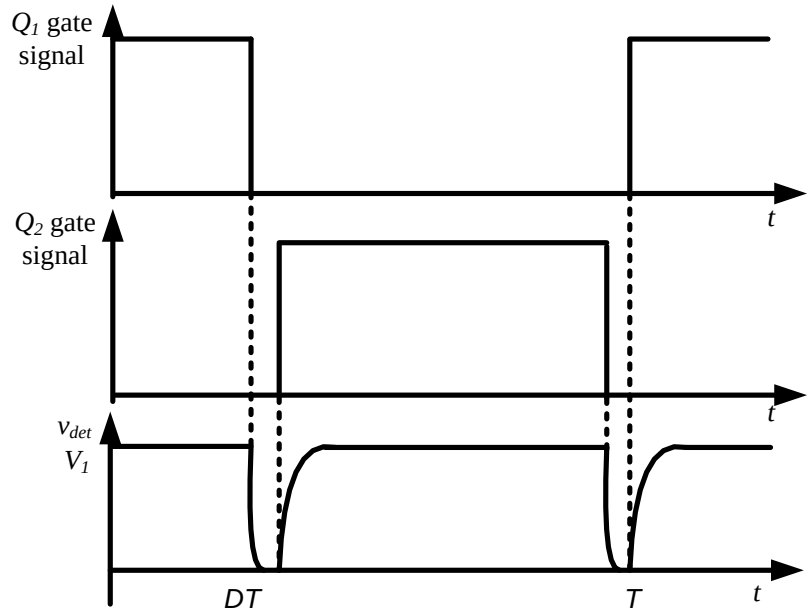

Figure 3.2 The detection signal from the proposed dead-time detection circuit

3.3 Detection Signal Adjustment Circuit

The proposed signal adjustment circuit is provided in Figure 3.3. The purpose of this adjustment circuit is to convert the dead-time detection signal, v_{det}, into a pulse waveform so that it will be easier for the controller input. Figure 3.4 shows voltage variation at several points of the circuit, including those at points a, b, and c as well as the input and output ports.

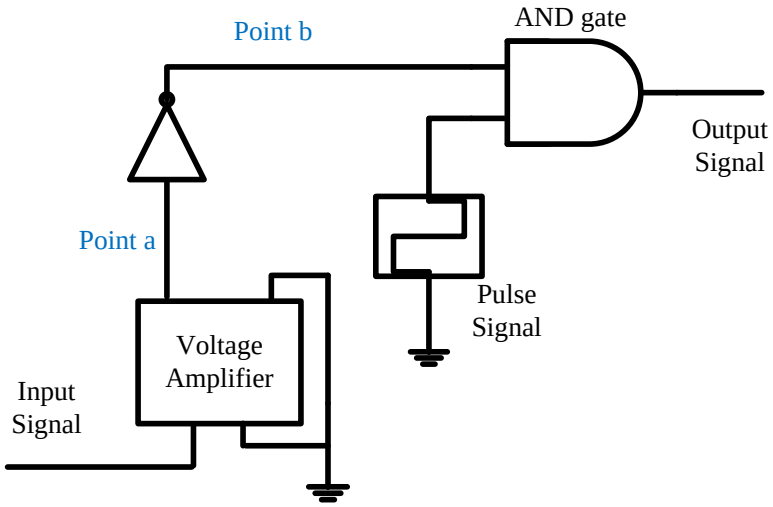

Figure 3.3 The adjustment circuit used to modify the detection signal

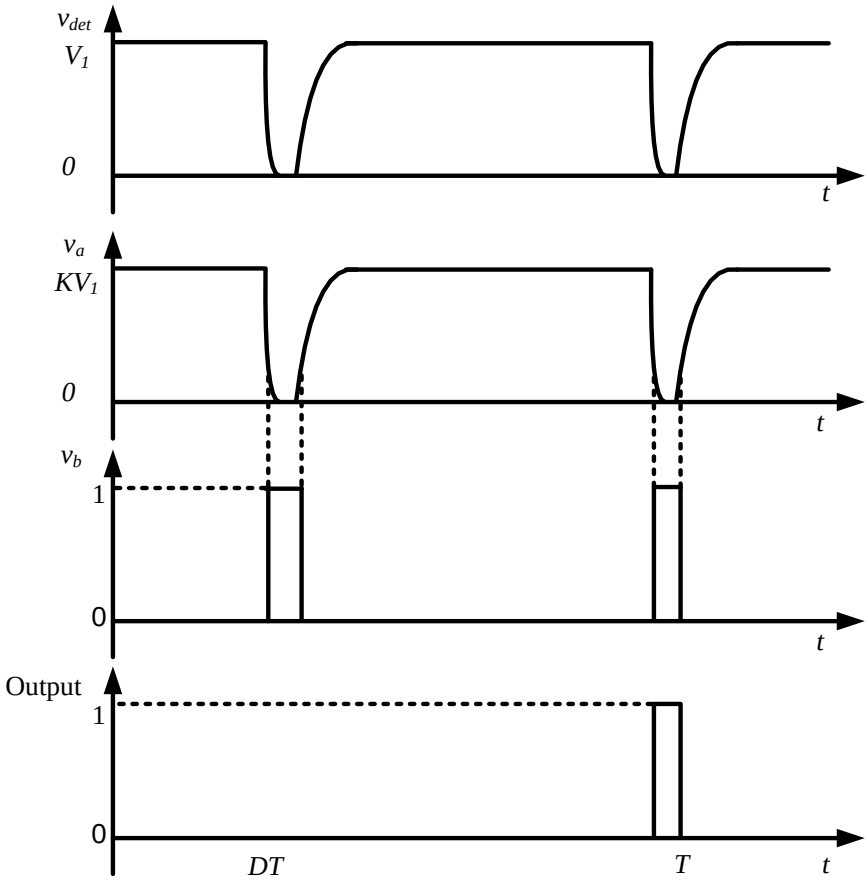

Figure 3.4 Voltage variations at point a, b, and c as well as input and output ports in the detection signal adjustment circuit

The adjustment circuit first magnifies the input signal v_{det} by K times through a voltage amplifier, generating signal v_a. K is an adjustable parameter of the voltage amplifier and is chosen to be a positive integer for this design. Then a logic inverter changes v_a to be pulse signal v_b.

Both the power MOSFET Q_1 and the synchronous MOSFET Q_2 are switched on and off once in every switching cycle. Therefore, each has two on-off transitions during one switching cycle, one while switching on and the other while switching off. Thus, there are two dead-time pulses in a switching cycle, as given by v_b in Figure 3.4. However, these two pulses are usually not of the same width because Q_1 and Q_2 typically have different characteristics and therefore

have different switching characteristics. Moreover, the inductor current also varies at the two switching edges. In steady state the inductor current reaches its maximum value when the MOSFET Q_1 turns off and minimum value when Q_1 turns on. Therefore, the two dead-time intervals should be optimized independently. Accordingly, a 50%-duty-cycle selecting pulse at the switching frequency is applied to one input of the AND gate in Figure 3.3, while v_b is applied to the other. Thus, if the selecting pulse does not have any phase delay, the dead-time signal at the switching on edge is output to the optimization circuit; otherwise, if the selecting pulse has a phase delay of 180 degrees, the dead-time signal at the switching off edge is output. For the design example in this chapter, the latter signal is chosen, as shown in Figure 3.4.

3.4 Implementation of the Detection Diode

The trend in modern power integrated circuit manufacturing is to build two, or more devices on the same die in order to reduce parasitic elements. In this section, the detection diode is proposed to be manufactured on the same die as the synchronous MOSFET Q_2.

The structure of the MOSFET has been reviewed in Chapter 2. The proposed implementation for the detection diode D_{det} is illustrated in Figure 3.5(a). The detection diode can be located immediately to the right of the MOSFET Q_2 with an isolation barrier in the *p*-substrate. The cathode of D_{det} is connected to the drain of Q_2, which is consistent with the circuit arrangement shown in Figure 3.5(b).

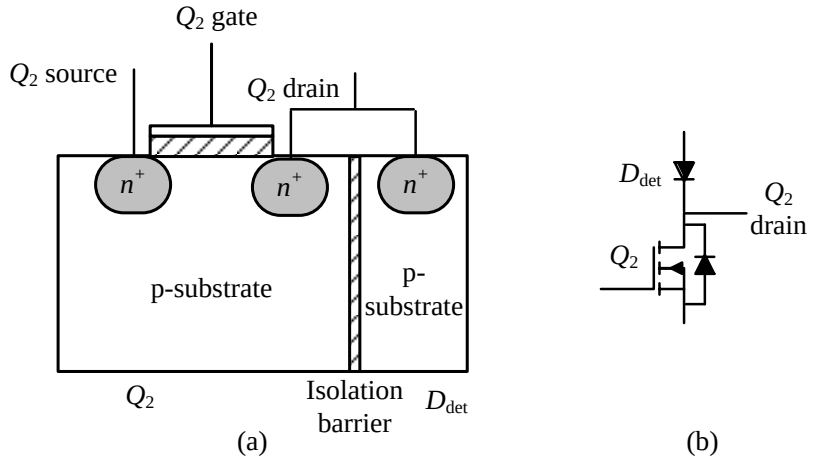

Figure 3.5 (a) The detection diode, D_{det}, is proposed to be manufactured beside the synchronous MOSFET, Q_2, on the same die and (b) the circuit symbol for this device

There are three advantages of the proposed implementation. First, it is denser than two discrete semiconductors, D_{det} and Q_2, so, the dead-time controller can be made smaller. Second, this implementation gives a shorter connection between the Q_2 drain and the D_{det} cathode than that of two discrete devices. This results in less parasitic inductance and capacitance, which enables the controller to be utilized in higher frequency applications. Third, since D_{det} and Q_2 are using the same semiconductor material, the body diode of Q_2 and the detection diode D_{det} have the same forward voltage drop, enabling the detection circuit to be more sensitive and accurate.

3.5 Detection Circuit Design Procedure

Relationships between the circuit parameters of the buck converter are discussed in this section and equations are given in order to illustrate how one parameter influences another. Understanding these relationships enables a designer to choose the right devices for the circuit design and to optimize the expected results. Usually, parameters are chosen sequentially, starting from the initial given ones. Here, the application of the buck converter and design objectives are given. The design procedure for a buck converter is first introduced, followed by the design of the

proposed dead-time detection circuit.

3.5.1 Buck Converter Design

Given the input voltage, V_{in}, output voltage, V_{out}, switching frequency, f_s, load current, I_{load}, and peak-to-peak output voltage ripple assuming 100% efficiency, the duty cycle, D, of the power MOSFET is given by (3.1), and the switching period T, is given by the inverse of frequency f_s, as in (3.2).

$$D = \frac{V_{out}}{V_{in}} \tag{3.1}$$

$$T = \frac{1}{f_s} \tag{3.2}$$

In a design, the specifications for the two MOSFETs in the buck converter need to be decided using the above parameters. The switching speed for both MOSFETs should be sufficient such that the turn-on and turn-off transient times are much smaller than T. In addition, the drain-source voltage rating of both power MOSFETs must be larger than V_{in}, and the drain current rating must be larger than I_{load}. The larger the ratings chosen, the more robust the design will be. However, high ratings require MOSFETs that are large and therefore more expensive. Typically, the V_{ds} voltage rating is chosen to be about twice as large as V_{in}, leaving some safety margin in the design. Another factor that needs to be considered is the overall efficiency of the buck converter. For the power MOSFET Q_1, the switching loss can be larger than the conduction loss, thus MOSFETs with faster switching speeds, and therefore smaller die size, are preferred. However, the synchronous rectifier MOSFET Q_2 does not have switching loss, but it does handle high currents, so minimizing conduction loss is most important and thus a large die size is preferred.

After selecting the MOSFET switches, the inductor value must be determined. The critical inductance value for continuous current mode is given by (3.3), where R_l in the equation

represents the resistance of a resistive equivalent load, given by (3.4). In order to produce a smooth output current, the buck inductor is usually chosen to be twice as large as L_{cri}, or even larger if the volume and the cost of the inductor are tolerable.

$$L_{cri} = \frac{1-D}{2} T_s R_l \tag{3.3}$$

$$R_l = \frac{V_{out}}{I_{load}} \tag{3.4}$$

The last component to be chosen for the power stage circuit is the capacitor. The minimal capacitance value, C_{min}, is given by (3.5), where L is the chosen inductance value and K_{rip}% is the allowed maximum output voltage ripple. A capacitance of 1.5 to 2 times C_{min} is typically selected.

$$C_{min} = \frac{1-D}{8L{f_s}^2(K_{rip}\%)} \tag{3.5}$$

3.5.2 Dead-time Detection Circuit Design

The detection diode D_{det} is proposed to be fabricated together with the synchronous MOSFET Q_2, so instead of finding an appropriate pre-made diode product, the manufacturing requirements need to be defined. The forward voltage drop of the detection diode, $V_{F\text{-}det}$, is a critical parameter since its value should be greater than $V_1+i_LR_{on}$ to prevent undesired forward biasing of D_{det} during the synchronous MOSFET on time. However, $V_{F\text{-}det}$ should be less than $V_1+V_{F\text{-}body}$, where $V_{F\text{-}body}$ is the forward voltage of the synchronous MOSFET's body diode. Otherwise the detection diode will not turn on as desired when the synchronous MOSFET body diode is on. Therefore, the forward voltage of the detection diode, $V_{F\text{-}det}$, should meet the conditions described in (3.6).

$$V_1 + i_L R_{on} < V_{F-det} < V_1 + V_{F-body} \tag{3.6}$$

Voltage source, V_1, is used to provide a reference voltage for the detection signal. Since (3.6) should be met and the forward voltage of a silicon diode is typically 0.7V, V_1 should be less than 0.7V. Therefore, a typical value for V_1 is 0.1V.

To choose R_1 and C_1, we need to analyze the variables in the circuit during the time when capacitor C_1 is being charged and discharged. Both the rising and falling transition times are much less than the dead-time, therefore the inductor current, i_L, can be assumed to be constant, as given by (3.7), where i_{Ddet} is the current through the detection diode D_{det}, and i_{Dbody} is that of the Q_2 body diode. Expressions for the circuit current and voltage during the transition can be derived from (3.8) and (3.9), where $v_{Ddet}(i_{Ddet})$ is the detection diode forward voltage given from the diode characteristic curve when detection diode current is at i_{Ddet}, and $v_{Dbody}(i_{Dbody})$ is the body diode forward voltage at i_{Dbody}. v_{C1} is the voltage across capacitor C_1, which is also the output signal of the detection circuit. Therefore, $v_{det} = v_{C1}$.

$$i_{Ddet} + i_{Dbody} = i_L = constant \tag{3.7}$$

$$\left(i_{Ddet} - C_1 \frac{dv_{C1}}{dt}\right) R_1 = V_1 - v_{C1} \tag{3.8}$$

$$v_{Ddet}(i_{Ddet}) + v_{C1} = v_{Dbody}(i_{Dbody}) \tag{3.9}$$

It is not necessary to solve (3.8) and (3.9), since we are most interested in the impact of R_1 and C_1 on the detection voltage, v_{det}, as it drops. It is noted that the smaller C_1 and R_1 are, the faster the transition is.

During the rising transition of the detection voltage, v_{det}, the diode D_{det} turns off. Voltage source V_1, resistor R_1, and capacitor C_1, form a typical first-order RC circuit. The circuit variables are given by (3.10) and (3.11), where i_{C1} is the current flowing through C_1.

$$i_{C1} = C_1 \frac{dv_{C1}}{dt} \tag{3.10}$$

$$i_{C1} R_1 + v_{C1} = V_1 \tag{3.11}$$

Substituting (3.10) into (3.11), results in a first-order ordinary differential equation, as given by (3.12). The solution to (3.12) is given by (3.13), where the time constant τ_1 is expressed in (3.14). Variable $v_{C1}(t)$ is the voltage across capacitor C_1 at time t. So, $v_{C1}(\infty)$ is the capacitor voltage value at infinite time, in other words, the steady state value, and $v_{C1}(0_+)$ is that at time zero, or the initial state value.

$$R_1 C_1 \frac{dv_{C1}}{dt} + v_{C1} = V_1 \tag{3.12}$$

$$v_{C1}(t) = v_{C1}(\infty) + [v_{C1}(0_+) - v_{C1}(\infty)]e^{-t/\tau_1} \tag{3.13}$$

$$\tau_1 = R_1 C_1 \tag{3.14}$$

The time constant is defined as the time needed for variable $v_{C1}(t)$ to reach 63% of the steady state value, $v_{C1}(\infty)$. It is often used to represent, or to estimate the transient speed. Therefore, the smaller C_1 and R_1 are, the smaller τ_1 is, and the faster the rising transition will be. Conversely, when the detection diode is on, the voltage across R_1 is approximately V_1, so R_1 must be large enough so as not to dissipate too much power.

For the detection signal adjustment circuit, the magnification parameter, K, of the voltage amplifier needs to be decided. K is given by (3.15), where V_{logic} is the threshold voltage of logic high.

$$K > \frac{V_{logic}}{V_1} \tag{3.15}$$

Parameters K and V_1 are relatively less critical, compared to other parameters discussed above, such as the time constant τ_1, the power stage inductor L, and capacitor C. K can be any

value that meets (3.15), and theoretically, V_1 can be any value that turns on the detection diode only during the body diode conduction time.

3.6 Design Example and Simulation Results

3.6.1 Design Example

The proposed dead-time controller is designed for computer regulators, which convert a 12V input voltage to a 1.2V output at a switching frequency of 500kHz and a load current of up to 25A. These parameters and a typical output voltage ripple specification of 1% are summarized in Table 3.2. The parameters provided are used in the design of the buck converter and its dead-time control circuit.

Table 3.2 Buck converter design parameters

Parameter	Value
Switching Frequency, f_s	500kHz
Input Voltage, V_{in}	12V
Output Voltage, V_{out}	1.2V
Load Current, I_{load}	15A
Output Voltage Peak-to-peak Ripple, K_{rip}%	1%

Using the design parameters in Table 3.2, the resultant circuit parameters from the design are provided in Table 3.3.

Table 3.3 Buck converter resultant parameters

Parameters	Value
Duty Cycle, D	10%
Switching Period, T	2us
Load Resistance, Rl	80mΩ
Critical Inductance, Lcri	72nH
Minimal Capacitance, Cmin	300uF

Using the parameters in Table 3.2 and Table 3.3, the power stage devices for the buck converter can be chosen, as shown in Table 3.4. Key parameters from the datasheets of these devices are also given. A Si7866DP MOSFET is selected for Q_1 [14] and an IRF6691 is selected for Q_2 [15].

Table 3.4 The selected MOSFETs, inductor and capacitor for the objective buck converter

MOSFETs	**Power MOSFET Q_1 Si7866DP**	**Synchronous MOSFET Q_2 IRF6691**
Drain-source Voltage, V_{ds}	20V	20V
Drain Current, I_d	18A	26A
Switch On Time, t_{on}	60ns	95ns
Switch Off Time, t_{off}	55ns	10ns
On Resistance, R_{on}	2.6mΩ	1.8mΩ
Passive Component Value	**Value**	
Inductor, L	150nH	
Capacitor, C	560uF	

The proposed detection circuit parameters are provided in Table 3.5. A 1N4148 detection diode was selected. Its parameters are also provided in Table 3.5 [16].

Table 3.5 Detection circuit parameters

Parameters	**Value**
Voltage Source, V_1	100 mV
Resistor, R_1	200 Ω
Capacitor, C_1	90 pF
Magnification Times, K	25
Voltage Source, V_2	2.5 V
Detection Diode	**1N4148**
Reverse Recovery Time, t_{rr}	4 ns
Forward Voltage, $V_{F\text{-}det}$	0.62 V-0.72 V

3.6.2 Simulation Results Using PSIM9

PSIM9 was used to simulate the proposed detection circuit in a synchronous buck converter. The circuit used in the simulation is provided in Figure 3.6.

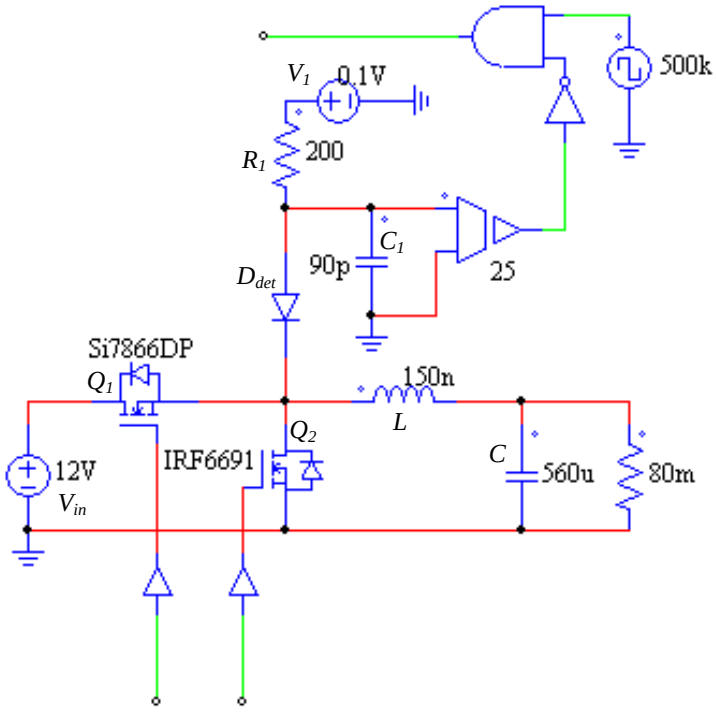

Figure 3.6 Simulation circuit of the buck converter with the proposed dead-time detection circuit

Simulation waveforms of v_x, v_{det}, and the detection signal at the rising edge v_{det_r} are provided in Figure 3.7. It is noted that body diode conduction occurs when v_x goes negative, which occurs twice in a switching period. When v_x goes negative, the v_{det} voltage drops, as expected and the rising edge detection logic signal goes high. Therefore, the proposed circuit functions as expected.

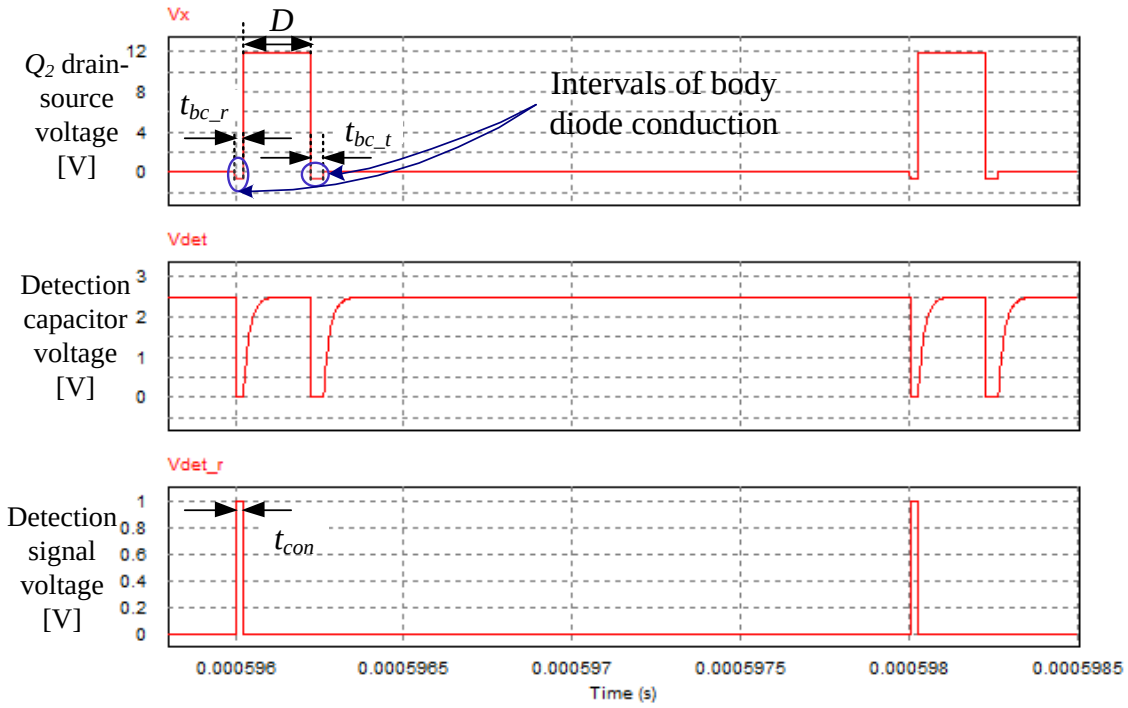

Figure 3.7 Simulated of the synchronous MOSFET voltage, v_x, detection voltage, v_{det}, and rising edge detection flag, v_{det_r}.

3.7 Summary

In this chapter, a novel body diode conduction detection circuit has been proposed for the synchronous buck converter. In addition to the circuit, a recommended silicon implementation, design procedure, design example and simulation results have been presented.

In order to minimize body diode conduction, a dead-time optimization circuit is required after the detection circuit. Therefore, a novel dead-time optimization circuit is proposed in Chapter 4.

Chapter 4

Proposed Dead-time Optimization Circuit

4.1 Overview

Using the body diode conduction detection signal of the synchronous MOSFET body diode, there are several methods which can be used to minimize dead-time, depending on the type of the dead-time detector employed for the buck converter. Existing analog and digital methods have been summarized in Chapter 2. In this chapter, a novel analog dead-time optimization circuit is proposed.

This chapter is organized in the following manner. The circuit operation is presented in Section 4.2. A design procedure is presented in Section 4.3. A design example and simulation results are presented in Section 4.4. Conclusions are presented in Section **Error! Reference source not found.**.

4.2 Dead-time Optimization Circuit

The proposed optimization circuit can be divided into two circuits, one for the PWM signal processing, and the other for the detection signal processing. A block diagram of the proposed dead-time control circuit is shown in Figure 4.1. The PWM signal processing and detection signal processing circuits are introduced in subsections 4.2.1 and 4.2.2, respectively. An explanation of how the combined circuit optimizes dead-time in subsection 4.2.3.

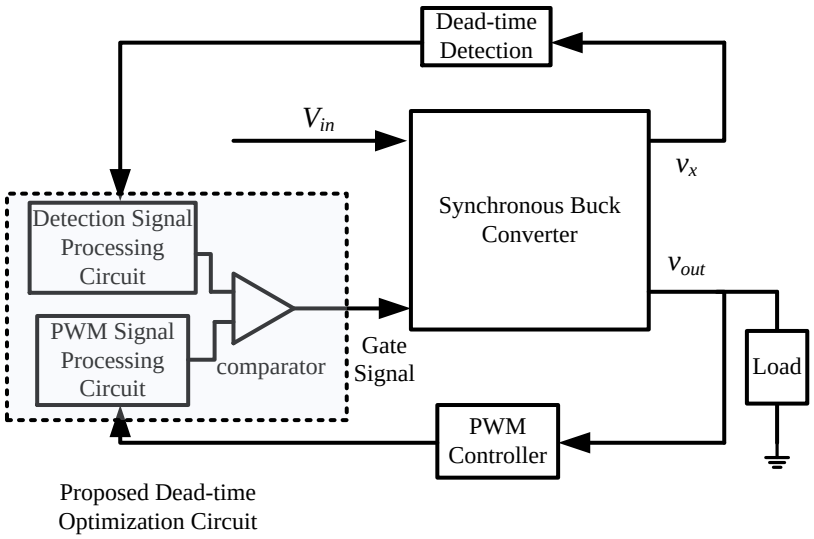

Figure 4.1 Block diagram of the proposed dead-time control circuit

4.2.1 The PWM Signal Processing Circuit

The purpose of the PWM signal processing circuit is to convert the perpendicular rising edge of the PWM signal to an inclining edge, as illustrated in Figure 4.2. The reason for this conversion will be explained later. The parameter t_1 in Figure 4.2 is determined by the processing circuit.

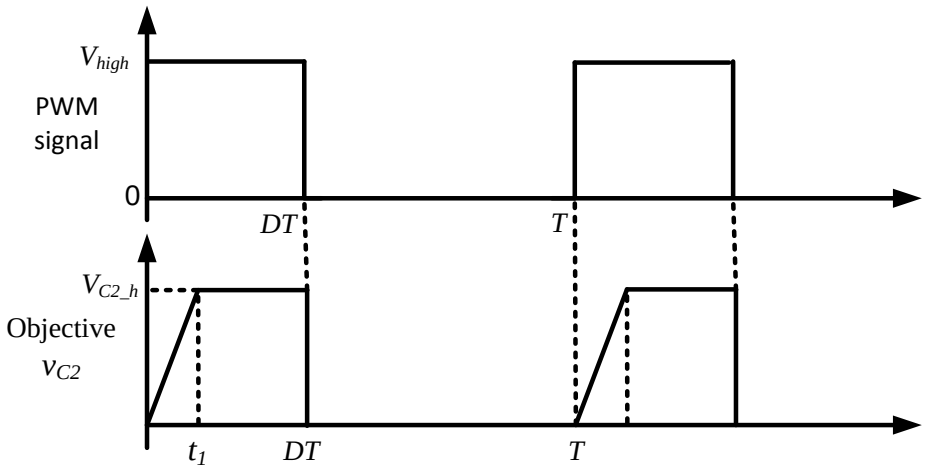

Figure 4.2 The objective output waveform from the PWM signal processing circuit with a PWM input signal

The simplest circuit that can achieve the ramped slope is a voltage driven resistor-capacitor (RC) circuit where the ramp amplitude is less than a single time constant. The time constant of an RC circuit determines the slope of the ramp, or how fast the capacitor voltage changes. Therefore, the above mentioned t_1 in Figure 4.2 can be related to the time constant of an RC circuit.

The proposed PWM signal processing circuit is illustrated in Figure 4.3. Waveforms for the circuit are illustrated in Figure 4.4. The input of this circuit is the PWM signal for the power MOSFET, or the inverted PWM signal for the synchronous MOSFET. The output signal of the circuit is the voltage across capacitor C_2, which is v_{C2}. V_{S1} is the voltage source for the control circuit.

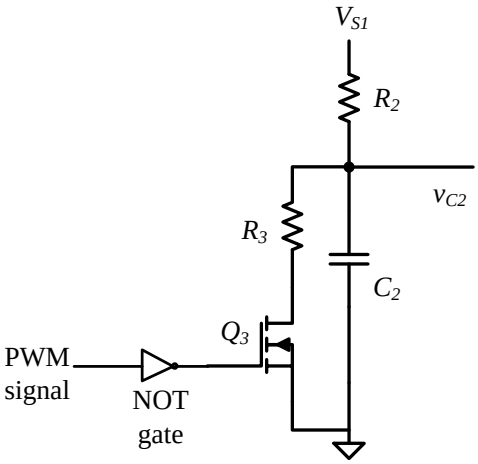

Figure 4.3 The proposed PWM signal processing circuit

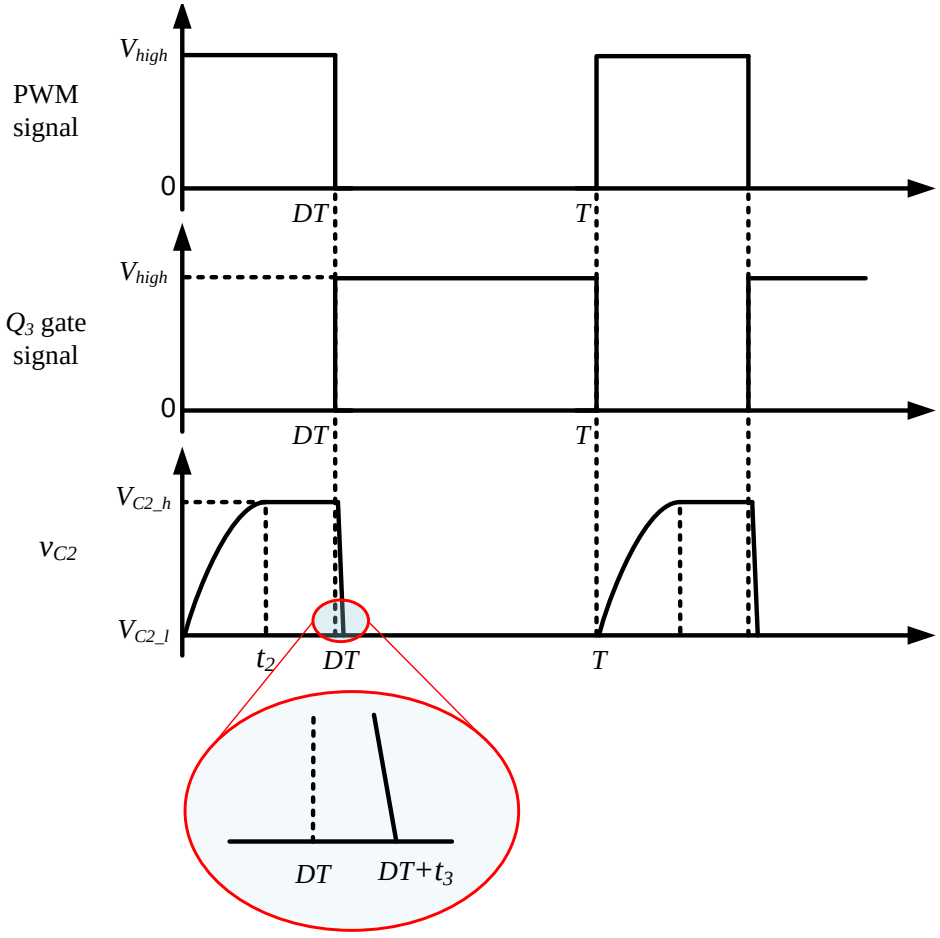

Figure 4.4 Waveforms for the input signal, Q_3 gate signal, and the output signal of the proposed PWM signal processing circuit

The circuit operation is explained as follows. Initially, Q_3 is in the off-state and v_{C2} is equal to V_{S1}. When Q_3 is turned on, capacitor C_2 discharges through R_3 and Q_3 until it reaches a new steady state value, V_{C2_1}, which depends on the voltage divider formed by R_2 and R_3. v_{C2} remains at this lower value until Q_3 is turned off at the beginning of the next switching cycle, when capacitor C_2 is charged to V_{S1} through R_2. It is noted that t_1 in Figure 4.2 and t_2 in Figure 4.4 are the same parameter. The former is a design objective while the latter is a parameter of the proposed design. Parameters t_2 and t_3 in Figure 4.4 are controlled by the value of the components used in the Figure 4.3 circuit, and will be discussed later in the design procedure section.

4.2.2 The Detection Signal Processing Circuit

The body diode conduction signal is required to be modified. The detection signal processing circuit should generate a voltage signal, which represents the length of the body diode conduction time. Therefore, the circuit output should vary proportional to the excess dead-time.

Waveforms of the input and the expected output are given in
Figure 4.5. At time t_4, the output voltage, v_{C3}, is charged up to the reference voltage, V_{S1}, for the new switching cycle. The time interval, t_{con}, is the body diode conduction time, during which v_{C3} is dropping linearly.

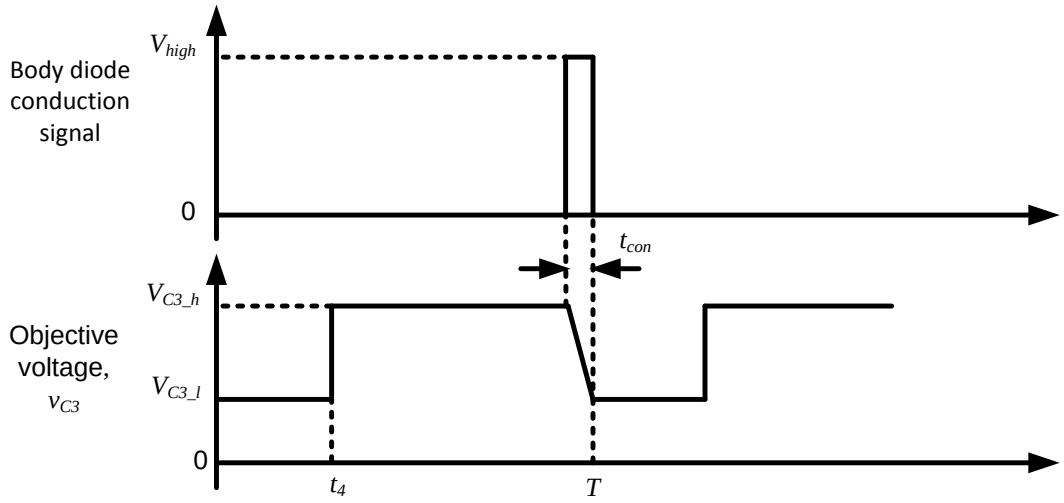

Figure 4.5 The expected output waveform of the detection signal processing circuit, where the body diode conduction signal is the input.

The proposed detection signal processing circuit is illustrated in Figure 4.6. The circuit input is the body diode conduction detection signal which feeds the gate node of MOSFET Q_5. The circuit output is v_{C3} which is the voltage across the capacitor C_3. MOSFET Q_4 is used to charge up the capacitor C_3 during each switching cycle.

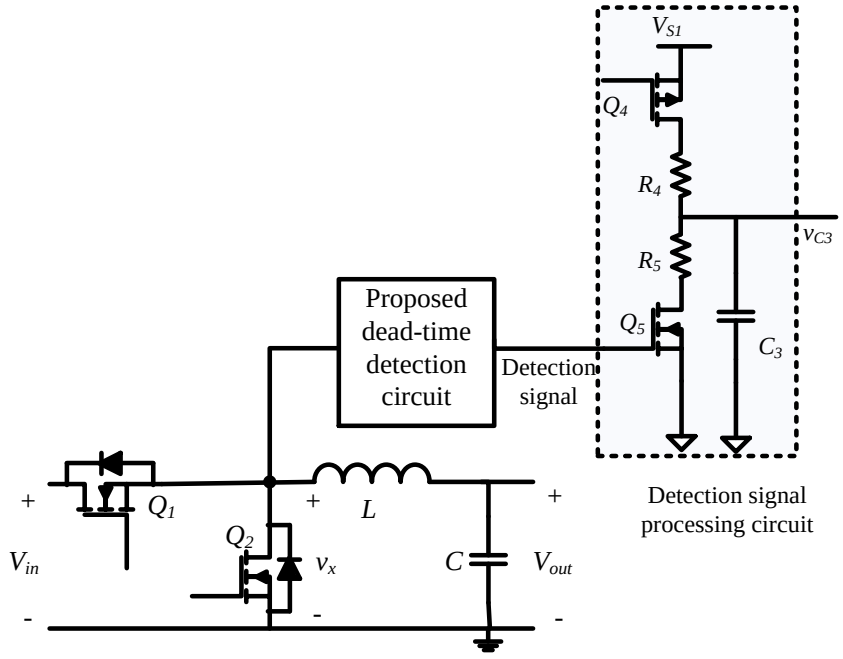

Figure 4.6 The proposed detection signal processing circuit

The circuit operation is explained as follows. The waveforms are provided in Figure 4.7. At time zero, the buck converter power MOSFET, Q_1, starts to conduct current and the body diode of the buck MOSFET Q_2 is off, therefore the detection signal is zero. Since both MOSFETs Q_4 and Q_5 are off in the detection signal processing circuit, capacitor C_3 holds its voltage from the previous state. Q_4 is turned on at t_5 by a square wave to charge up C_3 for the upcoming switching cycle. v_{C3} rises to a voltage level V_{C3_h}, which is proportional to V_{S1}. Then at the end of the switching cycle, synchronous MOSFET Q_2 is turned off while Q_1 has not yet been turned on. This leads to the body diode of Q_2, D_{body}, conducting, resulting in the pulsed detection signal from the body diode detection circuit. As a result, Q_5 turns on, and C_3 is discharged through Q_5 and R_5 until Q_5 turns off, or v_{C3} reaches a ground voltage level. Here, the body diode conduction time is very short, so when Q_5 is turned off at time T, v_{C3} drops to a voltage value V_{C3_l}, which is greater than the ground voltage, zero. V_{C3_l} is held for the first period of the next switching cycle until Q_4

turns on and the operation continues the same as the previous switching cycle.

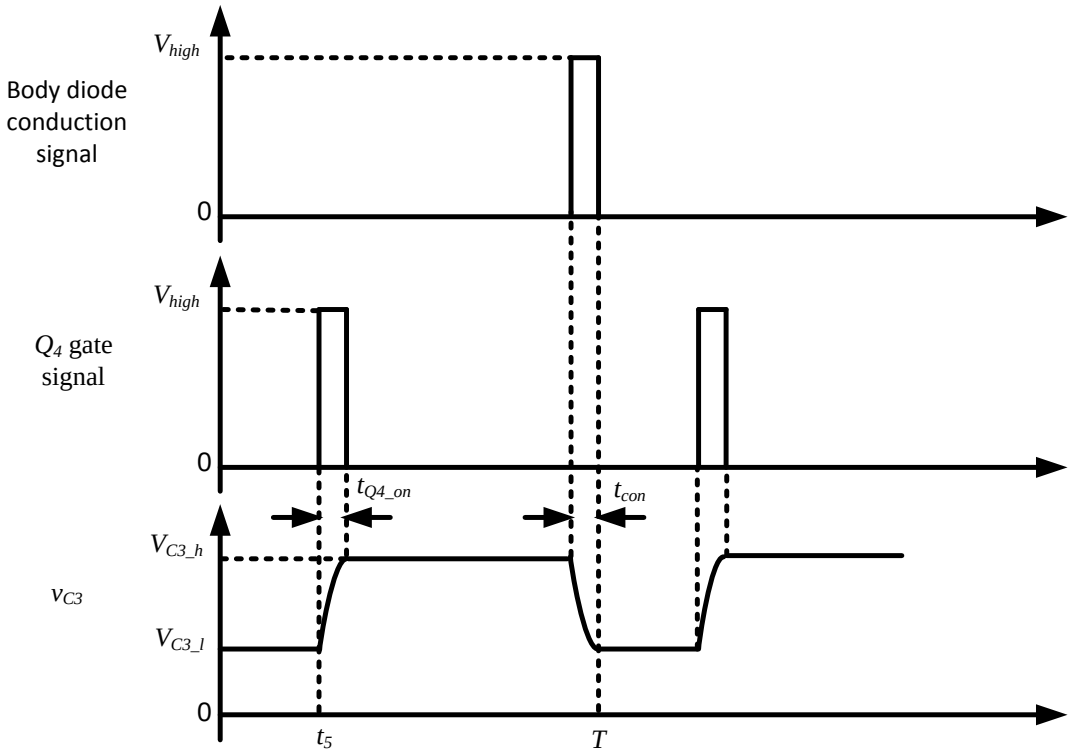

Figure 4.7 The input signal, Q_4 gate signal, and output signal of the proposed detection signal processing circuit

4.2.3 The Dead-time Optimization Circuit

If v_{C2} from the PWM processing circuit is connected to the positive input of a comparator, while v_{C3} from the detection signal processing circuit is connected to the negative node of the same comparator, the output of the comparator would be the optimized PWM signal for the power MOSFET, Q_1. Thus, the proposed dead-time optimization circuit is illustrated in Figure 4.8. Waveforms of the input (controller) PWM signal, v_{C2}, v_{C3}, and the comparator output, which is the dead-time optimized PWM signal, are provided in Figure 4.9.

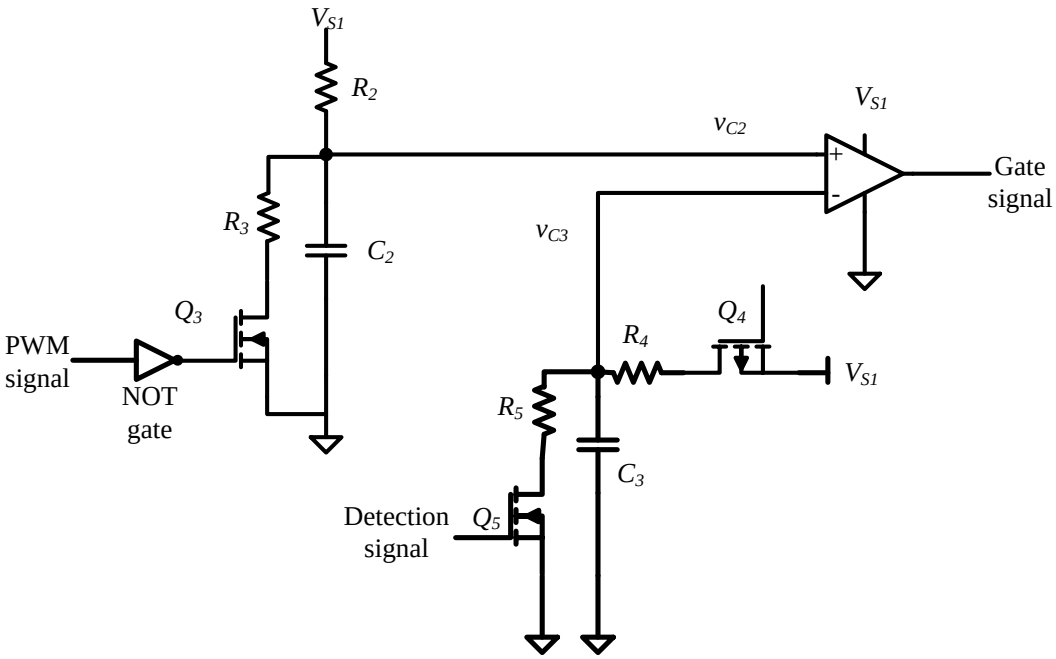

Figure 4.8 The proposed dead-time optimization circuit

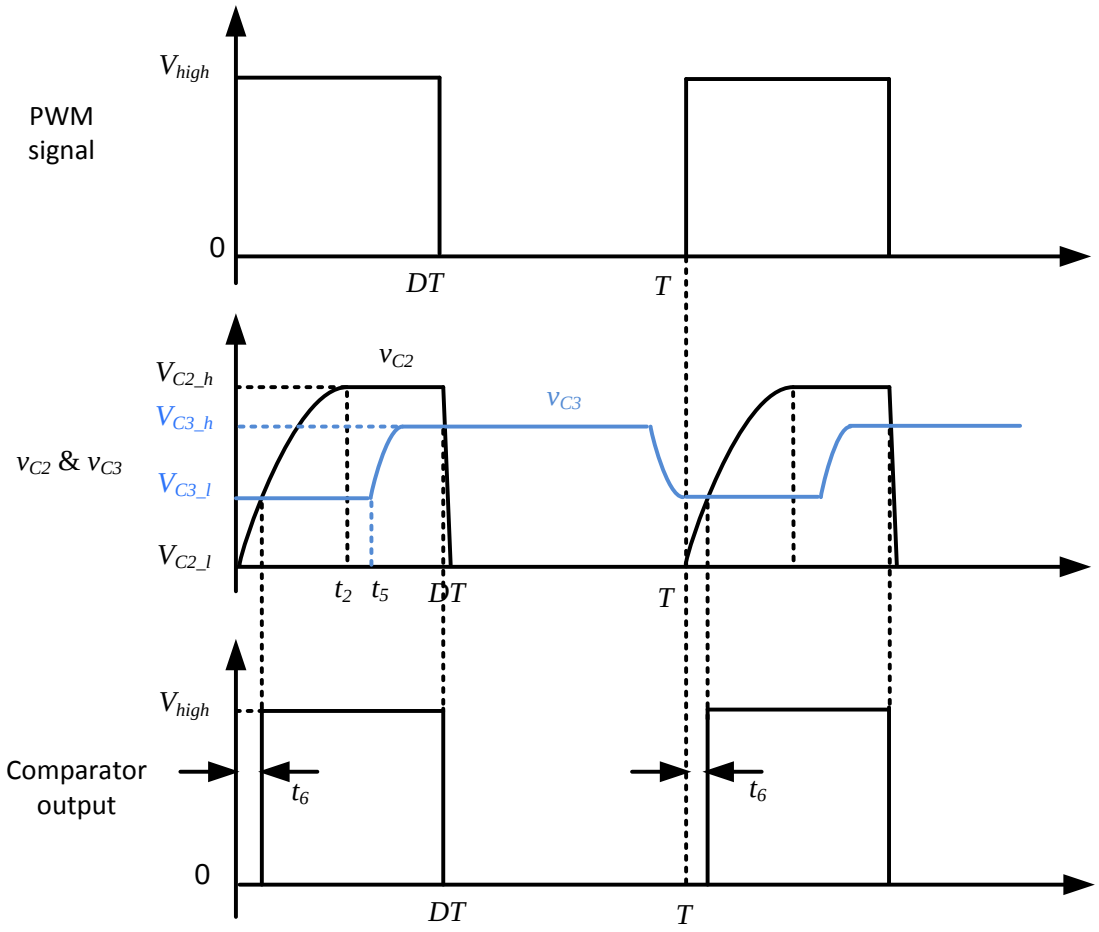

Figure 4.9 Signal waveforms of the non-optimized PWM signal, v_{C2}, v_{C3}, and the comparator output or the optimized PWM signal in the proposed dead-time optimization circuit when t_5 is smaller than DT

The dead-time optimization circuit operation is explained as follows. At time zero, the PWM signal changes from low to high, causing v_{C2} to increase, while v_{C3} is at V_{C3_l}. When v_{C2} reaches V_{C3_l}, the comparator output turns from low to high. The delay of the rising edge between the comparator output and the PWM signal, noted as t_6 in Figure 4.9, is the optimized dead-time for the rising edge of the PWM signal for the power MOSFET, Q_1.

For the PWM falling edge, when the PWM signal switches from high to low at time DT, v_{C2}

quickly drops less than v_{C3}, thus the comparator output switches from high to low. The drop occurs quickly provided the circuit parameters are properly chosen. This leads to virtually no delay between the trailing edges of the comparator output and the PWM signal.

The parameters noted in Figure 4.9, such as V_{C2_h}, V_{C3_h}, and t_2, depend on the circuit elements and will be discussed in the next section. In addition, certain the parameters influence other parameters. For example, the value of t_{con} determines V_{C3_l}. The longer t_{con} is, the lower V_{C3_l} is, and thus, the shorter t_6 is.

For the waveforms in Figure 4.9, it is assumed that t_5 is less than DT, however this is not always true. The parameter t_5 is usually preset in the dead-time controller, while DT varies primarily with input voltage and also with load. Generally, when the duty cycle of the buck converter is relatively small, t_5 is greater than DT. In these situations, waveforms of the proposed dead-time optimization circuit differ as illustrated in Figure 4.10.

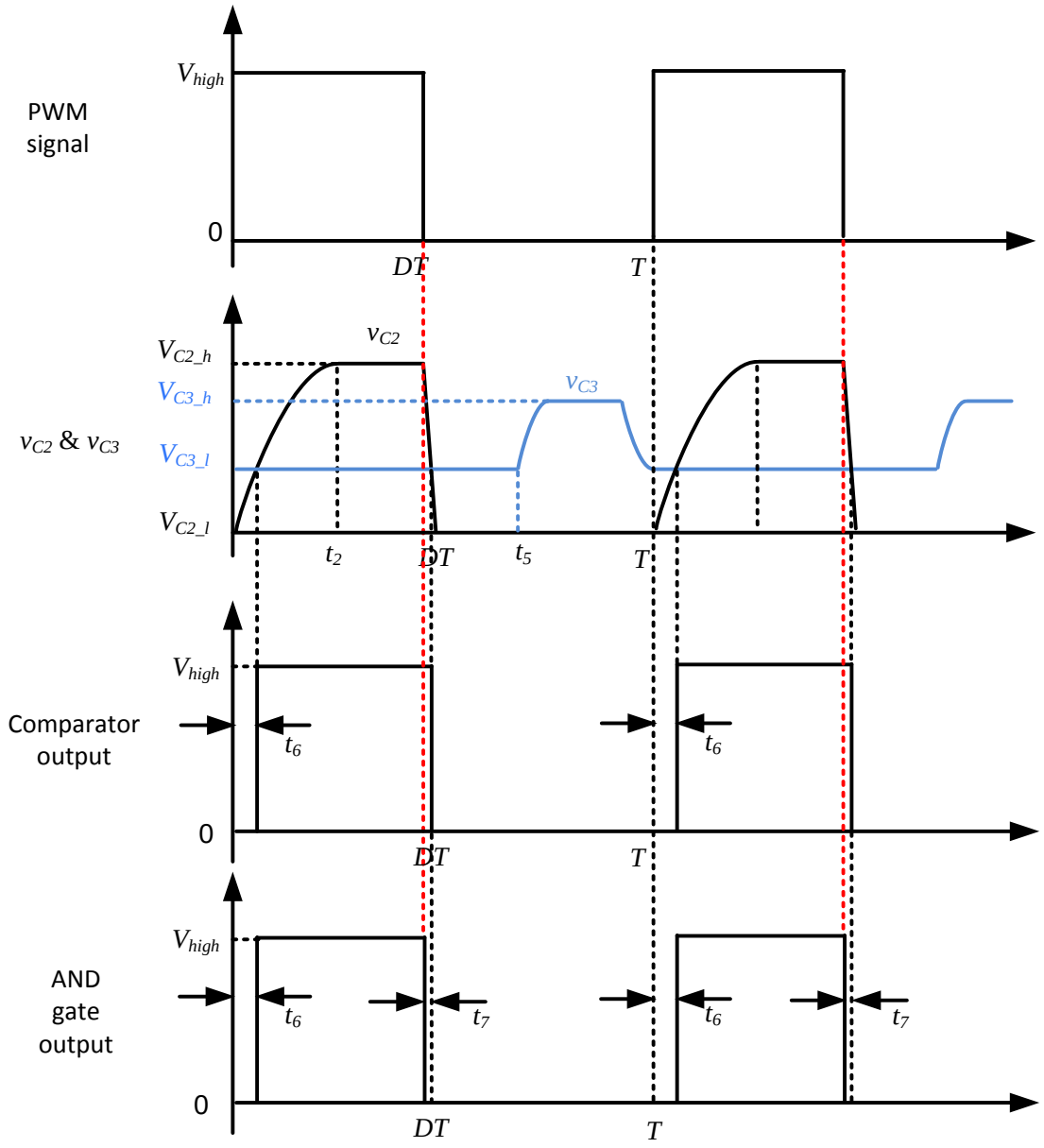

Figure 4.10 Signal waveforms of the non-optimized PWM signal, v_{C2}, v_{C3}, and the comparator output or the optimized PWM signal in the proposed dead-time optimization circuit when t_5 is greater than DT

When DT is less than t_5, the trailing edge of the comparator output has a small delay, t_7, from that of the PWM signal. The delay is due to the capacitor voltage, v_{C2}, not being able to drop

instantaneously. This delay is much smaller in Figure 4.9 than in Figure 4.10, since the comparator output reverses when v_{C2} drops to V_{C3_h}. In Figure 4.10, v_{C2} needs to drop further than V_{C3_l}, resulting in the delay in the trailing edge. To avoid this delay, an AND gate is used, with the PWM signal and the comparator output as its two inputs. Therefore, the AND gate output has the rising edge with the optimized dead-time which eliminates the undesired delay at the trailing edge.

4.3 Dead-time Optimization Circuit Design Procedure

In this section, equations of circuit variables are provided, in order to make it clear how circuit elements influence the waveforms. Design procedures for the PWM signal and detection signal processing circuits are also introduced. Requirements for each element in the circuit are provided as conclusions at the end of each subsection.

4.3.1 The PWM Signal Processing Circuit Design Procedure

Referring to Figure 4.3 and Figure 4.4, during time 0 to t_2, MOSFET Q_3 is off, so the current from the voltage source V_{S1} flows through R_2 to charge up capacitor C_2. Therefore, the dynamic equations of the circuit during this interval are given by (4.1) and (4.2), where v_{C2} and v_{R2} are the voltages across elements C_2 and R_2 respectively, and i_{C2} and i_{R2} are the currents flowing through C_2 and R_2. It is noted that in the analysis that follows, all lower case voltages and currents are a function of time.

$$v_{R2} + v_{C2} = V_{S1} \tag{4.1}$$

$$i_{C2} = C_2 \frac{dv_{C2}}{dt} = i_{R2} = \frac{v_{R2}}{R_2} \tag{4.2}$$

Equations (4.1) and (4.2) can be written as a single first-order ordinary differential equation, as given by (4.3), with the initial state of the capacitor voltage given by (4.4).

$$R_2 C_2 \frac{dv_{C2}}{dt} + v_{C2} - V_{S1} = 0 \tag{4.3}$$

$$v_{C2}(0_+) = \frac{R_3}{R_2 + R_3} V_{S1} \tag{4.4}$$

The solution to (4.3) is provided in (4.5), where time constant τ_2 is the time for v_{C2} to reach 63% of V_{C2_h} from V_{C2_l}. Furthermore, at $3\tau_2$, v_{C2} rises 95% of V_{C2_h}. Therefore, t_2 in Figure 4.4 can be approximated using (4.6).

$$v_{C2} = V_{S1} - \frac{R_2}{R_2 + R_3} V_{S1} e^{-t/\tau_2}, \qquad \tau_2 = R_2 C_2 \tag{4.5}$$

$$t_2 \approx 3\tau_2 \tag{4.6}$$

At time DT, Q_3 is turned on by the inverted PWM signal, allowing C_2 to discharge through R_2 and Q_3. The dynamic equations of this transition are given by (4.7) and (4.8), where v_{R3} is the voltage across R_3 and i_{R3} is the current through R_3.

$$v_{C2} = v_{R3} = V_{S1} - v_{R2} \tag{4.7}$$

$$i_{C2} = C_2 \frac{dv_{C2}}{dt} = i_{R3} - i_{R2} = \frac{v_{R3}}{R_3} - \frac{v_{R2}}{R_2} \tag{4.8}$$

Similarly, (4.7) and (4.8) can also be expressed as a first-order ordinary differential equation, given by (4.9). Equation (4.10) provides the initial state of v_{C2}.

$$R_3 C_2 \frac{dv_{C2}}{dt} - \left(1 + \frac{R_3}{R_2}\right) v_{C2} + \frac{R_3}{R_2} V_{S1} = 0 \tag{4.9}$$

$$v_{C2}(0_+) = V_{S1} \tag{4.10}$$

The solution to (4.9) is provided in (4.11), where the time constant of this first-order transition is τ_3. The parameter t_3 in Figure 4.4 is the time for v_{C2} to decrease from V_{C2_h} to V_{C2_l}. Therefore, t_3 can be approximated by (4.12).

$$v_{C2} = \frac{R_3}{R_2 + R_3} V_{S1} + \frac{R_2}{R_2 + R_3} V_{S1} e^{-t/\tau_3}, \qquad \tau_3 = R_3 C_2 \tag{4.11}$$

$$t_3 \approx 3\tau_3 \tag{4.12}$$

Using (4.5) and (4.11), the parameters, V_{C2_h} and V_{C2_l}, in Figure 4.4, Figure 4.9, and Figure 4.10, are given by (4.13).

$$V_{C2\_h} = V_{S1}, \qquad V_{C2\_l} = \frac{R_3}{R_2 + R_3} V_{S1} \tag{4.13}$$

The parameter t_3 should be much less than t_2 (Figure 4.4), therefore, τ_3 should be much less than τ_2. Accordingly, R_3 is much less than R_2. Furthermore, if R_3 is much less than R_2, V_{C2_l} can drop to a very low value, leaving design flexibility for the choice of V_{C3_l}. As for t_2, it should be less than DT, except for very low duty cycles, so the requirement can be expressed by (4.14) when choosing the resistor R_2 and the capacitor C_2.

$$0.01T \leq \tau_2 = R_2 C_2 = \frac{t_2}{3} \leq 0.06T \tag{4.14}$$

4.3.2 Detection Signal Processing Circuit Design Procedure

For the detection signal processing circuit, the discharge rate of capacitor C_3 can be neither too fast nor too slow, so that during t_{con} (representing the body diode conduction time), v_{C3} will reduce from V_{C3_h} to V_{C3_l}, yet not to zero, nor V_{C2_l}. v_{C3} will not be less than V_{C2_l}, provided that t_{con} is between zero and $0.05T$. The circuit elements should then be picked to meet this requirement.

The dynamic equations of the circuit when capacitor C_3 is charged at t_5 (Figure 4.9) are derived in the same manner as that of capacitor C_2. Equations (4.15) and (4.16) are derived using Kirchhoff's voltage and current laws, respectively. Equations (4.15) and (4.16) can be written as a first-order ordinary differential equation, given in (4.17), where (4.18) is the initial state of v_{C3}.

The solution to (4.17) is provided in (4.19).

$$v_{C3} + v_{R4} = V_{S1} \tag{4.15}$$

$$i_{C3} = C_3 \frac{dv_{C3}}{dt} = i_{R4} = \frac{v_{R4}}{R_4} \tag{4.16}$$

$$R_4 C_3 \frac{dv_{C3}}{dt} + v_{C3} - V_{S1} = 0 \tag{4.17}$$

$$v_{C3}(0_+) = V_{C3\_l} \tag{4.18}$$

$$v_{C3}(t) = V_{C3\_l} + \left(V_{S2} - V_{C3\_l}\right) e^{-t/\tau_4}, \qquad \tau_4 = R_4 C_3 \tag{4.19}$$

Similarly, dynamic equations during the transition when C_3 is discharged are given by (4.20) and (4.21). The equivalent first-order ordinary differential equation is provided in (4.22) with its initial state. The solution to this equation is given by (4.23).

$$v_{C3} = v_{R5} \tag{4.20}$$

$$i_{C3} = C_3 \frac{dv_{C3}}{dt} = i_{R5} = \frac{v_{R5}}{R_5} \tag{4.21}$$

$$R_5 C_3 \frac{dv_{C3}}{dt} - v_{C3} = 0, \quad v_{C3}(0_+) = V_{S1} \tag{4.22}$$

$$v_{C3}(t) = V_{S1} - V_{S1} e^{-t/\tau_5}, \qquad \tau_5 = R_5 C_3 \tag{4.23}$$

The value of V_{C3_l}, which is a floating variable related to the value of t_{con}, is expressed by (4.24).

$$V_{C3\_l} = V_{S1}(1 - e^{-t_{con}/\tau_5}) \tag{4.24}$$

As noted at the beginning of this section, τ_5 can neither be too long, nor too short. A reasonable range for τ_5 is three time constants between 5% and 15% of a switching period, expressed by (4.25).

$$0.05T \leq 3\tau_5 \leq 0.15T \tag{4.25}$$

Among the four time constants, τ_2 - τ_5, in this section, τ_2 is more critical than τ_3. In addition, τ_5 is more critical than τ_4. τ_2 represents the inverse of the rising slope of v_{C2}. If τ_2 is large, v_{C2} rises slowly, resulting in a large dead-time. As an optimum minimized dead-time is required, we need to minimize τ_2, while ensuring that τ_2 is sufficiently large to prevent cross-conduction. Therefore τ_2 is governed by (4.14). On the other hand, τ_3 is less important, since an AND gate is used to eliminate its effect at the falling edge of v_{C2}. Similarly, the value of τ_5 influences the dead-time directly while that of τ_4 does not.

4.4 Design Example and Simulation Results

4.4.1 Design Example

Using the design procedure provided in Section 4.3, a PWM signal processing circuit design was completed. A list of the circuit elements and is provided in Table 4.1. Values of the resistors and capacitors are chosen according to the standard E24 values for circuit elements, as given in 0. An Si1555DL MOSFET was chosen for the Q_3 MOSFET, due to its low gate charge and fast transition speed [17]. An NC7SZ04 inverter from FairChild Semiconductor was selected for the NOT gate. This device has a propagation delay of 2.9ns, which is suitable for a 500kHz switching frequency application [18].

Table 4.1 The parameters in the design of the PWM signal processing circuit

Parameter	**Value**
Voltage Source, V_{S1}	6V
Resistor, R_2	430Ω
Resistor, R_3	51Ω
Capacitor, C_2	51pF
MOSFET Q3	**Si1555DL**
Gate Charge, Q_g	0.8nC
Switch On Time, t_{on}	16ns
Switch Off Time, t_{off}	10ns
Drain-source Voltage, V_{ds}	20V
Drain Current, I_d	0.66A
NOT gate	**NC7SZ04**
Propagation Delay, t_{pd}	2.9ns
Input Rise and Fall Rate	5ns/V

The circuit parameters used in the detection signal processing circuit are given in Table 4.2. The voltage source, V_{S1}, was chosen to be 6V, which is the same voltage required for the buck controller. Resistors R_4 and R_5 were chosen to be equal so that the charge and discharge transitions for capacitor C_3 are symmetric, resulting in maximum design flexibility for t_{con}.

Table 4.2 The parameters in the design of the detection signal processing circuit

Parameter	Value
Voltage Source, V_{S1}	6V
Resistor, R_4	10kΩ
Resistor, R_5	10kΩ
Capacitor, C_3	5.1pF

The final component in the dead-time optimization circuit that was selected is the comparator. Not all high speed comparators can meet the design requirements. More specifically, comparators with small bias currents do not work well in this application. The bias current is defined as the average of the two input currents, provided in the manufactures datasheet. Comparators with very low bias currents (e.g. several nA), tend to charge up capacitor C_3 when v_{C2} is larger than v_{C3}, which leads to undesired circuit operation. Therefore, an LT1394 comparator was selected, which has an input bias current of 2μA [19].

Table 4.3 Parameters of the comparator LT1394

Comparator	LT1394
Propagation Delay, t_{pd}	7ns
Input current, I_{in_c}	10mA
Input Bias Current, I_B	2μA

4.4.2 Simulation Results

The proposed dead-time optimization circuit was simulated using PSIM9. The circuit is provided in Figure 4.11 and waveforms are provided in Figure 4.12.

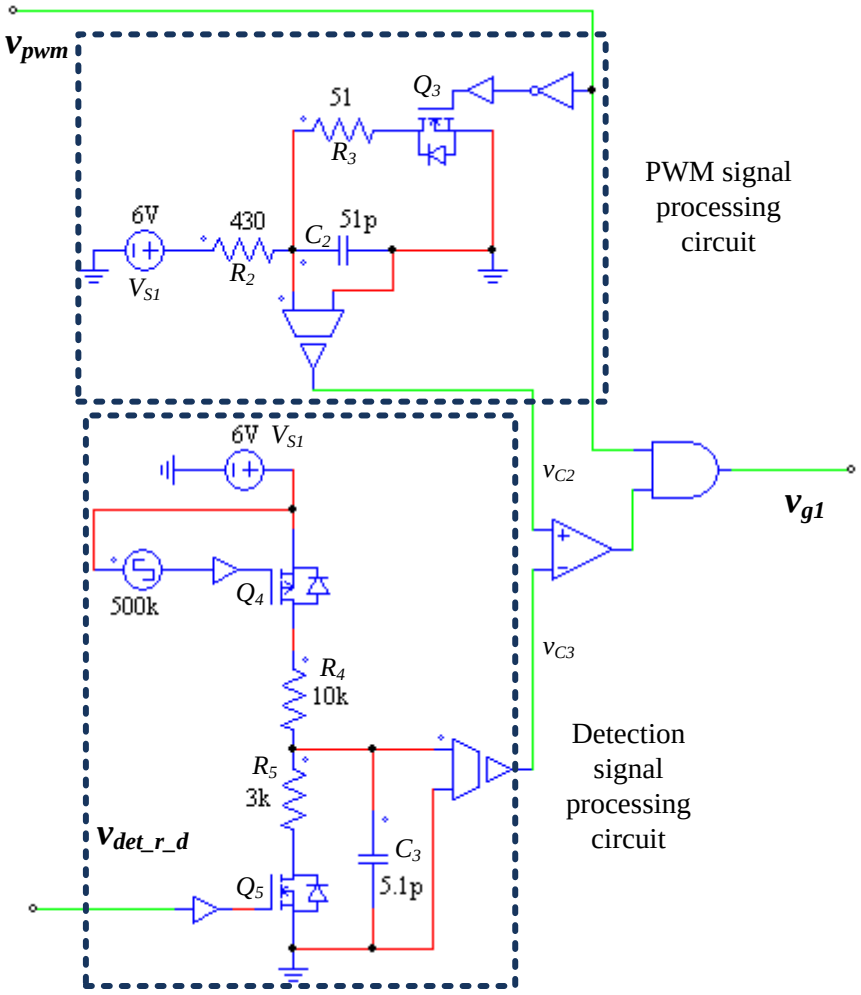

Figure 4.11 The dead-time optimization simulation circuit

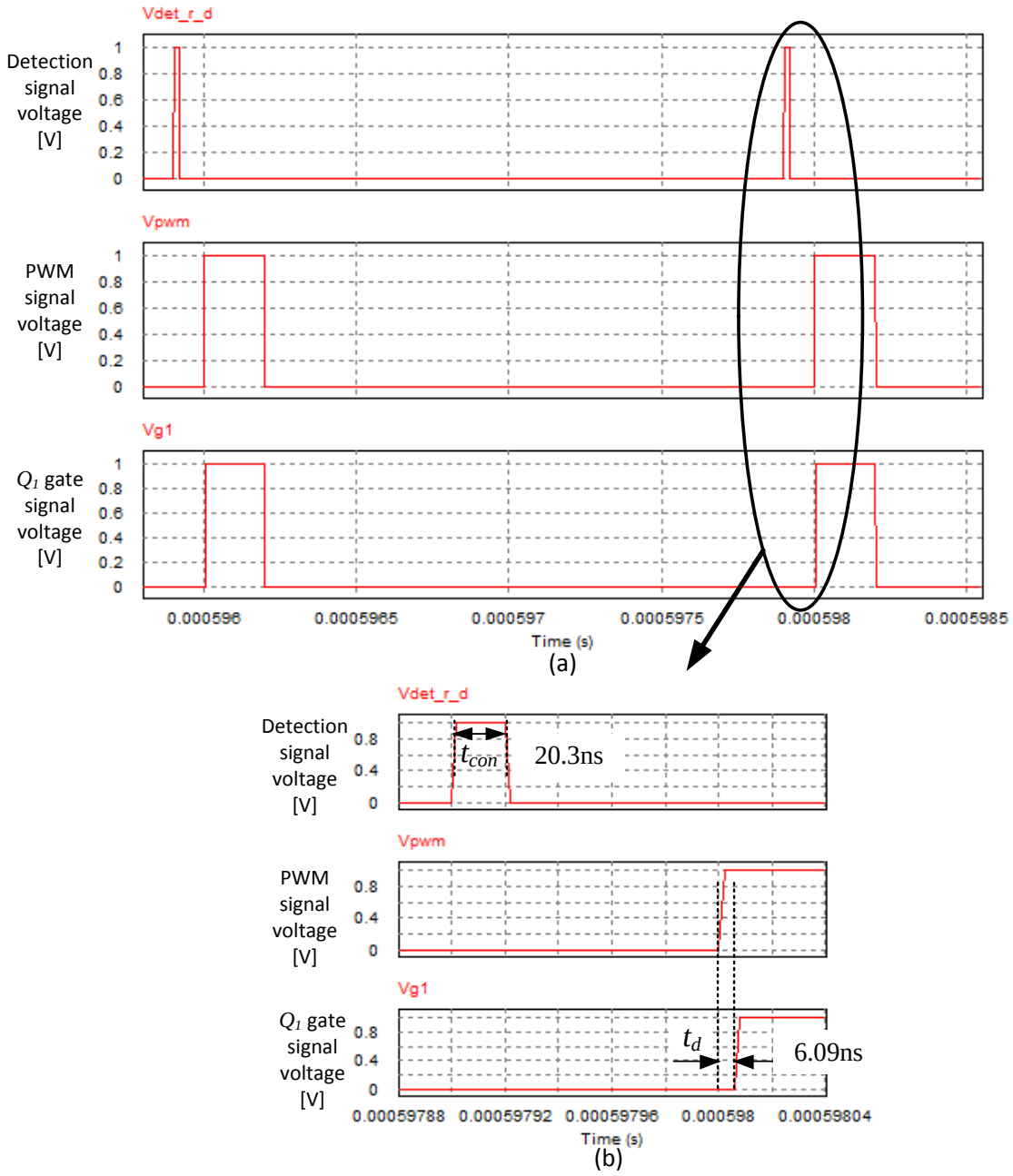

Figure 4.12 Simulation results of the dead-time optimization circuit (a) the delayed detection signal for the rising edge, the PWM signal, and the gate signal, (b) the enlarged drawing of the above signals

To test the proposed dead-time optimization circuit, pulse signals with a width of 20ns were input as a detection signal to replicate the output of the circuit proposed in Chapter 3. From

Figure 4.11(b), it is noted that the delay time between the rising edge of the PWM signal and that of the Q_1 gate signal is 6.09ns. This indicates that the proposed circuit is able to produce a smaller dead-time, given a large dead-time from the previous switching cycle. Therefore, the circuit operates as expected

4.5 Summary

In this chapter a novel dead-time optimization circuit has been proposed for the synchronous buck converter. In addition to the circuit, a design procedure, design example and simulation results have been presented.

In order to minimize body diode conduction, which degrades the power converter efficiency, the proposed body diode detection circuit introduced in Chapter 3 and the proposed dead-time optimization circuit introduced in this chapter can be combined into a new dead-time controller circuit. The combined circuit and simulation results are presented in Chapter 5.

Chapter 5

Simulation Results of the Dead-time Control Circuit

5.1 Overview

Body diode conduction in a synchronous buck DC-DC converter degrades the power conversion efficiency and increases heat generation in the buck synchronous MOSFET, which degrades the converter reliability. To solve this problem, a new circuit has been proposed to minimize body diode conduction. To minimize body diode conduction, detection and optimization circuits are required. A body diode conduction detection circuit was proposed in Chapter 3 and an optimization circuit was proposed in Chapter 4.

In this chapter, a current mode PWM controller is first presented in Section 5.2. It is used to regulate the output voltage to compensate for input voltage, or load current changes. Next, the proposed dead-time controller is integrated with the PWM control circuit, forming the complete closed-loop buck converter control for the PWM rising edge in Section 5.3. The dual PWM edge combined circuit is presented in Section 5.4. These sections include simulation waveforms using PSIM9, verifying proper closed- loop operation of the buck converter. In Section 5.5, a comparison is made between the proposed circuit and a benchmark circuit, illustrating the improvements in dead-time and efficiency with the proposed circuit.

5.2 Closed-loop Control

A current mode PWM controller was designed to regulate the output voltage of the buck converter [20]-[22]. The controller and synchronous buck converter are illustrated in Figure 5.1. Waveforms illustrating the current mode PWM controller operation are illustrated in Figure 5.2. The clock signal initiates the PWM pulse to turn the high-side buck switch at a fixed frequency,

e.g. 500kHz. The pulse ends when the inductor current reaches the threshold established by the error amplifier, which amplifies any low frequency error in the output voltage in comparison to the desired reference output. The error signal controls the inductor peak current rather than the width of the pulse, and therefore is called current mode control. Four switching cycles of the output voltage of the converter are illustrated in Figure 5.3. The maximal, average, and minimal value of the output at steady state is 1.212V, 1.200V, and 1.182V respectively. Therefore, the converter output ripple is 30mV.

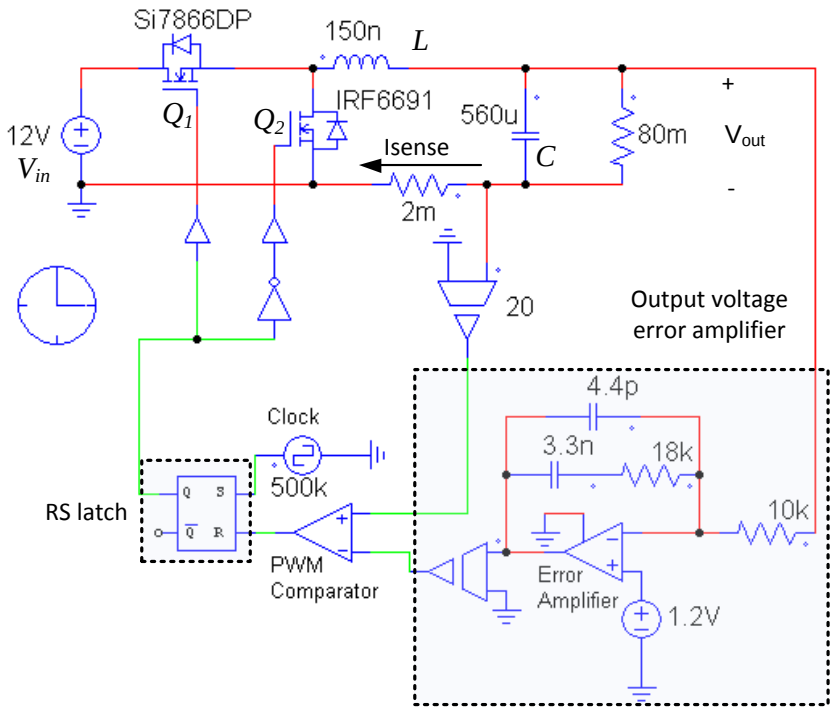

Figure 5.1 A current mode PWM controller for the buck converter

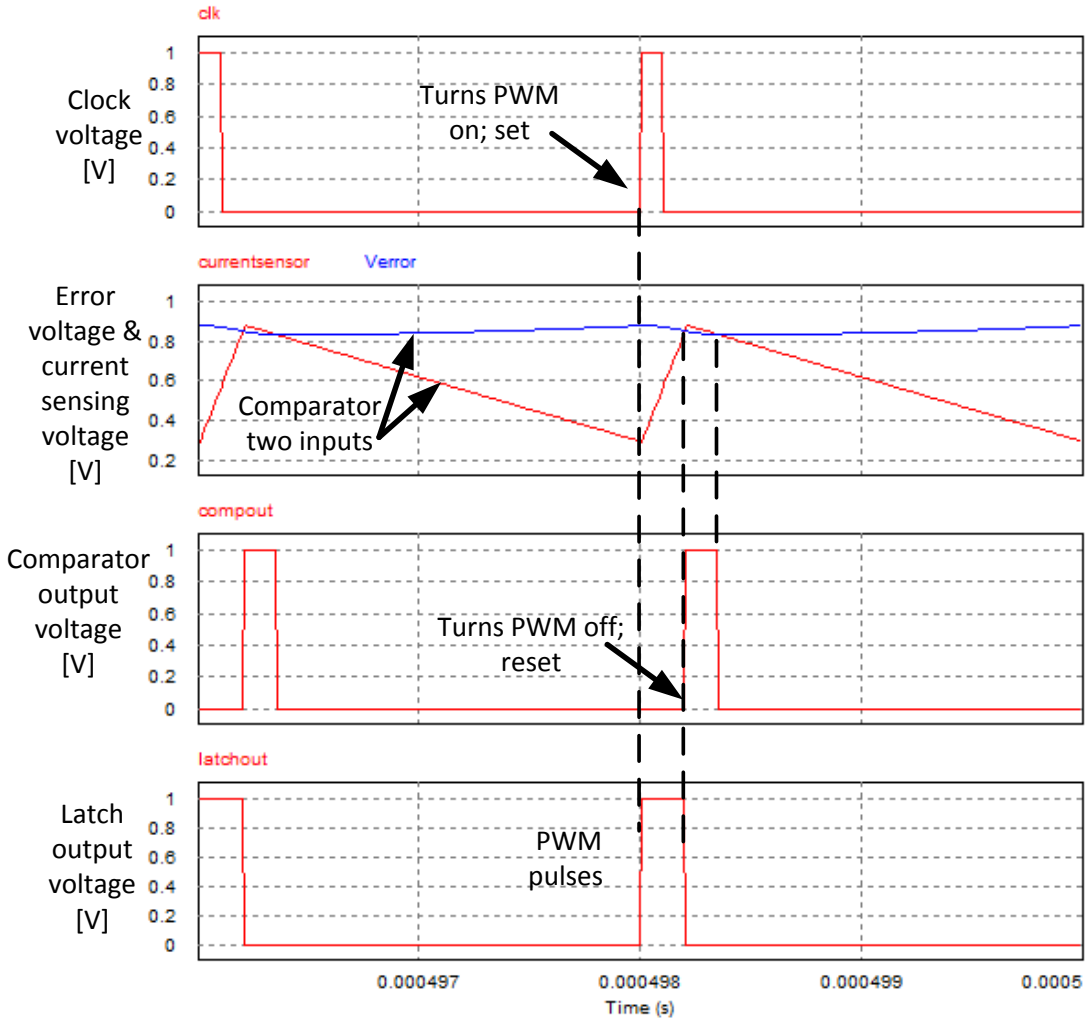

Figure 5.2 Waveforms from the current mode PWM controller

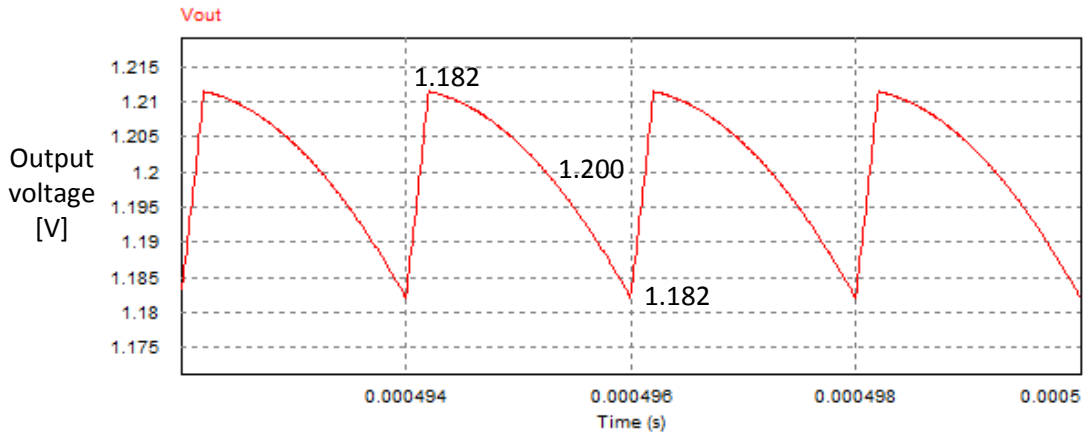

Figure 5.3 Four switching cycles of the output voltage of the buck converter

There are several advantages of current mode control. First, by controlling the peak current, the pole due to the buck converter output filter inductor is effectively removed from the dynamics, so there is only one pole due to the output capacitor, compared with 2 poles using voltage mode control [21]. Therefore, the error amplifier compensation circuit is simpler. Secondly, the input voltage changes are compensated instantaneously by the current sensor and PWM comparator, allowing the error amplifier to correct for load variation exclusively. Finally, current mode control monitors the peak inductor current, simplifying over current protection circuit design.

5.3 PWM Rising Edge with Dead-time Control

The circuits proposed in Chapter 3 and Chapter 4 were integrated with the current mode PWM controller presented in Section 5.2. The combined circuit minimizes the dead-time for the rising edge of the PWM signal, and is illustrated in Figure 5.4. The proposed dead-time control circuit follows the current mode PWM controller output signal, v_{pwm}.

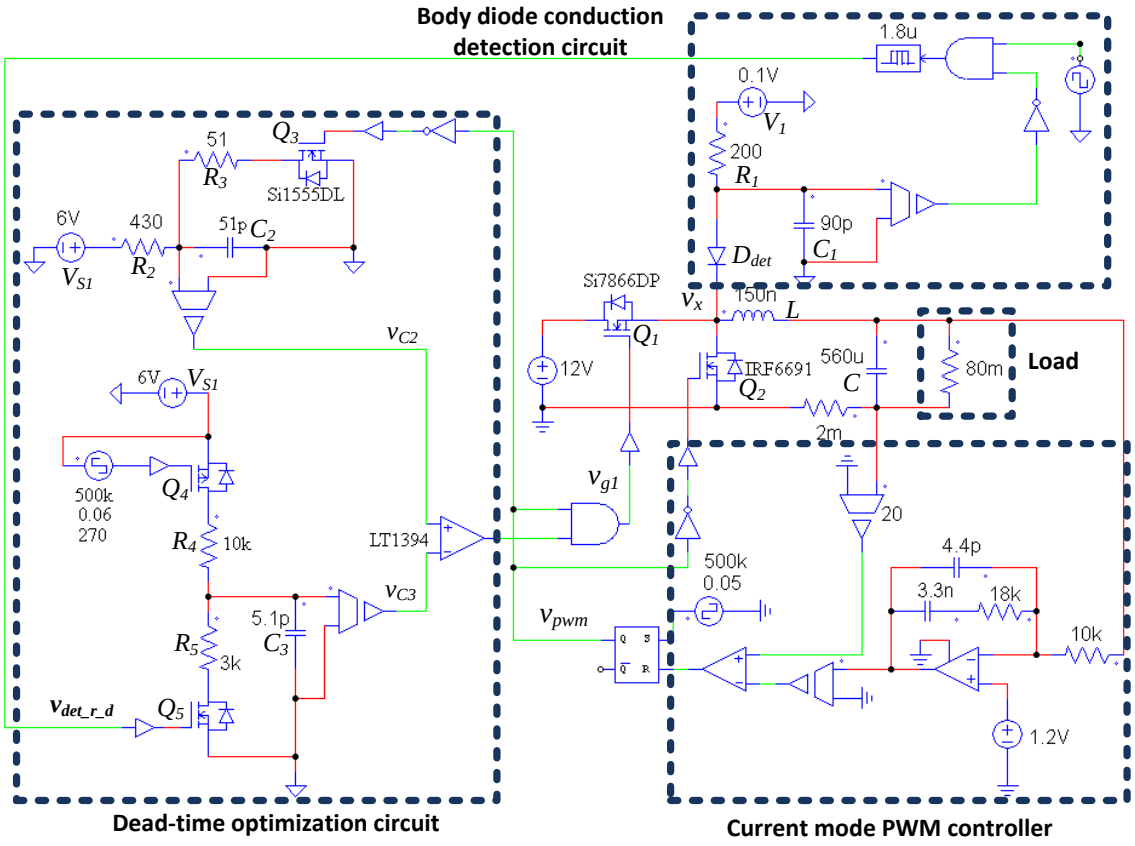

Figure 5.4 The proposed dead-time control circuit for the rising edge combined with the current mode PWM control circuit

The circuit in Figure 5.4 has 4 sub-circuits: 1) the synchronous buck converter power stage, 2) the current mode PWM control circuit, 3) the dead-time detection circuit, and 4) the dead-time optimization circuit. Each of these sub-circuits has been introduced. The current mode PWM controller generates PWM signals that ensure the output voltage of the buck converter meets the design specifications. The PWM signal and the dead-time detection signal from last switching cycle are input to the dead-time optimization circuit. The output of the dead-time optimization circuit is the gate signal for the power MOSFET Q_1, with an optimized minimal dead-time inserted on the rising edge of the original PWM signal to prevent simultaneous turn-on of Q_1 and Q_2.

Simulation results of this circuit using PSIM9 are given in Figure 5.5. Waveforms of the output of the PWM controller, v_{pwm}, the gate signal for Q_1, v_{g1}, and the voltage across Q_2, v_x, are provided. Referring to Figure 5.5(b), it is clear that there is a small time delay, t_d, between the rising edge of v_{pwm} and that of v_{g1}. This is achieved by the dead-time optimization circuit, and the value of t_d is affected by the body diode conduction time of the synchronous MOSFET Q_2 in last switching cycle. The body diode conduction time of Q_2 for this switching cycle, t_{con_org}, is noted, as well as t_d.

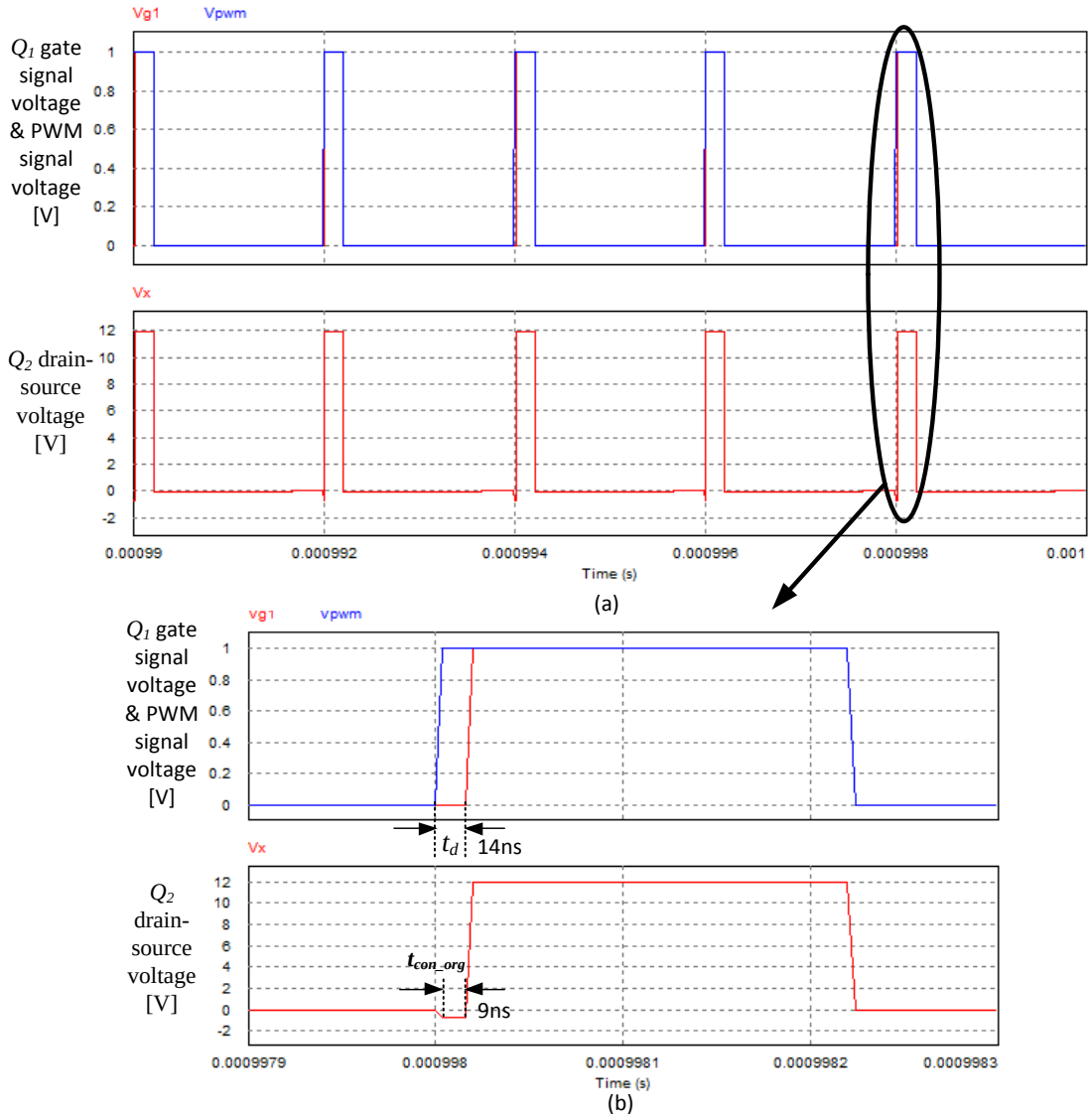

Figure 5.5 (a) PWM controller output, v_{pwm}, Q_1 gate signal, v_{g1}, and v_x over five switching cycles; and (b) v_{pwm}, v_{g1}, and v_x illustrating one pulse width

5.4 Dual PWM Edge Dead-time Control

In the last subsection, it was noted that the dead-time control of the proposed circuit is achieved by adding an optimized delay to the rising edge of the pulse. However, the trailing edge of the pulse also requires dead-time optimization. Therefore, a second dead-time optimization

circuit can be added to postpone the rising edge of the Q_2 gate signal to avoid current shoot through. The complete circuit with two dead-time optimizers adjusting the dead-time at either edge of the PWM pulse is provided in Figure 5.6.

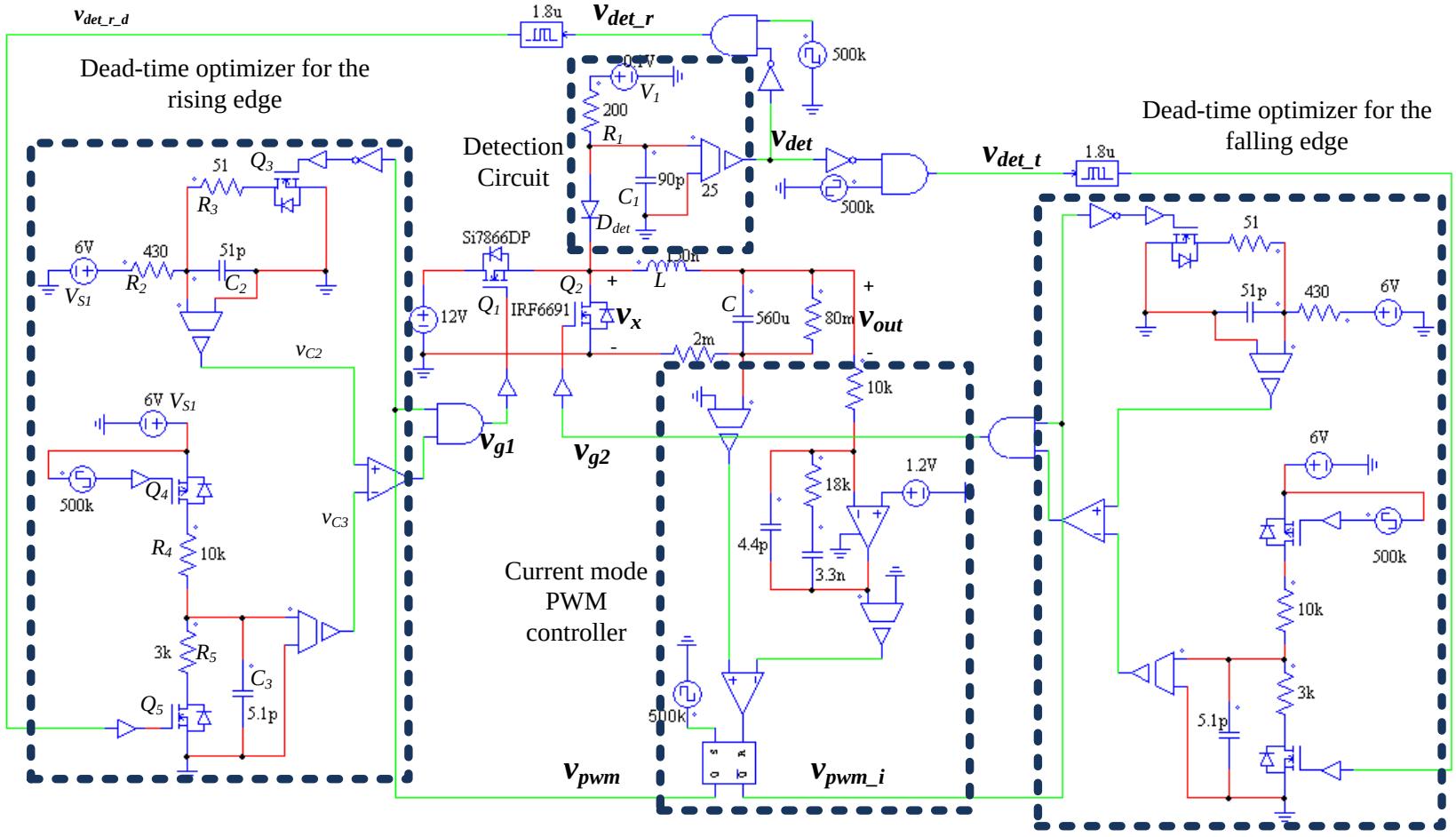

Figure 5.6 Complete dead-time optimization circuit including dual edge PWM dead-time control and closed-loop output voltage regulation

The complete dead-time control circuit was simulated using PSIM9. Waveforms of the Q_1 gate signal, v_{g1}, the PWM pulse generated by the current mode PWM controller, v_{pwm}, Q_2 gate signal, v_{g2}, the inverted PWM pulse, v_{pwm_i}, and the voltage across the synchronous buck MOSFET Q_2, v_x, in steady state are provided in Figure 5.7. One PWM pulse of the above noted waveforms in provided in Figure 5.7(b). From the figure, it is noted that the rising edges of both v_{pwm} and v_{pwm_i} are postponed while the trailing edges are not. Since v_{pwm} and v_{pwm_i} are complementary, dead-time is added to both edges of the pulse. Body diode conduction of the synchronous MOSFET occurs when the waveform is negative. Body diode conduction intervals are visible in Figure 5.7(c) and (d). The body conduction time at the rising edge, t_{bc_r}, is 4.06ns. While that at the trailing edge, t_{bc_t}, is 3.98ns. These values are very low, and combined, represent less than 0.5% of a total switching period.

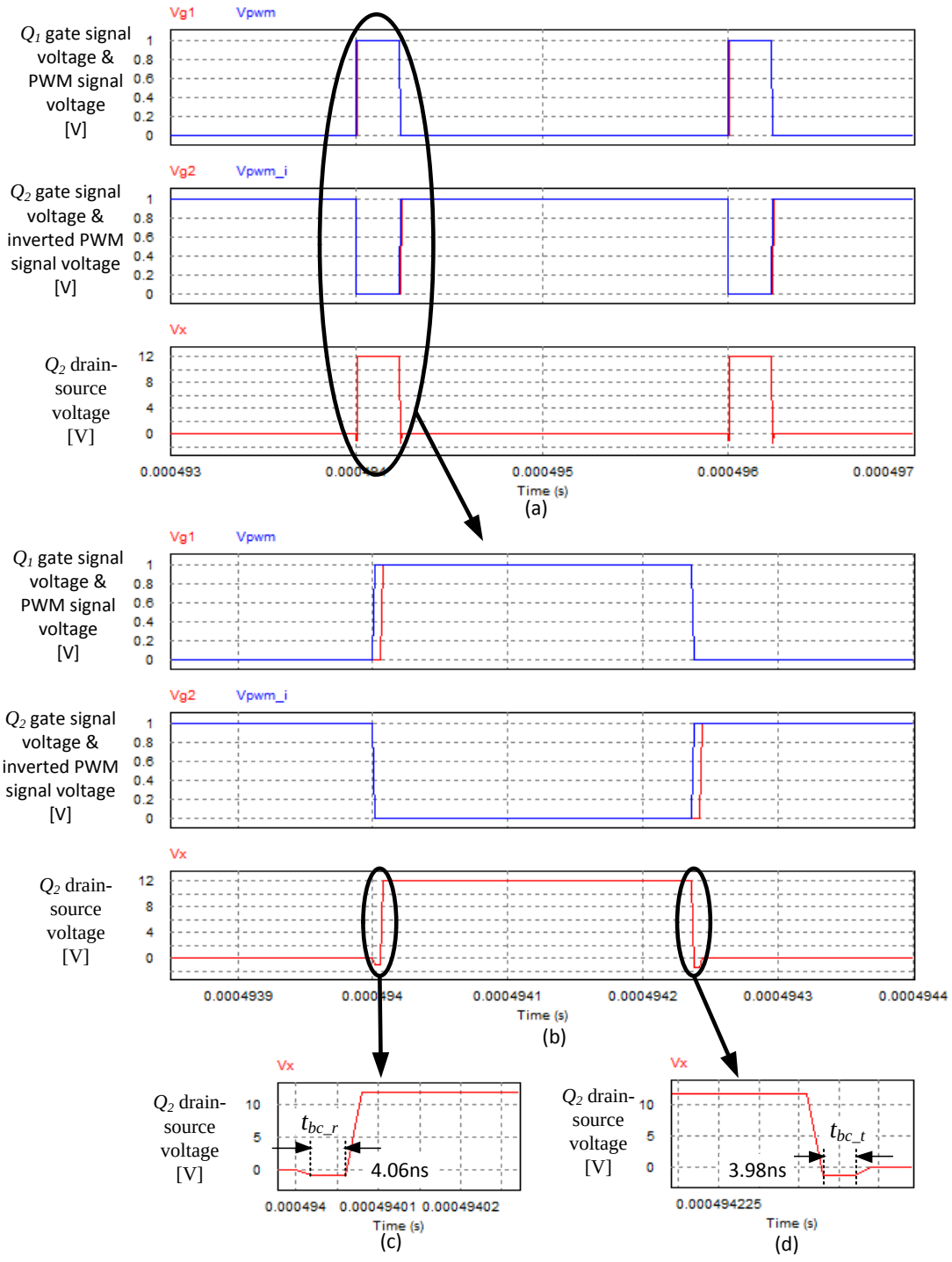

Figure 5.7 (a) Waveforms of the Q_1 gate signal, PWM signal, Q_2 gate signal, inverted PWM signal, and the voltage at the joint point of the two MOSFETs; (b) one PWM pulse; (c) body diode conduction time at the rising edge; (d) body diode conduction time at the falling edge

5.5 Comparison with Adaptive Dead-time Control

In this subsection, the proposed circuit is compared with a benchmark adaptive dead-time controller.

5.5.1 Body Diode Conduction Time Comparison

Adaptive dead-time control is used in the TPS2832, fast synchronous buck MOSFET driver IC. In the datasheet for this driver, it is noted that the minimal dead-time achievable is 15ns [23]. Therefore, a fixed dead-time controller was modeled in PSIM to represent the TPS2832 benchmark circuit. The dead-time was set to 15ns. The buck converter with the current mode PWM controller and a 15ns fixed dead-time controller is illustrated in Figure 5.8.

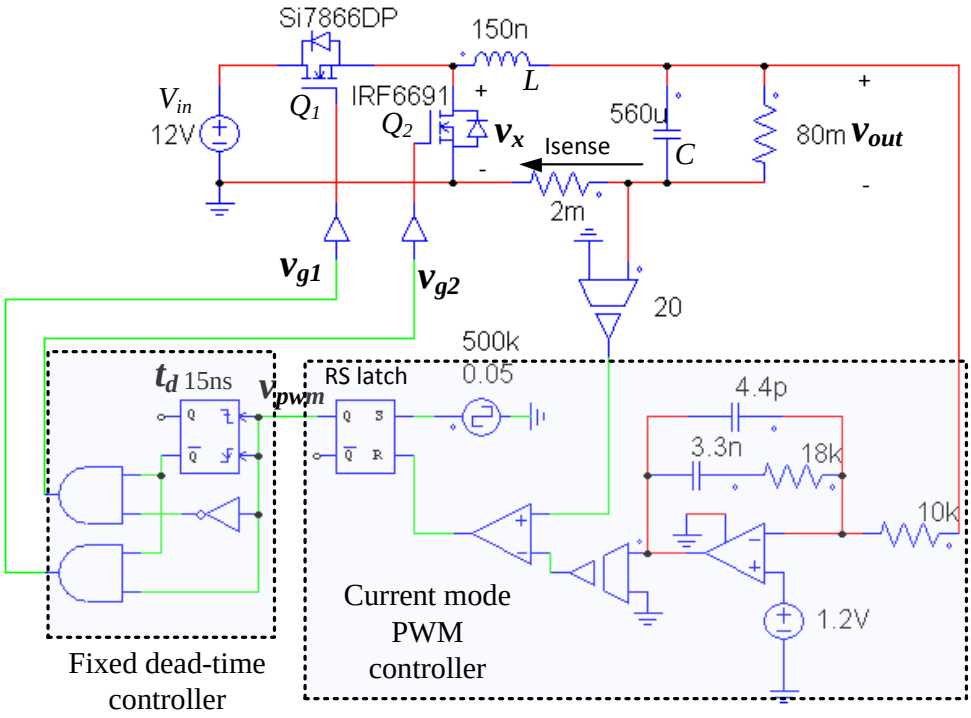

Figure 5.8 The benchmark circuit (fixed dead-time control)

Waveforms of the voltage across the buck synchronous rectifier, v_x, for the benchmark circuit and the proposed circuit are provided in Figure 5.9 for a load current of 15A. The duration

when v_x is negative is the conduction time of the synchronous MOSFET body diode. It is noted that the body diode conduction times at rising and trailing edges for fixed dead-time control are 15.4ns and 15.9ns, respectively, and those in the proposed circuit are 4.06ns and 3.98ns. Therefore, the body diode conduction time is reduced significantly at both edges of the PWM pulse. Similar buck synchronous MOSFET drain voltage waveforms are also provided in Figure 5.10 for a load current of 20A. At 20A load, the body diode conduction times with fixed dead-time control are 14.0 and 16.1ns, while those in the proposed circuit are 2.01 and 3.94ns. It is noted that for all edges in the two examples, the body diode conduction time has been reduced by at least a factor of four times, which reduces body diode conduction loss by at least four times.

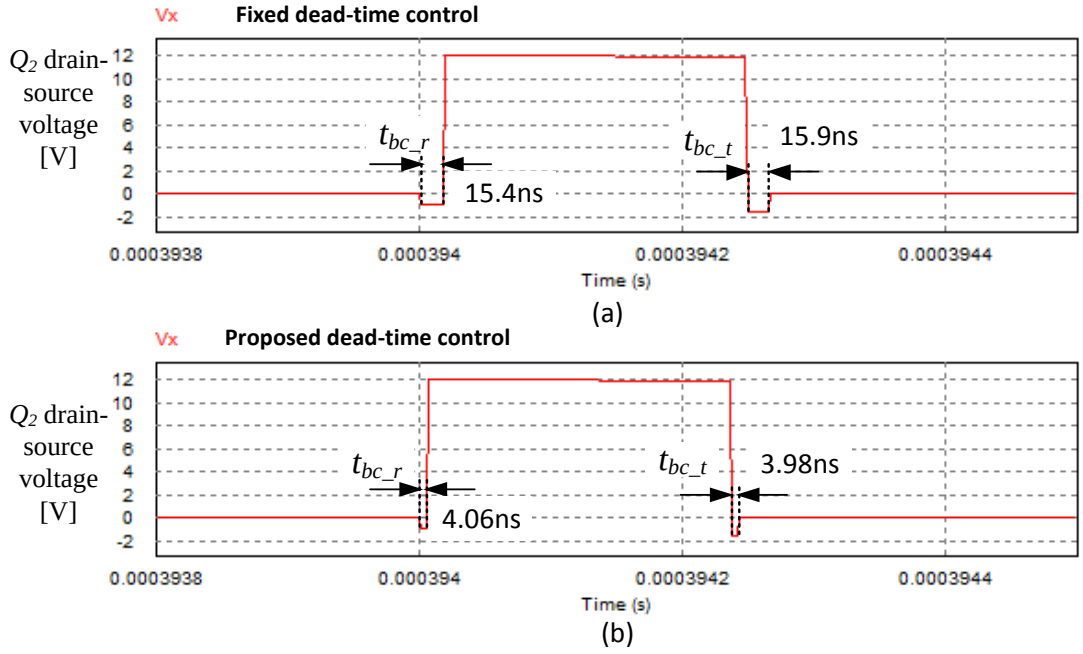

Figure 5.9 Buck synchronous MOSFET voltage at a load current of 15A (a) benchmark fixed dead-time control (b) proposed dead-time control

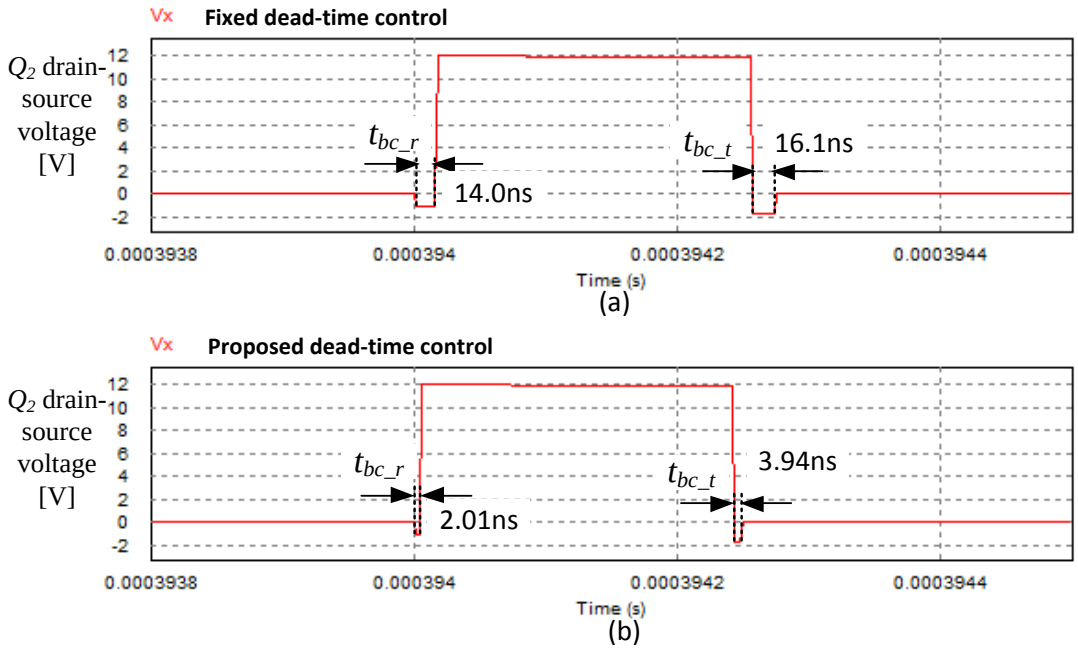

Figure 5.10 Buck synchronous MOSFET voltage at a load current of 20A (a) benchmark fixed dead-time control (b) proposed dead-time control

5.5.2 Efficiency and Loss Comparison

In this subsection an efficiency comparison is presented between the benchmark fixed dead-time controller and the proposed dead-time controller.

The purpose of reducing the body diode conduction time is to reduce the conduction loss in the device, thus improving the efficiency of the buck converter. The average input power of the buck converter over a switching cycle is given by (5.1). The input voltage can be considered as a constant, regardless of the line voltage variations. Therefore it can be taken out of the integration operator, and the input power can be expressed as the product of the DC input voltage and the average input current.

$$P_{in} = \frac{\int_t^{t+T} p_{in} d\tau}{T} = \frac{\int_t^{t+T} v_{in} i_{in} d\tau}{T} = V_{in} \frac{\int_t^{t+T} i_{in} d\tau}{T} = V_{in} I_{in\_avr} \tag{5.1}$$

The average output power over a switching cycle is given by (5.2). Since it is the square of

the output voltage is integrated, the root mean square of the output voltage is required to get the average output power. The power conversion efficiency is the ratio of the output power to the input power and is given by (5.3).

$$P_{out} = \frac{\int_t^{t+T} p_{out} d\tau}{T} = \frac{\int_t^{t+T} [(v_{out})^2 / R_L] d\tau}{T} = \frac{1}{R_L} \frac{\int_t^{t+T} (v_{out})^2 d\tau}{T} = \frac{(V_{out\_rms})^2}{R_L} \quad (5.2)$$

$$\eta = \frac{P_{in}}{P_{out}} 100 \quad (5.3)$$

The circuit presented in Figure 5.6 was simulated using PSIM9. All parameters remained unchanged except the buck converter load resistance (i.e. 80mΩ in the figure). At 10A load current, the average input current of the buck converter with the proposed dead-time controller is 1.103A, and the root mean square of the output voltage is 1.201V. As a result, the average input power, output power and efficiency of the proposed circuit at 10A load current are given by (5.4), (5.5), and (5.6) respectively.

$$P_{in} = V_{in} I_{in\_avr} = 12V * 1.103A = 13.24W \quad (5.4)$$

$$P_{out} = \frac{(V_{out\_rms})^2}{R_L} = \frac{(1.201)^2}{0.12} = 12.02W \quad (5.5)$$

$$\eta = \frac{P_{in}}{P_{out}} * 100\% = \frac{12.02}{13.24} * 100\% = 90.8\% \quad (5.6)$$

Similarly, using the benchmark circuit in Figure 5.8, the efficiency of the benchmark circuit at 10A load current is 89.2%. Therefore, an improvement of 1.6 % is achieved with the proposed dead-time control, corresponding to a power loss reduction of 0.24W, or 16.3% reduction in the total conduction losses.

Additional simulations were run for both circuits at load currents in 5A increments from 5A to 25A. The average input current and the root mean square output voltage are recorded in Table

5.1 and 5.2. The data in Table 5.1 is for the converter with the proposed dead-time controller while the data in Table 5.2 is for the benchmark circuit. Using (5.1) to (5.3), the efficiencies of the buck converter can be calculated and these results are also given in Table 5.1 and 5.2. Efficiency curves as a function of a load are provided in Figure 5.11. From Figure 5.11, it is noted that there is an improvement of more than one percentage point across the full load range with the proposed circuit in comparison to the benchmark. In order to understand the impact of this efficiency improvement the converter conduction loss must be examined.

Table 5.1 Simulated efficiency measurement data of the buck converter with proposed dead-time control circuit

Load Current I_{Load} [A]	Load Resistance R_L [Ω]	Average Input Current I_{in_avr} [A]	Root Mean Square Output Voltage V_{out_rms} [V]	Input Power P_{in} [W]	Output Power P_{out} [W]	Efficiency η [%]
5	0.24	0.542	1.201	6.51	6.01	92.3%
10	0.12	1.103	1.201	13.24	12.02	90.8%
15	0.08	1.709	1.201	20.51	18.02	87.9%
20	0.06	2.329	1.200	27.94	24.01	85.9%
25	0.048	2.984	1.200	35.81	29.98	83.7%

Table 5.2 Simulated efficiency measurement data of the benchmark circuit

Load Current I_{Load} [A]	Load Resistance R_L [Ω]	Average Input Current I_{in_avr} [A]	Root Mean Square Output Voltage V_{out_rms} [V]	Input Power P_{in} [W]	Output Power P_{out} [W]	Efficiency η [%]
5	0.24	0.550	1.201	6.60	6.01	91.1%
10	0.12	1.123	1.201	13.48	12.02	89.2%
15	0.08	1.733	1.201	20.80	18.02	86.6%
20	0.06	2.355	1.200	28.26	24.01	85.0%
25	0.048	3.037	1.200	36.45	29.98	82.2%

Converter conduction loss is the power that is dissipated by the buck converter MOSFET switches rather than the load. This loss is given by (5.7) since PSIM does not include second

order loss components, including switching loss, gate loss, and core loss.

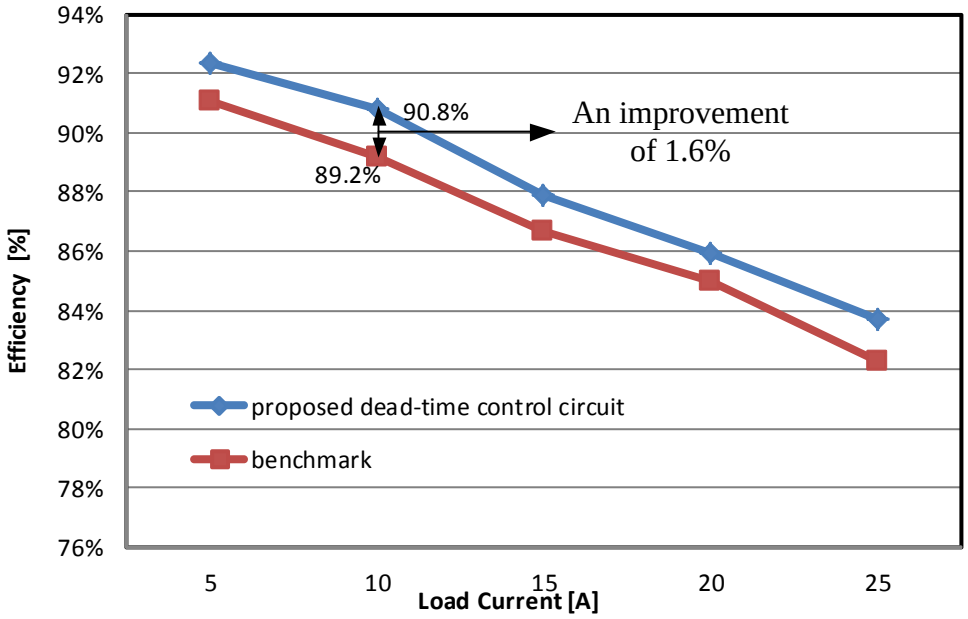

Figure 5.11 A comparison of the buck converter efficiency between the proposed circuit and the benchmark circuit at different load currents

$$P_{ls} = P_{in} - P_{out} \tag{5.7}$$

P_{ls1} is the conduction loss in the buck converter with the proposed dead-time controller, while P_{ls2} is that of the benchmark circuit. By definition, P_{ls1} and P_{ls2} values at different load currents can easily be calculated using the data provided in Table 5.1 and 5.2. The difference in conduction loss between the proposed circuit and benchmark circuit is given by (5.8)

$$\Delta P_{ls} = P_{ls2} - P_{ls1} \tag{5.8}$$

The loss reduction, expressed as a percentage relative to the benchmark converter power loss, is given by (5.9).

$$\Delta P\% = \frac{P_{ls2} - P_{ls1}}{P_{ls2}} * 100 = \frac{\Delta P_{ls}}{P_{ls2}} * 100 \tag{5.9}$$

The absolute loss reduction and loss reduction data as a function of load are provided in

Table 5.3. Observing the last column of Table 5.3, it is noted that the proposed dead-time controller can reduce the power loss of the buck converter by up to 16.3%. The loss reduction is significant since the savings represents reduced localized heating in the synchronous rectifier MOSFET, which occupies a board are of less than $1cm^2$. Reduced heat leads to increased device lifetime in addition to energy savings.

Table 5.3 Power loss reduction by the proposed circuit

Load Current I_L [A]	**Proposed circuit power loss P_{ls1} [W]**	**Benchmark circuit power loss P_{ls2} [W]**	**Loss reduction ΔP_{ls} [W]**	**Loss reduction percentage ΔP [%]**
5	0.50	0.59	0.1	15.1%
10	1.22	1.46	0.2	16.3%
15	2.49	2.78	0.3	10.5%
20	3.93	4.25	0.3	7.4%
25	5.83	6.47	0.6	9.9%

Curves representing the conduction loss in the proposed circuit and benchmark circuit are provided in Figure 5.12.

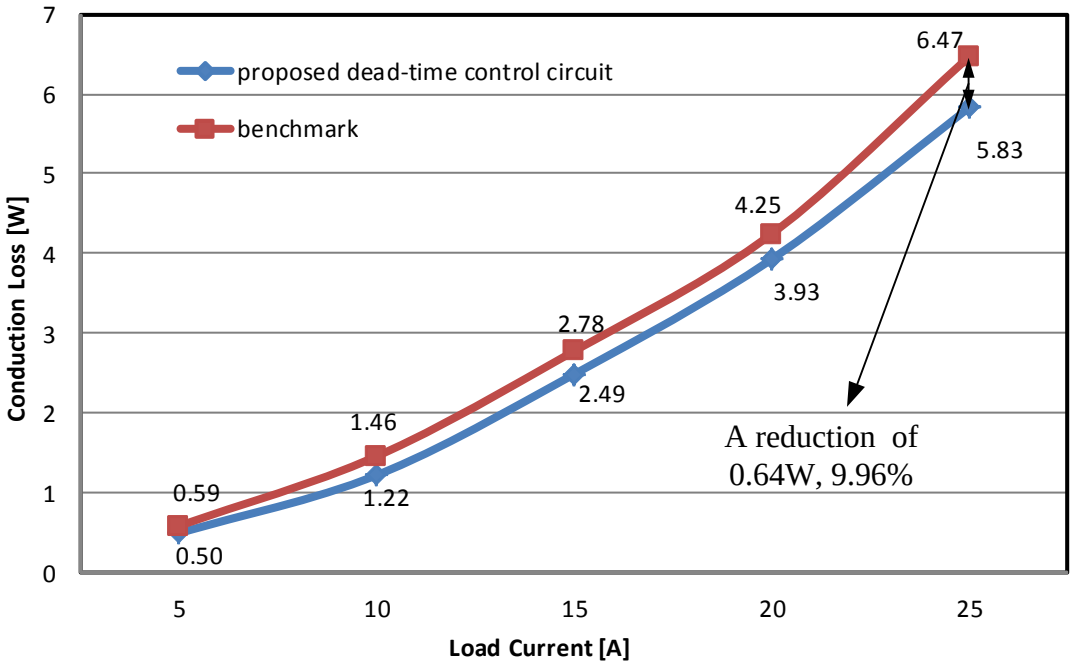

Figure 5.12 Comparison of the conduction loss in the proposed circuit and benchmark

5.6 Summary

Simulation results for the proposed dead-time control circuit were presented in this chapter. The synchronous buck converter with a current mode PWM controller is the application for the dead-time controller. A fixed dead-time benchmark circuit with 15ns dead-time was used for comparison with the proposed circuit. With the proposed analog dead-time control circuit, the body diode conduction time is minimized to under 5ns. The simulation results clearly demonstrate the reduction of the body diode conduction. The converter efficiencies resulting from the two dead-time controllers are also calculated and compared as a function of load current. In comparison to the benchmark fixed dead-time controller, the proposed dead-time controller enables an efficiency improvement of 1.6% for the synchronous buck voltage regulator. The reduction of the power loss in the buck converter is also analyzed to illustrate the significance of the improvement. The proposed buck converter reduces the total conduction losses by 16.3%.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

In Chapter 1, the synchronous buck converter and the concepts of body diode conduction and dead-time were introduced. In addition, the research motivation and objectives were established. In Chapter 2, a literature review was presented.

In Chapter 3, a novel body diode conduction detection circuit was proposed. In addition to the circuit, a signal adjustment circuit was presented, a possible silicon implementation was proposed and a design procedure, design example and simulation results were presented.

In Chapter 4, a novel dead-time optimization circuit was proposed, including signal processing circuits for body diode conduction detection and PWM signal processing. This was followed by a design procedure, design example and simulation results.

In Chapter 5, a current mode control implementation was presented in order to enable closed-loop output voltage control. Then, the proposed circuits from Chapter 3 and Chapter 4 were combined with the controller and a complete dead-time control circuit was presented for a synchronous buck voltage regulator. The new proposed circuit was then compared with a commercially available dead-time control integrated circuit model as a benchmark enabling a direct comparison of time domain, efficiency and loss results via PSIM simulation.

Notably, for the 12V to 1.2V power conversion application studied in this thesis, the proposed circuit can be projected to reduce the voltage regulator conduction loss by up to 0.64W, or 16.3% at 25A load.

6.2 Summary of Contributions

The objective of this thesis is to propose a fast and accurate dead-time control circuit that can be applied to high frequency synchronous buck converters and that can minimize the body diode conduction time of the buck converter synchronous MOSFET. Simulation results were presented to prove that the proposed circuit meets the design specifications and manages to increase the efficiency of the buck converter. The novel contributions proposed in this thesis include the following.

1) The proposed dead-time detection circuit

Integrating a detection diode on the same die as the synchronous MOSFET was proposed. With additional circuitry, the detection diode is able to provide an accurate signal of the body diode conduction time of the synchronous MOSFET. Furthermore, since the detection diode and the MOSFET are on the same die, external wires are not required, reducing parasitic components and therefore enabling the circuit to work at higher frequencies.

2) The proposed dead-time optimization circuit

A novel analog dead-time optimization circuit was proposed. Rather than a digital optimization circuit using a digital signal processor, an analog circuit eliminates one-step window dithering in steady state, which is caused by not being able to have continuous dead-time values with a digital signal processor. Furthermore, a digital controller usually optimizes the dead-time step by step in each switching cycle. While the proposed optimization circuit is able to get the optimal dead-time in one switching period. Finally the proposed analog optimization circuit can be used with other dead-time detection circuits.

3) The proposed dead-time control circuit

A dead-time control loop based on using the proposed detection and optimization circuits

was implemented and applied to a current mode controlled synchronous buck converter. One advantage of the proposed dead-time controller is accuracy. Due to the sensitive detection circuit and being able to have continuous dead-time control, the proposed dead-time controller manages to make the body diode conduction time quite small, e.g. 2ns at 20A load current. Another advantage is the potential for fast transient response since the proposed dead-time controller is a one-step predictive controller. It is able to achieve the optimal dead-time in one switching cycle.

6.3 Future Work

The following future work can be considered.

1) Hardware implementation

In this thesis, the simulation software PSIM9 was used to verify the proposed circuit. Although the simulation results prove the feasibility of the circuit and the potential for improved efficiency of the buck converter, there may be unexpected problems occurring in the real circuit, requiring modifications to the proposed circuit.

2) Additional applications

The proposed dead-time control circuit was designed for the synchronous buck converter operating at 500kHz, 12V input, and 1.2V output, which is an application broadly used in computer voltage regulators. It is worth trying to make adjustments so that the proposed dead-time control circuit can be extended to a broader range of synchronous buck converter applications.

References

[1] S. Mapus, "Predictive gate drive boosts synchronous dc/dc power converter efficiency," Texas Instruments, Dallas, Application Report, SLUA281, April 2003.

[2] J. A. Abu-Qahouq, H. Mao, H. J. Al-Atrash, and I. Batarseh, "Maximum efficiency point tracking (MEPT) method and digital dead-time control implementation," *IEEE Trans. Power Electronics*, vol. 21, no. 5, pp. 1273-1281, Sep. 2006.

[3] V. Yousefzadeh, D. Maksimovic, "Sensorless optimization of dead-times in dc-dc converters with synchronous rectifiers," *IEEE Trans. Power Electronics*, vol. 21, no. 4, pp. 994-1002, July 2006.

[4] A. Zhao, A. A. Fomani, and W. T. Ng, "One-step digital dead-time correction for dc-dc converters," in *Proc.25th Annu. The Applied Power Electronics Conference and Exposition*, pp. 132-137, Feb. 2010.

[5] W. Yan, C. Pi, W. Li, and R. Liu, "Dynamic dead-time controller for synchronous buck converters," *IEEE Electronics Letters*, vol. 46, pp. 164-165, Jan. 21, 2010.

[6] O. Trescases, W. T. Ng, and S. Chen, "Precision gate drive timing in a zero-voltage-switching dc-dc converter," in *Proc.16th Annu. International Symposium on Power Semiconductor Devices and ICs*, pp. 55-58, May 2004.

[7] A. Pizzutelli, A. Carrera, M. Ghioni, and S. Saggini, "Digital dead-time auto-tuning for maximum efficiency operation of isolated dc-dc converters," in *Proc. 38th Annu. Power Electronics Specialists Conference*, pp. 839-845, June 2007.

[8] W. Al-Hoor, J. Abu-Qahouq, L. Huang, C. Ianello, W. Mikhael, and I. Bataseh, "Multivariable adaptive efficiency optimization digital controller," in *Proc. 39th Annu. Power Electronics Specialists Conference*, pp. 4590-4596, June 2008.

[9] B. Acker, C. R. Sullivan, and S. R. Sanders, "Synchronous rectification with adaptive timing control," in *Proc. 26th Annu. Power Electronics Specialists Conference*, pp. 88-95, June 1995.

[10] A. V. Peterchev, and S. R. Sanders, "Digital loss-minimizing multi-mode synchronous buck converter control," in *Proc. 35th Annu. Power Electronics Specialists Conference*, pp. 3694-3699, June 2004.

[11] F. Lima, M. Santos, J. Barata, and J. Aguiar, "Dead-time control system for a synchronous buck dc-dc converter," in *Proc. International Conference on Power Engineering, Energy and Electrical Drives*, pp. 423-428, April 2007.

[12] *PSIM User Manual*, Powersim Inc., Woburn, MA, 2001.

[13] B. Andreycak, "The UC3823A,B and UC3825A,B enhanced generation of PWM controllers", TI Unitrode Corporation, Merrimack, NH, Application Note, 1999.

[14] *Si7866DP N-Channel 20-V (D-S) MOSFET Data Sheet*, Vishay Siliconix, Shelton, CT, Aug. 2003.

[15] *IRF6691 HEXFET Power MOSFET plus Schottky Diode Data Sheet*, International Rectifier, El Segundo, CA, Nov. 2005.

[16] *IN4148; 1N4448 High-speed Diodes Data Sheet*, Philips Semiconductors, Netherlands, Jan. 2002.

[17] *Si1555DL Complementary Low-Threshold MOSFET Pair Data Sheet*, Vishay Siliconix, Shelton, CT, May 2010.

[18] *NC7SZ04 TinyLogic UHS Inverter Data Sheet*, Fairchild Semiconductor Corporation, San Jose, CA, Feb. 1996.

[19] *LT1394 7ns, Low Power, Single Supply, Ground-Sensing Comparator Data Sheet*, Liner Technology Corporation, Milpitas, CA, 1998.

[20] *UC3842 Current-mode PWM Controller Product Specification*, Philips Semiconductors, Netherlands, Aug. 1994.

[21] *UC3842/3/4/5 Provides Low-cost Current-mode Control Application Note*, TI Unitrode Corporation, Merrimack, NH, pp. 53-66, Nov. 1998.

[22] D. W. Hart, *Introduction to Power Electronics*. Upper Saddle River, NJ: Prentice-Hall, 1997, pp. 273-277.

[23] *TPS2832 ,TPS2833 Fast Synchronous-buck MOSFET Drivers with Dead-time Control Data Sheet*, Texas Instruments Inc., Dallas, TX, Jan. 2001.

Appendix A.

E24 is one of the standard ranges set by Electronic Industries Association (EIA) with a tolerance of 5% for passive component values. The numbers in the table are the available values for each decade.

Table A.1 Preferred values for passive circuit components

E24 (5%)							
10	11	12	13	15	16	18	20
22	24	27	30	33	36	39	43
47	51	56	62	68	75	82	91