A LOW-PHASE-NOISE mm-WAVE OSCILLATOR AND ITS APPLICATION IN A LOW-POWER POLAR TRANSMITTER

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in
The Faculty of Graduate Studies
(Electrical and Computer Engineering)

The University of British Columbia
(Vancouver)
December 2011

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Abstract

Over the past decade, there have been substantial activities as well as changes in the design of high-speed radio-frequency millimeter-wave (mm-wave) integrated transceivers and their building blocks such as oscillators, mixers, low-noise amplifiers, and power amplifiers. One of the popular mm-wave frequency bands is the 7 GHz unlicensed band available around 60 GHz, which is attractive for a variety of applications including wireless local area networks (WLANs), short-range high data-rate wireless personal area networks (WPANs), and vehicular radar. One of the critical challenges in the design of 60 GHz integrated transceivers is the local oscillator signal generation. One of the main objectives of this thesis is to present and experimentally validate techniques to achieve better phase noise for high-frequency oscillators, especially for high data rate applications.

This thesis studies the phase noise performance of a new rotary-wave coupled oscillator. The presented oscillator is a traveling-wave oscillator with a reduced phase distortion. This oscillator hybridizes the standing-wave oscillator and travelling-wave oscillator to take advantage of the benefits of each structure, i.e., low phase noise and low power consumption. The structure of this circuit is based on a travelling-wave oscillator tapped with four standing-wave oscillators along a transmission line to accurately provide multiphase outputs. This oscillator produces eight phases, 45° apart from each other. A proof-of-concept prototype oscillator, fabricated in a 0.13-μm CMOS technology, provides a −17.5 dBm tone at 67 GHz and achieves a 5.2 GHz tuning range (8%) while it consumes 43.2 mW from a 1.2-V supply. The measured phase noise is −87 dBc/Hz (−102 dBc/Hz) at 1 MHz (10 MHz) offset.
As an application for this type of oscillator, a circular quadrature-amplitude modulation (QAM) small-signal polar transmitter is proposed and a proof-of-concept 16-level QAM modulator is designed and simulated. In this architecture, the proposed oscillator has been combined with an 8-to-1 multiplexer and four-level variable-gain amplifier to implement the QAM transmitter. Based on the post-layout simulation results, (which are in an excellent agreement with measured results for the oscillator block) the transmitter consumes 25% less power as compared to state-of-the-art 60-GHz transmitters with comparable performance.
Preface

I, Neda Nouri, am the first author and principle contributor of all chapters. All chapters are co-authored with Dr. Shahriar Mirabbasi, who supervised the research and provided technical consultation and editing assistance on the manuscript. Chapter 3 is also co-authored with Dr. J. F. Buckwalter, who contributed in formulating the phase noise of the rotary-wave oscillator. Furthermore, appendix material is co-authored with Dr. M. R. Nezhad-ahmadi, who helped on the design review and Dr. S. Safavi Naeini who provided editing assistance.

The following publications describe the work completed in this thesis. The second conference papers contain material that overlaps with the first journal paper.

Journal Papers Published


Conference Papers Published


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Acknowledgments

First, I would like to express my gratitude to my advisor, Dr. Shahriar Mirabbasi, whose wise direction during my Ph.D. program was a great help in finishing this project. I am indebted to him for his tireless support and incredible patience in every step of my research. His immense knowledge and great personality are an inspiration for me.

I would also like to thank Dr. James F. Buckwalter for his never-ending help and guidance in developing and refining the ideas for my dissertation. His help was invaluable. I would always keep in mind he was my first high-frequency circuit design teacher.

My former manager, Dr. Ali Fotowat-Ahmadi, was a great help during the course of my work at Unistar-micro Technology Company; his guidance about both analog circuit design and my long-term career goals have been immeasurably appreciated.

My special thanks go to Wesley d’Haene my manager at Gennum Corporation for all his support and understanding during the last year of my program. I am lucky to work under his supervision.

I would also like to express my respect and appreciation to my dear colleagues at UBC for encouraging me to reach my goals. I also would thank Roozbeh Mehrabadi for the CAD support at SOC. My special thank will go to Dr. Roberto Rosales for his help. Whenever I needed to find my answer to any test-related issue, he was there to help with his great ideas.
I thank CMC Microsystems Collaboratory for their fabrication and test support and facilities which made it possible to finish this project. Also, I am thankful for funding support from NSERC for my graduate studies.

Many special thanks go to my parents, Reza and Roghi, who have supported me throughout graduate school. I have achieved everything in my life because of their unconditional love and support. My brother, Nima, gets the special thank for showing me his strength and inspiring me to be strong and happy.
CHAPTER 1 : INTRODUCTION

1.1. Motivation

Silicon-based radio-frequency (RF) technology has had a dramatic impact on variety of wireless applications, including personal mobile communication devices, military radar systems, radio astronomy, and space programs. Based on Shannon’s theorem, one way to increase the communication data rate is to use more bandwidth [1]. In 2001, the US Federal Communication Commission (FCC) allocated a bandwidth of 7 GHz at the frequency range of 57 to 64 GHz for wireless communication [1][2]. This is an unlicensed band, meaning that the users are not required to pay for or acquire any permission to operate in this frequency band. The major advantage of the 60 GHz band over the other unlicensed bands is its wider available bandwidth that enables high data-rate transmission. Also, the high absorption by oxygen at this frequency is another benefit for high security and interference-free operation, which makes this frequency band a suitable candidate for short range high-data-rate applications.

Furthermore, operation at 60 GHz provides more advantages in terms of integration as the wavelength of the signals within this band is around 2.5 mm in silicon. This is especially beneficial for integrating the antenna on the chip. On-chip antennas offer several significant benefits, such as obviating the use of expensive and lossy packaging, transmission of higher power for a given voltage swing, simplifying the coupling to the antenna, and the possibility of using multiple antennas in a beam-forming array [3][4].
This mm-wave band has become so popular that the IEEE 802.15.3c standard group is proposing to use it for wireless personal area networks (WPANs). Such WPAN systems operate at high data-rates (>2 Gb/s) in ranges shorter than 10 m [5]. The applications mentioned in this standard cover uncompressed video streaming, office desktop data transfer and kiosk file downloading.

Since the introduction of this unlicensed band, many works have been done on the integration of the transceivers for this frequency. Early designs were implemented in technologies such as SiGe and GaAs, where faster transistors were available [6]. However, due to the lower cost and higher level of integration of CMOS designs and improved speed of operation of CMOS transistors brought the interest of many groups, both in industry and academia, to be attracted to CMOS-based designs for this frequency band [1][7]–[13]. The high level of integration makes CMOS technology a compelling choice. However, implementing mm-wave in digital processes requires extra fabrication steps [1]. To accommodate the mm-wave designs, special thicker top metal layers have been provided in CMOS technology in order to enhance the opportunities for high frequency circuit design. These layers help to improve the design of the inductors and transmission lines with higher quality factor for RF and mm-wave frequencies.

Through continued scaling of the CMOS process, unity gain frequency \( f_T \) and unity power gain frequency \( f_{max} \) of CMOS transistors are pushed beyond 100 GHz, and thus implementation of all-CMOS solutions at 60 GHz have become feasible. It should be noted that a major driving force behind CMOS technology scaling (also known as Moore’s Law) has been increasing the level of integration and cost reduction. As can be seen from the graph in
Figure 1-1, the technologies with feature size of 130nm or finer are suited for implementation of 60-GHz circuits.

Figure 1-1: The $f_T$ and $f_{max}$ trends with scaling of CMOS technology according to the ITRS [14].

At mm-wave frequencies such as 60 GHz, the size of interconnect wires become comparable to the wavelength of signals (in silicon) and it will be very important to consider the effect of wire impedance in the design. In particular, the line impedance becomes comparable with the component impedances used in the circuit. Therefore, the choice of architecture, circuit design, and the layout can immensely affect the performance of the circuit.

One way to increase the data rate in a communication link is to use more complex modulation schemes with high-order constellations; however, such schemes are less tolerant to noise. In particular the local oscillators, the key block of many designs, are required to have a tighter phase noise performance.

For many short-range applications such as WPAN and wireless universal serial bus (USB), low-power transceivers capable of delivering reasonably high data rates (over 100 Mb/s) are required [6] [15]-[17]. In such systems, phase-locked loop (PLL)-based solutions are often
favored for low-power applications, because of their hardware efficiency. For high-data-rate applications (e.g., Worldwide Interoperability for Microwave Access (WiMAX), Long Term Evolution (LTE), and Enhanced Data Rates for GSM (Global System for Mobile Communications) Evolution (GSM EDGE), spectrally efficient modulation schemes such as quadrature amplitude modulation (QAM) are widely used [18]. In QAM schemes data symbols form a constellation that is distributed in a complex plane. The commonly used QAM schemes can be classified into two classes: square QAM [19] and circular (or star) QAM [19]. Circular QAM has the property that the peak-to-average power ratio of the transmitted signal is less than that of the square QAM [20]. This means that circular (star) QAM can operate at higher transmit power in a practical radio transmitter. In general, the low phase noise oscillator is a key in the design of high-data-rate QAM systems to minimize the bit error rate of the system.

In order to further reduce the baud-rate and to increase the spectral efficiency, more bits can be encoded in one symbol using the multi-level quadrature amplitude modulation (QAM) format [21][22]. For example, in 16 QAM signaling 4 bits are encoded in each symbol and thus the spectral efficiency doubles as compared to Quadrature Phase Shift Keying (QPSK or 4-QAM). This comes, however, at the cost of reduced tolerance to signal-to-noise ratio (SNR) and phase noise. Therefore, employing a low-phase noise oscillator is important.

1.2. Thesis Objective

Having briefly described the motivation for this research, a concise thesis statement is as follows: the aim of this research is to develop a new architecture for designing mm-wave
mixer-less transmitters in CMOS technology with an emphasis on the design and experimental validation of a low-phase-noise, low-power, multi-phase rotary-wave oscillator structure.

In particular, the following contributions are made:

1) Design of a multi-phase low-phase-noise rotary-wave oscillator that uses a hybridized structure based on a travelling-wave oscillator (TWO) and a standing-wave oscillator (SWO) to provide low phase noise outputs (shown in Figure 1-2). (Chapter 3)

The structure is suitable for generating the multi phases required in high data rate applications (for example, in the 16-QAM structure discussed in the thesis, eight different phases, 45° apart, are used). Once a wave becomes established, it takes a small amount of energy to sustain it. This is because unlike a ring oscillator, the energy that goes into charging and discharging MOS gate capacitances is re-circulated in the closed electromagnetic paths. This offers potential power savings as losses are not related to $CV^2f$ but rather to $I^2R$ dissipation in the conductors where R can be reduced, e.g., by adoption of
copper metallization. The travelling-wave oscillator is tapped with standing-wave oscillators (which conventionally use back-to-back inverters). Also, this architecture is very promising for low-phase-noise systems, as any noise perturbation will be averaged out along the transmission-line ring and will result in a lower phase noise.

2) Development of small-signal polar transmitter architecture (shown in Figure 1-3) for high-data-rate wireless communications: The mixer-less structure has been chosen to avoid/minimize the problems associated with the mixer feed-through and in-phase/quadrature (I/Q) mismatch. As a proof of concept a 16-QAM transmitter is designed and fabricated. The rotary-wave oscillator is employed to provide both low power and low phase noise outputs. An 8-to-1 multiplexer along with two variable gain amplifiers (VGAs) is used to provide four different levels of gain to achieve the 16-QAM constellation (Chapter 4).

![Small-Signal Mixer-Less Polar Transmitter Architecture](image)

Figure 1-3: A small-signal mixer-less polar transmitter architecture.

A combination of a multiplexer and a current-steering variable-gain amplifier (VGA) is used to save area and provides the levels of amplification required for 16-QAM constellations. Typically, the distance between the rings is chosen to reduce the error vector magnitude (EVM) to within an acceptable range for the standard used. This multiplexer uses less
transistors as compared to the conventional one [4], which in turn means less noise will be added to the output.

To the best of the author’s knowledge, the approach of combining standing- and rotary- wave oscillators to make multiple phases for making QAM transmitters has not been used before although there is still considerable room for improvement as will be discussed in the future work section. Also the phase noise of the conventional rotary-wave oscillator has been analyzed, but the phase noise of the proposed hybrid RWO/SWO has not been previously analyzed.

1.3. Thesis Organization

Chapter 2 overviews different polar transmitter topologies and provides a literature review of recent high-frequency transmitter designs. In particular, a mixer-less architecture is considered. In addition, a brief overview of the shortcomings and strengths of these designs is provided.

Chapter 3 provides a detailed explanation of different types of oscillators and phase-noise calculation methods and then presents the structure of the proposed rotary-wave oscillator. Also, a comprehensive analysis of the phase noise of this type of oscillator is provided.

In Chapter 4, the design of the combined multiplexer and VGA is described in detail. First, different structures of variable-gain amplifiers are compared, and then the design of both the multiplexer and VGA is discussed, which are building blocks of any transmitter.

Chapter 5 presents the measurement results of two fabricated chips. The first chip has been fabricated in a 0.13-μm BiCMOS technology and includes the oscillator and the 8-to-1
multiplexer to test the oscillator. The second chip is fabricated in a 0.13-\textmu m CMOS technology and includes the main building blocks of the transmitter. Chapter 6 presents concluding remarks and directions for future work.
CHAPTER 2 : BACKGROUND

2.1. Overview

This chapter provides the background and an overview of different transmitter architectures and a literature review of previously designed high-data-rate transmitters. Section 2.2 reviews the basic concept of the transmitter design. Section 2.3 discusses the modulation methods. In Section 2.4, different structures of polar transmitters are reviewed.

2.2. Transmitter Architectures

Wireless transmitter architectures can be broadly divided into two groups: mixer-based and phased-locked loop (PLL)-based transmitters. PLL-based transmitters which are typically mixer-less are often favored for low-power applications and multi-mode operations. Mixer-based structures can be further categorized into direct-conversion and two-step conversion transmitters [23]. If the transmitted carrier frequency is equal to the local oscillator frequency, the transmitter architecture is called direct-conversion or homodyne architecture. On the other hand, if the baseband signal is up-converted in two steps, the transmitter architecture is called a two-step or heterodyne architecture.

In direct conversion, the signal is directly transferred to the desired frequency. This method seemingly needs less complex circuitry and is more suitable for integration. However, it has two main problems, disturbance of transmit local oscillator, and local oscillator (LO) pulling [23]. The two-step transmitter is the approach to alleviate the LO pulling issue, by making the PA output frequency far from the frequency of the VCOs.
2.2.1. Direct-Conversion Architecture

Figure 2-1 shows the architecture of a direct-conversion transmitter. In this type of transmitter, in-phase data, $I_{in}$, and quadrature data, $Q_{in}$, are up-converted using orthogonal (quadrature) LO signals. The quadrature signals are then added and amplified. The RF signal (the input of the VGA) can be described using its baseband components, $I(t)$ and $Q(t)$, as follows:

$$V(t) = I(t) \cos(\omega_o t) + Q(t) \sin(\omega_o t)$$  \hspace{1cm} (2-1)

where $\omega_o$ is the RF carrier frequency.

As mentioned before, the two major design challenges in a direct conversion transmitter (Figure 2-1) are disturbance of transmit local oscillator by the power amplifier and LO pulling. Because of the high power spectrum centered around the LO signal, its noisy output can corrupt the oscillator spectrum. The LO pulling phenomena can be alleviated by moving the PA spectrum sufficiently far from the LO spectrum.
The other issue that can be caused by the mixer is the LO feedthrough. The LO signal can directly feed to the output IF signal. The leakage can be minimized with careful design and layout of the mixers and quadrature local oscillator. Also, some calibration can be done on LO leakage through adding the proper amount of DC offset to either of $I$ or $Q$ signals. This technique is discussed by Cavers et al. [24] and is now commonly used in Cartesian transmitter design. Due to the above-mentioned problems, the design of direct-conversion transmitters is challenging.

2.2.2. Polar Transmitter Architecture

In contrast with the Cartesian-based architectures such as the direct conversion structure, polar modulation techniques use magnitude and phase. Thus, they make it possible to process the two components (phase and magnitude) differently and more efficiently. As shown in Figure 2-2, the RF signal can be decomposed into polar form using the amplitude and phase of the RF carrier. With a polar representation, the modulated RF signal at the VGA input can be written as:

$$V(t) = a(t)[\cos(\omega_t t) + \varphi(t)],$$  \hspace{1cm} (2-2)

where $a(t)$ and $\varphi(t)$ are the amplitude and phase of the carrier, respectively [25]. The phase component, i.e., phase modulation (PM) is processed using the PLL while the amplitude component, i.e., amplitude modulation (AM) is processed by the variable-gain amplifier (VGA). Efficient amplifiers can be used to amplify the signal at the PLL output, as it has a constant envelope (as opposed to variable envelope of the RF signal at the input of the VGA in Figure 2-1). This will reduce the power consumption of the transmitter.
Mapping the complex signal into its phase and amplitude components is a nonlinear and complicated process. Furthermore, it is not uncommon for the phase and amplitude signals to abruptly change directions, which means there is a need to widen the spectrum of the modulation. Polar transmitters can be categorized as: (1) small-signal polar transmitter: as shown in Figure 2-2(a), the AM and PM signals combine and are then transferred to the PA; (2) direct polar transmitter: it works by combining the AM and PM modulated signals at the high-power PA (shown in Figure 2-2(b)).

2.2.3. Phase and Amplitude Modulations

A detailed view of a PLL supporting phase modulation is shown in Figure 2-2(a). The feedback is applied to minimize the phase difference between the reference and the VCO output signal. The required phase is selected in the phase-select block and the output of the PLL is amplified by the variable-gain amplifier to provide the required amplitude for the
selected phase. The phase modulation is implemented by the PLL. In order to operate properly, the phase modulation signal must first be differentiated, because the control input to the VCO adjusts the output frequency, not the phase. This can be done by measuring the difference between consecutive PM samples.

An ideal polar modulator combines the amplitude and phase components to construct the desired complex transmit signal, which necessitates proper alignment of these two components. Any timing offset causes excess EVM. EVM will be described in more detail in the next subsection. In practice, the required accuracy depends on the data rate of the baseband transmit signal. Any group delay caused by filtering should be compensated for or removed.

2.3. Complex Modulations

Digital modulation schemes encode data in symbols which can be considered as vectors with unique amplitude and phase. Each symbol can represent multiple bits of digital information, where more complex constellations represent more bits per symbol. In Figure 2-3(a), binary phase shift keying (BPSK) involves changing the phase of the carrier between two points that are 180° out of phase. In BPSK, only 1 bit is represented for each symbol. To improve the spectral efficiency, it is better to send multiple bits (for example, a pair or four bits) instead of one bit and represent them with different levels. For sending two bits, $b_m$ and $b_{m+1}$, with one symbol, they can be represented as:

$$x(t) = b_m a_e \cos \omega_c t - b_{m+1} a_e \sin \omega_c t$$  \hspace{1cm} (2-3)

Higher order modulation formats have more points in the symbol constellation. Figure 2-3(b) shows the constellation for a 4-QAM signal. This allows two bits to be encoded on each
symbol, increasing the data rate by a factor of 2 as compared to BPSK. Figure 2-3(c) shows a 16-QAM constellation which uses 4 bits per symbol. Higher order QAM schemes allow higher data transmission rates for a given symbol rate. This results in higher spectral efficiency, or higher data-rate for a given amount of available spectrum [26].

![Figure 2-3: Symbol constellations for different numbers of bits/symbol.](image)

However, given a fixed transmit power, by increasing the number of levels of amplitude and phase modulation, the distance between symbols and thus the symbol detection becomes more sensitive to noise. Constant envelope modulation schemes generally have to use lower symbol rates to keep the output spectrum within limits [26][27].

In practical systems, the transmitted symbol vectors suffer from noise and distortion. This noise and distortion causes an error between the ideal and actual symbol location which can be shown by an error vector. A common figure of merit for reliability of the symbol constellation is the error-vector magnitude (Figure 2-4). The EVM is calculated as a normalized average power of the error vector between the ideal and actual transmitted signal constellation points. Mathematically, EVM is typically defined as the root-mean-square quantity across a number of symbol measurements:
$$EVM = \frac{\sqrt{\frac{1}{N} \sum_{j=1}^{N} (V_e^2)}}{|V_m|}$$  

(2-4)

where $V_e$ is the magnitude of the error vector for each symbol, $V_m$ is the magnitude of the desired symbol vector, and $N$ is the number of measurements.

The requirements for the maximum allowable EVM level used by the communication system. Specific requirements for the EVM of different MCSs considered in this work and the EVM measurement procedure are taken in accordance with the IEEE 802.11a standard [28]. The EVM requirements for the analyzed MCSs are listed in Table 2-1. The peak value for EVM may also be specified in the standard. EVM requirements vary widely depending on the standard [27].

<table>
<thead>
<tr>
<th>Relative constellation error (dB)</th>
<th>Modulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>-5, -8</td>
<td>BPSK</td>
</tr>
<tr>
<td>-10, -13</td>
<td>QPSK</td>
</tr>
<tr>
<td>-16, -19</td>
<td>16-QAM</td>
</tr>
</tbody>
</table>

Figure 2-4: Error vector is the difference between the actual and ideal symbol vectors.
If the EVM is measured over large values of $N$ [29], then:

\[
EVM = \sqrt{\frac{N_o}{E_o}} = \sqrt{\frac{1}{SNR}}
\]  

(2-5)

where $E_o/N_o$ and SNR are representing the energy per bit to noise power spectral density ratio, and normalized signal-to-noise ratio, respectively. These parameters offer a good representation of the polar transmitter performance.

Noise leads to random distribution of the error vectors, while distortion may cause patterns in the error vector that are correlated with the symbol amplitude and phase. In transmitters it is common to specify AM-AM (amplitude-driven amplitude) distortion and AM-PM (amplitude-driven phase) distortion [30]. AM-AM distortion is caused by variation in the transmitter gain as the signal amplitude changes. A common form of AM-AM distortion is quantified through the -1 dB compression point in RF amplifiers [27][30]. Compression happens due to the nonlinearity of the system, when the output amplitude is saturated and is not linearly proportional to the input amplitude.

In contrast to Cartesian transmitters where the data is encoded in Cartesian $I$ and $Q$ signal components, in polar transmitters the data is encoded in the amplitude and phase components of the signal. The polar representation can be calculated from the Cartesian representation as:

\[
a(t) = \sqrt{I(t)^2 + Q(t)^2}
\]  

(2-6)
\[
\varphi(t) = \arctan\left(\frac{Q(t)}{I(t)}\right)
\]  

(2-7)

where \(a(t)\) and \(\varphi(t)\) are the time-domain amplitude and phase of the polar signal. A major difference between the polar and Cartesian representations is that the polar basis vectors, amplitude and phase, have different spectral properties as compared to the \(I\) and \(Q\) basis vectors. This can be seen from (2-6) and (2-7) as \(a\) and \(\varphi\) are derived from \(I\) and \(Q\) through nonlinear operations. Non-linearities in (2-6) and (2-7) cause the polar basis vectors to have a wider bandwidth as compared to the Cartesian \(I\) and \(Q\) components. To design the system with low EVM and high spectral reliability, the wider-band nature of the amplitude and phase paths should be considered at both the architecture and circuit level design steps.

2.4. Polar Transmitter Implementation

There are several techniques that have been used to design a polar transmitter. The Kahn envelope elimination and restoration (EER) technique is an early example of polar modulation where the amplitude and phase are extracted directly from the modulated RF signal [31].

In the Kahn technique, shown in Figure 2-5, a limiter keeps the zero crossings of the RF signal intact (preserving the phase information), while converting the signal (which is applied to the input of the PA), to a constant envelope signal. The amplitude information is extracted with an envelope detector and then restored in the envelope of the transmitted signal, leading to the EER implementation. A more recent example of this technique is presented by Raab et al. [32]. The Kahn technique continues to be the basis of many of the modern polar transmitter structures [31][33]-[37].
Figure 2-5: The Kahn envelope elimination and restoration (EER) transmitter architecture [31].

There are many ways to implement the phase path in a polar system. As shown in Figure 2-5, the goal is to convert an RF signal representation of the baseband phase signal to a phase-modulated RF signal. The work of Staszewski in 2005 [38], opens the range of possibilities for such techniques. They show another version of the polar architecture highlighting the wide variety of such systems close to Figure 2-5. The PA is used as a variable-gain amplifier (VGA). In a general sense, any signal which modulates the amplitude of the carrier can effectively be used in a polar system.

Polar transmitters provide the potential for efficient implementation of multimode wireless transmitters. They provide a single architecture for different systems that eliminate RF mixers and their associated spurious and leakage problems. Also, due to amplifying a constant envelope signal, as compared to their Cartesian counterparts, they have better efficiency, leading to higher output power capability. However, their wider spectra and tighter accuracy requirements place greater demands on phase and amplitude modulation. The challenges in the design of polar transmitters can be summarized as follows:

(1) These types of transmitter usually require wider band signal components (i.e., polar amplitude and phase signals). A Cartesian representation with a simple band-limited
spectrum may have wider band spectral content with an equivalent polar representation. The wideband nature of the polar representation requires higher bandwidth circuit design for the amplitude and phase modulators.

(2) Another major issue for polar systems is distortion. In Cartesian transmitters, the PA operates with a fixed supply voltage and is only subject to the normal input-output nonlinear characteristics.

At low supply voltages, additional AM-PM distortion may be caused by the feed-through of the PA input signal to the output, which is problematic if the phase-path signal is a constant envelope [31]. The phase signal can also leak directly to the output of the PA or indirectly through the parasitic capacitors [25].

2.5. Summary

Two major transmitter architectures and their advantages and disadvantages have been explained. The polar transmitter requires an accurate phase generation, which reduces the phase distortion and increases the accuracy of the system design. Accurate phase generation at mm-wave frequencies is challenging and one objective of this thesis is to design a class of mm-wave oscillators that generate multiple phases and have low phase noise (Figure 1-3). In Chapter 3, the design and analysis of the multi-phase oscillators is explained in detail.
CHAPTER 3 : ANALYSIS AND DESIGN OF ROTARY-WAVE OSCILLATORS

Even though oscillators have been extensively used over the past decades, high-performance oscillators operating in the mm-wave range continue to pose various design challenges in today’s advanced technologies [1]. In this chapter, the discussion begins with oscillator fundamentals, and then continues by comparing different types of oscillators, and then the proposed new architecture for the rotary-wave oscillator is introduced. Also a comprehensive analysis of the phase noise of the proposed oscillator is presented.

3.1. Oscillator Fundamentals

The local oscillator (LO) circuit is responsible for creating the internal oscillatory signals required in the transceiver which have a critical impact on the performance of the entire system. In most wireless applications, narrow-band channels reside close to each other, and even a slight non-linearity in the LO could cause significant distortion from adjacent channels [23] and enforce stringent requirement on the phase noise (PN) of the oscillators [39]. In addition to phase noise, there are application-specific requirements for the oscillator such as the oscillation frequency, output power, and frequency tuning range (e.g., 7 GHz for 60 GHz applications) that must be met.

Voltage-controlled oscillators (VCOs) are one of the main building blocks of LOs. In addition to the design issues mentioned above, capacitive loading on the oscillator output, which degrades the tuning range and phase noise, and passive component (e.g., inductors) losses become predominantly important in the microwave regime.
Oscillation behavior can be explained with the well-known feedback model shown in Fig. 3-1(a), where an amplifier $a(j\omega)$ is placed in a feedback loop with a feedback gain of $\beta(j\omega)$. The overall transfer function is given by

$$H(j\omega) = \frac{V_{\text{out}}(j\omega)}{V_{\text{in}}(j\omega)} = \frac{a(j\omega)}{1 - \beta(j\omega)a(j\omega)} \quad (3-1)$$

To make the structure oscillate at a certain frequency, $\omega_0$, the Barkhausen criterion should be satisfied:

$$a(j\omega)\beta(j\omega) = 1 \quad (3-2)$$

That is, at the oscillation frequency, $\omega_0$, the magnitude of the loop gain is unity and the total phase shift around the loop is 0° (or a multiple of 360°).

Typically, oscillation initiates from noise or an input waveform with sufficient spectral content. In practice, the loop gain has to be greater than one in the beginning to start up the oscillation. Once the oscillation is started typically the loop gain drops to one. For a microwave circuit, a closed loop gain function (Eq.(3-1)), can be developed as follows. Fig.
3-1(b) shows the one-port model a generic oscillator; a simple tank with the impedance of \(Z_L\), and the active block which is responsible to generate negative impedance with the total impedance of \(Z_m\) to cancel out the loss of the tank.

The resonator alone cannot sustain oscillation since part of the energy stored in the tank at every cycle is dissipated in the parasitic resistor of the tank. By using the active device, the energy loss is replenished in every cycle so that stable oscillation occurs.

3.2. Different Types of Oscillators

There are different classifications for oscillators. One common classification is to categorize oscillators into three types: ring oscillators, LC oscillators, and distributed oscillators.

3.2.1. Ring Oscillators

This type of oscillator, composed of several gain stages in a single feedback loop, is usually referred to as “resonator-less” oscillator. In most digital and analog applications, ring oscillators are used to generate the internal clock of the system. However, ring oscillators suffer from a relatively large phase noise which prohibits their use in applications with stringent phase noise requirement [40][41], especially, in wireless applications where many neighboring channels reside just a few kHz apart from each other. The advantage of this type of oscillator is its simplicity and wide tuning range. As shown in Fig. 3-2, a ring of inverters make a ring oscillator.

![Fig. 3-2: Ring oscillator.](image-url)
Total phase shift around the loop at the frequency of oscillation should be equal to 360° (or integer multiples of 360°). Assume $N$ inverter stages each with phase shift of $\Delta \phi$ are connected to each other. Then $\Delta \phi$ can be calculated using:

$$2N\Delta \phi = 360^\circ \Rightarrow \Delta \phi = \frac{180^\circ}{N}$$

(3-3)

Ring oscillators are area-efficient structures that provide a wide tuning range for multi-phase outputs; however, they have a poor phase noise which is one of the major parameters to choose an oscillator structure especially for high frequencies.

3.2.2. LC Oscillators

LC-tank oscillators are typically used in high-speed low-phase-noise systems. A simple yet symmetric configuration facilitates high-speed and differential design with a large output swing, reasonable tuning range, and low power consumption. It also allows for low-supply operation. One of the commonly used LC oscillator structures is the cross-coupled oscillator. Depending on the inductor quality factor ($Q$), cross-coupled oscillators can achieve low phase.

A typical realization of a cross-coupled oscillator is shown in Fig. 3-3, where the pair $M_1$-$M_2$ provides negative resistance $-2/g_{m1,2}$ (differentially) to compensate for the inductor loss $R_p$, where $g_m$ is the transconductance of each transistor. At resonance, these two resistances cancel each other and the oscillation frequency is given by

$$\omega_o = \frac{1}{\sqrt{L_p C_p}}$$

(3-4)
where $L_p$ and $C_p$ denote the loading inductor and parasitic capacitance at output nodes, respectively, and D is (MOS) varactor that makes the oscillator tunable, i.e., a voltage-controlled oscillator (VCO). Barkhausen criteria imply that if $R_p g_{m_{1,2}} \geq 1$ then the circuit oscillates, while in a practical design a higher than unity value ($\approx 3$) is used to ensure oscillation over process, supply voltage, and temperature (PVT) variations.

It is instructive to derive an alternative expression for oscillation frequency, $\omega_o$, with simplified conditions to examine what factors limit the operation frequency. The relation between $R_p$ and $\omega_o$ in stable oscillation can be represented as

$$R_p = Q \omega_o L = \frac{1}{g_{m_{1,2}}} \quad (3-5)$$
\[ \omega_o = \frac{1}{\sqrt{L(C_p + C_{gs})}} \]  

(3-6)

where \( Q \) represents the quality factor of the tank, and \( C_{gs} \) the average gate-source capacitance contributed by \( M_{1,2} \) (For simplicity, the varactor is ignored).

In practice, high-speed oscillation presents many challenges: (1) the on-chip inductors usually have a self-resonance frequency of a few tens of GHz; (2) due to the physical limitations for on-chip inductors, they cannot provide a high \( Q \); (3) the varactors present a low quality factor which can degrade the overall \( Q \) of the tank; (4) in high frequencies, \( C_p \) is comparable with other parasitics. One solution for improving the \( Q \) of the tank, i.e., decreasing the tank loss at high frequencies, is to use transmission lines instead of inductors as the \( Q \) of transmission lines is higher than that of inductors.

An approach to reduce the noise contribution of the tail current source is illustrated in Fig. 3-3. A large bypass capacitor \( C_f \) absorbs the noise of the current source. With the \( L_f - C_{par} \) network resonating at twice the output frequency, at the oscillation frequency the common-source node P still experiences high impedance to ground. The differential operation improves the common-mode rejection.

To extend the tuning range of such LC oscillators a popular techniques is to use a capacitor array (preferably binary-weighted for better efficiency) to coarsely tune the VCO frequency (Fig. 3-4) [42]. As shown in Fig. 3-4, by using \( 2N \) control switches, a wide range of frequencies can be covered. It should be noted that the poor quality factor of the varactors still degrades the phase noise of the oscillator.
Another important VCO topology that has been widely used in high-speed systems is Colpitts oscillator. First proposed in 1920’s [43], this type of oscillator could operate with only one transistor. Because of the better performance of the differential circuits at high-speed operation, a symmetric Colpitts oscillator with differential output is usually used [23]. A Colpitts oscillator uses a capacitive feedback from drain to source (Fig. 3-5(a)) and its oscillation criteria is $R_p g_m \geq 4$, where $g_m$ is the transconductance of NMOS transistor and $R_p$ is the equivalent parallel resistance seen at the drain of the transistor including the non-idealities of inductors and capacitors.

![Fig. 3-5: (a) Colpitts oscillator, (b) its linear model [23].](image)
Looking from a different perspective, the Colpitts circuit can be considered as a negative resistance in parallel with an LC tank, Fig. 3-5(b) (if the bottom plate of $C_2$ is considered connected to the gate of the NMOS device (AC ground)). In order to oscillate, the signal in the feedback path through the $C_1$-$L$-$C_2$ network must satisfy Barkhausen criterion. By applying this criterion on the oscillator open loop, the oscillation frequency can be calculated as

$$\omega_o = \left(1 + \frac{1}{Q^2} \right) \sqrt{\frac{1}{LC_2}} \sqrt{\frac{1}{C_1} + \frac{1}{C_2}}$$

(3-7)

Here, $Q$ is the quality factor of the inductor. In Fig. 3-5(b), $R_p = \omega_o L Q$. Due to using only one transistor in this architecture, it exhibits good phase noise performance. Comparing Colpitts and cross-coupled oscillators, cross-coupled oscillators can provide a lower power consumption and wider tuning range (as Colpitts oscillators have a fixed capacitor as part of their structure).

3.2.3. Transmission-Line

One of main components of the distributed oscillators is transmission line. A brief introduction of its basic parameters is presented as follow.

Fig. 3-6: Lumped transmission-line model with distributed transconductors.
The equivalent lumped model for a transmission line is shown in Fig. 3-6, where $R$, $L_o$, $C_o$, and $G$ are the lumped transmission-line parameters per unit length. The effective interconnect propagation constant, $\gamma$ can be calculated by

$$\gamma = \sqrt{(R + j \omega L_o)(G + j \alpha C_o)} = \alpha + j \beta$$  

(3-8)

The propagation constant consists of the loss constant, $\alpha$, and phase constant, $\beta$, as shown in (3-8). Assuming low-loss for the values of the transmission-line parameters, the equations for $\alpha$ and $\beta$ can be simplified to

$$\alpha \approx \frac{R}{2} \sqrt{ \frac{C_o}{L_o} } + \frac{G}{2} \sqrt{ \frac{L_o}{C_o} } \approx \frac{R}{2Z_o} + \frac{GZ_o}{2}$$  

(3-9)

$$\beta \approx \omega \sqrt{ L_o C_o }$$  

(3-10)

where $Z_o$ is the characteristic impedance of interconnect and can be approximated as $\sqrt{L_o/C_o}$. These equations provide some intuition about how $\alpha$ and $\beta$ change as a function of transmission-line parameters. Any other losses added to the transmission line can be modeled as a series resistance or a parallel conductance.

### 3.2.4. Distributed Oscillators

A distributed amplifier (Fig. 3-7(a)) can be placed in a feedback loop to form an oscillator (Fig. 3-8) [44]. The input signal propagates down the “gate” line and is amplified by the distributed devices. The outputs of the devices add coherently on the “drain” line. Because the capacitance of the active devices is absorbed into transmission lines, distributed amplifiers are
capable of providing a gain that exceeds the transmission line loss [41]. They are also well-suited for integration in standard CMOS processes [45].

This approach shows some promise for overcoming interconnect losses at microwave frequencies. Instead of using a single transistor to provide negative resistance, it is preferable to distribute the negative resistance along the input and output lines to reduce gain limitations imposed by the transmission line (t-line) loss. Back-to-back inverters (Fig. 3-7 (b)) have been used [46] to provide the negative resistance. A better approach is to use cross-coupled NMOS transistors (Fig. 3-7 (c)) instead of back-to-back inverters that work up to very high frequencies. This approach allows tuning of the negative resistance through controlling the current source. As shown in Fig. 3-8, the output of a distributed amplifier is returned back to the input, yielding to wave circulation along the loop (a distributed oscillator).

**Fig. 3-7:** (a) Distributed amplifier, (b) negative resistance circuits: back-to-back inverters, (c) cross-coupled pair with current source.

**Fig. 3-8:** Distributed oscillator.
To insure the oscillation, the total delay of the inverting amplifier must translate to a phase shift of 180° at the frequency of interest. As mentioned before, to assure the oscillation, a minimum loop gain of unity is required, and the oscillation frequency can be calculated [47]. The transistor capacitance lowers the characteristic impedance and not translating to a time constant. Each common-source stage along with an additional length of t-lines increases the gain by $g_m Z_{l}/2$, by assuming that the transmission line is loss-less. Assuming the $n$ common-source stages uniformly distributed over a t-line with a length of $\ell$. The characteristic impedance of the amplifier will be

$$Z_{oL} = \sqrt{\frac{L_o}{C_o + \frac{nC_{gs}}{\ell}}}$$  \hspace{1cm} (3-11)

The total voltage gain is equal to

$$A_v = \frac{ng_m Z_{oL}}{2} = \frac{ng_m}{2} \sqrt{\frac{L_o}{C_o + \frac{nC_{gs}}{\ell}}}$$  \hspace{1cm} (3-12)

As $f_T$ can be calculated from:

$$2\pi f_T = \frac{g_m}{C_{gs}}$$  \hspace{1cm} (3-13)

By replacing (3-13) in (3-12):
By considering that $C_o$ is negligible as compared to $\frac{nC_{gs}}{\ell}$, $A_v$ can be summarized as follow:

$$A_v = \frac{\ell}{2\pi f_T}$$  \hspace{1cm} (3-15)

Therefore, the $A_v$ can be written as:

$$A_v = \frac{\pi f_T}{2f_o}$$  \hspace{1cm} (3-16)

By assuming that the $A_v$ should be equal to one for oscillation

$$A_v = 1 \Rightarrow f_o = \frac{\pi}{2} f_T$$  \hspace{1cm} (3-17)

Oscillation is therefore obtained at any point along the transmission line. Here, the transmission line loss is overcome by the gain generated along the line. It is more specific to assume that the two propagation lines in Fig. 3-8 are identical in the characteristic impedances, group velocities, and physical length. The oscillation period under such circumstances is twice the propagation time along the length $\ell$: 
\[ f_o = \frac{1}{2L_o \left( C_o + \frac{nC_{gs}}{\ell} \right)} \]  

(3-18)

It can be shown that the oscillation frequency is more than the device \( f_T \) [47]. While looking attractive, the distributed oscillators suffer from a number of drawbacks: (1) the group velocities along the two lines may depart from each other due to the difference between the gate and drain capacitances; (2) the circuit needs larger area, and (3) the frequency tuning could be difficult. The third point becomes clear if adding any varactor to the lines can cause significant degradation on the oscillation frequency and the effective quality factor \( Q \). Varying the bias voltage of the transistors may change the intrinsic parasitics (and therefore the oscillation frequency), but the imbalanced swing and the mismatch between the lines could make things worse.

It has been shown that the phase of an electrical standing-wave – one of the important aspect for clock distribution – is determined almost entirely by the transmission line loss and termination [48]. A standing-wave is a superposition of two traveling waves of equal magnitude and frequency that are propagating in opposite directions. Fig. 3-9 shows how a standing wave is generated and expressed by

\[ V(z, t) = A \cos(\omega t - \beta z) + A \cos(\omega t + \beta z + \theta) = 2A \cos\left(\beta z + \frac{\theta}{2}\right) \cos\left(\omega t + \frac{\theta}{2}\right) \]  

(3-19)

where \( \theta, A, \) and \( z \) are the phase relationship between the two traveling waves, the signal amplitude, and the distance of the wave travelled with reference to the wave origin, respectively. Eq. (3-19) shows that the magnitude of a standing-wave varies with position but
the phase is constant. Standing-waves contain magnitude values whose positions are determined by $\theta$. The polarity of the wave changes at zero (on the other word, it is viewed as a discrete $180^\circ$ phase change). Thus, a standing-wave can be generated by reflecting the incident wave back to the source and by superimposing the two incident and reflected waves.

![Standing Wave Diagram](image)

**Fig. 3-9: A standing-wave formed from a right-travelling-wave (+z) and a left-travelling-wave (-z).**

### 3.2.5. Millimeter-Wave Oscillators

Microwave oscillators with transmission-line-based tanks fall into two categories: standing-wave oscillators (SWO) and rotary-wave oscillators (RWOs). Trade-offs between implementing each type of such oscillators depends on the design requirements. The SWO tends to minimize phase noise by appropriately tailoring the tank impedance for low loss based on the maximum current and voltage along the tank. On the other hand, the RWOs have been suggested to distribute negative resistance around a differential transmission line ring and provide multiple low phase-noise phases. In this research, a hybridized version of RWO and SWO has been used.
3.2.5.1. Standing-Wave Oscillators

Based on the discussion of standing-waves, the main limiting factor for generating ideal standing-waves is the lossy interconnects which can be compensated by using distributed gain circuits across the transmission line. The circuit (shown in Fig. 3-10) is a standing-wave oscillator composed of a tank (the resonator has made of lossy transmission lines) and gain stages (distributed negative transconductors \( g_d \)) similar to all conventional RF oscillators) to overcome the loss of interconnects.

![Interconnect with distributed transconductors.](image)

Assuming differential operation, the resonator has a virtual ground at both ends. The unloaded \( Q \) of the resonator can be calculated based on the interconnect properties by [49],

\[
Q = \frac{\beta}{2\alpha} \tag{3-20}
\]

To guarantee oscillation, the total transconductance gains should be equal to the interconnect loss. The oscillation frequency is determined by the resonant frequency of the resonator including the loading made by transconductances to make the effective loss to zero. As mentioned previously, the cross-coupled pair is a good choice for negative transconductor which can be characterized by an equivalent transconductance, \( g_d \), and capacitance, \( C_d \).
Assuming that the transconductors are properly placed (based on the transistor sizing to make sure enough enough energy is provided to the wave to accommodate its propagation), they behave as a distributed equivalent transconductance, \( G_d \), and distributed capacitance, \( C_d \) can be approximated by

\[
G_d \equiv \frac{ng_d}{\ell}, \quad C_d \equiv \frac{nc_d}{\ell},
\]

where \( n \) is the number of transconductors and \( \ell \) is the length of the interconnect (which they will add in parallel with the transmission line parameters \( C_o \) and \( G \)). Based on adding the cross-coupled transconductances, the effective interconnect propagation constant, \( \gamma \), can be calculated by

\[
\gamma = \sqrt{(R + j\omega L_o)((G - G_d) + j\omega(C_o + C_d))} = \alpha + j\beta
\]

However, this equation does not provide any intuition about how each parameter is affected by the transconductors. By making some low-loss assumptions about the values of the transmission-line parameters the equations for the loss constant, \( \alpha \) and the phase constant, \( \beta \) can be simplified as:

\[
\alpha \approx \frac{R}{2} \sqrt{\frac{(C_o + C_d)}{L_o}} + \frac{(G - G_d)}{2} \sqrt{\frac{L_o}{(C_o + C_d)}} \approx \frac{R}{2Z_o} + \frac{(G - G_d)Z_o}{2}
\]

\[
\beta \approx \omega \sqrt{L_o(C_o + C_d)}
\]
where $Z_o$ is the effective characteristic impedance of the interconnect and can be approximated by $\sqrt{L_o/(C_o + C_d)}$. These equations provide information on how $\alpha$ and $\beta$ change with the transmission-line parameters. The interconnect loss is a simple function of the series resistance, the conductance and transconductance, and the characteristic impedance. Note that ideally $G_d$ is chosen such that there is no signal attenuation. By differentiating (3-23) and (3-24), the sensitivity of $\alpha$ and $\beta$ to the transconductance can be expressed as

$$\frac{\partial \alpha}{\partial G_d} \approx \frac{Z_o}{2}, \quad \frac{\partial \beta}{\partial G_d} \approx 0$$

(3-25)

Based on this analysis, the characteristic impedance of interconnect determines the impact of the transconductance on the interconnect loss while the phase constant is completely independent of the transconductance. The analysis is slightly more complicated by adding the effects of $C_d$. Based on (3-25), parasitic capacitance both increases the loss (the first term) and decreases the effect of $G_d$ (second term). In effect, the transconductor capacitance self-loads interconnect and reduces the effectiveness of the transconductor. Therefore, a good figure-of-merit for the transconductor is

$$\omega_d \equiv \frac{g_d}{C_d}$$

(3-26)

where $\omega_d$ is similar to the high-frequency figure-of-merit (transit frequency) $\omega_T$ for a transistor. The transconductor parasitic capacitance also increases the phase constant, effectively reducing the propagation velocity along interconnect.
3.2.5.2. Rotary Traveling-Wave Oscillator

The rotary traveling-wave oscillator (RTWO) was first presented by John Wood et al., who realized CMOS test chips for 950 MHz and 3.4 GHz clocks [46]. The principle of the circuit is quite similar to two cross-coupled distributed oscillators. RTWOs are generated based on the Moebius effect, [46][48]: the differential line has two stable states; the one polarized positively, the other negatively. (Initial state of zero volts on the two lines is considered).

![Moebius effect diagram](image1)

![RTWO principle diagram](image2)

In the first case an open differential transmission line, with a delay of $\tau$, is connected to a voltage source through a switch. When the switch is closed, the voltage wave signal travels along the line. As the wave travels, the signal will be weaken because of the transmission-line loss. The second case shows the differential line with a cross-coupled feedback, so that the signal is inverted after one round (delay $\tau$). If the feedback is strong enough to reverse the
stable state of the line, then the state effectively switches. So the oscillation between the two polarized states occurs with a $2\tau$ period.

There is no reason why the oscillation should prefer to occur in the counterclockwise or in the clockwise rotational direction as long as the system stays symmetric. In practice, the path is not perfectly symmetric and it is the direction with the lowest energy losses which is dominant.

The differential line has two stable states because of the cross-coupled inverters distributed around the ring (Fig. 3-12). Similarly to the single-ended distributed oscillators, the input and output capacitance of the inverters can be considered as distributed on the line. The oscillation frequency is given by the propagation speed of the voltage wave on the distributed line. The time that the voltage needs to propagate a one full circle on the ring represents half the period of the oscillation. It is interesting to note that it is the nonlinearity of inverters which is allowing oscillations. Indeed, if inverters were perfectly linear, the feedback reverse signal would just be able to compensate exactly the following polarization, leading to a zero polarized state and stopping any oscillation. There are several advantages in using such an oscillator as compared to the single-ended Distributed VCO or to a standard ring oscillator. The architecture is fully differential; the coupled strip lines have a better predictable inductance than a single strip line [46]. Indeed, the forward and backward paths of current are well defined for the strip pair as they have less dependency on substrate’s capacitance and substrate losses.

The resonator is fully closed which eliminates the bandwidth limitation caused by the impedance termination. The only section which disturbs the perfect symmetry is the feedback,
requiring the strip-line to pass in another metal layer (shown with gray line in Fig. 3-11) leading to a slight local mismatch of the impedance. Indeed, contrary to the ring oscillator, the energy which charges and discharges the MOS gate capacitances is part of the wave energy. This energy is not lost at each stage but re-circulates from one stage to another into the closed path [46].

![Diagram of Coupled LC Oscillator](image)

**Fig. 3-13:** (a) Coupled LC oscillator (b) Coupled rotary wave oscillator.

In a conventional multi-phase LC oscillator, the coupling transistor is placed in parallel to the main switching pair (shown in Fig. 3-13(a)); therefore, the coupling factor is determined by the transconductance of the coupling transistor in the case of fixed oscillator cores [50][51]. Choosing larger coupling transistors, leads to higher transconductance, and the coupling factor will be higher while the phase imbalance will be lower. On the other hand, the higher transconductance will increase the noise contribution from the coupling transistors and stronger signal for a given power supply. Therefore, a trade-off between multi-phase
imbalance and phase noise is always present [52]. To solve this problem, the transmission line loading can be used in the coupling path (shown in Fig. 3-13-(b)) to increase the injection current and improve the coupling factor without increasing the transconductance of the transistors [52].

In contrast to LC-tank oscillators, wave-based oscillators are capable of providing an output frequency that is close to the transit frequency \( f_T \) of the device by distributing parasitic capacitances along the transmission line [53]-[57]. The characteristics of the transmission line determine the oscillation frequency [57].

3.3. General Phase Noise Methods

Different noise sources will affect an oscillator: thermal, shot, and flicker noise will produce fluctuations in the output of the oscillator in terms of amplitude and frequency and furthermore, substrate and supply noises are the other reasons for frequency impurity. These noise sources result in frequency fluctuations and their effect should be minimized. For example, using differential signaling would ideally eliminate the common-mode noise. The output of the oscillator is described as

\[
V_{out}(t) = V_o \left[ 1 + a(t) \right] f \left[ \omega_o t + \varphi(t) \right]
\]

(3-27)

where the amplitude, \( V_o \) is the maximum voltage swing and \( f \) is a periodic function for representing the shape of the output waveform of the oscillator with the frequency of \( \omega_o \), the phase fluctuation of \( \varphi(t) \), and the amplitude of \( a(t) \).
There are several ways for quantifying frequency instabilities of an oscillator. While detailed reviews of various techniques and measurement methods can be found in [58]-[61], the focus of this section is on the most popular figure of merit for characterizing the phase noise.

In the frequency domain, an oscillator’s frequency impurities are usually characterized in terms of the single sideband noise spectral density. It conventionally has the units of decibels below the carrier per Hertz (dBc/Hz) and is defined as:

\[
L\{\Delta \omega\} = 10 \log \left[ \frac{P_{\text{sideband}(\omega_0 + \Delta \omega, 1Hz)}}{P_{\text{carrier}}} \right]
\]  

(3-28)

where \(P_{\text{sideband}(\omega_0 + \Delta \omega, 1Hz)}\) represents the signal sideband power at a frequency offset, \(\Delta \omega\) from the carrier in a measurement bandwidth of 1Hz as shown in Fig. 3-14, and \(P_{\text{carrier}}\) is the total power of the carrier.

![Graph showing phase noise per unit bandwidth](image)

**Fig. 3-14: The phase noise per unit bandwidth.**

The plot of the free-running oscillator phase noise \(L\{\omega\}\) as a function of \(\Delta \omega\) on logarithmic scales is shown in Fig. 3-15. At large offset frequencies, there is a flat noise floor. The
spectrum of phase-noise can be described in three distinct regions: 1) rapid roll-off around the carrier (close-in phase noise) with $1/f^3$ rate, 2) $1/f^2$ roll-off in intermediate offsets (out-of-band region), and 3) flat phase noise where the phase noise hits the noise floor.

There are three popular approaches for analysis of the phase noise of circuits: Leeson’s model, Hajimiri’s approach, and Rael’s method. Hajimiri’s method is a useful numerical procedure to determine phase noise and provides insights into $1/f$ noise up-conversion and impact of noise current modulation. Rael’s method is useful for CMOS negative-resistance topology which provides a great insight into the design. In this research, both Leeson’s and Rael’s methods are applied in our oscillator phase noise calculation discussion.

![Fig. 3-15: A typical phase noise plot for a free running oscillator.](image)

### 3.3.1. Leeson’s Formula (Time-Invariant Phase Noise Model)

The phase noise model proposed in [62] and later expanded in [63][64] is widely known as the Leeson’s model, and is the most popular model used in practice, partly due to its simplicity. It
is based on a linear time-invariant (LTI) approach for oscillators. It predicts phase noise as follows:

\[
L\{\Delta \omega\} = 10 \log \left[ \frac{2FkT}{P_s} \left( 1 + \left( \frac{\omega_o}{2Q_L \Delta \omega} \right)^2 \right) \left( 1 + \frac{\omega_{1/f}^3}{\Delta \omega} \right) \right]
\] (3-29)

where \( F \) is an experimental parameter, \( k \) is Boltzmann’s constant, \( T \) is the absolute temperature, \( P_s \) is the average power dissipated in the resistive part of the tank, \( \omega_o \) is the oscillation frequency, \( Q_L \) is the effective quality factor of the tank with all loadings accounted for (also known as loaded \( Q \)), \( \Delta \omega \) is the offset from the carrier, and \( \omega_{1/f}^3 \) is the frequency of the corner between them \( 1/f^3 \) and \( 1/f^2 \) regions, as shown in Fig. 3-15.

3.3.2. Rael’s Method [65]

Rael discussed the factors which change the ‘\( F \)’ in the Leeson’s formula. In a negative-resistance differential pair oscillator (Fig. 3-16(a)), the \( F(\Delta f) \) can be represented as:

\[
L\{\Delta \omega\} = 10 \log \left[ \frac{2F(\Delta f)kT}{P_s} \left( \frac{\omega_o}{2Q_L \Delta \omega} \right)^2 \right]
\] (3-30)

\[
F(\Delta f) = 1 + \frac{2\gamma I_{bias} R_P}{\pi A} + \frac{4}{9} \gamma g_{d,M} R_P
\]

where \( F(\Delta f) \) is related to three different noise sources; noise from tank resistance, noise from differential pair, and noise from current source transistor, respectively (shown in Fig. 3-16).
Fig. 3-16: Noise Sources from different parts of a cross-coupled transistor.

To achieve minimum phase noise, it is desirable to minimize $F(\Delta f)$. To better understand the noise coming from the tail current, the effect of the differential pair switching on the tail current should be considered as it acts similar to a single-balanced mixer. The noise is translated up and down in frequency, and enters the resonator. The single-balanced mixer shows the largest conversion gain around the fundamental switching frequency, that is why only mixing by the fundamental is important. Noise originating in the tail current at $\omega_n$ up-converts to $\omega_b \pm \omega_n$. Similarly, noise at $2\omega_n \pm \omega_m$, downconverts to $\omega_b \pm \omega_m$. The phase noise caused by thermal noise originally at $2\omega_n$, is:

$$L\{\Delta \omega\} = \frac{4}{9} \gamma g_{d,M3} R_P \frac{kT R_P}{P_s} \left(\frac{\omega_o}{2Q\Delta \omega}\right)^2$$

(3-31)

where $\gamma$ is the noise factor of a single transistor (usually, $\sim 4/3$). By adding an LC filter resonating at $2\omega_b$ in the common-mode, the $2\omega_b$ component will be attenuated (ideally eliminated). This is because the white noise of the tail current source experiences a significant conversion gain around the second harmonic of the oscillation frequency [65].
As mentioned before, the related noise of the differential pair in $F(\Delta f)$ can be represented as

$$F(\Delta f) = \frac{2\gamma I_{bias} R_p}{\pi A}$$

(3-32)

The output amplitude, $A$, is represented as $(2/\pi)I_{bias}R_p$. It is not simple to replace $A$ with its equivalent and cancel out the $I_{bias}$ from numerator and denominator because as $I_{bias}$ increases, there is a limit for output amplitude which is defined by the supply voltage. Above that maximum amplitude which is imposed by supply voltage, by increasing the $I_{bias}$, the amplitude will not change but the power consumption will increase. Therefore, the operation region of oscillation can be divided to two different regions: current-limited regime which is set by amplitude, and voltage-limited regime in which the amplitude is saturated. The best phase noise can be achieved at boundary of these two regimes.

3.4. The Proposed Design

In this Section, the step-by-step design of the proposed oscillator is explained starting with the design of the standing-wave oscillator (SWO), and the rotary-wave oscillator (RWO), followed by discussions on phase noise in RWOs, phase noise in loaded SWOs, and the coupled oscillator dynamics. This chapter will conclude by RWO phase noise reduction techniques and related simulations.

As a starting point of the design, it is important to choose the transistor sizes properly to make the circuit operate at desired frequency with the minimum noise figure. The $f_{max}$ and $NF$ are plotted in Fig. 3-17 with respect to the width the transistor in a 0.13-$\mu$m CMOS technology for different current densities. Total width is kept constant as 50 $\mu$m. And the finger width varies
from 0.5 µm to 50 µm. As shown in Fig. 3-17, the current density varies from 50 µA/µm to 150 µA/µm. To be able to neglect the gate resistance, the finger width should be chosen narrow. Based on two parameters of maximum frequency of operation \( f_{\text{max}} \) and minimum noise figure \( NF_{\text{min}} \) for the transistors, the finger width of 1 µm is chosen for this design. At this width both maximum \( f_{\text{max}} \) and minimum \( NF \) is achievable which is favorable for CMOS design in high frequency.

![Graph showing noise figure and \( f_{\text{max}} \) measurement for the NMOS device in 0.13-µm CMOS Technology.](image)

**Fig. 3-17:** Noise figure and \( f_{\text{max}} \) measurement for the NMOS device in 0.13-µm CMOS Technology.

\( f_{\text{max}} \) is a better parameter to be considered than \( f_T \) because it considered the gate resistance. shown as follow:

\[
f_{\text{max}} \propto \sqrt{\frac{f_T}{R_{\text{gate}}}}
\]  

(3-33)

and the transient frequency can be calculated through;
\[
2\pi f_T = \frac{g_m}{C_{gs}} = \frac{\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}}{\frac{2}{3} C_{ox}WL} = \frac{\sqrt{2\mu_n C_{ox} \frac{1}{L} I_D}}{\frac{2}{3} C_{ox}L}
\] (3-34)

For a given drain current density, i.e., \(I_D/W\), to the first order of approximation, based on the above equation, \(f_T\) is independent of \(W\); therefore, the \(f_{max}\) is proportional to \(W^{3/2}\). The other important parameter is NF which is affected by different noise sources including gate, source, and drain, given as [66],

\[
NF = 1 + \frac{R_g}{R_s} + \gamma \left(\frac{R_g + R_s}{R_s R_{cho}}\right)^2 \left(\frac{f}{f_T}\right)^2
\]

where \(R_g, R_s,\) and \(R_{cho}\) are the gate, source, and channel resistance, respectively. The relationship of \(f_T\) with \(W\) is shown in (3-33). \(R_{cho}, R_g,\) and \(R_s\) can be calculated through

\[
R_g = \frac{1}{3n_f} \left[ R_s \ast \frac{W_f}{L} \right]; \quad R_{cho} = \frac{1}{\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}}; \quad \frac{R_s}{R_L} = \left(\frac{\omega_f}{\omega}\right)^2
\]

(3-36)

and \(I_D\) can be calculated through,

\[
I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2
\]

(3-37)

For simplicity the gate related noise can be ignored. Looking into (3-34), and considering the relationship of \(R_g, R_{cho}\) and \(f_T\) with width, it can be easily seen that NF relatively changes with \(W^{3/2}\).
3.4.1. Standing-Wave Oscillator (SWO)

The schematic of a differential quarter-wave ($\lambda/4$) SWO is shown in Fig. 3-18(a) with its equivalent differential small-signal model. A standing-wave is supported in the transmission line tank when negative resistance generated from cross-coupled NMOS transistors compensates the tank losses.

The transistors contribute loading through the drain-bulk capacitance, $C_{db}$, gate-source capacitance, $C_{gs}$, and gate-to-drain overlap capacitance, $C_{gd}$, which is enhanced due to the Miller effect. Additionally, the output buffer differential capacitance, $C_{buff}$, loads the tank. The desired frequency tuning range is provided through the tuning varactor, $C_{var}$. An equivalent differential capacitance for the tank circuit is (shown in Fig. 3-19)

$$C_{equ} = C_{var} + \frac{1}{2} C_{db} + \frac{1}{4} \left( C_{gs} + C_{sg} \right) + 2C_{gd} + C_{buff}.$$  \hspace{1cm} (3B38)

A minimum transconductance, $g_m$, is required to overcome the tank losses due to the transmission line quality factor, $Q_{TL}$, and capacitance quality factor, $Q_C$.

![Fig. 3-18: Standing-wave oscillator and equivalent small-signal model.](image)
As shown in [67], the impedance of the lossy transmission line is calculated from

\[
Z (-\ell) = Z_o \frac{Z_L + jZ_o \tanh (\gamma \ell_s)}{Z_o + jZ_L \tanh (\gamma \ell_s)}
\]

The used resonator is shorted at the end, therefore, the related admittance will be

\[
Y_{TL} = Y_o \coth (\gamma \ell_s)
\]

where \( \gamma = \alpha + j\beta \) is the propagation constant comprised of the attenuation (\( \alpha \)) and phase (\( \beta \)) constants, \( Y_o = 1/Z_o \) is the characteristic admittance, and \( \ell_s \) is the transmission line length. The total differential admittance of the tank is

\[
Y_{SWO} = \frac{1}{2} \left( 2j\omega C_{equ} + G - g_m + Y_o \coth (\gamma \ell_s) \right),
\]

where \( G \) is the parasitic conductance including the NMOS channel conductance, \( g_{ds} \), and conductance due to the series resistance of the varactor and device capacitances, \( G_C \). At the oscillation frequency, \( f_o \), the varactor conductance (which dominates the loss) is
\[ G_C = \frac{\omega_o C_{var} Q_c}{1 + Q_c^2} \approx \frac{\omega_o C_{var}}{Q_c} = r_v \left( \omega_o C_{var} \right)^2, \]  \hspace{1cm} (3-42)

where \( r_v \) is the series resistance of the varactor. Hence, the loaded quality factor of the oscillator is defined by

\[ Q_{SWO} = \frac{\omega_o}{2} \left| \frac{\partial Y_{SWO}}{\partial \omega} \right|_{\omega=\omega_o} \]  \hspace{1cm} (3-43)

For the SWO with a lossy tank and varactors, the loaded quality factor is

\[ Q_{SWO} = \frac{1}{2} \frac{\tau \omega_o - v_p^{-1} \omega_o \ell_s \text{csch}^2 \left( \gamma \ell_s \right)}{j \tau \omega_o + \frac{1}{2} GZ_o + \coth \left( \gamma \ell_s \right)}, \]  \hspace{1cm} (3-44)

where \( \tau = 2 Z_o C_{eq} \) is a time constant for the capacitive loading of the transmission line and \( v_p \) is the phase velocity \( \left( v_p = \frac{1}{\sqrt{LC}} \right) \). When device loading is eliminated (i.e., \( C_{eq}, G = 0 \)), the loaded \( Q \) reduces to \( Q_L = \beta/2 \alpha \), the unloaded quality factor of a \( \lambda/4 \) transmission line.

In Fig. 3-20, the loaded quality factor for the SWO tank is plotted versus the loading time constant (for different capacitance quality factors). The unloaded quality factor of the transmission line is assumed to be 15, a typical value for a shielded microstrip line in a silicon integrated circuit process. If the quality factor of the capacitance, \( Q_C \), is very large, the quality factor of the tank improves since more energy is stored in the high quality capacitor.

50
Fig. 3-20: $Q_L$ vs. loading time constant for various $Q_C$ ($Q_{TL} = 15$).

Typically varactors offer a low quality factor in the range of 2 to 10 for the 60 GHz frequency range, and in this case, Fig. 3-20 illustrates the capacitive loading on the tank reduces the overall tank quality factor. In compare with the transmission line quality factor, the worse varactor quality factor will degrade the overall tank $Q$. The lower loaded quality factor will be shown to reduce the phase noise of the SWO. Based on the one-port oscillator model, the active and load admittances can be written as

$$Y_{IN} = -\frac{g_m}{2}$$

$$Y_L = \frac{Y_o \coth(\gamma \ell_S)}{2} + j\omega C_{equ} + \frac{G}{2} \tag{3-45}$$

From (3-45), the oscillation conditions (i.e., $\Gamma_L \Gamma_{IN} = 1$) are found by separating the real and imaginary parts of the oscillator admittance.
\[ j\omega\tau + \text{Im}\{\coth \gamma \ell_s\} = 0 \]
\[ (G - g_m) \text{Re}\{\coth \gamma \ell_s\} = 0 \]

(3-46)

The reactive behavior of the oscillator in (3-46) indicates that the capacitive loading reduces the electrical length of the transmission line. The oscillation frequency of the SWO, \( f_o \), is calculated from a linear approximation around \( \beta \ell_s = \pi/2 \) of the imaginary term in (3-46).

\[ f_o \approx \frac{1}{4(v_p \ell_s + \tau)} \]

(3-47)

For a given oscillation frequency, the loading time constant reduces the necessary electrical length of the transmission line tank and allows more frequency tuning. From (3-46), the appropriate loading for tuning range of at least 5% implies a capacitive loading time constant of at least \( \tau \geq 0.05 v_p \ell_s \). The real term in (3-45) indicates that capacitive loading reduces the loaded \( Q \) and increases the required transconductance to start-up and maintain the oscillation. Therefore, the minimum transconductance for oscillation is

\[ g_m \geq G + Y_o \text{Re}\{\coth \gamma \ell_s\} \approx \frac{\omega_o C_{\text{var}}}{Q_C} + \frac{Y_o}{Q_{\text{TL}}} \]

(3-48)

The varactor tuning range determines the tuning range of the oscillator and tank loading from (3-47). Nonetheless, larger frequency tuning range for the SWO costs additional transconductance and power consumption.

Leeson’s formula predicts the phase noise of the SWO by accounting for the loaded quality factor and the oscillation power [68]. The noise of active and passive devices can be
decomposed into in-phase and quadrature noise contributions with respect to the oscillation and expressed as noise conductance, $G_n$, and susceptance, $B_n$.

$$Y_n = \frac{Y_{\text{noise}}}{G_L} = \frac{G_{\text{noise}} + jB_{\text{noise}}}{G_L} = G_n + jB_n = \frac{i_{n,I}}{V_o} + j\frac{i_{n,Q}}{V_o},$$

(3-49)

where $Y_{\text{noise}} = G_{\text{noise}} + jB_{\text{noise}}$ is the equivalent noise admittance of the oscillator [73].

$G_n = G_{\text{noise}} / G_L$, $B_n = B_{\text{noise}} / G_L$, and $G_L$ is the oscillator load admittance in the free-running state, and $V_o$ is the amplitude of oscillation. It has been shown that the noise conductance more strongly impacts amplitude fluctuations while the noise susceptance dominates the phase perturbation of the oscillator. Thus, we focus our attention to the noise susceptance, $B_n$.

The oscillator operation is generally chosen between the voltage- and current-limited regimes of operation based on the bias current, $I_{\text{bias}}$ that generates a voltage swing, $V_o$, to minimize the oscillator phase noise [99]. For low bias currents, bias current variations result in a proportional change in this voltage swing. The phase noise at a frequency offset $\Delta \omega$ for an SWO is [69]:

$$L\{\Delta \omega\} = \frac{4kTF}{GV_o^2} \left(\frac{\omega_o}{2Q_{\text{SWO}}\Delta \omega}\right)^2,$$

(3-50)

where

$$F = 1 + \gamma \left(\frac{4I_{\text{bias}}\omega_o}{\pi GS} + \frac{\pi V_o}{2V_{\text{eff}}^2}\right).$$

(3-51)
where $V_{\text{eff}}$ is the effective voltage of the bias transistor. The excess noise factor, $F$, consists respectively of noise contributions from the tank conductance, differential pair, and current source. The differential pair current noise depends on the channel noise coefficient, $\gamma$, bias current, and slope of the differential waveform, $S$. The current source noise is inversely proportional to the effective gate voltage, $V_{\text{eff}}$. The relative contribution of each noise source depends on the $I_{\text{bias}}$, $f_o$, and the transistor, $f_T$ [69]. For instance, high $f_T$ supports fast rise and fall times that in turn reduce the contribution of differential pair noise [71]. It should be added that the effect of the output extra parasitic can change the output rise and fall time.

At millimeter-wave frequencies, the slope is largely determined by the first harmonic, i.e., $S = \omega_o$. For $I_{\text{bias}} = 3mA$, $\gamma=4/3$, $V_{\text{eff}} = 0.2V$, and $V_o = 1V$, the excess noise factor is sixteen. For $Q_{\text{SWO}} = 15$, the phase noise is -93 dBc/Hz at a 1 MHz offset. When $I_{\text{bias}}$ reaches a critical level, additional current does not change $V_o$ because of transconductance compression ($g_m$ saturated value).

In the voltage-limited regime, the phase noise is

$$L \{ \Delta \omega \} = \frac{i_{n,Q}^2}{V_o^2 G^2} \left( \frac{\omega_o}{Q_{SWO} \Delta \omega} \right)^2 = \frac{B_n^2}{G^2} \left( \frac{\omega_o}{Q_{SWO} \Delta \omega} \right)^2$$

(3-52)

where $i_{n,Q}^2 = 4kTG^2$. The noise susceptance, $B_n$, is independent of $I_{\text{bias}}$, since in the voltage-limited regime, the amplitude voltage is saturated and thus does not depend on $I_{\text{bias}}$.

The phase noise of an SWO VCO is simulated in Spectre at 45 GHz for a tuning range of 5% based on an NMOS cross-coupled pair and plotted in Fig. 3-21 as a function of bias current.
As can be seen from the figure, the phase noise at a 1 MHz offset decreases by 10 dB as the tail current increases and flattens above 3 mA as the tank enters the voltage-limited regime.

![Graph showing phase noise as a function of bias current](image)

**Fig. 3-21:** Spectre simulation of the phase noise at 1 MHz offset for a standing-wave oscillator as a function of bias current ($W = 10\mu m$).

### 3.4.2. Rotary-Wave Oscillator

In our analysis, the proposed RWO is decomposed into two circuits; one that supports standing-wave modes and one that supports rotary-wave modes. The proposed RWO (shown in Fig. 3-22) comprises of four standing-wave oscillator stages (coupled together) distributed around a differential transmission line ring with one differential inversion along the transmission line ring.

To support the traveling wave around the loop, four SWO stages are coupled together with a $\lambda/8$ transmission line (i.e., $\beta \ell_R = \pi/4$). Hence, the traveling wave locks each of the SWO stages at 45° with respect to its neighbors. Therefore, each SWO stage is effectively injection locked to the neighboring stage such that the overall structure behaves as a single oscillator. In
this topology, the direction of the rotating wave is arbitrary. Previous work has discussed how
the direction of the rotating wave may preferentially be chosen [72]. One other way that has
been suggested is having an imbalance in the fully symmetric layout which forces the wave to
travel in the lower loss path [46].

Fig. 3-22: Millimeter-wave RWO with four SWO stages distributed around a transmission line coupling
network.

A small-signal model of the proposed RWO is shown in Fig. 3-23. The oscillators are assigned
an arbitrary absolute phase. By choosing one of the SWOs as a reference node at 0°, the
standing-wave mode forces the nearest neighbors to have an identical phase. However, one
oscillator must be out-of phase (180°) with respect to the reference oscillator. This implies that
two virtual grounds exist along the horizontal and vertical axes.
The horizontal virtual ground exists along the differential standing-wave oscillator admittance. Similarly, a vertical virtual ground exists at the oscillator that is on the opposite side of the reference oscillator because the path length corresponds to a $90^\circ$ phase shift from the reference node.

The virtual ground cuts through this opposite oscillator and implies that only two neighboring oscillators couple to the reference oscillator. Consequently, the standing-wave admittance is calculated from the circuit model in the top of Fig. 3-24 and incorporates the contribution of
the original SWO tank as well as the coupling network. This is consequently referred to as the
loaded standing-wave tank. The standing-wave oscillator injects a current, \( I_{SWO} \), into the
coupling transmission lines. The current is split into two components that travel in opposite
directions into the coupling network. The coupling admittance looking into the neighboring
SWO is calculated as

\[
Y_{C,SWO} = \frac{Y_0 \coth \left( \gamma \ell_R \right) + 2Y_{SWO} + Y_o \tanh \left( \gamma \ell_R \right)}{2Y_o + 2Y_{SWO} \tanh \left( \gamma \ell_R \right)}.
\]  

(3-53)

The admittance of the loaded SWO is the parallel combination of two coupling networks and
the single-ended admittance of the original SWO, i.e. \( Y = 2Y_{SWO} + 2Y_{C,SWO} \). The proper
length of the RWO coupling lines is derived from \( \Im \{2Y_{SWO} + 2Y_{C,SWO} \} = 0 \). Assuming that
\( \alpha = 0 \), the coupling transmission line length is determined from the roots of

\[
\cot (\beta \ell_R) - \left( 1 - 2\left| Y'_{SWO} \right|^2 \right) \tan (\beta \ell_R) \\
- \left( 5 + \left( 1 - 2\left| Y'_{SWO} \right|^2 \right) \tan^2 (\beta \ell_R) \right) \Im \{Y'_{SWO} \}, \\
+ 2 \tan (\beta \ell_R) \Im \{Y'_{SWO} \}^2 = 0
\]  

(3-54)

where the prime superscript denotes an admittance normalized to \( Y_o \). When the SWO is tuned
to resonate at the oscillation frequency (\( \Im \{Y_{SWO} \} = 0 \)), the solution to this equation is given
by \( \cot (\beta \ell_R) = \sqrt{1 - 2\left| Y'_{SWO} \right|^2} \). Therefore, an SWO with high \( Q \) results in a coupling
transmission line length of \( \beta \ell_R = \pi/4 \). To absorb the loading capacitance, \( C_{equ} \), into the
RWO tank rather than the SWO tank, the coupling transmission line length has to be adjusted
according to (3-53). The $Q$ of the loaded SWO tank is found by substituting the parallel admittance combination, $2Y_{SWO} + 2Y_{C,SWO}$ into (3-42);

$$Q_L = \frac{\omega_o}{2} \left| \frac{\partial Y_{SWO}}{\partial \omega} + \frac{\partial Y_{C,SWO}}{\partial \omega} \right| \frac{Y_{SWO} + Y_{C,SWO}}{Y_{SWO} + Y_{C,SWO}} \right|.$$  \hspace{1cm} (3-55)

The $Q$ of the loaded SWO tank is approximated from the parallel combination of $Q$s contributed by the SWO and coupling network, i.e., $Q_L \approx 2Q_{SWO} \parallel Q_{C,SWO}$. The quality factor for the SWO in the presence of loading from the coupling transmission lines depends on whether the $Q$ of the coupling network is greater or less than the quality factor of the SWO. If the SWO tank and coupling network have similar $Q$s, the loaded $Q$ is the same as the unloaded SWO $Q$.

The $Q$ of the RWO also depends on the quality factor of the capacitive loading. For low parasitic conductance (large $Q_C$), the quality factor of the loaded SWO is higher than the RWO. For high parasitic conductance, the RWO has a higher tank quality factor. The RWO quality factor is improved with respect to the SWO quality factor because more energy is stored in the RWO coupling networks than in the SWO tank.

A rotary-wave current, $I_{RWO}$, is also present through the RWO illustrated in Fig. 3-22 and presumably dominates the standing-wave mode. From the figure, the rotary-wave current bypasses the SWO cell and does not interact with the SWO admittance. The coupling admittance of the rotary-wave mode is found by the translation of the coupling admittance of the next stage through coupling transmission line.
\[ Y_{C,RWO} = Y_0 \left( \frac{Y_{C,RWO} + 2Y_{SWO}}{Y_0 + (Y_{C,RWO} + 2Y_{SWO}) \tanh(\gamma \ell_R)} \right) \]

Solving for \( Y_{C,RWO} \),

\[ Y_{C,RWO} = Y_{SWO} \times \left( -1 + \sqrt{1 + \frac{2}{Y_{SWO}} \coth(\gamma \ell_R) + \left( \frac{1}{Y_{SWO}} \right)^2} \right) \]

Fig. 3-25: Theoretical calculation of the ratio of rotary-wave to standing-wave currents for different transmission line quality factors, \( Q = 5 \).

The ratio of the rotary- and standing-wave currents determines whether the rotary-wave mode dominates the locked behavior and is plotted in Fig. 3-25 as a function of the loading time constant of the SWO. Notably, more current is stored in the rotary-wave current with respect to the standing-wave current as the loading capacitance is reduced. Additionally, the energy stored in the rotary-wave mode is increased with high quality factor transmission lines. Intuitively, the SWO and RWO modes become increasingly decoupled as the \( Q \) of the passive
elements increases. As the transmission line and capacitor quality factor reduces, less current propagates in the rotary-wave mode through the coupling network. If the ratio is small, the oscillator will no longer support rotary-wave oscillations.

3.4.3. Phase Noise in Rotary-Wave Oscillators

The phase noise of the conventional rotary-wave oscillator has been analyzed in [62] and [69], but the phase noise of the proposed hybrid RWO/SWO has not been previously analyzed. This section quantifies the phase noise reduction of the proposed RWO with respect to an individual SWO. The phase noise analysis is decomposed into the impact of the rotary-wave coupling network and the coupled oscillator dynamics.

3.4.3.1. Phase Noise for the Loaded SWO

A small-signal model for the noise is illustrated in Fig. 3-26. The noise current sources in the RWO are generated by the active devices in the SWO and will see the SWO coupling network admittance \( Y_{C,SWO} \) given in (3-52). Assuming the oscillator is biased in the voltage-limited regime, the phase noise for the loaded SWO is

\[
L\{\omega\} \propto \frac{B_n^2}{G_L^2} \left( \frac{\omega_o}{Q_L \Delta \omega} \right)^2
\]

(3-58)

where \( G_L \) is the loaded conductance formed from the parallel combination of the SWO and the coupling network conductance; e.g., \( G_L = G_{SWO} + NG_{C,SWO} \). \( N \) is the number of coupling networks seen at the SWO and \( Q_L \) is defined as (3-54). Normalizing the RWO phase noise to the SWO phase noise, the predicted phase noise reduction is
If the coupling network and the standing-wave oscillator $Q$ are similar, the $Q$ of the loaded SWO is unchanged, i.e., $Q_L \approx Q_{SWO}$, and only a small change in the phase noise occurs. However, the coupling network increases the conductance seen at the oscillator tank.

Fig. 3-27 plots the phase noise reduction of the loaded SWO with respect to the unloaded SWO. If only one coupling network is connected to the SWO, the phase noise is at most 6 dB lower since the conductance doubles. For the proposed RWO, each SWO sees two coupling networks and the phase noise decreases by as much as 9.5 dB. In both cases, the phase noise reduction is limited by the loading time constant as more energy is dissipated in the lossy capacitor. The reduction of phase noise due to the increase of parallel conductance must be accompanied by additional current/power consumption to maintain the voltage-limited operation.

![Noise Model](image)

**Fig. 3-26: Small signal model of noise injected into rotary-wave structure.**
3.4.3.2. Coupled Oscillator Dynamics

Injection locking between each oscillator also impacts the phase noise. As each oscillator injects noise into the rotating wave, this noise induces a phase shift which continues to propagate around ring. The phase noise of coupled oscillators has been studied from the standpoint of standing-wave coupling for beam-steering applications by Chiang et al. [73]. This coupled oscillator treatment is adapted to develop an expression for the phase noise for the RWO phase noise.

![Diagram](image)

**Fig. 3-28:** Determination of coupling strength from the combination of standing- and rotary-wave modes.
The phase perturbation of the $i^{th}$ oscillator in the RWO from the desired phase is represented as $\theta_k \rightarrow \theta_k + \delta\theta_k$ and is related to the noise susceptibility, $B_n$, of the SWO where the noise contributions are assumed to be independent, identical random variables. In [73], the general frequency-domain phase dynamics of the coupled oscillators is given by

$$\frac{j \omega}{\omega_{3dB}} \delta\theta_k = -\sum_{j=1}^{N} \varepsilon_{kj} \frac{I_{SWO,j}}{I_{SWO,k}} (\delta\theta_k - \delta\theta_j) - \frac{B_n}{G_L},$$

(3-60)

where $\omega_{3dB} = \omega_o / 2Q_L$, $\varepsilon_{kj}$ is a coupling factor from $j^{th}$ oscillator to the $k^{th}$ oscillator, and $I_{SWO,j}$ and $I_{SWO,k}$ are the amplitude of the current of the $j^{th}$ and $k^{th}$ oscillators, respectively. Finally, $G_L$ is the parallel conductance seen at the resonant tank, i.e., $G_L = G_{SWO} + 2 \ G_{C,SWO}$.

To solve the dynamics of the rotary-wave coupled oscillator system, the oscillator current at each stage and the coupling factor must be determined for the RWO. The superposition of the standing-wave and rotary-wave currents determines the current injected from one SWO to the next and is illustrated in Fig. 3-28. We arbitrarily assign the direction of propagation from left to right. Defining the current entering the SWO stage on the coupling transmission line as $I_-$ and the current that exits along the coupling transmission line as $I_+$, the superposition of the two currents in Fig. 3-24 is

$$I_- = I_{RWO} - \frac{1}{2} I_{SWO} = I_{SWO} \left( \frac{I_{RWO}}{I_{SWO}} - \frac{1}{2} \right)$$

(3-61)

$$I_+ = I_{RWO} + \frac{1}{2} I_{SWO} = I_{SWO} \left( \frac{I_{RWO}}{I_{SWO}} + \frac{1}{2} \right)$$

(3-62)
Since \( I_{+,k-1} = I_{-,k} \), the current injected from the \( k-1 \)th SWO to the \( k \)th SWO is

\[
\begin{align*}
\varepsilon_{k-1,k} &= \frac{I_{SWO,k}}{I_{SWO,k-1}} = \frac{I_{+,k-1}}{I_{SWO,k}} \frac{I_{SWO,k}}{I_{-,k}} \\
Y_{C,SWO} + Y_{C,RWO} + 2Y_{SWO} &= 2Y_{C,SWO} \quad Y_{C,SWO} + Y_{C,RWO} + 2Y_{SWO}.
\end{align*}
\] (3-63)

Since each cell is identical, the coupling factor at each stage is identical, \( \varepsilon = \varepsilon_{k-1,k} \). Based on the admittances calculated in the previous section, the coupling factor is plotted in Fig. 3-29.

![Fig. 3-29: Analytical prediction of the coupling factor and phase as a function of the SWO loading time constant.](image)

For a small loading time constant, the coupling factor is small and implies that the SWOs are weakly coupled. Increasing the loading time constant increases the coupling factor and additionally introduces an undesirable coupling phase between the neighboring stages.

The phase perturbation of each SWO is expressed as a vector \( \delta \bar{\theta} = [\delta \theta_1 \delta \theta_2 \ldots \delta \theta_N]^T \).

Therefore, the coupled phase dynamics in (3-60) are expressed in an \( N \times N \) matrix that captures
the interaction of \( N \) SWOs. The coupling network topology is a matrix, \( N \), that represents the RWO network. The RWO coupling matrix for four SWO is represented as a \( 4 \times 4 \) matrix where each row expresses the dynamics from (3-60):

\[
N = \begin{pmatrix}
-\varepsilon - jw & 0 & 0 & \varepsilon \\
\varepsilon & -\varepsilon - jw & 0 & 0 \\
0 & \varepsilon & -\varepsilon - jw & 0 \\
0 & 0 & \varepsilon & -\varepsilon - jw
\end{pmatrix}, \quad (3-64)
\]

where, \( w = \frac{\omega}{\omega_{dB}} \). Now, the coupled dynamics in (3-59) are expressed as \( N \Delta \theta = \frac{B_n}{G_L} \) and the phase perturbation due to the noise susceptance is

\[
\Delta \theta = P \frac{B_n}{G_L}, \quad (3-65)
\]

where \( P = N^{-1} \). The phase noise of each SWO is expressed in terms of the phase noise contributions of each SWO in the system;

\[
|\Delta \theta_k|^2 = \frac{B_n^2}{G_L^2} \sum_{j=1}^{N} |p_{kj}|^2, \quad (3-66)
\]

where \( p_{kj} \) is an element in the matrix \( P \). In the four element coupling network, the phase noise is:
\[
\left| \theta_k \right|^2 = \frac{w^6 + 4w^4 \varepsilon^2 + 6w^2 \varepsilon^4 + 4 \left( \frac{1}{w^2 G_L^2} \right)}{w^6 + 4w^4 \varepsilon^2 + 4w^2 \varepsilon^4 + 16 \left( \frac{1}{w^2 G_L^2} \right)} \approx \frac{1}{4} \left( \frac{1}{w^2 G_L^2} \right),
\]

(3-67)

where the final approximation holds at low frequency offsets, i.e., \( \Delta \omega < \omega_{3,db} \). The term in parenthesis represents the phase noise of the uncoupled SWO. Therefore, the coupling reduces the phase noise by a factor of \( N \), in this case an additional 6 dB. At large frequency offsets, the phase noise reduction approaches 0 dB.

### 3.4.3.3. RWO Phase Noise Reduction and Simulation

Substituting the phase noise reduction due to the loaded tank conductance and the coupled oscillator dynamics, the phase noise reduction for low frequency offsets is approximated as

\[
PN_{red} = \left( \frac{G_{SWO}}{G_L} \right)^2 \left( \frac{Q_{SWO}}{Q_L} \right)^2 \frac{1}{N}.
\]

(3-68)

For a four-oscillator RWO, SWO coupling reduces the phase noise by an additional 6 dB compared to (3-58). As the frequency offset approaches the injection locking bandwidth, i.e., \( \Delta \omega \rightarrow \omega_{3,db} \), the phase noise reduction due to coupling degrades and approaches 0 dB. Since the coupling strength is relatively large (\( \varepsilon \sim 0.4 \)), the phase noise reduction extends above 100 MHz; well beyond the 1 MHz of interest in many communication applications. Therefore, the minimum phase noise reduction of the RWO with respect to the SWO is roughly 15.5 dB. The overall absolute phase noise can be expressed as
\[
L \{ \Delta \omega \} = \frac{1}{N} \left( \frac{G_{SWO}}{G_L} \right)^2 L_{SWO} \{ \Delta \omega \},
\]

(3-69)

where \( L_{SWO} \{ \Delta \omega \} \) is calculated in (3-50 (a)). To verify this analysis, harmonic balance simulations of the SWO, loaded SWO, and RWO using a 0.13\( \mu \)m NMOS process is presented in Fig. 3-30.

Each SWO is biased at 3.5 mA and the nominal oscillation frequency is 45 GHz. When the SWO is loaded by the finite-\( Q \) coupling network, the phase noise of the loaded SWO is 7 dB lower than the original SWO. This is less than the 9.5 dB predicted from (3-58) as accounted for by the capacitive loading of the NMOS transistors. Below the \( 1/f \) corner (around 200 kHz) of the oscillator, the phase noise reduction is smaller. For the RWO, the phase noise is suppressed by an additional 4 dB relative to the loaded SWO at a 1 MHz offset. Therefore, the simulated phase noise reduction is predicted from a combination of the increased tank conductance and the interaction between SWOs through the RWO network.

The phase noise at a 1-MHz offset is plotted as a function of the bias current in Fig. 3-31 for the unloaded SWO and the RWO, ignoring the impact of varactors. The quality factor of the varactor is low and will degrade the phase noise of the oscillator. To have a fair comparison between the phase noise of the oscillators and not VCOs, the varactors are ignored for comparing the phase noise of RWO and SWO.
Fig. 3-30: Harmonic balance simulation of the phase noise for an SWO, loaded SWO, and RWO ($I_{bias} = 3.5$ mA, $Q_L = 20$).

Fig. 3-31: Simulation of phase noise reduction at 1 MHz offset for the RWO and SWO with no varactor loading versus bias current.

At a low bias current (in the current-limited regime), the phase noise reduction is 10 dB. As the bias current increases and the oscillator enter the voltage-limited regime, the phase noise
reduces by around 16 dB. This agrees relatively well with the prediction of the bound on the phase noise reduction of 15.5 dB. Additionally, the minimum phase noise occurs at 4 mA as opposed to 3 mA due to the low tank conductance.

3.5. Circuit Implementation in 0.13-µm BiCMOS Technology

The RWO circuit is fabricated in a seven metal-layer, 0.13-µm SiGe BiCMOS process. The implemented circuit includes the rotary-wave oscillator, an 8-to-1 phase selector, and a 50-Ω output buffer described in [16]. Microstrip transmission lines are realized with thick aluminum metal layers (AM) and a copper metal layer (MQ) as a shielded ground to eliminate substrate coupling (modeled in HFSS and shown in Figure 3-32).

![HFSS model for coupled transmission line.](image)

The series and shunt losses of coupled transmission lines affect the quality factor, and consequently the phase noise of the oscillator. The geometry of the interconnect width (w) and separation (s) impacts the transmission line losses. Increasing either w or s tends to decrease series loss due to the reduced skin effect but it increases shunt loss due to increased losses in the silicon dioxide. The Q for the thick-metal transmission line is plotted as a function of these parameters in Figure 3-33.
Also not only one transmission line has been simulated in HFSS to choose the proper width and length, but also the SWO load transmission line has been simulated in HFSS to make sure of proper quality factor shown in Figure 3-33. As shown in Figure 3-34(a), the top metal layers are thicker and more proper for high frequency design to achieve lower parasitic capacitors.

Figure 3-33: Coupled transmission line quality factor for various width and spacing at 45 GHz.

Figure 3-34: (a) Technology layer models (b) SWO load layout imported from Cadence to HFSS.
To achieve high $Q$, the spacing between the RWO differential transmission line are optimized for width of 4 $\mu$m and space of 16 $\mu$m, respectively, resulting in a differential characteristic impedance of 50 $\Omega$ while maintaining area efficiency. The attenuation of these transmission lines is 0.92 dB/mm. The length of the SWO and RWO transmission lines are respectively 0.185 mm and 0.45 mm. The SWO transmission line length absorbs the additional loading introduced by the varactors and transistor parasitic capacitances.

![Figure 3-35: Monte-Carlo simulation for transient output of the oscillator for all eight different phases.](image)

A Monte Carlo simulation of the RWO is plotted in Figure 3-35 and shows the simulated output for mismatch and process variations at all eight oscillator nodes of the RWO. The steady-state phase difference of each oscillator is 45° apart. Monte Carlo simulation shows that in 92% of 100 runs, the phase mismatch between each SWO is less than 1° (0.38 psec) against circuit mismatch and 8% of the runs it is less than 0.95° (0.35 psec). As mentioned before, each SWO stage is loaded with an output buffer to isolate the oscillator core from a differential 8:1 multiplexer. To drive the 50-Ω output impedance, the phase selector output is buffered by a differential 50-Ω driver. The multiplexer is implemented in two stages; the first stage is a 4:1 multiplexer implemented with four HBT differential pair legs and NMOS
cascode transistors. The second stage is a 2:1 multiplexer selects the differential output phase. To drive the 50-Ω output impedance, the phase selector output is buffered by a differential 50-Ω driver.

Figure 3-36: Chip microphotograph of the RWO with output multiplexer and buffer.

Figure 3-37: Test chip setup.
The die micrograph of the circuit and the die under test with probe station are illustrated in Figure 3-36 and Figure 3-37, respectively. The layout of the chip occupies a total area of 0.9 mm × 0.7 mm. The active area of the RWO, including buffers between the oscillator and phase selector, is 500 µm × 500 µm. Notably the first multiplexer of the phase selector is located in the interior of the RWO to allow symmetric loading of the RWO. The second multiplexer is placed outside of the RWO. Therefore, only one differential signal is routed underneath the RWO, which has been modeled with transmission line.

3.5.1. RWO Measurement Results
The rotary-wave oscillator operates at 1.2 V with a current consumption of 11.5 mA. Therefore, the oscillator core consumes 13.8 mW. The phase selector and 50-Ω driver operate from a 2.5 V supply and draw 8.5 mA and 10 mA current, respectively. The overall power consumption of the chip including the output buffers is 58.4 mW. The chip is tested with on-wafer probing using Picoprobe 40A GSG RF probes. An Agilent E4448A 50GHz spectrum analyzer measured the frequency and phase noise characteristics. One differential output is terminated by a 50-Ω termination through a bias-tee to generate a single-ended output.

In Figure 3-38, the measured frequency spectrum illustrates a carrier power of -21.5 dBm at 45 GHz. The reason for achieving lower frequency of oscillation in measurements as compared to simulations can be attributed to the fact that the foundry-provided models used in this design were characterized only up to 40 GHz. To alleviate this problem, in the next design, HFSS modeling is used for the transmission lines’ model over the desired frequency range.
When the cable loss of 10 dB and probe losses of 1.5 dB are de-embedded from the power measurement, the actual power of the oscillator circuit is -10 dBm. The path through the RWO buffer, phase selector, and output buffer accounts for additional 10 dB of loss between the RWO core and the bondpads and suggests an oscillator core power of 0 dBm. Spurious tones are present on the oscillator spectrum at a 5 MHz offset from the carrier as well as at 25 MHz offset. While the voltage supply, $V_{DD}$, is biased using batteries, a switching supply is used to bias the current source which introduced the spurious tones.

![Figure 3-38: Measured output frequency spectrum at 45 GHz.](image)

Figure 3-39 shows the amplitude and frequency dependence of the oscillator over the tuning range. Only 2 dB of variation is seen in the amplitude while achieving a 6.5% tuning range. The simulation result in Spectre is plotted in the dashed line and compared to the measurement result; plotted in the solid-line. The difference between the measured and the simulated tuning range is less than 2 GHz while the amplitude error is less than 1 dB. The simulation result predicts less variation in amplitude than the measured tuning range.
Figure 3-39: Tuning range and amplitude variation of the measured RWO as compared to the simulation results.

Figure 3-40: Phase noise measurement for free-running oscillator at 45 GHz.

Figure 3-40 shows the phase noise measurement of the free-running oscillator. At 45 GHz, the phase noise is -91.32 dBc/Hz at a 1 MHz offset at a 3 mA bias. This oscillator has a phase noise of -112 dBc/Hz at an offset of 10 MHz.

As shown in Figure 3-41, the phase noise at a 1 MHz offset decreases as the tail current increases and flattens as the tank leaves the current-limited regime. From this plot, the
minimum phase noise is -93 dBc/Hz at a tail current of 4 mA. Above this current level the phase noise increases indicating the onset of the voltage-limited oscillation regime. This compares favorably with the simulation for the phase noise variation of the individual SWO in Fig. 3-31.

![Graph showing phase noise and FOM vs bias current.](image)

**Figure 3-41: Measured phase noise at 1MHz for RWO current values and the FOM at 45 GHz.**

Additionally Figure 3-41 illustrates the FOM for the oscillator;

\[
FOM = PN - 20 \log \left( \frac{f_o}{\Delta f} \right) + 10 \log \left( \frac{P_{dc}}{1mW} \right)
\]  

The optimum operating point from the standpoint of the FOM is when the bias current for each SWO cell is chosen to be equal to 4 mA. The FOM is slightly lower than previous work (Table 3-1) but this oscillator is capable of providing multiple phases. In comparison with other works, the phase noise of the fabricated chip is higher than the rest in the price of lower power as one of the major goals of this design is to be low power. Otherwise, by increasing the oscillator power consumption, a better noise performance is achievable.
Table 3-1: Performance comparison of microwave oscillators in silicon processes.

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<th>Frequency (GHz)</th>
<th>Tuning Range (GHz)</th>
<th>Phase Noise @ 1MHz (dBc/Hz)</th>
<th>Power Consumption (mW)</th>
<th>FOM (dBc/Hz)</th>
<th>Area (mm²)</th>
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CHAPTER 4 : MULTIPLEXER AND VGA DESIGN

Variable-gain amplifiers (VGAs) are one of the important building blocks of communication systems. Particularly, in transmitters, they have been used extensively in implementation of different modulation schemes. Also, they are almost ubiquitously used in transceivers to improve the overall linearity and dynamic range. In this chapter, first different types of variable-gain amplifiers (VGAs) are reviewed. Then the design of the proposed VGA is presented. Next, the multiplexer structure that is used to choose the desired phase is explained, followed by a discussion on the design of the combined multiplexer and VGA.

4.1. Overview

In previously reported VGA designs, gain-control mechanisms are typically achieved by using ladder attenuator [77], variable transistor transconductance \(g_m\) [78], current splitting [79], feedback triode region transistor [80], and adding cascade transistor, variable load resistor, and current steering [81]. As shown in [77] and [80], attenuator and feedback transistor introduce high loss in mm-wave range. The current splitting topologies, developed by K. L. Feng et al. [79], are not suitable for low power mm-wave applications, because of their narrow gain control range and high loss in mm-wave range. Among these variable-gain mechanisms, the topology proposed in [81] has the advantages of wide and linear gain control range, low dc power, as well as simple topology, and thus is suitable for high-frequency design.

From the amplifier design point of view, different CMOS amplifier topologies such as common-gate (CG), common-source (CS), and cascode are utilized and implemented for millimeter-wave receivers including 60 GHz band [83]. The schematics in Figure 4-1 show
the CS, CG, and cascode amplifiers. The common-gate structure provides a wideband input matching with good reverse isolation. However, the CG noise figure is larger than the noise figure in the CMOS CS or cascode amplifiers. Compared to the CS or CG topologies, the cascode topology is more stable. Higher gain can be achieved in cascode topology, but the noise figure is higher due to the additional noise introduced by the cascode transistor. In fact, the cascode topology can be considered as cascaded combination of CS and CG stages.

![Figure 4-1: Different CMOS amplifier topologies (a) common source (b) common gate (c) common gate cascode amplifiers.](image)

As mentioned before, different VGA topologies that have been investigated in the literature. One way to control the gain (i.e., $g_m$) is by changing the bias current of the transistor, as shown in Figure 4-2(a). Reducing the tail current lowers the $g_m$ of the differential pair and consequently the gain of the stage. Reducing the tail current source causes the voltage drop across the load to decrease and thus changes the output common-mode voltage. To compensate this voltage change, additional current can be passed through the load (shown as
$I_{AGC}/2$ in Figure 4-2(a)) [82]. A drawback of this technique is that the maximum input voltage for linear operation is reduced with the reduction in the gain, which results in the lowest gain setting for the largest input signal. Another approach is to change $g_m$ via reducing the drain-source voltage by adding cascode transistors (see Figure 4-2(b)). The gate voltage of the cascode transistors, $V_{AGC}$, controls the gain. By not changing the tail current, the output common-mode voltage remains constant and the output dynamic range is less sensitive to the gain setting.

**Figure 4-2**: Four methods of controlling of $g_m$ (a) by changing the bias current (b) by adding the cascade transistor (c) a variable load and (d) a variable series feedback [82].
The third method is to change the load resistance. Since the gain of an amplifier stage is approximately equal to $R_L g_m$, varying $R_L$ changes the gain. In order to achieve a constant input range, one can use a differential variable load, as shown in Figure 4-2(c). A technical problem with this approach is the change of resistor over process (variations) which should be compensated for carefully. Figure 4-2(d) shows a differential pair with series feedback provided by the variable source degeneration resistor, $R_{AGC}$. In this example, the tail current $I_o$ is split in two halves; a single tail-current source could be connected to the midpoint of $R_{AGC}$. This stage has an approximately constant bandwidth, a constant output common-mode voltage, however, its dynamic range as the gain increases needs to be improved.

4.2. VGA Design

In the proposed VGA design, a current steering mechanism is adopted to achieve wide and linear gain control range [81]. The unit gain control cell is illustrated in Figure 4-3. $M_1$ and $M_2$ are combined as a cascode device and $M_3$ is used for gain control. To explain the variable-gain behavior, a simple analysis is given in [81] by Gopinathan et al. for calculating the current and transconductance of transistor $M_2$. The current passing through $M_2$, i.e., $i_m$, can be expressed as:

$$i_m = \left[ \frac{1}{2} + 4 \left( \frac{k_1 (V_{G2} - V_{C1})^2}{I_o - \frac{1}{4} k_1 (V_{G2} - V_{C1})^2} \right) \right] i_o$$

where $I_o$ is the current of transistor $M_1$, $k_1$ is the transconductance parameter and is equal to $\mu_n (W/L)_2 C_{ox}$. The transconductance of the current steering gain amplifier cell, $G_m$, can be express as:
\[
G_m = \frac{di_m}{dV_{in}} \approx \left[ \frac{1}{2} + \frac{1}{4} \sqrt{\frac{k_1(V_{G2} - V_{C1})^2}{I_o - \frac{1}{4} k_1(V_{G2} - V_{C1})^2}} \right] \frac{di_o}{dV_{in}} \\
\left[ \frac{1}{2} + \frac{1}{4} \sqrt{\frac{k_1(V_{G2} - V_{C1})^2}{I_o - \frac{1}{4} k_1(V_{G2} - V_{C1})^2}} \right] g_{m1}
\]

(4-2)

where \( g_{m1} \) is the transconductance of \( M_1 \). The dc current \( I_o \) remains constant during the application of gain control bias when \( M_2 \) and \( M_3 \) are operating in the active region. The current \( i_m \) is controlled by the gain control bias \( (V_{C1}) \) based on equation (4-2), while \( G_m \) and the small-signal gain of the VGA are controlled by \( i_m \).

Figure 4-3: The current steering gain amplifier cell.

To achieve the maximum gain performance, appropriate channel width to length ratio \( (W/L) \) for the transistors should be chosen.

In the high-gain mode, the gate voltage \( V_{C1} \) of the gain control transistor, \( M_3 \), is biased below the threshold voltage to keep it off. While the gain control transistor is off, \( i_m = i_o \). The current
$i_m$ flows through the CG and CS transistors ($M_2$ and $M_1$) which are biased in active region so that the VGA is operating in the high gain mode. When $V_{C1}$ of the gain control transistor goes high, $M_3$, is turned on. According to equation (4-2), as $V_{C1}$ increases the transconductance ($G_m$) decreases, and thus the gain of the current steering gain amplifier cell decreases. To ensure that the CG transistor can be turned off, i.e., $i_m = 0$. The size of the gain control transistor is selected to be larger than that of the CG transistor. All networks are conjugate matched to achieve the maximum gain.

4.3. Multiplexer

Each SWO stage is loaded with an output buffer (shown in Figure 4-4) to isolate the oscillator core from a differential 8-to-1 multiplexer. The multiplexer is implemented in two stages; the first stage is a 4-to-1 multiplexer implemented with four differential pairs and NMOS cascode transistors. The second stage is a 2-to-1 multiplexer to select the differential output phase. To drive the 50-$\Omega$ output impedance, the phase selector output is buffered by a differential 50-$\Omega$ driver.

As previously mentioned, all eight phases of the LO should be accessible separately. In order to minimize the complexity of the phase-selection circuitry, the appropriate phase of the LO for each path is selected in two steps. The idea is to sense multiple phases by means of differential pairs, choosing each pair by non-overlapping pulses. As a result, the output signal is equal to one of the input pairs at the time. Initially, an array of four differential pairs ($M_1$-$M_2$) with switchable transistors ($M_3$-$M_4$) at the load of each 2-to-1 multiplexer and a shared tuned load ($\lambda/4$ transmission line) are used to select one of the four output pairs of the oscillator by using one of the select bits (sel[0:3]) (Figure 4-4(a)).
The designed multiplexer for the first chip is as shown in Figure 4-4(a) which is designed and fabricated in a BiCMOS technology. For the second chip, the entire transmitter circuit is implemented in a CMOS technology and all BJT transistors are replaced by CMOS transistors.

In the basic mode of operation, at any given time, one of the LO phases is fed to the output of the main analog multiplexer, while other phases are fed to the output of the unused multiplexer. In the next step, a 2-to-1 multiplexer selects the sign bit (Figure 4-4(b)), resulting in complete access to all LO 8 phases by choosing either the select bit number 4 or 5. The above-mentioned configuration reduces the necessary number of phase selectors (i.e., differential pairs in our case) from $2^3$ to $2^2+2$ for each path. Adding a cross-coupled differential pair at the output of the multiplexer can partially cancel the loss associated with the transmission line outputs at the expense of higher power consumption. Phase interpolation
can be achieved by turning on more than one switch transistor at any given time, forcing the output to be the sum of all the turned-on phases. A first-order interpolation can be achieved by turning two adjacent paths ON simultaneously, doubling the phase resolution. Thus, there is a possibility of getting more phases than the eight original phases produced by the LO.

![Diagram of 8-to-1 BiCMOS multiplexer layout]

**Figure 4-5: The 8-to-1 BiCMOS multiplexer layout.**

The layout of the multiplexer is shown in Figure 4-5. The 4-to-1 multiplexer is drawn on top to fit interior of the RWO to save area. All the lines drawn from 4-to-1 multiplexer to the 2-to-1 multiplexer are modeled by transmission lines to make sure of the required frequency operation.
A number of simulations have been done on the designed polar oscillator in Cadence. Applying two different control gate voltages to the current steering transistor, two levels of gain are achievable for each VGA cell as shown in Figure 4-6 (note that for VGA with two such stages in cascade for levels of gain are achieved). If needed (e.g., for higher-order QAM systems), more levels of gains can be achieved by changing the control voltage of the VGA.

![Figure 4-6: Post-layout simulation for one VGA cell.](image)

As a proof-of-concept, a 16-QAM polar transmitter (four-level gain) is implemented. To apply different gains on each phase, a current steering gain structure \((M_5 - M_6)\) is added to the multiplexer to make a combined multiplexer and variable-gain amplifier (see Figure 4-7). By choosing different values for \(V_{C1}\) and \(V_{C2}\), different levels of gain are applied to the output signal.

4.4. Summary

This chapter is started with a brief explanation on different VGA structures followed by the multiplexer structure. Also it is explained how the combined structure of VGA and multiplexer is used in this research. The multiplexer is implemented in BiCMOS for the first
fabrication and all in CMOS for the second fabrication (Figure 4-7). The high gain benefit of using BJT is given in the price of more integration. The effort to reduce the number of transistors is taken to decrease the total noise of CMOS multiplexer.

Figure 4-7: 8-to-1 multiplexer including a 4-to-1 to select one of the four differential output of the oscillator, and a 2-to-1 multiplexer to select the sign.
CHAPTER 5 : MEASUREMENT RESULTS

5.1. Overview

In this chapter, the measurement results of the two chips designed and fabricated during the course of this research are presented. The first chip, explained in Chapter 3, is designed in a BiCMOS technology and includes the proposed RWO oscillator and an 8-to-1 multiplexer. It operates at 45 GHz, providing eight different phases. To implement the entire polar transmitter plus improving the level of integration and adding more functionality, the transmitter (shown in Figure 5-1) is designed and implemented in a 0.13μm CMOS technology.

The second chip extends the first chip by adding the VGA block to the circuit and also included the improvements mentioned in Chapter 3: increasing the frequency range of operation up to 5.2 GHz which is desired for 60 GHz technology. The entire polar transmitter

Figure 5-1: 16-QAM polar transmitter.
circuit based on the components discussed in the previous chapters is shown in Figure 5-1. It includes the proposed RWO and a combined 8-to-1 multiplexer with a 4-level-gain VGA.

The proposed RWO has been already explained. The distributed nature of the oscillator absorbs transistor parasitic capacitances into transmission lines. As shown in Figure 5-2, each SWO stage is effectively injection locked to the neighboring stage such that the overall structure behaves as a single oscillator.

![Image of Multi-phase rotary wave oscillator](image)

**Figure 5-2: Multi-phase rotary wave oscillator.**

As the phase noise of the oscillators is one of their most important characteristics, in comparison with the designed oscillator in BiCMOS, the following techniques are used to improve the phase noise, phase error, and tuning range of the CMOS VCO.

To minimize the phase noise, a transmission-line-based filter ($T_f$ along with parasitic capacitance at the source of $M_1$ and $M_2$, shown in Figure 5-3 (a) which resonates at $2\omega_b$ is
added in the common node of the differential pair to attenuate the second-order harmonic. This filter significantly improves the phase noise of the CMOS SWO [84]. The capacitor \( C_f \) is added to provide a low impedance path to minimize the effect of the thermal noise of the tail transistor around \( 2\omega_o \). This component of the noise contributes to phase noise when the oscillator mixer-based structure down-converts it to \( \omega_o \) [84].

Figure 5-3: Standing-wave oscillator (a) architecture, and (b) small signal model.
Although there are techniques for phase mismatch calibration in rotary-wave oscillators [69], applying such techniques to mm-wave oscillators is more challenging due to the adverse effects of parasitic capacitances on the frequency of operation. In this work, each oscillator is separately controlled to oscillate at the desired frequency and as will be shown later, a phase-offset calibration technique is applied to the last stage of the 2-to-1 multiplexer to compensate for device mismatches.

To achieve a wide tuning range, both coarse and fine tuning methods are used to cover multiple overlapped tuning sub-bands and thus covering the desired frequency range [85][86]. Figure 5-3 illustrates the designed multi-phase SWO VCO with both coarse and fine tuning circuits to cover a 5.2 GHz tuning range. An accumulation-mode varactor (Figure 5-5 (a)) is used to provide the fine tuning. For coarse tuning, the switching capacitor technique is used to achieve four overlapping frequency ranges (using control bits $B_0$ and $B_1$). Previous designs with similar RWO structure [87] have focused on fine tuning which has resulted in design trade-offs between the quality factor ($Q$), phase noise, and the tuning range. The $Q$ of the varactor has a great impact on the total phase noise of the oscillator. To maximize the varactor $Q$ (which in turn limits the tuning range of the oscillator), the minimum length varactors should be used because the varactor resistance ($R_v \propto L/W$) and capacitance ($C_v \propto WL$) are directly proportional to the length of the varactor. Based on simulations, reducing the effect of the parasitic resistor of the varactor, using a number of small varactors in parallel is better than using a large varactor.

To provide an intuitive explanation for this statement, note that a varactor is typically implemented as shown in Figure 5-5 (a). As the n-well material has a high resistivity (shown
in Figure 5-4), the series resistor of the varactor with the reversed-biased diode lower the quality factor of the capacitor.

![Varactor diagram](image)

**Figure 5-4:** Varactor realized in CMOS technology [47].

![Switched capacitor diagram](image)

**Figure 5-5:** (a) Varactor and (b) switched capacitor.

In the context of capacitor switching, it is important to consider all parasitic capacitors associated with each switch. As shown in Figure 5-5 (b), the maximum and minimum value for the switched capacitor is changing between $C_t$ when $V_{ctrl}$ is ON and $(C_{db,Ms} + C_{gd,Ms})$ when $V_{ctrl}$ is OFF.

The parasitic capacitances contributing to the output capacitance are (shown in Figure 5-3 (b)) the drain-bulk capacitance; $C_{db}$, gate-source capacitance, $C_{gs}$, and gate-drain overlap capacitance, $C_{gd}$, which is enhanced due to the Miller effect. Additionally, the output buffer differential capacitance, $C_{buff}$, loads the tank. The desired frequency tuning range is achieved
through tuning the varactor and its parasitic, \( C_{\text{var}} \) and \( C_{\text{par}} \). An equivalent differential capacitance for the tank circuit for the fine tuning is

\[
C_{\text{equ}} = C_{\text{var}} + C_{\text{par}} + C_{db} + C_{gs} + 4C_{gd} + C_{\text{buff}}
\]  

(5-1)

A large tuning range requires minimizing the capacitances that are not contributed by the varactor and suggests using smaller devices. However, a minimum transconductance, \( g_m \), is required to overcome the tank losses due to the transmission line quality factor, \( Q_{\text{TL}} \), and capacitance quality factor, \( Q_C \). Also, for the coarse tuning capacitance, shown in Figure 5-5 (b), the two different values of \( C_I + \left( C_{gd,Ms_2} + C_{db,Ms_2} \right) \) and \( 2C_I + \left( C_{gd,Ms_1} + C_{db,Ms_1} \right) \) should be considered when the \( M_{S1} \) is ON and \( M_{S2} \) is OFF and vice versa, respectively.

5.2. 16-QAM Transmitter Chip Implementation

The circuit is designed and laid out in an eight metal layer 0.13-\( \mu \)m CMOS process. The circuit includes the proposed rotary-wave oscillator, a phase selector, a VGA, and a 50-\( \Omega \) output buffer. The die micrograph of the transmitter circuit is shown in Figure 5-6, which occupies a total of 0.9 mm \( \times \) 1 mm. This includes the GSG high-frequency probe pads, three sets of DC probe pads, and the 50-\( \Omega \) output buffer. The active area of the RWO including the buffers between oscillator and phase selector is 500 \( \mu \)m \( \times \) 500 \( \mu \)m. It should be noted that the phase selector (4-to-1 multiplexer) and two levels of gain for VGA are placed inside the RWO to allow symmetric loading of each SWO and saving the area.

Since this chip is designed to operate at 60 GHz, however, the spectrum analyzer (E4448A) available to us is working up to 50 GHz. Therefore, to be able to test the chip, it is required to use a down-conversion mixer. For measuring the loss of the down-conversion mixer, a PSA
spectrum analyzer is used along with a signal generator. The connections are done with SMA cables and 1.85-mm cable as shown in Figure 5-7.

Figure 5-6: Chip die photograph.

Figure 5-7: Down-conversion mixer characteristic measurement.

To measure the total losses of the mixer and cable, the RF input amplitude is swept for a range of frequencies and the 1-dB compression point has been measured. Cadence SpectreRF is used to design and simulate the proposed circuit. A transient simulation of the RWO is plotted in Figure 5-8 which shows the output waveforms at all eight different phases of the RWO. These outputs are 45° apart from their adjacent outputs. Figure 5-9 shows the output spectrum of the transmitter. The measured output at the frequency of 67 GHz is equal to -32.5 dBm, excluding
the RF cable loss, the mixer conversion loss, and 1.5 dB loss of the probe, the RF signal level at the input of the mixer is equal to $-15.5$ dBm.

Figure 5-8: Post layout simulated outputs of RWO.

Figure 5-9: Output spectrum of the polar transmitter.

Figure 5-10 shows four levels of coarse tuning that are achieved by changing the switching capacitor block control bits from 00 to 11. Then by continuous change of the varactor, the frequency is adjusted. By this tuning, the 5.2 GHz of tuning range is achieved. Also on each coarse tuning step, the amplitude of the output will change mostly by 2.3 dBm.
Figure 5-10: Measurement tuning range for transmitter output.

Figure 5-11: Output phase noise measurement at 67 GHz.

Figure 5-11 shows the measured phase noise spectrum. At 67 GHz, the measured phase noise is -82.26 dBc/Hz and -93.49 dBc/Hz at a 1 MHz and 10 MHz offset, respectively. By excluding the phase noise of the external mixer (i.e., -14 dBc/Hz), the actual phase noise of the oscillator is -96 dBc/Hz (-106.49 dBc/Hz) at 1 MHz and 10 MHz offsets, respectively.

The polar transmitter operates from a 1.2 V supply and draws 30 mA current. The oscillator core consumes 14 mW. By changing the $V_{C1}$ and $V_{C2}$, the output amplitude level can be changed for 4 levels of gain to form a 16-QAM constellation by turning ON and OFF the current-steering transistors as control bits from 00 to 11.
The error-vector magnitude of the modulator is calculated through:

\[ EVM = \sqrt{\frac{1}{N} \sum_{i=1}^{N} (V_e^2)} \]

where \( V_e \) is the magnitude of the error vector for each symbol, \( V_m \) is the magnitude of the desired symbol vector, and \( N \) is the number of measurements. From comparing the ideal amplitude and the measured magnitude of the output spectrum, there is an error of -27.5 dB which is acceptable based on the IEEE 802.11a standard [28].

5.3. Summary

In this chapter, the measurement results for the 0.13-µm CMOS 67 GHz rotary-wave oscillator along with post layout simulations for 16-QAM polar transmitter are presented. The experimental results show that the oscillator achieves a 5.2-GHz tuning range (8%) and consumes 36 mA from a 1.2-V supply. The measured phase noise at 67 GHz is −96 dBc/Hz (−106.49 dBc/Hz) at 1 MHz (10 MHz) offset. This phase noise difference shows that the measured and post-layout simulated phase noise of the oscillator match well. Also, the EVM is -27.5 dB. The performance comparison of microwave oscillators in CMOS process and the post-layout simulation results of the polar transmitter are shown in Table 5-1 and Table 5-2, respectively.
Table 5-1: Performance comparison of microwave oscillators in CMOS processes.

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<th>Paper #</th>
<th>[69]</th>
<th>[88]</th>
<th>This Work</th>
</tr>
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<tr>
<td>Technology (nm)</td>
<td>130</td>
<td>90</td>
<td>130</td>
</tr>
<tr>
<td>Frequency (GHz)</td>
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<td>58</td>
<td>67</td>
</tr>
<tr>
<td>Tuning Range (GHz)</td>
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<td>5.2</td>
<td>5.2</td>
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<tr>
<td>Phase Noise @ 1MHz (dBc/Hz)</td>
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<td>-91</td>
<td>-96</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
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<td>8.1</td>
<td>14</td>
</tr>
<tr>
<td>Area (mm$^2$)</td>
<td>0.17</td>
<td>0.07</td>
<td>0.3</td>
</tr>
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</table>

Table 5-2: Transmitter post-layout simulation performance.

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<thead>
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<th>Parameters</th>
<th>Transmitter Simulation</th>
</tr>
</thead>
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<tr>
<td>Technology (nm)</td>
<td>130 CMOS</td>
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<tr>
<td>Frequency (GHz)</td>
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<tr>
<td>Tuning Range (GHz)</td>
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<td>Phase Noise @1MHz (dBc/Hz)</td>
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</tr>
<tr>
<td>Power Consumption (mW)</td>
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</tr>
<tr>
<td>Modulation data rate</td>
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</tr>
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CHAPTER 6 : CONCLUSIONS AND FUTURE WORK

This chapter summarizes the contributions of the research. Furthermore, the limitations of the work and avenues for future research are discussed.

6.1. Research Summary and Contributions

The growing demand for higher-rate wireless data transfer (e.g., gigabit wireless Ethernet) has resulted in a plethora of research activities in transceiver design for mm-wave bands where relatively less populated spectrum with larger bandwidths are available [1][91][98]. For example, the available 7-GHz spectrum in the unlicensed 60-GHz band provides sufficient bandwidth for high-data-rate applications such as gigabit wireless Ethernet, video distribution through mobile devices and content exchanging of compressed/uncompressed streaming data [92]. Point-to-point streaming video links for high-definition multimedia interface (HDMI) replacement have already been demonstrated at 60 GHz [1].

Mobile devices require low power consumption, placing the emphasis on energy-efficient circuits. However, modulation formats such as quadrature amplitude modulation (QAM) and orthogonal frequency-division multiplexing (OFDM) that are commonly used in high-data rate systems require more stringent phase-noise requirement (below -90 dBC/Hz @ 1MHz) for reliable operation in the 60-GHz band [96]. Unfortunately, there is a trade-off between low phase noise and low power consumption [62], [96]. Phase noise also tends to degrade with the wider tuning range required for robustness to process, voltage, and temperature variations [100]. Furthermore, for QAM-type schemes, multiphase local oscillators (LOs) facilitate frequency conversion of in-phase and quadrature RF signals.
In this work, a new architecture for a low phase noise, low power, and multi-phase oscillator is developed which hybridizes standing- and rotary- wave oscillators suitable for high-data-rate applications. This structure has been chosen to take advantage of both the low phase noise of SWO and the multi-phase accessibility of the RWO with the high $Q$ transmission line structure. During the course of this research, two proof-of-concept prototype chips are designed, fabricated and successfully tested. As a proof of performance, a mixer-less architecture for a polar transmitter is developed in CMOS technology.

The oscillator structure is suitable for generating the multi phases required in high data rate applications (for example, in the 16-QAM structure discussed in this thesis, eight different phases, 45° apart, are used). Once a wave becomes established, it takes a small amount of power to sustain it. The travelling-wave oscillator is tapped with standing-wave oscillators to sustain the wave travelling along the transmission line ring. Also, this architecture is very promising for low-phase noise systems, as any noise perturbation will be averaged out along the transmission-line ring and will result in a lower phase noise.

As a proof of concept a 16-QAM transmitter is designed and simulated (shown in Figure 6-1). The mixer-less structure has been chosen to avoid/minimize the problems associated with the mixer based transmitter. The rotary-wave oscillator is employed to provide both low power and low phase noise outputs. An 8-to-1 multiplexer along with two variable gain amplifiers (VGAs) is used to provide four different levels of gain to achieve the 16-QAM constellation.

In a Cartesian architecture, the complex output is encoded with band-limited $I$ and $Q$ vectors. Other issues with Cartesian transmitters are LO leakage, LO pulling, and imbalance of the
quadrature LO signals. On the other hand, mixer-less polar transmitters are dealing with amplitude and phase with wideband spectral properties desired in 60 GHz design.

![Figure 6-1: 16-QAM polar transmitter using the proposed RWO.](image)

The first fabricated chip includes a 45-GHz rotary-wave oscillator and is fabricated in a 0.13-µm BiCMOS technology. The phase-noise analysis predicts a maximum phase-noise reduction of 15.5 dB due to the coupling behavior in respect to non-coupled single oscillator. The oscillator draws 16 mA from a 1.2-V supply. The measured phase noise of the 45-GHz RWO is -93 dBc/Hz at 1-MHz offset. This oscillator provides a 2.9-GHz tuning range with eight outputs 45° apart. In addition to chip implementation, a comprehensive analysis on the phase noise of the oscillator has been provided.

In the second chip, a 67-GHz tunable rotary-wave oscillator is implemented in a 0.13-µm CMOS technology. The experimental results show that the oscillator achieves a 5.2-GHz
tuning range (8%) and consumes 14 mW from a 1.2-V supply. The measured phase noise at 67 GHz is $-96$ dBc/Hz ($-106.49$ dBc/Hz) at 1 MHz (10 MHz) offset.

As an application of the proposed oscillator, a 67 GHz circular-QAM transmitter topology is presented and a prototype 16-QAM system is designed and simulated in the same 0.13-$\mu$m CMOS technology. The polar transmitter draws 36 mA from a 1.2-V supply. The transmitter consumes 2 to 4× less power as compared to the other state-of-the-art 60-GHz transmitters with similar noise performance. Using a VGA, the 4-levels of output amplitude levels are achieved to form the 16-QAM constellations. Post layout simulation results show a phase noise of $-98$ dBc/Hz at 1 MHz. This phase noise difference shows that the measured and post-layout simulated phase noise of the oscillator is in excellent agreement. Also, the EVM is $-27.3$ dB.

6.2. Limitations and Future Work

There are many interesting avenues to improve the proposed architecture and make it more accurate from both design and test point of views. High-frequency testing is always challenging, in particular measuring and capturing 60-GHz signals in the time-domain requires specialized high-speed oscilloscopes which unfortunately were not available during our testing period. Due to the lack of access to such oscilloscopes, it was not possible to measure and record the physical multi-phase outputs of the oscillator. However, the functionality of the oscillator and the frequency of oscillation of its outputs were measured using a spectrum analyzer. Also, due to the limited available chip area as well as high-speed probes, we were not able to include a pad to inject high frequency injection signal to the oscillator for measuring its locking range.
Furthermore, based on the work done in this research and from a survey of recent published data, new directions for further research have surfaced that would expand the scope and impact of the limitations and future the work. Some of these ideas are discussed in below:

1) Use the proposed oscillator in a phase-locked loop (PLL) (shown in Figure 6-2) or use an injection signal to enhance the performance of the oscillator. Although these approaches have been confirmed by simulations, verification via testing would be valuable.

![PLL circuit for proposed oscillator.](image)

2) Amplitude variation can deteriorate the oscillator operation and consequently the transmitter performance, in particular in high data rate applications. This can be addressed by employing an amplitude tuning circuit. Although based on the measurement results of the oscillator chip, the amplitude variations of the proposed design are within a small range (refer to Table 2-1); however, to have a more robust design, it is required to add an amplitude tuning circuit to make sure that the transmitter EVM is acceptable.

3) One of the design considerations in differential circuits is offset calibration which can be added to the future versions of the circuit. There are different methods to measure the offset and compensate for it [69]. These methods can be applied to each stage
individually to calibrate the differential outputs of each stage. Alternatively, it can be
done at the last stage, when all offsets have been added together.

4) In this work, the focus was on circular-QAM transmitters. Looking into efficient
structures for square-QAM systems using the proposed oscillator structure would be
useful.
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Appendix:

Double-Balanced Down-conversion CMOS Mixer with On-Chip Balun for 60-GHz Receivers

Down-conversion mixers, being responsible for translating the input RF signal to an intermediate frequency (IF), are one of the key building blocks of almost all wireless receivers. In the context of spectral analysis and measurement, they can be used to down-convert a high-frequency signal to a frequency that is within the frequency range of the measurement instrument, e.g., a spectrum analyzer. In this research, although we eventually used the mm-wave measurement instruments available to us through CMC Microsystems Testing Collaboratory to test the 60-GHz oscillator designed in the course of this research, we also designed a 60-GHz down-converter mixer to have the opportunity to test the oscillator using the 27-GHz spectrum analyzer available at UBC SOC lab. Furthermore, such mixer can be used in a dual-conversion, RF phase-shifting array architecture. In this appendix, we present the design of such a mixer whose design requirements are low noise, high linearity, large LO-to-RF and LO-to-IF isolations, and moderate conversion gain.

A. Mixer Design

To achieve low noise figure (NF) performance and high SNR in the overall system, the 60-GHz mixer structure is chosen to be differential. The double-balanced structure in Figure A-1 provides a better LO-to-RF isolation compared to the single-gate mixers [101] or single-balanced mixers [102]. The LO-to-RF isolation is crucial for the successful performance of the
overall receiver especially in direct-conversion receivers or for the cases where the front-end has some gain at the LO frequency.

![Double-balanced mixer with passive baluns](image)

**Figure A-1: 60 GHz double-balanced mixer with two passive baluns.**

Also, the linearity can be improved by increasing the gate overdrive voltage. The transconductance stage transistor can be operated in strong inversion if a sufficient overdrive is obtained. The trade off in improving the linearity is to lowering the conversion gain.

The down-converting mixer in the proposed architecture provides a reasonable gain over the IF center frequency range of 11.4 to 12.8 GHz. It is needed to provide at least 2-GHz bandwidth (typical channel bandwidth) around the center frequency. For this purpose, a tunable filter shown in Figure A-1 is implemented to provide the wideband output. A varactor
is employed to provide tuning for the IF output frequency. Inductive load is used for higher conversion gain and increased headroom. At the resonant frequency of the tank, the gain becomes $g_m R_F$ ($g_m$ is the transconductance of the input transistor, and $R_F$ is the total resistance of the output tank). As mentioned in [84], $C_N$ and $T_N$ are added to improve the noise figure of the overall mixer.

Two passive baluns (Figure A-2) are used to provide single-ended to differential conversion at the RF and LO inputs of the mixer. The balun has a relatively small footprint at mm-wave frequencies ($83 \times 83 \, \mu m^2$) and is implemented in the top two metals (MA as signal layer and E1 as the ground layer). Metal width, spacing, number of turns and sizing are all optimized to provide low insertion loss and maximum voltage swing at the output port by using HFSS.

![Figure A-2: 60 GHz passive balun.](image)

B. Simulations and Measurement Results

The mixer is fabricated in a 0.13-$\mu m$ CMOS technology that has 8-metal layers (3 thin, 2 thick copper layers and 3 RF layers). An output buffer using the shunt peaking technique is implemented in order to drive the 50-Ω load of the measurement instruments. The measured results presented in this section reflect the performance of the mixer and the subsequent
buffer. For these measurements (Figure A-3) DC probes, 5C2CR probe, 5D25X probe, and Agilent E4448A PSA spectrum analyzer are used.

![Measurement Setup Diagram](image1)

**Figure A-3: The measurement setup.**

![Die Micrograph](image2)

**Figure A-4: Die micrograph of mixer chip including the PADs, buffer, and baluns.**

The die micrograph of the fabricated mixer is shown in Figure A-4. The overall system, including the two on-chip baluns, test PADs, mixer and the buffer, occupies an area of $1100 \times 746 \ \mu m^2$. Electro-static-discharge (ESD) protection has been added to all PADs. To
report the chip measurement results, the losses associated with the probes and interconnect cables should be excluded from the measured results.

Figure A-5 shows the spectrum of the mixer IF output (black curve). The output at the frequency of 12.2 GHz is equal to −44 dBm. By excluding the 7.2 dB loss of the IF cable and 1.5 dB loss of the probe, the output power at the IF of 12 GHz is equal to −35 dBm.

Also, at the RF port, excluding 15 dB loss of the RF cable and 1.5 dB loss of the probe, the RF signal level at the input of the mixer is equal to −36.5 dBm. Therefore, the conversion gain of the mixer is equal to 1.5 dB. Considering all the losses at the LO port the input LO signal is 1.5 dBm. Based on the measurement results, the IF output covers a 2.3 GHz bandwidth. The center frequency of IF can also be tuned by the varactor (gray line in Figure A-5).

Figure A-6 depicts the interpolated measured (diamonds are measured points) conversion gain variation over the IF frequency range. As shown on this figure, the IF bandwidth is about 2.3 GHz. The simulated $IIP3$ of this mixer by applying the same amplitude of RF and LO as
the measurement situation, is equal to 14.2 dBm. Moreover, the mixer core works from a 1.5-V voltage supply and consumes 6 mW. The buffer operates from a 1.3-V supply and consumes 7.8 mW. The overall chip including the buffers consumes 13.8 mW. Performance summary and comparison with recent work on mm-wave mixers are provided in Table A-1.

![Figure A-6: Measured conversion gain by sweeping LO and RF frequency by excluding the cable and probe losses.](image)

C. Conclusion

In conclusion, in the Appendix, the design of a 0.13-μm CMOS 60-GHz down-converting double-balanced mixer is presented. The designed mixer shows 1.7 dB of conversion gain at LO level of 1.5 dBm over the 2.3 GHz bandwidth at IF frequency. The $I_{IP3}$ of 14.2 dBm has been simulated for the mixer. The total chip power consumption is equal to 13.8 mW, where the mixer core and buffer consume 6 mW and 7.8 mW respectively.
Table A-1: Comparison with recent work on mm-wave mixers.

<table>
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<tr>
<th>Paper #</th>
<th>[101]</th>
<th>[103]</th>
<th>[104]</th>
<th>This Work</th>
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<td>-6</td>
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