Monolithic Integration of AlGaAs Distributed Bragg Reflectors on Virtual Ge Substrates via Aspect Ratio Trapping

by

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Abstract

Over the past two decades, researchers have devoted great efforts on Si photonics to overcome the communication bottleneck of integrated circuits. In order to realize short-reach optical interconnects, excellent performance has been achieved so far on waveguides, modulators and detectors, which use Si compatible materials (e.g. SiO$_2$, Si$_3$N$_4$ and SiGe) and processes. However, lasers on Si have been much more difficult to implement. Monolithically integrated vertical cavity surface emitting laser (VCSEL) on Si platforms are a suitable choice as output devices on Si, and is the long-term goal of this project. The research for this thesis work chose Ge/Si ART (aspect ratio trapping) substrates as the Si platform to overcome the material mismatch between AlGaAs/GaAs system and Si, and investigated the first and crucial step of successful VCSEL integration on Si platforms, which is the VCSEL distributed Bragg reflector (DBR) growth and characterization on Ge/Si ART substrates.

Three types of samples were grown and characterized to reveal the quality of DBRs and ART substrates. The results show good quality and potential for high performance VCSEL. The ART-based DBRs have reflectance spectra comparable to those grown on conventional bulk GaAs substrates and have smooth morphology. High-resolution X-ray diffraction (HRXRD) rocking curves show that the residual stress and crystal quality of the Ge films depend on oxide trench patterns. Though GaAs-DBRs have sharper satellite peaks, ART-DBRs also show good structural quality, considering the effect of more complex substrate structure with SiO$_2$, Ge and strained-Ge. The main peaks’ full-width-at-half-maximum (FWHM) of ART-DBR are about twice as GaAs-DBR’s. Transmission electron microscopy (TEM) images reveal very good periodicity and uniformity that are
unaffected by threading dislocations or residual strain. These results are very encouraging for the successful full VCSEL growth on these substrates and also confirm that virtual Ge substrates via the ART technique are effective Si platforms for optoelectronic integrated circuits.
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CHAPTER 1 Introduction

1.1 Motivation of Lasers on Silicon Platforms

1.1.1 Optics as a Possible Solution to Communication Bottleneck

In the past few decades, our patterns of life have been greatly changed by the incredible revolution in communications and computing, which is based on the advancement of photonic and electronic devices. While optical fibre-based communication has historically been used for long distances (> 100 km), they have been adopted at smaller distances for metro networks, and recently down to the 10-100 m range for very-short reach applications to replace conventional metal cables with slower speed, such as in machine interconnectivity and local area networks (e.g. fibre to the home). Besides the applications in fiber communications, optical interconnects are also under extensive research for applications in silicon (Si) based microelectronics, which is presently experiencing metal interconnect bottleneck in integrated circuits (ICs) and large scale computer systems (e.g. supercomputers), such as chip-to-chip and rack-to-rack communications (e.g., between microprocessor and memory, between multiple microprocessors and between racks), which traditionally use copper interconnects and copper cables. As device dimensions are shrinking, the metal interconnects also shrink in size. This scaling results in more RC (i.e. resistive capacitive) delay in interconnects, which slows down the speed of the whole chip and becomes the bottleneck of the system speed, known as the “interconnect bottleneck” [1,2]. It also causes signal desynchronization. Optical interconnects in supercomputers help to lower energy consumption and cost. These motivate intensive research on short-reach optical
interconnects in fibre communications and in microelectronics, which will bring many benefits and may solve the problem.

Compared with conventional metal interconnects, optical interconnects have possible practical advantages such as higher interconnect density, lower energy consumption, better clock and signal synchronization [2].

Optics avoids a key limit to the density of information that can be sent over relatively long distances. Because of the resistive loss in electrical lines, in lines without repeater amplifiers, the bit rate $B$ on electrical lines is limited to

$$B \leq B_0 \frac{A}{L^2}$$

where $A$ is the cross-sectional area of the wiring, $L$ is the length of the wires, and $B_0$ is a constant [2]. The fact that the ratio $A/L^2$ is dimensionless means that once we have filled all available space with wiring, the bit rate capacity of the system cannot be increased by making the whole system either bigger or smaller. Since optics does not have this resistive loss physics limiting it, it can be particularly attractive for relatively long lines with high data rates and limited cross-sections.

Power dissipation in information processing systems is now a major limitation at many levels. The inability to handle higher powers limits the performance of chips. When we communicate electrically, we charge up the electrical wire (whole line or a section) to at least the signaling voltage. This can consume significant energy and generate a lot of heat. Optics may be able to save energy in interconnection because it is not necessary to charge the line to the operating voltage of the link. In 2008 the best result for electrical transceivers are $\sim 2.8 – 6.5$ pJ/bit for board or backplane interconnects with a relatively ideal electrical channel [3]. At the same year, however, IBM reported 1.5 pJ/bit optical
interconnect operating at 10 Gbps (G bits per second), which employs a 990nm vertical cavity surface emitting laser (VCSEL) with high efficiency and low threshold current, and a 130nm CMOS driver [4]. This demonstrated the great potential of low power consumption for VCSEL-based interconnects.

Meanwhile, optics may be able to deliver and retain very precise timing in clocks and signals. Optical signals, including short (e.g., picosecond) pulses, do not spread substantially in propagating over the size scale of an information processing machine. Additionally, short pulses can directly deliver very precise timing edges, and could have other benefits, including reducing latency and improving signal timing [2]. Optics could also be useful for reducing the number of levels in the clock distribution tree thereby reducing clock power dissipation.

1.1.2 Integration of Photonic Devices on Si IC platform

To realize optical interconnects in shorter distance (<100 m) in short reach fiber communication, rack-to-rack, chip-to-chip and even across chip communications, we need to integrate optical devices (i.e. photodetectors, lasers, waveguides etc.) with electrical devices (i.e. transistors), such that the communication functions work with electronic circuits that generate signals to be transported by optics and process signals received from the optics.

It has been a long-term dream for the semiconductor industry to integrate photonic devices with electronic devices on a single Si platform to take advantage of the well-established low-cost silicon technology and the high speed of photonic devices. Compared to the approach where electronic circuits and optical circuits on separate substrates, the integration will increase the capacity of very-short reach optical
communications networks at a lower cost and lower power consumption, as well as provide effective solutions to the metal interconnect bottleneck in ICs and large scale computer systems [1,2, 5-9]. For example, IBM recently reported the optical interconnect for POWER7-IH supercomputer systems, which provides high bandwidth, low power consumption and low-latency connectivity for 100,000s of high-performance CPU cores [9]. This high performance opto-electronic link utilized extremely large number of high-speed VCSEL arrays which were bonded onto Si chips. Other than the above rack-to-rack communication, Intel also demonstrated a 50 Gbps optical interconnect between two microprocessor chips using four edge-emitting lasers, which were also bonded onto Si chips [10].

There generally two main approaches to integrate electronic circuits and optical circuits, namely hybrid integration and monolithic integration. Hybrid integration is to fabricate each device component separately, and then integrate them into a functional system [11-14]. This could be achieved by simply bonding individual optoelectronic devices and ICs in the same package or substrate as the IBM and Intel examples discussed above. However, in this approach the device density is low, and packaging cost is prohibitively high. An alternative approach that has been steadily gaining attention is the monolithic integration, which means fabricating optical and electronic devices simultaneously on the same optoelectronic integrated circuit (OEIC) chip. This approach could provide the advantages of high density, system reliability, increased functionality and the use of well-established low-cost Si fabrication techniques. This approach, also termed silicon photonics, aims to implement the entire collection of optical and photonic functionalities in silicon, to enable unprecedented levels of photonic integration.
There are many challenges in monolithic integration approach, as photonic and electronic devices are normally built from different materials. Photonics (optoelectronics) are made from compound semiconductors (also known as III-Vs, such as gallium arsenide GaAs, indium phosphide InP); and electronics from Si. The most challenging problem for the integration of optical communication devices with silicon electronics is the mismatch of the materials, i.e. lattice mismatch, thermal expansion coefficient mismatch and valence number mismatch, and different fabrication processing conditions. Naturally, the silicon platform is very good for passive optical components (e.g. waveguides, detectors and modulators), using Si compatible materials such as Si, SiO₂, Si₃N₄, germanium (Ge) and SiGe [1-2, 3-6, 15]. However, lasers on Si are much more difficult to achieve because Si is a poor electricity to light converter due to its indirect bandgap structure, and has not been a suitable material for efficient light emission.

Obviously, an on-chip integrable laser is an essential element in photonic circuits to emit single wavelength light signals. As most of other functions for optical interconnects can be now realized using Si and Si compatible materials, the potential photonic-electronic marriage now comes into a critical point: everything is almost ready except for the driving signal sources, which are lasers on Si platforms. Therefore, electrically pumped lasers on Si platforms become the Holy Grail and it will determine the ultimate viability of a commercial silicon photonic technology.

1.2 Review of Available Integration Methods for Lasers on Si Platforms

Considering the current technology status, lasers on Si platforms may be realized by the following five schemes:

1) Off-chip lasers that optically pumps Si Raman lasers on Si platforms.
2) Off-chip lasers that communicate with Si based ICs via fiber optics.

3) Hybrid integration of III-V lasers on Si platforms.

4) On-chip Si or Ge based lasers.

5) Directly grown III-V lasers on Si platforms.

6) Monolithically integrated electrically pumped III-V lasers on Si platforms.

Obviously, off-chip lasers (scheme 1 and 2) are not ideal light sources because they cannot satisfy the compactness and reliability requirements in today’s IC industry.

Many methods have been investigated toward obtaining on-chip Si or Ge based lasers, including rare-earth doping [16], nanocrystalline Si structures [17], and band-engineered Ge lasers [18-21]. Since III-V semiconductor compounds have been well known as efficient light emitting materials, integration of these materials on Si platform is considered as the most promising approach. In the following we will review several schemes that are being implemented for this integration.

1.2.1 Integrating III–V Materials with Si by Hybrid Bonding (scheme 3)

As lasers are typically grown on III-V substrates, the most straightforward way is to transfer the fabricated lasers onto Si. This technique is generally termed bonding, including wafer bonding [11], flip-chip bonding [9] and DVS-BCB bonding [22], et al.

Wafer bonding refers to the phenomenon where mirror-polished, flat, and clean wafers of almost any material, when brought into contact at room temperature, are locally attracted to each other by van der Waals forces and adhere or bond. For many applications, the room-temperature-bonded wafers have to undergo a heat treatment to strengthen the bonds across the interface. Wafer bonding provides a way to join together two different materials without the restriction of matching lattice constants, which is a
key issue of heterostructure epitaxial growth. Such hybrid silicon laser involves a novel
design employing InP-based material for light generation and amplification while using
the silicon waveguide to contain and control the laser [11]. Figure 1.2.1 shows the
schematic structure of such a hybrid Si laser and its cross-section scanning electron
microscope (SEM) image.

Fig. 1.2.1. (a) Schematic drawing of the hybrid laser structure with the optical mode
superimposed; (b) A cross section SEM image of a fabricated hybrid AlGaInAs silicon
evanescent laser. Reprinted with permission from [11], ©2006 OSA.
The key to manufacturing the device is the use of a low-temperature, oxygen plasma (an electrically charged oxygen gas) to create a thin oxide layer (roughly 25 atoms thick) on the surfaces of both materials. Applying heat and pressure together, the oxide layer functions as a “glass-glue” fusing the two materials into a single chip. When voltage is applied, light generated in the Indium Phosphide-based material passes through the oxide “glass-glue” layer and into the silicon chip’s waveguide, where it is contained and controlled, creating a hybrid silicon laser. DVS-BCB bonding is similar to wafer bonding but it utilizes a special polymer as bonding glue [22].

Flip-chip bonding is another way to integrate lasers. The solder bumps are deposited on the chip pads on the top side of the wafer. Then this chip is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the other chip, and then the solder is flowed to complete the interconnect. EMCORE and IBM have used this way to fabricate 850nm VCSEL and photodetector arrays [9]. Seven micron thick, 35 mm-diameter AuSn solder bumps were deposited on both VCSEL and photodetector (PD) contact pads supporting subsequent flip-chip bonding onto silicon carriers (see Figure 1.2.2).
Fig. 1.2.2. Photographs of 2x12 VCSEL array (up) and photodetector array (down) with Au/Sn solder bumps on pads. Reprinted with permission from [9], ©2010 OSA.

To integrate VCSELs with Si, other hybrid bonding approaches have also been studied and shown to be effective [23, 24]. For chip-to-chip and rack-to-rack communications, however, small size, low power consumption and a short cavity design are all critical. Hybrid bonding techniques are not volume efficient and not suitable for large scale fabrication. Thus it’s not an ideal solution for these applications.

1.2.2 Rare-Earth-Doped Si/SiO\textsubscript{2} Light-Emitting Devices (scheme 4)

Researchers have recently reported that an electrically pumped rare-earth-ion laser on Si is approaching realization [25, 26]. This p-i-n diode structure consists of a stack of very thin Si layers alternating with very thin erbium-doped SiO\textsubscript{2} layers. Carriers injected laterally into the Si films make their way into the oxide films to excite the erbium. By introducing dislocation loops into Si along with erbium implantation, room temperature electroluminescence and optical gain at a wavelength of 1.5 \( \mu \text{m} \) have been achieved. However, this approach is still facing some physical limitations, e.g. silicon is not a good host of erbium.
1.2.3 Epitaxial Ge Lasers on Si (scheme 4)

Another exciting approach is Ge based lasers by Ge-on-Si epitaxial growth. It has been shown that Ge can be band engineered by tensile strain and n-type doping to achieve efficient light emission and optical gain from its direct bandgap transition. Room-temperature direct-bandgap electroluminescence [19] and room-temperature optically pumped pulse operation of Ge-on-Si lasers [20] have been achieved recently. Figure 1.2.3 shows the emission spectra, cross-section scanning electron microscope (SEM) image of the Ge-on-Si laser and a schematic drawing of the experimental setup for optical pumping. In this Ge-on-Si laser, a thermally induced tensile strain of 0.24%, together with a phosphorous doping level of $1 \times 10^{19}$ cm$^{-3}$, allowed enhanced light emission from direct gap of 0.76 eV. However, the laser threshold is still very high, partially due to the low doping level. According to calculation using Fermi statistics, $7 \times 10^{19}$ cm$^{-3}$ n-type doping is needed to raise the Fermi level to the minimum of the direct $\Gamma$ valley, making Ge a virtual direct bandgap material [21]. However, this doping level and activation is hard to achieve due to limited dopant solubility and activation.
Fig. 1.2.3 Edge-emission spectra of a Ge waveguide with mirror polished facets under 1064 nm excitation from a Q-switched laser with a pulse duration of 1.5 ns and a repetition rate of 1 kHz. The spectral resolution of the measurement was 2 nm. The three spectra at 1.5, 6.0, and 50 μJ/pulse pumping power correspond to spontaneous emission, threshold for lasing, and laser emission. The arrow indicates the peak optical gain wavelength reported in [18]. The inset shows a cross-sectional SEM picture of the Ge waveguide and a schematic drawing of the experimental setup for optical pumping. Reprinted with permission from [18, 20], © 2009, 2010 OSA.

1.2.4 Direct growth of III-V VCSEL on Si (scheme 5)

As described in Ch 1.2.1, hybrid laser integration is not an ideal solution for chip-to-chip and rack-to-rack communications, because it is not volume efficient and not suitable for large scale fabrication. On the contrast, monolithic integration has the advantages of high density, system reliability, increased functionality and the ease of using well-established low-cost Si fabrication techniques. Several studies of monolithic integration
have been reported, however, the performance was insufficient for communication applications [27, 28].

D.G Deppe et al are among the first to investigate VCSEL growth on Si substrates [27]. In their study, epilayers of AlGaAs/GaAs were grown by MBE (Molecular Beam Epitaxy) directly on Si substrates (which were cut 3° ~ 4° off (100) towards <011>). The device was operated at room temperature using 100 ns current pulse. The measured threshold is 125 mA for device with aperture diameter of 15 μm (see figure 1.2.4).

![Spectral characteristics measured for a 15-μm-diameter AlGaAs/GaAs VCSEL grown on Si. Reprinted with permission from [27], © 1990 AIP.](image)

T. Egawa et al reported an improved device with a threshold current of 82 mA [28]. This device was grown by MOCVD on Si substrates which were cut 2° off (100) towards <011>. However, this device is tested under continuous wave (cw) condition at 150 K. Figure 1.2.5 shows it was pointed out that the degraded DBR heterointerface results in difficulties in obtaining high reflectance and room-temperature continuous-wave operation.
It is obvious that the performances of those devices are all far from today’s most VCSELs whose threshold are typically under 1 mA [29]. That is because conventional VCSELs are based on III-V compound semiconductors such as GaAs and AlGaAs. GaAs and AlGaAs have very close lattice constants ($\frac{\Delta a}{a} < 0.13\%$), however their lattice constants differ from Si lattice constant by 4.2%, and the thermal expansion coefficient of GaAs differs from that of Si by almost 50% (Table 1.1). It results in unacceptably high densities of threading dislocation defects ($>10^8$ cm$^{-2}$) in the active region of GaAs-based devices grown directly on Si [27, 28].
As discussed above, bonding (scheme 3) is not volume efficient and not suitable for large scale fabrication. On the other hand, direct growth of III-V materials (scheme 5) hasn’t approached application stage due to material mismatch. Under such a context, we chose scheme 6, which is monolithic integration of III-V lasers on Si platforms using Ge as intermediate layer. The reason for choosing Ge as buffer layer will be discussed in the following section. The laser of our choice is vertical cavity surface emitting lasers (VCSELs). Compared to edge emitting lasers, VCSELs are very suitable as output devices for optical interconnects on Si platforms. The advantages of VCSELs include high-density two-dimensional array fabrication, low-cost testing and packaging, easy fiber coupling and low power consumption [31]. Figure 1.2.6 shows a possible optoelectronic integrated circuit (OEIC) design which could fully explore the unique merits of VCSEL as array light source.

Table 1.1. Lattice constants and thermal expansion coefficients of Si, Ge, GaAs and AlAs. [30]

<table>
<thead>
<tr>
<th>Materials</th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>AlAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lattice constant at 300K (Å)</td>
<td>5.4307</td>
<td>5.6575</td>
<td>5.6532</td>
<td>5.6622</td>
</tr>
<tr>
<td>Linear coefficient thermal expansion ($10^{-6}$ K$^{-1}$)</td>
<td>2.49</td>
<td>5.8</td>
<td>5.4</td>
<td>3.5</td>
</tr>
</tbody>
</table>
Fig. 1.2.6. A schematic structure of a possible optoelectronic integrated circuit (OEIC) design using VCSEL array as light source. Figure courtesy of Dr. Nicolas Rouger.

1.3 Monolithic Integration of VCSEL on Si via ART Technique

To overcome the difficulties in GaAs/Si monolithic integration, most attention has been focused on utilizing Ge/SiGe layers as transition buffers between Si substrates and GaAs based devices, which efficiently reduced the defect density. This mainly owes to two facts: the Ge lattice constant is nearly identical to that of GaAs (also 4.2% lattice match between Ge and Si), and Ge is the most compatible material with Si because they are both group IV semiconductor elements and are miscible at any ratio. Prof. Fitzgerald’s group at MIT has pioneered the investigation of graded Ge/SiGe buffer layers [32], and they have successfully integrated Si substrate with edge emitting lasers, solar cells and III-V MOSFETs [33-35]. This technique greatly reduces the defect density to meet device quality requirement, but it needs more than 10 μm thickness between Si
and GaAs, which has similar problem of hybrid integration. The large transition SiGe buffer layer thickness is not desirable for high density integrated chip and it is hard to reduce without increasing threading dislocation due to the 4.2% lattice mismatch between Ge and Si.

To reduce the thickness of buffer layers, various techniques have been developed, such as Ge condensation [36]. In this technique, when SiGe is oxidizing, Ge atoms are rejected from the oxidizing SiO$_2$ layers and diffuse into the remaining SiGe layers. After removing the SiO$_2$ layers by wet chemical etching, SiGe layer with higher Ge concentration is achieved. However, it is hard to get good quality when Ge concentration surpasses 50% where agglomeration of Ge atoms is inevitable. Other methods such as double-amorphous buffer [37] and low/high-temperature alternating annealing process [38] are also reported but none of them could achieve a good balance between quality (e.g. threading dislocations density $<$10$^6$ cm$^{-2}$) and size ($<$1 μm).

Another approach, namely Aspect Ratio Trapping (ART) technique, is developed by Amberwave Systems [39-42], and is one of the most promising solutions so far. By introducing SiO$_2$ trenches array before Ge deposition, the threading dislocations can be trapped by the trench side walls and the total thickness can be less than 0.5μm (see Figure 1.3.1). Though higher density defects exist where Ge facets contact each other on top of trench sidewalls, improved process of 2-step growth have solved this problem and achieved large area ($>$ 4 μm$^2$) of defect free regions [41]. Direct GaAs deposition on Ge/Si ART substrates was also attempted and the result was quite encouraging. Other than the excellent balance ART has achieved, low thermal budget and simple procedure are also its benefits.
Fig. 1.3.1. Illustration and cross-section TEM images of Ge in oxide trenches showing dislocations originating at the Ge/Si interface trapped by the oxide sidewalls and defect free Ge at the top of the trenches. Figure courtesy of AmberWave Systems Corporation.

It is worth to note that the amount of anti-phase domain (APD) defects raised from GaAs/Ge interface using Ge ART on Si is dramatically reduced compared to GaAs layers grown on exact (001) Ge substrate [42]. APD normally forms between III-V compound and Ge or Si interfaces, due to the heterovalent nature of the interfaces. It is a region of a crystal where the atoms are configured in the opposite order to those in the perfect lattice system. APD formation is certainly undesirable in the epitaxial growth of III-V materials on Ge or Si substrates, as they degrade device performance and decrease the yield. To reduce APD formation, offcut substrates are normally used [43]. This problem is addressed in GaAs/Ge/Si ART substrates. SEM surface images of GaAs grown on exact (001) Ge substrate and on polished Ge/Si substrate via ART are shown in Figure 1.3.2 (a) and (b), respectively. Clearly, a commonly seen high-density antiphase disordered network appeared in GaAs grown on exact (001) Ge substrate, while very few APD defects were observed for GaAs on Ge/Si in Figure 1.3.2(b). A possible explanation for the APD reduction is related to the crystallographic growth behavior of the Ge buffer.
layer. It has been demonstrated that (113) facets are primarily formed during initial Ge growth inside the trenched area [44]. As the Ge film grows above the SiO$_2$ mask, a coalesced wavy Ge growth front is formed, and faceting orientation gradually change from (113) to (001). Therefore, in the vicinity of coalesced Ge region, the as-polished Ge surface may have miss-oriented facets in a periodically modulated fashion, which would provide equivalent off-cut surface feature and lead to suppressed APD formation in the overgrown GaAs layers.

**Fig. 1.3.2.** Surface SEM images of GaAs samples grown in the same run: (a) grown on exact oriented (001) Ge substrate and (b) grown on polished Ge/Si substrate via ART. Reprinted with permission from [44], © 2009 Elsevier.

As discussed above, ART technique is able to use a much thinner transition layer thickness from Si to Ge with low dislocation density and APD defects between GaAs and Ge interfaces. Therefore, it is a good platform for monolithic III-V/Si integration and is the choice of this work.
CHAPTER 2 ART-DBR Design and Fabrication.

A complete structure of monolithic integrated VCSEL on Si via ART technique is shown in Figure 2.1.1. A VCSEL consists of a top and bottom distributed Bragg reflectors (DBRs), and an optical gain layer sandwiched in between. Most VCSELs are based on GaAs/AlGaAs or GaAs/InGaAs material systems. In this work, the DBRs are superlattices of $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{Al}_y\text{Ga}_{1-y}\text{As}$ with different composition for efficient light reflection, and the layers with different compositions are shown with different colors in Figure 2.1.1. For a laser device to lase, light needs to travel back and forth between two reflectors with high reflectance, smooth surfaces in the designed wavelength window, such that stimulated emission can be turned on and reach enough amplification to dominate over spontaneous emission. Meanwhile, the surface morphology of bottom DBRs directly determines the optical gain and ultimate device performance. Therefore the reflectance spectrum, crystal quality and surface morphology are all very important figures of merits for DBRs. To achieve high performance VCSELs on Si platforms, we need at first demonstrate high quality DBRs on ART substrates, which is the aim of this master thesis project.

The design and fabrication of Ge/Si ART-based distributed Bragg reflectors (ART-DBR) involve two stages: 1) Ge/Si ART-substrate with a 2 micron GaAs buffer layer; 2) another 0.5 micron thick GaAs buffer layer and $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{Al}_y\text{Ga}_{1-y}\text{As}$ based distributed Bragg reflectors, which will be addressed in this chapter.
2.1 ART-Substrate Design and Fabrication

The schematic structure of the DBRs grown on Ge/Si ART substrate is shown in Figure 2.1.1. The ART substrates used in this study were based on p-type on-axis (001) eight inch Si substrates. The growth process was developed and conducted by AmberWave Systems Corporation. Here we will discuss the process briefly, and more growth details can be found in reference [45].

![Schematic structure of a complete monolithic integrated VCSEL grown on Ge/Si ART substrate with GaAs buffer layer.](image)

To have high quality Ge grown directly on Si, Silicon oxide (SiO₂) trenches and their sidewalls are used to reduce defect density due to the lattice mismatch between Ge and Si as discussed in Chapter 1. First, a thin SiO₂ layer was thermally grown on the Si substrate, followed by conventional photolithography and reactive ion etching to form different parallel trenches and waffle patterns (see Figure 2.1.2), which are designed to study the effects of oxide trench patterns on crystal quality of the subsequent epitaxial Ge and
GaAs films. The oxide trenches in all patterns are 0.25 μm wide and 0.5 μm deep. The 
SiO₂ spacer width between neighboring trenches varied from 0.25 to 20 μm for the 
parallel trench patterns, shown in Figure 2.1.2. Waffle and dash line patterns are also 
adopted here as they may trap dislocations more efficiently.

After trench patterning, 3 μm thick epitaxial Ge films were grown on the patterned 
substrates using ASM Epsilon E2000 reduced pressure chemical vapor deposition (RP-
CVD) [45]. A chemical-mechanical polishing (CMP) process was utilized to planarize Ge 
films before 2 μm GaAs buffer layers were grown in a Veeco D180 metalorganic 
chemical vapor deposition (MOCVD) reactor, which finalized the growth of the 
GaAs/Ge/Si ART substrates.

![Fig. 2.1.2. SiO₂ trench patterning of ART-substrate. The distances shown in the figure is trench spacing. All trenches are 0.25 μm wide.](image)
2.2 Distributed Bragg Reflectors Design and Fabrication

This DBR was designed to have a center of peak reflectance wavelength of 850 nm for 850 nm wavelength VCSELs. This wavelength corresponds to the bandgap of GaAs/AlGaAs system, which is typical in GaAs-based VCSELs. DBRs were grown on these ART substrates at LandMark Optoelectronics Corporation, an epitaxial foundry in Taiwan. Figure 2.2.1 shows its structure design. To have a center of peak reflectance wavelength of 850 nm for 850 nm, each DBR is designed to consist of 34 periods of n-type doped Al$_x$Ga$_{1-x}$As (x: 0.12→0.9) /Al$_{0.9}$Ga$_{0.1}$As /Al$_x$Ga$_{1-x}$As (x: 0.9→0.12) /Al$_{0.12}$Ga$_{0.88}$As, and the thickness of each layer is shown in Table 2.1. Considering the uncertainty of new substrates, we slightly increased the number of periods for the DBRs (>30 periods) to enhance its reflectance, compared to its normal design.

![Fig. 2.2.1 Schematic structure of the DBRs grown on Ge/Si ART substrate with GaAs buffer layer.](image)

---

**Fig. 2.2.1** Schematic structure of the DBRs grown on Ge/Si ART substrate with GaAs buffer layer.
Table 2.1. DBR structure design details showing DBR layer composition, thickness and doping density. Design courtesy of Wei Shi and Professor Lukas Chrostowski, the University of British Columbia.

<table>
<thead>
<tr>
<th>Thickness (μm)</th>
<th>Composition</th>
<th>Doping level (cm⁻³)</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>GaAs</td>
<td>n-3×10¹⁸</td>
<td>Buffer</td>
</tr>
<tr>
<td>0.02</td>
<td>Al₀.₁₂Ga₀.₈₈As → Al₀.₉Ga₀.₁As</td>
<td>n-2×10¹⁸</td>
<td>DBR (34 periods)</td>
</tr>
<tr>
<td>0.05</td>
<td>Al₀.₉Ga₀.₁As</td>
<td>n-2×10¹⁸</td>
<td>DBR (34 periods)</td>
</tr>
<tr>
<td>0.02</td>
<td>Al₀.₉Ga₀.₁As → Al₀.₁₂Ga₀.₈₈As</td>
<td>n-2×10¹⁸</td>
<td>DBR (34 periods)</td>
</tr>
<tr>
<td>0.039</td>
<td>Al₀.₁₂Ga₀.₈₈As</td>
<td>n-2×10¹⁸</td>
<td>DBR (34 periods)</td>
</tr>
</tbody>
</table>

The ART wafers were cut into rectangular pieces (less than 2 cm × 3 cm) from the original 8 inch ART substrates and transferred to a separate MOCVD reactor, which only has three inch size wafer pockets. As the sample stage in this MOCVD reactor rotates at the speed of 50 rpm (round-per-minute), we need a wafer holder to confine the sample position so that the sample would not move during DBR growth. Therefore, three inch Si dummy wafers with center rectangular holes were used as holders to position the ART wafer pieces in those three inch size wafer pockets. The reason for choosing Si is that its melting point (1414 °C) is much higher than DBR growth temperature (760 °C) and it produces little contamination to the reactor. We also need to match the thickness of the Si holder with the ART sample thickness such that we don’t disturb the gas dynamics in the MOCVD reactor too much. As the ART samples are from 8 inch Si wafers, whose nominal thickness is 725 microns. A common 3 inch Si wafer has a nominal thickness of
375 microns, much thinner than the ART samples. Therefore, we need customized 3 inch Si wafers with around 700 micron thickness to ensure that the gas flow is not disturbed too much by the thickness difference of the dummy holders and the samples.

These Si wafers with special thickness and the Si holders were supplied by our collaborator Professor Zigang Duan’ group from Shenzhen University, China.

The Si dummy wafers were sliced from Czochralski-grown (CZ) silicon ingot. Then they were polished to about 700 μm thick. As the Si wafers are single crystal with cleavage planes, the center rectangular holes are very hard to make by mechanical processing without breaking the wafers into pieces. Therefore a 20 Watts high power semiconductor laser marking machine was used to make these holes. Mr. Wei Shi at UBC ECE first created an image file for the center hole shape to be read by the laser marker. The laser’s wavelength is 1064 nm. The laser position movement was under precision control. The laser melts a shallow layer on the surface during each scan. As our purpose is to cut through the 700 μm thick wafer, which is far beyond the etching depth, we need to repeat laser scan many times. Meanwhile, we scanned the laser point both along cutting line and width direction to facilitate this process. Figure 2.2.2 shows an example of a cut ART wafer pieces enclosed in its Si holders.
ART substrates together with the Si holders were sent to an epi foundry company in Taiwan, LandMark Optoelectronics, for GaAs buffer layer and DBR superlattice growth. At LandMark Optoelectronics, a 0.5 μm thick GaAs buffer layer and a DBR superlattice were grown on the ART substrates together with a three inch 10 degree offcut bulk GaAs substrate (a conventional substrate for VCSELs) as a control sample. The growth conditions for each layer are shown in Table 2.2. Before growth, the wafers were cleaned by “1H2SO4 : 5H2O” solution for 20 seconds. The growth temperature was 760 °C and the gas pressure was 100 torr. The gas used in GaAs growth were H2, SiH4, AsH3 and Ga(CH3)3 (TMG) which is the preferred metalorganic source of gallium for MOCVD. During AlxGa1-xAs growth, Al2(CH3)6 (TMA) was added for providing aluminum source.
It’s worth to note that the total area of each ART sample is less than 2 cm × 3 cm, and each section is 9 mm × 9 mm. Typically, the 3~5 mm margin of a wafer has large non-uniformity. Therefore our samples for DBR growth, which are originally close to the ART wafer edge area, may also have large non-uniformity. After the growth at LandMark Optoelectronics, the wafer pieces are shipped back to UBC for characterizations.

<table>
<thead>
<tr>
<th>Layer No.</th>
<th>Structure</th>
<th>Temperature</th>
<th>Pressure</th>
<th>Gas</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GaAs</td>
<td>760°C</td>
<td>100 torr</td>
<td>H₂、SiH₄、TMG、AsH₃</td>
</tr>
<tr>
<td>2</td>
<td>34×AlₓGa₁₋ₓAs (x: 0.12 → 0.9)</td>
<td>760°C</td>
<td>100 torr</td>
<td>H₂、SiH₄、TMG、TMA、AsH₃</td>
</tr>
<tr>
<td>3</td>
<td>34×Al₀.₉Ga₀.₁As</td>
<td>760°C</td>
<td>100 torr</td>
<td>H₂、SiH₄、TMG、TMA、AsH₃</td>
</tr>
<tr>
<td>4</td>
<td>34×AlₓGa₁₋ₓAs (x: 0.9 → 0.12)</td>
<td>760°C</td>
<td>100 torr</td>
<td>H₂、SiH₄、TMG、TMA、AsH₃</td>
</tr>
<tr>
<td>5</td>
<td>34×Al₀.₁₂Ga₀.₈₈As</td>
<td>760°C</td>
<td>100 torr</td>
<td>H₂、SiH₄、TMG、TMA、AsH₃</td>
</tr>
</tbody>
</table>
CHAPTER 3 ART Substrate and ART-DBR Characterization

Good DBR optical and material properties, i.e. reflectance spectra, smooth morphology and low threading dislocation density, are essential for the operation of VCSELs. To investigate the impact of the Ge/Si ART substrates on the DBR quality, optical imaging, high-resolution X-ray diffraction (HRXRD), cross-section transmission electron microscopy (XTEM) and etch pit density (EPD) analysis were used together with optical reflectance spectra measurements. The materials analysis details and conclusions will be discussed in this chapter.

The target of this work is to build DBRs on virtual GaAs substrate on Si wafers by Ge/Si ART technique, and to have DBR properties as close as conventional bulk GaAs substrates. Therefore we investigated 3 groups of samples to compare their properties and performances, whose structures are shown in Figure 3.1.

[1] ART substrates (Figure 3.1 a);
[2] ART-DBRs (Figure 3.1 b);
[3] GaAs-DBRs (Figure 3.1 c);

Fig. 3.1. Three groups of samples used in material characterization and comparison.
In our notations, ART-DBRs refer to DBRs grown on ART-substrates. GaAs-DBRs refer to DBRs grown on conventional bulk offcut GaAs substrates, which are commonly used in 850 nm VCSELs. In our experiments, the GaAs substrates are 10 degree offcut bulk GaAs substrates (the angle between (001) and wafer normal is 10 degree). In the following sections, we will discuss the characterization details.

3.1 Optical Imaging

We used a Zeiss optical microscope for morphology observation of the ART substrates before DBR growth to check the ART trench patterns and smoothness of the substrates. The available magnification ranges from 50× to 1000×. Here the presented sample series is: JLM169, E03952, with 2 μm n-GaAs Base. As the ART substrates are grown in different batches at AmberWave, the series number is used to identify each growth batch. There is not much difference between sample series under optical microscope, except for some irregular cracking and surface impurities.

Among the 9 sections of various oxide trench patterns, the one with 20 μm trench spacing, also known as the epitaxial lateral overgrowth (ELO) section [46] shows different morphology compared with other sections with less or equal to 2 μm spacing. It shows very rough coalesced regions, which come from the epitaxial lateral overgrowth. Figure 3.1.1 shows such images of the ELO regions under 100× and 500× magnifications. The parallel lines (dark color lines in the images) are coalesced regions and are evenly distributed with 20 μm spacing (measured result). The uniformity varies from place to place.
The other 8 sections generally show smooth surfaces with parallel wavy lines (Figure 3.1.2). In our structure Ge layer is 3 μm, which is much thicker than the critical thickness for epitaxially grown Ge layers on Si. The critical thickness is defined as the thickness of a film on a lattice-mismatched substrate, above which it is energetically unfavorable to have film fully strained with its lattice coherence with the substrate [47]. In the ART substrates, the SiO2 trenches release most strain due to Ge and Si lattice mismatch. However, there is still some residue strain, and the parallel wavy morphology helps to relax the residual strain and is seen as cross hatched pattern shown in Figure 3.1.2.
3.2 Normal Incidence Reflectance Measurements

One of the most important properties of a DBR is the reflectance spectrum, which shows its reflectance as a function of incident light wavelength. In this section, we will discuss the role of DBR reflectance in VCSEL operation and our experimental results of the reflectance spectra of ART-DBRs and GaAs-DBRs. For our DBR design, we expect to see a reflectance spectrum stopband centered at 850 nm wavelength. We’d also like to see that the peak reflectance of ART-DBR is close to that of GaAs-DBR. These are the purposes of the reflectance measurements.

3.2.1 The Function of DBR in VCSELS

To explain the function of DBR and the importance of DBR’s reflectance, we need to recall the working principle of a laser, especially VCSEL working principles.

A laser consists of a gain medium (active region) inside a optical cavity, as well as a means to supply energy to the gain medium. The optical cavity of a VCSEL consists of two mirrors (also called reflectors) with $R_1$ and $R_2$ as the power reflectance of these two
mirrors. The gain medium is a material with properties that allow it to amplify light by stimulated emission. When the light travels a distance of $L$ in the gain medium, the light power will be amplified by a factor of $e^{2(\gamma-\alpha)L}$, where $\gamma$ is the optical gain factor and $\alpha$ is the optical loss factor. Considering the two mirrors, the light amplification after a round trip will become $R_1R_2e^{2(\gamma-\alpha)L}$. In a steady state, the light should recover its original intensity after a round trip, i.e. $R_1R_2e^{2(\gamma-\alpha)L} = 1$. The value of $\alpha$ depends on the materials properties and $\gamma$ is determined by the energy supply condition (e.g. electrical current injection). Therefore, for a given condition (fixed $\alpha$ and $\gamma$ value), there is a negative exponential relationship between cavity length $L$ and mirror reflectance. That means a shorter cavity length requires higher reflectance of mirrors.

For VCSEL, the active region is usually a thin slab of a few hundred nanometres in thickness, which is also the cavity length. Therefore we need mirrors with very high reflectance to compensate the low optical gain due to the short cavity length. Generally the power reflectance must be larger than 99% for a working VCSEL. The only mirrors that can provide this level of reflectance are dielectric stacks composed of multiple layers with alternating high and low index, i.e. DBR. Therefore, for successful integration of VCSELs on ART substrates, we need to have high quality DBRs on ARTs substrates with comparable power reflectivity to GaAs-DBRs, which was confirmed in our reflectivity measurements discussed below.

### 3.2.2 Reflectance Measurement Calibration Procedure

We used a Filmetrics F20 Thin-Film Analyzer to characterize the DBRs’ normal-incidence reflectance performance at room temperature (Figure 3.2.1).
In any optical system, there are many components whose characteristics vary with wavelength (e.g., the output of the light source and the sensitivity of the spectrometer). When reflectance measurements are made, only variations in reflectance vs. wavelength due to the sample are of interest and the effect from other parts needs to be subtracted. Therefore, we must perform a calibration to determine the spectral response of the system (system calibration). This is done by making a measurement of a “reference” sample which has precise known reflectance characteristics. This reference sample in all our experiments was a Si wafer, which was supplied by the equipment manufacturer.

After system calibration, we can use a special test wafer to check how well the system calibration is done. This test wafer is Si wafer coated by a thin SiO$_2$ layer (SiO$_2$ on Si wafer) whose thickness is accurately known. The test principle is based on light interference. Because of its wave-like properties, light reflected from the top and bottom interfaces of a thin-film can be in-phase or out-of-phase. Whether the reflections are in- or out-of-phase (or somewhere in between) depends on the wavelength of the light, as
well as the thickness and properties of the film. Therefore the result is characteristic intensity oscillations in the reflectance spectrum (see Figure 3.2.2). As the material properties are known, a simulation could be performed by the software and compared to the measured data. Generally, the higher “goodness of fit” means a better system calibration.

![Figure 3.2.2](image)

**Fig 3.2.2. An example of measured and simulated reflectance of SiO$_2$/Si test wafer.**

As we calibrated the system and its “goodness of fit” is reasonable, we could begin the reflectance measurements. Out of our expectation, the measured reflectance was around 110% to 125%, including the GaAs-DBR, whose peak reflectance is trusted to be 99%~100% (see the discussion in Ch 3.2.1). The measured DBRs’ reflectance was
obviously not well scaled. After thorough investigation, we believe that it is due to the sample height difference between GaAs-DBR, ART-DBR and oxide/Si calibration sample (see Table 3.2.1). By inserting 1 mm thick glass slide one by one under the silver mirror to change sample height, we found that 1 mm thick height change would induce about 5% intensity change (see Figure 3.2.3). A possible reason could be found in the operation principle of this F20 tool (Figure 3.2.4). We could see that the light path is not vertical to the sample surface. Therefore different sample height will cause different reflected light path. This could explain why absolute intensity is sensitive to sample thickness (or surface height). That means the absolute intensity should be calibrated by other approaches after system calibration.

Table 3.2.1. Nominal thicknesses of samples used in reflectance measurement.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Si reference</th>
<th>SiO₂/Si test wafer</th>
<th>GaAs-DBR</th>
<th>ART-DBR</th>
<th>Silver mirror</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness (mm)</td>
<td>0.525</td>
<td>0.525</td>
<td>0.65</td>
<td>0.75</td>
<td>5</td>
</tr>
</tbody>
</table>

Fig. 3.2.3. Sample height dependence of reflectance from silver mirror.
Usually, accurate intensity calibration needs a standard mirror (such as gold or silver mirror) with known reflectance to define the 100% reflectance for each wavelength point [48]. This mirror should have accurately known reflectance in the spectral range of interest. Special coated sample could also be used for intensity calibration, such as BK7 glass [49], if only the reflectance spectrum is known. Under such calibration procedure, the reflectance measurement accuracy could be around +/- 1.5%. Therefore, we tried to use commercial silver-coated mirror for further intensity calibration.

Our silver mirror is more than 5 mm thick but the ART-DBR and GaAs-DBR is only about 0.75 mm and 0.65 mm respectively. To achieve 1% calibration accuracy, we need a height-tuneable stage with 0.2 mm accuracy, according to the measurement result shown in Figure 3.2.3. Currently we are not able to realize it. Fortunately, the thickness difference between ART-DBR and GaAs-DBR is small (~0.1 mm) so we can compare their relative intensity within +/- 0.5% accuracy.
In this section, all reflectance data in the following figures are rescaled by intensity peak of each scan itself. When two or more scans are put together for comparison, the intensities are rescaled by the highest peak intensity of all samples. This is reasonable based on the mature DBR fabrication technique. 34 pairs AlGaAs/GaAs DBR is believed to possess more than 99.8% reflectance [50].

Accurate mirror calibration will be conducted in the future. Here we focus only on the relative intensities for comparison.

3.2.3 Reflectance Spectra Cross-Sample Uniformity

![Image](image.png)

**Fig. 3.2.5. The relative positions and size of light spots on an ART-DBR sample.**

During these measurements, we found that the reflectance spectra vary across the sample even for locations in the same section. Therefore, we checked the uniformity for each section of each sample first. The relative positions and size of the incident light spots and sample are shown in Figure 3.2.5. There are two types of results; one shows very close spectra while the other has larger non-uniformity across the section. Figure 3.2.6 shows such a comparison whose DBRs are grown on the same ART-substrate
section, but in two separate samples (sample 3 and sample 5). These two samples are located in 2 individual pockets in the MOCVD reactor for DBR growth, which is a possible reason for the growth non-uniformity of these samples. According to the epitaxial foundry LandMark Opotoelectronics, this across sample and between sample non-uniformity are within normal ranges of their MOCVD growth on conventional bulk GaAs substrates, which means that the ART-DBRs are not more non-uniform than conventional bulk GaAs substrates.
Fig. 3.2.6. ART-DBR reflectance spectra uniformity for the same trench pattern on sample 3 and 5 respectively. Sample 5 has a larger non-uniformity across the sample.
Fig. 3.2.7 shows the DBR reflectance uniformity of the control sample, which is grown on a standard offcut bulk GaAs substrate (GaAs-DBR). The spectrum deviation of the control wafer is also within ±10 nm range. This phenomenon is similar with the ART-DBR of sample 5.

Therefore, for a fair comparison, we chose relatively representative regions of each sample. We selected “k” spot for ART-DBR, which is located at the center of each...
section. As the control sample is only a piece of the 3” wafer, we selected “a”, “b”, “e” and “f” spot which is closer to center in the whole wafer, and the comparison is discussed in the section below.

3.2.4 Reflectance Spectra Comparison: ART-DBR vs. GaAs-DBR

Fig. 3.2.8 shows the normal-incidence reflectance spectra of the DBRs on the ART substrate and those grown on the bulk GaAs substrate. The spectra of the ART-DBRs have very similar shape, stop-band width and peak height as the standard GaAs-DBRs (control sample). This means the ART-DBRs satisfy the reflectance requirement. The stop-band width of the Ge/Si ART-DBRs and the bulk GaAs-DBRs are 78.1 nm and 77.4 nm respectively. This difference is within the uniformity ranges of both samples. There is a noticeable spectral shift between the two samples. The stop-band centers of GaAs-DBRs vary from 858 nm to 868 nm across the sample, while those of the ART-DBRs range from 848 nm to 860 nm, closer to the 850 nm design target. Though the reflectance spectra show a pattern dependence of the ART oxide trench patterns, the stop-band centers of most patterns are shorter and closer to 850 nm (by 10 ~15 nm) than the control sample based on bulk GaAs substrate. This implies the different properties between the Ge/Si ART substrates and bulk GaAs (e.g. thermal conductivity, offcut, air flow dynamics and size) have a small impact, if any, on the growth rate of the DBR superlattices.
Fig. 3.2.8 Normal-incidence reflectance spectra of DBRs grown on the ART substrate and on the bulk GaAs substrate. The ART-DBRs were grown on parallel SiO$_2$ trench pattern with 1 μm trench spacing.
3.3 High-Resolution X-ray Diffraction (HRXRD) Measurements

In order to compare the crystal quality between the bulk GaAs-based and Ge/Si ART-based DBRs, HRXRD ω/2θ rocking curves were measured. Peak positions used in comparison are calibrated by silicon peak position, which is 34.564 degree corresponding to a lattice constant of 5.43095 Å. This is valid for ART samples because X-ray could easily penetrate into Si substrates, which are in fully-relaxed state.

The samples observed here typically have 2 × 3 or 2 × 2 sections per sample. The samples are mounted onto glass slides using double-sided tapes. Careful positioning is necessary in every mounting because the X-ray spot size is comparable to each section of the samples. It’s important to make sure that only one section is illuminated in each scan, otherwise signals from different sections will be mixed together.

3.3.1 XRD Experiment Preparation and Setup

As each section of an ART sample (ART substrate and ART-DBR) is 8.8×8.8 mm², we should make sure that the X-ray spot size is smaller than this area and could be calibrated to target the center of pattern section. Therefore X-axis and Y-axis scan were conducted separately to determine the spot dimension in each direction using different slits and masks. The results were 2 mm and 6 mm for Y-axis and X-axis separately when choosing 0.5 degree slit and 2# mask (see Figure 3.3.1). The monochromator used here was in hybrid mode, whose accuracy is 25 arc second.
The hybrid monochromator was used for ART-substrate scan (see Figure 3.3.2(a)). It consists of a parabolic shaped graded multi layer (X-ray mirror) and a special channel-cut germanium crystal. The X-ray mirror performs a pre-collimation of the divergent beam to a quasi-parallel beam. Thereafter the $K\alpha_1$ spectral component is separated by the monochromator crystal. However, its accuracy (25 arc second) was insufficient for DBR analysis because it had a lot of satellite peaks.

**Fig. 3.3.1. X-ray spot size determination.**
Fig 3.3.2. The X-ray beam path in hybrid and 4-bounce monochromators. (a) hybrid monochromator; (b) 4-bounce monochromator.

Another type of monochromator called Bartels monochromator (4-bounce) has higher resolution of wavelength selection, thus it can provide higher angular resolution (see Figure 3.3.2(b)). The crystals have (110) surfaces and are preset for Ge (220) Cu $K\alpha_1$ reflection. Figure 3.3.3 shows the difference between 4-bounce and hybrid monochromator which were used to scan the same sample. It is obvious that 4-bounce monochromator creates much sharper diffraction peaks. Therefore 4-bounce monochromator with 14 arc second accuracy was used instead for DBR scans. The X-ray spot size of 4-bounce monochromator was much smaller than the hybrid type, thus there’s no need to check the accurate spot size. We only need to care about the X-ray spot position during initial optimization.
Fig. 3.3.3. Comparison of a hybrid and a 4-bounce monochromator. Data was collected from the same sample.

After we make sure the X-ray spot size is smaller than each section of ART samples (8.8×8.8 mm²), we should also align the sample precisely to X-ray spot. The X-ray spot has always been well aligned to project to stage center. The typical ART sample contains 6 8.8×8.8 mm² ART pattern sections and it was attach to a glass slide and mounted onto XRD stage. The glass slide was fixed by 3 locking buttons and these 3 buttons are confined in their own corresponding locking path. Fortunately, the width of locking path happens to be equal to the section side length’s projection to locking path ($\approx \frac{8.8 \text{ mm}}{\sin 30^\circ}$). This is shown in Figure 3.3.4, where the locking paths are labelled by parallel lines. Mounting the sample in such a special position, we can make sure that the X-ray spot was projected precisely to the center of ART-section side-length as indicated in the figure. In other words, we can align the X-ray spot position with sample position by this method. This procedure was carried out in every sample mounting.
Fig. 3.3.4. Illustration of XRD sample mounting and alignment procedure. (a) Principle illustration; (b) photography of ART sample on XRD stage.
3.3.2 Comparison Between ART and ART-DBR Substrates

Since the ART substrates have patterned SiO₂ and Ge in the trenches, they generate more complicated signals and overlap with DBR’s signals in X-ray scans. Therefore, we should at first differentiate the origin of each signal. The comparison between ART and ART-DBR samples could separate the DBR signals from ART-substrates.

Fig. 3.3.5. The (004) ω/2θ diffraction curves from ART substrates and ART-DBR for a before and after DBRs growth comparison. Both samples were grown on 1 μm spacing pattern section.

According to the literature lattice constants of Ge and GaAs, in the ART-substrate curve the peak at 33.03° corresponds to the 3 μm thick Ge layers and the peak at 32.99° is from
the 2.5 μm thick GaAs buffer layers. These curves have been calibrated by the Si peaks from substrate. It shows that both GaAs and Ge layers have been almost fully relaxed. The lower intensity peak at 32.88° should correspond to the Ge inside the oxide trench with lateral compressive stress, which agrees with previous report [40]. It is also observed that waffle patterns reduce the strain level for regions with the same oxide trench spacing.

3.3.3 XRD Measurements Comparison Between ART-DBR and GaAs-DBR

The comparison was used to determine the DBR quality on ART substrates compared to those on conventional bulk GaAs substrates. The comparisons of crystal plane (004) and (002) ω/2θ diffraction between ART-DBRs and GaAs-DBRs are shown in Figure 3.3.6 and Figure 3.3.7 respectively. As the GaAs-DBRs don’t possess a Si peak for calibration, the curves are arbitrarily aligned in x-axis and angles are converted to seconds.

The main peaks’ full width at half maximum (FWHM) of ART-DBR are about twice as GaAs-DBR’s (labeled in figures). Though GaAs-DBRs have sharper satellite peaks, ART-DBRs also show good structural quality, considering the effect of various signal source (e.g. SiO₂, Ge and strained-Ge). As X-ray penetrates GaAs, Ge, SiO₂ layers and top of Si substrates, a more complex substrate gives broader peaks. The existence of satellite peaks confirmed the smoothness and periodicity of ART-DBRs, and no wavy morphology after 4.4 μm’s growth. This result is confirmed by TEM in Ch. 3.4. The superlattice period of GaAs-DBRs calculated from the DBR superlattice XRD fringes was 134.9 nm, slightly thicker than the designed value 129 nm.
Fig. 3.3.6. (004) $\omega/2\theta$ rocking curves comparison between Ge/Si ART-DBRs and GaAs-based DBRs.

Fig. 3.3.7. (002) $\omega/2\theta$ rocking curves comparison between ART-DBRs and GaAs-DBRs.
3.3.4 Pattern Dependence of ART-Substrate and ART-DBR

As stated in section 2.1, different oxide trench patterns are used to investigate Ge and GaAs epitaxial layer quality dependence on the oxide trench patterns. To find the pattern dependence, we measured and plotted the \( \omega/2\theta \) rocking curves of different sections together for comparison. Figure 3.3.8 shows 5 example curves from ART-substrates. There are two major differences between the XRD curves of these sections: (1) the extent of separation for GaAs and Ge peaks; (2) the width, height and position of strained Ge peaks.

![Graph showing rocking curves](image)

Fig. 3.3.8. (004) \( \omega/2\theta \) rocking curves of 5 ART-substrate sections with different oxide trench patterns. It shows ART-substrate pattern dependence.
For ART-DBRs, similar comparison is presented in Figure 3.3.9. We can see some differences in the satellite peaks. However, the strained-Ge peak seems to be shadowed or merged into satellite peaks. The stress also shifts the overall peak positions.

![ART-DBR sections](image)

Fig. 3.3.9. (004) $\omega/2\theta$ rocking curves of 5 ART-DBR sections with different oxide trench patterns, which shows ART-DBR pattern dependence.

3.3.5 ART-Substrate Sample-to-sample Uniformity Measurements Using XRD

Cross-sample uniformity was discussed in Ch. 3.2.3. Sample-to-sample uniformity was also checked. X-ray diffraction from (004) peaks were scanned for sections with the same oxide trench pattern but on different samples (Figure 3.3.10). The three samples were cut from the same wafer, i.e. they were fabricated in the same run, so the only difference is position. We see the GaAs/Ge peaks show slight deviations in terms of
shape and position. The peak position shifts about 0.02 degree at most, which corresponds to 5% relaxation (see discussion in Ch. 3.3.7). The Si peaks (used for peak position calibration) also show deviations in peak intensities. This non-uniformity should mainly result from fabrication deviation. Cross-sample uniformity was not checked by XRD since the X-ray spot size is too large and is difficult to be accurately positioned on samples.

Fig. 3.3.10. X-ray diffraction from (004) peaks were scanned for ART sections with the same oxide trench pattern but on different samples.
3.3.6 Dependence on XRD Incident Beam Direction

As reported previously, X-ray analysis of ART samples could show beam orientation dependence, i.e. difference between diffraction along trenches vs. parallel to the trenches, when unoptimized procedure was used in fabrication [40]. Therefore, we also checked the effect of incident beam direction. Figure 3.3.11 shows the X-ray incidence in two directions. For parallel and dashed trenches, one incidence comes along the trench while the other is normal to the trench wall. For waffle pattern they are symmetrical.

![Experimental configuration to investigate incident beam direction dependence.](image)

Fig. 3.3.11. Experimental configuration to investigate incident beam direction dependence.

Two typical examples are shown in Figure 3.3.12. The dependence of X-ray incidence beam direction varies from section to section. A possible major difference is
the overall peak shift. The peak shift (≈ 0.6 degree) corresponds to 15% relaxation. It suggests that the strain state is different in two directions. The peak shape and width are also different to some extent. In Figure 3.3.12(b), it is obvious that the peak is broadened when \( \Phi = 90 \) degree. The difference is smaller in Figure 3.3.10(a), which shows almost identical pattern. This result is similar with previous report [51], which conducted detailed investigation on the strain state of Ge in SiO\(_2\) trenches. It shows that the broadened peaks must be related to the coalescent Ge layer above the SiO\(_2\) trenches.

![Graph](image)

**Fig. 3.3.12.** Dependence on XRD incident beam direction. Two typical samples are shown.
3.3.7 XRD Simulation

As a complement, X’pert Epitaxy software was used to simulate the ω/2θ rocking curve of our samples. This will help us understand the experiment data and find out the origins of various signals. In simulated structure, each grading layer is constructed by 5 layers of constant composition. The compositions of these 5 layers are linearly changed, e.g. Al$_{0.9}$Ga$_{0.1}$As/ Al$_{0.8}$Ga$_{0.2}$As/ Al$_{0.7}$Ga$_{0.3}$As/ Al$_{0.6}$Ga$_{0.4}$As/ Al$_{0.5}$Ga$_{0.5}$As. Due to the limitation of software, this simulated structure is slightly different from design structure shown in Table 2.1.

Fig. 3.3.13 shows the comparison of simulation result and experimental data on GaAs-DBR, for both (004) and (002) peaks. The broadened peaks show that the material quality is not perfect. The positions of each satellite peak match well and the relative intensity is also similar. However, we can still see that the period of satellite peaks from experiment data are slightly smaller than simulation result, which means the fabricated DBRs are thicker than design structure. It agrees with the conclusion at Ch. 3.3.3, which indicates that the measured DBR superlattice period is 134.9 nm while it was designed to be 129 nm.

This simulation is not conducted for ART-DBR because the SiO$_2$ trench structure could not be built in software, which only simulates layered structures.
Fig. 3.3.13. Comparison of simulation result and experimental data on GaAs-DBR, for a) (004) and b) (002) peaks.
As described in Ch. 3.3.2, residual stress still remains in the structures. Then it is useful to get an estimation of the stress state from peak positions in XRD rocking curves. To relate the peak positions and the degrees of relaxation in Ge, we simulated (004) peak positions from full-strained Ge to full-relaxed Ge (Figure 3.3.14). This structure is made only for display convenience. We could see that for the 75% strain relaxation, the Ge peak will shift 0.1 degree (in terms of Omega) from the position of the 100% relaxed Ge peak, which is the case of the Ge peak position in Figure 3.3.5.

Fig. 3.3.14. The simulated (004) peak positions from full-strained Ge to full-relaxed Ge. The above part is the simulated structure.
3.4 Cross-Section Transmission Electron Microscopy (XTEM)

XTEM is a direct way to check the DBR layer smoothness, uniformity and periodicity. Therefore we conducted a TEM imaging for ART-DBR on 1 μm spacing pattern section.

3.4.1 Instruments and Procedures for XTEM Sample Preparation and Imaging

The XTEM samples were prepared with the help of Dr. Ting-Chang Chang from National Sun Yat-Sen University, who was a visiting scholar of our group in 2010. ART-DBR XTEM sample was directly cut from ART-DBR sample by focus ion beam (FIB) using a SMI 3050 two-beam system (SEM/FIB). The FIB resolution is 4 nm and the XTEM sample was less than 0.1 μm thick. Figure 3.4.1 shows an example of XTEM sample cut from substrate using FIB.

![Fig. 3.4.1. An example of XTEM sample cut from substrate using FIB. (a) side view; (b) top view. Figure courtesy of Dr. Chang-Ting Chang.](image-url)
Sample imaging was conducted using Hitachi H-800 TEM in our department at UBC. The operation voltage is 200 kV. The ART-DBR TEM sample was loaded on two-axis sample holder which enabled orientation in all directions. TEM image was exposed to black-and-white photographic film, developed in dark room and then scanned to digital image.

3.4.2 TEM Imaging for ART-DBR

XTEM images of Ge/Si ART-DBRs are shown in Figure 3.4.2(a). It reveals good periodicity and uniformity that are unaffected by threading dislocations or residual strain in the Ge transition layer. The DBR superlattice keeps a uniform thickness period from GaAs layer to sample surface. A corresponding higher resolution image of the DBRs in Figure 3.4.2 (b) shows abrupt and smooth interfaces between the alternating layers.

No dislocations are found within the TEM imaging area. As the dislocation density of ART-substrate is on the order of $10^6 \text{ cm}^{-2}$, which was measured using etch pit density discussed in the next section, statistically there is only about one dislocation within TEM sample range. This is estimated as follows:

$$10^6 \text{ cm}^{-2} = 10^{-2} \mu m^{-2} = 1 \times (10 \mu m)^{-2}$$

This shows that there’s about 1 dislocation in every $10 \mu m \times 10 \mu m$ area. Our TEM sample size is about $(10 \mu m \times 100 \text{ nm}) \times 20 \mu m$, in which the $20 \mu m$ side was in growth direction and $10 \mu m \times 100 \text{ nm}$ was on wafer plane. Therefore it is hard to find dislocations within TEM sample imaging range.
Fig. 3.4.2. XTEM images of ART-DBR at two different magnifications.

The TEM images in Figure 3.4.3 shows the complete structure of an ART-DBR. In the full structure image we could see clear and smooth interfaces between neighbouring layers. As this sample is very large (20\(\mu m\) depth during FIB cutting), it is hard to keep a uniform thickness over the entire sample area. Therefore lots of thickness fringes exist in the full structure. Actually the above local image was carefully tuned and the selected imaging area was relatively free of thickness fringes.
3.5 Etch Pit Density Measurements (EPD)

Etch pit density (EPD) analysis is a common way to measure threading dislocation density of semiconductors by using chemicals that etch dislocations preferentially. Bulk GaAs substrates commonly have an EPD of $10^5$ cm$^{-2}$. EPD analysis was conducted on Ge/Si ART substrates before DBR growth. To etch the GaAs layer on top of ART substrates for dislocation etch pit delineation, several solutions have been tried [52], such as HF:HNO$_3$:H$_2$O, AgNO$_3$:HNO$_3$:HF, until a good result is obtained using
H$_2$O:AgNO$_3$:CrO$_3$:HF solution. The original reported composition is 2 ml: 8 mg: 1 g: 1 ml [53]. Here we used dilute AgNO$_3$ solution instead. We found that more HF solution is preferred in our experiments, so the optimized HF content is doubled.

Nomarski or differential interference contrast (DIC) microscopy was conducted to measure dislocation density. EPD counted under a Nomarski microscope ranges from 10$^5$ to 6×10$^6$ cm$^{-2}$ for ART substrates with different patterns, which agrees with previous report [54]. Figure 3.5.1 to Figure 3.5.3 shows 3 examples with different etch pit density. This result indicates that oxide trenches with different pattern in the ART-substrate show different dislocation trapping ability. Systematic investigation on the pattern dependence of dislocation density has not been done due to the lack of samples for destructive EPD testing.

The large bubbles distributed on the sample surface are due to adhesive dust particle as these samples have been exposed to non-cleanroom environment for XRD experiments before EPD tests.
Fig. 3.5.1. Optical microscopy image of an ART-substrate after etching. EPD is $1 \times 10^5 \text{ cm}^{-2}$. Etching time is 50 seconds.

Fig. 3.5.2. Optical microscopy image of an ART-substrate after etching. EPD is $3 \times 10^6 \text{ cm}^{-2}$. Etching time is 50 seconds.
Fig. 3.5.3. Optical microscopy image of ART-substrate after etching. EPD is $6 \times 10^6$ cm$^{-2}$. Etching time is 20 seconds. To avoid etch pit overlapping, etching time is reduced in this section.

EPD analysis is not suitable for DBR wafers because each solution is effective only for a certain range of composition. However, each DBR period contains a grading layer whose Al:Ga ratio varies from 0.12:0.88 to 0.9:0.1. So far, no single solution has been found to etch over such a wide range of composition. Therefore we could only use the ART substrates’ dislocation densities to represent the ART-DBRs’ quality. This is reasonable under most conditions and actually the ART-DBR could have even less dislocations when optimized deposition procedure is applied.

As reported previously, dislocation densities measured by EPD are typically within 30% to 50% of the actual threading dislocation densities (TDD) [55, 56]. Thus the actual TDD of ART-substrates should be $3 \times 10^5$ cm$^{-2}$ to $2 \times 10^7$ cm$^{-2}$. Since these dislocations are
populated in specific directions [57], it’s possible to select relatively dislocation free regions for VCSEL active regions. P.J. Taylor et al has reported that 2.1 meV was measured in 4 K photoluminescence spectra from a GaAs-on-Si structure with TDD of $3 \times 10^6$ cm$^{-2}$ [58]. G. Balakrishnan et al reported a threshold current density of 0.1 mJ/cm$^2$ from GaSb VCSEL on Si with average TDD of $8 \times 10^5$ cm$^{-2}$ [59]. Therefore, the sections on the ART-substrates with lower TDD counts should be able to satisfy the requirement for VCSEL fabrication in terms of dislocation density ($\sim 10^6$ cm$^{-2}$).

### 3.6 Chapter Summary

Three types of samples are characterized to reveal the quality of DBR on ART substrates. The results show good quality and potential for high performance VCSEL.

1. The reflectance spectra of the Ge/Si ART-DBRs have very similar shape, stop-band width and peak height as the standard GaAs-based DBRs. This means the ART-DBRs are as effective mirrors as GaAs-DBRs.
2. Though GaAs-DBRs have sharper satellite peaks, ART-DBRs also show good structural quality, considering the effect of more complex substrate structure with SiO$_2$, Ge and strained-Ge.
3. XTEM images of ART-DBR reveal good periodicity and uniformity that are unaffected by threading dislocations or residual strain.
4. The dislocation densities measured by EPD ranges from $10^5$ to $6 \times 10^6$ cm$^{-2}$ for sections with different patterns. Some sections of the ART-substrate satisfy the device requirements in terms of dislocation density.
CHAPTER 4  Conclusions and Suggestions for Future Work

4.1 Conclusions

Over the past two decades, researchers have devoted great efforts on Si photonics to overcome the communication bottleneck of integrated circuits and the network. Excellent performance has been achieved so far on waveguides, modulators and detectors, which use Si compatible materials (e.g. SiO$_2$, Si$_3$N$_4$ and SiGe) and processes. However, lasers on Si have been much more difficult to implement. Monolithically integrated VCSELs on Si platforms are a suitable choice as output devices on Si, and is the long-term goal of this project. The research for this thesis work chose Ge/Si ART substrates as the Si platform to overcome the material mismatch between AlGaAs/GaAs system and Si, and investigated the first and crucial step of successful VCSEL integration on Si platforms, which is the VCSEL DBR growth and characterization on Ge/Si ART substrates.

Three types of samples were grown and characterized to reveal the quality of DBRs and ART substrates. The results show good quality and potential for high performance VCSEL. The ART-based DBRs have reflectance spectra comparable to those grown on conventional bulk GaAs substrates and have smooth morphology. HRXRD rocking curves show that the residual stress and crystal quality of the Ge films depend on oxide trench patterns. Though GaAs-DBRs have sharper satellite peaks, ART-DBRs also show good structural quality, considering the effect of more complex substrate structure with SiO$_2$, Ge and strained-Ge. TEM images reveal very good periodicity and uniformity that are unaffected by threading dislocations or residual strain. These results are very encouraging for the successful full VCSEL growth on these substrates and also confirm
that virtual Ge substrates via the ART technique are effective Si platforms for optoelectronic integrated circuits.

4.2 Suggestions for Future Work

There are a number of remaining issues to be investigated towards successful VCSEL integration on Si platforms.

1. Based on the above work, our next step is to fabrication full VCSELs on ART substrates followed by optical and material characterization. After that, the pattern dependence of VCSEL performance can be revealed and correlated to oxide trench patterns on ART substrates. Then optimization on the substrate pattern design and fabrication procedure can be feasible.

2. Lasers are known to generate large amount of heat during continuous operation at room temperature. This can greatly reduce laser lifetime if the heat cannot be dissipated in time. Therefore the thermal conductivities of laser’s substrate materials must be high enough for heat dissipation to keep lasers working. By replacing GaAs with ART substrate, we introduced 3 different materials: Si, Ge and SiO₂. Table 4.1 shows a comparison of thermal conductivities of these materials. Silicon, as the major substrate material, has better performance in heat transfer while SiO₂ is a poor heat conductor. On the other hand, SiO₂ occupies only 0.5 μm thickness in the whole structure. It’s not easy to predict the overall thermal property of ART substrates analytically. Therefore a heat conduction simulation and analysis need be done to find out how thermal property of ART substrate will affect the VCSELs’ performance.
Table 4.1. Thermal conductivities of GaAs, Si, Ge, and SiO$_2$ at room temperature.

<table>
<thead>
<tr>
<th>Materials</th>
<th>GaAs</th>
<th>Si</th>
<th>Ge</th>
<th>SiO$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal conductivity ($W \cdot m^{-1} \cdot K^{-1}$)</td>
<td>56</td>
<td>124</td>
<td>64</td>
<td>1.3</td>
</tr>
</tbody>
</table>

3. The ultimate goal of Si photonics is to implement a complete optical system on Si platforms. Therefore, less transition thickness is preferred for higher throughput and lower cost. As the first experimental demonstration, we used 5 μm thickness buffer layers for transition from Si to DBR. More investigations should be done to reduce this buffer layer thickness and fabricate more compact VCSELs.

4. Etch pit density is measured on ART substrates and the result varies a lot from section to section. However, due to the lack of systematic investigation on all sections, we are still unable to relate the dislocation density and its pattern type. This deserves a detailed investigation to fully explore the potential of ART technique.
Bibliography


