

An Ultra-Low Power SAR ADC

by

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Abstract

Wireless sensor networks are used in variety of applications including environmental monitoring, industrial control, healthcare, home automation, traffic control, and temperature and pressure monitoring systems. Many one-time use wireless micro sensor applications require ultra-low-power devices due to the limited energy capacity and lifetime of their small-size battery. Many sensor nodes require an analog-to-digital converter (ADC) to convert the analog output of the sensor to digital for storage and/or further processing. In this work, an 8-bit ultra-low-power successive approximation register (SAR) ADC is presented that operates from a low power supply voltage of 1V. The circuit is implemented in a 0.18 μm bulk CMOS technology without using any low- V_T devices. In terms of active components, this ADC requires one comparator, 18 D flip-flops, several switches, and one voltage doubler. The ADC achieves an effective number of bits of 7, while operating with a sampling rate of 100kS/s and consuming 1.4 μW from a 1 V supply.

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Chapter 1

Motivation

Analog-to-digital converters (ADCs) are ubiquitous blocks that are used in almost all electronic systems to convert physical analog signals to digital data. Often, an ADC is accompanied with a digital signal processor (DSP) to further process and manipulate data in the digital domain. Current trends are to implement as much as the signal processing as possible in the digital domain. Due to the relatively low cost of transistors and digital logic in CMOS, this has made CMOS technology a prime candidate for circuit implementation. In the past, many researchers have focused on developing new ADC architectures such as delta-sigma [1] and pipeline converters [2], which aim to push the performance limits of ADC in terms of resolution, speed, and power. Recently, there has been increasing interest in ultra-low power ADCs for use in battery powered or self-sustaining systems such as wireless sensor network [3, 4].

Potential applications of ultra-low-power ADCs are quite diverse: industrial monitoring, home appliance control, wildlife population tracking, weather pattern prediction, hearing aids, micro-robotic systems, and tire pressure monitoring system (TPMS), to name a few. In large scale wireless sensor networks, power management is important because many one-time use wireless micro-sensor nodes require ultra-low-power devices due to the limited lifetime of their battery [5]. The average life time for a 1 cm³ Lithium battery continuously supporting 100 μ W power is one year [6]. It is also possible to use energy harvesting

techniques to create a self-sufficient system, as long as the power requirement of the electronic circuitry is low enough. To satisfy these ultra-low power requirements, sensor network nodes must leverage both low cost CMOS device and micro-electromechanical system (MEMS) technologies in order to integrate sensors, DSP, communication blocks, and energy sources into one ultra-low-power miniature sensor node.

The ADC presented here is aimed for general wireless sensor network applications and in particular for use in TPMS. In such applications, the ADC is the interface block between the environmental sensor and the processing unit. In these systems, not only the power consumption and standby power are critical, but also the performance of the ADC in terms of the required resolution is important. This work describes the design and implementation of an 8-bit successive-approximation register (SAR) ADC in a $0.18\text{ }\mu\text{m}$ CMOS technology. The target supply voltage for this design is 1 V and the circuit performance and power consumption are achieved without using any low- V_T devices. This work is based on the thesis work done by M. Scott [7]. The major differences between this work and Scott's work are the use of the metal sandwiched capacitors instead of poly-to-poly capacitor (as poly-to-poly capacitors are not available in the $0.18\mu\text{m}$ CMOS technology targeted in this work) the floorplan of the capacitor array, and the voltage doubler.

This research is intended to develop an ultra-low power ADC in a $0.18\text{ }\mu\text{m}$ bulk CMOS process. It targets an ultra-low-power of few microwatts and lower wafer cost which translate into avoiding the use of special mask layers such as low- V_T device mask or metal-insulator-metal capacitors. In this work, only the standard process is used. To achieve the goal of ultra-low power, the individual blocks in the ADC need to be as simple as possible.

The more transistors in the circuit, the more power will be consumed at the moment when the transistors are being turned on/off. Also, the power consumption is the product of supply voltage and the overall current that the circuit draws from the supply. Consequently, lowering the power supply would be beneficial to for reducing the overall power consumption.

1.1 Organization of the Thesis

This thesis is organized as follows: first, Chapter 2 gives an overview of an ideal ADC and briefly discusses its fundamental limitations. Next, Chapter 3 discusses the ADC architecture used in this work, design flow and the circuit design of individual blocks of the ADC. This chapter also analyzes the circuit design of each individual component. Chapter 4 explains the evaluation of the ADC and provides the test and measurement results from the fabricated chip.

Chapter 5 explores some important layout techniques used in this design and discusses the potential latch-up issues that might damage the circuit and techniques to minimize the possibility of latch up. Finally, Chapter 6 presents concluding remarks and suggestions for future work.

Chapter 2

Background

ADCs are the interface block between the analog and the digital domains. Among the important trade-offs in an ADC, is that of between speed and accuracy. The choice of an ADC architecture depends on the application and the requirements of the overall system. In addition, each architecture has its own limitation on different performance criteria, such as speed, power, and area. Nowadays, power consumption is one of the important design specifications in almost all applications. A good understanding of the fundamental limits of ADCs is necessary to achieve an ultra-low-power design. These fundamentals are overviewed in this chapter.

2.1 Ideal A/D Converter

An ideal A/D converter has an analog input (V_{in}), reference signal (V_{ref}), and digital outputs (B_{out}), as shown in Figure 2-1. In most ADCs, a voltage quantity is used as an analog input rather than a current quantity partly because it is usually easier to compare and store voltages. However, some ADCs still use current quantities [14].



Figure 2-1 An ideal A/D converter block diagram

The relationship between an analog input, reference signal, and digital outputs can be presented as the following equation:

$$V_{in} = V_{ref} (b_1 * 2^{-1} + b_2 * 2^{-2} + b_3 * 2^{-3} + \dots + b_N * 2^{-N}) \quad 2-1$$

where, b_1 is the most significant bit (MSB) and b_N is the least significant bit (LSB). The voltage change that corresponds to the minimum step size change at the output of the ADC is defined as V_{LSB}

$$V_{LSB} = \frac{V_{ref}}{2^N} \quad 2-2$$

A 2-bit ideal A/D converter transfer characteristic is presented below.

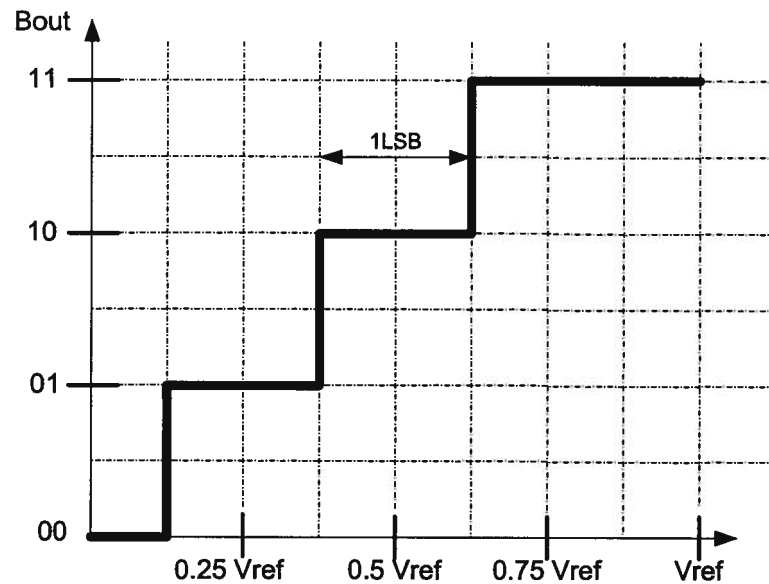


Figure 2-2 Transfer function of an ideal 2bit ADC without quantization error

Any deviation from the nominal input values that produces the same digital output is referred to as the quantization error. In other words, the difference between the original analog input and the confined digital output is called quantization error, ϵ_q . Note that quantization error only exists in an ADC. There is no occurrence of quantization error in a digital-to-analog converter (DAC) because the output is well defined by specific input bit values. The detail of quantization noise will be discussed in section 2.2.

2.2 Quantization Noise

The digital outputs of an ADC represent quantized values of a continuous input signal. The difference between the actual analog value and their respective quantized value is called quantization noise.

The quantization is a “many to one” mapping. That is a specific digital output code corresponds to a range of analog input signal values. To illustrate quantization noise, the output of an ideal ADC (B_{out}) is fed to an ideal DAC so that the digital signal can be transformed back to the analog domain. The block diagram of this flow is shown in Figure 2-3.

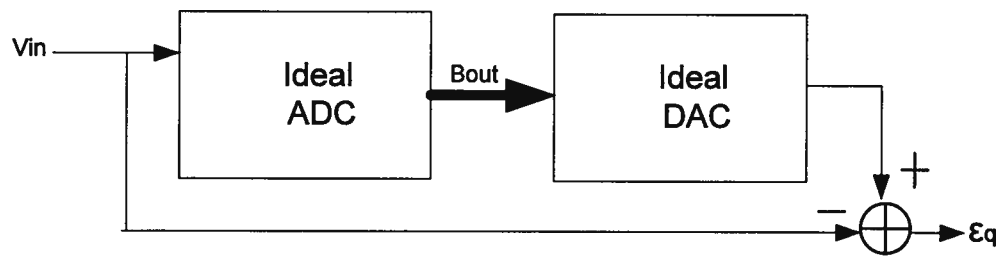


Figure 2-3 Block diagram of a circuit investigating quantization noise behaviour

When a ramp input is applied at V_{in} in Figure 2-3, the resulting output of the DAC will appear as a staircase. The quantization error, ϵ_q , is shown in Figure 2.4.

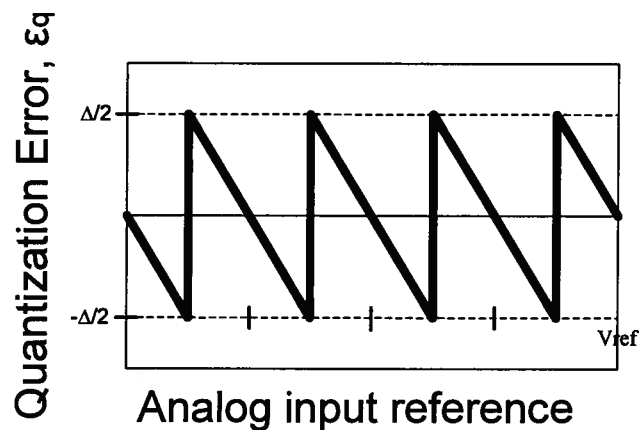


Figure 2-4 Quantization error plot with a ramp input

The level of quantization noise decreases as the number of bits of the ADC increases. The number of bits of the ADC is referred to as the ADC's resolution. Quantization noise exists in all ADCs, including ideal ADCs. Usually, the input signal range is within the conversion range, but it may go beyond or below the specified voltage range. Consequently, large errors may occur if the output is not confined to these limits.

In order to approximate the power of the quantization noise, a common simplifying assumption is that the quantization error is independent of the analog input and uniformly distributed between $-\Delta/2$ and $+\Delta/2$, where Δ is equal to V_{LSB} . Although this assumption is not always valid, it provides a reasonable approximation when the resolution of the ADC is above 4 bits. With this assumption, the total quantization noise power is given by [8]:

$$\begin{aligned}\overline{\epsilon_q^2} &= P_{QNoise} \\ &= \frac{1}{V_{LSB}} \int_{-V_{LSB}/2}^{+V_{LSB}/2} \epsilon_q^2 d\epsilon_q \\ &= \frac{V_{LSB}^2}{12}\end{aligned}\tag{2-3}$$

The full-scale signal-to-noise ratio (SNR) of the ADC is defined as the full-scale signal power in the input divided by the quantization noise power in the output. To calculate this SNR, a full-scale sinusoid input signal with amplitude of $V_{ref}/2$ is applied. Using equations 2-1 and 2-2, the input signal power is given by

$$P_{input} = \frac{V_{LSB}^2 \cdot 2^{2N}}{8}\tag{2-4}$$

Given the input signal power and quantization noise power, the SNR is

$$\begin{aligned}
 SNR &= \frac{P_{input}}{P_{QNoise}} \\
 &= \frac{2^{2N-3} \cdot V_{LSB}^2}{V_{LSB}^2 / 12} \\
 &= \frac{3}{2} 2^{2N}
 \end{aligned}
 \tag{2-5}$$

In decibels, the SNR becomes,

$$SNR = 6.02N + 1.76 \quad dB \tag{2-6}$$

This SNR is often used to evaluate the performance of a given N-bit ADC. This is the maximum SNR value that any N-bit ADC can achieve when the input is sinusoid. However, in practice, this maximum SNR cannot be achieved due to other noise sources, nonlinearities, and system limitations.

2.3 Device Noise

There are many sources of circuit noise that a designer has to take into consideration while designing a circuit. The presence of device noise is unavoidable in all real circuits. Device noise plays an important role in ADC design because it determines the performance of the ADC. Unlike the quantization noise which is a result of the analog-to-digital conversion process, a circuit designer can minimize device noise by using the appropriate circuit architecture and design. A good circuit design can minimize the power of the circuit, while achieving the desirable performance and limiting the level of the noise to tolerable amounts.

The main forms of device noise in CMOS and bipolar junction transistor (BJT) technology are thermal noise, flicker noise, and shot noise. Thermal noise exists in transistors and resistors, flicker noise and shot noise exist in all transistors and diodes with MOS transistors having higher levels of flicker noise as compared to BJTs. All of these noise sources will degrade performance and limit the achievable resolution of an ADC.

Thermal noise is the most common and major device noise appearing in most circuits because it exists in both transistors and resistors. It is found to be the small current caused by the thermal motion of the conduction electrons in the resistive channels with a random noise which will increase with temperature. Thermal noise is present in both conventional resistors and distributed gate resistance in MOSFETs [9]. Due to the property of frequency independence, thermal noise is also called “white noise” for having a uniform power spectrum.

Flicker noise is another significant noise source appearing from the random trapping of charge at the oxide-silicon interface of MOSFETs. The noise spectral density is given by [10],

$$\overline{V_n^2} = \frac{K}{WLC_{ox}} \cdot \frac{1}{f} \quad 2-7$$

where K is a process-dependent constant, f is the frequency, W is the width of the transistor, L is the gate length of the transistor, and C_{ox} is the gate oxide capacitance per unit area. The noise spectral density is inversely proportional to the gate area and frequency. Therefore, flicker noise is also called $1/f$ noise. Due to the property of inverse relationship with

frequency, flicker noise becomes the dominant noise source at low frequencies. Figure 2-5 shows a typical noise spectral density for a MOSFET [11].

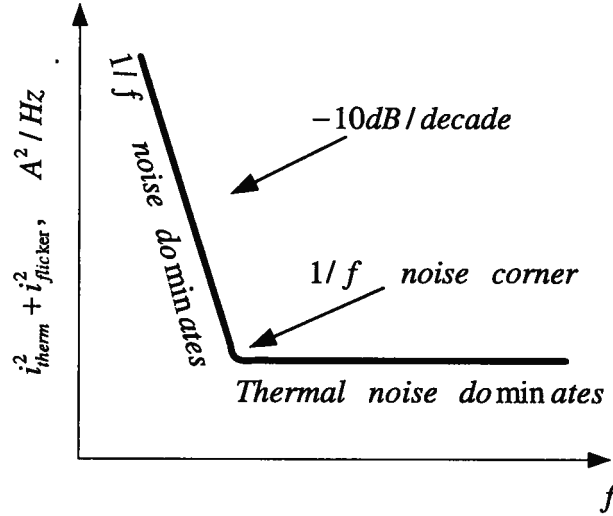


Figure 2-5 MOSFET noise

Shot noise refers to the fluctuating current that is composed of discrete charge carriers crossing the potential barrier at the semiconductor pn junction. The charge carriers can pass the barrier independently of one another at an average rate given by the direct current flow in both diode and bipolar transistors. The spectral density of shot noise is given by [12],

$$i_{no}^2 = qkI_o \quad A^2 / Hz \quad 2-8$$

where q is the electron charge, I_o is the direct current flow through the junction, and k is the constant that varies from device to device and depends on how the junction is biased. From equation 2-8, shot noise is proportional to the direct current. Like thermal noise, the shot noise has a white frequency spectrum.

In general, any type of noise source would degrade the achievable resolution of an ADC for a given amount of power consumption. While thermal, flicker, and shot noise contribute a great deal of device noise, the total ADC noise still depends on the circuit architecture and the technology which the circuit would be implemented in. In a real circuit, device noise can never be eliminated, but can be minimized with proper design. In addition to proper device sizing and biasing, there are circuit techniques to minimize noise, for example chopper stabilization [13].

2.4 Power Supply Noise

Power supply noise arises when the power supply is drifting or changing due to current/voltage fluctuation in other parts of the chip. The current fluctuations introduce voltage fluctuations across the series resistance and inductance of the bondwires and pins from the external supply to the core of circuitry. One approach to avoid the power supply noise is to design a supply independent reference voltage to be used as V_{DD} for the rest of the circuits on chip. However, power consumption and area will increase due to this extra stage. Another approach is to maximize the power supply rejection ratio of the entire system.

2.5 Other Non-idealities and Performance Limitation

In practice, there are several important non-idealities that can degrade the circuit performance due to the imperfect circuits. Some of these non ideality factors are shown in Figure 2-6: charge injection, gain, harmonic distortion, hysteresis error, settling time, clock

skew and jitter. Most of the non-ideality errors depend on the circuit architecture and implementation. Some arise from the systematic level and layout as well. For example, in amplifiers and comparators, random input offset is one of the imperfections due to the variations in the device. Process variation can be another non-linearity factor when the die is fabricated.

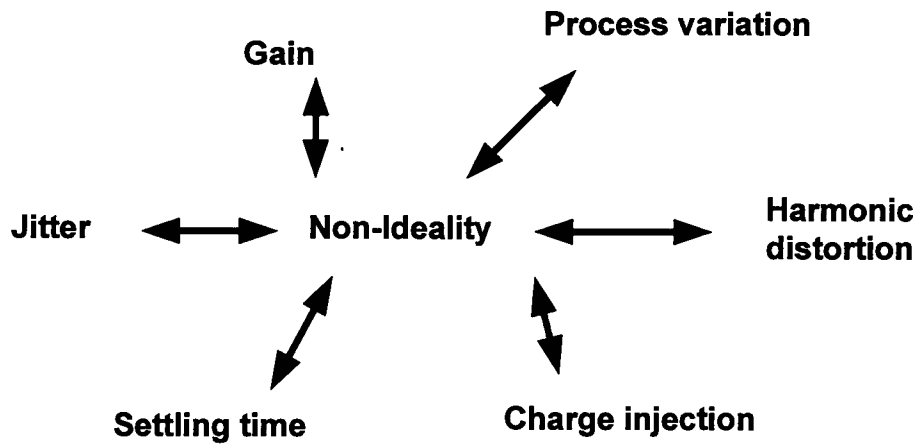


Figure 2-6 Non-ideality factors

Those errors are difficult to relate to the final resolution of the ADC due to large variety of error behaviours. The effect of each circuit non-ideality can be analyzed individually on how severe each factor can degrade the ADC performance. In general, circuit non-ideality can be reduced with careful circuit design and layout. However, more power consumption and devices might be required for reducing the effect of non-ideality. Thus, there is a trade-off between circuit performance, complexity, power consumption, and die area.

Chapter 3

Circuit Design

The process of designing ultra-low-power circuits starts with examining the power consumption of various circuit architectures. The choice of architecture is critical in the design process since a poor choice could lead to a sub-optimal design, no matter how well designed the sub-blocks are. On the other hand, a proper choice of architecture can result in not only dramatic energy savings but also good performance with respect to other metrics. Although power consumption is of paramount importance in this application, there are other considerations that will affect the choice of architecture.

In the target TPMS design, there will be a main module in the car controlling the sensor node in each tire. Although each sensor node has very limited capability and functionality, the entire network system can still be powerful by utilizing the sensing and data processing power of each individual node. Each sensor node has its own hardware and embedded software, such as MEMS sensors, pre-amplifier, ADC, microprocessor, and a RF transceiver. In distributed sensor networks, each node is designed to operate using very little energy and meeting the required performance specification and communicating with the main module or other nodes to exchange data.

In our application, the ADC performance specification is not particularly strict. Better performance can be achieved at the cost of more power dissipation. Each node has different

modes of operation such as sensing pressure or temperature. Due to the low voltage nature of this design, it is desirable for the ADC to have a rail-to-rail input conversion range, and use a pre-amplifier to scale the sensed voltage to the proper input range for ADC according to different modes. This would allow for a greater noise margin. In most ADCs, the circuit consumes more power during the sampling phase and uses as little power as possible during the conversion phase. Therefore, power consumption can be effectively minimized if energy saving techniques can be used during the sampling phase.

In this TPMS application, the ADC is designed in a $0.18\ \mu\text{m}$ CMOS technology without using any low- V_T devices. The threshold voltages for the NMOS and PMOS devices are typically around $0.5\ \text{V}$ and $-0.5\ \text{V}$, respectively. Metal-insulator-metal capacitors (MIM caps) are used to implement the capacitors in the voltage doubler design. The ADC was designed to meet the following performance specifications:

1. Resolution of 8-bits
2. Input range equal to rail-to-rail
3. Low supply voltage of $1\ \text{V}$
4. Sampling rate greater than $50\ \text{kSample/s}$
5. Power consumption less than or equal to $5\ \mu\text{W}$

3.1 ADC Architecture

There are many types of ADC architectures. In Figure 3-1, major ADC architectures are categorized in terms of power, resolution, and sampling rate. As shown in the figure, only a

few architectures are suitable for the TPMS application. Since low power consumption is of paramount importance for this design, the high-speed architectures which also have high power dissipation characteristics are not suitable choices.

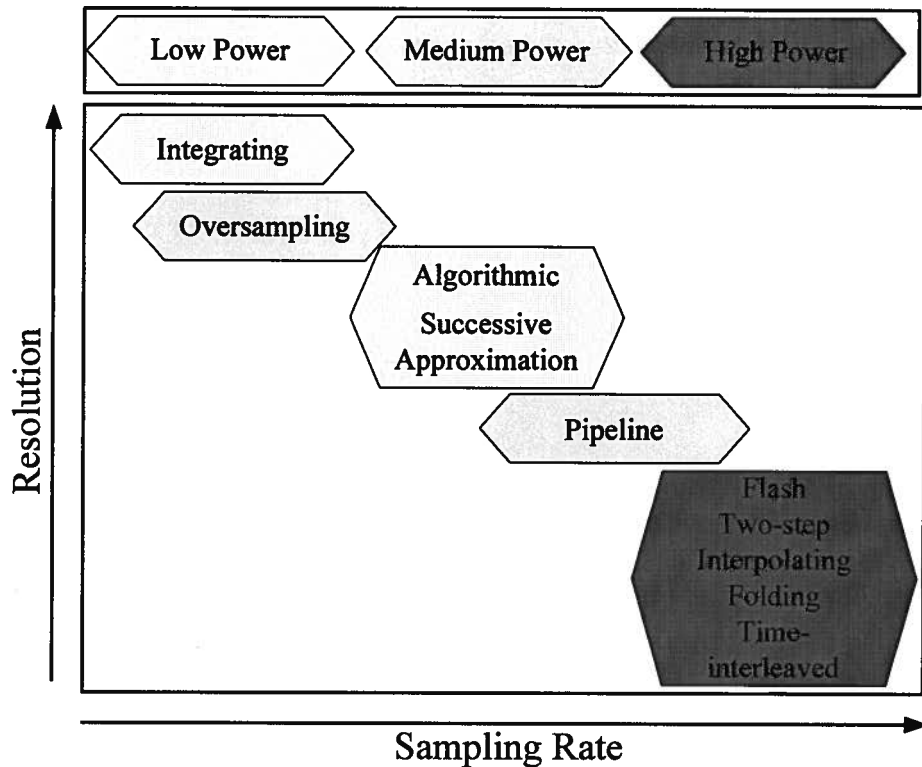


Figure 3-1. Categoring of ADC architectures based on the power consumption, resolution and speed of ADCs (adapted from [14])

Time-interleaved converters usually require multiple sets of analog hardware such as sample-and-hold circuits and sub-ADCs to segment the input signals. By splitting the input signal into segments, different portions of the signal can be processed in parallel, thus reducing the time needed for conversion, however, the high power consumption is a drawback [15]. Flash converters are generally known as the simplest and fastest architecture

for implementing ADCs. In this type of converters, a resistive ladder divides the reference voltage into 2^N different values which can be compared in parallel with the analog input. In order to do the conversion in parallel, 2^N comparators are required [16]. This results in a high power dissipation and makes the flash converter impractical for low power and high resolution designs. Folding and interpolating converters are variants of flash converters and contain less comparators while maintaining a relatively high speed of operation; however, the architecture still consumes too much power and is not suitable for this design [17]. The architecture of two-step converters separates the task of most significant bit (MSB) conversion and the least significant bit (LSB) conversion [18]. This enables coarse resolution comparator to be used for MSB conversion while the fine resolution comparator is used for LSB conversion. Pipeline converters are not suitable for this application because they contain several comparison channels requiring excess amount of hardware, resulting in additional power consumption.

Integrating (dual slope) converters can become a viable architecture for this application if they can achieve higher sampling rates. They have very low offset and gain errors, and can achieve very linear outputs. This architecture consists of small amount of circuitry so it can be very low power [14]. Two disadvantages of the integrating converters are that the conversion speed is very slow and accurate clock timing is required. In the TPMS application, it is difficult to generate a high precision clock without consuming excess power. In our application, not only the slow conversion speed of integrating converters could be an issue, but also the conversion period could vary depending on the operation mode. Therefore, precise timing requirements and varying conversion periods made

integrating converters unsuitable for this application, even though the power consumption of this architecture is very low.

Oversampling converters are a popular approach for high resolution medium-to-low speed applications. They are also known as delta-sigma ADCs [14]. Delta-sigma ADCs can be made to be low power for a given resolution and sampling rate. However, they require complex clocking circuitry and for meeting the required specification of this application that would need excess power.

Algorithmic converters are one of the suitable architectures for this application. They require a small amount of analog circuitry which consumes very little power and they re-use the same circuit to perform conversion cyclically over time. During the conversion cycle, a comparator, two sample-and-hold circuits, and an amplifier with a gain of 2 are needed. Implementing an accurate multiply-by-two gain amplifier can be one of the drawbacks. Fortunately, it is possible to design the gain amplifier so that it does not rely on any capacitor matching [14]. Another drawback of this architecture is that it cannot compare the input against the reference voltage directly. The input signal always needs to be sampled twice using the same capacitor and then use the gain of 2 amplifier to perform the conversion process. This process leads to a relatively slow conversion speed. A 10-b cyclic algorithmic with $1 \mu\text{W}$ power dissipation has a sampling rate of 2.9 kS/s [19].

The successive-approximation register (SAR) architecture possesses all the desired advantage of algorithmic ADCs. In addition, it has the flexibility of performing comparison on the input signal and reference value. The main difference between SAR and algorithmic

architectures is that a SAR converter halves the reference voltage in each cycle while an algorithmic converter doubles the error voltage and leaves the reference voltage unchanged [14]. Similar to algorithmic converters, SAR converters consist of small amount of analog circuitry to repeatedly process the data during the conversion cycle. Figure 3-2 shows that SAR architecture only uses one reference switch for sampling the input, one comparator which is used repeatedly, and a logic network to perform the search algorithm.

The power consumption of SAR is distributed in two phases: (1) charging the binary weighted capacitors to the reference voltage during the sampling phase and (2) comparing the input value and reference voltage during the N comparison operations where N is the resolution in bits. The successive approximation register consumes very little power relative to the comparator because the digital logic processes one bit at a time.

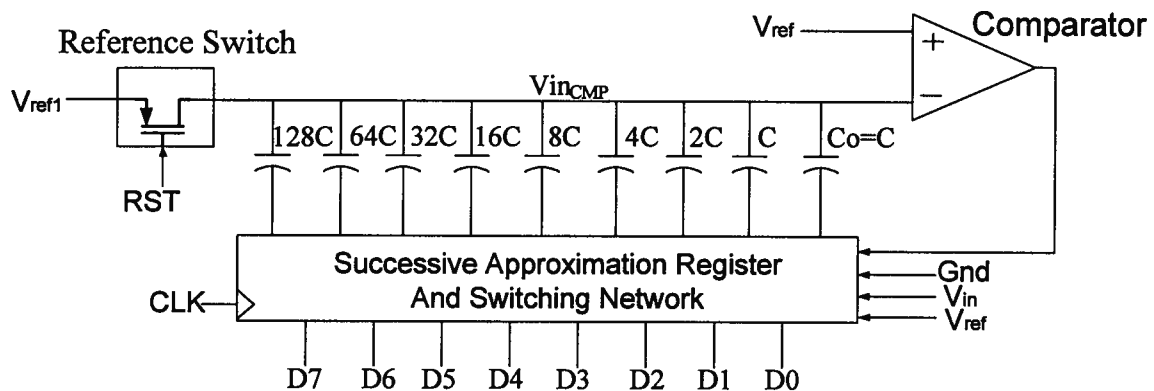


Figure 3-2 A N-bit charge redistribution successive approximation architecture.

Since the SAR uses digital logic to perform the search algorithm, it can be reconfigured and modified easily. Although it is not easy to change the implementation of the SAR ADC, the algorithm can easily be modified when the ADC is integrated with an on-chip

microprocessor. For example, lower resolution samples can be achieved by ending the search algorithm early. In this way, no changes will be made to the actual circuit implementation. Also, lower resolution samples can contribute to energy saving per sample. Therefore, the architecture is somehow flexible.

3.2 Design Flow

Based on energy consideration, hardware flexibility, and feasibility of design implementation, the successive-approximation architecture is chosen for this TPMS application. Figure 3-3 shows the systematic flow of the search algorithm in a SAR ADC.

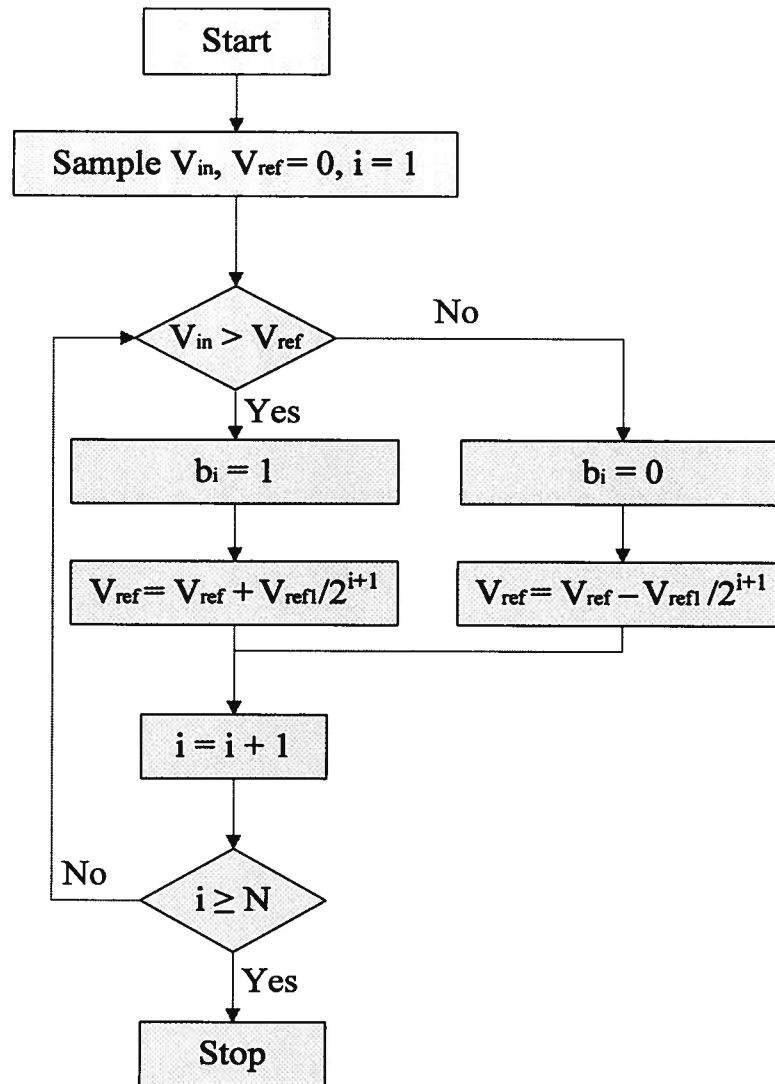


Figure 3-3. Systematic flow of the search algorithm in a SAR ADC [13]

The SAR presents an N-bit digital output code to the switching network, and these output codes can be converted back to a voltage at V_{inCMP} by properly configuring the capacitor array. On the other hand, the SAR, switching network, and the capacitor array form a digital-to-analog converter (DAC). The output of the DAC is continuously refined using the results of the comparator from MSB to LSB until the output voltage of DAC equals the input voltage V_{in} or the difference is less than or equal to V_{LSB} . The output of the ADC is

considered to be ready when the N-bit digital code is a representation of the sampled input voltage. As the SAR ADC employs the standard binary search in a feedback loop, the final N-bit digital output code will be available after the Nth conversion cycle.

The entire flow can be divided into two phases: sampling phase and bit conversion phase. During the sampling phase, the input voltage is sampled through the bottom plate of the capacitor array, shown in Figure 3-4. In the meantime, V_{inCMP} is charged to the reference voltage of the comparator. Therefore, the total charge on the capacitor array during the sampling phase is:

$$Q_{total} = C_{array} \cdot (V_{ref} - V_{in}) = 2^N \cdot C \cdot (V_{ref} - V_{in}) \quad 3-1$$

Note that the overall capacitance of the array is $2^N C$ where C is the unit capacitance. Although the total charge will be redistributed throughout the bit conversion phase, (neglecting leakage) it remains fixed due to the conservation of energy principle unless the entire ADC is reset for the next sample.

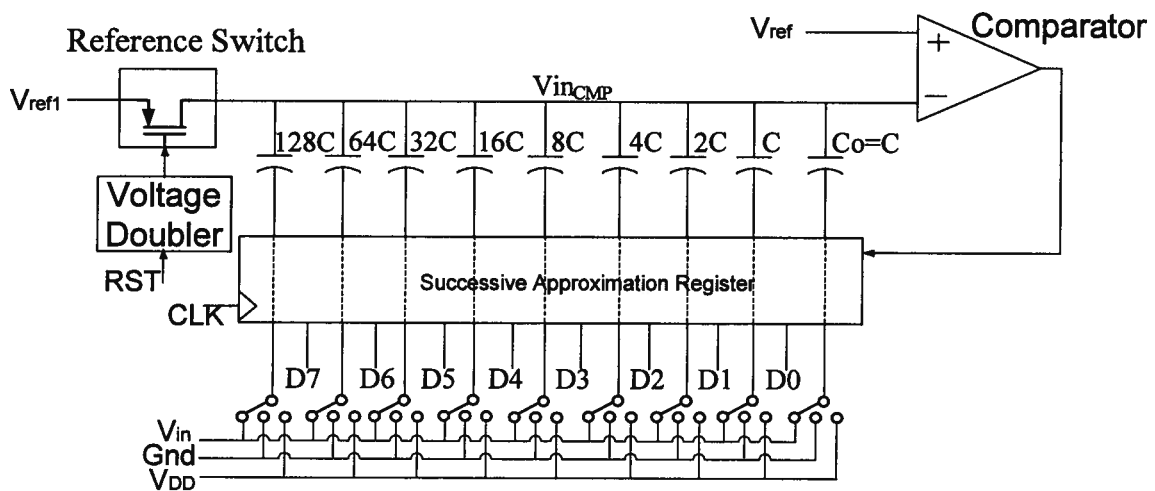


Figure 3-4. SAR ADC at sampling phase.

At the beginning of the bit conversion phase, the reference switch is turned off and the bottom plate of the capacitor array is connected to ground. Then, the bit cycle of the SAR begins. The SAR is implemented to have an initial value starting at midscale, $V_{ref1}/2$. Figure 3-5 shows the SAR ADC at the most significant bit comparison cycle. The switching network corresponds to the midscale, $10000000_2=128_{10}$ in the binary search and forces the output of DAC to be $V_{ref1}/2$. Since the off state of the reference switch leaves V_{inCMP} floating in the conversion phase, the voltage can change while the total charge on the capacitor array remains constant as calculated in equation 3-1. The voltage at V_{inCMP} node at the MSB comparison cycle can be estimated by

$$V_{inCMP} = \frac{3}{2} \cdot V_{ref} - V_{in} \quad 3-2$$

If the V_{in} is greater than $0.5V_{ref1}$, the comparator will return a “1” to indicate the input voltage is greater than $V_{ref1}/2$. The result of this cycle will be carried onto the next bit approximation by SAR. In this case, the next bit approximation will be $11000000_2=192_{10}$, or if V_{in} is less than $0.5V_{ref1}$ the next bit approximation will be $01000000_2=64_{10}$.

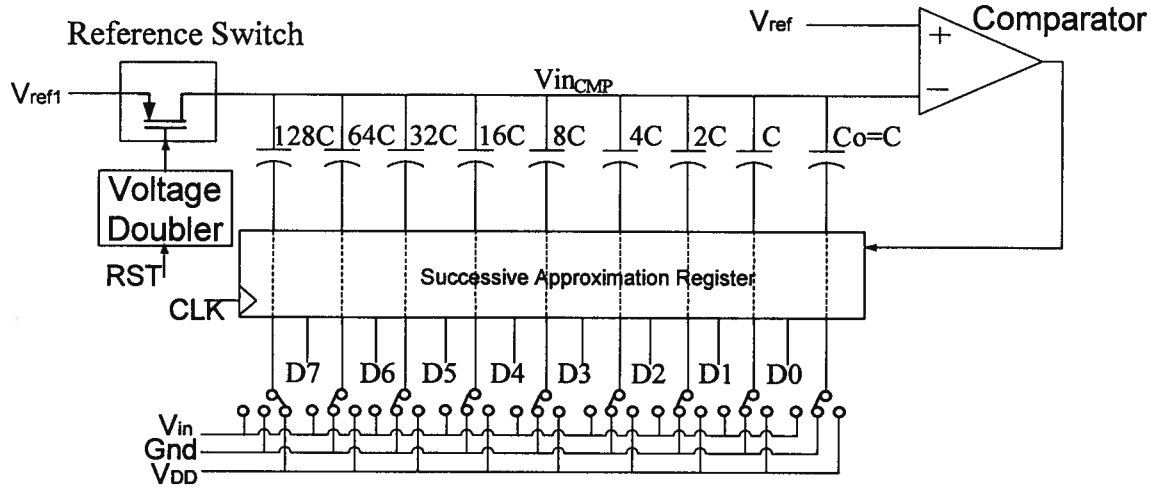


Figure 3-5. SAR ADC at bit conversion phase

Due to the simplicity of the binary search algorithm, the implementation of each individual block in SAR ADC is not as complicated. However, each individual circuit block still plays its important role on the overall ADC performance. Therefore, the analysis on how the implementation and performance of each individual block affects the ADC as a whole becomes necessary and will be presented in the following sections.

3.3 Reference Switch and Switching Network

The switching network and the reference switch control the sampling and bit conversion states. They can limit both the linearity and sampling speed of the ADC. The linearity is affected by issues such as charge injection, clock feedthrough, and the “on” resistance of the reference switch. A small change in the analog signal due to a nonideal switch can result in a voltage error at the input of the comparator. If this error is comparable to a V_{LSB} , the overall ADC linearity and resolution can be reduced by one bit or more. The “on” resistance

of the switch also determines the minimum sampling period of the ADC since it limits the settling time.

As mentioned in Section 3.1, generating a separate reference voltage would increase the complexity, area, and power consumption of the circuit to the extent that the reference voltage generator might dissipate more power than the ADC. Choosing the supply voltage itself as the reference voltage can minimize these issues. Another advantage of using supply voltage as the reference is to force V_{inCMP} to be between $0.5V_{DD}$ and $1.5V_{DD}$, as shown in Figure 3-6. The minimum voltage of V_{inCMP} is at $0.5V_{DD}$, which is 0.5 V in this design. Since this voltage is greater than the threshold voltage of the comparator's input transistor, the DC biasing circuitry at the input of the comparator can be eliminated for additional power savings.

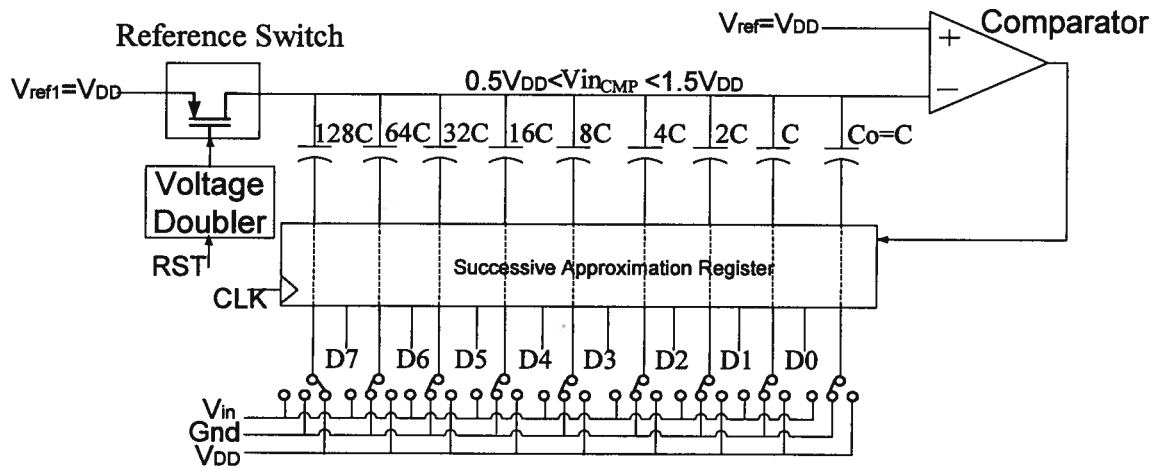


Figure 3-6. Voltage range at V_{inCMP} node of the SAR ADC

The linearity of the ADC depends on the fixed charges at the V_{inCMP} node during the bit conversion process. In order to maintain a fixed charge at this node, the reference switch

has to be strongly off regardless of the voltage at the V_{inCMP} node throughout the conversion phase. When the worst case voltage of V_{inCMP} is at $1.5V_{DD} = 1.5\text{ V}$, there is a chance for the simple PMOS reference switch to have source/drain reversal. Not only the source/drain reversal can cause circuit malfunction, but also the leakage current can also cause additional power consumption. In order to maintain a strong off-state in the PMOS reference switch, the following equations have to be satisfied.

$$|V_{gs}| < |V_{tp}| \quad 3-3$$

$$|V_{ref} - V_g| < |V_{tp}| \quad 3-4$$

$$|V_{inCMP} - V_g| < |V_{tp}| \quad 3-5$$

When V_g (the gate voltage of the PMOS reference switch) is at the voltage of $1.5V_{ref1}$, equations 3-4 and 3-5 can be satisfied.

There are several methods to reduce the effects of leakage. One approach is to adjust the threshold voltage of the PMOS switch by modifying the well potential. An alternative approach is to boost the gate voltage of the PMOS reference switch above V_{DD} so that the switch will be in off-state when ADC is in the comparison phase. For a PMOS device, the bulk terminal must be at the highest voltage to avoid reverse biasing the diode between the p-channel transistor source and drain and its N-well. Therefore, the bulk terminal of the PMOS reference switch must be boosted too. The technique of voltage boosting is described in Section 3.4.

As mentioned earlier, using the power supply as a reference voltage offers increased power savings. However, the disadvantage of this technique is a reduction in the power supply

rejection (PSR) of the ADC. As the V_{DD} changes, V_{ref} also changes and the ADC output codes change accordingly even though the input signal is independent of the supply voltage. In the extreme case of significant power supply drifts, the data taken at sampling phase cannot be compared because the reference voltage is constantly changing.

There are two approaches to maximize the system PSR. The first method is to generate a supply independent reference voltage for the ADC at the cost of increased power consumption. This way the ADC samples will be independent of power supply voltage variation. The constraint of this method is that the ADC input has to be power supply independent; otherwise the overall PSR is still poor. Now the problem lies on the sensor. Since this TPMS application uses a MEMS sensor, the design of the ADC and sensor are tightly linked. Therefore, using the supply independent reference voltage for both the ADC and the sensor would be necessary to improve the overall sensor-ADC PSR. However, the higher power consumption required by this method leads us to consider other options.

The second method is to make the sensor output track the supply as well, which is the approach used in this design [7]. Using sensors that are inherently ratiometric with V_{DD} (such as bridge sensors) can maximize the power supply rejection of the sensor-ADC system. In this case, the MEMS sensor is a type of bridge sensor whose output changes based on the supply voltage and resistor bridges. Although both the ADC and the sensor itself are power supply sensitive, the overall system can be designed to be less sensitive to slow power supply variation. The advantage of this approach is that no extra circuits are needed to generate a power supply independent reference.

3.4 Voltage Doubler

During the sampling phase, the top plate of the capacitor is charged to V_{ref} through the PMOS switch and the bottom plate of the capacitor is charged with the input signal. At the same time, the microcontroller sends a reset low signal to reset the entire ADC. When the ADC is in the bit conversion phase, the comparator and SAR are implementing the bit comparison algorithm and the PMOS switch must remain off to fix the total charge on the capacitors. As mentioned in Section 3.3, choosing V_{DD} as the reference voltage will cause potential source/drain reversal for the PMOS switch, but the potential circuit malfunctions can be avoided if the gate and bulk voltages of the PMOS switch are boosted.

The normal range of operating voltages is usually limited in semiconductor technology; however, voltages higher than the power supplies are required in certain applications. Switched-capacitor voltage doublers, level shifters, and charge pumps are the most popular techniques to increase voltages, and they work by transferring charges to a capacitive load involving neither amplifiers nor regular transformers. A switched-capacitor voltage doubler, shown in Figure 3-7, was implemented based on the circuit reported in [20]. This voltage doubler consists of a simple voltage booster and proper well-biasing circuitry.

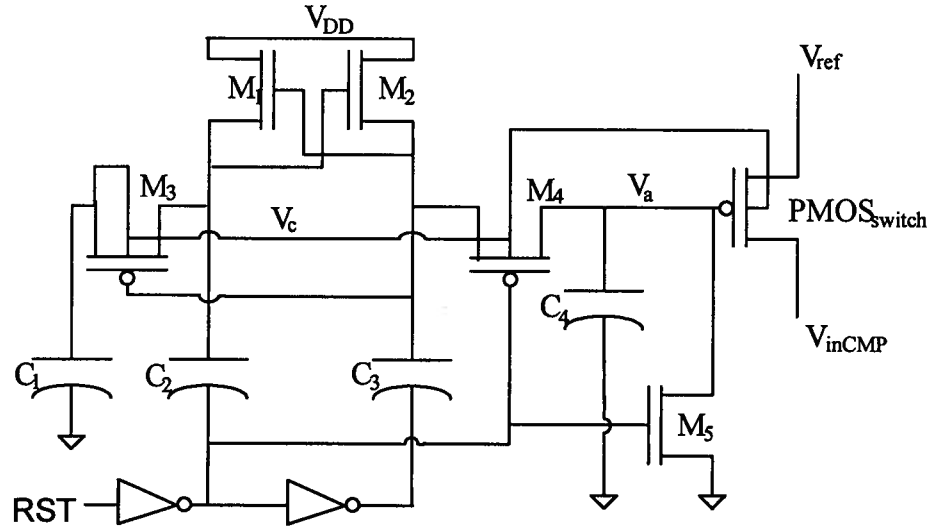


Figure 3-7. Voltage doubler with PMOS reference switch

The left half of the circuit is generating the DC well bias voltage and storing the charges in C_1 and C_2 for M_3 and M_4 while the right half of the circuit is generating the voltage-doubled signal through C_3 and C_4 . The cross-coupled transistors M_1 and M_2 with the capacitors C_1 and C_2 form the DC well bias voltage for M_3 and M_4 to ensure no leakage occurs, and that intrinsic diodes between the source/drain and the bulk terminal of the PMOS devices are reverse biased when the output voltage, V_a , is doubled. In this design, the output voltage, V_a , is targeted at $1.5V_{DD}$ because increasing the voltage any higher than needed results in wasting energy. Due to the cross-coupled NMOS and capacitor C_1 , V_c settles to above $1.5V_{DD}$ so that it can be used to boost up the N-well substrate of the PMOS_{switch}. When RST is low in the sampling phase, M_5 is “ON” to discharge C_4 to turn the PMOS_{switch} on completely. At the same time, C_1 , C_2 , and C_3 are being charged. When RST is high during the conversion phase, M_4 is on and V_a settles to 1.5 V. With 1.5 V at the gate of the PMOS_{switch}, the device is guaranteed to remain off even if V_{inCMP} swings higher than V_{DD} .

The voltage doubler circuit is relatively insensitive to the transistor sizes used; however, the NOT gates have to be large enough to drive the capacitor C_2 and C_3 . Also, C_4 has to be designed large enough such that small quantities of charge are stored and can be used to overdrive the PMOS_{switch}. The waveforms of RST, V_a , and V_c are shown in Figure 3-8.

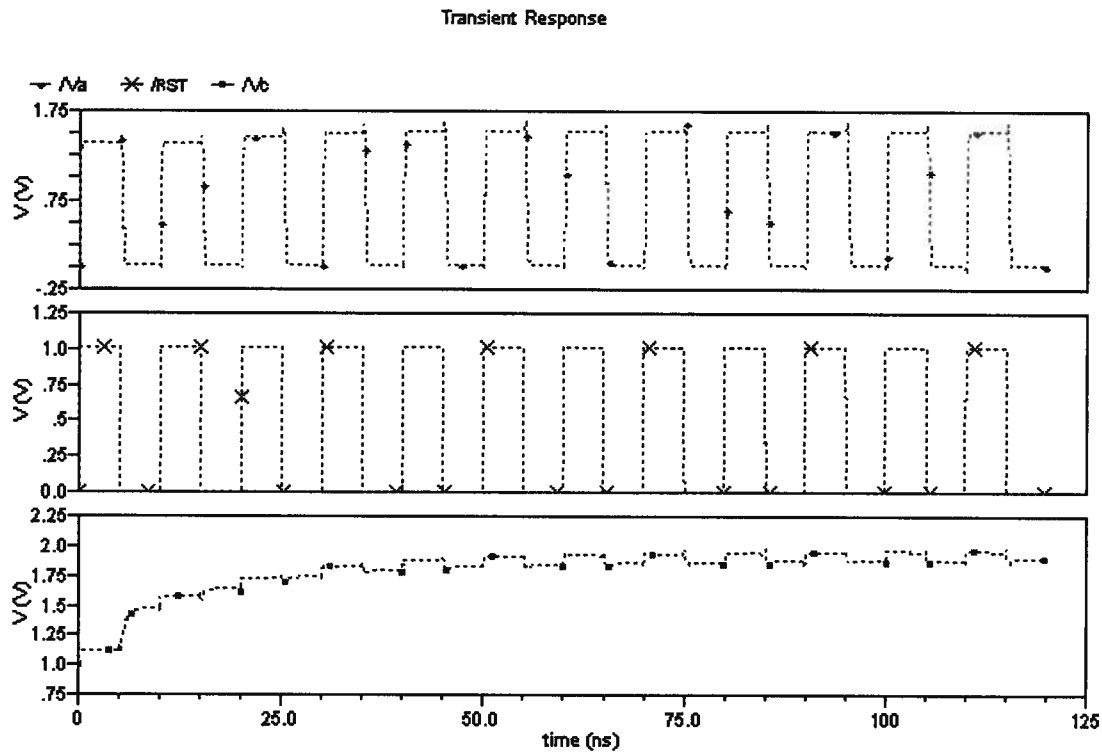


Figure 3-8. Transient response of the voltage doubler

When the internal signals and output signal of voltage doubler go above the supply voltage, oscillatory noise like signals in the substrate can become an issue [7]. To make sure that the signals rising above V_{DD} will not cause oscillation on the power supply, a test circuit of Figure 3-9 is used and the Fourier transform of the resulting V_{DD2} signal is analyzed. From the discrete Fourier transform (DFT) of the signal shown in Figure 3-10, it can be seen that

there is no harmonics at higher frequencies. The signal-to-noise ratio is 24.225dB (from Matlab simulations).

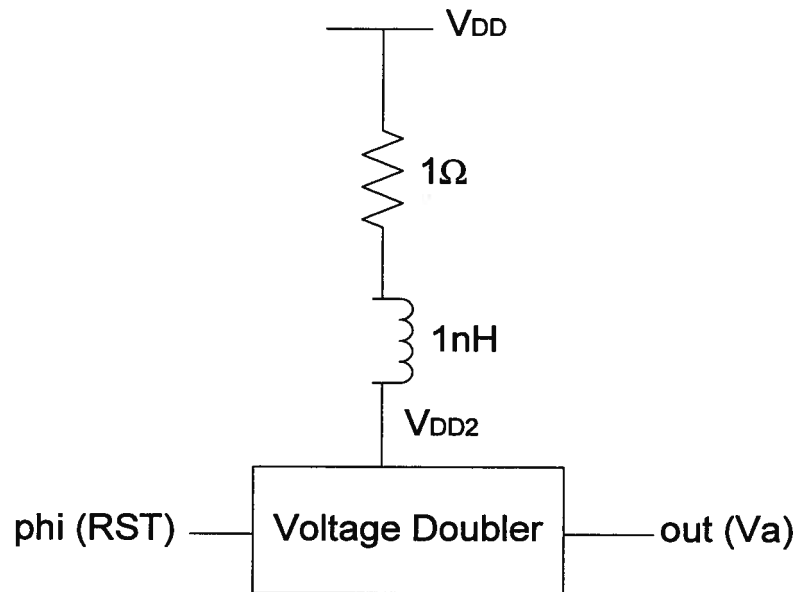


Figure 3-9. Circuit setup for DFT analysis

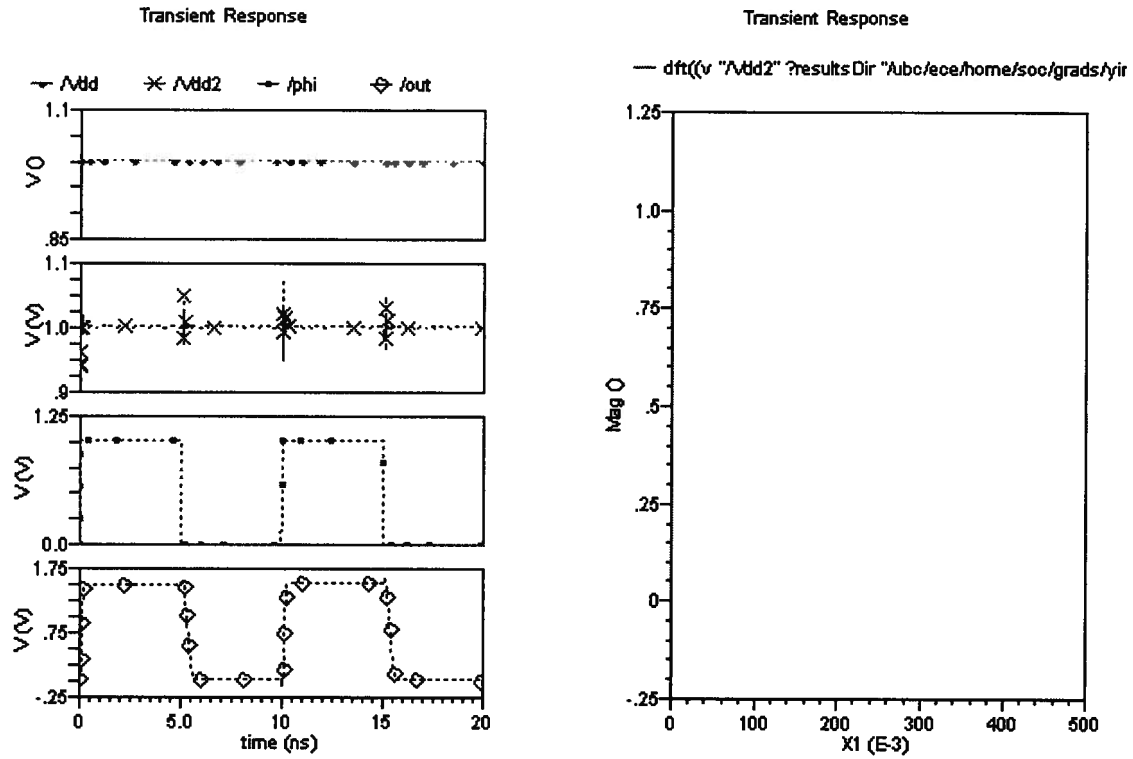


Figure 3-10. Waveform and DFT result on Vdd2 of voltage doubler

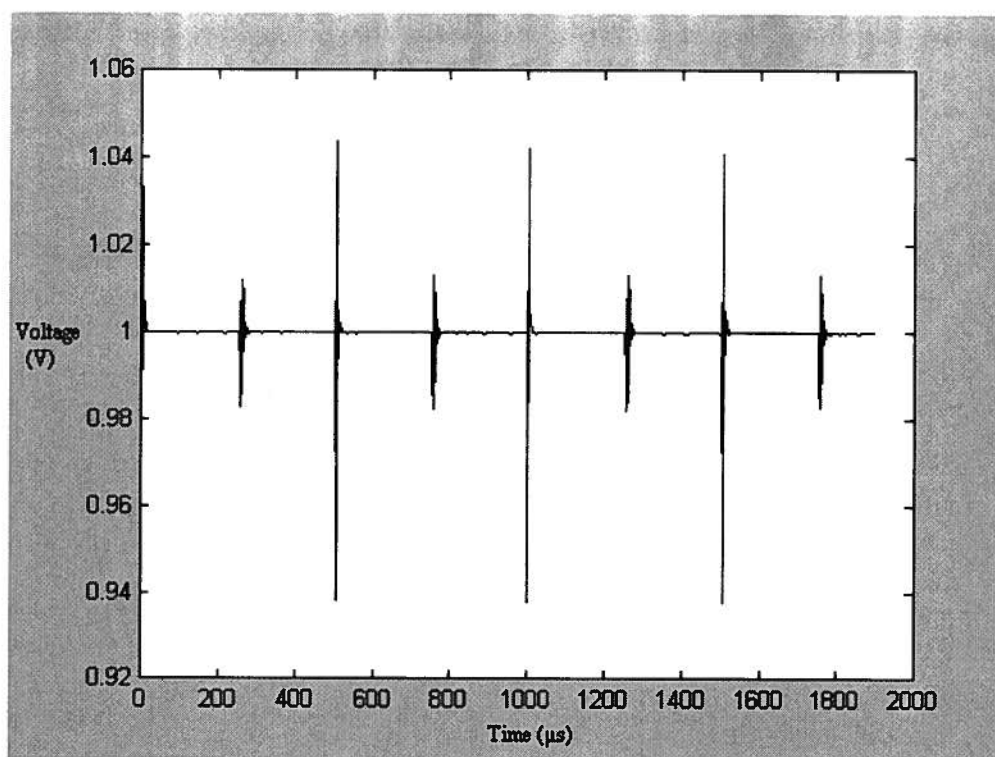


Figure 3-11. Voltage doubler switching time

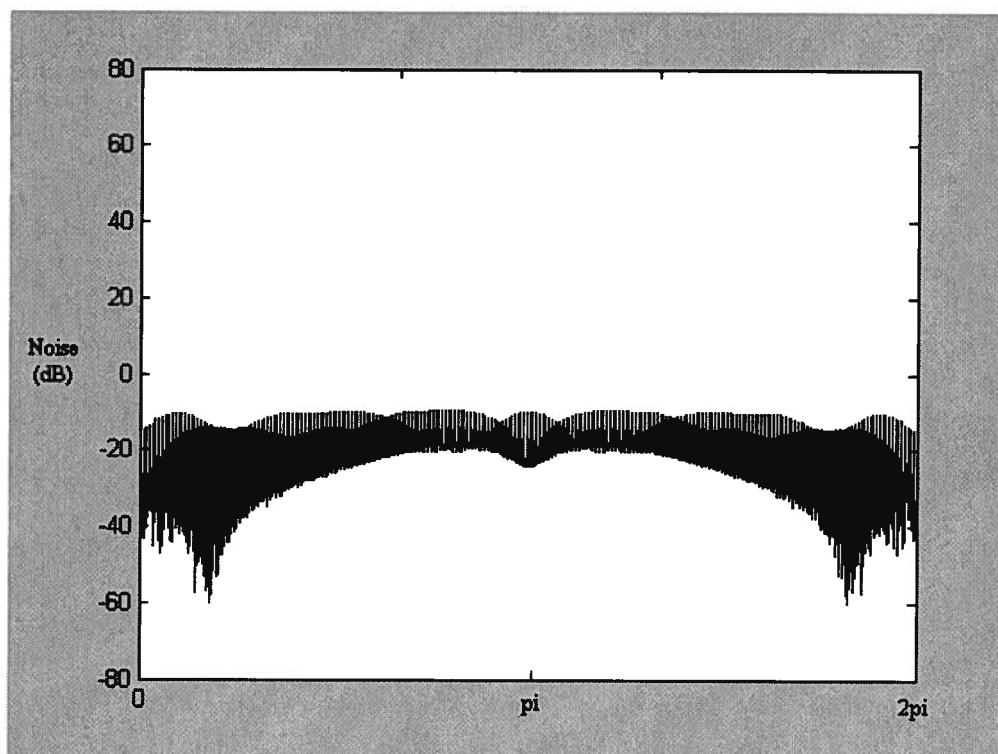


Figure 3-12. Voltage doubler FFT

3.5 Capacitor Array

The speed and linearity are the most important factors when the performance of an ADC is evaluated. The speed and linearity of the ADC can be limited by the speed and linearity of the DAC performing the charge redistribution. The DAC consists of the SAR, switching network, and the capacitor array. The SAR generates the 8-bit digital codes from the comparator output, and controls the switching network and the capacitor array to translate the 8-bit digital code to an analog voltage at V_{inCMP} node. The speed of this process is limited by the settling time of the DAC, which depends on the capacitor size of each individual bit and the corresponding effective “on” resistance of the switches in the switching network. The capacitor array plays a critical role in the ADC design because both ADC linearity and maximum sampling rate are determined by its design.

The linearity of the DAC is determined by the matching in the capacitor array in the layout and the nonidealities in the switching network. Assuming the comparator and the switching network are ideal, the overall ADC linearity is determined by the process variation of the capacitor array and the matching error in the capacitor layout. Since the layout of the capacitor array is the main factor of determining the desired ADC linearity, it has to be done very carefully. Additionally, each unit capacitor has to be designed large enough to compensate the device matching error and make the array insensitive to the parasitic capacitances.

The last two paragraphs illustrate one of the trade-offs in selecting a unit capacitor size. We would like small capacitors to maximize the sampling rate of the converter, but large capacitances to maximize the matching error, and thus the linearity of the ADC.

The power consumption of the ADC is also related to the unit capacitor size. Larger capacitors consume more energy per sample due to charging and discharging the capacitors in the array. As a result, there is another design trade-off between linearity and power consumption. Decreasing the size of the unit capacitor allows the ADC to achieve faster sampling rate and lower power consumption at the cost of lower linearity performance.

Most circuits, especially analog circuits, depend on device matching in both active and/or passive components. Depending on the circuit architecture, device matching can be the dominant factor in determining the circuit performance. Unfortunately, device matching error is limited by manufacturing and present in all designs and geometry dependant layout techniques such as a common-centroid structure [21] must be used to minimize the error associated with mismatched devices.

There are two types of random variations, peripheral and areal fluctuations, occurring during manufacturing the passive and active devices. Peripheral fluctuations occur along the edges of the device while the areal fluctuations occur throughout the device. The capacitor standard deviation matching error can be written as [21]:

$$\sigma_c = \frac{1}{\sqrt{C}} \sqrt{k_{ac} + \frac{k_{pc}}{\sqrt{C}}} \quad 3-6$$

where k_{aC} and k_{pC} are the areal and peripheral fluctuation constants for a capacitor. Increasing the device area increases the capacitance and reduces the total amount of areal matching error due to the tendency for the variations to cancel out. Increasing the device periphery also decreases the total peripheral error because fluctuations tend to cancel out over larger device peripheries. Therefore, based on the properties of both peripheral and areal fluctuations, larger device sizes allow for more precise matching.

The metal-insulator-metal (MIM) capacitors are available in the 0.18 μm CMOS technology used in this work; however they cannot be used in this application because the minimum size of the MIM capacitor is 200 fF which is too large for the size of the unit capacitor. Therefore, parasitic capacitances between metal plates are used in this design.

When the device matching, linearity, power consumption, and speed are taken into consideration, the size of the unit capacitor should be as small as possible while still achieving optimal linearity and power consumption. The worse case total capacitance error for an 8-bit ADC occurs when every capacitor is switched, from the code transition of 01111111_2 to 10000000_2 in the successive approximation register. Taking the assumption that σ_C is the Gaussian distribution of the individual capacitor error, the worst case DNL of the converter can be characterized by a Gaussian distribution given by

$$\sigma_{DNL} = \sqrt{2^N - 1} \cdot \sigma_C \cong 2^{\frac{N}{2}} \cdot \sigma_C \quad 3-7$$

where N is the resolution of the ADC. To ensure that almost all fabricated ADCs have a worst case differential nonlinearity (DNL) error of less than 1 LSB, σ_{DNL} has to be less than 1/3 (i.e., $3 \sigma_{DNL} < 1$). This will set the minimum unit capacitance value for the capacitor;

however, a safety margin must be included to account for the parasitic capacitances associated with routing. With all the factors considered, the unit capacitance of 15 fF is chosen for this design. The overall capacitance in the array is approximately 3.8 pF.

The capacitor is designed to have the metal plate size of $10.3\ \mu\text{m}$ by $10.3\ \mu\text{m}$ by using the top four metal layers stacked on top of each other and connected in parallel. The three parasitic capacitances formed by the four metal layers add up to yield roughly 15 fF. This structure is shown in Figure 3-13, where the capacitance values were obtained from the layout using an extraction tool. The top four metal layers were used in order to achieve minimum parasitic capacitance between the bottom plate of the unit capacitor and the substrate. Of course, the bottom plate of this structure has a greater parasitic capacitance than the top plate, so the orientation used when connecting this capacitor to the rest of the circuit must be considered carefully.

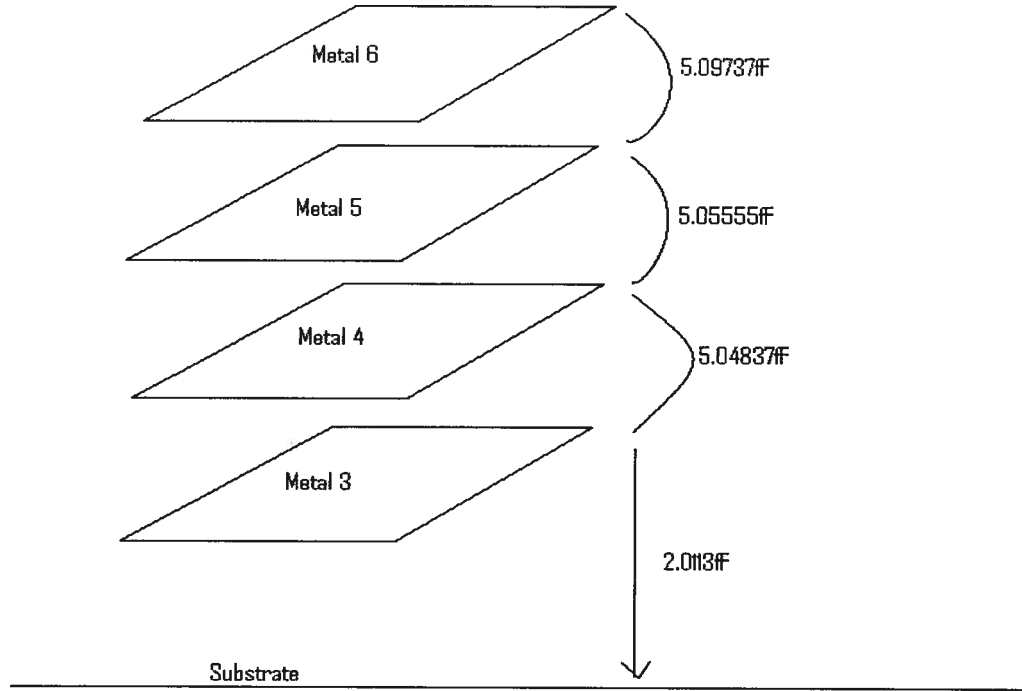


Figure 3-13. Parasitics capacitance extraction of unit capacitor

During the first cycle of the bit conversion phase of ADC, the voltage at the V_{inCMP} node can be expressed as

$$V_{inCMP} = V_{ref} + \frac{C_{array}}{C_{array} + C_{pCMP}} \cdot \left(\frac{1}{2} \cdot V_{ref} - V_{in} \right) \quad 3-8$$

where C_{array} is the total capacitance of the array and C_{pCMP} is the total parasitics capacitance at the input of the comparator. Although this equation is derived at the first cycle of bit conversion phase, it shows that any additional parasitic capacitances at the input of the comparator degrade the input signal to the comparator. As a result, it affects the overall resolution of the ADC. Using the metal 6 layer as the common plate for the capacitor array can effectively minimize the parasitic capacitance at the input of the comparator. The bottom layer of the capacitor structure will be connected to the switch network, and as long

as the switches can drive the additional parasitic capacitance, the performance of the ADC will suffer minimally.

Adopting the common centroid layout technique to the capacitor array results in the scheme shown in Figure 3-14 [7].

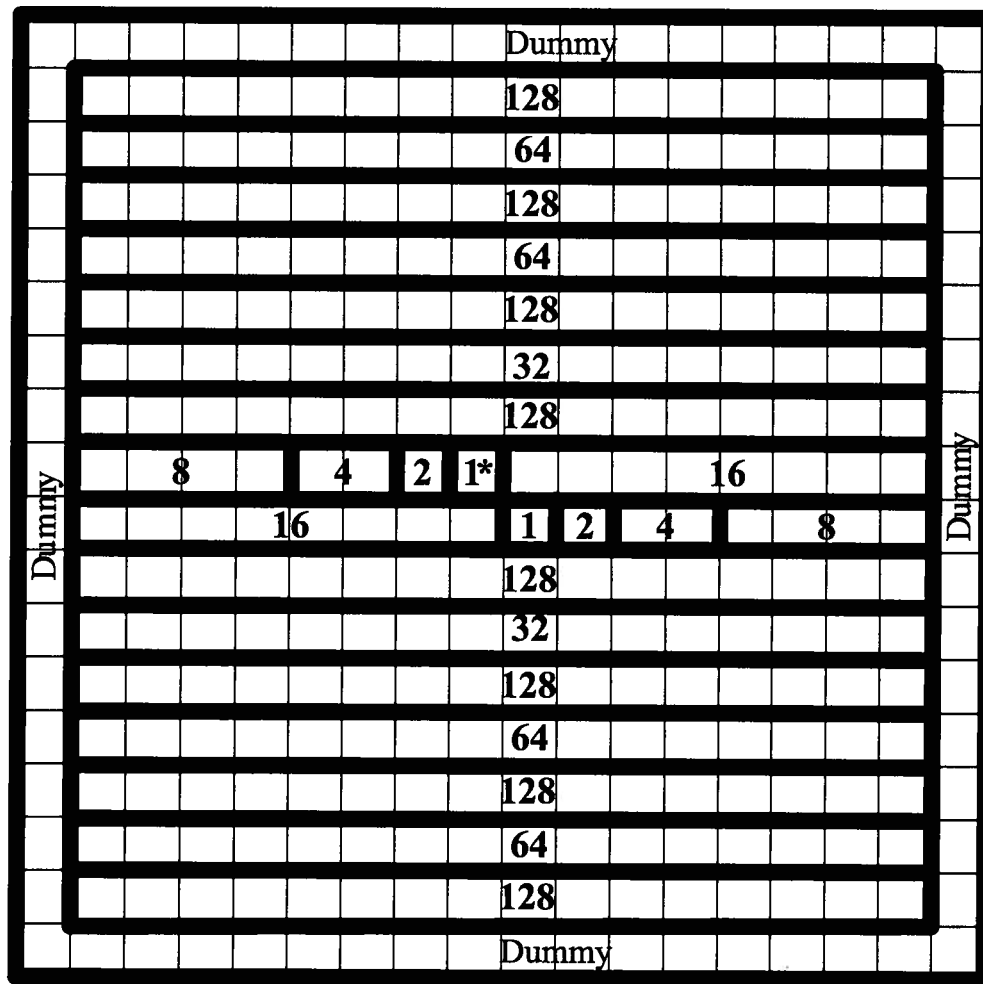


Figure 3-14. Common centroid layout for the capacitor array

In Figure 3-14, the existence of the dummy capacitor around the outside of the structure ensures that all capacitors in the core array have exactly the same structures and parasitic capacitance on each side in order cancel out any systematic matching error.

However, the floorplan shown in Figure 3-14 is not suitable for the designed metal capacitors due to the parasitic capacitances associated with the routing. Even using the top metal layer for the routing paths to reduce the parasitic capacitance to ground, the percentage of parasitics will be greater for the smaller capacitances since they must be routed from the center of the array. Therefore, the small capacitors are placed on one side of the structure so the parasitics due to wiring are minimized. The proposed floorplan is shown in Figure 3-15 (with the expanded view of the single unit capacitor layout). Metal 4 and metal 6 plates are connected to form the top plate of the unit capacitor while metal 3 and metal 5 plates are connected to form the bottom plate.

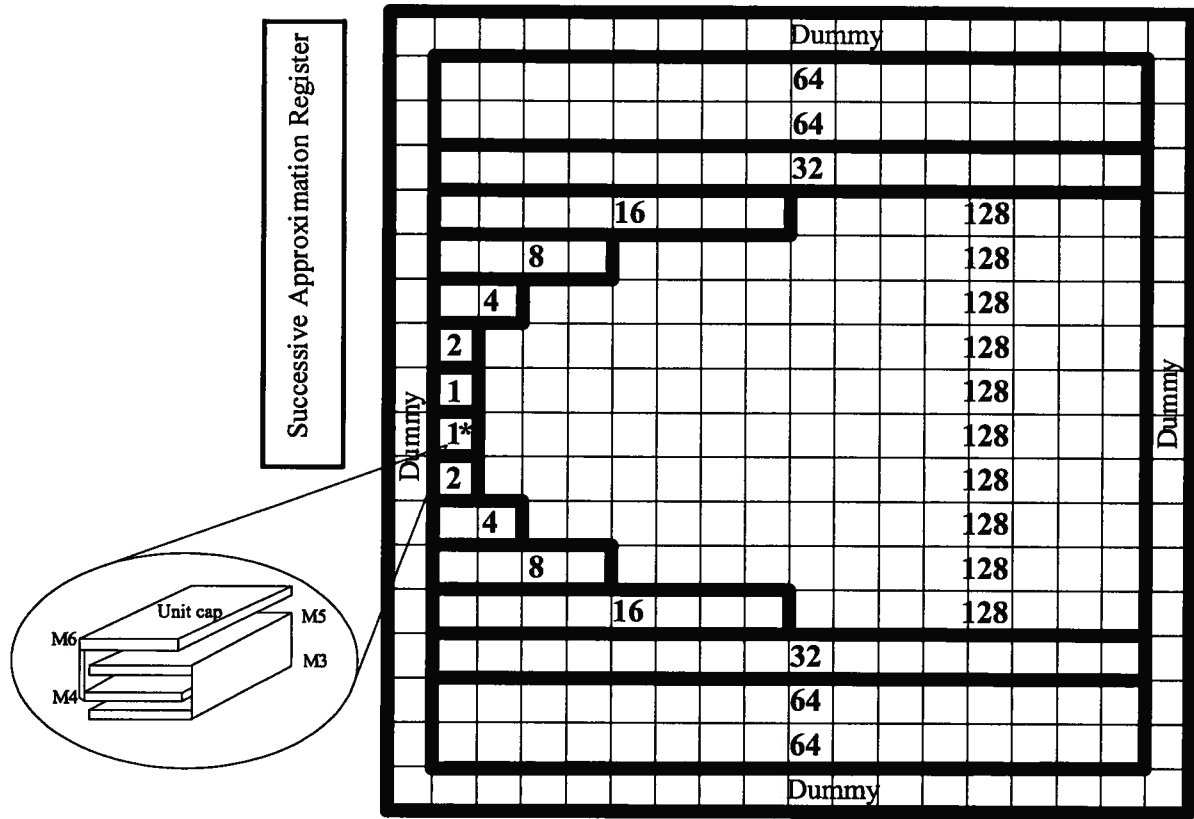


Figure 3-15. The proposed layout floorplan for metal plate capacitor array.

3.6 Switching Network

The switching network is another component in the charge redistribution DAC which can degrade the performance of the ADC. The speed of the ADC is determined by the settling time of the charge redistribution process, which limits the maximum sampling rate of the ADC. The settling time is determined by the “on” resistances of the switching network and the capacitor array. Any circuit nonidealities in the switching network such as charge injection and clock feedthrough will degrade the linearity of the overall system. The error caused by those circuit nonidealities can result in a voltage error at the V_{inCMP} node that is

comparable to or larger than an LSB, meaning the linearity of the ADC could be reduced by one or more bits. Consequently, some circuit techniques must be used to minimize the nonidealities of the switches.

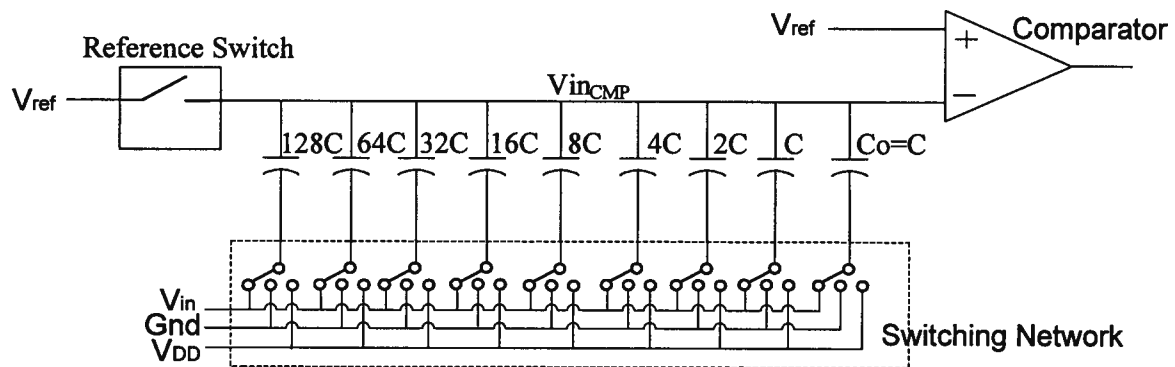


Figure 3-16. Simplified ADC block diagram with switching network diagram detail.

In general, simple NMOS and PMOS switches consume less power than the CMOS transmission gates, however, a single transistor switch will have a voltage swing that is one threshold voltage lower than rail-to-rail. The input voltage in this application has a rail-to-rail voltage swing, therefore, CMOS transmission gates must be used in order to pass the entire signal. The constraint for CMOS transmission gates to be fully functional is that the power supply must be greater or equal to the sum of the NMOS and PMOS threshold voltages.

$$V_{DD\min} \geq V_m + V_{tp} \quad 3-9$$

Equation 3-10 sets the minimum supply voltage for the ADC. When the supply voltage is a little lower than the minimum required V_{DD} , the CMOS transmission gates still can be

functional; however, their resistance could be high and the transistors may be forced to operate in the weak inversion region which will limit the input bandwidth of the ADC.

The maximum sampling rate of the ADC is determined by the input sampling time and the speed of the switching network. During the sampling phase, the top plates of the capacitors in the array are charged to V_{ref} while the bottom plates are charged to V_{in} . Then during the bit conversion phase, the top plates of the capacitor are left floating while the bottom plates are charged to V_{DD} or ground. In both the sampling and bit conversion phases, the MSB capacitor, $128C$, is always the maximum load to be charged. During the sampling phase, the maximum load capacitance seen by the input CMOS transmission gate switch is equal to the MSB capacitor plus the bottom plate capacitance of other seven bit capacitors. During the bit conversion phase, each bit is switched to V_{DD} or ground according to the output of the comparator and the order of the SAR. Therefore, the capacitance varies according to the converted bit pattern. The worst case capacitance seen is at the MSB capacitor which is half of the total array capacitance. Assuming the small signal “on” resistance is fixed, the settling error can be calculated as:

$$\mathcal{E}_{setling} = e^{-t/(R_{ON}C)} < \frac{1}{2^N} \quad 3-10$$

where R_{ON} is the “on” resistance of the switch, C is the capacitive loading seen by the switch, and N is the resolution of the ADC. Assuming the ADC is ideal and there is no other source of error, the settling error must be less than 0.39 % for an ADC with 8-bit resolution. To achieve this settling error accuracy, 5.6x the time constants ($R_{ON}C$) is required. Usually in practice, there are many other sources of error in the ADC so that the

resolution tends to be over designed. With 9-bit accuracy, the settling error must be less than 0.2% and the settling must be achieved within 6.3x the time constant.

In Table 3-1, the “on” resistance is calculated based on the switch size used in the switching network. With equation 3-10 and a 9-bit accuracy, the calculated settling time is similar to the simulated settling time. The settling time of the sampling phase is limited by the PMOS used in the reference switch rather than the transmission gates used for the input since it has a higher “on” resistance. At the bit conversion phase, the settling time is limited by the PMOS switch passing V_{DD} rather than the NMOS switch passing ground.

| | “on” resistance ¹ Hand calculation | Settling Time (6.3 $R_{ON}C_{worst\ case}$) Hand calculation | Settling Time Simulation |
|-----------------------------|---|---|---------------------------------|
| NMOS for ground | 2.08 k Ω | 25 ns | 24 ns |
| PMOS for V_{DD} | 2.5 k Ω | 30 ns | 43 ns |
| PMOS for reference switch | 4 k Ω | 95 ns | 135 ns |
| Transmission gate for input | 0.74 k Ω | 17.43 ns | 60 ns |

Table 3-1. Summary of switch resistance and settling time corresponds to 9-bit accuracy.

The data from the last column in Table 3-1 is recorded from simulation by using typical device models. According to the simulated settling time stated in Table 3-1, the worst case in the sampling phase requires a minimum time of 135 ns for the PMOS reference switch to

¹ The “on” resistance is hand-calculated based on the transistor size. NMOS and PMOS switches are 2x of minimum sized transistors. PMOS for the reference switch is 2.5x of the minimum sized transistor. NMOS and PMOS in the transmission gates are 4x the minimum sized transistors.

sample the input voltage properly. The PMOS switches are the limiting factor during the bit conversion phase due to a larger “on” resistance compared to the NMOS switches. Assuming that every bit uses the same fixed amount of time, which is limited by the largest capacitor in the array, there are 8 cycles in the conversion phase for total time of 344 ns. Although this assumption of a fixed time is a worst-case estimate for every bit other than the MSB, it allows for a simplified clock circuit. The minimum time for one ADC sample is thus equal to:

$$T_{ADC,min} = T_{sampling} + T_{conversion} = 135ns + 344ns = 479ns \quad 3-11$$

The maximum sampling rate can be expressed as:

$$f_{ADC,max} = \frac{1}{T_{ADC,min}} = 2.09MHz \quad 3-12$$

It should be noted that this minimum time per sample does not yet include the time for the 8 comparisons from the comparator that must be taken into account during the bit conversion phase. The settling time may also vary significantly depending on the actual threshold voltage of each individual transistor, which can significantly vary the “on” resistance. Therefore, equation 3-9 must be satisfied at all times to ensure the acceptable performance of 1 V supply ADC even with the consideration of variations in the threshold voltage and the comparison time included in the total time for one ADC sample, equation 3-12 shows that the design goal of a 50 kHz sampling rate can be achieved.

As mentioned earlier, another source of error from the activity of the switching network can come from charge injection and clock feedthrough. This type of error usually occurs at a

transient event. Therefore, most of the switches in the switching network such as NMOS for ground and PMOS for V_{DD} do not contribute this type of error if they settle fast enough. The PMOS reference switch and the CMOS transmission gates for sampling input voltage are the possible switches contributing charge injection error and clock feedthrough error onto the capacitor array at the end of the sampling phase. The PMOS reference switch is purposely designed to switch off before the CMOS transmission gate switches. The V_{inCMP} node is capacitively isolated. Consequently, the charge injection from the transmission gate to the bottom plate of the capacitors becomes negligible. During the bit conversion phase, there are no switches interacting with the V_{inCMP} node so that top plates of the capacitors are still capacitively isolated. Therefore, the total charge remains fixed on the top plates of the capacitor and no charge error can be introduced onto the V_{inCMP} node during the bit conversion phase. Although the bottom plates of the capacitors are charged either to V_{DD} or ground at all times during the bit conversion phase, the comparator makes a decision only after all the transient events are settled. Therefore, the effect of errors due to charge injection is minimal during the bit conversion phase.

According to the analysis above, the PMOS reference switch is the only switch that may introduce error due to charge injection and clock feedthrough to V_{inCMP} node. Assuming the channel charge injection is equally distributed to two sides of the switch [22], the error voltage on the top plate capacitor plates at the end of the sampling phase is calculated as:

$$\Delta V = \frac{WLC_{ox}(V_{gate,ref} - V_{ref} - V_{TH,ref})}{C_{total}} \quad 3-13$$

where $V_{gate,ref}$ is the gate voltage of the PMOS reference switch, $V_{TH,ref}$ is the threshold voltage of the PMOS reference switch, and C_{total} is the total capacitance of the array seen at the end of sampling phase. Assuming the overlap capacitance is constant, the clock feedthrough error can be expressed as:

$$\Delta V = V_{gate,ref} \frac{WC_{ov}}{WC_{ov} + C_{total}} \quad 3-14$$

where C_{ov} is the overlap capacitance per unit width. The overlap capacitance is very small as compared with C_{total} , therefore, the clock feedthrough error is approximately equal to zero. Using the charge injection cancellation techniques, shown in Figure 3-17, a NMOS switch is added to the circuit so that the opposite charge packets, injected by the PMOS reference switch and the NMOS, cancel each other [22].

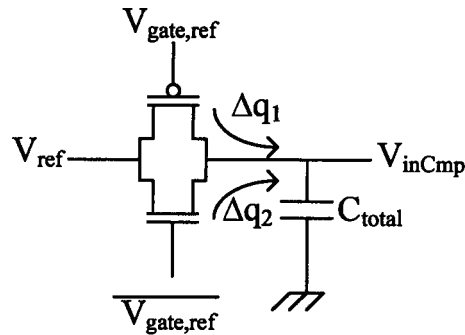


Figure 3-17. One technique for reducing the cause of charge injection by adding a complementary NMOS switch.

The PMOS reference switch creates Δq_1 , consisting of holes while the NMOS switch creates Δq_2 , which are electrons. To ensure Δq_1 (approximately) cancels Δq_2 at the end of sampling phase, the size of the NMOS switch must satisfy equation 3-15.

$$W_P L_P C_{ox} (V_{gate,ref} - V_{ref} - |V_{THP}|) = W_N L_N C_{ox} (V_{ref} - V_{THN}) \quad 3-15$$

As mentioned earlier, the NMOS switch does not cause charge injection only if the switch settles fast enough. To avoid the charge injection caused by the NMOS switch and the PMOS switch which are used to pass ground and V_{DD} , another technique is used to reduce charge injection and the effect of the clock feedthrough, shown in Figure 3-18 [22].

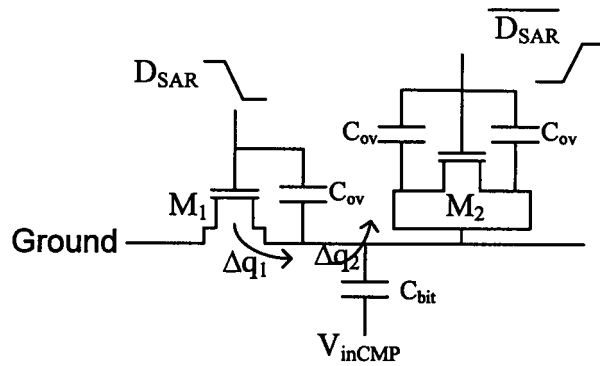


Figure 3-18. Another technique for reducing the cause of charge injection and clock feedthrough.

When the NMOS switch is turned off, charge injection phenomenon is formed by the gate channel of M_1 . Assuming the total charge is equally distributed to the source and drain of M_1 , Δq_1 , can be calculated as:

$$\Delta q_1 = \frac{W_1 L_1 C_{ox}}{2} (D_{SAR} - 0 - V_{TH1}) \quad 3-16$$

where Δq_1 is half of the total charge injected by M_1 , and D_{SAR} is the digital signal from SAR. The charge injection cancellation technique suggests a dummy switch can absorb the channel charge injected from M_1 , which would otherwise be deposited onto C_{bit} . This is true when Δq_1 is equal to Δq_2 .

$$\Delta q_2 = W_2 L_2 C_{ox} (D_{SAR} - 0 - V_{TH2}) \quad 3-17$$

When $W_2=0.5W_1$ and $L_2=L_1$, then Δq_1 is equal to Δq_2 . With this dummy switch size, the effect of clock feedthrough is suppressed. Derivation is shown in Equation 3-18 [22].

$$-D_{SAR} \frac{W_1 C_{ov}}{W_1 C_{ov} + C_{bit} + 2W_2 C_{ov}} + D_{SAR} \frac{2W_2 C_{ov}}{W_1 C_{ov} + C_{bit} + 2W_2 C_{ov}} = 0 \quad 3-18$$

The drawback of this technique is that the assumption of equal splitting the charge injected by M_1 is not valid in general.

3.7 Comparator

As mentioned in earlier section, the comparison time of the comparator determines the major portion of the overall ADC conversion period in which N comparisons must be processed completely. Yet, the comparator also determines the overall performance of the ADC because the resolution of the comparator limits the resolution of the ADC. Due to the low supply limitation, there is limited number of comparator architectures that this design can be used. Here, the comparator circuit is based on the circuit reported by M. Scott [3, 7], which is used to compare the voltage at V_{inCMP} node with the reference voltage, V_{DD} , at each clock cycle to determine whether the previous bit signal should stay high or low. In Figure 3-19, the comparator consists of the input NMOS differential pair determining the input signal level, the cross-coupled PMOS loads, M_3 and M_4 , forming the latch to store the result, the other PMOS devices, M_1 and M_2 , are the switches to reset the V_{O-} and V_{O+} , nodes to V_{DD} . The CMOS inverters are used to convert the NMOS differential output to a comparable logic output comparing with the input. When the reset signal, RST, goes off,

the V_{O-} and V_{O+} will go either to V_{DD} or GND quickly depending on the input signal level. At the same time, transistors M_3 and M_4 , form the latch to store the result, and stay in deep-triode mode. To force the transistors M_3 and M_4 to be out of the latch mode, the RST has to be “on” before the next cycle comparison. Therefore, the RST signal on the schematic refers to the clock. The voltage, V_b , is biased at 550mV by external input voltage.

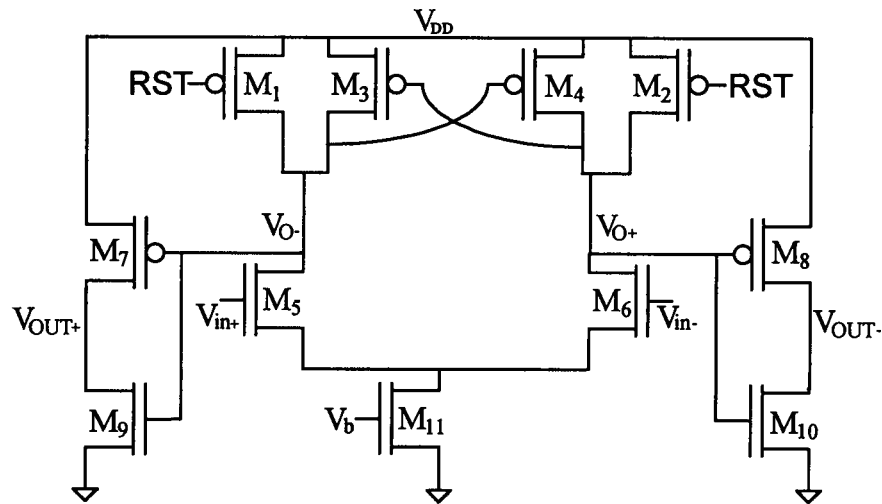


Figure 3-19. Comparator Schematic.

3.8 Successive Approximation Register

The search algorithm in the ADC is implemented in the SAR which consists of digital circuits such as flip-flops which consumes lower power comparing with other analog circuitry. To minimize the amount of energy used in the SAR, the SAR has to be carefully designed to avoid unnecessary signals switching and keep the most of signals static. The SAR in [23] is implemented with required search algorithm while keeping the signal activity

Chapter 4

Measurement Results

This section describes the performance of the ADC which is packaged and tested using a custom PCB board. Each output of the converter is buffered on-chip to allow it to drive the input resistance of the measurement equipment. The ADC is setup for test in Figure 4-1.

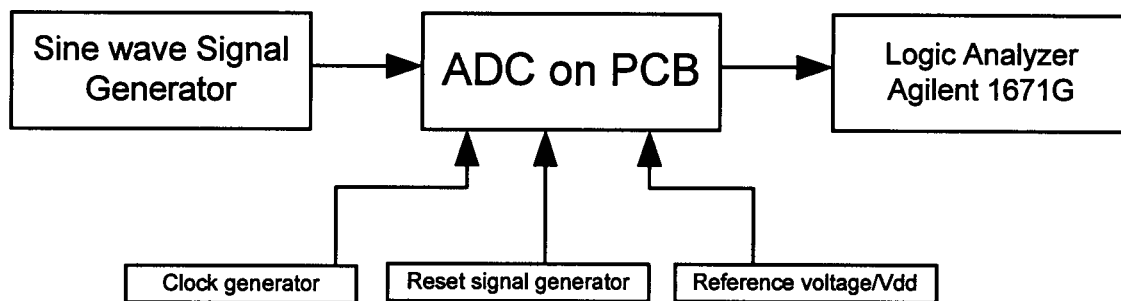


Figure 4-1. ADC test setup

There are several metrics for characterizing the accuracy of the ADC. Most commonly used metrics are differential nonlinearity error, DNL, integral nonlinearity error, INL, and the effective number of bits (ENOB).

4.1 Differential and Integral Nonlinearity

In an ideal ADC, it should have no offset or gain error. Therefore, those errors need to be removed before calculating the DNL and INL. In Figure 4-2, the DNL and INL of an ADC transfer function are defined.

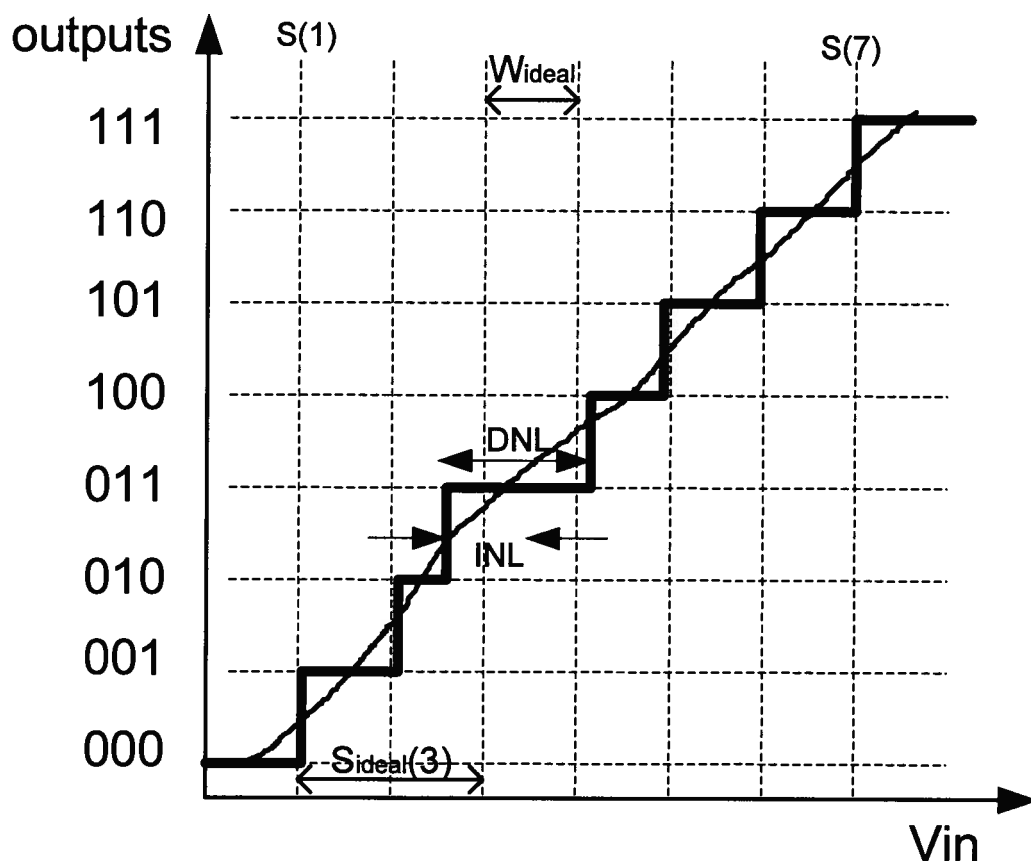


Figure 4-2. Example of an ADC transfer function with DNL and INL

The DNL error defines the difference of the input width of each code with the ideal input width which each dotted grid width in Figure 4-2. Although each unique ADC output code corresponds to a certain input signal range, the output code width can be slightly different in

reality. When the output code corresponds to a large range of the input signal, it means the code appears too many times comparing with other codes. This results the DNL error to be positive. Consequently, a narrow output code indicates a negative DNL. The DNL equation is defined as:

$$DNL(a) = \frac{W(a) - W_{ideal}}{W_{ideal}} \quad 4-1$$

The DNL error unit is defined as an ADC LSB. If the DNL error is -1LSB, it means there is a completely missing output code. In Figure 4-3, the plot shows the DNL of the ADC designed. As mentioned earlier, the output offset and gain error must be removed before calculating the DNL and INL.

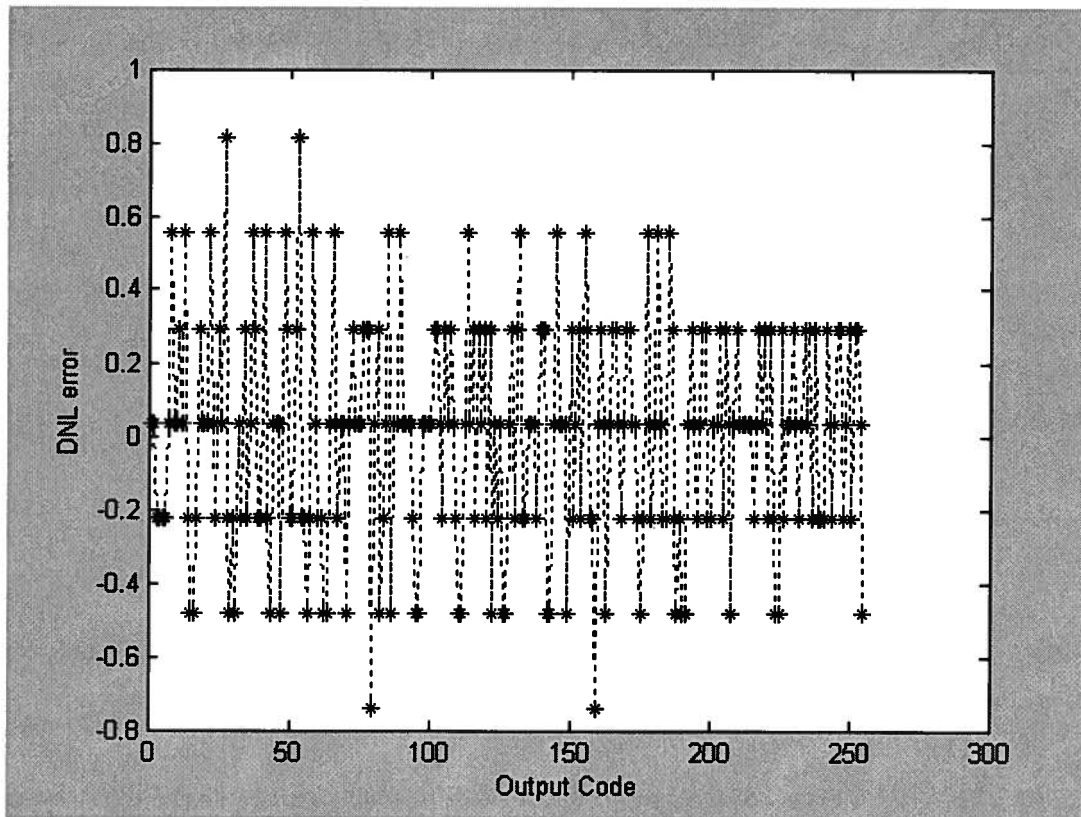


Figure 4-3. Differential nonlinearity error of the ADC.

The INL defines the error between the appearance of a certain output code and the actual ideal appearance of the output code. This is also the integral of the DNL errors. From Figure 4-2, an example of bit 3 INL is labeled. INL error is also presented in terms of ADC LSB. Because the INL measures the integral of the output code errors, the magnitude of an INL error can be greater than 1LSB without having any missing output codes.

$$INL(a) = \frac{S(a) - S_{ideal}}{W_{ideal}} \quad 4-2$$

In Figure 4-4, the INL of the designed ADC is plotted by using Matlab.

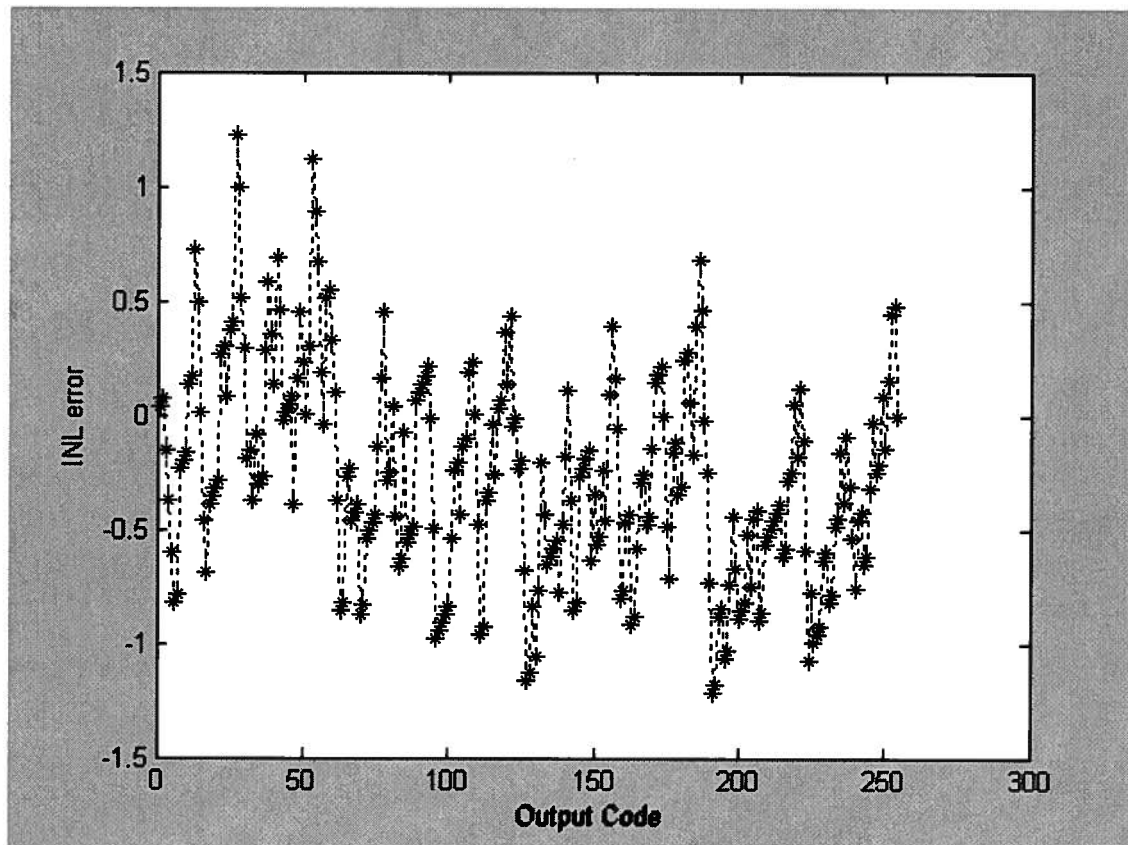


Figure 4-4. Integral nonlinearity error of the ADC.

4.2 Distortion Ratio and Effective Number of Bits

In addition to the DNL and INL, which are usually referred to as static (low frequency) performance measures, another metric to determine the dynamic performance of the ADC is to measure the distortion ratio by applying a sinusoidal input signal and analyze the output codes in terms of frequency content. The frequency power spectrum can later be used to calculate the signal-to-noise and distortion ratio, SNDR, which is the power strength and the effective-number-of-bits, ENOB, which is the actual resolution of the ADC. The ENOB is defined in [14] as:

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad 4-3$$

where the SNDR is the signal power divided by any distortion and noise in the ADC output with unit in dB.

In Figure 4-5, ENOB is plotted as a function of the input frequency at different sampling rate. It shows the best performance at ENOB of 7.09 for an input signal of 10kHz sampled at 100kS/s. The sample-and-hold PMOS switch limits the maximum speed limit of the ADC per sample due to its large settling time for passing V_{DD} .

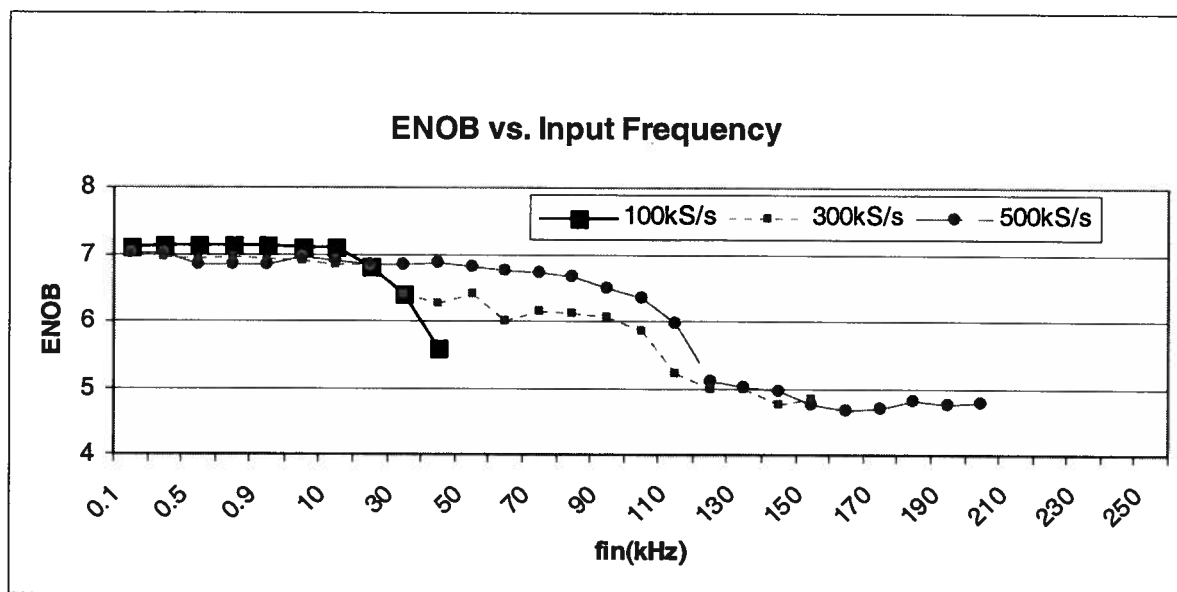


Figure 4-5. Effective number of bits, ENOB, vs input frequency, f_{in}

In Figure 4-6, ENOB is plotted versus sampling frequency with a fixed input frequency of 10kHz.

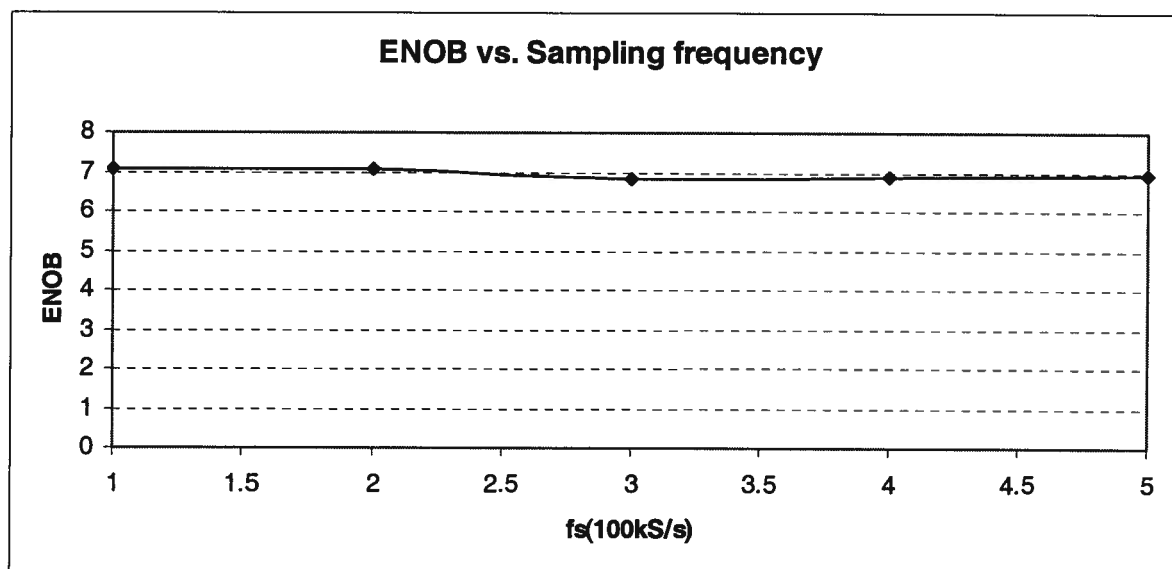


Figure 4-6. ENOB vs sampling frequency, f_s

4.3 Power Consumption

Power consumption of the ADC is one of the most important performance metrics in low-power ADC. Most of the power is consumed at the stage of sampling because the capacitors are charged by both input signal and the reference voltage. In Figure 4-7, the total power consumption includes both the conversion power and standby power due to leakage at different sampling frequency. The higher sampling frequency, the high power the circuit consumes. Figure 4-7 shows measured power consumption versus sampling frequency, f_s , and the relationship is found to be linear.

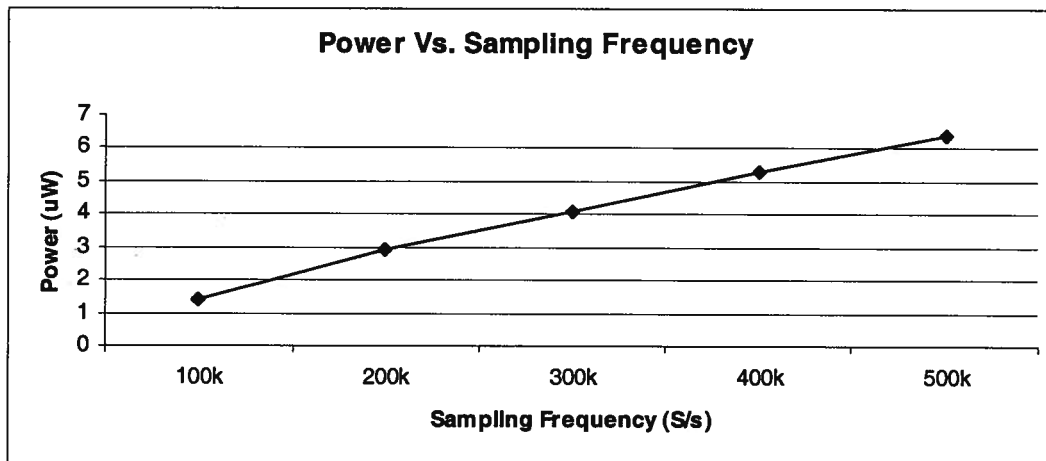


Figure 4-7. Power consumption measured at different sampling frequencies.

With the measurement, the standby leakage power is less than 100pW. Using the figure-of-merit (FoM) defined as:

$$FoM = \frac{Power}{2^{ENOB} \times 2 \times f_{in}} \quad 4-4$$

With $f_{in} = 10\text{kHz}$ with a sampling rate of 100kS/s , a FoM of $514\text{fJ/conversion-step}$ is achieved. The ADC performance comparison between Scott et al [3] and Sauerbrey et al [4], and this work is presented in Table 4-1.

| | Sauerbrey et al [4] | Scott et al [3] | This work |
|-----|------------------------|------------------------|-------------------------|
| FoM | 3.48pJ/conversion step | 2.63pJ/conversion step | 0.514pJ/conversion-step |

Table 4-1. Figure of merit comparison table.

The SAR ADCs reported in [3, 4] having sampling frequency between 100kS/s and 150kS/s while the power consumption ranges between $0.85\mu\text{W}$ to $30\mu\text{W}$ with a 1V supply. The performance of this ADC is listed in Table 4-2.

| | |
|-------------------|---|
| Technology | TSMC $0.18\mu\text{m}$ CMOS |
| Resolution | 8 bits |
| Sampling rate | 100kS/s |
| Supply | 1V |
| Input range | Rail-to-Rail |
| Power consumption | $1.4\mu\text{W}$ (Comparator: $0.8\mu\text{W}$, Voltage Doubler: $0.6\mu\text{W}$) |
| ENOB | 7.09 @ $f_s=100\text{kS/s}$, $f_{in}=10\text{kHz}$ |

Table 4-2. Summary of measured performance.

Chapter 5

Layout

In Figure 5-1, the location of each individual circuit block is marked on the complete SAR ADC die micrograph. The overall circuit area is 0.25 mm^2 . From this figure, it can be seen that the majority of the ADC area is occupied by the capacitor array. The entire layout was done very conservatively in terms of area, especially the capacitor array. Each unit capacitor was spaced out by roughly 1.5X away from each other to reduce the parasitic capacitance between adjacent unit capacitors. The core area could be reduced by minimizing the capacitance spacing in the next iteration.

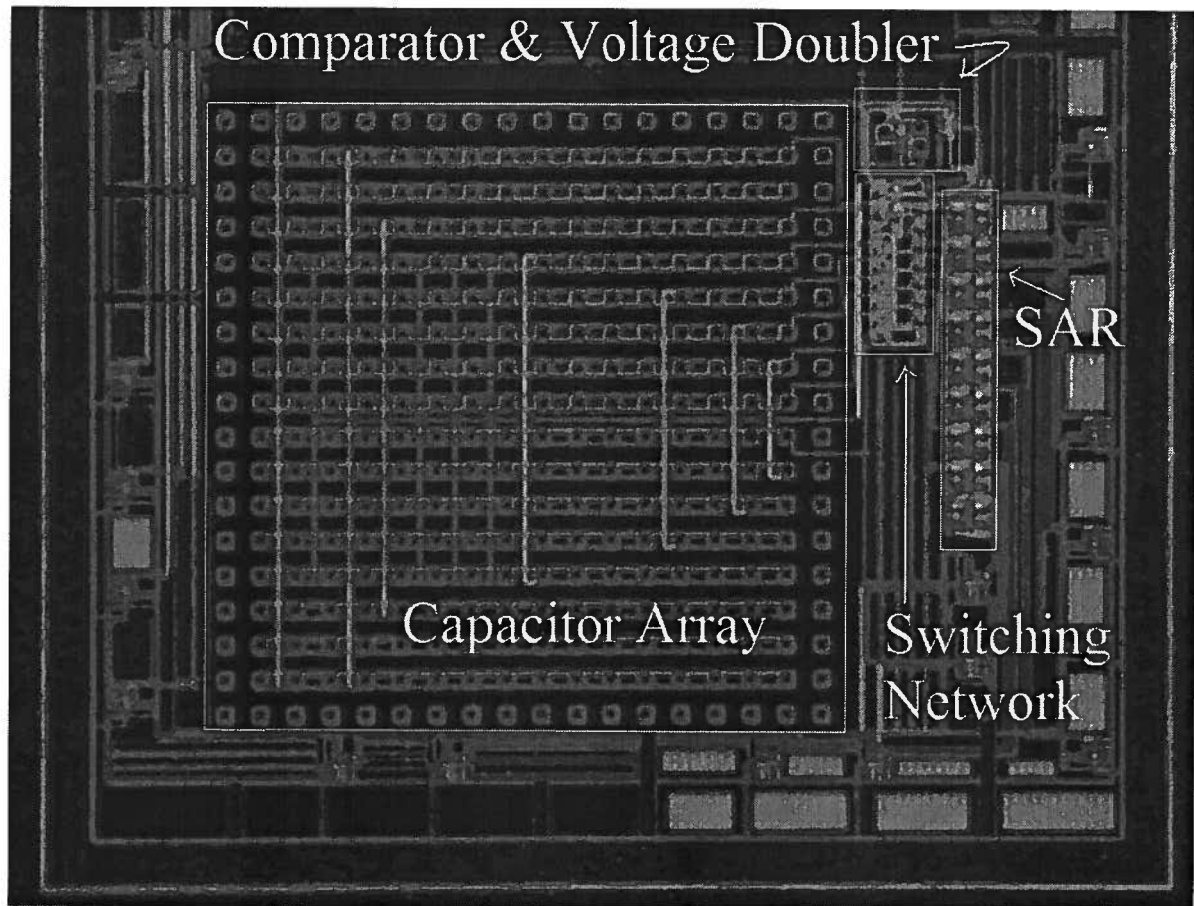


Figure 5-1. Complete SAR ADC die micrograph with circuit location noted.

5.1 Device Matching

Quite often, the test results of a circuit may not match with the simulation result after the chip fabrication. There are many possibilities to cause this discrepancy such as extra parasitics, latch-ups, leakage of the device, or even device mismatch. To minimize these problems, layout plays an important role. An excellent circuit may not work after fabrication if the layout of the circuit was done poorly.

In most circuit designs, controlling the gate voltage determines the amount of current flow through the transistor. Therefore, the poly formation of the transistor becomes extremely

important. Poly is known as a resistive material so a little amount of poly difference can make the transistor behaviour different. The layout of the comparator used in this ADC is shown in Figure 5-2 for all the poly gate contacts are either on the top or bottom. During the process of the fabrication, the poly layer is formed on the entire wafer. In order to get rid of the places that poly is not needed, the technique called “etching” is used. In [24], the critical process control for resist and poly etch chamber is discussed. The dummification for poly mask is also explained. At almost all times, all the matched devices are preferred to be placed in the same orientation which means channel direction of devices must be the same. Some studies were done to examine the intrinsic statistical fluctuations in device characteristics due to different orientation of the poly placement [25].

[illegible]

perfect when the devices are properly placed in the same orientation. Placing the channel in the same direction only can minimize the different amount of poly being etched between devices. In order to match the devices better, interdigitation of the fingers between devices is required. The metal routing is also important and critical. In Figure 5-2, half of the layout is placed on the left of the centre line which shows the layout is done symmetrically on the left and right for the metal routing and device placement. The inputs and outputs are designed to be dual ports and therefore they see the same load and can be easily routed out from either left or right side of the block without adding extra unbalanced parasitics.

5.2 Capacitor matching and necessary dummies

The layout of the capacitor array that was discussed in Section 3.5 is shown in Figure 5-3. The unit cell capacitors placed along the perimeter of the capacitor array acts as dummy capacitors which allow the unit capacitor inside the capacitor array experience the same amount of parasitics from all its neighbors. This ensures the unit capacitor picks up equal amount of capacitance from four side neighbors. However, the distance between capacitors is far enough to make the parasitic capacitance less than 2% of the unit cap value. The routings are done carefully to avoid picking up the unnecessary parasitic capacitance along the route. From Figure 5-3, most of the connections are done across the 128C unit capacitors is because the ratio between the parasitic capacitance associated with the other capacitor routing being added to the 128C capacitor and the 128C capacitor is negligible.



Figure 5-3. Capacitor array layout

5.3 Latch-ups and guard rings

Latch-up is a failure mechanism caused by the parasitic thyristors, also called as parasitic silicon controlled rectifier, which are created by between MOS substrate. Once the parasitic bipolar is accidentally triggered, it allows high amount of current continuously flow through it and possibly cause permanent damage to the device if the current is large.

The cause of the latch-up exists between the junction and the bulk of the CMOS process. In Figure 5-4, the parasitic resistance between different junctions simply forms the lateral bipolar MOSFETs, PNP and NPN, from a CMOS inverter. After re-drawing the circuit from the cross section, shown in Figure 5-5, the trigger path can be seen more easily.

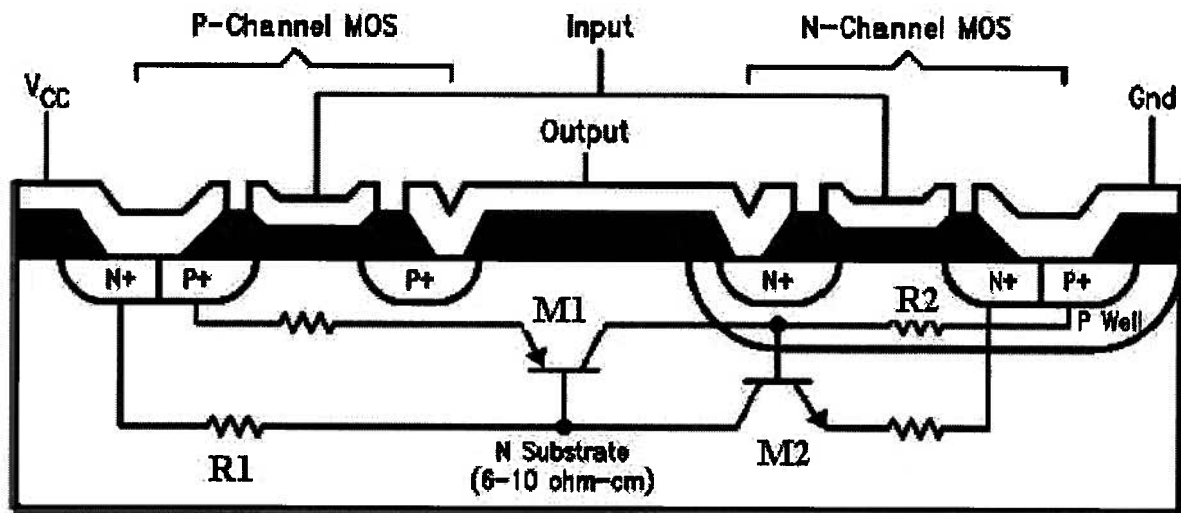


Figure 5-4. Latch-up circuit model from a CMOS inverter cross section [26]

The gate of M1, which is the N-well tie of the p-channel MOS, should be tied to the power supply and the gate of M2, which is the P-substrate tie of the n-channel MOS, should be tied to ground. However, the lateral resistors R1 and R2 form between the power supply and ground if the N-well tie and P-substrate tie is not properly laid out. As soon as the leakage current being injected to the substrate, it triggers the latch-up loop.

Although nowadays the vendors of CMOS IC are aware of the latch-up problems and improved the designs and process to reduce the chance of latch-up happening under normal

usage, the CMOS designers still need to be aware of the issues. The good practice for preventing latch-up happening is to put solid guard rings around each circuit if possible.

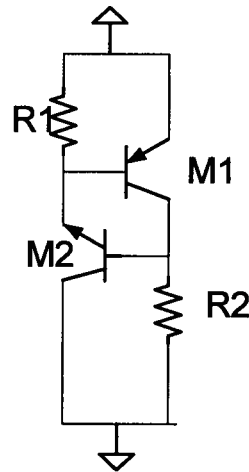


Figure 5-5. Latch-up circuit is re-drawn from figure 5-4.

The advantage of the guard ring is minimizing the distance from the collector to the base-emitter region of M1 and M2; therefore, the resistance of R1 and R2 is reduced. The cross section of the added guard ring is shown in Figure 5-6.

Chapter 6

Conclusions

The design and performance measurement results of a 1V 8-bit ultra-low-power successive approximation register analog-to-digital converter are presented. The ADC is implemented in a 0.18 μm CMOS technology without using any low- V_T devices. The ADC achieves an ENOB of 7.09 for a 10kHz input signal at sampling rate of 100kS/s while consuming $1.4\mu\text{W}$ from a 1V supply. The ADC is intended for use in power-constraint applications such as micro-sensors requiring ultra-low-power devices due to the limited energy and lifetime of their power supply.

Possible future work topics include: study of achievable accuracy with the proposed structure for capacitor arrays with the focus on reducing the parasitics capacitance in the capacitor array and the capacitor array, techniques to improve ENOB, and techniques to improve power consumption such as turning off the comparator during the sampling phase [7] and decreasing the standby power of blocks.

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