A DSP-based AC Electronic Load for Unintentional Islanding Tests

by

Wei Feng

B.Sc., Tsinghua University, Beijing, China, 2004
M.Sc., Institute of Electrical Engineering, CAS, China, 2007

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF
THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF APPLIED SCIENCE

in

The Faculty of Applied Science

(Electrical and Computer Engineering)

THE UNIVERSITY OF BRITISH COLUMBIA

(Vancouver)

August 2009

Abstract

The distributed generation (DG) system for the renewable energy resources is being used more and more widely around the world in the past decades. In order to protect the whole power system from the islanding situation, the interface inverters of the DG system have to pass the unintentional islanding test. In this study, a single phase AC electronic load is introduced to simulate the local loads under unintentional islanding conditions.

This thesis proposes a proper schematic of the electronic loads based on the H-bridge dc-dc converter and analyzes the performance of this system with PowerSIM. Then, a set of specifications for different ranges of the electronic loads are calculated through theoretical formulas and the PSIM simulations. Meanwhile, the transfer function of the system is also derived to analyze the stability of the PI control system.

According to the theoretical analysis and simulations, a control program is implemented based on the Texas Instruments (TI) Digital Signal Processor (DSP) TMS320F2407A for the different kinds of electronic loads.

A test circuit is then built to validate the performance of the system. Some experiments are performed for the resitive, inductive and capacitive loads respectively.

Table of Contents

Appendices

List of Tables

List of Figures

Acknowledgements

I wish to express my deepest gratitude to my supervisor, Dr. William G. Dunford. During the thesis research, Dr. William G. Dunford provided enormous help and encouragement. This work would not be possible without his broad knowledge and patient instruction.

I would like to thank Dr. Juri Jatskevich for his insights and valuable suggestions toward the completeness of this thesis.

I would like to express my thanks to Michel AlSharidah who worked with me together in this research and shared with me his experience and optimism in the islanding tests and simulations.

Thanks are extended to my colleges Tom De Rybel, Dean Chen, Yong Zhang and Mehmet Sucu for their great suggestions.

Finally, I am expressing my sincerest gratitude to my parents and my girlfriend for their love and support during my studies.

Chapter 1

Introduction

1.1 Project Background

Distributed Generation (DG) which is gaining more and more interest around the world generally refers to small-scale (typically $1kW$ – $50MW$) electric power generators that produce electricity at a site close to customers or that are tied to an electric distribution system. Among DG technologies, some are tried and tested but a number are new and developing technologies which use renewable energy sources, such as wind energy, biofuels and photovoltaic (PV) energy.

Compared with the traditional larger power stations, DG promises significant reductions in the power transportation cost and reduces the capital and operating costs which will encourage their further growth. The integration of Distributed Generation into the main electricity networks doesn't only bring in numerous benefits but some security issues. The anti-islanding protection[1] is the most frequent issue raised by DG interconnection to the utility networks because the island is an unregulated power system. Its behaviour is unpredictable due to the power mismatch between the load and generation and the lack of voltage and frequency control. Therefore, it is creating the possibility of damage to customer equipment in a situation over which the utility has no control.

In wind and PV energy applications, the inverter is the most frequently used interface[2] which interconnects DG to the grids. According to IEEE standard 1547, the inverters used as interface in the distributed generation systems have to pass a series of tests and evaluation before interconnection to the utility. The unintentional islanding test is to verify that the anti-islanding protection of the DG interconnection component is capable of detecting the islanding conditions and ceasing to energize the electric power system. In the unintentional islanding test, a resistance, inductance and capacitance (RLC) load is employed as simulated local loads and shall be tuned at the nominal frequency of electricity networks.

With increasing of the power rating of DG, the size of RLC loads used in the unintentional islanding test become bigger and bigger which makes

the tuning process of RLC circuits very time-consuming and inconvenient. Therefore, a compact and programmable electronic load is needed which can simulate different RLC networks.

1.2 System Overview

1.2.1 Unintentional Islanding Test Scheme

As described in the previous section, an interface inverter has to pass the unintentional islanding test before put into practical use. IEEE standard 1547 defines a generic system for unintentional islanding test which is illustrated in Figure 1.1.

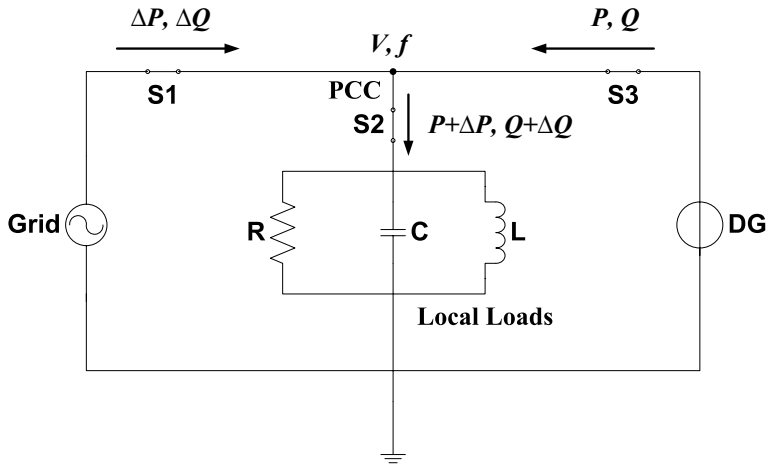

Figure 1.1: Generic System for Unintentional Islanding Test

In the normal operation mode, switches $S1$, $S2$ and $S3$ are closed and the electricity network, local loads and DG interface inverter are interconnected together. The real and reactive power consumed in local loads are provided by both utility network and distributed generation system. Once the switch $S1$ is open, the electricity network is unable to provide power for customers and local loads are connected solely to DG system which is called "islanding situation".

If the power generated by the DG system matches the RLC load power, i.e., in Figure 1.1, $\Delta P = \Delta Q = 0$. Under this condition, even if switch $S1$ is open, the voltage and frequency at the Point of Common Coupling (PCC)

will not be changed and an unintentional islanding situation occurs which is considered the worst case for islanding detection.

1.2.2 AC Electronic Loads for Unintentional Islanding Test

In this thesis, a single phase AC electronic load is designed to replace the *RLC* load shown in Figure 1.2 so that the tuning of *RLC* circuits can be achieved more easily by adjusting the values of electronic loads in the software.

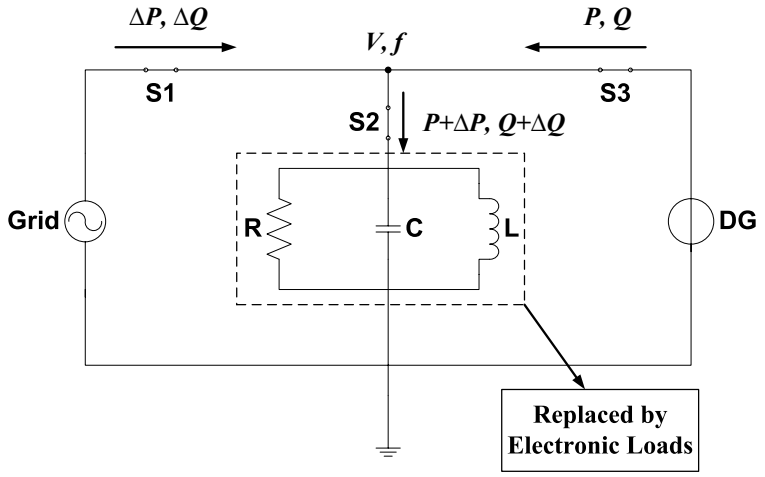

Figure 1.2: Electronic Loads for Unintentional Islanding Test

The AC electronic loads consist of three parts:

- A bidirectional H-Bridge based current source.
- Voltage and current sensor circuits.
- A TMS320LF2407A DSP control board.

1.3 Thesis Objective

The objective of this thesis is to clarify the practical approaches needed to set up a programmable AC electronic load used in unintentional islanding test. The specific objectives include:

- To find a suitable structure of the bidirectional current source

- To find the design criteria of H-bridge based current source for the different ranges of the resistive, inductive and capacitive electronic loads with the $60Hz$ AC source.
- To build a DSP-controlled H-bridge based current source.
- To develop a control method for the programmable RLC electronic loads
- To generate a DSP program for the TMS320LF2407A DSP.
- To simulate different ranges of resistive, inductive and capacitive loads with a $60Hz$ sinusoidal voltage excitation and verify the theoretical analysis using the prototype.

The thesis is organized into six chapters. Chapter 1 gives a brief introduction of the system and outlines the objectives of this thesis. In Chapter 2, the principles of the AC electronic loads are proposed and the PSIM simulations for different electronic loads are performed to give a set of specifications of the system. Chapter 3 is focused on hardware setup for the electronic loads. Chapter 4 will be dealing with software implementation. Some design illustration concerning software is presented. Selective experimental results are included in Chapter 5. The last chapter concludes the design and the implementation and proposes some work needed to be done in the future.

Chapter 2

Principles of the Simulated Loads

In this chapter the principles of the simulated loads will be introduced step by step. First of all, the schematic of the simulated loads will be proposed carefully. Secondly, the ac small-signal model of the circuit will be derived as well as the stability of the system. Then, the relationship between the parameters of the circuit and the range of the simulated loads will be analyzed. At the end, a series of PSIM simulations for different kinds of loads will be performed and several groups of parameters will be given for different ranges of the simulated loads.

2.1 Schematic of Electronic loads

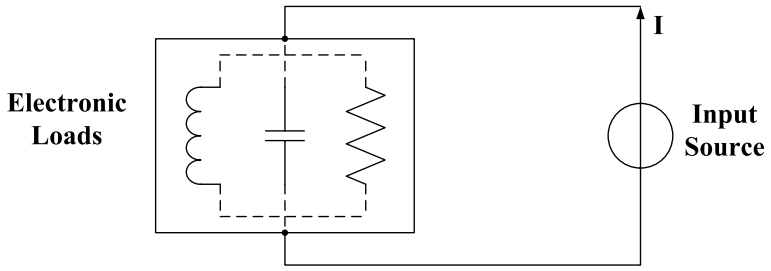

Figure 2.1: Diagram of Electronic Loads

Figure 2.1 shows the diagram of the electronic loads. It can be seen that the different load will draw the different current I from the input voltage source and thus the load characteristics can be changed if the output current of the source is under control.

For an AC input source, the direction of the output current could be either positive or negtive, which means a bidirectional controllable current source is needed to control the output current of the source so that it can

simulate different load characteristics. In this project, an H-bridge inverter-based bidirectional current source will be designed as an electronic load.

2.1.1 H-Bridge Bidirectional Current Source

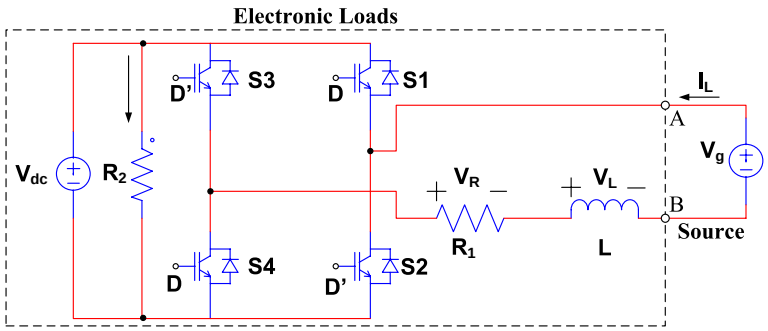

Figure 2.2: Controllable Current Source with Regulated DC Bus Voltage

The schematic of the H-bridge inverter-based bidirectional current source is illustrated in Figure 2.2. It is very similar to the traditional H-bridge dc-dc converter but the difference is that the port "AB" is used as the input port instead of the output port.

The parameters of the circuit is explained as follows:

- DC bus voltage. In order to make this circuit work properly, the DC bus voltage is regulated by a DC power supply which must be positive so that there are no short-circuits caused by the flywheel diodes which may lead to the serious damage of IGBTs.
- Resistor R_1. In the real system, a series resistor R_1 always exists because of the equivalent series resistance of the inductor L and the resistance of the conductors.
- Resistor R_2. The resistor R_2 is a dumping resistor and used to provide a closed loop for the inductor current I_L.
- Inductor L. the series inductor L is capable of smoothing the current I_L so that this circuit can work as a current source.

2.1.2 The Range of Inductor Current

In the following parts, the range of the current I_L will be derived in order to analyze the electronic load characteristics. In simple terms of, a DC voltage source V_g will be applied in the circuit as an input source. However, the results are also available for low-frequency AC voltage sources, such as $60Hz$.

As depicted in Figure 2.2, the duty ratio D is the fraction of time that the switches $S1$ and $S4$ spend in the conducting position, and is a number between zero and one. The complement of the duty ratio, D', is defined as $(1 - D)$, which means the fraction of time that the switches $S2$ and $S3$ spend in the conducting status.

The small ripple approximation and the principles of inductor volt-second balance[3] will be applied here to find the steady state of the inductor current I_L. Figure 2.3 illustrates the operation topologies of the H-bridge inverter with regulated DC bus when the switches commutate.

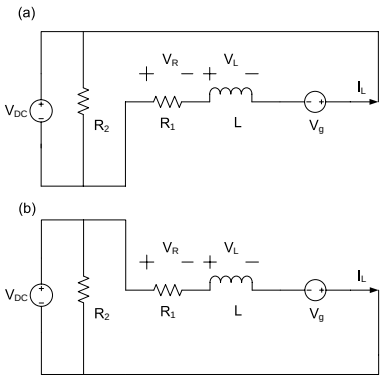

Figure 2.3: H-Bridge Inverter With Regulated DC Bus: (a) the first subinterval: D, (b) the second subinterval: D'

As illustrated in the Figure 2.3(a), during the first subinterval, DT, the switches $S1$ and $S4$ are on and the other switches $S2$ and $S3$ are off. The inductor voltage for this subinterval is given by

$$v_L = V_g - V_{dc} - i_L \times R_1 \tag{2.1}$$

Use of the small ripple approximation, $i_L \approx I_L$, leads to

$$v_L = V_g - V_{dc} - I_L \times R_1 \tag{2.2}$$

Similarly, during the second subinterval, $D'T$, the status of the switches are illustrated in the Figure 2.3(b). The inductor voltage for this subinterval is

$$v_L = V_g + V_{dc} - i_L \times R_1 \tag{2.3}$$

Use of the small ripple approximation again leads to

$$v_L = V_g + V_{dc} - I_L \times R_1 \tag{2.4}$$

According to the principles of inductor volt-second balance, the total volt-seconds applied to the inductor over one switching period is

$$< v_L >= 0 \tag{2.5}$$

Substitution of Eq.(2.2) and Eq.(2.4) into Eq.(2.5), and the result is

$$D\left(V_g - V_{dc} - I_L R_1\right) + D'\left(V_g + V_{dc} - I_L R_1\right) = 0 \tag{2.6}$$

Upon collecting terms, one obtains

$$V_g = \left(2D - 1\right) V_{dc} + I_L R_1 \tag{2.7}$$

From Eq.(2.7), the average inductor current I_L can be obtained

$$I_L = \frac{V_g + \left(1 - 2D\right) V_{dc}}{R_1} \tag{2.8}$$

Therefore, the controllable range of the current flowing through the inductor L can be derived easily according to Eq.(2.8). When the switches $S2$ and $S3$ are always on, the inductor current I_L reaches to the maximum value; when the switches S_1 and S_4 are always off instead, the minimum value can be obtained. The results are given by

$$\begin{array}{rcl} I_{L\,\max} & = & (V_g + V_{dc})/R_1 \\ I_{L\,\min} & = & (V_g - V_{dc})/R_1 \end{array} \tag{2.9}$$

2.2 AC Small-Signal Modeling and PI Control Method

In this section, the ac small-signal modeling technique is employed for the derivation of the system transfer function and a conventional PI controller is designed accordingly for the PWM current controller.

2.2.1 AC Small-Signal Model

The ac small-signal model is always used in the analysis of the dynamic performance of power electronic circuits. With this model, the transfer function of the system can be derived which is very useful for the stability analysis of the control system. However, this model only works at the low-frequency and the disturbance of the switching frequency will be neglected.

According to Figure 2.3, the voltage equations during these two intervals can be derived respectively.

$$\begin{aligned} d: \quad v_g &= v_{dc} + \langle i_L(t)\rangle_{Ts} \cdot R_1 + L\frac{d\langle i_L(t)\rangle_{Ts}}{dt} \\ d': \quad v_g &= -v_{dc} + \langle i_L(t)\rangle_{Ts} \cdot R_1 + L\frac{d\langle i_L(t)\rangle_{Ts}}{dt} \end{aligned} \tag{2.10}$$

Where $\langle i_L(t)\rangle_{Ts}$ denotes the average of $\langle i_L(t)\rangle$ over an interval of length T_s which represents one PWM switching period.

Using Eq.(2.10), the average of voltage v_g over one switching period equals:

$$\left(d+d'\right)v_g = \left(d-d'\right)v_{dc} + \left(d+d'\right)\left[\langle i_L(t)\rangle_{Ts} \cdot R_1 + L\frac{d\langle i_L(t)\rangle_{Ts}}{dt}\right] \tag{2.11}$$

Upon collecting items, it can be rewritten as:

$$v_g = (2d-1)v_{dc} + \langle i_L(t)\rangle_{Ts} \cdot R_1 + L\frac{d\langle i_L(t)\rangle_{Ts}}{dt} \tag{2.12}$$

Perturbing the inductor current, duty-cycle, input voltage and DC bus voltage with small signals of $\hat{i_L}$, $\hat{d}$, $\hat{v_g}$ and $\hat{v_{dc}}$ respectively; also, assuming the quiescent value of these variables are I_L, D, V_g and V_{dc} then:

$$\langle i_L(t)\rangle_{Ts} = I_L + \hat{i_L} \tag{2.13}$$

$$d = D + \hat{d} \tag{2.14}$$

$$v_g = V_g + \hat{v_g} \tag{2.15}$$

$$v_{dc} = V_{dc} + \hat{v_{dc}} \tag{2.16}$$

Insert Eq.(2.13) to (2.16) into Eq.(2.12), one obtains:

$$V_g + \hat{v_g} = \left[2\left(D + \hat{d}\right) - 1\right]\left[V_{dc} + \hat{v_{dc}}\right] + \left(I_L + \hat{i_L}\right) R_1 + L\frac{d\left(I_L + \hat{i_L}\right)}{dt} \tag{2.17}$$

Linearizing Eq.(2.17), the ac small signal equation can be derived:

$$\hat{v_g} = (2D-1)\,\hat{v_{dc}} + 2V_{dc}\,\hat{d} + R_1\,\hat{i_L} + L\frac{d\,\hat{i_L}}{dt} \tag{2.18}$$

Taking the Laplace transform for Eq.(2.18), the inductor current to duty ratio transfer function can be obtained:

$$G_{id}(s) = \left.\frac{\hat{i_L}}{\hat{d}}\right|_{\hat{v_{dc}},\hat{v_g}=0} = \frac{-2V_{dc}}{R_1 + sL} \tag{2.19}$$

2.2.2 The Transfer Function of Control System

In this system, a traditional PI compensator is chose for the current feedback loop due to the uncompensated system containing a single pole. The transfer function of the compensator can be expressed as:

$$G_c(s) = k_p + \frac{k_i}{s} \tag{2.20}$$

The function of the pulse-width modulator is to produce the duty ratio d that is proportional to the output voltage of the compensator. Figure 2.4 shows the schematic diagram of the pulse-width modulator.

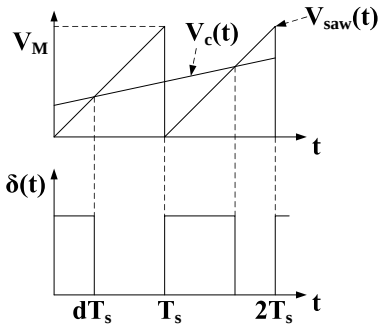

Figure 2.4: Schematic Diagram of PWM Modulator

In terms of the waveform above, the duty cycle d will be a linear function of V_c. Hence, we can write

$$d\left(t\right) = \frac{v_c\left(t\right)}{V_M} \tag{2.21}$$

Perturbation and linearization of Eq.(2.21), the transfer function of the pulse-width modulator is:

$$G_{pwm}\left(s\right) = \frac{\hat{d}}{\overset{\wedge}{v_c}} \tag{2.22}$$

Based on the analysis above, the system transfer function can be derived as follows (Figure 2.5). Note that the pwm modulator outputs d' in our design, and thus a negative transfer function of the circuit is applied. In addition, a saturation block is also added to the PI compensator to eliminate the effect of integral saturation.

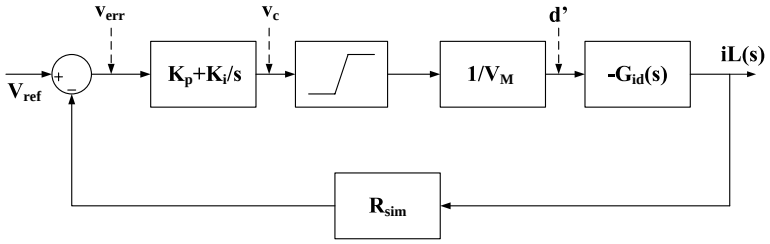

Figure 2.5: Block Diagram of the System Transfer Function

2.2.3 Control System Stability Analysis

In this project, a set of PI parameters of the control system is obtained using PSIM simulations and practical experiments:

- PI parameters: $k_p = 1$ and $k_i = 5 \times 10^5$.
- Saturation block: -20 to 20.
- PWM modulator: $V_M = 40$.

According to the analysis above, the stability of these PI parameters can be investigated using Simulink7.0 and LTIViewer in MATLAB2008a. The bode diagram of the open-loop transfer function is depicted in Figure 2.6. It can be seen that the phase margin is always larger than zero so the system is stable.

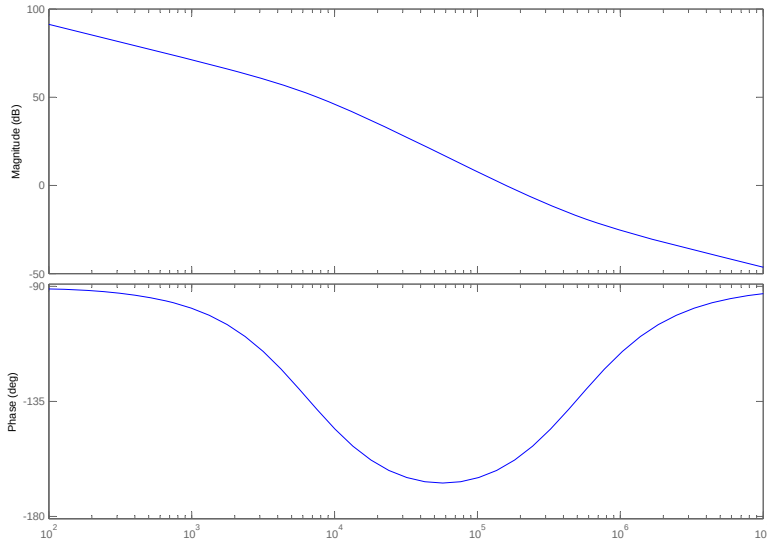

Figure 2.6: Bode Diagram of the Open-Loop Transfer Function

2.3 System Performance Analysis

The electronic load designed in this project works in the switching mode, so the triangle waveforms are used to track the given sinusoidal waveforms. In order to meet the accuracy requirements, the effects of circuit parameters on the switching ripples and the system response time have to be investigated carefully. Therefore, this section will explore the relationship between the circuit parameters and the system performance.

2.3.1 Current Ripple

Figure 2.2 shows that the inductor L which prevents the current from being changed suddenly plays the most important role in the current control. In this section, the effect of circuit parameters on the current ripple will be investigated carefully and the formula of the current ripple will be derived for the calculation of circuit parameters according to the given accuracy demands .

The current ripple used here is defined as $\Delta i_L/2I_L$. Where Δi_L is the peak-to-peak current change and I_L is the average current over one switching period. The following parts will introduce the relationship between the current ripple and the circuit parameters for the simulated resistive, inductive

and capacitive loads separately.

Current Ripple for Resistive Loads

In simple terms, a DC voltage source V_g is employed as the input voltage source as shown in Figure 2.2 and the circuit is controlled to simulate the resistance characteristic. To the extent of an low-frequency AC voltage source, such as 60Hz, the analysis still works fine because the AC source can be discretized into a series of DC voltage source at low frequency.

As illustrated in Figure 2.2, the current change Δi_L is related to the inductor L and the current ripple $\Delta i_L/2I_L$ should be as small as possible so that the high frequency noise of the electronic loads can be decreased greatly. Only consider the intervals $D'T$ that $S2$ and $S3$ are on. According to the inductance characteristic, one obtains

$$L\frac{di_L}{dt} = v_L \tag{2.23}$$

Where

$$v_L = V_{dc} + V_g - v_{R_1} \tag{2.24}$$

When $R_1 \ll R_{sim}(R_{sim}$: simulated resistor), v_{R_1} can be ignored

$$v_L \approx V_{dc} + V_g \tag{2.25}$$

Insert Eq.(2.25) into Eq.(2.23), one obtains

$$L\frac{di_L}{dt} \approx V_{dc} + V_g = (1+k)\,V_g \tag{2.26}$$

Where $V_{dc} = V_g$, then the current change Δi_L is equal to

$$\Delta i_L = \frac{(1+k)\,V_g}{L} \times \Delta t \tag{2.27}$$

Using Eq.(2.8), the steady state of inductor current I_L is given by

$$\begin{aligned} I_L &= \tfrac{V_g+(1-2D)V_{dc}}{R_1} \\ &= \tfrac{V_g+(1-2D)kV_g}{R_1} \\ &= \tfrac{1+(1-2D)k}{R_1}V_g \end{aligned} \tag{2.28}$$

Because the circuit is working as resistance loads, the average current of inductor I_L is also equal to

$$I_L = \frac{V_g}{R_{sim}} \tag{2.29}$$

The duty ratio D can be derived through combination of Eq.(2.28) and Eq.(2.29)

$$\begin{aligned} &\tfrac{1+(1-2D)k}{R_1} \times V_g = \tfrac{V_g}{R_{sim}} \\ &\Rightarrow D = \tfrac{1}{2k}\left(k+1-\tfrac{R_1}{R_{sim}}\right) \end{aligned} \tag{2.30}$$

The time interval Δt can be obtained using Eq.(2.30)

$$\begin{aligned} \Delta t &= (1-D) \times T_{pwm} \\ &= \tfrac{(k-1)R_{sim}+R_1}{2 \cdot k \cdot R_{sim}} \times T_{pwm} \end{aligned} \tag{2.31}$$

Combining Eq.(2.27) and Eq.(2.29), the ratio of the current change Δi_L to inductor current I_L is equal to

$$\frac{\Delta i_L}{I_L} = \frac{(k+1)\,R_{sim}}{L} \times \Delta t \tag{2.32}$$

Insert Eq.(2.31) into Eq.(2.32), the current ripple is obtained

$$\begin{aligned} \tfrac{\Delta i_L}{2I_L} &= \tfrac{1}{2} \times \tfrac{(k+1)R_{sim}}{L} \times \tfrac{(k-1)R_{sim}+R_1}{2 \cdot k \cdot R_{sim}} \times T_{pwm} \\ &= \tfrac{1}{2} \times \tfrac{T_{pwm}}{L} \times \tfrac{\left(k^2-1\right)R_{sim}+(k+1)R_1}{2k} \end{aligned} \tag{2.33}$$

The equation above indicates that the current ripple $\Delta i_L / 2I_L$ is a function of the simulated resistive load R_{sim}, the PWM period T_{pwm} and the value of the inductor L when k and series resistor R_1 are constant. According to this function, the following relationship can be concluded:

- The maximum impedance of the simulated loads which is achievable on this system can be derived by Eq.(2.33) when all the circuit parameters and the current ripple requirement are given.
- The larger inductor L, the smaller the current ripple. Hence, the minimum value of the inductor L can be calculated with Eq.(2.33) when the simulated resistive load R_{sim} and the current ripple are given.
- The higher switching frequency f_{pwm}, the smoother the current ripple.

Current Ripple for Inductive and Capacitive Loads

The expression of current ripple for the inductive and capacitive loads are exactly same, so here we only take the inductive loads for example to derive the current ripple expression.

From the schematic of the current source, it can be concluded that the largest current ripple will occur when the AC input source reaches zero. Therefore, following the similar process shown in the previous section, one obtains

$$L\frac{di_L}{dt} \approx V_L \tag{2.34}$$

Where

$$v_L = V_{dc} - v_{R_1} \tag{2.35}$$

When $R_1 \ll Z_{sim}$(Z_{sim}: the impedance of the simulated inductive or capacitive loads), v_{R_1} can be ignored

$$v_L \approx V_{dc} \tag{2.36}$$

Insert Eq.(2.36) into Eq.(2.34), one obtains

$$L\frac{di_L}{dt} \approx V_{dc} = kV_g \tag{2.37}$$

Then the current change Δi_L is equal to

$$\Delta i_L = \frac{kV_g}{L} \times \Delta t \tag{2.38}$$

According to Eq.(2.8), when $V_g = 0$, the average current I_L over one switching cycle is given by

$$I_L = \frac{1-2D}{R_1} kV_g \tag{2.39}$$

When $V_g = 0$, the average current I_L also equals

$$I_L = \frac{V_g}{\|Z_{sim}\|} \tag{2.40}$$

Combining Eq.(2.39) and (2.40), the duty cycle D is equal to

$$D = \frac{1}{2}\left(1 - \frac{R_1}{k\,\|Z_{sim}\|}\right) \tag{2.41}$$

When $R_1 \ll \|Z_{sim}\|$, the duty cycle D is approximately 0.5 and the time interval $\Delta t = 0.5T_{pwm}$. Therefore, combining Eq.(2.38) and (2.40), the current ripple for inductive or capacitive loads is

$$\frac{\Delta i_L}{2I_L} = \frac{1}{2} \times \frac{k\,\|Z_{sim}\|}{L} \times \frac{T_{pwm}}{2} \tag{2.42}$$

The expression above shows the similar function as the resistive loads. However, compared with the function of the resistive loads, the current ripple of the simulated inductive or capacitive loads will be larger with the same circuit parameters.

2.3.2 Relationship between Response Time and Z_{sim}

To simulate electronic loads under low-frequency voltage source, the response time of the system should be small enough so that the system is capable of tracking the required load characteristic curves. The following derivations are based on the resistive simulated loads and the conclusion is also available for the inductive or capacitive simulated loads.

According to Eq.(2.27) and (2.31), the current change function can be derived

$$\Delta i_L = \frac{(1+k)\,V_g}{L} \times \frac{(k-1)\,R_{sim} + R_1}{2k \times R_{sim}} \times T_{pwm} \tag{2.43}$$

It can be derived that if the circuit parameters keep constant, the current change Δi_L will increase with the decreasing of R_{sim}. However, the series inductor L will prevent the current from changing suddenly and thus the response time will increase greatly when the simulated load R_{sim} decreases. Hence, for a given series inductor L and other given parameters, the minimum achievable impedance of the simulated loads can be found considering the proper response time. In the following part, the unit step response of the system will be investigated to find the proper minimum values for the given parameters previously.

2.3.3 Conclusions of System Performance

The previous sections explain the relationship between the circuit parameters and the system performance. Therefore, a general design procedure can be used according to the requirements of the system performance:

- First of all, determine the proper values of k and f_{pwm} and the maximum impedance of the simulated loads.

- Secondly, according to the current ripple requirement, calculate the minimum inductor L with Eq.(2.33) or Eq.(2.42).
- At the end, find the minimum impedance of the simulated loads according to the given circuit parameters so that the response time of the system is small enough for the $60Hz$ AC source.

2.4 Calculation of Circuit Parameters

The schematic and performance of the system have been explained previously. This section will introduce how to calculate the circuit parameters according to the given accuracy demands and a set of values of circuit parameters will be listed for the different ranges of the simulated loads. The analysis proposed here is all based on the PSIM simulations and the theoretical derivation.

2.4.1 Introduction of PSIM Simulation Diagram

Powersim (PSIM) is a powerful circuit simulation software which is specially suited to power electronic circuit simulations. All kinds of semiconductor parts and the control blocks have been integrated in the software package, which makes it very easy to use.

In order to analyze the circuit parameters, a PSIM simulation program for the simulated resistive loads will be used in this section and the conclusions obtained from this system is also suitable for the inductive and capacitive loads with some minor changes.

Figure 2.7 shows the schematic of the resistive load simulation consisting of the H-Bridge current source and the control program. The control program senses the inductor current i_L and the input voltage source V_g to calculate the error between the actual voltage and the demanded voltage using equation:

$$error = V_{source} - I_{sense} \times R_{sim} \tag{2.44}$$

Where R_{sim} represents the resistance of the simulated resistive loads. With a set of proper PI parameters (given in the previous section), the error V_{err} can be obtained which is used to compared with a saw-tooth waveform to generate PWM signals.

In the PSIM simulation, the per-unit system is employed and the voltage and current base values are equal to $30V$ and $0.78125A$ separately which are also used in the DSP program and thus the impedance base value is 38.4Ω. The choice of the base values will be explained in the chapter four.

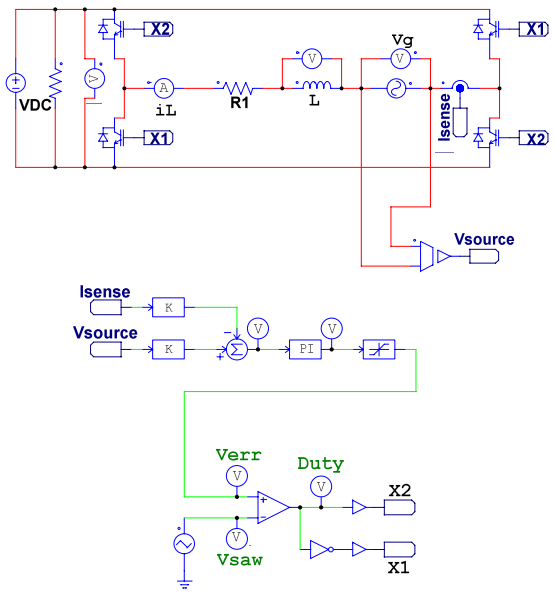

Figure 2.7: Resistance Load Simulation

2.4.2 DC Bus Voltage: V_{dc}

As discussed in the previous sections, the DC bus voltage V_{dc} must be positive so that there are no short-circuits and according to Eq.(2.9), V_{dc} should be greater than or equal to V_g to increase the range of the inductor current, in other words, to increase the range of the electronic loads.

A parameter of k is defined as the ratio of V_{dc} to V_g and should be larger than or equal to 1. However, if k is 1, it's going to take a very long period to decrease the current due to the zero reverse voltage across the series inductor; if k is much larger than 1, the current ripple will be increased significantly.

Through the practical experiments, the parameter of k is kept to be 1.3 to improve the dynamic performance of the device as well as the current ripple.

2.4.3 Series Resistor: R_1

From Eq.(2.9), $I_{L\max} = (V_g + V_{dc})/R_1$, it can be seen that the minimum impedance of electronic loads is decided by the series resistor R_1. When

$V_{dc} = 1.3V_g$, the minimum simulated impedance $|Z_{sim}|_{\min} = R_1/2.3$. In our system, the series resistor R_1 is 17Ω and the minimum limitation of the simulated impedance is about 7.4Ω.

2.4.4 Switching Frequency: f_{pwm}

As discussed previously, the current ripple depends upon the switching frequency f_{pwm} and the higher switching frequency, the smaller current ripple. In this project, the switching frequency f_{pwm} is set to $20kHz$ which is the most typical frequency of IGBTs.

2.4.5 Inductor: L

It has been discussed in the previous sections that the value of inductor L is determined by the requirement of the current ripple (Eq.(2.33) and Eq.(2.42)).

On the other hand, once the inductor value and other parameters are chosen, the range of the impedance of the simulated loads can be calculated with the consideration of both the current ripple and the response time. The following parts will show how to calculate the inductor value and the range of the simulated loads.

Calculation of Inductor L

For resistive loads, three different ranges of the simulated loads are given in Table 2.1. From Eq.(2.33), a set of minimum values of the series inductor L can be calculated for the resistive loads according to the given current ripple and the maximum impedance of the simulated loads.

Assume the current ripple $\Delta i_L/2I_L$ should be less than 0.3, the minimum inductors for the simulated resistive loads are shown as follows.

Range of R_{sim}	L_{min}	Maximum Current Ripple
$0 - 2p.u.$	$2.6mH$	0.34 (actual value: 0.3)
$0 - 20p.u.$	$26mH$	0.21
$0 - 200p.u.$	$260mH$	0.19

Table 2.1: Series Inductors for Different Ranges of Resistance Loads: switching frequency $f_{pwm} = 20kHz$, voltage ratio $k = 1.3$, series resistor $R_1 = 17\Omega$ and the impedance base value $\|Z\| = 38.4\Omega$

It can be found that the current ripple is larger than 0.3 at $R_{sim} = 2p.u.$ but the real current ripple is equal to 0.3 because the equation we used here is derived with the approximation of $R_1 \ll R_{sim}$ but $R_{sim} = 2p.u.$ is comparable with R_1. Therefore, the actual current ripple at small simulated resistance is less than the calculated value (the real current ripple can be found using the PSIM simulations in Figure 2.20).

The similar results for the inductive or capacitive simulated loads can be obtained with Eq.(2.42). Considering the hardware consistency, the same set of values of the series inductor L as shown in Table 2.1 will be used in the calculations, so the maximum impedance of the simulated loads and the associated current ripple are calculated as follows.

Maximum $\|Z_{sim}\|$	Series Inductor L	Maximum Current Ripple
$1.25p.u.$	$2.6mH$	0.30
$12.5p.u.$	$26mH$	0.30
$125p.u.$	$260mH$	0.30

Table 2.2: Series Inductors for Different Ranges of Inductive or Capacitive Loads: switching frequency $f_{pwm} = 20kHz$, voltage ratio $k = 1.3$, series resistor $R_1 = 17\Omega$ and the impedance base value $\|Z\| = 38.4\Omega$

Practically, with the consideration of simplicity, another set of values of $\|Z_{sim}\|$ is given in Table 2.3 after the rounding adjustment.

The parameters listed above are all based on the assumption that the current ripple is less than 0.3. If a smaller current ripple is required for the specific application, the simplest approach is just to increase the switching frequency f_{pwm} proportionally and retain other parameters.

Maximum $\|Z_{sim}\|$	Series Inductor L	Maximum Current Ripple
$1p.u.$	$2.6mH$	0.24
$10p.u.$	$26mH$	0.24
$100p.u.$	$260mH$	0.24

Table 2.3: Series Inductors for Different Ranges of Inductive or Capacitive Loads: switching frequency $f_{pwm} = 20kHz$, voltage ratio $k = 1.3$, series resistor $R_1 = 17\Omega$ and the impedance base value $\|Z\| = 38.4\Omega$

2.4.6 Calculation of the Range of Z_{sim}

As discussed above, once the current ripple requirement and the series inductor are given, the maximum achievable impedance of the simulated loads is also set up. However, not all impedances less than the maximum value are able to be simulated with this system. In this section, the response time of the system will be analyzed and the minimum achievable impedance of the simulated loads can be determined by the response time.

Simulation Results of the Response Time

Here we takes $L = 26mH$ for example to find the minimum limitation of the impedance. In the PSIM simulations shown in Figure 2.7, the parameters are: $f_{pwm} = 20kHz$, $R_{sim} = 2p.u.(76.8\Omega)$, $R_1 = 17\Omega$ and $L = 26mH$. To explore the unit step response, a unit step input voltage source V_g is applied.

Figure 2.8 depicts the unit step response of the system at $R_{sim} = 2p.u.$. Replacing the unit step source with a $60Hz$ AC source, the voltage across $R_{sim}(2p.u.)$ is plotted in Figure 2.9. It can seen that the rise time is equal to $0.46ms$ and the settling time is $3.50ms$ which is fast enough for the application of $60Hz$.

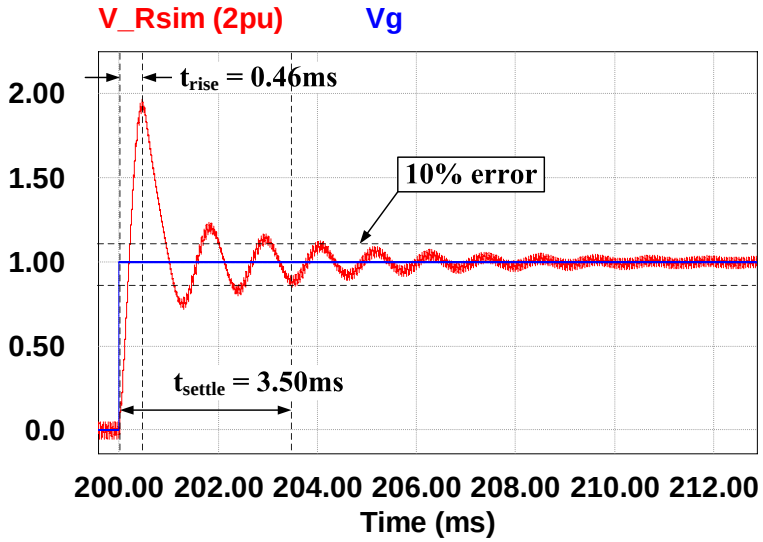

Figure 2.8: Unit Step Response at $R_{sim} = 2p.u.$

However, if the resistive simulated load R_{sim} keeps going down to $1p.u.$,

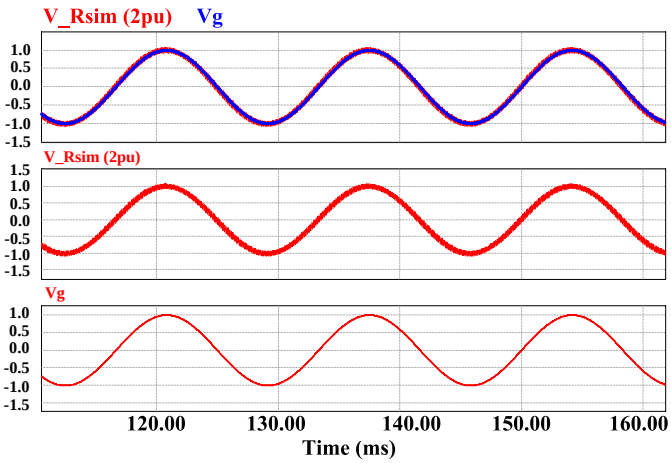

Figure 2.9: Voltage across $R_{sim} = 2p.u.$

the unit step response time will increase consistently as shown in Figure 2.10. Replacing the unit step input source with a 60Hz AC source, the voltage waveform across R_{sim} is depicted in Figure 2.11. It can be seen that the average value of V_{Rsim} is no longer equal to the input voltage due to the long response time.

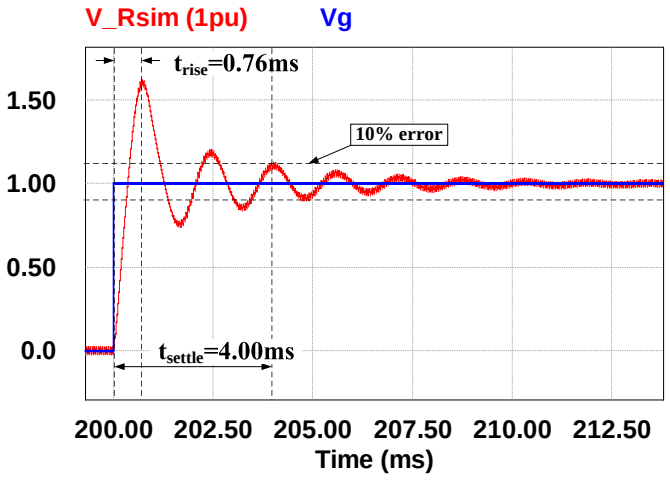

Figure 2.10: Unit Step Response at $R_{sim} = 1p.u.$

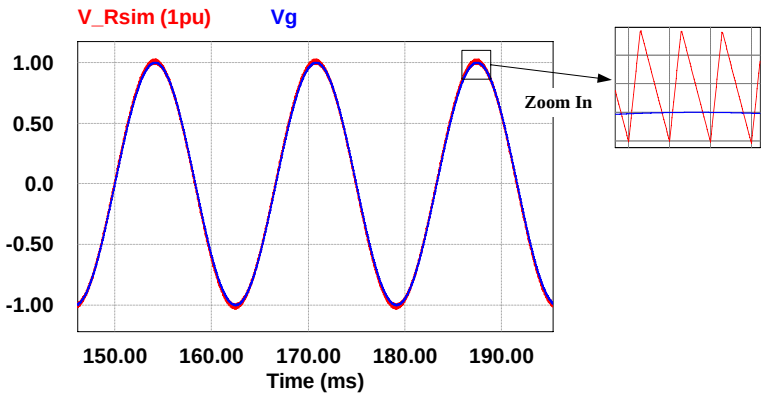

Figure 2.11: Voltage across $R_{sim} = 1p.u.$

On the other hand, if R_{sim} increases, the response time will keep decreasing and the response time for $R_{sim} = 20p.u.$ is illustrated in Figure 2.12. Compared with the response time at $R_{sim} = 2p.u.$, the response time at $R_{sim} = 20p.u.$ is much faster but more ripples.

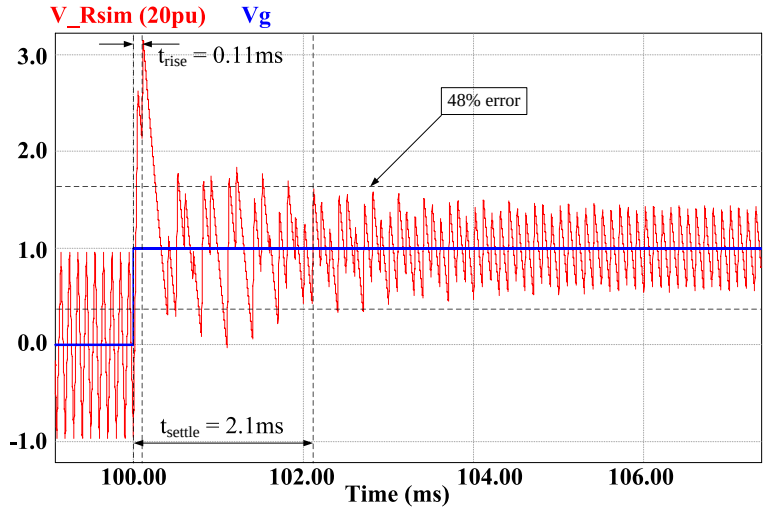

Figure 2.12: Unit Step Response at $R_{sim} = 20p.u.$

The Range of Z_{sim}

Based upon the discussion above it can be concluded that the minimum achievable impedance of the simulated loads is determined by the response time if the value of the series inductor is given. With the help of PSIM simulations, a set of values of the minimum R_{sim} is found in Table 2.4.

Series Inductor L	Minimum R_{sim}
$2.6mH$	$\geq 0.2p.u.$
$26mH$	$\geq 2pu$
$260mH$	$\geq 20pu$

Table 2.4: Minimum R_{sim} for the Given Series Inductor: switching frequency $f_{pwm} = 20kHz$, voltage ratio $k = 1.3$, series resistor $R_1 = 17\Omega$ and the impedance base value $\|Z\| = 38.4\Omega$

Similarly, the minimum impedance of the inductive or capacitive simulated loads is also able to be found in the table below with the PSIM simulation programs.

Series Inductor L	Minimum L_{sim} (or C_{sim})
$2.6mH$	$\geq 0.1p.u.$
$26mH$	$\geq 1pu$
$260mH$	$\geq 10pu$

Table 2.5: Minimum L_{sim} (or C_{sim}) for the Given Series Inductor: switching frequency $f_{pwm} = 20kHz$, voltage ratio $k = 1.3$, series resistor $R_1 = 17\Omega$ and the impedance base value $\|Z\| = 38.4\Omega$

2.4.7 Duty Ratio D

This section will introduce the effect of the duty cycle D on the range and resolution of the simulated loads. According to Eq.(2.28) and Eq.(2.29), a resistive simulated load can be represented as:

$$R_{sim} = \frac{V_g}{I_L} = \frac{R_1}{1 + (1 - 2D) \cdot k} \tag{2.45}$$

In a continuous system, the value of R_{sim} could be infinite when the denominator is approaching zero. However, the real system we used in this

project is a digital system with a 16-bit DSP so the step size of the duty ratio D is $1/2^{16}$. With this step size, the range of the resistive load is illustrated in Figure 2.13 for the given parameters above.

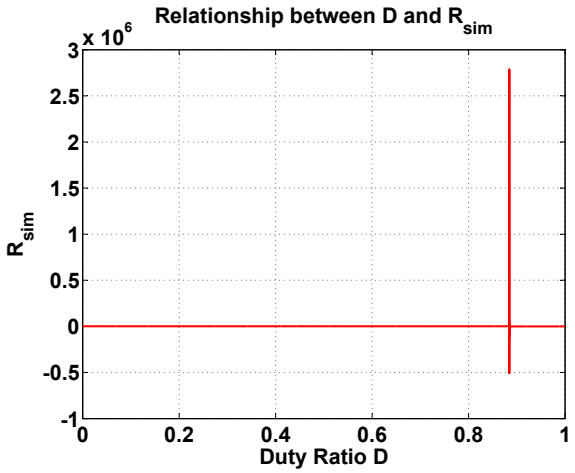

Figure 2.13: Relationship between R_{sim} and D

It can be found that the slope of the function $R_{sim}(D)$ will increase significantly when the duty cycle D approaches the value which makes the denominator equal zero (Here it is 0.8846). This phenomenon indicates that if the step size of D is fixed, the resolution of the simulated resistive load is going down when D approaches that sensitive value.

In order to achieve a higher resolution of the simulated resistive load, the simulated impedance should fall into a reasonable range depending on the required resolution. Using Eq.(2.45), the resolution can be calculated for the simulated resistive loads shown in the previous section (See Table 2.6).

Range of R_{sim}	Resolution (%)
$< 2p.u.$	≤ 0.018
$< 20p.u.$	≤ 0.18
$< 200p.u.$	≤ 1.8

Table 2.6: The Resolution of R_{sim}: switching frequency $f_{pwm} = 20kHz$, voltage ratio $k = 1.3$, series resistor $R_1 = 17\Omega$ and the impedance base value $\|Z\| = 38.4\Omega$

For the impedance larger than $200p.u.$, the resolution becomes too small to be applied in the practical system. Figure 2.14 depicts that the resolution of R_{sim} at $2000p.u.$ is going up to 18.7% and this error is too big for a practical application.

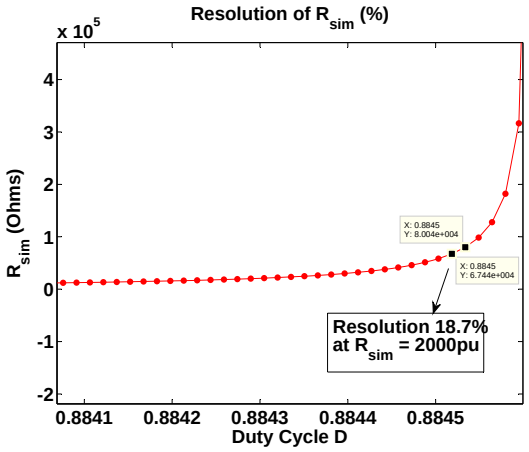

Figure 2.14: Resolution at $R_{sim} = 2000pu$

According to Eq.(2.41), the similar results can be derived for the inductive or capacitive simulated loads (as shown in Table 2.7)

Range of L_{sim} (or C_{sim})	Resolution (%)
$< 1p.u.$	≤ 0.0089
$< 10p.u.$	≤ 0.090
$< 100p.u.$	≤ 0.90

Table 2.7: The Resolution of L_{sim} (or C_{sim}): switching frequency $f_{pwm} = 20kHz$, voltage ratio $k = 1.3$, series resistor $R_1 = 17\Omega$ and the impedance base value $\|Z\| = 38.4\Omega$

2.4.8 Specifications of Electronic Loads

From the previous discussion, a series values of the circuit parameters can be derived for the resistive, inductive and capacitive simulated loads shown in the Table 2.8 and 2.9 respectively.

R_{sim}	Inductor L	Resolution (%)	Current Ripple
$0.5 - 2p.u.$	$2.6mH$	≤ 0.018	≤ 0.3
$2 - 20p.u.$	$26mH$	≤ 0.18	< 0.3
$20 - 200p.u.$	$260mH$	≤ 1.8	< 0.3

Table 2.8: Specifications for the Resistive Simulated Loads: switching frequency $f_{pwm} = 20kHz$, , voltage ratio $k = 1.3$, series resistor $R_1 = 17\Omega$ and the impedance base value $\|Z\| = 38.4\Omega$

L_{sim} (C_{sim})	Inductor L	Resolution (%)	Current Ripple
$0.5 - 1p.u.$	$2.6mH$	≤ 0.00089	≤ 0.24
$1 - 10p.u.$	$26mH$	≤ 0.090	≤ 0.24
$10 - 100p.u.$	$260mH$	≤ 0.90	≤ 0.24

Table 2.9: Specifications for the Inductive or Capacitive Simulated Loads: switching frequency $f_{pwm} = 20kHz$, , voltage ratio $k = 1.3$, series resistor $R_1 = 17\Omega$ and the impedance base value $\|Z\| = 38.4\Omega$

These parameters are all obtained based on the 0.3 current ripple assumption and increasing the switching frequency is able to achieve the smaller current ripple.

2.5 Simulations of Electronic Loads

In this section, RLC electronic loads will be simulated using PSIM8.0 separately to verify the principles derived in the previous sections and the calculations of the specifications suggested above.

2.5.1 Resistive Load Simulation

The PSIM simulation program for the resistive simulated loads has been depicted in Figure 2.7. Based upon the previous introduction and the parameters, the simulations can be performed and the waveforms are shown below for the current ripple analysis.

Current Ripple and Inductor L

According to Eq.(2.33), the current ripple can be calculated when $R_1 \ll R_{sim}$. But when the resistance of the simulated load is comparable to R_1, the

actual ripples are smaller than the calculated values obtained with Eq.(2.33).

For example, assume the switching frequency $f_{pwm} = 20kHz$, voltage ratio $k = 1.3$, series resistor $R_1 = 17\Omega$ and series inductor $L = 2.6mH$. The calculated ripple is equal to 0.19 at $R_{sim} = 0.5p.u.$, 0.24 at $R_{sim} = 1p.u.$ and 0.34 at $R_{sim} = 2p.u.$. However, in the PSIM simulations, the actual ripples can be obtained (See Figure 2.15 to 2.20) and equal 0.13, 0.19 and 0.3 separately which are smaller than the calculated values.

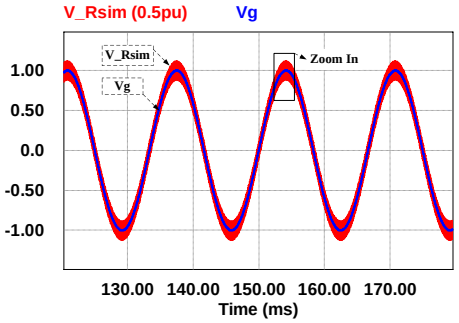

Figure 2.15: $R_{sim} = 0.5p.u.$ at $f_{pwm} = 20kHz$

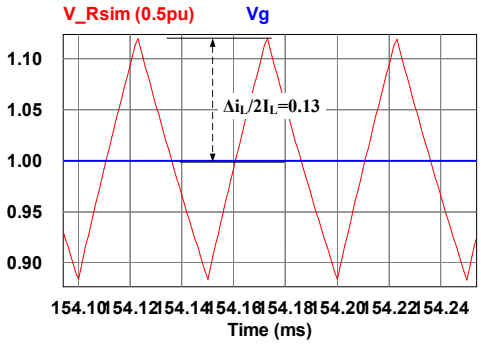

Figure 2.16: Current Ripple at $R_{sim} = 0.5p.u.$

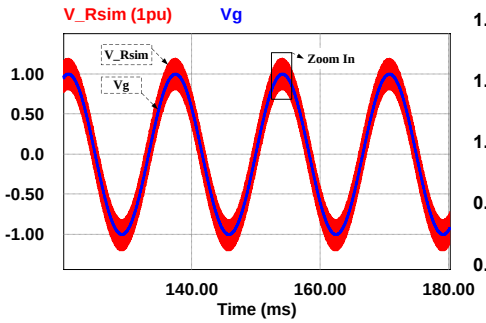

Figure 2.17: $R_{sim} = 1p.u.$ at $f_{pwm} = 20kHz$

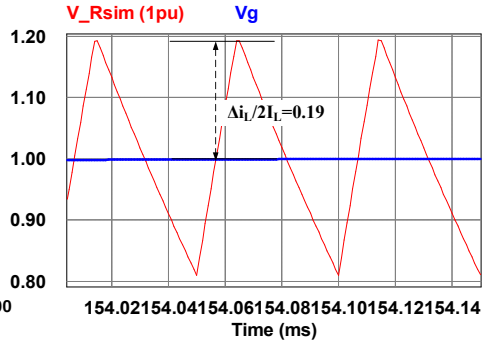

Figure 2.18: Current Ripple at $R_{sim} = 1p.u.$

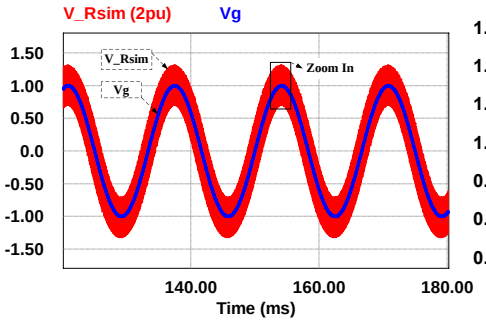

Figure 2.19: $R_{sim} = 2p.u.$ at $f_{pwm} = 20kHz$

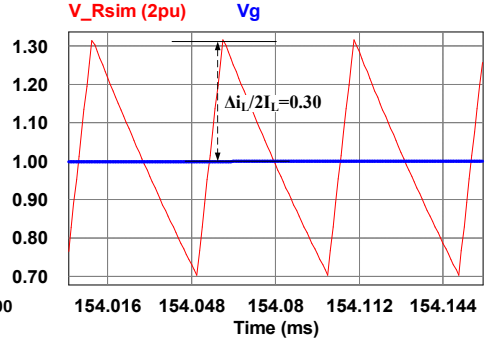

Figure 2.20: Current Ripple at $R_{sim} = 2p.u.$

To investigate the current ripples for $2p.u. \leq R_{sim} \leq 20p.u.$, the $2.6mH$ inductor is replaced with a $26mH$ inductor to simulate $R_{sim} = 2p.u.$ and $20p.u.$ respectively.

Using Eq.(2.33) again, the current ripple equals 0.21 at $R_{sim} = 20p.u.$. The waveforms of voltage across R_{sim} and the associated current ripples are depicted in Figure 2.21 to 2.24.

Figure 2.24 shows that the current ripple at $R_{sim} = 20p.u.$ equals 0.20 which is very close to the calculated value 0.21 because $R_{sim} = 20p.u. = 768\Omega$ is much bigger than $R_1 = 17\Omega$.

In Figure 2.22,the current ripple is 0.03 at $R_{sim} = 2p.u.$ and $L = 26mH$. Compared with the value when L is $2.6mH$, the current ripple goes down to 10% which is inversely proportional to the series inductor L same as the relationship shown in Eq.(2.33).

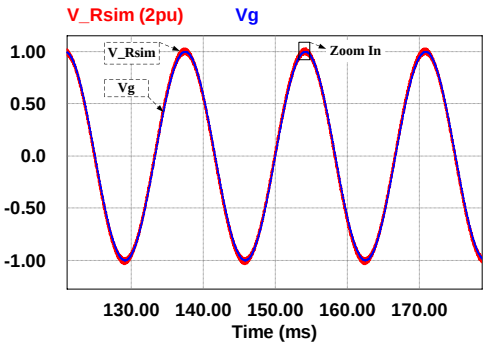

Figure 2.21: $R_{sim} = 2p.u.$ at $f_{pwm} = 20kHz$

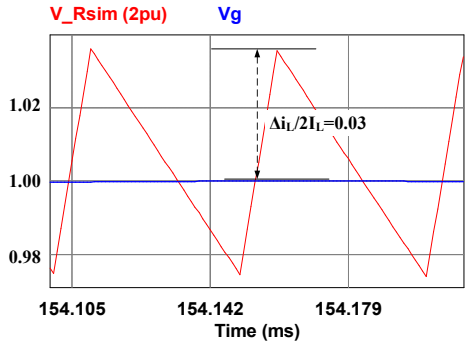

Figure 2.22: Current Ripple at $R_{sim} = 2p.u.$

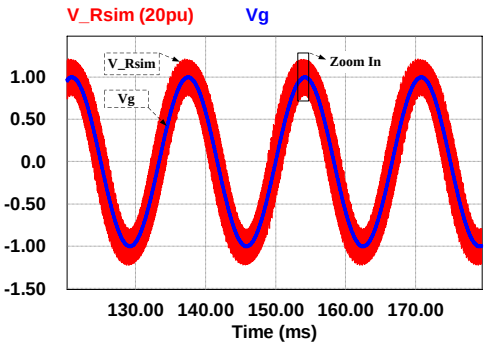

Figure 2.23: $R_{sim} = 20p.u.$ at $f_{pwm} = 20kHz$

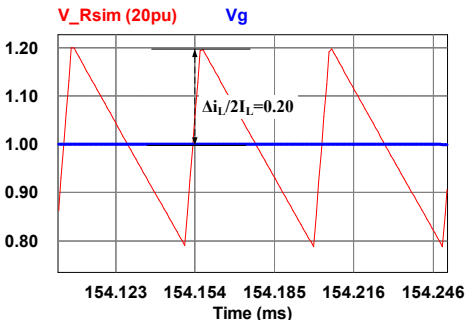

Figure 2.24: Current Ripple at $R_{sim} = 20p.u.$

Current Ripple and Switching Frequency f_{pwm}

Using Eq.(2.33), the current ripple is inversely proportional to the switching frequency f_{pwm} and the PSIM simulation results are shown in following figures.

It can be seen in Figure 2.26 that the current ripple $\Delta i_L/2I_L$ equals to 0.61 and is 2 times of the current ripple at $20kHz$ which proves the inversely proportional relationship between the current ripple and the switching frequency.

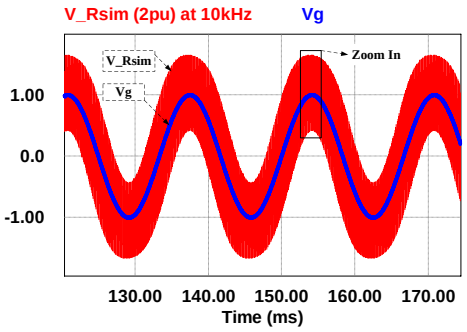

Figure 2.25: $f_{pwm} = 10kHz$, $R_{sim} = 2p.u.$ and $L = 2.6mH$

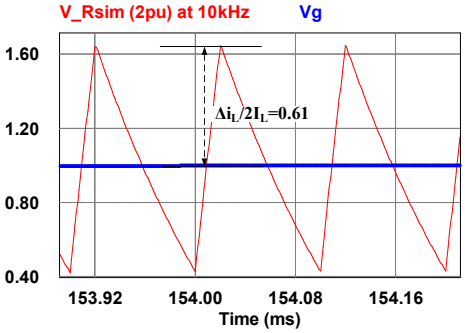

Figure 2.26: Current Ripple at $R_{sim} = 2p.u.$ and $f_{pwm} = 10kHz$

2.5.2 Inductive Load Simulation

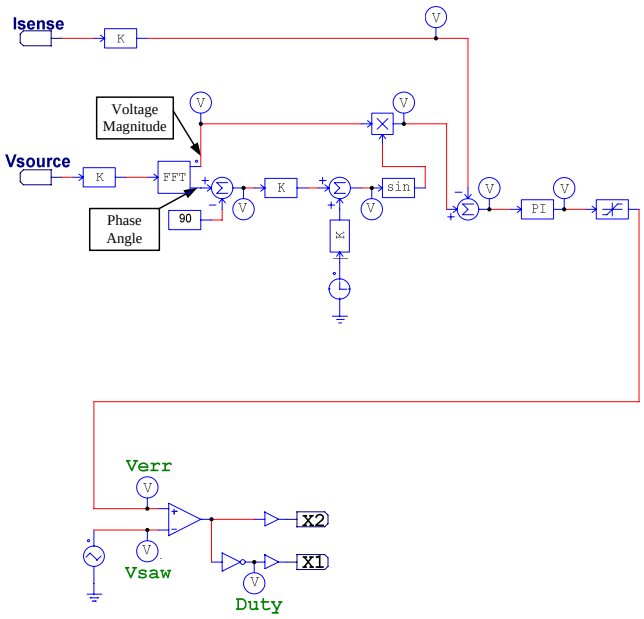

Figure 2.27: Control Loop for Inductance Loads Simulations

For the inductance load simulations, no changes have to be done in the circuit but the control algorithm which is shown in Figure 2.27. The control program senses the inductor current i_L and input voltage V_g at first. Then, the magnitude and phase angle of V_g are detected and with 90 degrees phase delay, a new voltage magnitude is calculated which can be compared with the inductor current i_L directly.

Waveforms for Different Ranges of the Inductive Loads

With the control program mentioned above, the inductive loads simulations can be achieved using the parameters given previously. The parameters used in the simulations are: $V_g = 10V$, $f_{pwm} = 20kHz$, $\|L_{sim}\| = 0.5p.u.$ and $1p.u.$, $R_1 = 17\Omega$ and $L = 2.6mH$. The waveforms of simulated inductor voltages are depicted in Figure 2.28.

It can be found in Figure 2.28 that the AC input voltage V_g is leading the current flowing through the series inductor and resistor by 90 degrees which

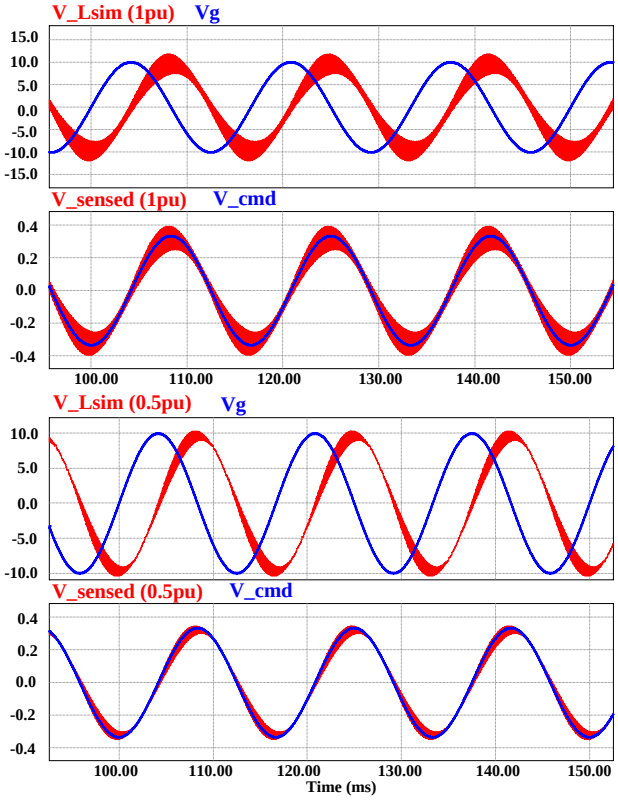

Figure 2.28: Simulated Inductor Voltages: V_{sensed} is the simulated inductor voltages in per-unit system and V_{cmd} is the AC input voltage source in per-unit system with 90 degrees phase delay

represents the inductive load characteristics. The waveforms for other ranges of the inductive simulated loads are illustrated in Figure 2.29 and 2.30.

Current Ripple Waveforms

From the previous discussion, when $\|Z_{sim}\| \geq R_1$, the current ripple can be calculated using Eq.(2.42); when $\|Z_{sim}\|$ is comparable with the series resistor R_1, the actual current ripple should be smaller than the calculated value. Figure 2.31 and 2.32 show the current ripples of the inductive simulated loads when $L = 26mH$ and $f_{pwm} = 20kHz$.

As shown in these figures, the current ripple at $L_{sim} = 10p.u.$ is 0.23

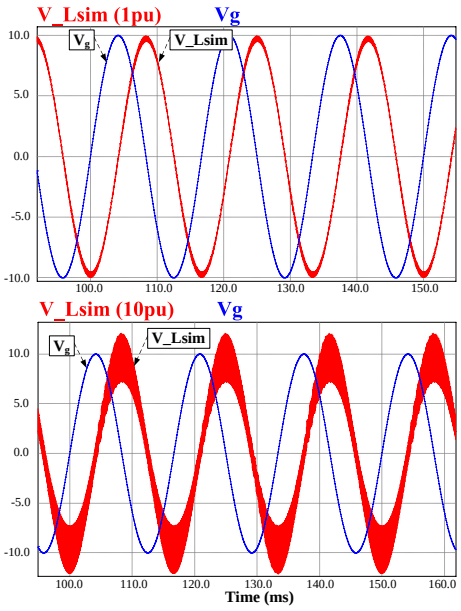

Figure 2.29: Simulated Inductor Voltages at $\|L_{sim}\| = 1p.u.$ and $10p.u.$

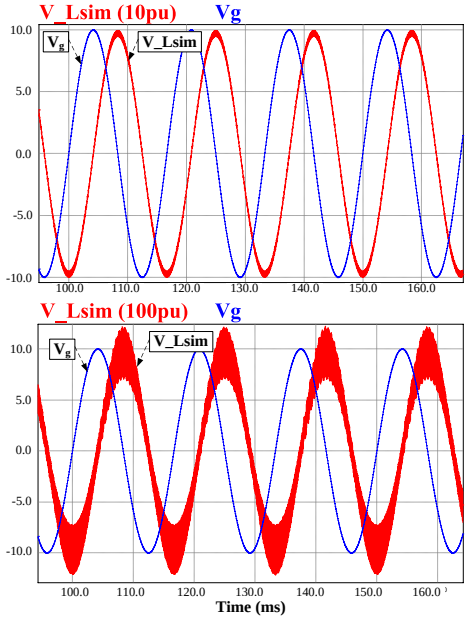

Figure 2.30: Simulated Inductor Voltages at $\|L_{sim}\| = 10p.u.$ and $100p.u.$

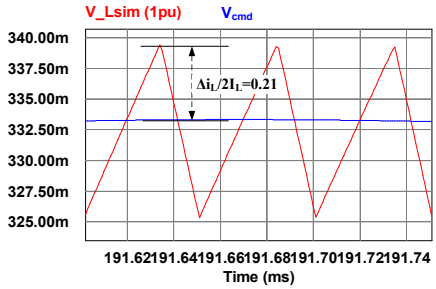

Figure 2.31: Current Ripple at $L_{sim} = 1p.u.$

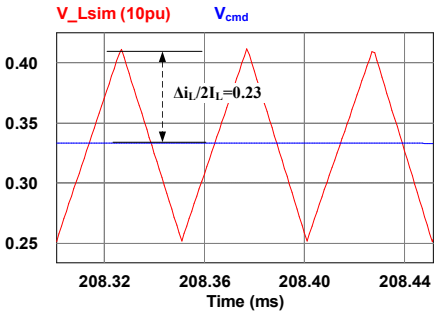

Figure 2.32: Current Ripple at $L_{sim} = 10p.u.$

which is very close to the calculated value 0.24; the current ripple at $L_{sim} = 1p.u.$ is 0.21 which is smaller than the calculated value 0.24 because $1p.u.$ is comparable with the series resistor R_1.

2.5.3 Capacitive Load Simulation

The control program of capacitance loads simulations is almost the same as the program used in the inductance loads simulation except that the phase angle of series inductor current i_L leads that of input voltage V_g by 90 degrees instead of 90 degrees delay.

Using the parameters given previously, Figures 2.33 and 2.34 show the waveforms of the different ranges of capacitive loads.

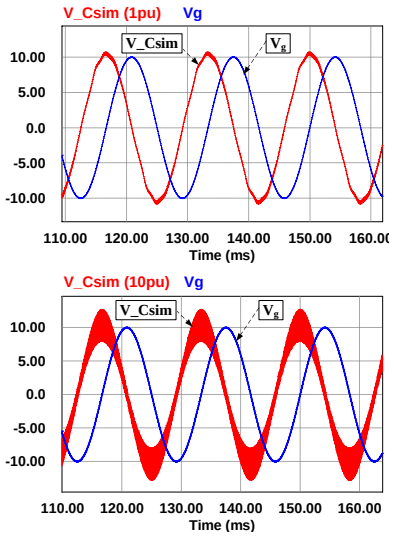

Figure 2.33: Simulated Capacitor Voltages at $\|C_{sim}\| = 1p.u.$ and $10p.u.$

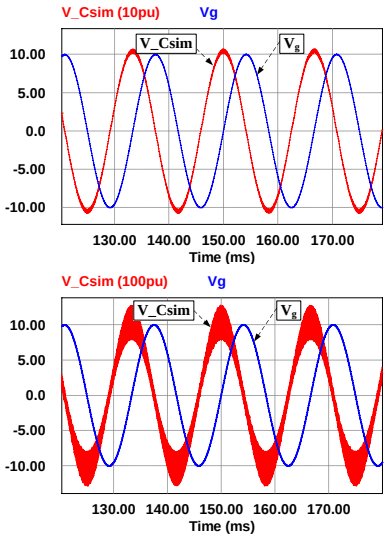

Figure 2.34: Simulated Capacitor Voltages at $\|C_{sim}\| = 10p.u.$ and $100p.u.$

Chapter 3

Hardware Implementation

Based on the theory discussed in chapter 2, a practical AC electronic load system will be built for experimental results. In this chapter, emphasis will be given on how to choose suitable components and integrate them to form a prototype of AC electronic load.

3.1 Introduction of System

The whole system is depicted in Figure 3.1. It consists of a regulated DC bus, an H-bridge inverter, a current filter, an IGBT driver module, sensor circuits, a DSP control board and a power supply circuit.

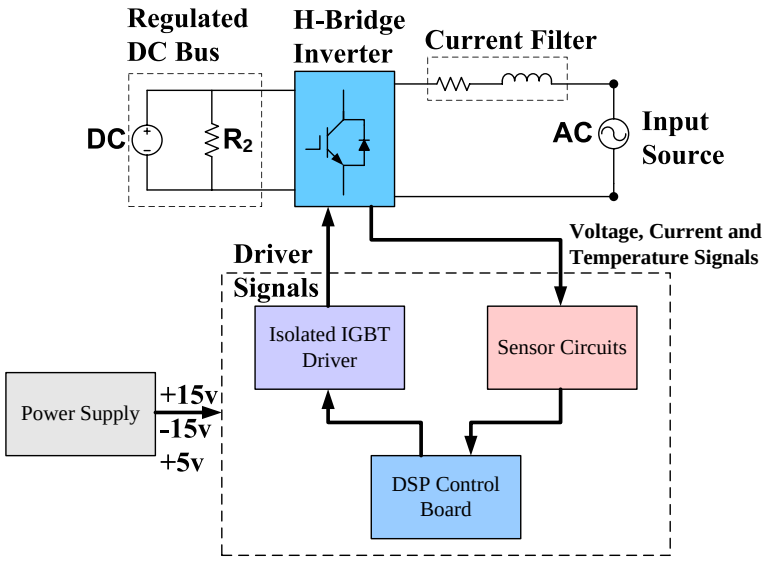

Figure 3.1: Hardware System of Electronic Loads

The sensor circuits sense voltage, current and temperature signals. Voltage and current signals will be used to calculate current reference in the DSP

software, and temperature signal will be used for overheat protection. An on-board power supply with some accessorial components provides $\pm 15V$, $+15V$ and $+5V$ for the whole hardware system. In the following parts, each subsystem will be introduced in detail.

3.2 IGBT Inverter Module

In this design, an IGBT module, MUBW 20-06 A7[4], produced by IXYS Corporation is employed to set up the H-bridge inverter. As depicted in Figure 3.2[4], the IGBT module includes a three phase full-bridge rectifier, a three phase DC-AC inverter and a NTC temperature sensor. For the application of single phase AC electronic loads, only the 3-phase inverter and NTC temperature sensor will be used.

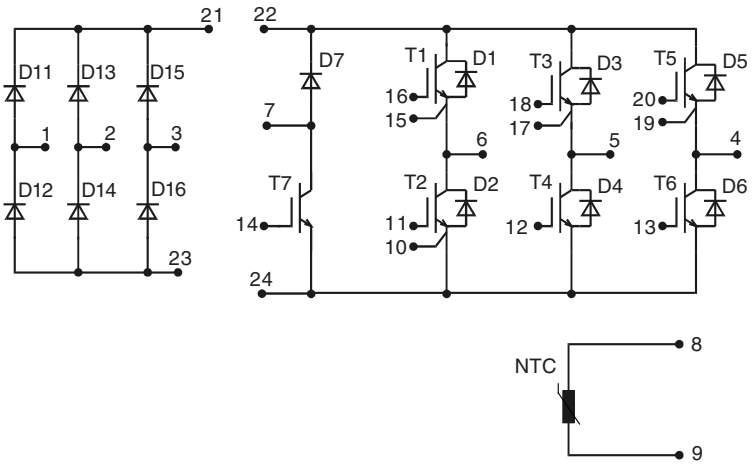

Figure 3.2: Structure of IGBT Module

According to the supposed conditions of unintentional islanding test (Appendix C), a voltage rating above $120V_{RMS}$ and a current rating above $8.33A_{RMS}$ are required. The chosen IGBT module, MUBW 20-06 A7, which can stand up to $600V$ and $35A$, meets these requirements.

The integrated temperature sensor consists of an NTC thermistor whose resistance gets smaller with the increasing of temperature. This sensor will be used in the design to prevent IGBTs damage from overheating.

3.3 IGBT Driver Circuit

Main purpose of the IGBT Driver is to provide enough power to the gate to make the IGBT switch properly. In this system, a compact IGBT driver module (6SD106EI) by Concept Technologie[5] was used at hand which is able to output high gate current of $\pm 6A$. This driver module can operate in two different modes: direct mode and half-bridge mode and is capable of outputting either six independent driver signals or three pairs of driver signals with dead time. Safety is another important issue in IGBT driver selection and the driver 6SD106EI integrate a short circuit and over-current protection circuit inside.

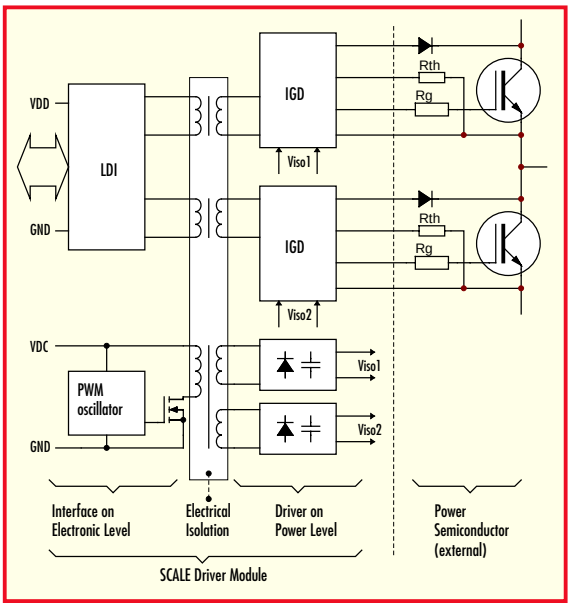

Figure 3.3: Structure of IGBT Driver Module: 6SD106EI

Figure3.3[5] shows the structure of a two-channel driver on the chip set. For a three-phase version, there is only one PWM oscillator, all other components are present in triplicate.

For each channel, the driver module contains the electrical isolation between the control and power sides which prevents damage of control sides from high voltage and current of power sides. The internal block IGD contains an over-current and short-circuit protection circuit for the power transistors, a feed monitoring circuit as well as a status acknowledgement circuit.

An electrically separated power supply can provide $\pm 15V$ for the drive electronics via an integrated DC/DC converter.

Mode Selection

As mentioned above, the driver module 6SD106EI can operate in two different modes. Two sets of complementary drive signals are needed for the H-Bridge inverter. Hence, in this specific system, the driver module will work in the half-bridge mode[5] which is able to output three pairs of complementary IGBT drive signals.

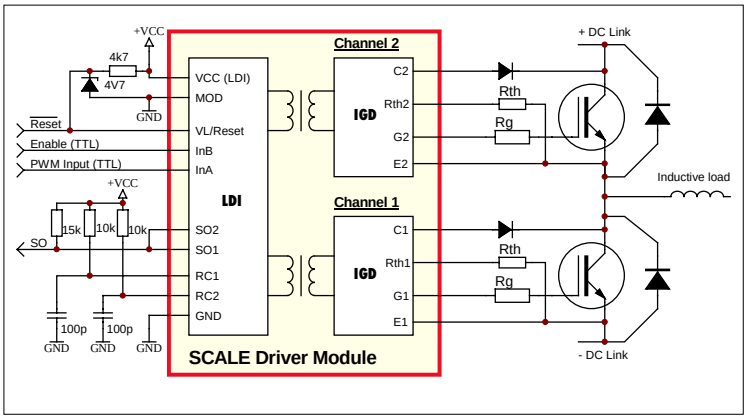

Figure 3.4: HalfBridge Mode Selection

In order to select the half-bridge mode, the pin MOD should be connected to GND and inputs pins of RC1 and RC2 must be connected to RC networks. The dimensioning will be discussed further in the next section.

Dead Time

Because any real power electronic devices do not turn on or off instantaneously, it is necessary to include a protection time, called the dead time, to avoid cross conduction of two switching devices in the same leg of the H-bridge inverter. The dead time can be set either in DSP software or in the driver module 6SD106EI by selecting the half-bridge operation mode. In this design, the dead time is set in the driver module.

In the half-bridge mode, RC networks must be connected to the pins RC1 and RC2. According to Table.3.1, $22k\Omega$ and $150pF$ are selected and the dead time is set to $2.1\mu s$.

R	C	typ. dead time
$10k$	$47pF$	$\approx 200ns$
$10k$	$100pF$	$\approx 500ns$
$15k$	$120pF$	$\approx 1.1\mu s$
$22k$	$150pF$	$\approx 2.1\mu s$
$33k$	$220pF$	$\approx 4.6\mu s$

Table 3.1: Values of the dead times of RC networks

Short-Circuit and Over-Current Protection

Every channel of the driver module is equipped with a Vce monitoring circuit as illustrated in Figure 3.5[5]. A resistor (Rthx) is connected to the pin Rthx as a reference. It defines the maximum voltage drop across the turned-on power transistor at which the protection function of the drive circuit is activated and thus the power transistor is turned off.

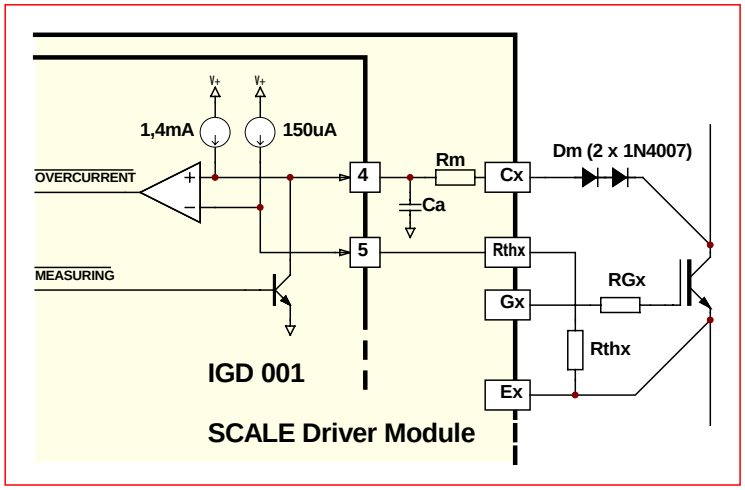

Figure 3.5: Protection Circuit of Driver Module 6SD106EI

If the voltage at Cx exceeds the voltage at Rthx, a Vce or under-voltage error occurs and the protection function is activated. The driver blocks the power semiconductor and accepts no drive signals. Meanwhile, the status outputs SOx (See Figure3.4, The "x" in "SOx" stands for the number of the drive channel in the driver module.) for the corresponding channels

are pulled to the logic low level which will be used in the DSP protection routine.

The pin Cx must be never connected directly to the collector of the power transistor and a high-blocking diode is needed to protect the measuring terminal Cx. For $600V$ IGBT modules, one diode of type $1N4007$ is connected to pin Cx. It is recommended that the peak repetitive reverse voltage of these diodes be over-dimensioned by at least 40%.

According to the application manual of 6SD106EI, a threshold voltage $V_{th} = 5.85V$ is recommended to use in IGBT drives. The reference resistor R_{th} can be calculated as follows:

$$R_{th} = \frac{V_{th}}{150\mu A} = \frac{5.85V}{150\mu A} = 39k\Omega \tag{3.1}$$

3.4 Voltage Measuring Circuit

Voltage measuring circuit consists of a voltage sensor, voltage level shifter circuits and a voltage buffer. In the following section, these blocks will be introduced one by one in detail.

Voltage Sensor

Voltage is measured with a voltage transducer LV 25-P (LEM Inc.). Its range goes up to $500V$ which is suited for $120V_{RMS}$ and the output of this sensor is a current with the ratio of 2.5 : 1 of the primary current. This module is supplied by $\pm 15V$ power and the connection is depicted in Figure 3.6.

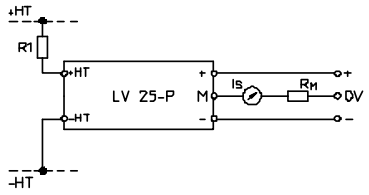

Figure 3.6: Voltage Sensor Connection

For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor R1 which is selected by the user and installed in series with the primary circuit of the transducer. In our case, $R1 = 6k\Omega$ was selected to measure $60V$ voltage which corresponds

to $10mA$ primary current in the testing experiments. For the real islanding test,a $17k\Omega$ resistor will be used to measure $120V_{RMS}$ voltage.

Voltage Level Shifter

A voltage level shifting circuit is required because the input voltage range of ADC module on the ezDSPlf2407A board used in this case is $0V - 3.3V$ which is different from that of the voltage sensor output. This function can be implemented with a two-level operational amplifier (OPA) circuit as shown in Figure 3.7.

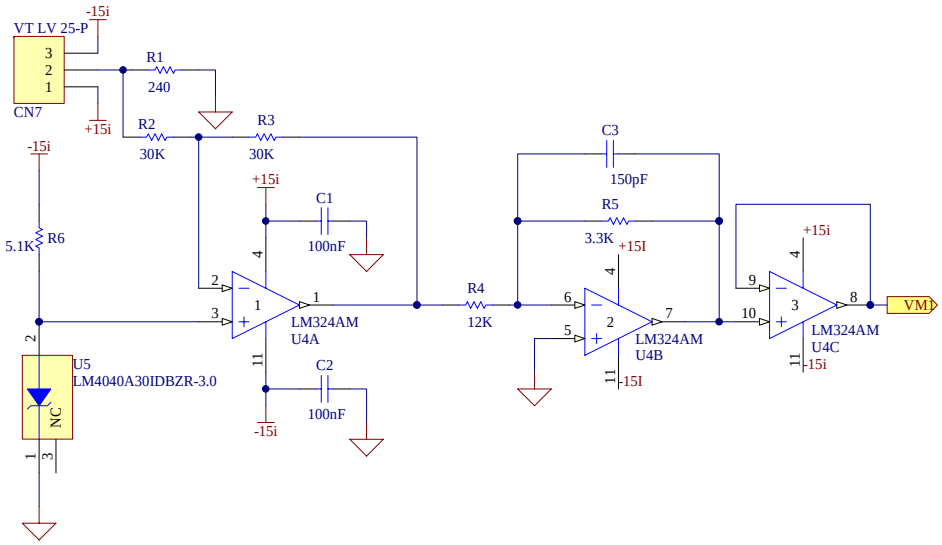

Figure 3.7: Voltage Measuring Circuit

The current signal from LV 25-P is transformed into a voltage signal with $R1$, the range of which is $-6V$ to $6V$. The voltage across $R1$ is then offset with the first level OPA circuit and the output voltage of U4A is given by:

$$V_{out1} = V_{REF}\left(1 + \frac{R_3}{R_2}\right) - V_{IN} \times \frac{R_3}{R_2} \tag{3.2}$$

The voltage V_{REF} is voltage across the precision voltage reference LM4040A and equals to $3V$. Through the second level OPA circuit, the output voltage of U4B is scaled by:

$$V_{out} = -\frac{R_5}{R_4} \times V_{out1} \tag{3.3}$$

Plugging in values for the components in Figure 3.7, the scaling of signals from the primary current to DSP analog voltage is illustrated in Figure 3.8.

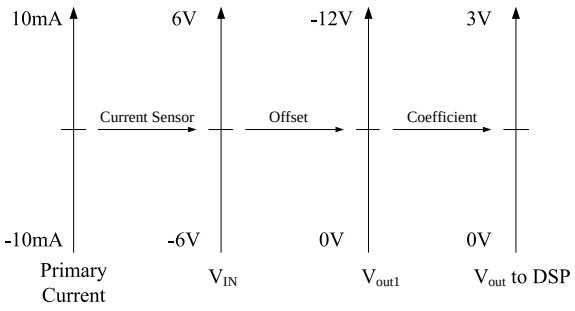

Figure 3.8: Voltage Scaling from Primary current to DSP Analog Voltage

Voltage Buffer

The ADC module in DSP is an unbuffered multiplexed ratiometric ADC which contains a multiplexer, a sample/hold circuit and an ADC comparator. This type of ADC has no internal buffer amplifiers to introduece input offset and gain errors.

The structure of ADC is shown in Figure 3.9. A disadvantage of this kind of on-chip ADC is that the sample capacitor within the ADC is directly charged by the external signal, and the charge left on the sample capacitor by the previous conversion of a channel can affect the accuracy of the channel currently being converted if inadequate settling time is allowed for a given source impedance. This phenomenon is referred to as channel-to-channel crosstalk[6].

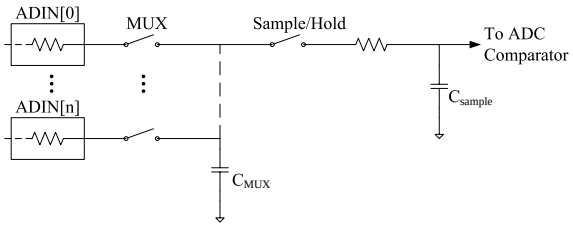

Figure 3.9: Structure of DSP On-chip ADC

In order to avoid the crosstalk, the source impedance of input signals should be much less than the input impedance of ADC. Therefore, a voltage buffer U4C in Figure 3.7 is added to decrease the output impedance of the scaling circuit so that ADC module can work properly.

3.5 Current Measuring Circuit

The current measuring circuit is mostly the same as the voltage measuring circuit except a few changes of parameters. In this case, the current is measured with a LEM current transducer LT 100-S, the range of which goes up to $\pm 100A$. The output of this module is a current with a ratio of $1 : 1000$ of the primary current. With the consideration of accuracy, the current should be close to $100A$. The current measuring circuit is illustrated in Figure 3.10.

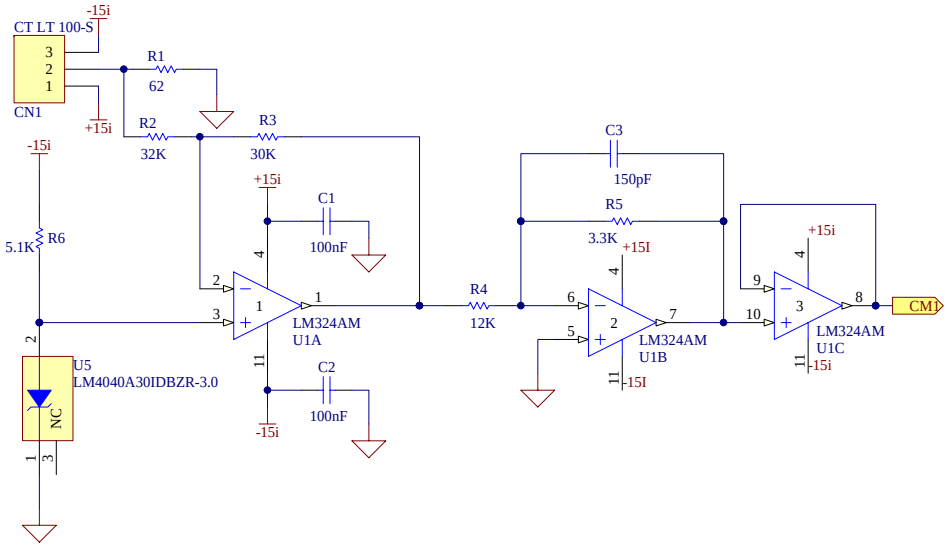

Figure 3.10: Current Measuring Circuit

Substitution of parameters shown in the figure above into Eq.(3.2) and (3.3), a solution for scaling of current signals is depicted in Figure 3.11.

In the testing experiments, the maximum current is below $3A$ and 32 turns of coil is used so that the range of measured current is close to $100A$, the primary nominal current of the current sensor.

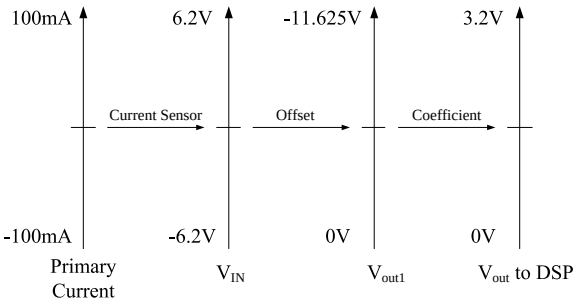

Figure 3.11: Current Scaling from Primary Current to DSP Analog Voltage

3.6 Temperature Sensor

A temperature sensor circuit is provided on the PCB to achieve IGBT over-heat protection. The temperature sensor used in this project is an NTC thermistor integrated in the IGBT module. According to the datasheet of this module, the IGBT operating temperature has a range from $-40\,°C$ to $125\,°C$ and the NTC thermistor resistance equals to 300Ω at $125\,°C$.

Because the NTC thermistor resistance varies with temperature significantly, a circuit detecting the variation of thermistor resistance can be applied for temperature sensing. In the practical application, a failure recovery from an over-heat fault will take a period of time. Therefore, a hysteresis comparator circuit shown in Figure 3.12 is used as temperature sensor circuit to aviod frequent alarms.

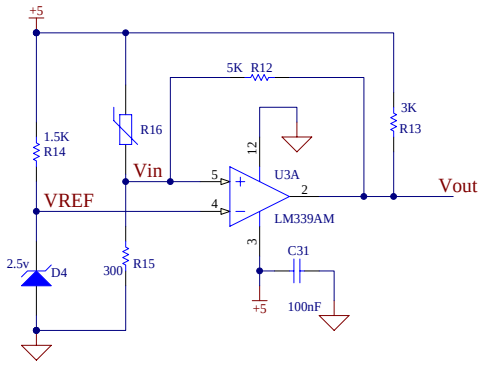

Figure 3.12: Temperature Sensor Circuit

As depicted in Figure 3.12, in normal conditions, the temperature keeps below 125 °C and the thermistor resistance $R_{16} > 300\Omega$. The output of comparator U3A is zero. When the temperature rises above the maximum value, R_{16} is less than 300Ω and the output of U3A jumps up to high voltage level ($V_H = 5V$). Due to the hysteresis loop R_{12}, the lower limit of V_{in} is solved by:

$$V_{in\_\min} = V_{REF} - \frac{R_{16} \parallel R_{15}}{R_{16} \parallel R_{15} + R_{12}} \times V_H \tag{3.4}$$

Substitution of parameters shown in Figure 3.4 into Eq.(3.4) yields $V_{in\_\min} = 2.35V$, which means V_{out} will not drop to zero unless V_{in} is less than $2.35V$ instead of $2.5V$. Convert voltage to resistance and a range of resistance from 300Ω to 338Ω can be obtained. Looking up the characteristic of thermistor resistance versus temperature leads to a temperature hysteresis loop in Figure 3.13.

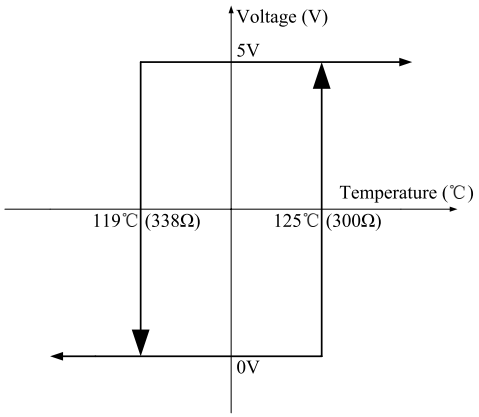

Figure 3.13: Temperature Hysteresis Loop

3.7 Protection Circuits

The pin $\overline{PDPINTA}$ of ezDSPlf2407A[7] is used to prevent the system from overheat and over-current faults. If this pin is driven low, a fault occurs in DSP program and all PWM output pins will be put in the high-impedance state immediately. A logic circuit collecting all fault signals of the system is applied as an interface shown in Figure 3.14.

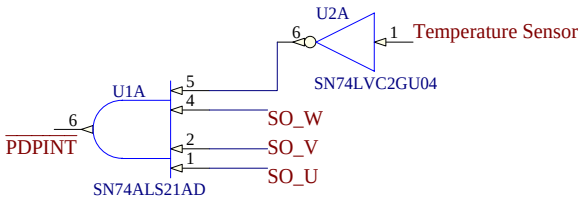

Figure 3.14: System Protection Circuit

The pin "Temperature Sensor" is the output of temperature sensor circuit which is in high voltage level when an overheat fault occurs. In order to fit the logic level of $\overline{PDPINTA}$, an inverter SN74LVC2GU04 is used to invert the logic level.

Pins of "SO_x" ($x = U, V or W$) are the status pins of driver module. When an over-current fault occurs, the logic levels of "SO_x" are pulled down to zero and a $\overline{PDPINTA}$ interrupt is activated in DSP program.

3.8 DSP Control Board

An ezDSPlf2407A board manufactured by TI company is employed in this case as a control unit. It contains a TMS320LF2407A digital signal processor, an on-board JTAG connector which provides interface to emulators for program debugging, and other peripherals. The major features of the TMS320F2407A include:

- A high-speed CPU with 40MHz clock rate and capable of processing 40 million instructions per second (MIPS).
- 64K words of on-chip data/program RAM, 32K words of on-chip program ROM or Flash EEPROM, 64K words of program, 64Kwords of data and 64K words of I/O space of addressing space.
- Sixteen multiplexed analog inputs 10-bit ADC core with built-in Sample and Hold (S/H) circuit and fast conversion time (S/H + Conversion): $375ns$. It supports up to four trigger sources for start-of-conversion (SOC) sequence and autosequencing function.
- Two Event Manager (EV) modules provide a broad range of functions and features that are particularly useful in motion control and motor control applications.

- 40 multiplexed general-purpose I/O pins.
- Watchdog Timer which monitors software and hardware operations, and implements system reset functions upon CPU disruption.
- Controller Area Network (CAN).
- Serial communications interface (SCI).

The EV modules in this DSP are very versatile and the major features are:

- Two general-purpose (GP) timers.
- Three general-purpose up and up/down timers, each with a 16-bit compare unit capable of generating one independent PWM output.
- Pulse-width modulation (PWM) circuits that include space vector PWM circuits, dead-band generation units, and output logic.
- Three 16-bit simple compare units capable of generating 4 independent PWM outputs.
- Three capture units.
- Quadrature encoder pulse (QEP) circuit.

3.9 Power Supply

The printed circuit boards are supplied by a commercial switching power supply VOF-65-15. Two other commercial dc dc converters were used to provide proper supply voltage for the circuits. A $5V$ dc dc converter (CC10-1205SF-E) supplies the ezDSP board, the temperature sensor circuit and the protection circuit; a $\pm 15V$ supply (CC10-1212DF-E) provides power for the op amp circuits; the switching power supply (VOF-65-15) feeds the driver circuits.

All these converters were equipped with the suggested input and output filters as stated in the corresponding data sheets and application notes. The input filter consists in all three cases of a Π-type filter, consisting of two capacitors and one inductor. On the output side, there are only smoothing capacitors and a zener diode, to protect devices from an unexpected over-voltage. The complete power supply circuit is shown in the Figure A.1 in the Appendix A.1.

Chapter 4

Software Implementation

The hardware system of AC electronic loads has been described in the previous chapter. In this chapter, a software applied to implement the control algorithm will be introduced in detail. All implementations of software are based on TI's (Texas Instruments) DSP TMS320LF2407A and the associated assembly language.

4.1 Program Overview

As the previous introduction, the DSP TMS320LF2407A has many peripherals and is enough for this application. The peripherals used in the control program contains: event managers (EV), general purpose timers 1 and 2, the PWM generation unit, the 16-channel ADC unit and the digital I/O ports module[8],[9],[10].

The AC electronic loads control program has several major functions: accurate voltage and current acquisition, current command calculation and PWM duty cycle update. With the consideration of software portability, the program was divided into several sub-function blocks. The flowchart of the control program is shown in Figure 4.1.

The control program consists of four routines:

- System initialization and Main Loop.

  All initializations are finished in this routine and an endless loop is waiting for different ISRs to achieve all major features of AC electronic loads.

- Timer1 Interrupt service routine (ISR).

  This routine calculates the required current command and update PWM duty ratios.

- Timer2 Interrupt service routine (ISR).

  Average voltage and current sampling are implemented in this routine.

- $\overline{PDPINTA}$ Interrupt service routine (ISR).

  Over-heat and over-current protection is achieved here and makes the whole system safer and more reliable.

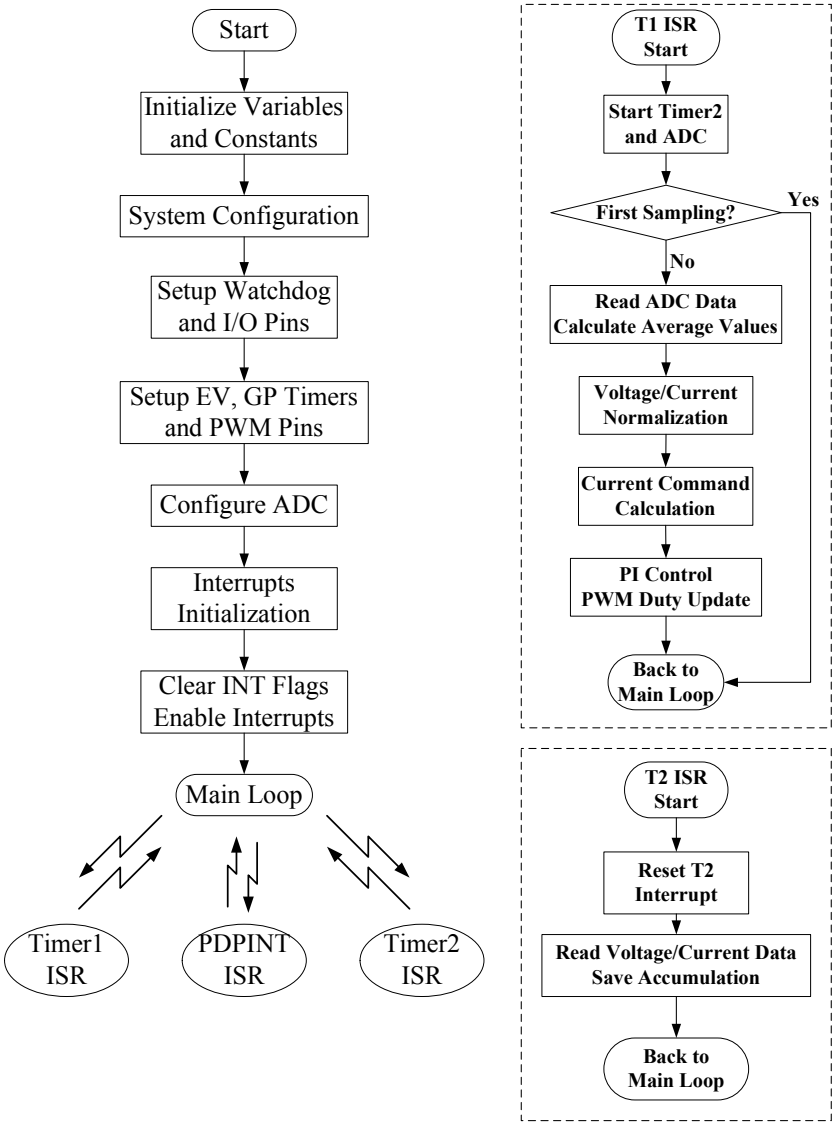

Figure 4.1: Program Flow Chart

The following sections will explain the details of these routines.

4.2 Variables Normalization

TMS320LF2407A is a 16-bit fixed-point DSP and unable to represent floating-point numbers directly. Therefore, the normalization of variables is required in the program so that the real values of voltage and current signals can be represented correctly.

4.2.1 Q Format

In fixed-point DSPs, all the numbers must be represented as a collection of bits. Each bit represents either "0" or "1", hence the number system naturally used in microprocessors is the binary system. In order to represent fractional numbers, fixed-point system requires the programmer to create a virtual decimal place in between two bit locations for a given number. Q-format is such kind of fractional fixed-point representation suitable for DSPs algorithms[11]. The labeling convention of Q-format is as follows:

$$Q\,[QI]\,.\,[QF] \tag{4.1}$$

Where QI is the number of integer bits and QF is the number of fractional bits. In a 16-bit DSP used in our system, the sum of QI and QF equals to 15 and the MSB is the sign bit.

In addition and subtraction of two Q-format numbers, the fixed-point decimal places must be aligned and an appropriate dynamic range has to be chosen to handle the overflow of the addition. In multiplication, the number of integer and fractional bits in the product is the sum of the corresponding multiplier and multiplicand Q-format numbers as described the following equations:

$$\begin{aligned} QI_{product} &= QI_{multiplicand} + QI_{multiplier} \\ QF_{product} &= QF_{multiplicand} + QF_{multiplier} \end{aligned} \tag{4.2}$$

4.2.2 Normalization of Voltage and Current

As mentioned above, there is a trade-off between dynamic range and precision for Q-format numbers. Higher precision leads to a narrower dynamic range, hence the real voltage and current values need to be normalized and thus the Per Unit (PU) system will be applied to achieve the high precision as well as the wide dynamic range. Because the measured current in the experiments is less than $3A$, 32 turns of the current will be measured to achieve higher accuracy.

In this system, the base values of variables are as follows:

$$\begin{aligned} V_{base} &= 30V \\ I_{base} &= 100A/(4 \cdot 32turns) = 0.78125A \\ |Z|_{base} &= V_{base}/I_{base} = 38.4\Omega \end{aligned}$$

With the consideration of both precision and dynamic range, the PU values will be represented in Q[3].[12] format (or $Q12$). The maximum values of current and voltage in the experiments are $i_{max} = 3.125A$ and $V_{max} = 60V$. When the current reaches the maximum value, the ADC result i_{binary} is 512. The corresponding per-unit value of the Q-format number is given by $i_{PUQ12} = (i_{\max}/i_{base}) \times 2^{12} = 2^{14}$, and a conversion ratio $K_{current} = i_{PUQ12}/i_{binary} = 2^{14}/512 = 32$. All measured values of current can be converted into the PU values in $Q12$ format:

$$i_{PUQ12} = K_{current} \times i_{binary} \tag{4.3}$$

Following the same steps, the voltage conversion ratio $K_{voltage}$ equals to 16 and the conversion formulas is

$$v_{PUQ12} = K_{voltage} \times v_{binary} \tag{4.4}$$

4.3 System Initialization

To implement the specific functions, the initialization module performs the following tasks.

4.3.1 Event Manager Modules Initialization

As mentioned above, event manager modules are the most significant function blocks which provide a flexible method for controlling both dedicated I/O and shared pin functions. The following blocks are initialized in this module:

PWM generation block

To drive the H-bridge inverter, four PWM pins 1-4 are employed and the polarity of PWM pins are set in Compare Action Control Register A (ACTRA) as follows:

- PWM 1 and 4 are active high.

- PWM 2 and 3 are active low.

PWM 1-4 corresponds to switches 1-4 and "active high" means the output of PWM pins are set to one when a compare match happens. Additionally, asymmetric PWM waveforms are used in this program and associated timers are set to continuous-up count mode.

General-Purpose (GP) Timers 1&2

GP timer 1 is employed in the software to control the switching frequency of PWM signals. Usually, PWM frequencies are in the range of $10kHz$. In this project, a PWM frequency of $20kHz$ has been chosen.

GP timer 2 is used to setup the voltage and current sampling frequency. In order to achieve higher precision, the sampling frequency is set to $160kHz$.

4.3.2 ADC Module Initialization

ADC Clock Prescaler

ADC conversion time consists of two time segments: Sample/Hold (S/H) window and conversion window, as shown in Figure 4.2. The S/H window can be tailored to accommodate the variation in source impedances by the ACQ PS3-ACQ PS0 bits and the CPS bit in the ADCTR1 register.

In this project, the ACQ PS3-ACQ PS0 bits are set to "0111b" and the CPS bit is set to "0b" to accommodate a 2290Ω source impedance.

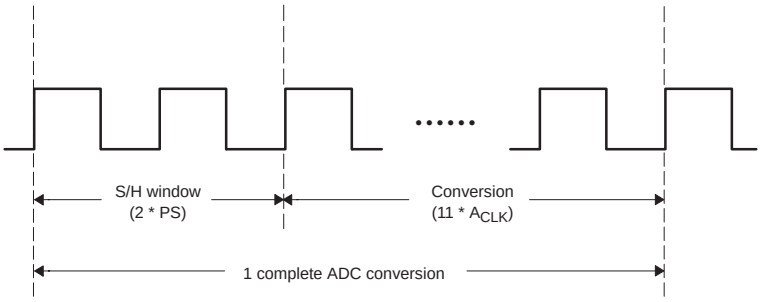

Figure 4.2: ADC Conversion Time

ADC Conversion Sequencer

The ADC module in TMS320LF2407A contains a 16-state sequencer which can perform a series of conversions without external intervention and the conversion sequence is stored in the ADC input channel select sequencing control registers (CHSELSEQn).

In this project, a timer2 underflow interrupt is used as a trigger to start an auto-conversion sequencer. The number of auto-conversions is two and a single sampling of voltage and current signals is performed for each trigger.

4.3.3 I/O Ports Module Initialization

The commercial driver module contains an enable pin InB (shown in Figure 3.4) which is able to block all PWM channels if pulled to zero. Therefore, the $\overline{PDPINTA}$ interrupt service routine employs the digital I/O port IOPB4 as an enable pin for the commercial driver module to achieve the protection function. The pin IOPB4 is configured as an output port with the I/O mux control register A (MCRA) and set to zero when a fault occurs.

4.4 Interrupt Service Routine (ISR)

As shown in Figure 4.1, three ISRs are applied to perform the current control and protection functions.

Timer 1&2 ISRs

The major features of Timer 1&2 ISRs have been described in Figure 4.1. Here the discussion will be focused on the time sequence between two ISRs. In these two routines, the timer underflow events are configured to generate interrupts which means an interrupt event will occur once the counter of timer 1 or 2 reaches “0000h”.

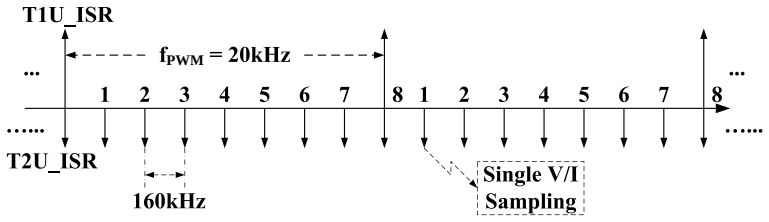

Figure 4.3: Timer 1 and 2 ISR Sequence

Figure 4.3 depicts the time sequence of two ISRs (TxU_ISR represents the associated interrupt routine, $x = 1 or 2$). It can be seen that each underflow interrupt event of timer2 will perform two conversions: one is voltage sampling and the other is current sampling. Due to the ADC auto-conversion sequencer, the pointer of the sequencer will move to the address of next two channels in the sequence. Because the frequency of timer2 is eight times of the timer1's, 16 conversions are implemented in one PWM period and the pointer of the ADC sequence is set to the original address automatically.

Additionally, timer 1 and 2 must be synchronized to keep the correct time sequence between two timers. Therefore, the timer2 is reset and started at the beginning of each T1U_ISR.

$\overline{PDPINTA}$ ISR

With the protection circuit shown in Figure 3.14, the system is capable of monitoring the overheat and overcurrent faults. Figure 4.4 shows that the pin IOPB4 is set to low level which will block all PWM outputs of the driver module so that the whole system is able to survive a severe accident.

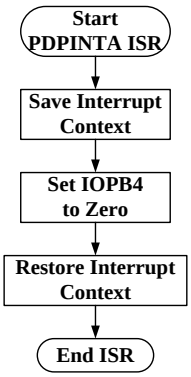

Figure 4.4: Flowchart of $\overline{PDPINTA}$ ISR

4.5 Generation of Sine Wave

To simulate an inductive or capacitive load with different input sources, a general approach based on $Ldi_L/dt = v_L$ or $Cdv_c/dt = i_c$ might be possible. In each PWM switching period, Δi_L or Δv_c can be calculated using these

two equations and after comparison with the actual Δi_L or Δv_c, a new duty cycle D can be calculated and used to control the current to track the required load characteristics.

However, this prototype only focuses on the $60Hz$ sinusoidal voltage source and thus a sine look-up table will be implemented to achieve the inductive or capacitive loads. Compared with the general approach, the sine look-up table needs less operation time.

The table contains 512 words to represent sine values of phase angles in the range of $[0°, 360°]$. As a result, the resolution on phase angle of electronic loads is limited to $360/512 = 0.703125°$.

In the binary system of DSP, the phase angle θ varies from 0 to 4095. As only 512 words are available to represent this range, θ is divided by 8 and stored into the variable index that will be used to address the lookup table.

The content of the table row pointed by the index is fetched in indirect addressing mode via AR5 auxiliary register (Figure 4.5). This content coded in $Q12$ format is stored in the variable *sincos* that will be used in the phase angle calculation of electronic loads.

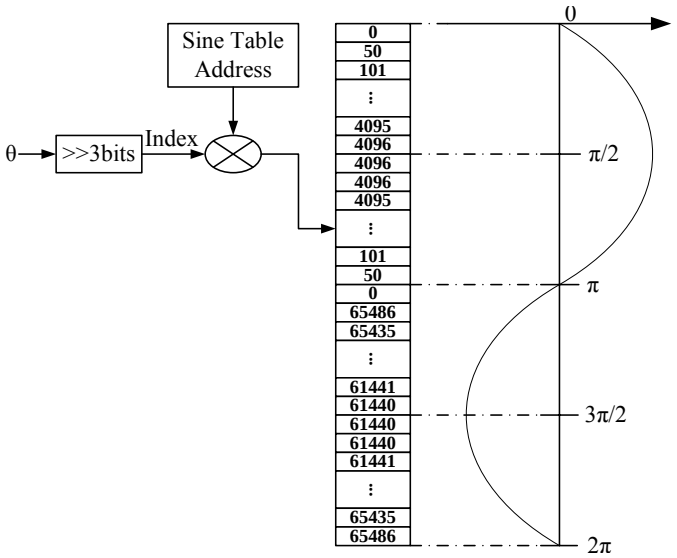

Figure 4.5: Sine Look-up Table

Note that 90° is added to θ to get the cosine value of the phase angle. This operation corresponds to addition of 128 (512/4) to the value of index.

4.6 Digital PI Control

The PI controller is a generic control loop feedback mechanism widely used in industrial control systems. It is an effective approach in nearly all types of the feedback system, especially for systems containing a single pole. In our control program, a digital PI control will be implemented.

An analog PI controller can be expressed by:

$$u(t) = K_P \left[e(t) + \frac{1}{T_I} \int_0^t e(t)\, dt \right] + u_0 \tag{4.5}$$

Where K_P is the proportional gain, T_I is the time constant of the controller and thus the integral gain $K_I = K_P/T_I$; $e(t)$ and $u(t)$ are the input and output of the controller respectively.

The proportional term means that the system responds in proportion to the deviation from the set point and determine the sensitivity of the controller to the error. A high proportional gain results in a large change in the output for a given change in the error. If the proportional gain is too high, the system can become unstable. In contrast, a small gain results in a small output response to a large input error, and a less sensitive controller.

The integral term means that the system will respond in proportion to the integral of the error over time. A small time constant accelerates the movement of the process towards setpoint and eliminates the residual steady-state error that occurs with a proportional only controller. However, since the integral term is responding to accumulated errors from the past, it can cause the present value to overshoot the setpoint value.

In order to implement the PI controller in a DSP, it has to be converted into digital form. A common way of doing this is to discretize the controller to approximate the continuous time derivatives as follows:

$$u_k = K_P \left[e_k + \frac{T_{pwm}}{T_I} \sum_{j=0}^{k} e_j \right] + u_0 \tag{4.6}$$

Where k represents the k_{th} sampling, T_{pwm} is the switching period and u_0 is the initial value of the output. Considering the k_{th} and $(k-1)_{th}$ samplings, the change of output at the k_{th} sampling can be derived:

$$\Delta u_k = u_k - u_{k-1} = K_P (e_k - e_{k-1}) + T_{pwm} K_I e_k \tag{4.7}$$

Upon collecting items, one obtains

$$u_k = u_{k-1} + (K_P + T_{pwm} K_I) e_k - K_P e_{k-1} \tag{4.8}$$

With Eq.(4.8), a digital PI controller can be implemented easily in the DSP program. Additionally, a saturation block is also implemented in the program to protect the control system from the integration saturation.

4.7 RLC Algorithm

The device we designed outputs different kinds of load characteristics by controlling the inductor current. Hence, a current command calculation block shown in Figure 4.1 is required for different electronic loads and the algorithms of different loads will be described here.

For the resistive loads, the current command calculation is quite straightforward and easy to implement in the DSP program. As a resistor, the current flowing through and the voltage across it are in phase, and thus the inductor current i_L is proportional to the source voltage V_g at each sampling point. Therefore, in the software, the current command can be obtained by simply dividing V_g by the simulated resistor R_{sim}.

When it comes to the inductive or capacitive loads, however, such a simple algorithm couldn't be used any more due to the phase difference between i_L and V_g. Because the inductive and the capacitive loads have similar $V - I$ characteristics, only the algorithm of the inductive loads will be discussed here in detail.

Phase Detection Block

In order to simulate the inductance $V - I$ characteristic with respect to the reference voltage V_g, it is necessary to detect the phase angle of V_g so that the control software can output the correct current with 90-degree phase delay (90-degree lead for the capacitance loads). In our program, the first cycle of V_g is used for phase detection without any other operations.

As shown in Figure 4.6, checking the zero points of V_g is an effective approach of the phase detection. In the program, two variables are defined to save the previous and current voltage values: V_1 is the old value and V_2 is the current value. When $V_1 > 0$ and $V_2 \leq 0$, Z_1 can be found and the phase angle is 90° ($v_g = V_g \times \cos(\omega t)$); when $V_1 < 0$ and $V_2 \geq 0$, Z_2 can be found and the phase angle is 270°. Once the zero-crossing and the phase angle are detected, the correct phase shift ϕ can be generated using $\omega t + \phi$ ($\phi = 90°$ for the inductive loads).

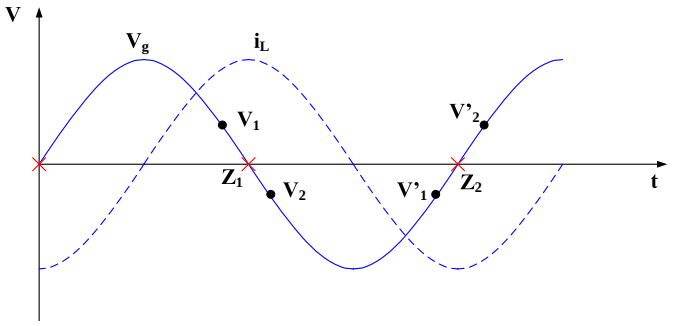

Figure 4.6: Phase Detection Diagram

Frequency Detection Block

In the first cycle of V_g, the frequency is also detected to calculate the phase angle using $\theta = \omega t$. Digitalizing this equation, one obtains

$$\theta = \omega \cdot \Delta t = 2\pi f \cdot N \cdot T_{pwm} \tag{4.9}$$

Where f is the frequency of V_g, T_{pwm} is the switching period and N represents the N_{th} switching cycle. The frequency f also equals

$$f = \frac{1}{N_{period} \times T_{pwm}} \tag{4.10}$$

Where N_{period} represents the period of V_g which can be got by $N_{period} \times T_{pwm}$. Insert Eq.(4.10) into Eq.(4.9) and θ can be derived

$$\theta = 2\pi \times \frac{N}{N_{period}} \tag{4.11}$$

In the program, once the first zero point of V_g is found, a counter FRQ_CNT will be started immediately until the second zero point occurs and the period N_{period} is equal to $2 \times FRQ\_CNT$. Then, the phase angle can be derived using Eq.(4.11) and the program will start to generate the correct current command from the second zero point.

Magnitude Detection Block

The current command i_{cmd} equals $I_{cmd} \cdot \cos(\omega t + \phi)$, where I_{cmd} is the magnitude of the current and can be obtained by

$$I_{cmd} = \frac{\|V_g\|}{\|Z\|} \tag{4.12}$$

Z represents the impedance of the inductive load (or the capacitive load) and the voltage magnitude can be detected in the first cycle of V_g by checking the maximum value of V_g. Figure 4.7 shows the flowchart of the current calculation block. The variable PhD_FLAG indicates whether the phase detection is finished or not and the program will jump over the current calculation block unless $PhD\_FLAG \neq 0$.

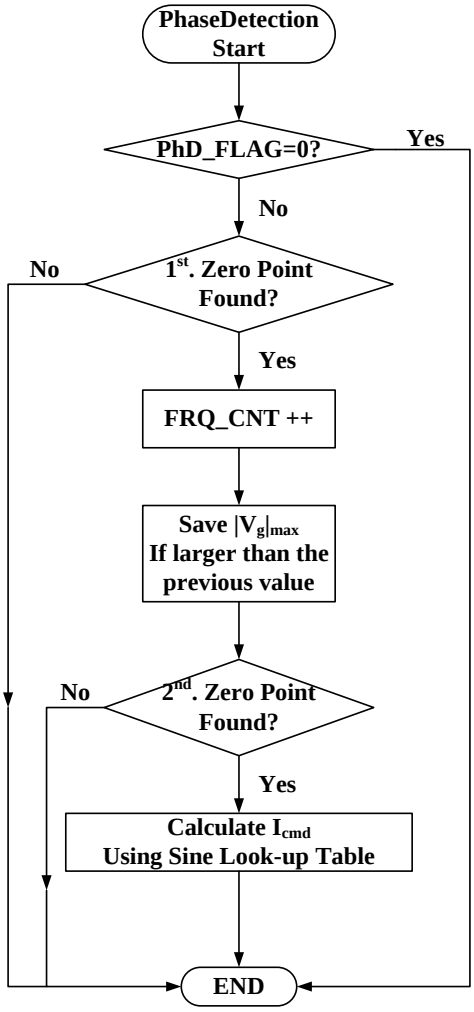

Figure 4.7: The Flow Chart of the Current Calculation Block

Chapter 5

Experimental Results

In the previous discussions, the principles, hardware and software implementations of this AC electronic load system have been introduced in detail. The following chapter will show a series of experimental results to prove the principles and real hardware system.

5.1 Experimental Conditions

On the basis of theory study and software simulation a prototype is researched and developed shown in Figure 5.4.

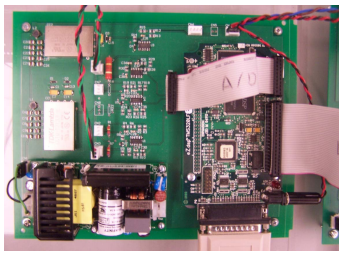

Figure 5.1: Control Circuit Board

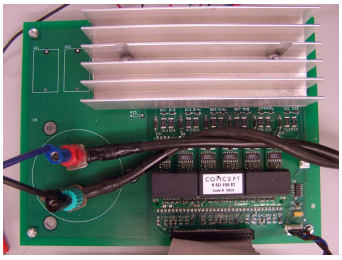

Figure 5.2: Power Circuit Board

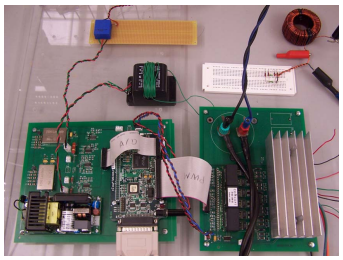

Figure 5.3: The Whole Circuits

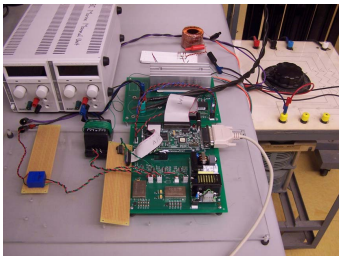

Figure 5.4: Experimental System

The experimental system consists of:

- A system control board including: voltage and current sensor circuits, protection circuits, an ezDSP board and power supply circuits.
- A IGBT-based power board containing: an IGBT driver circuit and an H-bridge IGBT inverter.
- A 3-phase AC source and a 3-phase transformer used to adjust the voltage level of AC source.
- A DC power supply HPD 30-10 by XANTREX which can provide $60V$ and $3A$ DC source
- Two series inductors, $2.6mH$ and $26mH$, are used for ripple studies.
- A 315Ω power resistor is used as the parallel resistor.

In the experiments, a 4-channel 500MHz Oscilloscope (Lecroy 6050A) is used to measure and save the results.

5.2 Resistive Load Results

With the consideration of simplicity and typicality, the electronic load experiments will start with resistance loads. The peak voltage of AC source $V_{gpeak} = 10V$, the voltage ratio $k = 1.3$ and thus DC bus voltage $V_{dc} = 13V$.

5.2.1 The Range of Resistance Loads at $L = 2.6mH$

In the PSIM simulations, it is found that the value of the series inductor L has to be changed with the variation of electronic load impedances. According to Table 2.8, an inductor of $2.6mH$ is selected to achieve resistance load experiments, the range of which is from $0.5p.u.$ to $2p.u.$. The experimental results are depicted in Figure 5.5 to 5.10.

The variable V_{Rsim} shown in following figures represents the voltage across R_{sim} which is calculated by $V_{Rsim} = i_L \times R_{sim}$ and supposed to equal to the AC source V_g. It can be seen that V_{Rsim} is mostly same as V_g, both in magnitude and in phase.

On the other hand, the current ripple increases with increasing of R_{sim} and introduces more high frequency interference. The current ripples for different R_{sim}s can be obtained in the following Figures 5.6, 5.8 and 5.10.

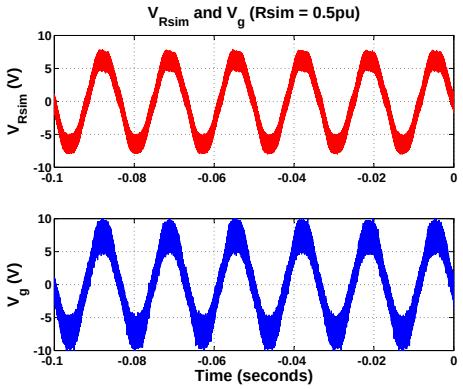

Figure 5.5: $R_{sim} = 0.5p.u.$ at $f_{pwm} = 20kHz$

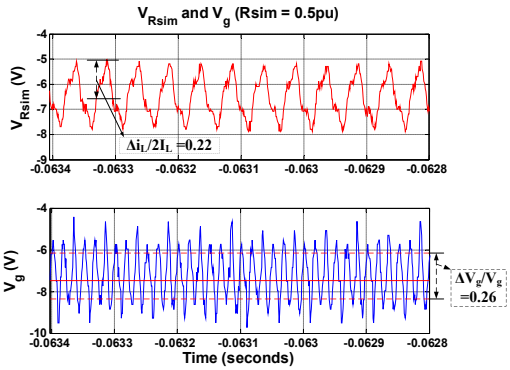

Figure 5.6: Current Ripple at $R_{sim} = 0.5p.u.$

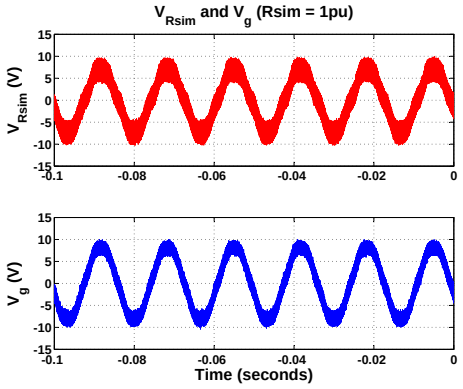

Figure 5.7: $R_{sim} = 1p.u.$ at $f_{pwm} = 20kHz$

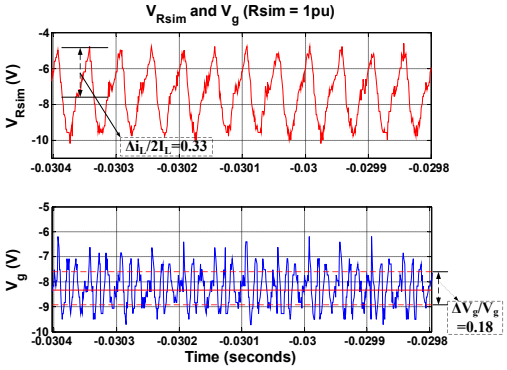

Figure 5.8: Current Ripple at $R_{sim} = 1p.u.$

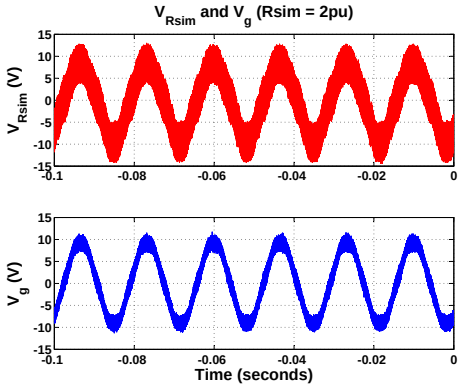

Figure 5.9: $R_{sim} = 2p.u.$ at $f_{pwm} = 20kHz$

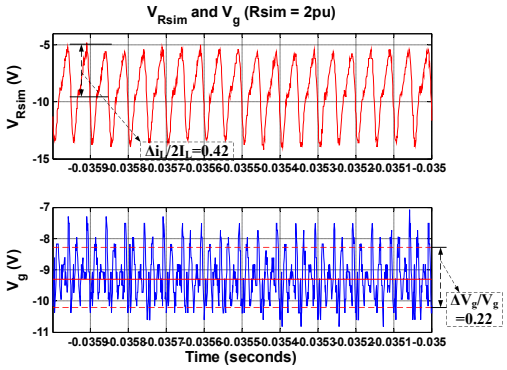

Figure 5.10: Current Ripple at $R_{sim} = 2p.u.$

Table 5.1 shows the comparisons of current ripple between the results of PSIM simulations and the experimental results. It can be seen that the experimental results have 30% to 40% error with respect to the simulation results. The main reason is because of the noise introduced by the AC source V_g and the noise $\Delta V_g/V_g$ shown in Figure 5.6, 5.8 and 5.10 is around 20%.

$R_{sim}(p.u.)$	Simulation Results	Experimental Results	Error(%)
0.5	0.13	0.22	40.9
1.0	0.19	0.33	42.4
2.0	0.30	0.42	28.6

Table 5.1: Comparisons of Current Ripple between Simulation Results and Experimental Results

5.2.2 Switching Frequency and Current Ripple

According to Eq.(2.33), the PWM switching frequency is inversely proportional to the current ripple. In this section, the effect of f_{pwm} will be studied at $10kHz$ and $20kHz$ separately and R_{sim} is set to $2p.u.$. Figures 5.11 to 5.14 show the current ripples at different frequencies.

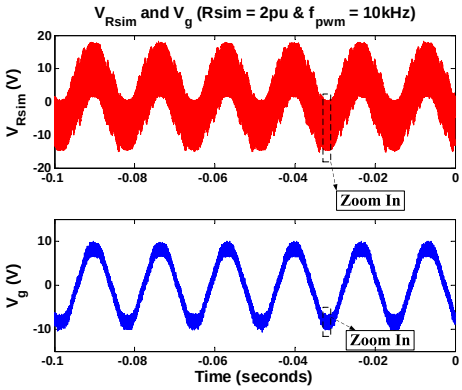

Figure 5.11: $R_{sim} = 2p.u.$ at $f_{pwm} = 10kHz$ and $L = 2.6mH$

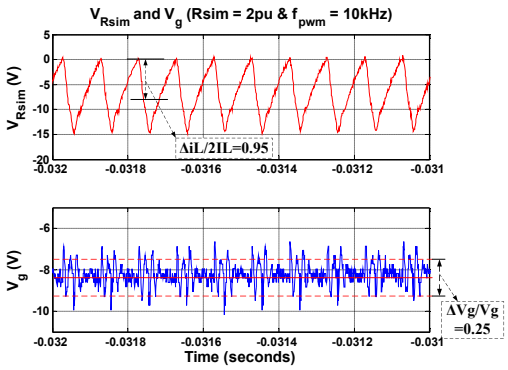

Figure 5.12: Current Ripple at $R_{sim} = 2p.u.$ and $f_{pwm} = 10kHz$

Table 5.2 shows the comparisons of experimental results at different switching frequencies. It can be derived that the current ripple at $10kHz$ is about 2.6 times of the ripple at $20kHz$.Considering the measurement errors

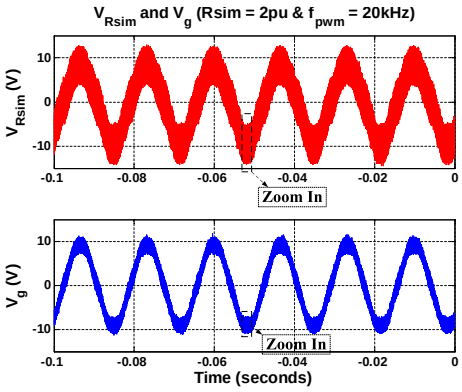

Figure 5.13: $R_{sim} = 2p.u.$ at $f_{pwm} = 20kHz$ and $L = 2.6mH$

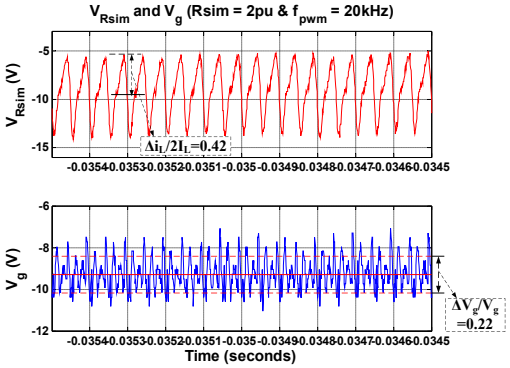

Figure 5.14: Current Ripple at $R_{sim} = 2p.u.$ and $f_{pwm} = 20kHz$

and the noise introduced by V_g, the experimental result agrees well to the theoretical value "2 times".

$f_{PWM}(kHz)$	Simulation Results	Experimental Results	Error(%)
10	0.6	0.95	36.8
20	0.3	0.42	28.6

Table 5.2: Comparisons of Current Ripple at $20kHz$

5.2.3 Series Inductor L and Current Ripple

The inductance of the series inductor L is also supposed to be inversely proportional to the current ripple and the associated experimental results are illustrated in Figure 5.15 to 5.18 to prove this relationship.

For the experiments, two inductors of $2.6mH$ and $26mH$ are selected and the switching frequency equals to $20kHz$ and R_{sim} is still set to $2p.u.$.

It can be seen that the current ripple with the $2.6mH$ inductor is 7.7 times of the current ripple with the $26mH$ inductor which has about 20% error compared with the theoretical value "10 times". With the consideration of measurement errors and the noise of the input source, the series inductance is inversely proportional to the current ripple(Table 5.3).

$L(mH)$	Simulation Results	Experimental Results	Error(%)
26	0.03	0.06	50.0
2.6	0.30	0.46	34.8

Table 5.3: Comparisons of Current Ripple at $20kHz$

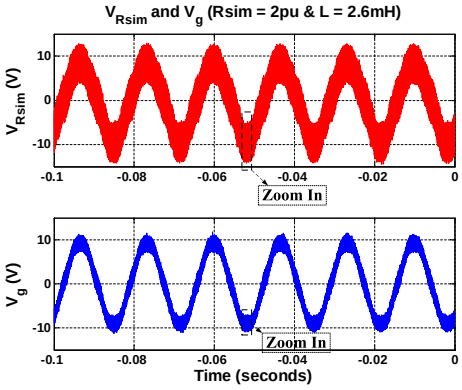

Figure 5.15: $L = 2.6mH$, $R_{sim} = 2p.u.$ and $f_{pwm} = 20kHz$

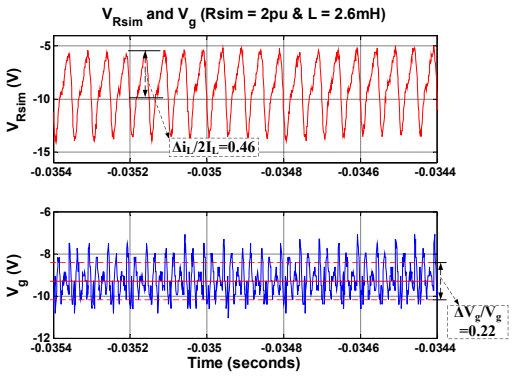

Figure 5.16: Current Ripple at $L = 2.6mH$

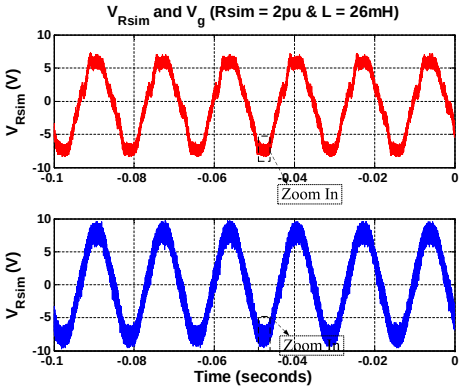

Figure 5.17: $L = 26mH$, $R_{sim} = 2p.u.$ and $f_{pwm} = 20kHz$

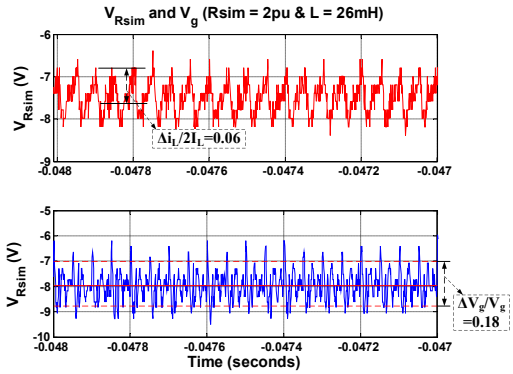

Figure 5.18: Current Ripple at $L = 26mH$

5.3 Inductive Load Results

The principles and PSIM simulations of inductance have been introduced previously and the experimental results will be shown in this section. From Table 2.9, the parameters for different inductance ranges can be found. Here, two inductors of $2.6mH$ and $26mH$ are selected, the switching frequency is $20kHz$ and the DC bus voltage $V_{dc} = 1.5 \times V_g$.

The range of Inductance loads at $L = 2.6mH$

First of all, the range of inductance loads at $L = 2.6mH$ will be depicted in Figures 5.19 and 5.20.

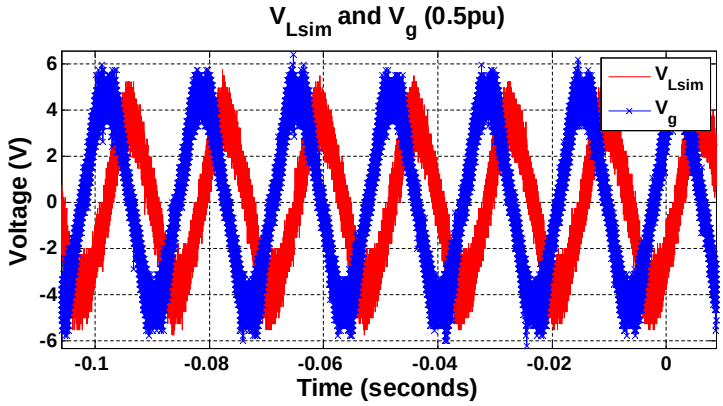

Figure 5.19: $L_{sim} = 0.5p.u.$ at $f_{pwm} = 20kHz$

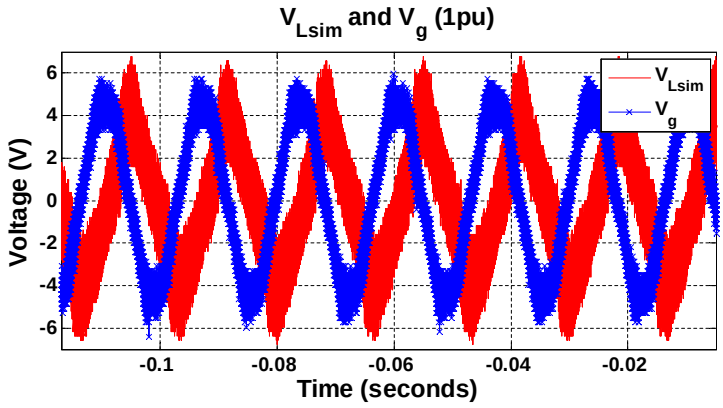

Figure 5.20: $L_{sim} = 1p.u.$ at $f_{pwm} = 20kHz$

The variable V_{Lsim} in the figures represents the voltage across L_{sim} and can be calculated by $V_{Lsim} = i_L \times \|L_{sim}\|$. It can be found that the magnitude of V_{Lsim} is mostly equal to V_g's and has 90 degrees phase delay to V_g. Similarly with the resistance loads, the current ripple goes up with the increasing of the impedance L_{sim}.

Series Inductor L and Current Ripple

In order to obtain better performance, the current ripple should be reduced to a certain range and the most efficient method is increasing the series inductance. In the experiments, $2.6mH$ and $26mH$ inductors are used separately to show the improvement on current ripples (Figure 5.21 to 5.24)

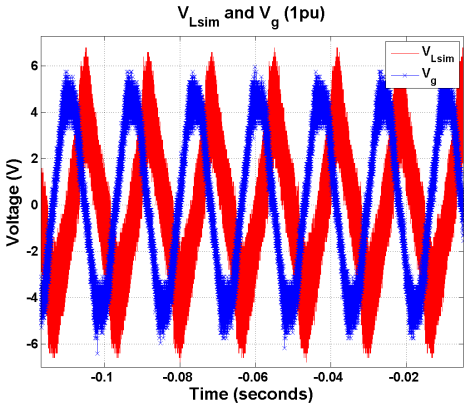

Figure 5.21: $L = 2.6mH$,$L_{sim} = 1p.u.$ and $f_{pwm} = 20kHz$

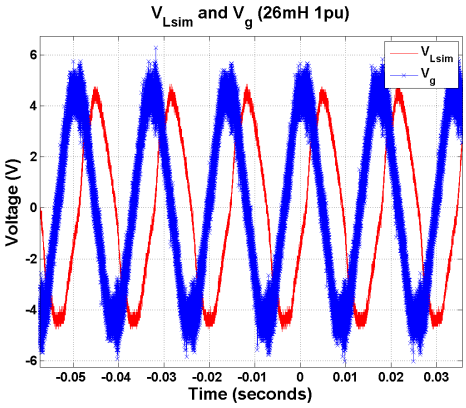

Figure 5.22: $L = 26mH$,$L_{sim} = 1p.u.$ and $f_{pwm} = 20kHz$

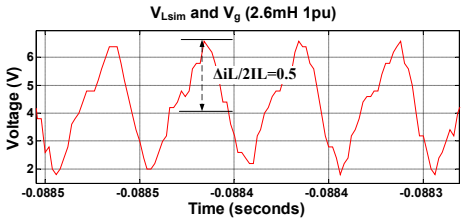

Figure 5.23: Current Ripple at $L = 2.6mH$

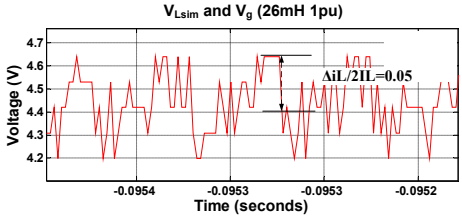

Figure 5.24: Current Ripple at $L = 26mH$

It can be seen in the figures above that the current ripple decreases significantly with the increasing of series inductance. The current ripple at

$L = 2.6mH$ is 10 times of the ripple at $L = 26mH$, which means the current ripple is inversely proportional to the series inductance.

5.4 Capacitive Load Results

The capacitance loads have the same features as the inductance loads and the only difference is that the phase angle of capacitance loads leads the AC source V_g by 90 degrees instead of 90 degrees delay. The following figures depict the range of capacitance loads at $L = 2.6mH$.

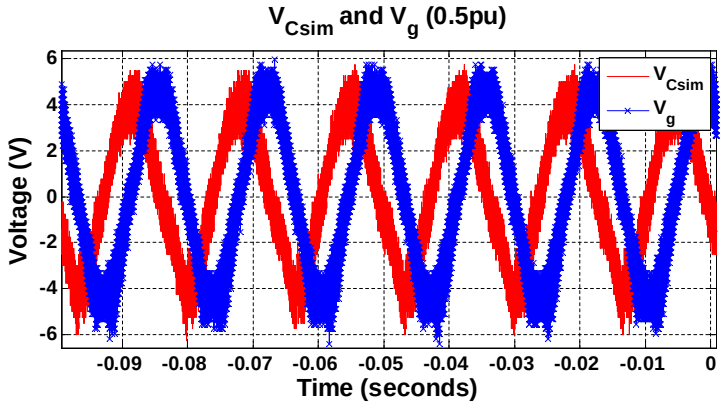

Figure 5.25: $C_{sim} = 0.5p.u.$ at $f_{pwm} = 20kHz$

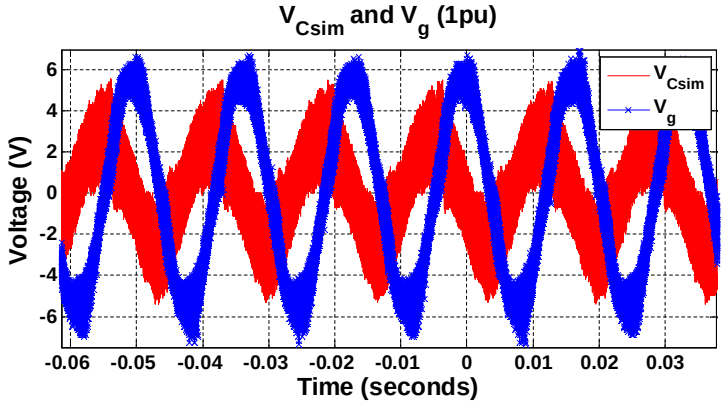

Figure 5.26: $C_{sim} = 1p.u.$ at $f_{pwm} = 20kHz$

Figures 5.27 to 5.30 show the the relationship between current ripple and series inductance. From the experimental results, it can be derived that the

current ripple is inversely proportional to the series inductance as same as the conclusion of inductive loads.

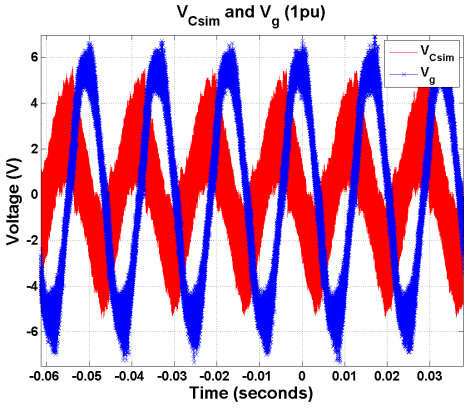

Figure 5.27: $L = 2.6mH$,$C_{sim} = 1p.u.$ and $f_{pwm} = 20kHz$

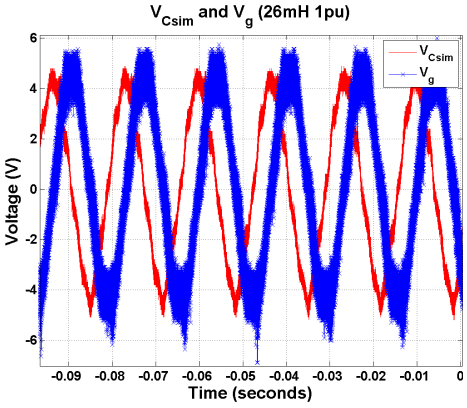

Figure 5.28: $L = 26mH$,$C_{sim} = 1p.u.$ and $f_{pwm} = 20kHz$

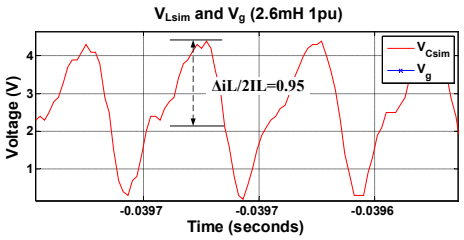

Figure 5.29: Current Ripple at $L = 2.6mH$

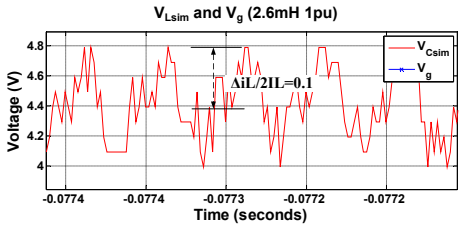

Figure 5.30: Current Ripple at $L = 26mH$

Chapter 6

Conclusions and Future Work

In this thesis, a DSP-controlled programmable AC electronic loads used in the unintentional islanding test has been implemented. A number of issues regarding the principles and the specifications of electronic loads have been investigated. In this final chapter a summary of the contributions contained in this thesis is made and some conclusions from this work are also presented. In the final section ideas for extending the results of this thesis are presented.

6.1 Synopsis

The chapter 2 introduced the basic principles of the AC electronic loads designed in this project. A schematic of AC electronic loads based on the H-bridge dc-dc converter with a regulated DC bus voltage was presented first. Then, some theoretical analysis of the limitations of this circuit was developed and the relationship between the parameters of the circuit and the range of the electronic loads was introduced to determine the specifications of this circuit for different electronic loads. At the end, some simulations using PSIM were performed to verify the specifications for different ranges of electronic loads obtained from the principles. Additionally, the ac small-signal model of this system was derived and a set of PI parameters was obtained using MATLAB and PSIM.

In the following chapter the hardware implementation was presented in detail. The features of the main parts, such as the IGBT module, the driver module and the ezDSP board, were introduced as well as the configurations of these parts. Then, the voltage and current measuring circuits, the temperature sensor and the protection circuits were presented.

The chapter 4 described the realization of the control program on TI's DSP TMS320LF2407A. At the beginning, a Q-format floating point representation for the fixed-point DSP was introduced and the normalization of voltage and current in the per-unit system was developed. A digital PI

control program was also presented here. At the end, the current control algorithm for different types of loads was described.

The chapter 5 showed the experimental results for different loads and conditions. The current ripples of the experimental results were analyzed and matched well with the theoretical analysis in the chapter 2.

6.2 Conclusions

This thesis has explored the design of an AC electronic loads used for the unintentional islanding test and a real hardware system has been developed and tested with a $60Hz$ AC voltage source. According to the experimental results, it is proved that this system is able to simulate different types of loads and in this project it was programmed to simulate resistive, inductive and capacitive loads. In order to simulate a complex circuit, some minor modifications of the current command calculation algorithm are required. Therefore, this device could work as a programmable AC electronic loads for the real unintentional islanding test.

However, because this system is based on an H-bridge inverter and works in the switching mode, the current ripple is much higher than that of the traditional electronic load which works in the linear mode.

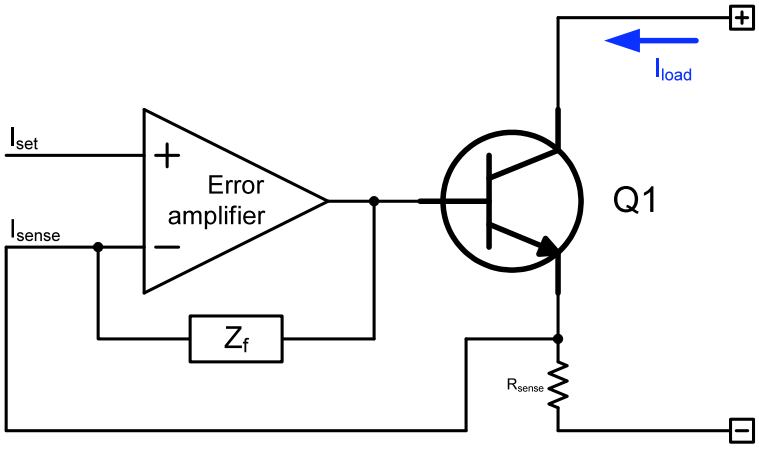

Figure 6.1: Simplified Electronic Load Diagram

Figure 6.1 shows the simplified structure of the traditional electronic load. I_{set} is the load current set value. I_{sense} is the actual load current

sense signal. The feedback circuit consists of error amplifier and feedback network Z_f. The amplifier compares the I_{set} and I_{sense}, the output signal is used to control power transistor $Q1$ base voltage. As a result, the power transistor $Q1$ only pulls current I_{load} equal to I_{set}, into the electronic load. When $I_{load} < I_{set}$, feedback circuit will turn on Q1 harder to pull more current until $I_{load} = I_{set}$. When $I_{load} > I_{set}$, feedback circuit will turn on Q1 less to pull less current until $I_{load} = I_{set}$.

Therefore, a combination of the switching mode and the linear mode might be a better solution for the higher accuracy requirement (shown in Figure 6.2). The switching mode block could track the required load characteristics and the linear mode block can compensate the current ripple induced by the switching operation to achieve the smoother load characteristics.

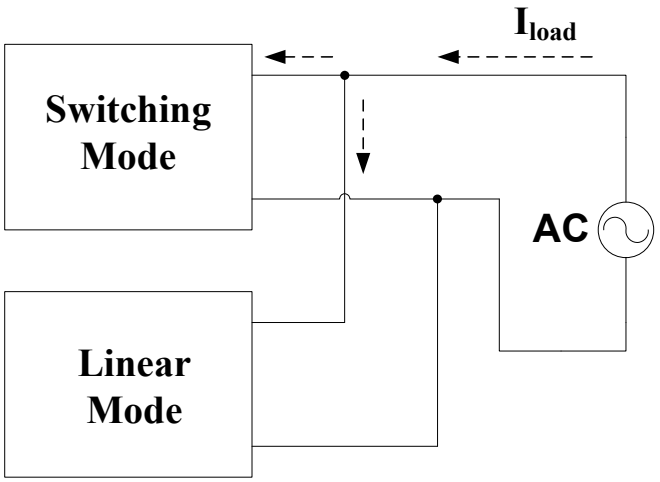

Figure 6.2: Combination Electronic Load Diagram

6.3 Suggestions for Future Work

It has been proved that the system designed in this thesis is able to work as an electronic load. But in order to finish the real unintentional islanding test, there is still a lot of work to do.

- A DC power supply which can output up to $220V$ is required for the real islanding test. As the previous analysis, the system need a

regulated DC bus voltage. Therefore, the islanding test needs a high voltage DC power supply to provide a high enough DC bus voltage.

- A three-phase four-leg inverter is required for the three-phase unintentional islanding test. In our design, the system is an H-bridge inverter which is only able to do the single phase islanding test. For the three-phase test, a four-leg inverter should be used and the schematic is shown in the Appendix B.

- The output filter has to be designed for the real test. Due to the switching parts are used in the circuit, a lot of high frequency interference is introduced. But in the real islanding test, too much noise will lead to the testing failure. Therefore, an output filter is needed to reduce the high frequency noise. (Shown in the Appendix B)

- A phase-locked loop (PLL) circuit is required for the frequency detection. In our design, the frequency detection was implemented in the DSP program. However, it is not very accurate and unable to perform a real-time frequency detection. The PLL circuit can detect the real-time frequency of the applied voltage source and provide a high precision.

- Modify the current calculation algorithm for the islanding test. The islanding test requires a variable LC circuit with respect to the different output reactive power generate by the device under test. So a new current calculation algorithm has to be implemented.

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Appendix A

Schematics

A.1 Schematics of Control Board

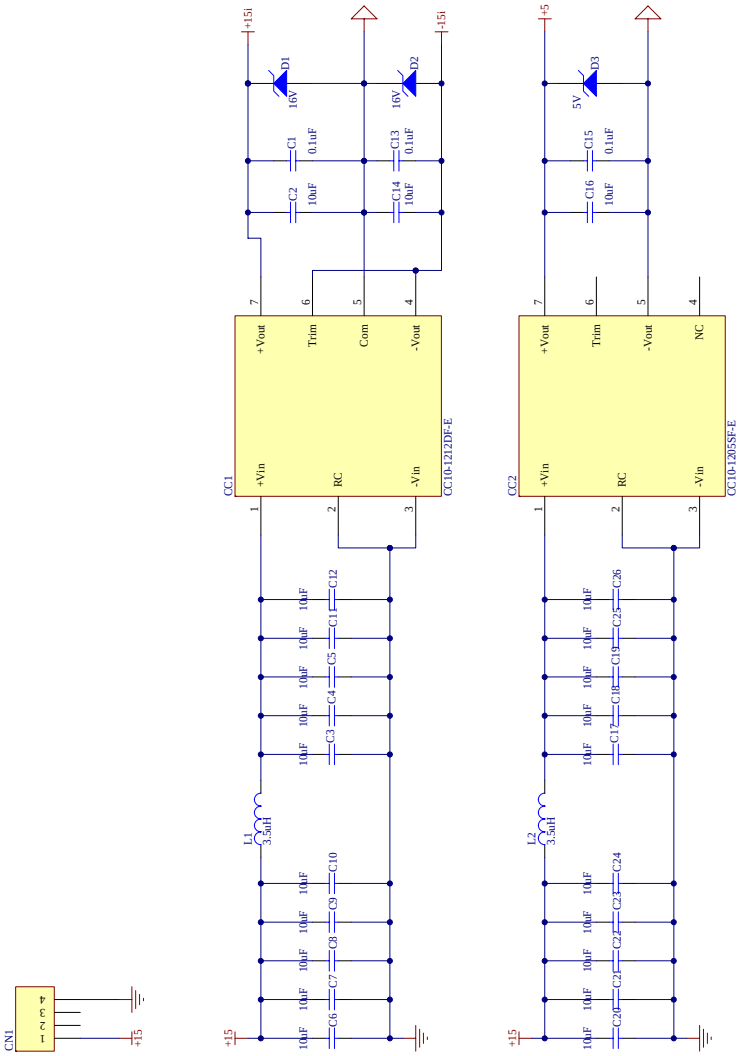


Figure A.1: PowerSupply_AD.SCHDOC

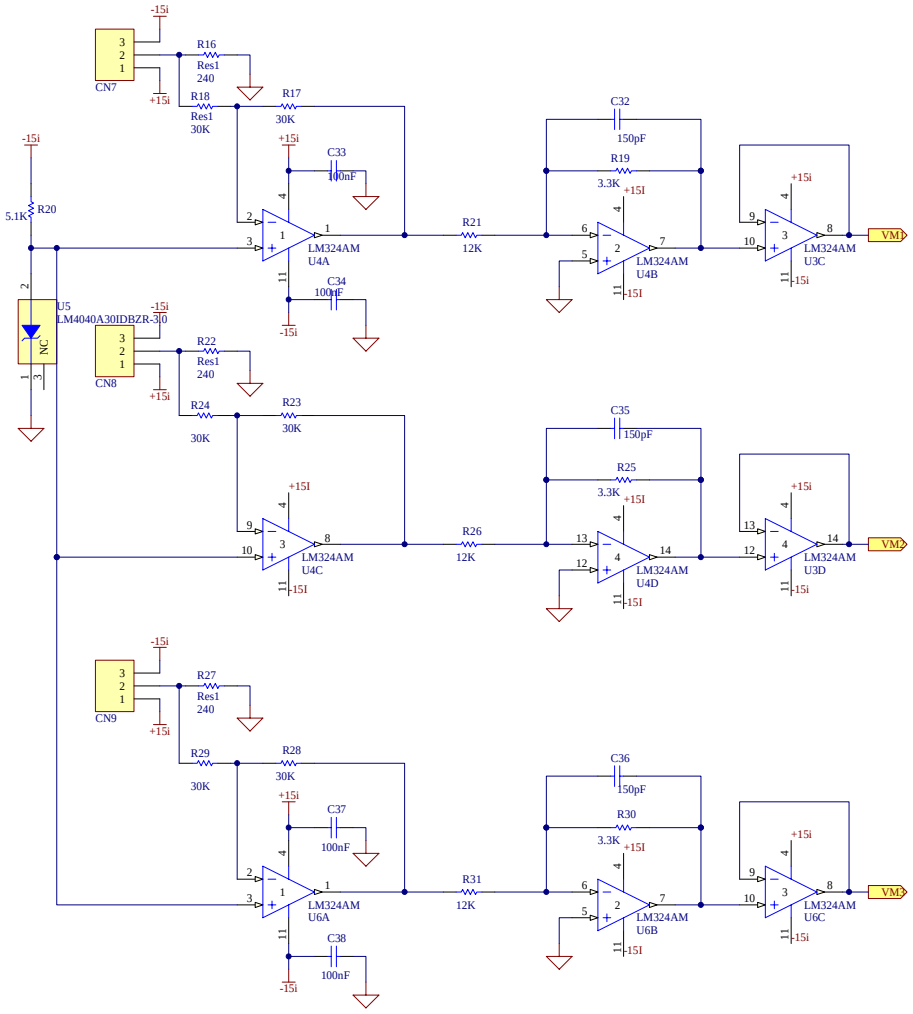


Figure A.2: VoltageSensor.SCHDOC

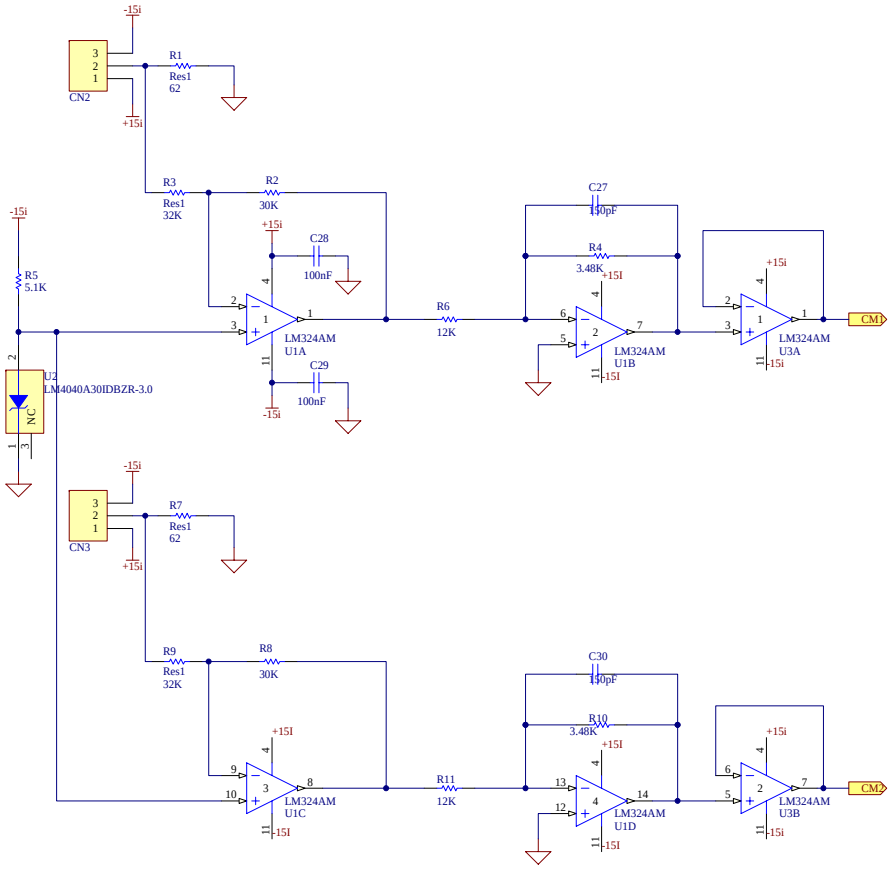
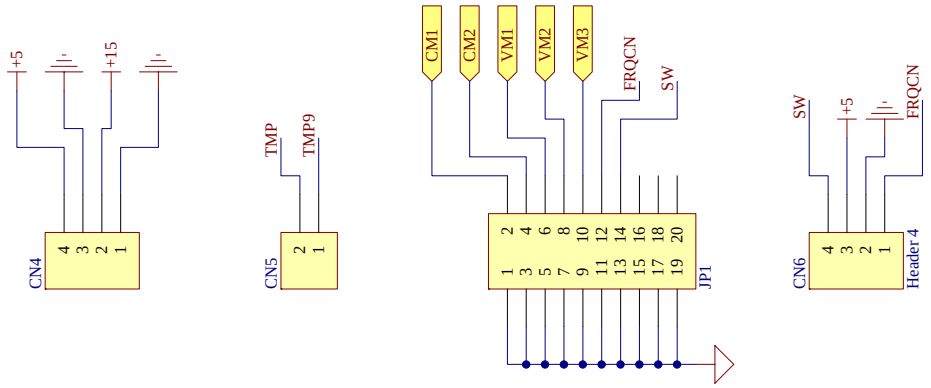


Figure A.3: CurrentSensor.SCHDOC



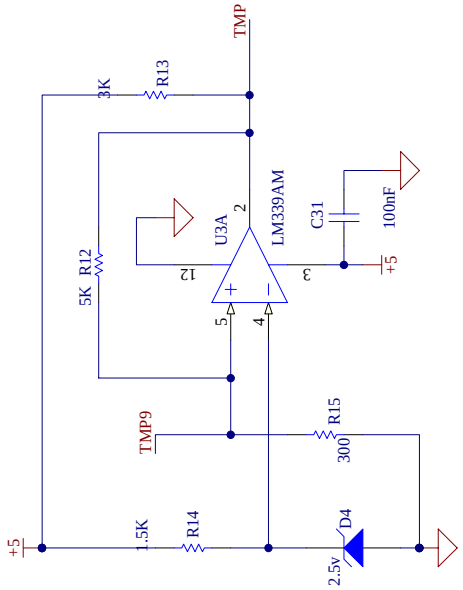


Figure A.4: TMPSensor.SCHDOC

A.2 Schematics of Power Board

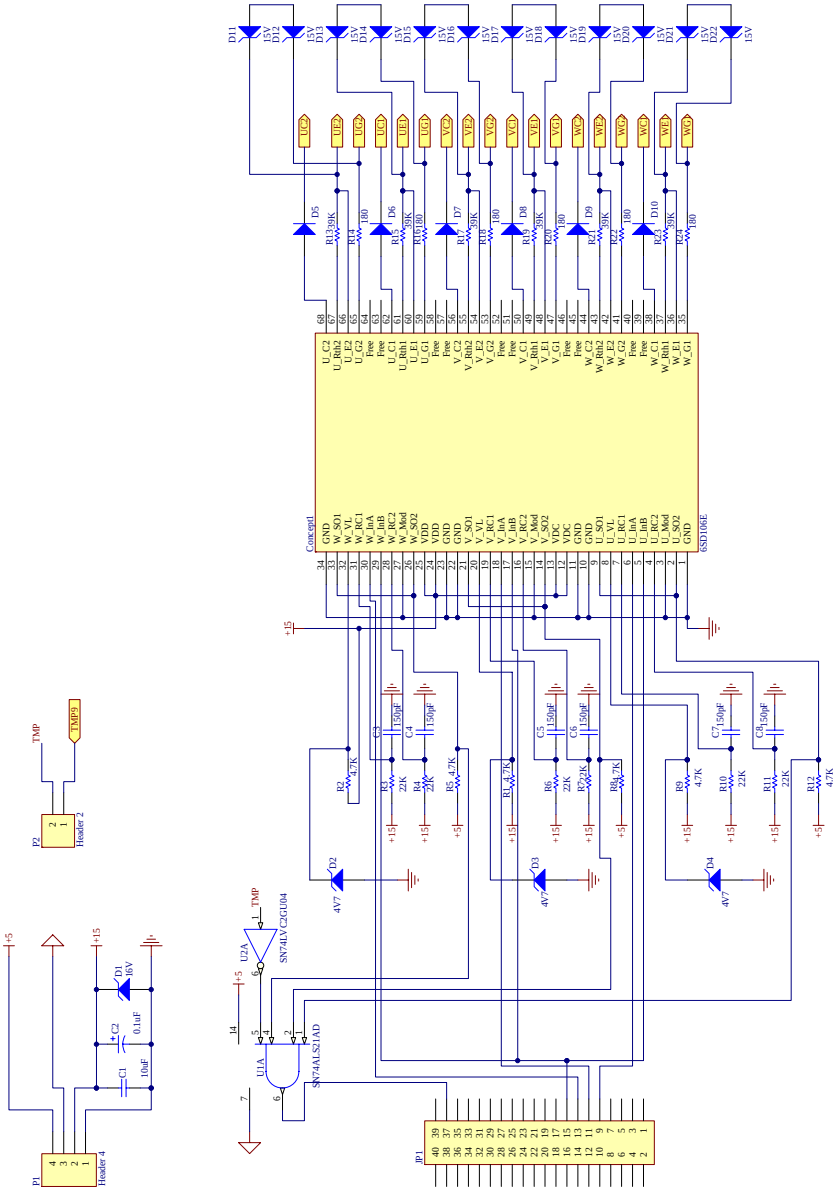


Figure A.5: Driver.SCHDOC

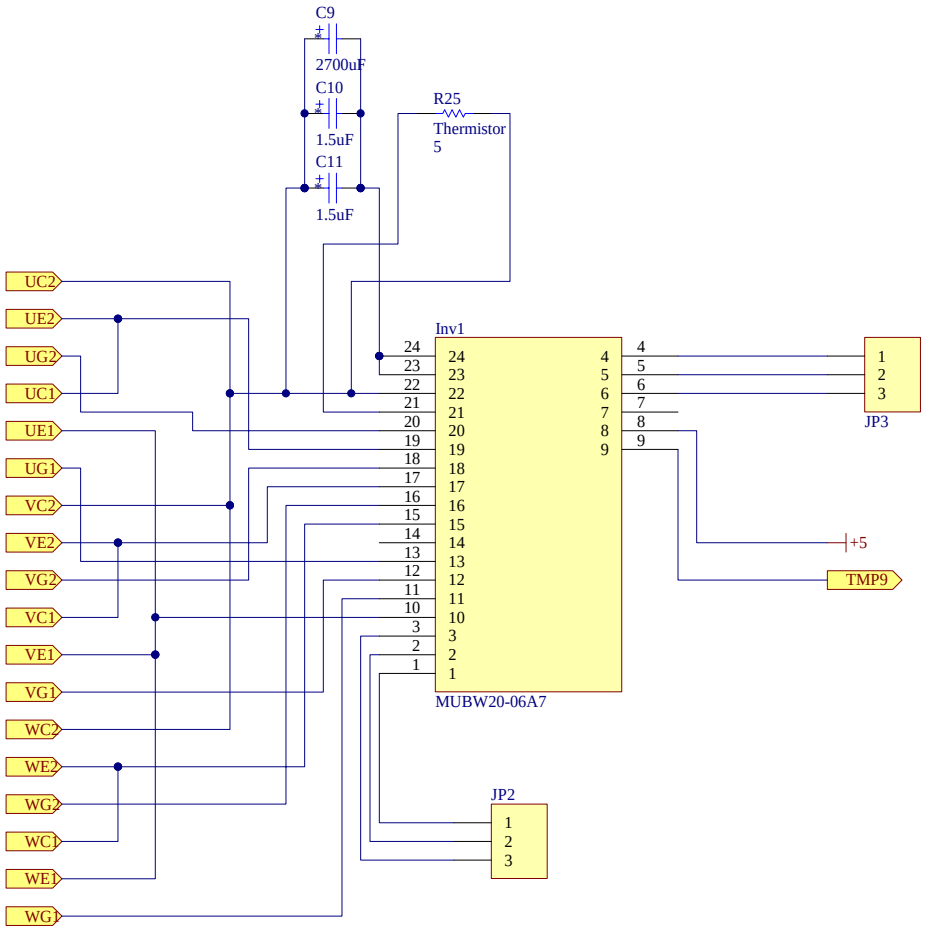


Figure A.6: MUBW20.SCHDOC

A.3 PCB Layouts

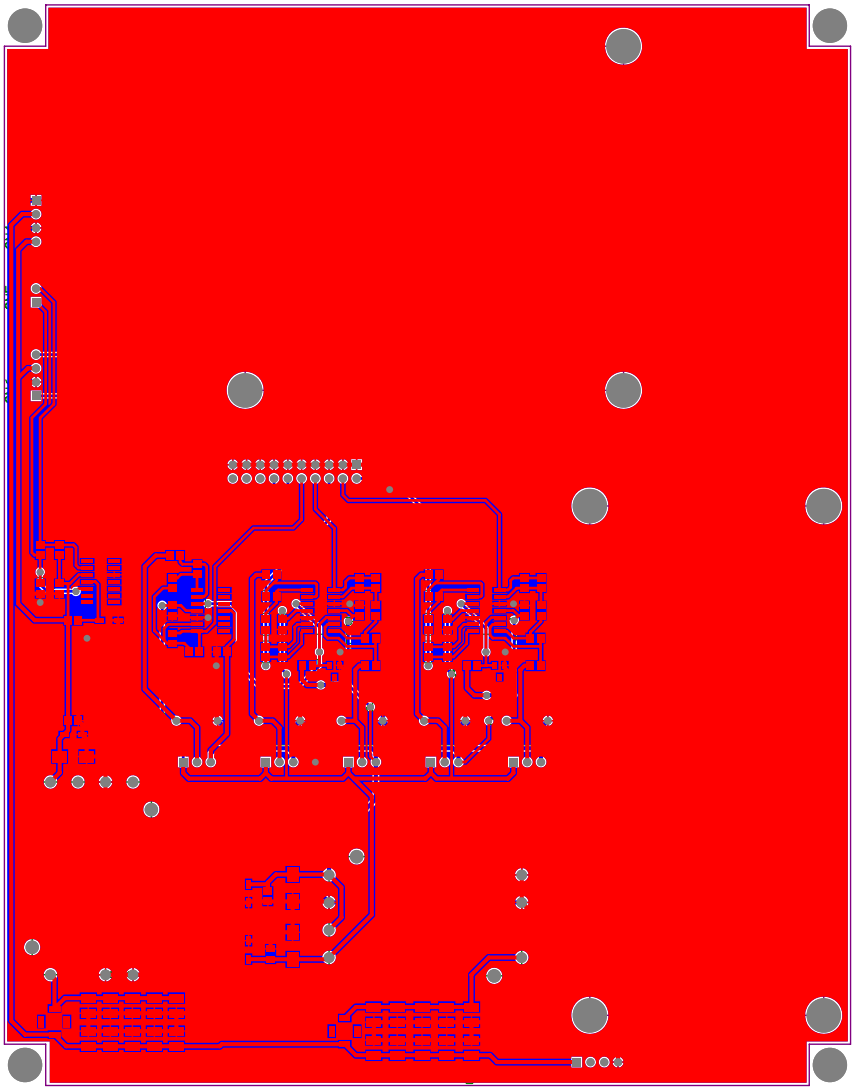


Figure A.7: Control Board PCB

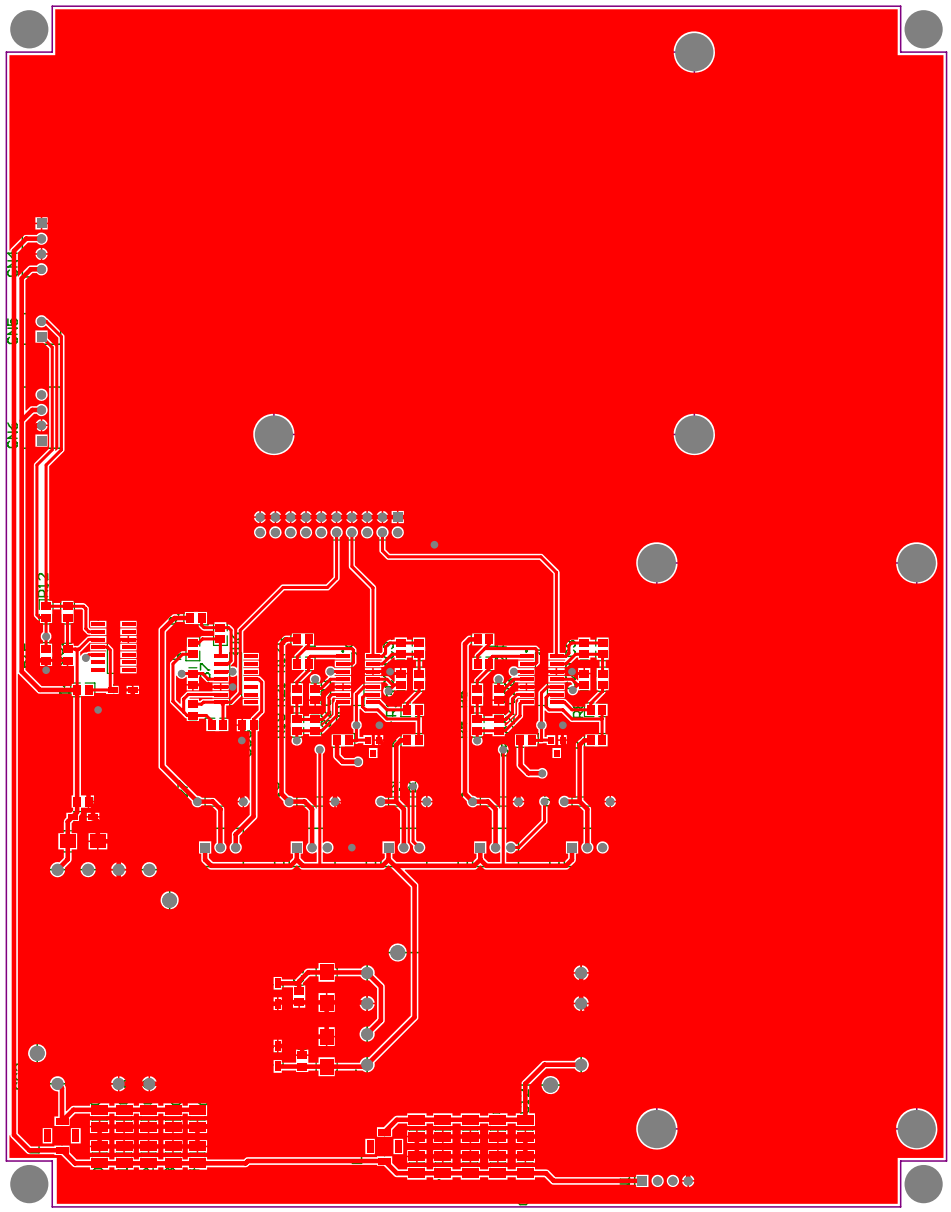


Figure A.8: Control Board PCB Top Layer

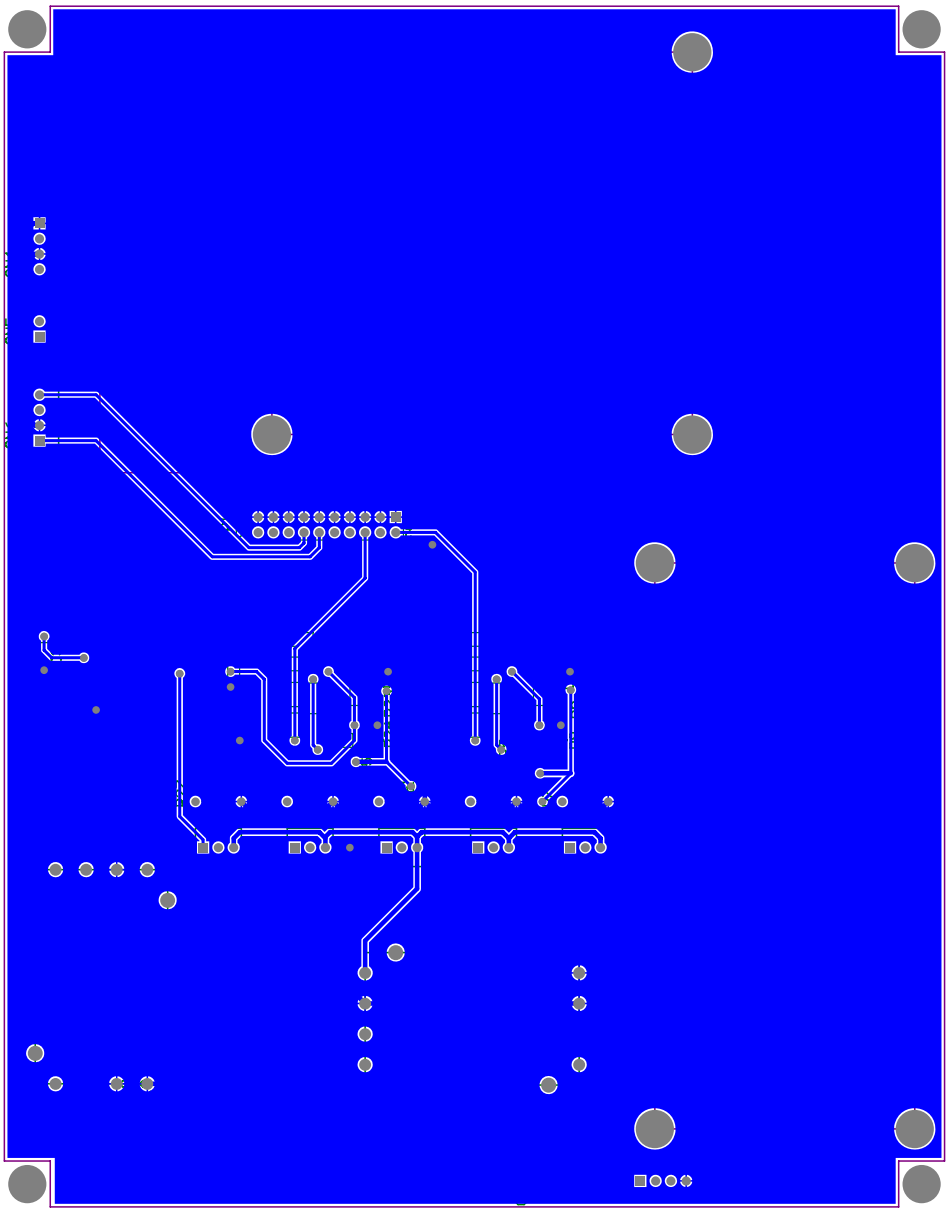


Figure A.9: Control Board PCB Bottom Layer

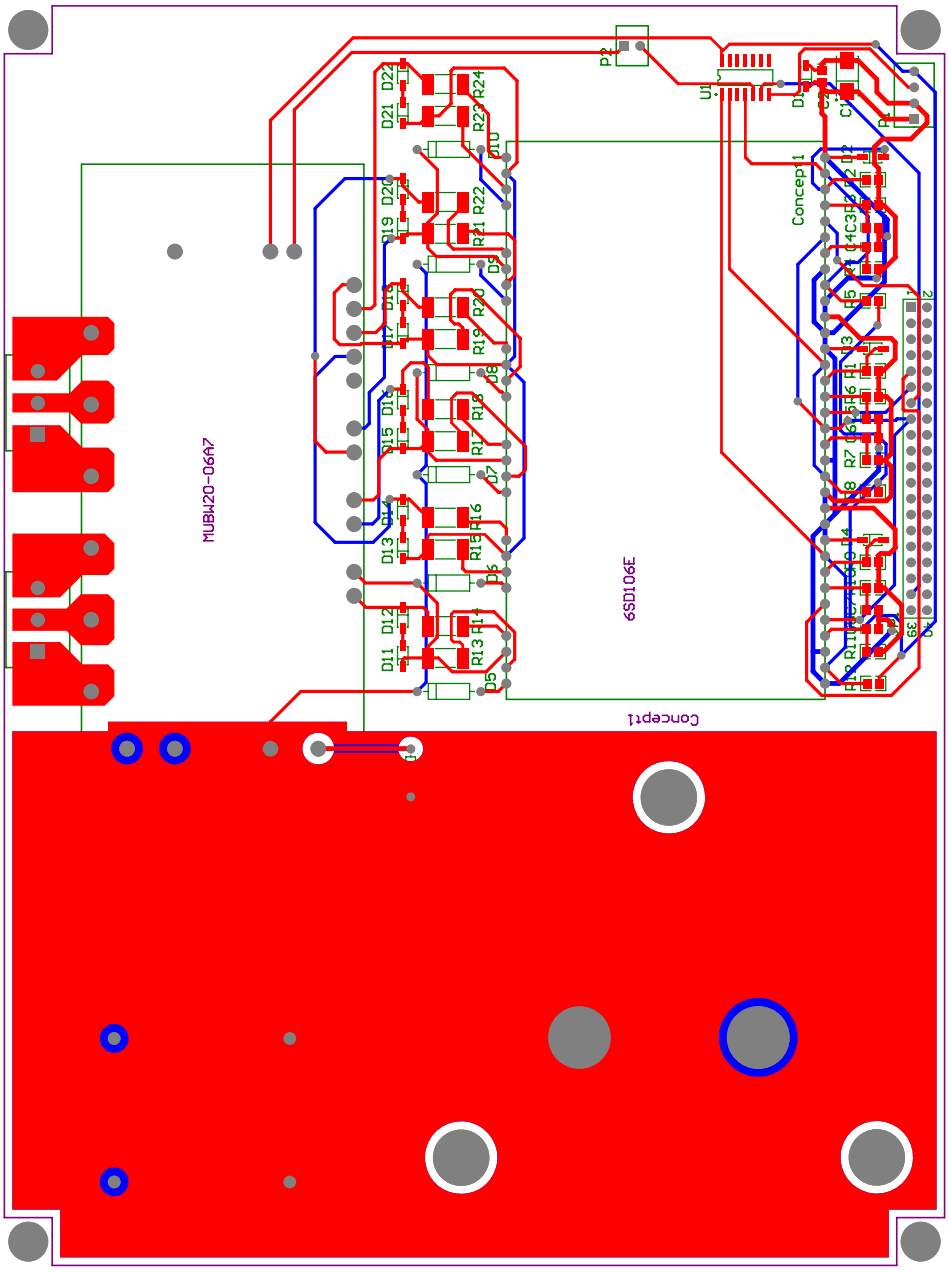


Figure A.10: Power Board PCB

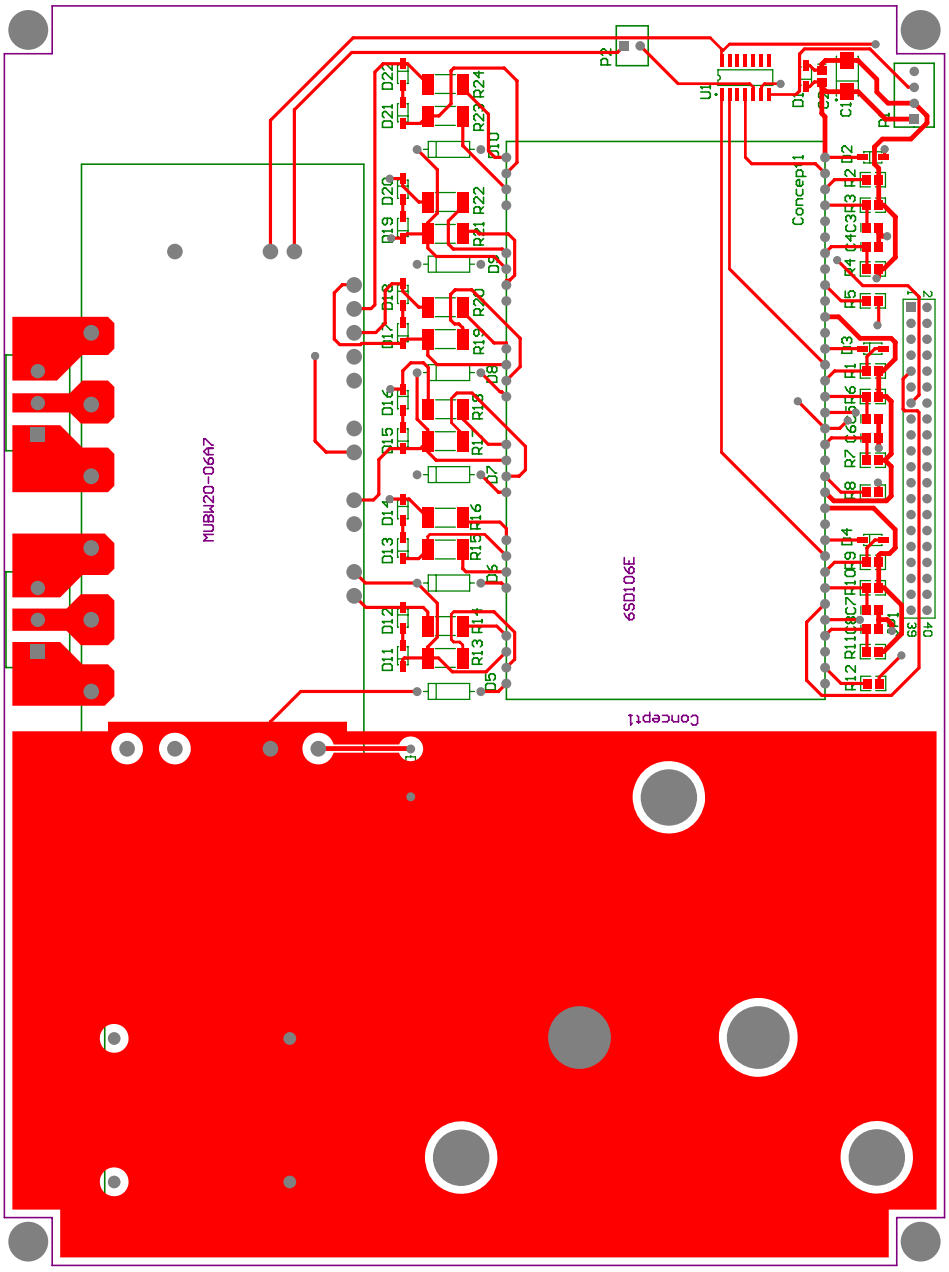


Figure A.11: Power Board PCB Top Layer

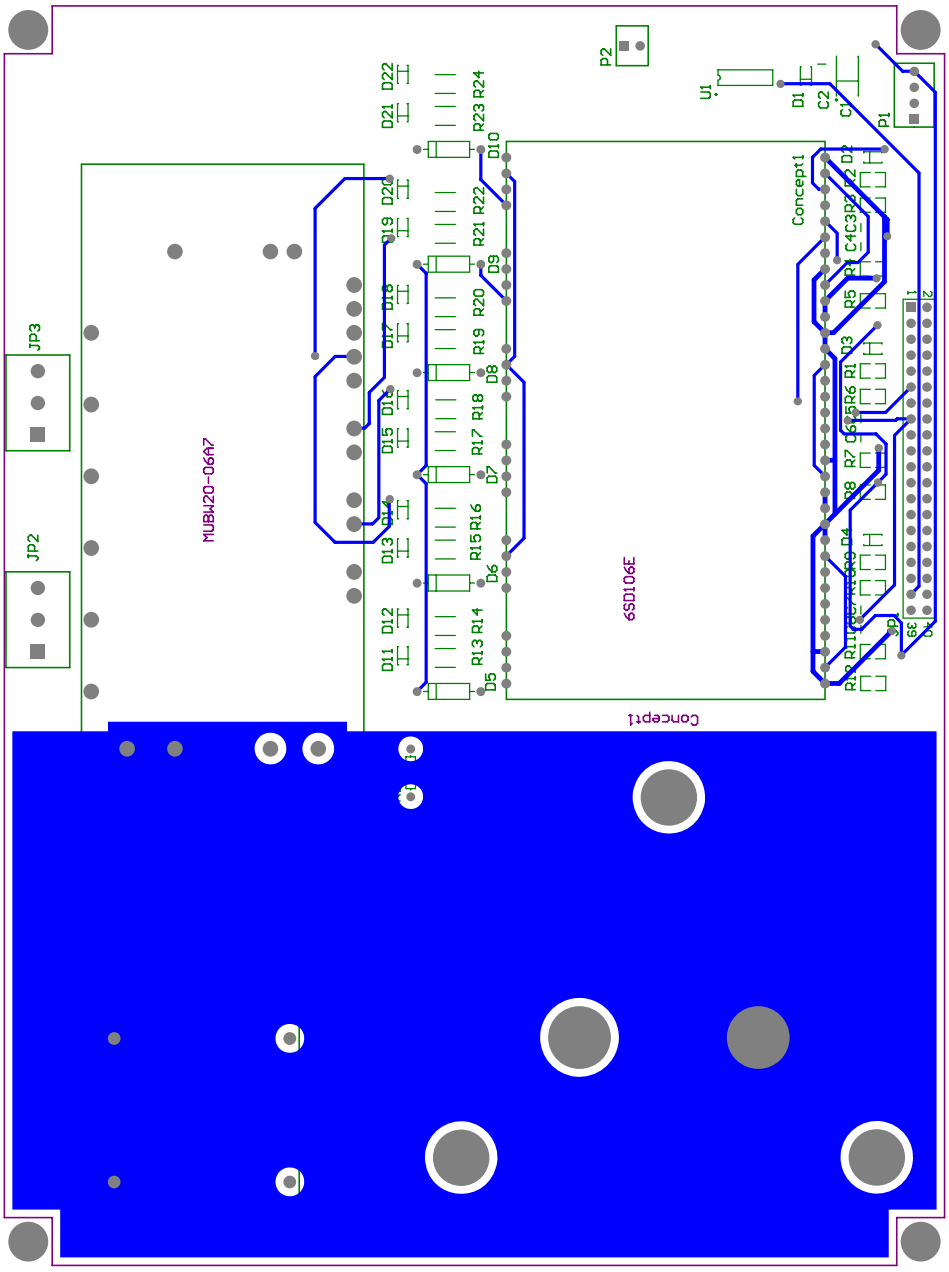


Figure A.12: Power Board PCB Bottom Layer

Appendix B

Schematics for 3-Phase Islanding Test

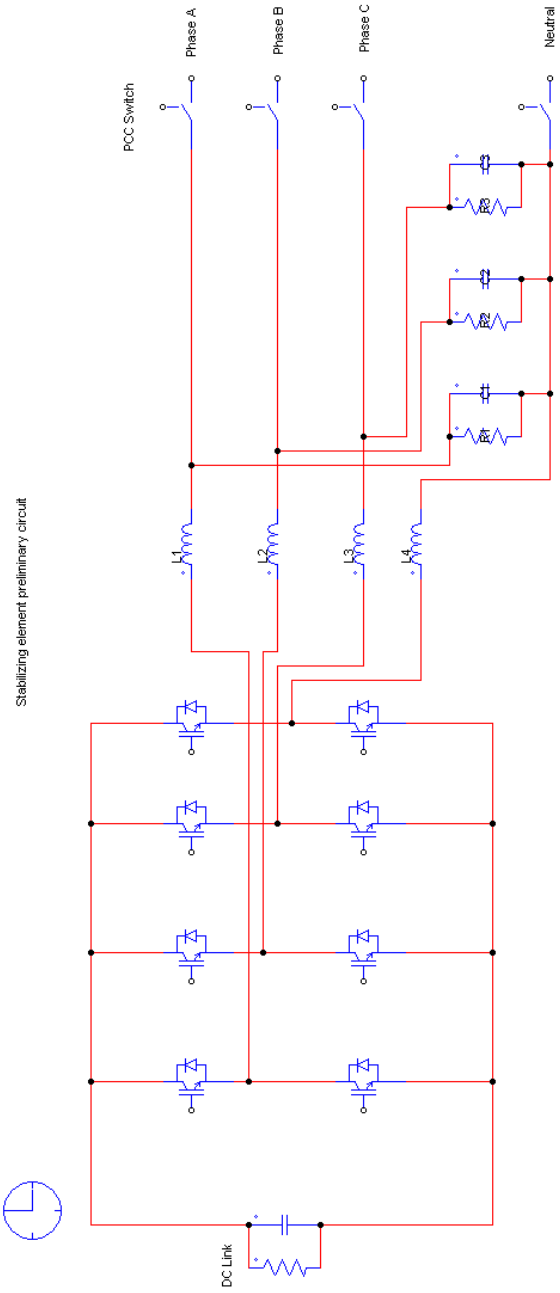


Figure B.1: Schematics for 3-phase Islanding Test

Appendix C

Unintentional Islanding Test Conditions

Unintentional Islanding Test
Test conditions:

1. *Single Phase* 120V / 60H$_Z$ / 1kW
2. $PF = [1, 0.37, 0.707] \Leftrightarrow Q_f = [0, 2.5, 1]$

Values Table:

Criteria	Value	Unit	Notes
P_{load}	1000	W	
Q_{load}	0	VAR	Matched LC
V_{EPS}	120	V	RMS
f_{EPS}	60	Hz	
V_{IUT}	120	V	Inverter Under Test
P_{IUT}	1000	W	
I_{IUT}	8.33	A	RMS
PF_{IUT}	0.95		θ=18.195^o
Q_f	1		RLC below designed for this Q_f
R_{load}	14.4	OHM	V^2/P
L_{Load}	38.197	*m*H	$R / (2\pi f_o Q_f)$, $i_L(0)$=11.785A
C_{Load}	184.207	μF	$Q_f / (2\pi f_o R)$
Q_f	2.5		RLC below designed for this Q_f
R_{load}	14.4	OHM	V^2/P
L_{Load}	15.28	*m*H	$R / (2\pi f_o Q_f)$, $i_L(0)$=11.785A
C_{Load}	460.52	μF	$Q_f / (2\pi f_o R)$

$Q_f = R\sqrt{\frac{C}{L}}$ for a parallel RLC load, and $Q_F = \sqrt{\frac{1}{PF^2} - 1}$.

$P_{IUT} = P_{Load} + P_{EPS}$ & $Q_{IUT} = Q_{Load} + Q_{EPS}$