DESIGN AND IMPLEMENTATION OF A BOOST ACTIVE POWER FACTOR CORRECTOR

by

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Abstract

The input current harmonics of the rectifier are very harmful. Not only do they reduce the power factor of the AC-DC converter and cause a lot of electrical energy loss, but also damage other devices and pollute the line power system. Measures should be taken to reduce these harmonics. The commonly used method is to design an effective PFC circuit for the AC-DC converter. In this thesis, a Boost APFC circuit will be discussed in detail.

This thesis presents a solution to design an appropriate APFC circuit with one Kilowatts output power and make this APFC circuit work satisfactorily from full load to half load scope. In this thesis, a detailed design process will be described for this project, including topology choice, theoretical calculation of the main components values, the determination of the main components for this circuit, circuit simulation and experimental verification. In the end, a concise conclusion will be made and the future improvement for this project will be introduced.

Several commonly used control methods for the Active Power Factor Corrector circuit will be compared and then a good method will be chosen for this project. The average current control method is finally decided to use for this circuit and the basic control chip UC3854 is used to build the control circuit for this project. The simulation and the final experimental results all verify that this is an appropriate choice for this project.

According to the schematic design and the simulation revision, a test prototype is built to verify the performance. Several tests are implemented and the final experimental results indicate that this circuit design can satisfy the project specification and it is feasible for this project.
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Chapter 1
Introduction

1.1 AC-DC Rectifier Overview

For the AC-DC-DC switching power supply, a full wave rectifier and a parallel capacitor are often used to get the initial DC voltage for the following DC-DC converter. Because the rectifier is non-linear and the filter capacitor is an energy-storage component, the combination of them will make the input current distort greatly [1]. Please see Fig. 1.1[A] for the corresponding waveforms where "t" for time (milliseconds), "V_{in}" for electrical input voltage (Volts), "V_o" for output voltage (Volts) and "I_{in}" for electrical input current (Amperes). Please see Fig. 1.2 for the corresponding spectrum of I_{in}.

Fig. 1.1 AC-DC Rectifier Circuit
Fig. 1.1[A] AC-DC Rectifier Simulation

$I_n$: Input Line Current (Amperes)
$V_{in}$: Input Line Voltage (Volts)
$I_{ind}$: Rectified DC Current (Amperes)
$V_o$: Output Voltage of the Rectifier (Volts)
The pulsing input current contains a lot of harmonic components. This will reduce the power factor greatly. Besides this, a lot of current harmonic emission will make the line voltage distort and the adjacent equipment out of order. In order to reduce the pollution caused by input harmonic current of AC-DC converter and improve the input power factor, measures should be taken to limit the harmonic components of the input current.

1.2 Two Widely Used Methods to Improve the Power Factor of the AC-DC Converter

1.2.1 Using Common “L” Filter

One way is to add an inductor between the rectifier and the filter capacitor $C$ to form an $L$ filter; another way is to connect an $L$ filter at the AC side of the rectifier. Certainly, these two methods can be combined together, and this will be more effective.
Chapter 1 Introduction

[1]. Please see Fig. 1.3[A] for the corresponding waveforms for this topology where “t” for time (milliseconds), “V_{in}” for input electrical voltage (Volts) and “I_{in}” for electrical current (Amperes). Figure 1.4 gives the FFT spectrum of I_{in} under this situation.

Fig. 1.3 Rectifier with "L" Filter

Fig. 1.3[A] Simulation of Rectifier with "L" Filter

I_{in}: Input Line Current (Amperes)
V_{in}: Input Line Voltage (Volts)
By comparing these two figures, it can be found that the “L” filter makes the input current from the line power much smoother than the pulsing input current created by the capacitor input filter. Therefore, the power factor will be improved. The advantages of this method are simple, cheap, reliable and low EMI. The disadvantages for this way are large volume, heavy and difficult to make the power factor approach unity. Its function is relevant to line frequency, load change and the variation of the input line voltage. There is high charging and discharging current between the inductor and the capacitor. It is often used in the situation without very strict requirement of input power factor, such as the frequency converter.

1.2.2 Using Active Power Factor Corrector

The objective of active power factor correction is to make the input to a power supply look like a simple resistor. An active power factor corrector does this by programming the input current in response to the input voltage. As long as the ratio between the voltage and current is a constant, the input will be resistive and the power

Fig. 1.4 Spectrum of $I_n$ with "L" Filter
factor will be equal to one. When the ratio deviates from a constant, the input current will contain phase displacement, harmonic distortion or both. Either one will degrade the power factor. The most general definition of power factor is the ratio of real power to apparent power.

\[
P_F = \frac{P}{(V_{rms} \times I_{rms})}
\]

Where \( P \) is the real input power; \( V_{rms} \) and \( I_{rms} \) are the root mean square (RMS) voltage and current of the load, or power factor corrector input in this case [5], [7]. If the load is a pure resistance, the real power and the product of the RMS voltage and current will be the same and the power factor will be equal to unity. If the load is not a pure resistance, the power factor will be less than unity.

Phase displacement is a measure of the reactance of the input impedance of the active power factor corrector. Any amount of reactance, either inductive or capacitive will cause phase displacement of the input current waveform with respect to the input voltage waveform. The phase displacement of the voltage and current is the classic definition of power factor which is the cosine of the phase angle between the voltage and current sinusoids.

\[
P_F = \cos \theta
\]

The amount of displacement between the voltage and current indicates the degree to which the load is reactive. If the reactance is a small part of the impedance, the phase displacement will be small. An active power factor corrector will generate phase displacement of the input current if there is phase shift in the feed-forward signals or in the control loops. Any filtering of the AC line current will also produce phase displacement.

Harmonic distortion is a measure of the non-linearity of the input impedance of the active power factor corrector. Any variation of the input impedance as a function of the input voltage will cause distortion of the input current and this distortion is the other contributor to poor power factor. Distortion increases the RMS value of the current
without increasing the total average power being drawn. Therefore, a non-linear load will have a poor power factor because the RMS value of the current is high but the total average power delivered is small. If the non-linearity is small the harmonic distortion will be low. Distortion in an active power factor corrector comes from several sources: the feed-forward signals, the feedback loops, the output capacitor, the inductor and the input rectifiers.

An active power factor corrector can easily achieve a high input power factor, usually much greater than 0.9. However, power factor is not a sensitive measure of the distortion or the displacement of the current waveform. It is often more convenient to deal with these quantities directly rather than with the power factor. For example, 3% harmonic distortion alone has a power factor of 0.999. A current with 30% total harmonic distortion still has a power factor of 0.95. A current with a phase displacement of 25 degrees from the voltage has a power factor of 0.90.

A DC-DC switching converter can be connected between the rectifier and load to realize active power factor corrector topology [1], [11]. In this way, the wave shape of the input current can be made similar to that of input line voltage by applying the current feedback control technology [1], [13]. Therefore, the power factor can be improved to 0.99 or higher.

Its advantages include high power factor [0.97–0.99], very low total harmonic distortion, stable output voltage, small volume and low weight.

Its disadvantages include complex electrical circuit, expensive cost and high EMI. Certainly, these will make the efficiency reduce a little.

1.3 Thesis Motivation and Objective

The objective of this thesis is to clarify the practical approaches to set up an active power factor corrector; this circuit must satisfy the power factor requirement from full load to half load range. The specific objectives include:
(1) To choose a reasonable topology for this APFC project
(2) To calculate the main component values with power electronic theory
(3) To determine appropriate control method for this project
(4) To simulate this APFC circuit during the required load scope and input power
(5) To test the prototype and characteristics related to the theoretical analysis

This thesis is organized into six chapters. Chapter 1 gives a brief introduction of the commonly used methods to improve power factor and outlines the objectives of this thesis. In Chapter 2, an appropriate main circuit topology and a suitable control method for this project will be explained at first and then the detailed theoretical calculation of the main components value will be given. Chapter 3 is focused on main component part number determination, hardware choice and setup for this boost APFC circuit. Chapter 4 will deal with the simulation of the determined topology in the required load scope and input power. Revision to the project circuit and some experimental results are included in Chapter 5. The last chapter gives a conclusion of this project design and suggests some meaningful work to be done in the future.

1.4 Project Specifications

According to the requirement for this active power factor corrector, the specifications for this project are determined as following:

(1) $P_{\text{out}}: 1000\text{W}$
(2) $V_{\text{in\ range}}: \text{AC } 200V_{\text{rms}} \sim 230V_{\text{rms}}$
(3) Line frequency range: 50Hz ~ 60Hz
(4) Output voltage: $400V_{\text{dc}}$
(5) Input power factor: 0.99 or higher
Chapter 2
Schematic Design of Boost Active Power Factor Corrector

2.1 Main Circuit Topology

It is very important to choose an appropriate topology in engineering project design; otherwise, it is impossible to make the circuit perform satisfactorily. Theoretically, any kind of DC-DC converter, such as Buck, Boost, Buck-boost or Cuk converter can be used as the main circuit of a power factor corrector, but the Boost converter is widely used because of its special advantages. Finally, the Boost converter is chosen to be the power circuit of this APFC project. These four converters will be compared and the reason for this topology selection will be explained in the following:

Buck Converter

The Buck converter is as following:

\[ V_o = D V_g \]  \hspace{1cm} (2-1)

\( V_o \) is the output voltage; \( V_g \) is input voltage and \( D \) is the duty cycle of the converter \((0 \leq D \leq 1)\) [11], [9]. It can be seen that the buck converter can only lower the input
voltage; however, as a part of a large power supply, it is often required that the output voltage of the APFC circuitry is in the range of 380Volts to 420Volts so that it can reduce the loss and improve the efficiency. This is the output voltage specification for this project. Obviously, the Buck converter can not satisfy the requirement either for European standard (230V/50 Hz) or North American standard (120V/60Hz). Therefore, it is not appropriate for this project.

**Buck-boost Converter**

The Buck-boost converter is as following:

![Buck-boost Converter circuit](Fig. 2.2)

The relationship between its input voltage $V_g$ and its output voltage $V_o$ is:

$$V_o = -DV_g / (1-D)$$

(2-2)

$D$ is the duty cycle of the converter ($0 \leq D \leq 1$) [11], [9]. This converter can both boost and lower the input voltage. Only from the view of satisfying the output voltage requirement, it can solve this question. However, the input current of this converter is not continuous and its input power factor is not satisfactory. Obviously, this conflicts with the aim of the power factor corrector. If it is used as the power circuit, a Low–Pass LC filter must be added to its input and this will make the circuit complicated. All these characteristics suggest that a better converter topology should be chosen for this project.

**Cuk Converter**

The Cuk converter is as following:
Chapter 2 Schematic Design of Boost Active Power Factor Corrector

Fig. 2.3 Cuk Converter circuit

The relationship between its input voltage $V_g$ and its output voltage $V_o$ is:

$$V_o = \frac{-D V_g}{(1-D)}$$  \hspace{1cm} (2-3)

$D$ is the duty cycle of the converter $(0 \leq D \leq 1)$ [11], [9].

It can increase or decrease the input voltage and its input current is continuous. It seems that the Cuk converter is a right choice for this question, however, it can be found that the Cuk converter is more complicated than Boost converter. Besides this, the energy transformation mainly relies on the capacitor $C_j$ in Cuk converter; this will require that the capacitor $C_j$ can endure great ripple current. This kind of capacitors is expensive and their reliability is not very good. Considering all of these factors, other simple feasible methods should be searched for this project.

Boost Converter

The Boost converter is as following:

Fig. 2.4 Boost Converter circuit

The ideal relationship between its input voltage $V_g$ and its output voltage $V_o$ is:
Chapter 2 Schematic Design of Boost Active Power Factor Corrector

\[ V_o = \frac{v_o}{1-D} \]  \hspace{1cm} (2-4)

\( D \) is the duty cycle of the converter \( (0 \leq D \leq 1) \) [11], [9].

Its input current is continuous and this will reduce the input current harmonics greatly. It is simple compared with Cuk and revised Buck-boost converter. It is easier to drive the power switch because the potential of its reference point (Source pole) is zero. The disadvantage of the boost regulator is the high output voltage required. The output voltage must be greater than the highest expected peak input voltage, but, it doesn’t matter for this project. After careful comparison of these four kinds of converters, it can be seen that the Boost converter is a good choice for this project.

2.2 The Theory of the Boost APFC

The input current of the boost regulator must be forced or programmed to be proportional to the input voltage for power factor correction. Feedback is necessary to control the input current. The power circuit of a boost power factor corrector is the same as that of a DC to DC boost converter. There is a diode bridge rectifier ahead of the inductor to rectify the AC input voltage but the large input capacitor which would normally be associated with the AC to DC conversion function has been moved to the output of the boost converter. If a capacitor follows the input diode bridge rectifier, it is a small one used only for noise control. The output of the boost regulator is a constant voltage but the input current is programmed by the input voltage to be a half sine wave. The power flow into the output capacitor is not constant but is a sine wave at twice the line frequency since power is the instantaneous product of voltage and current. The output capacitor stores energy when the input voltage is high and releases the energy when the input voltage is low to maintain the output power flow.

Generally speaking, there are three common controlling methods for Boost APFC. They are average current control, peak current control and hysteretic current control. Among these three methods, the average current control method is often used because the
total harmonic distortion is very low and the average current \( i_L \) is insensitive to the noise in this way. Certainly, the error between the peak value of the inductor current \( i_L \) and the average current in this way is lower than that in the other two ways. The average current control can be used in continuous conduction mode and discontinuous conduction mode. The other two methods can be used only in continuous conduction mode and the current peak value is sensitive to noise. For the Boost APFC with average current control, please see Fig. 2.5 [1]. An active power factor corrector must control both the input current and the output voltage. The current loop is programmed by the rectified line voltage so that the input to the converter will appear to be resistive. The output voltage is controlled by changing the average amplitude of the current programming signal. An analog multiplier creates the current programming signal by multiplying the rectified line voltage with the output of the voltage error amplifier so that the current programming signal has the shape of the input voltage and the average output voltage amplitude which controls the output voltage.

Here, the inductor current \( i_L \) is measured directly; the obtained signal \( i_L R_d \) is sent to CA---current error amplifier. The reference current of CA is the output signal of multiplier "M" which has two input signals---one is the error signal of output voltage \( V_o/H \) and reference voltage \( V_{ref} \); the other is the measured value of \( V_{dc} \). \( V_{dc} \) is full wave rectified value of input sine voltage \( V_i \). Therefore, the reference current signal is double half sine wave voltage. After comparing with standard current, the variation of the high frequency signal of the input inductor current \( i_L \) will be averaged by the current error amplifier---CA. After the amplified average current error signal is compared with ramp oscillator wave, the PWM will send the appropriate driving signal to the power switch IGBT and determine the proper duty cycle for this power switch. In the end, the current error will be corrected fast and accurately and the input power factor will be improved nearly to unity. The wave shape of the inductor current \( i_L \) is shown as Fig. 2.6. In order
to be clear, the two kilohertz is used as the input line frequency in this demonstrative example.

![Diagram of Boost APFC Circuit with Average Current Control](image)

**Fig. 2.5 Boost APFC Circuit with Average Current Control**
Fig. 2.6 Simulation of Inductor Current and Output Voltage

I\textsubscript{ind}: Inductor Current (Amperes)

V\textsubscript{o}: Output Voltage (Volts)

According to this average current control theory, the basic control chip UC3854 is used to construct the whole control circuit for this boost active power factor corrector. Please see Fig. 2.7 for the final schematic Boost APFC circuitry.
Chapter 2 Schematic Design of Boost Active Power Factor Corrector

UC3854 Controlled PFC Converter

Fig. 2.7 Boost APFC Schematic Circuit

Here, the choice of the switching frequency and main power switch will be

Note: This circuit can be simulated by the full version only.
explained separately because they are important for the converter to have satisfactory performance.

1: The Choice of the Switching Frequency:

It is well known that the switching frequency correlates to the performance of the power factor corrector. When the frequency is lower than 20kHz, the performance of the power factor corrector will not be satisfactory, the ripple will be large, the instant responding will be slow, the weight and volume of the equipment will increase greatly and it will produce the tiresome ac noise [2], [4]. When the frequency is more than 150 kHz, it will be favorable to improve the function of the power converter, such as to lower the ripple, to shorten the responding time and to reduce the volume and weight, but it will also bring about some defects, such as to increase radio-frequency interference (RFI), to make a higher demand on the high frequency properties of the main power switches, high frequency inductors and capacitors. Especially, the switching loss will increase and the efficiency will be decreased obviously for large power application [2], [4]. All these will increase the difficulty and the cost to build this power factor corrector. Considering all of these factors, it is appropriate to choose a frequency from 20 kHz to 150 kHz for this boost converter. In this range, there is no tiring ac sound and the power factor corrector is good in volume, weight, ripple, instant responding speed and the cost to build it; it can satisfy the requirement of many equipments. In the end, the value of 100 kHz is chosen as the switching frequency of the main converter; the final experimental results prove it is proper. Certainly, with the improvement of the electrical cell element properties and the development of power electronic technology, the frequency of the active power factor corrector will be higher in the future.

2: The Choice of the Main Power Switch:

The IGBT is chosen as the main power switch for the boost converter. The IGBT is equivalent to the combination of a MOSFET and a PNP transistor. Please see Fig. 2.8. This makes it have advantages of MOSFETs and transistors. Transistors have low saturated voltage and high current density, but the transistor needs high driving current.
On the contrary, the driving power for the MOSFET is very little, its on-and-off speed is very fast, but its turn-on state voltage is high and its current density is low. These make IGBT have low driving power and low saturated voltage. At present, the voltage and current level of IGBT is nearly the same as those of transistors. It is suitable to act as main switches for large power, high frequency converters.

Fig. 2.8 Equivalent Circuit of IGBT

2.3 Determination of Several Component Values

Because the common working knowledge of the Boost converter is very simple, there is no need to explain the steady working process of this converter or to investigate its conduction mode in detail. It can work well both in continuous conduction mode and discontinuous conduction mode if the average current control method is used for the boost active power factor corrector. Here, only the theoretical calculation of several main components value will be discussed in detail because the input power for the boost converter is half sine wave voltage, not a constant DC voltage and this is the difference between boost APFC circuit and the common boost converter.

2.3.1 Calculation of Inductance in Main Circuit

The inductance determines the amount of high frequency current ripple in the input current. Its value is chosen to satisfy the limit for some specific current ripple [11]. In
order to calculate the main inductance, it should be clear that there are two frequency currents in the APFC circuit. The frequency of the reference current is the same as the input line frequency; the frequency of the regulated current is the high frequency decided by the control circuit, for this project, it is equal to 100 kHz. The principle to design the inductance is to make the maximum inductor current ripple satisfy its restraint. For this project, this restraint is: $\Delta i_L \leq 12.5\%i_L$. According to this principle, the required inductance value can be decided. From the knowledge of the boost converter, the inductor current ripple $\Delta i_L$ is:

$$\Delta i_L = \frac{1}{2} \Delta i_{LPP} = \frac{V_{\text{ind}}}{2L} DT_S$$

Here, $V_{\text{ind}}$ is the average value of the rectified input DC voltage; $T_S$ is the high frequency switching period [11], for this question, it is: $T_S = 10\mu s$.

For ideal situation, the average inductor current can be expressed as following:

$$I_L = \frac{I_o}{1-D} \approx \frac{V_o}{R_o} \times \frac{1}{1-D}$$

$V_o$: average value of output voltage; $I_o$: average value of output current.

Therefore, the following expression can be derived for this question:

$$\Delta \frac{i_L}{I_L} = \frac{V_{\text{ind}}}{2L} \times DT_S \times \frac{R_o}{V_o} \times (1 - D) = \frac{V_{\text{ind}}}{2L} \times DT_S \times \frac{R_o}{V_{\text{ind}}} \times (1 - D)^2$$

$$= \frac{DT_SR_o(1-D)^2}{2L} \leq 0.125$$

It is equivalent to the following relation:

$$L \geq 4R_oT_S(1 - D)^2$$

If the satisfactory value of the inductance is to be determined, the maximum value for $4R_oT_S(1 - D)^2$ must be known first. Because the values of $R_o$ and $T_S$ are constant, only the maximum value of $D(1 - D)^2$ need to be calculated. In order to be convenient, it is written as: $f(D) = D(1 - D)^2 = D^3 - 2D^2 + D$ (2-9)

By equating the derivative of $f(D)$ to be zero, the corresponding values of the duty cycle can be got as following: $D_1 = 1; D_2 = 1/3$
It is well known that the boost converter can not work at the condition of \( D=1 \), it will be enough to consider the situation of \( D=1/3 \). Because the second derivative of \( f(D) \) is:
\[
f(\dot{D}) = 6D - 4
\]
(2-10)

Its value at \( D=1/3 \) is equal to \( f(\frac{1}{3}) = -2 < 0 \), it can be concluded that the expression \( f(D) \) will reach its maximum value at \( D=1/3 \) and its maximum value is equal to: \( f(\frac{1}{3}) = 4/27 \)
(2-11)

Now, the inductance value can be calculated as following:
\[
L \geq 4 \times 150 \times \frac{4}{27} \times \frac{1}{100 \times 1000} \approx 0.89 \text{(mH)}
\]
(2-12)

Certainly, this is the approximate calculation. After simulation revision, in the end, the value of this inductance is taken as: \( L = 1 \text{mH} \).

Although the input voltage has different values at different time, it is still able to use the ideal case formula to calculate the inductance. This is because the input line frequency (50Hz or 60Hz) is much lower than the switching frequency of the converter (100kHz), the value of the input half sine wave DC voltage of the boost converter can be considered to remain nearly the same during one short switching period.

### 2.3.2 Calculation of Capacitance in Main Circuit

The factors involved in the decision of the output capacitance include the switching frequency current ripple, the second harmonic current ripple, the DC output voltage, the output voltage ripple and the hold-up time. The total current through the output capacitor is the RMS value of the switching frequency ripple current and the second harmonic of the current. The large electrolytic capacitors which are normally chosen for the output capacitor have an equivalent series resistance which changes with frequency and is generally high at low frequencies. The amount of current which the capacitor can handle is generally determined by the temperature rise. It is usually not necessary to calculate an exact value for the temperature rise. It is usually adequate to calculate the temperature
rise due to the high frequency ripple current and the low frequency ripple current and add them together. The capacitor data sheet will provide the necessary ESR and temperature rise information. The hold-up time of the output voltage often dominates any other consideration in output capacitor selection. Hold-up time is the length of time that the output voltage remains within a specified range after input power has been turned off. Hold-up time of 15 to 50 milliseconds is typical. In off-line power supplies with a 400Vdc output the hold-up requirement generally works out to between 1μF and 2μF per watt of output power. In this 1Kw project design, the output capacitance is 1000μF. If hold-up is not required, the capacitance will be much smaller, perhaps 0.2μF per watt, and then ripple current and ripple voltage are the major concern. The output voltage waveform of this Boost APFC circuit under European input power is as following:

![Fig. 2.9 Simulation Output Voltage of the Boost APFC](image)

\( V_o \): Output Voltage of the Boost APFC (Volts)

The input DC voltage for this boost converter is as following:

![Fig. 2.10 Simulation Input DC Voltage of the Boost Converter](image)

\( V_{ind} \): Rectified DC Input Voltage (Volts)
Hold-up time is a function of the amount of energy stored in the output capacitor, the load power, output voltage and the minimum voltage the load will operate at. This can be expressed in an equation to define the capacitance value in terms of the hold-up time.

\[
C_o = \frac{2 \times P_{out} \times \Delta t}{V_o^2 - V_{o(min)}^2}
\]  

(2-13)

Where \( C_o \) is the output capacitance, \( P_{out} \) is the load power, \( \Delta t \) is the hold-up time, \( V_o \) is the output voltage and \( V_{o(min)} \) is the minimum voltage the load will operate at [5]. For this project converter: \( P_{out} \) is 1kW, \( \Delta t \) is 34msec, \( V_o \) is 400V and \( V_{o(min)} \) is 300V, so, \( C_o \) is equal to 971\( \mu \)F. In the end, the output capacitance value is chosen as: \( C_o = 1000\mu \)F

2.3.3 Calculation of Current Sense Resistor

A peak value from 0.5 Volts to 1.0 Volts or so across the current sense resistor provides a signal large enough to have a good noise margin but which is small enough to have low power dissipation. There is a great deal of flexibility in choosing the value of the current sense resistor. For this project circuit, it can be found that the peak current through this resistor is equal to:

\[
I_{pk(max)} = I_{pk} + \frac{\Delta I}{2} = \frac{1.414 \times 1000}{200} + \frac{1.414 \times 1000 \times 0.125}{200} \approx 7.95(A)
\]  

(2-14)

\[
R_s = \frac{V_{rs}}{I_{pk(max)}} = \frac{1.0}{7.95} \approx 0.125(Ohms)
\]  

(2-15)

The value of 0.10 Ohm is chosen for this current sense resistor temporarily.

2.3.4 Calculation of Voltage Divider \( R_{VI} \) and \( R_{VD} \)

The criteria for the choice of the value of \( R_{VI} \) are reasonably vague. The value must be low enough so that the operational amplifier bias currents will not have a large effect on the output and it must be high enough so that the power dissipation is small. In this APFC converter, a 511 k\( \Omega \) resistor was chosen for \( R_{VI} \) and it will have power dissipation about 300mW.
The output voltage is set by the values of voltage divider $R_{Vl}$ and $R_{VD}$. The value of $R_{Vl}$ is already determined, so, the value of $R_{VD}$ can be determined from the desired output voltage and the reference voltage which is equal to 7.50Volts.

$$R_{VD} = \frac{R_{Vl} \cdot V_{ref}}{V_{o} - V_{ref}} = \frac{511 \times 7.5}{400 - 7.5} \approx 9.76 (k\Omega) \tag{2-16}$$

Finally, the value of $R_{VD}$ is chosen as 10k$\Omega$ and this will give an output voltage of 390Vdc. This could be trimmed up to 400Vdc with a 414k$\Omega$ resistor in parallel with $R_{VD}$, but for this application 390Vdc is acceptable. $R_{VD}$ has no effect on the AC performance of the active power factor corrector. Its only effect is to set the DC output voltage.

### 2.3.5 Calculation of Oscillator Components $R_{SET}$ and $C_T$

The PWM oscillator frequency in Figure 2.7 is equal to 100kHz. This value is determined by $C_T$ at pin14 and $R_{SET}$ at pin 12. $R_{SET}$ should be chosen first because it affects the maximum value of $I_{MULT}$ according to the equation:

$$I_{MULT_{max}} = \frac{-3.75V}{R_{SET}} \tag{2-17}$$

This effectively sets a maximum PWM-controlled current. With $R_{SET}$=10k$\Omega$,

$$I_{MULT_{max}} = \frac{-3.75}{10000} = -375 (\mu A) \tag{2-18}$$

Also note that the multiplier output current will never exceed twice of $I_{AC}$. With the 4k$\Omega$ resistor from the multiplier output to the 0.10 Ohm current sense resistor, the maximum current in the current sense resistor will be equal to:

$$I_{max} = \frac{-I_{MULT_{max}} \times 4000}{0.1} = -15 (A) \tag{2-19}$$

Having selected the value of $R_{SET}$, the current sense resistor, and the resistor from the multiplier output to the current sense resistor, we can calculate the value of $C_T$ for the desired PWM oscillator frequency from the following equation:

$$C_T = \frac{1.25}{R_{SET} \times f_S} = \frac{1.25}{10K \times 100K} = 1.25 (nF) \tag{2-20}$$
2.3.6 Several Important Control Inputs

1. $V_{SENSE}$ (Output DC voltage sense):

The threshold voltage for the $V_{SENSE}$ input is equal to 7.5Volts and the input bias current is typically equal to 50nA. The values shown in Figure 2.7 are for an output voltage of 400Volts. In this circuit, the voltage amplifier operates with a constant low frequency gain for minimum output excursions. The feedback capacitor with the value of 47nF places a 15Hz pole in the voltage loop that prevents the 120Hz ripple from propagating to the input current.

2. $I_{AC}$ (Line waveform):

In order to force the line current wave-shape to follow the line voltage, a sample of the power line voltage in waveform is introduced at pin 6. This signal is multiplied by the output of the voltage amplifier in the internal multiplier to generate a reference signal for the current control loop. This input is not a voltage, but a current (hence $I_{AC}$). It is set up by the 150kΩ and 520kΩ resistive divider (see Figure 2.7). The voltage at pin 6 is internally held at 6Volts. The two resistors are chosen so that the current flowing into pin 6 varies from zero (at each zero crossing) to about 600μA at the peak of the wave-shape.

The following formulae were used to calculate the values of these resistors:

$$R_{VAC} = \frac{V_{pk}}{I_{VACpk}} = \frac{1.414 \times 230}{600 \times 10^{-6}} \approx 542 (k\Omega) \quad (2-21)$$

Finally, the value of this resistor is chosen as 520kΩ

$$R_{B1} = \frac{R_{VAC}}{4} = \frac{542}{4} \approx 135 (k\Omega) \quad (2-22)$$

Finally, the value of this resistor is chosen as 150kΩ

($V_{pk}$ is the peak value of line voltage)

3. $I_{SENSE}$/Multiplier Output (Line current):

The voltage drop across the 0.10 Ohm current-sense resistor is applied to pins 4 and 5 as shown. The current-sense amplifier also operates with high low-frequency gain, but unlike the voltage amplifier, it is set up to give the current-control loop a very wide bandwidth. This enables the line current to follow the line voltage as closely as possible.
Chapter 2 Schematic Design of Boost Active Power Factor Corrector

In the present circuit, this amplifier has a zero at about 500Hz, and a gain of about 18dB thereafter.

2.3.7 Three Important Protection Inputs

1. ENA (Enable):
   
   The ENA input must reach 2.5Volts before the REF and GT Drv outputs are enabled. This provides a means to shut down the gate in case of trouble, or to add a time delay at power up. A hysteresis gap of 200mV is provided at this terminal to prevent erratic operation. Under-voltage protection is provided directly at pin15, where the on/off thresholds are 16Volts and 10Volts. If the ENA input is unused, it should be pulled up to VCC through a current limiting resistor of 22kΩ.

2. SS (Soft start):
   
   The voltage at pin 13 (SS) can reduce the reference voltage used by the error amplifier to regulate the output DC voltage. With pin 13 open, the reference voltage is typically equal to 7.5Volts. An internal current source delivers approximately -14μA from pin 13. Thus a capacitor connected between that pin and the ground will charge linearly from zero to 7.5Volts in 0.54C seconds, with C expressed in microfarads.

3. PKLIM (Peak Current Limit):
   
   Use pin 2 to establish the highest value of current to be controlled by the power switch. With the resistor divider values shown in Figure2.7, the 0.0V threshold at pin 2 is reached when the voltage drop across the 0.10Ohm current sense resistor is 7.5V*1.8k/10k=1.35Volts, corresponding to 13.5Amperes. A bypass capacitor from pin 2 to the ground is recommended to filter out very high frequency noise.

   The values of other components can be determined according to the manual of UC3854 and the requirement of this project by trial and error method with the help of PSIM software. The calculation of them will not be listed here.
Chapter 3

Hardware Implementation

Based on the theory discussed in chapter 2, a practical boost active power factor corrector will be built for experiment. In this chapter, emphasis will be given on how to choose components and put them together to form a prototype of boost active power factor corrector.

3.1 Choice of the Main Circuit Components

The practical boost active power factor corrector circuit is depicted in Error! Reference source not found.. It includes an AC-DC rectifier, a boost DC-DC converter, an analog control circuit built with UC3854 basic control chip and other accessory components. It works on popular AC-DC-DC topology. The process to choose appropriate components for main circuit and control circuit will be discussed in detail. At first, the part number of main circuit components will be determined in this section.

3.1.1 The Choice of Single Phase Full-wave Bridge Rectifier

The appropriate rectifier diode should be chosen according to its maximum reverse break voltage, average current through this diode, maximum current through this diode and its dissipation power. Therefore, these four parameters should be calculated at first and then determine the suitable bridge rectifier for this project.

1: The Maximum Reverse Break Voltage

Because this is a single phase full wave bridge rectifier, the maximum reverse break voltage applied to each diode of this rectifier is equal to the maximum phase line voltage. According to this knowledge, there is:

\[ V_{Dr_{max}} = V_g = 230\sqrt{2} = 325 \text{ (V)} \]  

(3-1)
Chapter 3 Hardware Implementation

UC3854 Controlled PFC Converter

Fig. 3.1 The Complete Boost APFC Circuit

Note: This circuit can be simulated by the full version only.
2: The Average Current through Diode

For the full bridge rectifier, the current through diode is equal to the input line current of the rectifier when the diode is “ON” and every pair of diodes will conduct during half cycle if the load is resistive. For ideal case, the output power of this power factor corrector is equal to the input power for this circuit. Because this is a power factor corrector, the input power factor is nearly equal to one for approximate calculation. According to this principle, there is:

\[ P_{in} = U_{rms}I_{rms} = P_{out} = \frac{V_0^2}{R_0} = \frac{400^2}{150} \approx 1066.67 \text{ (W)} \]  \hfill (3-2)

\[ I_{rms} = \frac{P_{out}}{U_{rms}} = \frac{1066.67}{200} \approx 5.33 (A) \]  \hfill (3-3)

\[ I_{max} = 5.33 \times \sqrt{2} \approx 7.5 (A) \]  \hfill (3-4)

Therefore, the average current through the diode is equal to:

\[ \langle i_{DA} \rangle = \frac{1}{T} \int_{0}^{T} i_{DA} dt = \frac{1}{T} \int_{0}^{T} 7.5 \sin \omega t dt = \frac{7.5}{\pi} \approx 2.39 (A) \]  \hfill (3-5)

3: The Maximum Current through the Diode

Obviously, the maximum current through the diode is equal to the maximum value of the input line current for the full wave bridge rectifier. Therefore, there is:

\[ I_{D_{max}} = 7.5 (A) \]  \hfill (3-6)

Please see Fig. 3.2 for the input current wave form to make a choice for the diode.

![Input current wave form](image)

**Fig. 3.2 The Simulation Wave Form of the Input Current \( I_{in} \)**

*\( I_{in} \): Input Line Current (Amperes)*
4: Dissipation Power

The dissipation is mainly produced when the diode is in "ON" state. Therefore, the dissipation power for each diode in the rectifier bridge is equal to:

\[ P_D = \frac{1}{T} \int_0^T V_D i_D dt = \frac{V_D}{T} \int_0^T i_D dt = V_D(i_D) = 0.7 \times 2.39 \approx 1.673 (W) \] (3-7)

Therefore, the total dissipation power of these four diodes in the input rectifier is approximately equal to four times of "\( P_D \)" for convenient calculation:

\[ P_{DA} = 4P_D = 6.7 (W) \] (3-8)

According to these four parameters, the part number of the input bridge rectifier for this circuit is chosen as: KBU8G; its parameters are in the following table:

<table>
<thead>
<tr>
<th>Maximum Recurrent Peak Voltage (V)</th>
<th>Forward Average Current (A)</th>
<th>Forward Rectified Voltage Drop (V)</th>
<th>Operating Temperature Range (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>400</td>
<td>8.0</td>
<td>1.1</td>
<td>-55 ~ 125</td>
</tr>
</tbody>
</table>

**Table 3.1 Full Bridge Rectifier Parameters**

3.1.2 Selection of Main Switch IGBT

In order to choose an appropriate IGBT module, three parameters should be known at first. They are peak voltage across IGBT, peak current through IGBT and RMS current through IGBT. These three parameters will be calculated in the following:

1: The Peak Voltage across IGBT

According to the common knowledge of the boost converter, the diode will conduct during the period of \([DT_s, T_s]\) in each switching cycle and the voltage across IGBT will be equal to the output voltage, therefore, this peak voltage is equal to the maximum output capacitor voltage. From Fig. 2.9, it can be seen that the maximum output capacitor voltage is approximately equal to 402 Volts.

\[ V_{QP} = V_{outmax} + \Delta V_C = 402 + \frac{V_{out}}{2R_C} DT_s = 402 + \frac{402 \times 0.9 \times 10^{-5}}{2 \times 150 \times 1000 \times 10^{-6}} \]

\[ \approx 402 (V) \] (3-9)
2: The Peak Current through IGBT

The main switch IGBT will conduct during the period of \([0, DT_S]\) in each switching cycle and the inductor current will be equal to the current through IGBT, so, the peak current through IGBT is equal to the maximum value of the inductor current. Although this value can be calculated approximately according to the common knowledge of the boost converter, it will be better to use the simulation results to determine this value so that a more accurate estimation can be made. Please see Fig. 3.3 for the inductor current wave form under full load condition. From this inductor current wave form, it can be seen that the peak current value through IGBT is equal to:

\[
I_{p} = I_{L} + \Delta I_{L} = \frac{I_{D}}{1-D} + \frac{V_{in}D}{2L}T_S \approx 7.5(A) \tag{3-10}
\]

![Fig. 3.3 Simulation Inductor Current Waveform](image-url)

\text{I}_{\text{ind}}: \text{Rectified Input DC Current (Amperes)}
3: RMS Current through IGBT

When the switching frequency is much higher than the ac line frequency, then the RMS value can be well-approximated as a double integral. The square of the current is integrated first to find its average over a switching period, and the result is then integrated to find the average over the ac line period.

\[ I_{L_{rms}} \approx \frac{V_o^2}{R_0} \times \frac{1}{230} = \frac{400 \times 400}{150 \times 230} = 4.64(A) \]  
(3-11)

\[ I_{Q_{rms}} \leq I_{L_{rms}} = 4.64(A) \]  
(3-12)

Certainly, the RMS current value of IGBT can be calculated as following:

\[ I_{Q_{rms}} = \frac{1}{\sqrt{T_{ac}}} \int_{0}^{T_{ac}} i_Q^2 dt = \frac{1}{\sqrt{T_{ac}}} \int_{0}^{T_{ac}} \frac{1}{T_s} \int_{t}^{t+T_s} i_Q^2(\tau) d\tau dt \]

\[ = I_{L_{rms}} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V_o}} \]

\[ = 4.64 \sqrt{1 - \frac{8}{3\pi} \frac{325}{400}} \approx 2.58(A) \]  
(3-13)

According to these values estimated above, the part number of IGBT for this project is chosen as: IRG4P30WPBF. Its parameters are listed in the following table. The WARP for this kind of IGBT is: 60kHz ~150kHz.

<table>
<thead>
<tr>
<th>(V_{CES} ) (V)</th>
<th>(V_{CE(ON)} ) (V)</th>
<th>(I_C \ (25^{\circ}C) ) (A)</th>
<th>(I_C \ (100^{\circ}C) ) (A)</th>
<th>(P_D ) (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>600</td>
<td>2.7</td>
<td>23</td>
<td>12</td>
<td>100</td>
</tr>
</tbody>
</table>

**Table 3.2 Parameters of IGBT**

3.1.3 The Choice of Diode in Boost Converter

At first, it should be known which kind of diode should be chosen for this boost converter. Generally speaking, for this kind of high frequency application, a fast recovery diode, an ultra-fast recovery diode or a Schottky diode should be used. In order to make an appropriate choice for this project, the reverse peak voltage across the diode, the average current through the diode and the RMS diode current should be known. In the following, these three parameters will be calculated at first and then the suitable diode for
this boost converter will be chosen.

1: The Reverse Peak Voltage across the Diode

According to common knowledge of the boost converter, the main switch will conduct during the period of \([0, DT_s]\) in each switching cycle and the diode will be in “OFF” state in this period of time, therefore, the reverse voltage across this diode is equal to the output voltage “\(V_{out}\)”. Certainly, the reverse peak diode voltage “\(V_{DP}\)” is equal to the maximum of the output voltage. According to this principle, there is:

\[
V_{DP} = V_{out} + \Delta V_{out} = V_{out} + \frac{V_{out}}{2R_0C} \times DT_s \cong 407(V)
\]  

(3-14)

2: The Average Current through the Diode

\[
I_{D_{avg}} = \frac{1}{T_s} \int_0^{T_s} i_D dt = \frac{1}{T_s} \left[ \int_0^{DT_s} i_D dt + \int_{DT_s}^{T_s} i_D dt \right]
\]

\[
= \frac{1}{T_s} \left[ \frac{(IL+\Delta IL)+(IL-\Delta IL)}{2} \right] \times (1 - D)T_s = IL \times (1 - D) = \frac{I_o}{1-D} \times (1 - D)
\]

\[
= I_o = \frac{V_o}{R_o} = \frac{400}{150} = 2.67(A)
\]  

(3-15)

3: The RMS Current Value through Diode

Because the duty cycle of the boost converter is less than “1.0” for steady state, the RMS current value through diode must be less than that of inductor current. From the expression (3-11), it can be seen that the RMS value of inductor current is equal to 4.64 Amperes. Therefore, there is:

\[
I_{D_{rms}} \leq 4.64(A)
\]  

(3-16)

With regard to the strict mathematical calculation, it is easy to do it in a similar way according to the definition of RMS. There is no need to calculate it again. According to simulation, its value is equal to:

\[
I_{D_{rms}} = 3.04(A)
\]  

(3-17)

4: The Loss on Diode due to Voltage Drop

Generally speaking, the voltage drop across a diode is about “0.7Volts” when the diode is “ON”. Therefore, the loss is approximately equal to:

\[
P_{D_{loss}} \cong 0.7 \times I_{D_{rms}} = 0.7 \times 3.04 = 2.128(W)
\]  

(3-18)
According to these calculated values and the requirement of this project, the ultra-fast high voltage rectifier (one diode) is used. Its part number is: STTH8L06. Please see Table 3.3 for its parameters.

<table>
<thead>
<tr>
<th>Reverse Peak Voltage (V)</th>
<th>Forward RMS Current (A)</th>
<th>Forward Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>600</td>
<td>8</td>
<td>1.05</td>
</tr>
</tbody>
</table>

Table 3.3 Parameters of the Main Circuit Diode

3.1.4 The Choice of the Output Capacitor

The principle to choose a capacitor is to make clear its peak voltage value and its RMS current value at first and then to choose a suitable capacitor with a margin of 15% ~ 20% calculated value. Here, these two parameters will be calculated in the following:

1: The Peak Voltage Value of the Output Capacitor

It is very important to make the peak voltage value of the capacitor less than its rated value, otherwise, the capacitor will break. In order to satisfy this requirement, its peak voltage value for every possible cases should be known and choose the worst one to act as a reference. Please see Fig. 3.4 for the output voltage wave form at one-third load situation.

![Fig. 3.4 The Simulation Output Voltage Wave Form at One-third Load](image-url)

$V_0$: Output Voltage of This APFC (Volts)

From this figure, it can be seen that the maximum output voltage value is about
407.2 Volts. Because the output voltage is equal to the capacitor voltage, the peak capacitor voltage value is equal to:

\[ V_{cp} = V_{op} \approx 407.2(V) \]  (3-19)

2: The RMS Current through the Capacitor

\[
I_{crms} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_c^2 \, dt} = \sqrt{\frac{1}{T_s} \left[ \int_0^{D T_s} \left( -\frac{V_o}{R_0} \right)^2 \, dt + \int_0^{T_s} \left( \frac{D}{1-D} \times \frac{V_o}{R_0} \right)^2 \, dt \right]}
\]

\[
= \left( \frac{V_o}{R_0} \right)^2 \times D + \frac{D^2 V_o^2}{(1-D) R_0^2}
\]  (3-20)

From this expression, it can be found that the duty cycle “D” should be known at first in order to calculate the RMS value of the current. The purpose to calculate RMS value is to estimate its dissipation; it is a total average effect for the capacitor. Therefore, the average input voltage value and the rated output voltage value of the boost converter should be used to get the average duty cycle for this converter under steady state. The average input voltage value of the converter is:

\[
\langle V_{id} \rangle = \frac{2}{\pi} \int_0^T V_m \sin \omega t \, dt = \frac{2}{\pi} V_m = \frac{2 \times 325}{\pi} = 207(V)
\]  (3-21)

\[ V_o = \frac{\langle V_{id} \rangle}{1-D} \]

\[
1 - D = \frac{\langle V_{id} \rangle}{V_o} = \frac{207}{398} \approx 0.52
\]  (3-22)

Therefore, the average duty cycle for this converter under steady state is equal to:

\[ D = 1 - 0.52 = 0.48 \]  (3-23)

In practice, it is well known that the conduction resistance \( R_{on} \) of IGBT, the winding resistance of the inductor, the conduction resistance of the diode and its conduction voltage drop will make the output voltage reduce. In order to make the output voltage equal to the rated value, the feedback control circuit will increase the duty cycle accordingly. Therefore, it will be a little more reasonable to calculate the RMS current value with “D = 0.5”. In this way, the RMS current value through the capacitor can be calculated as following:

\[
I_{crms} = \sqrt{\left( \frac{400}{150} \right)^2 \times 0.5 + \left( \frac{400}{150} \right)^2 \times 0.5} = \frac{400}{150} \approx 2.67(A)
\]  (3-25)
According to these two parameters, the part number of the output capacitor is chosen as: DCMC102T500BC2B; please see Table 3.4 for its parameters.

<table>
<thead>
<tr>
<th>Capacitance (μF)</th>
<th>Rate Voltage (V)</th>
<th>RMS Current (A)</th>
<th>ESR (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>500</td>
<td>4.1</td>
<td>138.7</td>
</tr>
</tbody>
</table>

Table 3.4 Parameters of the Output Capacitor

3.1.5 The Determination of Inductor

The determination of an inductor is to determine what kind of magnetic core and the suitable magnet wire should be used. After determination of the magnetic core and magnet wire, the required winding turns should be calculated approximately to get the required inductance. Generally speaking, there are two commonly used methods to design the inductor. They are AP method and KG method. Here, another method is used to design this inductor according to the instruction manual of MAGNETICS company.

1: The Determination of the Magnetic Core

From the introduction of their several magnetic cores, it can be seen that the MAGNETICS Kool Mu powder cores are distributed air gap cores made from a ferrous alloy powder for low losses at elevated frequencies. The near zero magneto-striction alloy makes Kool Mu ideal for eliminating audible frequency noise in filter inductors. In high frequency applications, core losses of powdered iron, for instance, can be a major factor in contributing to undesirable temperature rises. Hence, Kool Mu cores are ideal because their losses are significantly less, resulting in lower temperature rises. It is possible that Kool Mu cores will offer a reduction in core size over powdered iron cores in a similar application. All these make them ideally suited for switching regulator inductors, flyback transformers and power factor correction (PFC) inductors. Therefore, the Kool Mu core is chosen for this inductor. There are two kinds of powdered Kool Mu cores, torroids cores and E cores. The principle to choose the suitable core is simple and cheaper. If the power is not very big, the torroids cores should be considered at first. Therefore, the Kool Mu powdered cores are used for this application. In the following,
Chapter 3 Hardware Implementation

the appropriate core size number, the number of turns and the wire size for this inductor will be determined according to their manual step by step easily. For the detailed description of this procedure, please see them from: http://www.mag-inc.com. The core and wire will be determined in the following according to this procedure.

2: Calculation of “LI^2”

\[ L = \text{inductance required with dc bias (milli-Henrys); } I = \text{dc current (Amperes)} \]

Because the small signal average current through the inductor is approximately dc half sine wave with the magnitude of 7.5 Amperes, the low frequency (50Hz/60Hz) average value can be used to represent its dc current. Its average value is:

\[ \langle \overline{I} \rangle = \frac{2}{\pi} \int_0^{\pi/2} I_m \sin \omega t \, dt = \frac{15}{\pi} \equiv 4.78(A) \quad (3-26) \]

\[ LI^2 = 1.0 \times 4.78^2 \equiv 23 \text{ (mH - Amperes}^2) \quad (3-27) \]

3: Locate the LI^2 value on the Core Selector Chart.

Follow this coordinate to the intersection with the first core size that lies above the diagonal permeability line. (Small core sizes are at the bottom; large core sizes are at the top.) This is the smallest core size that can be used. From the Kool Mu Core Selector Chart, it can be seen that this coordinate passes through 60\u03bc section. Therefore, the core part number is: 77090; two stacked 77090 cores are used to make this inductor.

4: Determination of the Initial Number of Winding Turns

From the core data sheet, the nominal inductance for this core can be found as:

\[ AL = 86\text{mH/1000turns} \pm 8\% \]

Therefore, the minimum nominal inductance of this core is equal to:

\[ AL_{\text{min}} = 86 - 86 \times 8\% = 79.12\left(\frac{\text{mH}}{1000\text{turns}}\right) \quad (3-28) \]

The inductance for a given number of turns is related to the nominal inductance by following expression:

\[ L_n = \frac{L_{1000}N^2}{10^6} \quad (3-29) \]

Where: \( L_n \) = Inductance for N turns (mH)

\[ L_{1000} = \text{nominal inductance (mH/1000 turns)} \]
Therefore, the required winding turns to produce 1mH inductance can be calculated as following:

\[
1 = \frac{L_{1000N^2}}{10^6} = \frac{79.12N^2}{10^6}
\]

\[
N = \sqrt{\frac{10^6}{79.12}} \approx 112 \text{ (turns)} \tag{3-30}
\]

5: Calculation of Adjusted Number of Turns

In order to get the adjusted number of turns, the bias in oersteds should be calculated at first. From the data sheet, the magnetic path length can be seen as: \( l_e = 11.63 \text{ cm} \); According to the given expression, there is:

\[
H = \frac{0.4 \times \pi \times N I}{l_e} = 0.4 \times \pi \times 112 \times \frac{4.78}{11.63} \approx 58 \text{ (oersteds)} \tag{3-31}
\]

From the Permeability vs. DC Bias curves of this core, the roll-off in per unit of initial permeability (\( \mu_{pu} \)) can be determined as: 68%

Therefore, the number of adjusted turns is equal to:

\[
N_a = \frac{112}{0.68} \approx 165 \text{ (turns)} \tag{3-32}
\]

6: Choice of Wire Number

The appropriate wire can be determined according to the current capacity easily. Here, AWG 16 magnet wire is chosen for this inductor.

According to the relevant information about the inductor, it can be wound easily. Certainly, the winding turns perhaps need to be adjusted a little so that the inductance is equal to 1mH.

With regard to other components in main circuit, there is no need to explain how to determine them in detail.
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Fig. 3.5 Core Selector Chart
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Table 3.5 Data of Kool Mu Core 77090
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Table 3.6 Magnet Wire Table
3.2 The Basic Control Chip for This Circuit

3.2.1 Introduction of UC3854

Here, the basic control chip UC3854 is chosen to build the control circuit for this project. The APFC provides active power factor correction for power systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. This device implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion. To do this, the UC3854 contains a voltage amplifier, an analog multiplier/divider, a current amplifier, and a fixed-frequency PWM. In addition, the UC3854 contains a power MOSFET compatible gate driver, 7.5V reference, line anticipator, load-enable comparator, low-supply detector, and over-current comparator. The UC3854 uses average current-mode control to accomplish fixed frequency current control with stability and low distortion. Unlike peak current-mode control, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients. The UC3854 high reference voltage and high oscillator amplitude minimize noise sensitivity while fast PWM elements permit chopping frequencies above 200kHz. The UC3854 can be used in single and three phase systems with line voltages that vary from 75Volts to 275Volts and line frequencies across the 50Hz to 400Hz range. To reduce the burden on the circuitry that supplies power to this device, the UC3854 features low starting supply current. These devices are available packaged in 16-pin plastic and ceramic dual in-line packages, and a variety of surface-mount packages.

3.2.2 PIN DESCRIPTIONS of UC3854

In order to build an effective control circuit for this boost active power factor corrector with the basic control chip UC3854, its inner structure and the function of its pins should be known. In this way, the whole control circuit can be built according to its instruction and the whole project circuit requirement. In order to be convenient to
understand it easily, its structure diagram is listed as following:

**Fig. 3.6 Block Diagram of UC3854**

- **Gnd** (Pin 1) (ground): All voltages are measured with respect to Gnd. VCC and REF should be bypassed directly to Gnd with a 0.1\(\mu\)F or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing capacitor to Gnd should also be as short and as direct as possible.

- **PKLMT** (Pin 2) (peak limit): The threshold for PKLMT is 0.0V. Connect this input to the negative voltage on the current sense resistor as shown in Figure 3.1. Use a resistor to REF to offset the negative current sense signal up to Gnd.

- **CA Out** (Pin 3) (current amplifier output): This is the output of a wide-bandwidth op amp that senses line current and commands the pulse width modulator (PWM) to force the correct current. This output can swing close to Gnd, allowing the PWM to force zero duty cycle when necessary. The current amplifier will remain active even if the IC is disabled. The current amplifier output stage is an NPN emitter follower pull-up and an 8k resistor to ground.

- **ISENSE** (Pin 4) (current sense minus): This is the inverting input to the current amplifier. This input and the non-inverting input Mult Out remain functional down to and
below Gnd. Care should be taken to avoid taking these inputs below −0.5V, because they are protected with diodes to Gnd.

**Mult Out** (Pin 5) (multiplier output and current sense plus): The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at Mult Out. The cautions about taking ISENSE below −0.5V also apply to Mult Out. As the multiplier output is a current, this is a high impedance input similar to ISENSE, so the current amplifier can be configured as a differential amplifier to reject Gnd noise.

**IAC** (Pin 6) (input AC current): This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (IAC) to Mult Out, so, this is the only multiplier input that should be used for sensing instantaneous line voltage. The nominal voltage on IAC is 6V, so in addition to a resistor from IAC to rectified voltage, connect a resistor from IAC to REF. If the resistor to REF is one fourth of the value of the resistor to the rectifier, then the 6V offset will be cancelled, and the line current will have minimal cross-over distortion.

**VA Out** (Pin 7) (voltage amplifier output): This is the output of the op amp that regulates output voltage. Like the current amplifier, the voltage amplifier will stay active even if the IC is disabled with either ENA or VCC. This means that large feedback capacitors across the amplifier will stay charged through momentary disable cycles. Voltage amplifier output levels below 1V will inhibit multiplier output. The voltage amplifier output is internally limited to approximately 5.8V to prevent overshoot. The voltage amplifier output stage is an NPN emitter follower pull-up and an 8k resistor to ground.

**VRMS** (Pin 8) (RMS line voltage): The output of a boost PWM is proportional to the input voltage, so when the line voltage into a low-bandwidth boost PWM voltage regulator changes, the output will change immediately and slowly recover to the regulated level. For these devices, the VRMS input compensates for line voltage changes
if it is connected to a voltage proportional to the RMS input line voltage. For best control, the VRMS voltage should stay between 1.5V and 3.5V.

**REF** (Pin 9) (voltage reference output): REF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. REF is disabled and will remain at 0V when VCC is low or when ENA is low. Bypass REF to Gnd with a 0.1μF or larger ceramic capacitor for best stability.

**ENA** (Pin 10) (enable): ENA is a logic input that will enable the PWM output, voltage reference, and oscillator. ENA also will release the soft start clamp, allowing SS to rise. When unused, connect ENA to a +5V supply or pull ENA high with a 22k resistor. The ENA pin is not intended to be used as a high speed shutdown to the PWM output.

**VSENSE** (Pin 11) (voltage amplifier inverting input): This is normally connected to a feedback network and to the boost converter output through a divider network.

**RSET** (Pin 12) (oscillator charging current and multiplier limit set): A resistor from RSET to ground will program oscillator charging current and maximum multiplier output. Multiplier output current will not exceed 3.75V divided by the resistor from RSET to ground.

**SS** (Pin 13) (soft start): SS will remain at Gnd as long as the IC is disabled or VCC is too low. SS will pull up to over 8V by an internal 14μA current source when both VCC becomes valid and the IC is enabled. SS will act as the reference input to the voltage amplifier if SS is below REF. With a large capacitor from SS to Gnd, the reference to the voltage regulating amplifier will rise slowly, and increase the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS will quickly discharge to ground and disable the PWM.

**CT** (Pin 14) (oscillator timing capacitor): A capacitor from CT to Gnd will set the PWM oscillator frequency according to this relationship: \( F = \frac{1.25}{RSET \cdot CT} \)

**VCC** (Pin 15) (positive supply voltage): Connect VCC to a stable source of at least 20mA above 17V for normal operation. Also bypass VCC directly to Gnd to absorb
supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate GT Drv signals, these devices will be inhibited unless VCC exceeds the upper under-voltage lockout threshold and remains above the lower threshold.

**GT Drv** (Pin 16) (gate drive): The output of the PWM is a totem pole MOSFET gate driver on GT Drv. This output is internally clamped to 15V so that the IC can be operated with VCC as high as 35V. Use a series gate resistor of at least 5 ohms to prevent interaction between the gate impedance and the GT Drv output driver that might cause the GT Drv output to overshoot excessively. Some overshoot of the GT Drv output is always expected when driving a capacitive load.

### 3.3 IGBT Gate Driver for This Circuit

Insulated gate bipolar transistors (IGBTs) are gaining considerable use in circuits requiring high voltage and current at moderate switching frequencies. Much of the popularity of IGBT stems from its simple MOSFET-like gate drive requirement. IGBT gate drive requirements can be divided into two basic application categories: Those that do not apply high dv/dt to the collector/emitter of the IGBT when it is off, and those that do [14], [15]. Examples of the former are boost regulators and forward converters, where only one switch is employed or multiple switches are activated synchronously. High dv/dt is applied during the off-state in most bridge circuits such as inverters and motor controllers, when opposing devices are turned on. Simultaneous conduction of opposing devices can occur in such circuits, often with catastrophic results if proper gate drive and layout precautions are not followed. This behaviour is caused by parasitic collector to gate (Miller) capacitance, effectively forming a capacitive divider with the gate to emitter capacitance and thus inducing a gate to emitter voltage as illustrated in Fig. 3.7.
When high off-state dv/dt is not present, the IGBT can be driven like a MOSFET using any of the gate drive circuits in the UC37XX family as well as from the drivers internal to many switching power supply controllers. Normally fifteen volts is applied from gate to emitter during the on-state to minimize saturation voltage. The gate resistor or gate drive current directly controls IGBT turn-on; however turn-off is partially governed by minority carrier behaviour and is less affected by gate drive. Therefore, the internal gate drive in UC3854 and a gate resistor $R_g$ (150Ω) are used to drive IGBT directly in this project circuit.
Chapter 4

Project Simulation

The schematic circuit and the hardware implementation for this project have been described in chapter 2 and chapter 3. The next step for the engineering design is to make the whole project simulation and revise the original circuit until the project specifications can be satisfied. Here, the PSIM 6.0 is used to simulate this whole project circuit for all possible situations. After the simulation and revision, the satisfactory results are gained. Here, it can be seen that this APFC circuit can work very well under the European input line power (230V/50Hz/60Hz) and the Asian line power (220V/50Hz/60Hz). The reason to take these two standards into account for this project design is mainly to enlarge its application area and make this APFC circuit more useful. In the end, another two simulations for input line powers of 200V/50Hz/60Hz and 240V/50Hz/60Hz will be listed respectively.

4.1 The Simulation for 230V/50Hz Input Power

Three different situations will be simulated under this input power. They are full load \((R_0=150\Omega)\), half load \((R_0=300\Omega)\) and one-third load \((R_0=450\Omega)\) because the active power factor corrector must be able to work satisfactorily when the load changes. This wide load scope will be able to satisfy the practical engineering requirement. You will find that the no load situation is not taken into account for the project simulation here. The reason is that the input power will be equal to zero theoretically when the output power is equal to zero. Therefore, it will have very little influence on the input power and other neighboring equipments. Besides this, it can be found that the current feedback branch will be broken when the output current is equal to zero, so, it can be concluded that this circuit can not realize the APFC function for the no load situation. Certainly, the
output current is not equal to zero for practical engineering problem, but it is very little and can be neglected.

4.1.1 The Simulation Circuit

**UC3854 Controlled PFC Converter**

![Simulation Circuit Diagram](image)

*Note: This circuit can be simulated by the full version only.*

**Fig. 4.1 Simulation Circuit for 230V/50Hz/60Hz**
4.1.2 Simulations

1: The waveform at full load situation (R=150 Ohms/f=50Hz):

![Waveform Diagram]

Fig. 4.2 Simulation of $V_{\text{in}}$ and $I_{\text{in}}$ for Full Load Situation

$V_{\text{in}}$: Input Line Voltage (Volts)

$I_{\text{in}}$: Input Line Current (Amperes)
**Fig. 4.2[A] Simulation of \( V_0 \) and \( I_{\text{ind}} \) for Full Load Situation**

\( I_{\text{ind}} \): Rectified DC Current (Amperes)

\( V_0 \): APFC Output Voltage (Volts)

For ideal case, the input power is equal to output power, there is:

\[
P_{\text{in}} = P_{\text{out}} = \frac{V_0^2}{R_o} \approx \frac{398 \times 398}{150} = 1056 \text{ (W)} \tag{4-1}
\]

\[
PF = \frac{P_{\text{in}}}{V_{\text{rms}} \times I_{\text{rms}}} = \frac{1056}{230 \times 4.597} \approx 0.998 \tag{4-2}
\]
2: The wave forms at half load (R=300 Ohms/f=50Hz):

**Fig. 4.3 Simulation of $I_{in}$ and $V_{in}$ for Half Load Situation**

$V_{in}$: Input Line Voltage (Volts)

$I_{in}$: Input Line Current (Amperes)
Fig. 4.3[A] Simulation of $I_{\text{ind}}$ and $V_o$ for Half Load Situation

$I_{\text{ind}}$: Rectified DC Current (Amperes)

$V_o$: APFC Output Voltage (Volts)
3: The waveform at one third load situation (R=450 Ohms, f=50Hz):

Fig. 4.4 Simulation of I_in and V_in for One Third Load

V_in: Input Line Voltage (Volts)
I_in: Input Line Current (Amperes)
From these simulations listed above, it can be seen that this Boost APFC circuit can satisfy the requirement under the required load scope. This suggests that it is a feasible design for this project and it can improve the power factor nearly equal to unity and reduce the harmonic distortion greatly.
4.2 The Simulation for 230V/60Hz Input Power

In order to verify that this Boost APFC circuit can work well when the input line frequency is 60Hz, the simulation for this situation is made. It is meaningful to do so because the line frequency for North American Standard is 60Hz; this project design will be more applicable if it can satisfy the specifications under this situation. The simulations are as following:

1: The waveform at full load situation (R=150 Ohms/ f=60Hz):

![Waveform Diagram]

---

**Fig. 4.5 Full Load Simulation of V\textsubscript{in} and I\textsubscript{in} (f=60Hz)**

- **V\textsubscript{in}:** Input Line Voltage (Volts)
- **I\textsubscript{in}:** Input Line Current (Amperes)
Fig. 4.5[A] Full Load Simulation of $I_{\text{ind}}$ and $V_0$ (f=60Hz)

$I_{\text{ind}}$: Rectified DC Current (Amperes)

$V_0$: APFC Output Voltage (Volts)

It can be found the power factor for 60Hz is nearly the same as that for 50Hz.
2: The waveform at half load situation (R=300 Ohms/ f=60Hz):

Fig. 4.6 Half Load Simulation of $I_{in}$ and $V_{in}$ (f=60Hz)

$V_{in}$: Input Line Voltage (Volts)

$I_{in}$: Input Line Current (Amperes)
Fig. 4.6[A] Half Load Simulation of I_{ind} and V_o (f=60Hz)

I_{ind}: Rectified DC Current (Amperes)

V_o: APFC Output Voltage (Volts)
3: The waveform at one-third load situation (R=450 Ohms/f=60Hz):

![Waveform Diagram]

**Fig. 4.7 One-third Load Simulation of $I_{in}$ and $V_{in}$ (f=60Hz)**

$V_{in}$: Input Line Voltage (Volts)

$I_{in}$: Input Line Current (Amperes)
From the simulations listed above when input line frequency is equal to 60Hz, it can be found that the Boost APFC circuit still works well and the power factor is nearly equal to unity.
4.3 The Simulation for 220V/50Hz Input Power

In order to verify that this Boost APFC circuit can be used for Asian Standard (220V/50Hz) input line power, the simulations for this situation are made under three cases: full load, half load and one-third load. The simulation wave forms are listed in the following. It can be found that this project design can work very well for the Asian Standard input power, too. Therefore, this project design is a very useful circuit. This will be very important for a commercial project design because many large companies are international companies at present and they probably have branch companies in Europe, North America or Asian countries. If this characteristic can be taken into account and make the design satisfy this requirement, it will be very helpful to promote the commercial market for the project design.

1: The waveform at full load situation (R=150 Ohms/ f=50Hz):

Fig. 4.8 Full Load Simulation of \( I_{in} \) and \( V_{in} \) (220V/50Hz)

\( V_{in} \): Input Line Voltage (Volts)

\( I_{in} \): Input Line Current (Amperes)
For the ideal case, input power is equal to output power, there is:

\[
P_{in} = P_{out} = \frac{V_0^2}{R_o} = \frac{398 \times 398}{150} \approx 1056 \text{ (W)} \tag{4-3}
\]

\[
P_F = \frac{P_{in}}{V_{rms} \times I_{rms}} = \frac{1056}{220 \times 4.835} \approx 0.993 \tag{4-4}
\]

\(I_{ind}\): Rectified DC Current (Amperes)

\(V_o\): APFC Output Voltage (Volts)

**Fig. 4.8[A] Full Load Simulation of \(I_{in}, I_{ind}\) and \(V_o\) (220V/50Hz)**
2: The waveform at half load situation (R=300 Ohms/ f=50Hz):

Fig. 4.9 Half Load Simulation of $I_{in}$ and $V_{in}$ (220V/50Hz)

$V_{in}$: Input Line Voltage (Volts)

$I_{in}$: Input Line Current (Amperes)
Fig. 4.9[A] Half Load Simulation of $I_{in}$, $I_{ind}$ and $V_o$ (220V/50Hz)

$I_{ind}$: Rectified DC Current (Amperes)

$V_o$: APFC Output Voltage (Volts)
3: The waveform at one-third load situation (\(R=450 \text{ Ohms/}\ f=50\text{Hz}\)):

![Waveform Diagram]

**Fig. 4.10 One-third Load Simulation of \(I_{in}\) and \(V_{in}\) (220V/50Hz)**

\(V_{in}\): Input Line Voltage (Volts)

\(I_{in}\): Input Line Current (Amperes)
Fig. 4.10[A] One-third Load Simulation of $V_o$, $I_{in}$ and $I_{ind}$ (220V/50Hz)

$I_{ind}$: Rectified DC Current (Amperes)

$V_o$: APFC Output Voltage (Volts)

From these simulation waveforms, it can be seen clearly that the performance of this active power factor corrector can work excellently for Asian Standard input power and the input power factor is nearly equal to one for three cases.
4.4 The Simulation for 220V/60Hz Input Power

In order to check whether this circuit can work with 60Hz line frequency input power or not, the simulation for this kind of input power is made. It will be meaningful for North American countries if it can work well too. Simulations for three cases (Full load, half load and one-third load) are made to verify that it can work satisfactorily.

1: The waveform at full load situation (R=150 Ohms/ f=60Hz):

![Waveform Image](image)

Fig. 4.11 Full Load Simulation of $I_{in}$ and $V_{in}$ (220V/60Hz)

$V_{in}$: Input Line Voltage (Volts)

$I_{in}$: Input Line Current (Amperes)
Fig. 4.11[A] Full Load Simulation of $I_{in}$, $I_{ind}$ and $V_o$ (220V/60Hz)

$I_{ind}$: Rectified DC Current (Amperes)

$V_o$: APFC Output Voltage (Volts)

It can be found that the power factor for 60Hz is nearly the same as that for 50Hz.
Chapter 4 Project Simulation

2: The waveform at half load situation (R=300 Ohms/ f=60Hz):

Fig. 4.12 Half Load Simulation of $I_{in}$ and $V_{in}$ (220V/60Hz)

$V_{in}$: Input Line Voltage (Volts)

$I_{in}$: Input Line Current (Amperes)
Fig. 4.12[A] Half Load Simulation of $I_{\text{ind}}$, $V_o$ (220V/60Hz)

$I_{\text{ind}}$: Rectified DC Current (Amperes)

$V_o$: APFC Output Voltage (Volts)
3: The waveform at one-third load situation (R=450 Ohms/ f=60Hz):

![Waveform Diagram]

**Fig. 4.13 One-third Load Simulation of I\textsubscript{in} and V\textsubscript{in} (220V/60Hz)**

\(V_{in}\): Input Line Voltage (Volts)

\(I_{in}\): Input Line Current (Amperes)
Fig. 4.13[A] One-third Load Simulation of $I_{in}$, $I_{ind}$ and $V_o$ (220V/60Hz)

$I_{ind}$: Rectified DC Current (Amperes)

$V_o$: APFC Output Voltage (Volts)

From these three simulation waveforms, it can be found that this circuit can be used directly in this situation. Certainly, it is meaningful to check that this project circuit can work well when the input power is 220V/50Hz/60Hz only for use in one region. This is because the input line voltage often has an error and fluctuations, too.
4.5 The Simulation for 200V/60Hz Input Power

Here, the performance of this active power factor corrector for this situation will be checked. At first, the simulation for input line frequency of 60Hz will be made. The corresponding wave forms are listed as following.

1. The wave form under full load situation (R=150Ohms/f =60Hz)

![Waveform diagrams showing V_in, I_in, and V_o for full load simulation.]

**Fig. 4.14 Full Load Simulation of V_in, I_in and V_o (200V/60Hz)**

- **V_in**: Input Line Voltage (Volts)
- **I_in**: Input Line Current (Amperes)
- **V_o**: APFC Output Voltage (Volts)
Fig. 4.14[A] Full Load Simulation of $I_{\text{ind}}$ and $V_d$ (200V/60Hz)

$I_{\text{ind}}$: Rectified DC Current (Amperes)

$V_d$: Rectified DC Voltage (Volts)
2. The wave form for half load situation (R=300Ohms/f =60Hz)

Fig. 4.15 Half Load Simulation of $V_{in}$ and $I_{in}$ (200V/60Hz)

$V_{in}$: Input Line Voltage (Volts)

$I_{in}$: Input Line Current (Amperes)
Fig. 4.15[A] Half Load Simulation $V_o$, $I_{ind}$ and $V_d$ (200V/60Hz)

$I_{ind}$: Rectified DC Current (Amperes)
$V_d$: Rectified DC Voltage (Volts)
$V_o$: APFC Output Voltage (Volts)
3. The wave form for one-third load situation (R=450Ωms/f =60Hz)

![Waveform Diagram]

**Fig. 4.16 One-third Load Simulation of V\textsubscript{in} and I\textsubscript{in} (200V/60Hz)**

**V\textsubscript{in}:** Input Line Voltage (Volts)

**I\textsubscript{in}:** Input Line Current (Amperes)
Fig. 4.16[A] One-third Load Simulation of $V_o$, $I_{ind}$ and $V_d$ (200V/60Hz)

$I_{ind}$: Rectified DC Current (Amperes)

$V_d$: Rectified DC Voltage (Volts)

$V_o$: APFC Output Voltage (Volts)
4.6 The Simulation for 200V/50Hz Input Power

In this section, the performance of this Boost APFC under 50Hz input line frequency will be checked. It is useful to do this because it is possible for this circuit to work under this input power situation. The simulations are listed in the following.

1. The wave form under full load situation (R=150Ohms/f =50Hz)

![Waveform Diagram]

**Fig. 4.17 Full Load Simulation of V_in and I_in (200V/50Hz)**

\(V_{in}\): Input Line Voltage (Volts)

\(I_{in}\): Input Line Current (Amperes)
Fig. 4.17[A] Full Load Simulation of $I_{\text{ind}}$, $V_d$ and $V_o$ (200V/50Hz)

$I_{\text{ind}}$: Rectified DC Current (Amperes)

$V_d$: Rectified DC Voltage (Volts)

$V_o$: APFC Output Voltage (Volts)
2. The wave form under half load situation (R=300Ohms/\( f =50\text{Hz} \))

![Graph of V_in and I_in](image)

**Fig. 4.18 Half Load Simulation of V_in and I_in (200V/50Hz)**

\( V_{in} \): Input Line Voltage (Volts)

\( I_{in} \): Input Line Current (Amperes)
Fig. 4.18[A] Half Load Simulation of $I_{ind}$, $V_d$ and $V_o$ (200V/50Hz)

$I_{ind}$: Rectified DC Current (Amperes)

$V_d$: Rectified DC Voltage (Volts)

$V_o$: APFC Output Voltage (Volts)
3. The wave form under one-third load situation (R=450Ohms/f =50Hz)

Fig. 4.19 One-third Load Simulation of $V_{in}$ and $I_{in}$ (200V/50Hz)

$V_{in}$: Input Line Voltage (Volts)

$I_{in}$: Input Line Current (Amperes)
Fig. 4.19[A] One-third Load Simulation of $V_o$, $I_{ind}$ and $V_d$ (200V/50Hz)

$I_{ind}$: Rectified DC Current (Amperes)

$V_d$: Rectified DC Voltage (Volts)

$V_o$: APFC Output Voltage (Volts)
4.7 The Simulation for 240V/60Hz Input Power

The practical input line power often fluctuates to some extent and makes the voltage more or less than the rated voltage. In order to ensure this Boost APFC circuit work normally for the rated 230V/50Hz/60Hz input line power, its performance under the input line power of 240V/50Hz/60Hz should be simulated accordingly. The simulation wave forms are listed as following.

1. The wave form under full load situation (R=150Ohms/f =60Hz)

![Waveform Diagram]

**Fig. 4.20 Full Load Simulation of V_{in} and I_{in} (240V/60Hz)**

- **V_{in}:** Input Line Voltage (Volts)
- **I_{in}:** Input Line Current (Amperes)
Fig. 4.20[A] Full Load Simulation of $V_0$, $I_{ind}$ and $V_d$ (240V/60Hz)

$I_{ind}$: Rectified DC Current (Amperes)

$V_d$: Rectified DC Voltage (Volts)

$V_o$: APFC Output Voltage (Volts)
2. The waveform under half load situation (R=300Ohms/f =60Hz)

Fig. 4.21 Half Load Simulation of $V_{in}$ and $I_{in}$ (240V/60Hz)

$V_{in}$: Input Line Voltage (Volts)

$I_{in}$: Input Line Current (Amperes)
Fig. 4.21[A] Half Load Simulation of $V_o$, $I_{\text{ind}}$ and $V_d$ (240V/60Hz)

$I_{\text{ind}}$: Rectified DC Current (Amperes)

$V_d$: Rectified DC Voltage (Volts)

$V_o$: APFC Output Voltage (Volts)
3. The wave form under one-third load situation (R=450 Ohms/f =60 Hz)

![Waveform Diagram](image)

Fig. 4.22 One-third Load Simulation of $V_{in}$ and $I_{in}$ (240V/60Hz)

$V_{in}$: Input Line Voltage (Volts)

$I_{in}$: Input Line Current (Amperes)
Fig. 4.22[A] One-third Load Simulation of $V_o$, $I_{ind}$ and $V_d$ (240V/60Hz)

$I_{ind}$: Rectified DC Current (Amperes)

$V_d$: Rectified DC Voltage (Volts)

$V_o$: APFC Output Voltage (Volts)
4.8 The Simulation for 240V/50Hz Input Power

For the same reason as before, the performance of this project circuit under the 240V/50Hz input power will be simulated to check whether it can still work well or not. The simulation waveforms under this situation are listed as following.

1. The waveform under full load situation (R=150Ohms/f= 50Hz)

![Waveform Image]

Fig. 4.23 Full Load Simulation of $V_{in}$ and $I_{in}$ (240V/50Hz)

$V_{in}$: Input Line Voltage (Volts)

$I_{in}$: Input Line Current (Amperes)
Fig. 4.23[A] Full Load Simulation of $V_o$, $I_{\text{ind}}$ and $V_d$ (240V/50Hz)

$I_{\text{ind}}$: Rectified DC Current (Amperes)

$V_d$: Rectified DC Voltage (Volts)

$V_o$: APFC Output Voltage (Volts)
2. The wave form under half load situation (R=300Ohms/f= 50Hz)

\[ V_{in}, I_{in} \]

\[ V_{in}: \text{Input Line Voltage (Volts)} \]

\[ I_{in}: \text{Input Line Current (Amperes)} \]
Fig. 4.24[A] Half Load Simulation of $V_o$, $I_{ind}$ and $V_d$ (240V/50Hz)

$I_{ind}$: Rectified DC Current (Amperes)

$V_d$: Rectified DC Voltage (Volts)

$V_o$: APFC Output Voltage (Volts)
3. The wave form under one-third load situation (R=450 Ohms/ f = 50Hz)

![Graph of wave forms]

**Fig. 4.25 One-third Load Simulation of V\textsubscript{in} and I\textsubscript{in} (240V/50Hz)**

- **V\textsubscript{in}**: Input Line Voltage (Volts)
- **I\textsubscript{in}**: Input Line Current (Amperes)
Fig. 4.25[A] One-third Load Simulation $V_0$, $I_{\text{ind}}$, and $V_d$ (240V/50Hz)

$I_{\text{ind}}$: Rectified DC Current (Amperes)

$V_d$: Rectified DC Voltage (Volts)

$V_0$: APFC Output Voltage (Volts)
In the end, the definition of these wave names will be listed again in the following so that it is convenient for others to check.

\[V_{in}: \text{Input Line Voltage (Volts)}\]
\[I_{in}: \text{Input Line Current (Amperes)}\]
\[I_{nd}: \text{Rectified DC Current (Amperes)}\]
\[V_{o}: \text{APFC Output Voltage (Volts)}\]
\[V_{d}: \text{Rectified Half Sine Wave DC Voltage (Volts)}\]

All these results listed above suggest that this design is feasible and this circuit can work satisfactorily under the input line voltage range from 200Vrms to 230Vrms with line frequency of 60Hz or 50Hz. Next, experiments will be made to verify its performance and revise this project circuit further.
Chapter 5

Experimental Results

After the schematic design for this boost active power factor corrector in chapter 2 and careful revision for it by simulation in chapter 4, the final simulations under all cases are satisfactory. However, this does not imply that the project circuit is feasible and this project design is finished. If a final reasonable Boost APFC circuit is to be got, practical experiments must be made to verify the performance of this schematic circuit and revise it. The hardware implementation of this project is explained and all components for the whole circuit are chosen in chapter 3. The next step is to do experiments and adjust some component values so that the desired results can be got and finish this project design in the end. Due to the line frequency in our lab is 60Hz, I will make the project experiments for 60Hz only. Certainly, we can get the line frequency of 50Hz by electrical generator at first and make the 50Hz experiment to check the performance of the Boost APFC circuit. The simulations in chapter 4 suggest that this circuit performs well for 50Hz line frequency input power if it can work well for 60Hz line frequency because the difference between these two frequency values is small. Therefore, it will be enough to make this APFC circuit satisfy the project requirement for line frequency of 60Hz. It can be found this is another advantage for project simulation.

5.1 The Experimental Results for Current Sensing Resistor $R_s$ of 0.1 Ohm and IGBT Gate Driving Resistor $R_g$ of 150 Ohms

The practical experiments are made to check whether the input voltage range and the load range of this designed project circuit can satisfy the requirement of the power factor corrector or not. The corresponding experimental results are as following.
1. The experimental results for full load situation ($R=150\Omega$, $f=60\text{Hz}$, $V=70\text{V}_{\text{rms}}$)

**Fig. 5.1 Full Load Experimental Results of $V_{\text{in}}$ and $I_{\text{in}}$ ($70\text{V}_{\text{rms}}/60\text{Hz}$)**

- **$V_{\text{in}}$ (C1 Signal): Input Line Voltage (Volts)**
- **$I_{\text{in}}$ (C2 Signal): Input Line Current (Amperes)**

Here, the signal for $C_1$ channel is input line voltage and the signal for $C_2$ channel is input AC current. Another resistor ($0.1\Omega$) is used to measure the input current. It can be found that the input current wave is a sinusoidal wave and it tracks the input voltage wave form very well. This suggests that the input power factor will be nearly equal to unity. The disadvantage is that the input current includes harmonics. Measures should be taken to reduce it. This will be explained later.
2. The experimental results for full load situation \( (R=150\Omega/f =60Hz/V_i=147V_{\text{rms}}) \)

![Graph showing experimental results](image)

**Fig. 5.2 Full Load Experimental Results (147V_{\text{rms}}/60Hz)**

\( V_{in} \) (C1 Signal): Input Line Voltage (Volts)

\( I_{in} \) (C2 Signal): Input Line Current (Amperes)

\( V_o \) (C3 Signal): APFC Output Voltage (Volts)
Here, the signal for C1 channel is input line voltage; the signal for C2 channel is input current and it is measured with a resistor (0.1Ω); the signal for C3 channel is the output voltage for this active power factor corrector and it is measured with a voltage divider formed with two resistors (510kΩ and 10kΩ). From these wave forms, it can be found that the input current can track the input voltage waveform and remain sinusoidal but with obvious harmonics. Certainly, high frequency switching current will produce harmonics, but the valid methods must be found to reduce it. Another characteristic for these waveforms is that the output voltage is not equal to 400 Volts. It can be found it is approximately equal to:

\[ V_o \approx 2 \times 2.2 \times \frac{520}{10} = 229(V) \]  
\[ I_{inmax} \approx \frac{0.2}{0.1} \times 1.8 = 3.6(A) \]
\[ P_o = \frac{V_o^2}{R_o} = \frac{229 \times 229}{150} \approx 349.6(W) \]
\[ P_{in} = \frac{V_{inrms} \times I_{inmax}}{1.414} = \frac{147 \times 3.6}{1.414} \approx 374.2(W) \]
\[ \eta = \frac{P_o}{P_{in}} = \frac{349.6}{374.2} \approx 93.4\% \]

It can be found that the efficiency for this APFC circuit under this situation is acceptable and this suggests that the input power factor is good. However, it can be found that the output power is less than 1kW and the maximum input voltage for this circuit to work normally is equal to rms160 Volts. What is the reason for this unsatisfactory characteristic? How to solve this problem? This will be discussed in detail later.

3. The experimental results under three-quarters load situation (R=200Ω/f=60Hz/Vi=75Vrms/Vo=150Vrms)

After several experimental trial, it can be seen that the load range for this circuit to work normally under this situation (Rs=0.1Ω/Rg=150Ω) is full load (R=150Ω) to three quarters load (R=200Ω) and the input voltage range nearly remains the same. The output voltage nearly remains the same as before. The corresponding wave forms will be listed as following:
Fig. 5.3 Three-quarters Load Experimental Results (75V\textsubscript{rms}/60Hz)

\( V_{in} \) (C1 Signal): Input Line Voltage (Volts)

\( I_{in} \) (C2 Signal): Input Line Current (Amperes)

\( V_o \) (C3 Signal): APFC Output Voltage (Volts)
Fig. 5.3[A] Three-quarters Load Experimental Results (150V rm/60Hz)

V_{in} (C1 Signal): Input Line Voltage (Volts)

I_{in} (C2 Signal): Input Line Current (Amperes)

V_{o} (C3 Signal): APFC Output Voltage (Volts)
It can be seen that the phenomenon is the same as before. The input current tracks input voltage very well with sinusoidal waveform, but it has obvious harmonics.

From this experimental wave form, it can be found that the output voltage nearly remains the same as the value under full load situation. Here, it can be taken the same value for it \(V_o=229\text{V}_{\text{ots}}\). The relevant values can be calculated as following:

\[
I_{\text{inmax}} \approx 0.2 \times 1.5 \div 0.1 = 3.0(A) \tag{5-6}
\]

\[
P_o = \frac{V_o^2}{R} = \frac{229 \times 229}{200} \approx 262.2(W) \tag{5-7}
\]

\[
P_{\text{in}} = \frac{V_{\text{inrms}} \times I_{\text{inmax}}}{1.414} \approx \frac{150 \times 3.0}{1.414} \approx 318.2(W) \tag{5-8}
\]

\[
\eta = \frac{P_o}{P_{\text{in}}} = \frac{262.2}{318.2} \approx 82.4\% \tag{5-9}
\]

It can be found that the efficiency under three-quarters load situation is still acceptable. After many times trial, it can be seen that the input voltage range for the APFC circuit to work normally is about \(\text{rms 75 Volts-160 Volts}\). If the input voltage is more than \(\text{rms 160 Volts}\), this circuit will not be able to work normally and the input current will become pulsed waveform. Here, the reason for this phenomenon will be explained. Because the power converter is a Boost converter, the output voltage must be always more than the input voltage for the converter to work normally; otherwise, the converter will not be able to work normally. When the input voltage is equal to \(\text{rms 160 Volts}\), its maximum value is equal to: \(V_{\text{inmax}}=1.414V_{\text{inrms}}=226\text{ Volts}\). The experimental results prove that this is always true for the boost converter. From the common knowledge of the boost converter, it is known that the output voltage is determined by the duty cycle \(D\) of the converter. The duty cycle \(D\) is controlled by the control circuit and the current sensing resistor in the main circuit together. From the measured results and calculated results, it can be found that the input power and output power are less than 1kW and output voltage is less than 400V, all these suggest that the duty cycle must be increased in order to increase the output voltage and output power. The fundamental measure is to reduce the value of current sensing resistor. This will increase the input current value and input power effectively. Certainly, the output power, the output voltage
and the input working voltage will be increased. This will solve this question effectively.

Generally speaking, there are two reasons for the obvious harmonics in the input current. The first one is because the output power and output voltage for this circuit is less than the specifications, but the circuit components values are designed for desired output power and output voltage. This means that the circuit does not work at the desired condition and this will produce the harmonics. The other reason is perhaps because of the value of gate driver resistance $R_g$ is not appropriate. In the following, the answer will be found to solve this problem step by step.

5.2 The Experimental Results for Current Sensing Resistor $R_s$ of 0.1 Ohm and IGBT Gate Driving Resistor $R_g$ of Different Values

Because the value of gate driving resistance $R_g$ is important for the normal work of IGBT, it is useful to check the circuit performance under different values of $R_g$ to ensure that the present value of $R_g$ is appropriate; otherwise, the circuit will not be able to work normally even if the main circuit and the control circuit are all excellent combination. The experimental results for different values of $R_g$ are listed as following.

1. The experimental results for full load situation ($R=150\Omega/R_g=85\Omega/V_i=130V_{rms}$)

![Fig. 5.4 Full Load Experimental Results (130V_{rms}/R_g=85\Omega)](image_url)
Compared with Fig. 5.3, it can be found that the input current harmonic becomes more obvious. This suggests that it is not appropriate for this APFC circuit to choose the value of $R_g$ lower than 150 Ohms. If a lower gate driving resistance for power switch IGBT is chosen, it can be found that the input current harmonics will become sharper and the input working voltage will be improved to some extent.

2. The experimental results for full load situation ($R=150\Omega/R_g=270\Omega/V_r=150V_{\text{rms}}$)

In order to find an appropriate gate driving resistance value for the power switch IGBT, a higher value should be tried for $R_g$ by experiment. Here, a value of 270 Ohms is chosen to make this experiment. The corresponding wave forms are as following.

\[
\begin{align*}
V_{\text{in}} \text{ (C1 Signal): Input Line Voltage (Volts)} \\
I_{\text{in}} \text{ (C2 Signal): Input Line Current (Amperes)}
\end{align*}
\]

\[
\begin{align*}
\text{Fig. 5.5 Full Load Experimental Results (150V_{\text{rms}}/R_g=270\Omega)}
\end{align*}
\]

\[
\begin{align*}
V_{\text{in}} \text{ (C1 Signal): Input Line Voltage (Volts)} \\
I_{\text{in}} \text{ (C2 Signal): Input Line Current (Amperes)}
\end{align*}
\]
Chapter 5 Experimental Results

Fig. 5.5[A] Full Load Experimental Results of $V_o$ (150V$_{rms}$/R$_g$=270Ω)

$V_{in}$ (C1 Signal): Input Line Voltage (Volts)

$I_{in}$ (C2 Signal): Input Line Current (Amperes)

$V_o$: (C3 Signal): APFC Output Voltage (Volts)

It can be found that the input current harmonic is reduced a little for this case, however, the output voltage, input power and output power do not satisfy the specifications.
3. The experimental results under deficient load situation \(R=180\Omega/R_g=270\Omega\)

![Image of experimental results graph]

**Fig. 5.6 Deficient Load Experimental Results \(R=180\Omega/V_i=96V_{rms}/R_g=270\Omega\)**

\(V_{in}\) (C1 Signal): Input Line Voltage (Volts)

\(I_{in}\) (C2 Signal): Input Line Current (Amperes)

After several trials, it can be found the circuit working load range is: \(R=150\Omega - 180\Omega\) when gate driving resistance \(R_g\) is equal to 270 Ohms. Therefore, the load range is reduced a little for \(R_g=270\Omega\) compared with the situation of \(R_g=150\Omega\). It can not solve the harmonics satisfactorily. Considering the waveforms and load range together, it can be found that it is appropriate to choose the gate driving resistance 150 Ohms for \(R_g\) for this 1Kilowatts boost active power factor corrector.

### 5.3 The Experimental Results for Current Sensing Resistor \(R_S=0.05\Omega\) and Gate Driving Resistor \(R_g=150\Omega\)

According to the project specification, measures should be taken to ensure this APFC circuit performs well for input voltage of “200Volts ~ 230Volts” and reduce the input current harmonics as lower as possible. From the above discussion, it is known that
the main reason for these discomforts is because the input power is lower than the specified value. The current sensing resistance should be reduced so as to increase the input power and the output power up to the specified value and check whether the performance of this APFC circuit can satisfy the requirement or not. Certainly, this will need higher current level main power switch IGBT and input diode rectifier. The circuit performance for this situation ($R_s=0.05\text{Ohms}$) with current components is checked and the results are satisfactory. The input power and output power all reach the specifications and there is no input current harmonics. Certainly, the present IGBT and diode rectifier all fired when I test the circuit under full load situation and there is no time for me to record the wave forms. In the end, the half load situation ($R_c=300\Omega$) is chosen to make this experiment so as to record the wave forms of this circuit. The experimental results are as following:

![Experimental Results](image)

**Fig. 5.7 Half Load Experimental Results ($22V_{rms}/300\Omega/R_c =150\Omega$)**

$V_{in}$ (C1 Signal): Input Line Voltage (Volts)

$I_{in}$ (C2 Signal): Input Line Current (Amperes)

From this experimental waveform, it can be seen that there is nearly no harmonics.
in the input current. The distortion of the input voltage is mainly because the diode rectifier and power switch IGBT fired. Therefore, there is no problem to get the satisfactory waveform if the higher current level diode rectifier and IGBT power switch are used in the experimental circuit. For the input power, it is equal to:

\[ P_{in} = \frac{V_{inmax} \times I_{inmax}}{2} \leq \frac{30 \times 3.8}{0.1 \times 2} = 570(W) \quad (5-10) \]

It can be found that it is correct for the half load situation of this project, so, this method can solve the input power problem effectively. There is no time to record the output voltage waveform before the burn-down of the diode rectifier and IGBT switch. However, the output voltage can be calculated approximately as following:

\[
P_o = \frac{V_o^2}{R_o}
\]

\[ \therefore V_o = \sqrt{P_o \times R_o} \equiv \sqrt{0.9 \times P_{in} \times R_o} \]

\[ = \sqrt{0.9 \times 570 \times 300} \equiv 392.3(V) \quad (5-12) \]

Therefore, the output voltage can satisfy the project specification very well, too.

For this case, it can be found that this circuit can work well from half load \((R_o=300\Omega)\) to full load range \((R_o =150\Omega)\). Therefore, the good choice for this project design is to choose the current sensing resistance value as \("R_s=0.05\Omega"\) and the gate driving resistance value as \("R_g=150\Omega"\); then, this boost active power factor corrector can satisfy the project specification.

Although the diode rectifier and IGBT switch fired shortly, a not very satisfactory waveform is recorded. This result proves that it is a satisfactory method to solve this question. If the higher current level diode rectifier and power switch IGBT are used to make the experiment, the satisfactory waveforms can be recorded. Since this is only to develop the APFC circuit, it will be enough to find the correct answer to the problem. There is no need to spend money to buy expensive components to record the satisfactory waveforms. They can be recorded conveniently when commercial product is built.

From all the experimental results listed above, it can be seen that this Boost APFC
circuit can satisfy the project specifications in the required input line voltage range and the wide load scope. Therefore, the final revised circuit is feasible for this project. This boost active power factor corrector can be used in North America (AC120V/60Hz), Asia (AC220V/50Hz) and Europe (AC230V/60Hz) directly.

Compared with the simulation for this Boost APFC in Chapter 4, it can be found they are nearly the same from half load to full load range. The main difference between the experiment and simulation is that the current sensing resistance must be reduced to 0.05Ohm; otherwise, this circuit can not provide 1Kw output power. The reason is that simulation can not include all factors of the practical circuit. There is a great deal of flexibility in the choice of current sensing resistance. This has to be solved by experiment. From this project design, it can be found that simulation is a very useful tool for practical design. A lot of element values can be determined by simulation directly; this will save a lot of time and money in project design. However, some component values have to be determined by experiment; this suggests that simulation can not replace experiment for the project design. A good engineer should combine the simulation and experiment effectively to solve the practical engineering problems.
Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this thesis, the development of a Boost Active Power Factor Corrector has been considered. A number of issues regarding the implementation of APFC circuit have been investigated. A brief conclusion opens in this section to summarize the major conclusive remarks obtained in the early chapters.

In chapter 2, a boost converter topology is presented as the main circuit of the active power factor corrector after theoretical analysis and comparison of several commonly used converters. After careful studies of several control methods, the average current control method is chosen to implement the control circuit for this Boost APFC project. Meanwhile, a theoretical calculation of the important component values in this active power factor corrector is described.

The next chapter explains the method to choose important components for this boost APFC circuit in detail. Then, the basic knowledge of control chip UC3854 is introduced because the control circuit is formed with it. Therefore, its basic working theory and application requirement should be understood before it is used to build the whole control circuit.

In chapter 4, a detailed simulation is given for this APFC circuit. In order to make this circuit multi-usable, the European Standards, Asian Standards and North American Standards are taken into account and make two sets of simulation (230V/50Hz/60Hz; 220V/50Hz/60Hz). Because the load maybe change in practical application, it is necessary to ensure that the PFC circuit can still work satisfactorily when the load changes in an allowable scope. The simulation is made for three different cases (full load,
half load and one-third load) to verify that this circuit can perform well and satisfy the load change requirement.

In chapter 5, experiments are made to check this project design for two sets of current sensing resistors (0.1 Ohms/0.05 Ohms) and several gate driving resistances. The final results are satisfactory. As for the 50 Hz input power situation, no experiment was made to verify the performance of this boost active power factor corrector because there is only 60 Hz line frequency power to use directly. From the simulations for these two situations, it can be inferred that the circuit will perform well for 50 Hz line frequency input power, too. Certainly, the performance of this Boost APFC for 50 Hz line frequency input power can be verified with an electrical generator which produces 50 Hz line frequency input power at first. Although the greatest efforts have been made in components selection and schematic circuit design of this project, some uncertainty still exists in the practical implementation. This is mainly for the choice of suitable values for current sensing resistor $R_s$ and gate driving resistor $R_g$. These problems have been solved step by step and the experiment is finished in the end. The experience gained from this implementation will give me some guidelines to the future work of IGBT related converters and the UC3854 related controllers.

### 6.2 Future Work for This Project

In order to make this boost active power factor corrector a commercial product, the next step is to build a PCB control circuit including the basic control chip UC3854 and relevant components to reduce the layout problem and improve the reliability of the product. Because the switching frequency of the boost converter is high (For this project, it is equal to 100 kHz), the switching loss will become more serious compared with other losses of the boost active power factor corrector. If we expect to improve the efficiency and switching frequency further, measures should be taken to reduce the switching loss greatly. An effective method to solve this question is to use Zero-Voltage-Switching technology [2], [3], [4]. In this way, the switching frequency of the power converter can
be improved and the product volume can be reduced greatly without reducing the converter efficiency. The ZVS can be realized by adding a parallel snubber circuit across the main switch IGBT and revise the control circuit according to the real project situation. In this way, the voltage across the IGBT can be reduced to zero before its “Turn-on” signal and make it realize “Turn-on” under zero voltage condition; thus, the switching loss will be reduced greatly and the efficiency will be improved [2], [3], [4]. The basic control chip UC3855 can be used to build the effective control circuit for this ZVS boost active power factor corrector. If there is a company interested in this ZVS PFC circuit, it can be improved in this way.
References


[14] Application Note, Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs, International rectifier, see http://www.irf.com/technical-info/appnotes/an-944.pdf

Appendix A

Permeability versus DC Bias Curve

In order to be convenient to check this property of Kool Mu Cores for MAGNETICS company, this curve is appended as following:

This figure is removed because of no copyright permission.

Fig. 1 Permeability versus DC Bias Curve
Appendix B

Permeability versus Frequency Curve

Because the switching frequency is 100kHz, this curve of Kool μ core is appended in the following so as to be convenient to check.

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Fig. 2 Permeability versus Frequency Curve
Appendix C

Normal Magnetization Curve

In order to be convenient to check the normal magnetization characteristic of Kool Mu cores, this curve is appended as following:

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Fig. 3 Normal Magnetization Curve