IMPROVEMENT OF LONGEVITY AND SIGNAL QUALITY IN IMPLANTABLE NEURAL RECORDING SYSTEMS

by

Arash Zargaran Yazd

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Abstract

Application of neural prostheses in today's medicine successfully helps patients to increase their activities of daily life and participate in social activities again. These implantable microsystems provide an interface to the nervous system, giving cellular resolution to physiological processes unattainable today with non-invasive methods. The latest developments in genetic engineering, nanotechnologies and materials science have paved the way for these complex systems to interface the human nervous system. The ideal system for neural signal recording would be a fully implantable device which is capable of amplifying the neural signals and transmitting them to the outside world while sustaining a long-term and accurate performance, therefore different sciences from neurosciences, biology, electrical engineering and computer science have to interact and discuss the synergies to develop a practical system which can be used in daily medicine practice.

This work investigates the main building blocks necessary to improve the quality of acquired signal from the micro-electronics and MEMS perspectives. While all of these components will be ultimately embedded in a fully implantable recording probe, each of them addresses and deals with a specific obstacle in the neural signal recording path. Specifically we present a low-voltage low-noise low-power CMOS amplifier particularly designed for neural recording applications. This is done by surveying a number of designs and evaluating each design against the requirements for a neural recording system such as power dissipation and noise, and then choosing the most suitable topology for design and implementation of a fully implantable system. In addition a surface modification method is investigated to improve the sacrificial properties and biocompatibility of probe in order to extend the implant life and enhance the signal quality.

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List of Abbreviations

AMP	Amplifier
CM	Common-Mode
CMFB	Common-Mode Feedback
CMOS	Complementary Metal Oxide Silicon
DA	Difference Amplifier
DEX	Dexamethasone
IEEE	Institute of Electrical and Electronics Engineers
IMU	Impedance Measurement Unit
LNA	Low Noise Amplifiwer
MEMS	Micro-Electro-Mechanical Systems
MUX	Multiplexer
NEF	Noise Efficiency Factor
PC	Propylene Carbonate
PM	Phase Margin
PPY	Polypyrrole
SNR	Signal to Noise Ratio
VLSI	Very Large Scale Integration

Acknowledgements

I am writing these lines while I am spending my last days as a MASc student. It definitely feels great knowing that a major era in my life is coming to an end with success. Fortunately, I learnt many lessons during this period and as a result, I am now a more qualified engineer compared to the being of my graduate studies at UBC. However, that does not stop me from feeling excited to start a new face of my life and face its challenges.

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Dedicated to

My mother, Mahasti

My father, Reza

and My sister, Hasti

Chapter 1

Introduction

1.1 Motivation

Many biomedical applications will benefit greatly with the development of implantable microscale components. Neural implants, such as deep brain stimulators and cochlear implants, interface nervous tissue with electronic devices. Microelectrode neural probes can simultaneously record signals at different regions in the nervous tissue, and can provide insight into processes such as memory pattern, perception, and muscle control. Typical amplitude of the signals from extracellular single spike activity and intracortical local field potentials are in the tens of microvolts range [1]. The very low amplitude of such signals calls for on-site amplification to minimize external noise and interfering signals to achieve an acceptable signal-to-noise ratio (SNR).

The desired proximity of the amplifier to the electrode has motivated embedding of the amplifiers on the neural probes and implanting them in the body. Low power consumption of these amplifiers is therefore of great importance, particularly in systems with multi-electrode arrays. Low power consumption makes the power management of the implant easier and/or improves the longevity of the device. It also reduces the heat generated by the amplifiers. Such low power amplifiers can be powered wirelessly using inducting coils.

Low-voltage operation of neural implants facilitates the use of smaller batteries. Also, the current trend in CMOS feature size scaling requires proportional scaling in the power supply to maintain device reliability. In designing biosignal amplifiers the trade-off among low-power, low-voltage, and low-noise operation should be considered. Many neural and biosignal amplifiers have been reported in the literature, however, such amplifiers use a conventional operational transconductance amplifier (OTA) biased with a tail current source, as their input stage. The voltage drop required across the current source to maintain its operations consumes a portion of the voltage headroom and makes it difficult to lower the supply voltage; these conventional OTA topologies are not suitable for low-voltage operation design.

Compounding the basic challenge of small extracellular signal amplitude is the commonly reported problem that some of the elements in a microelectrode array can no longer properly interface with nervous tissue. One factor that may contribute to this effect is the increased electrical impedance of the scar tissue surrounding the implant. The tissue response to a chronic implant is usually in the form of a compact scar layer that surrounds the device, having a thickness in range of tens to hundreds of microns. Single spike potentials have a kHz range frequency, while slow field neural activities range up to hundreds of Hz. Measurement of the tissue impedance over a wide frequency range may give information on the quality of the electrode-tissue contact, show change in the surrounding tissue, and indicate the recording ability of the electrode under these circumstances. This monitoring can be done *in vivo*. The measured impedance may also be used to compensate for signal attenuation with time.

1.2 Contributions

There are several electrical, biomedical and micro-mechanical challenges that should be considered and addressed in the design of a neural implant to sustain an appropriate quality and SNR for the recorded signals. Knowledge of electrical, biomedical and mechanical engineering combined with neuroscience and medicine is needed. The vast spread of the required knowledge is a major challenge and results in a partial focus through the previous works.

The reactive response of neural tissue which weakens the acquired signal is a major problem in maintaining a high quality signal. In this work we try to improve the signal quality and longevity by considering both biological and electrical requirements (and impediments) of the implant in harmony with each other.

1.2.1 Improvements from VLSI Perspective

We propose a method for compensating the signal attenuation due to scaring phenomenon. By monitoring the tissue-electrode interface impedance, we can make up for the decreased signal amplitude with signal processing techniques.

A popular technique for measuring this impedance is to apply stimulation currents with frequencies in the range of 0.1 Hz to few tens of kHz [3] to the electrode-tissue interface and perform the impedance measurement based on the recorded signals from the site. In order to perform such impedance measurements, it is desired that the recording amplifier accommodates the extended bandwidth required for such stimulations so that the resulting signals can be properly recorded. Therefore, we have designed a neural amplifier that can be used for both recording neural activities and the impedance measurement signals. The amplifier has sufficiently wide bandwidth for characterizing the electrode-tissue impedance while still keeping the input-referred noise below the required limit.

The designed amplifier consumes less than 80 μW (including biasing circuits) which makes it suitable to be implemented in a multi electrode neural recording system where a replica of the amplifier is used for each channel. Our ultra-low operation voltage is a great advantage for the low-power battery-powered neural implants which are intended to operate wirelessly. Other advantages of ultra-low-voltage operation will be discussed in Chapter 4. Finally we present test bench measurements results which are in accord with the simulations.

1.2.2 Improvements from MEMS Perspective

Although well-designed electronics can substantially enhance the signal quality, a good circuit by its own would be insufficient as the scar layer will thicken gradually and ultimately results in complete signal blockage. Thus, further improvements should be applied to the probe in order to decelerate the generation of isolation barrier between the electrodes and neurons.

Electrically Controlled release of anti-inflammatory agents from a conductive polymer (polypyrrole) was first introduced by [32]. Similar systems has been developed by [4] and [33] using different polymer and dopants. However, these woks have not studied the challenges and feasibility of integration a controllable polymer-based drug delivery system into an actual neural probe.

We modify the surface of the electrodes in a neural probe by a coating of polypyrrole which is a biocompatible polymer. The main advantage of Polypyrrole coating is that it can be loaded with an anti-inflammatory drug where the drug can be released in desired amounts with certain electrical stimulation patterns. We propose a design for an on-probe drug delivery system, and then we investigate the potential problems of using it for *in-vivo* signal recording. One of the issues affiliated with the implementation of such system are the potential attenuating effect of the polymer film on the recorded signals. However, the main drawback of using electrical signals to control the release profile inside the nervous system is the stimulation of neighboring neurons by the control voltage. To address

these issues, we study the impedance of different thickness of Polypyrrole film inside a solution which mimics the cerebrospinal fluid. Also, we propose a solution to reduce the amplitude of the leakage currents, which flow into the nervous tissue, below the stimulation threshold of neurons.

1.3 Proposed Neural Recording System Overview

We begin by giving an overview of the neural probe components and the requirements of a fully implantable recording system in Chapter 2. Key issues in the design and implementation are discussed, and we highlight which of those issues this work will be addressing. Chapter 3 discusses the challenges of preventing the scar layer formation around the probe and presents our controlled drug-delivery solution to avoid gradual isolation of the recording electrodes. In Chapter 4, we present an overview of a low-voltage design technique for analog circuits. We also discuss the design and implementation of our ultra-low-voltage low-noise OTA and the feedback configuration of the amplifier along with test results. Finally, Chapter 5 presents concluding remarks and the future work and possible improvements for neural recording systems.

Chapter 2

Fundamentals of Neural Implants

Neural implants have a significant ability to enhance our understanding of different states of the brain, and at the same time highly impact the design and use of prosthetic devices. The importance of neural implants is illustrated by the tremendous changes that they have made in different aspects of medicine such as the prosthetic cochlear implant, a commonly used treatment for deafness that involves implanting electrode arrays into the cochlea to stimulate the auditory nerve (Fig. 2-1). Also, micro-machined neural prosthetic devices are another example of these implants, which facilitate the recording from and functional stimulation of the central and peripheral nervous system [1].

Neural interfaces provide a connection to the neurons which are electrically active cells of the nervous system. Several examples of neural interfaces are cochlear implants, deep brain stimulators and cardiac pace makers [5], [6]. Implanted neural probes can either stimulate neurons or record signals directly from desired regions of the brain. In deep brain stimulation neural implants are used to treat a wide range of movement disorders and neurological conditions by applying high frequency electrical signals to specific regions of brain. The currents to excite single cells are in the range of picoamperes, while hundreds of microamperes are required to stimulate neurons as in the treatment of Parkinson disease [6].

Figure of cochlear implant removed for copyright reasons. Please refer to [7].

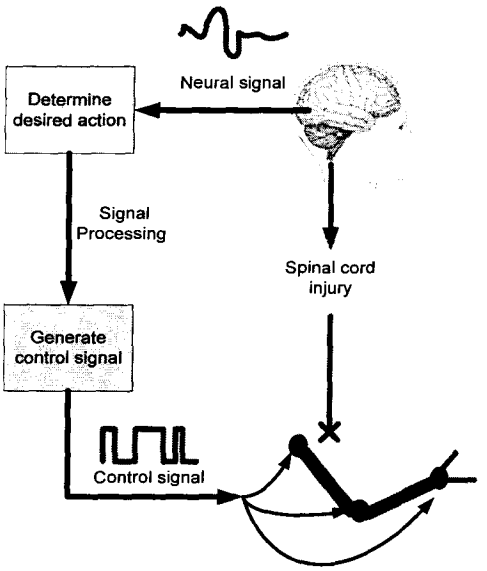

Figure 2-1. Stimulation (left), and recording (right) function of neural implants.

Invasive neural implants record neuro-potentials from inside the nervous system. Recording electrical signals from nerves in the body or neurons of the brain is not feasible without such electrodes. These signals usually range in the tens of microvolts during the intracortical signal recordings such as recording the single spike activities or local field potentials while the intracellar potential of cells is usually in the range of tens of millivolts. The studies on electrical properties of neural implants are focused on the biologically relevant frequency of 1 kHz because the majority of neural signals which are extracted from the brain or nerves have a frequency of about 1 kHz [9].

Although these devices have shown great promise in treating neurological disorders and monitoring neural signals, as they are implanted in the brain cortex they cause some degree of damage to the brain tissue which is unavoidable. The ideal implant has a very tiny cross section so as to minimize the damage and displacement of tissues during the insertion operation. Also, instead of having several shanks, it's usually better to have large number of electrode sites on a single shank to reduce the area of the tissue that is injured during surgery while retaining the ability to record separate

signals from different neurons. Yet after these modifications still a significant clinical risk is entailed due to the injury and potential infection at the implant site. Therefore the primary challenge is the inability to record neural potentials following surgery and implantation. The performance parameters of a neural recording system can be appropriately selected only if we have a good knowledge of the neural tissue characteristics and challenges of *in vivo* operation.

Recording signals directly from neurons requires stable amplification and signal processing techniques to interpret neural signals. Also, electrodes have to be stable for long periods of time to maintain an acceptable SNR. Besides that, the effectiveness of the implant decreases with time due to fibrous encapsulation and glial scarring which electrically isolate the probe contacts from the nervous system [10],[11]. Several solutions for improving the interface of implant and neurons have been considered and explored. Among them are covalent immobilizations of bioactive material and drugs [12], [13]; electrostatic layer by layer self-assemblies [14], electrochemical polymerization combined with immobilization of biomolecules [4]. Acquiring a high SNR signal from the nervous system requires several vital factors to be considered in the overall design of the implant. As the recording time increases to weeks and months more and more strategies should be implemented to retain the quality of signal during this extended amount of time.

This chapter discusses the various components of a fully implantable neural recording system, and the design issues surrounding each component. The emphasis is placed on electronic and biological solutions to increase the quality and longevity of the recorded signal. This has been addressed from both electronic and biological perspective by decreasing the noise level of the amplifier and making the electrode surface more biocompatible.

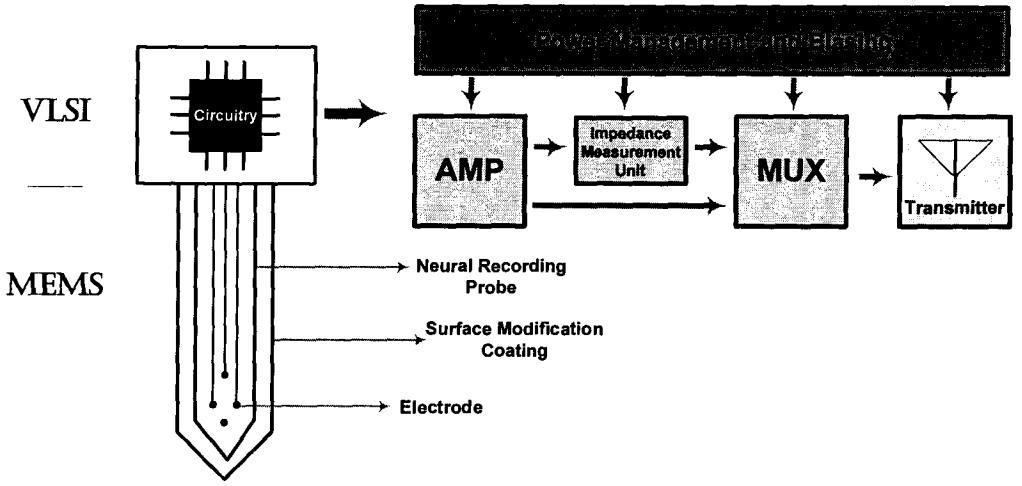

Figure 2-2. Block diagram of a fully implantable recording system. The system is composed of embedded circuits to process and transmit the signals (VLSI section), and the recording electrodes, which are usually fabricated on the same substrate, along with the surface modification coating (MEMS section).

1.4 Components of an Integrated Neural Recording System

Knowledge of several engineering and science fields should be combined to design an integrated neural recording system which conforms to the specifications and requirements of *in vivo* studies. There are many branches of science and engineering which must be combined to produce an integrated recording system. The most important of these are electrical engineering, biomedical engineering, and biology. A block diagram of an INRS is shown in Figure 2-2. This system has two main sections, the MEMS section and the VLSI section. The electrodes and surface modification coating (drug release unit) belong to the first section, whereas the microelectronic circuitries (amplifier, impedance measurement unit (IMU), multiplexer and transmitter) are parts of the second section. VLSI components perform the amplification, signal processing and signal communication. The data from IMU can be used to compensate for the signal attenuation due to tissue reactive response and also for controlling the drug release unit.

The electrodes are configured in the form of a two or three dimensional probe, and provide the interface between the biological signals being recorded and the electrical components of the system. We will elaborate on different types of probes and challenges in sustaining a high quality signal later in this chapter. Each electrode has an amplifier which boosts the recorded signal while adding minimal noise. The amplifiers feed into a multiplexer which performs time domain multiplexing on the signals to allow the information to be relayed to the outside world with minimal bandwidth consumption. The next component is the transmitter which is used to send the recorded signals to a receiver in the outside world. The system may be powered by a battery or by an inductive link which transfers the power through skin. At last, there should be reliable biasing circuitry for each of VLSI components; ideally the amplifier should be biased independent of supply voltage, temperature and process variations in order to have a stable gain and avoid unpredictable distortion of neural signals.

1.5 Types of Neural Probes

Microwires, the first electrodes which were used to record the brain signals, were made of insulated tungsten [15]. Utilizing this type of electrode, it is possible to perform individual extracellular recording from several cells with spike amplitude of tens of microvolts within 50 μm radius. They are still in use today for long lasting recordings from single neurons. Figure 2-3 shows an array of microwires. These electrodes are also used in deep brain stimulation due to their unique shape which allows them to access brain structures that are located deep into the brain [16]. Also by using an array of these electrodes, multi neural recording can be performed to capture dynamic interactions between neurons at different brain depths.

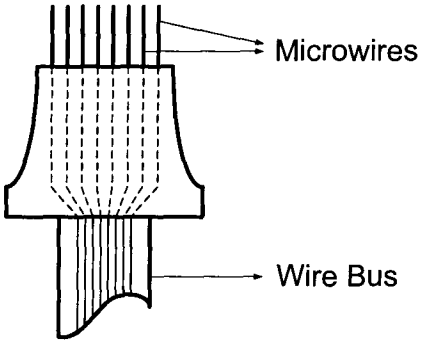

Figure 2-3. Microwire array.

Silicon is another material used in neural probes. Using photolithography and silicon etching techniques it is possible to fabricate multi electrodes from silicon. Their main advantage is that the fabrication technology which is used is similar to etching CMOS transistors on silicon wafers. Therefore, we are capable of forming any three dimensional arrangement out of the wafer. Based on the various shapes that this group of probes can have, they are able to simultaneously record signals from different brain structures and neurons. As the distance between recording endings are defined in the lithographic process, unlike the microwire arrays the distance between the tips of electrodes will not change after implantation surgery [17]. Michigan and Utah arrays are among this type of electrodes (Fig.2-4).

Another type of neural probes is flexible arrays which are generally made of polymers. Polymer- based implants such as polyimide probes are much more flexible than silicon ones thus, they can reduce the chronic responses of tissue. Also, *In vitro* tests on polyimide suggest that it has no cytotoxic response [18]. Considering these facts, polyimide implants are more biocompatible than Michigan and Utah arrays which are made of silicon wafers. Polyimide probes can be fabricated using standard photolithography techniques. Due to the inherent flexibility of polymers and their diverse fabrication methods, compared to silicon, it is possible to make the probe in various shapes such as cuff shaped or double sided for different purposes [15].

Figure of Utah array and Michigan probe removed for copyright reasons. Please refer to [19].

Figure 2-4. Utah array (Left) and Michigan probe (Right) .

1.6 Biocompatibility

Whether used for recording or stimulating, the neural implant has to ideally maintain a high quality interface with nervous tissue without causing damage and reactive response inside the tissue following its implantation. However, from the host tissue perspective, such a device is considered as foreign body which interrupts the normal biological function at the implantation site and peripheral area. Although the tissue damage and its consequences are inevitable, it is feasible to take its proliferation under control.

The biological attributes of an implant can be classified as structural biocompatibility and surface biocompatibility. Structural biocompatibility is related to the tissue damage caused by the implant and its acceptance by the host tissue. Device design, shape and rigidness should be in harmony with the biomechanical specifications of the host tissue [2]. Specifically, structural flexibility is important to avoid damage to surrounding tissue in the event of micro-motion and impulse movements. Silicon-based devices tend to be stiff and brittle, making them poor candidates as neural implants. The mechanical mismatch between the stiff silicon electrode and soft tissue increases the injury and inflammation levels during insertion of the electrode and also the usage period. This effect causes more scar layer around the probe which acts as a mechanical and electrical shield that inhibits the electrode and tissue attachment; as a result it is important to make the tip of the electrode which enters the cortical tissue as flexible as possible [18].

On the other hand, the surface biocompatibility deals with the interaction of the biomaterial and morphological surface properties of the foreign structure with the host tissue, and also consecutive reactive functions following the implantation. From this point of view, a material can be described as biocompatible if the concentration of glial cells (which result in rejection of the foreign structure) and released toxic substances around the implanted structure are negligible. Also the reaction of the tissue to the implant, which is generally in the form of encapsulating scar sheath, should be moderate [2]. A material would be considered incompatible with biological environment if, its penetration to tissue results in severe immunoresponse, toxic effects and inflammation. There is ongoing research to make biocompatible materials which can cover semi or non-biocompatible structure and form a biocompatible interface with the tissue, yet their integration into neural probes is still a major obstacle. One of the milestones of this project is to combine these coating substances with anti-inflammatory drugs and apply the resultant material to the surface of neural probe to reach a truly biocompatible interface.

Chronic and electrically active implants in neural prostheses have to fulfill high demands with respect to biostability and biofunctionality. The choice of interface surface materials in a neural implant ensures temporally stable transducer properties of the electrode–electrolyte interface throughout the lifetime of the implant, thus to reach this goal, we generally focus on the second definition of biocompatibility.

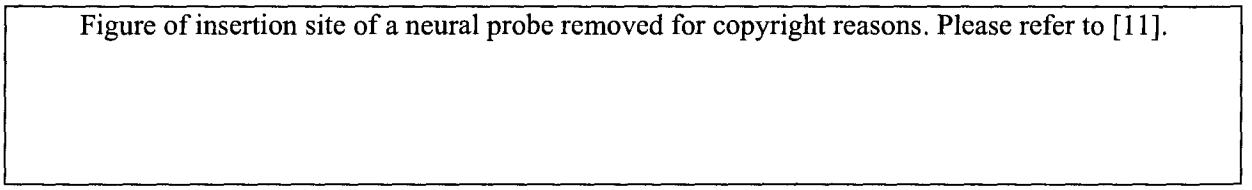

Figure 2-5. Insertion site of a neural probe . The dense scar layer isolates the recording electrodes.

1.7 Immune Response of Brain to the Implanted Probe

One common problem of all chronically implanted electrodes is retaining a long term and stable interface between the implant and nervous system. Current studies suggest that the biological response of the brain to the implanted electrode is the greatest challenge for obtaining a stable and consistent intracortical recording. Although current microelectrode arrays perform well in acute applications, chronic performance remains inconsistent. Using microwire arrays, [17] has reported a steady drop in the number of functional electrodes remaining over time. To alleviate this phenomenon the probe should be made as biocompatible as possible.

In order to design recording electrodes that minimize the immune response of the central nervous system, the biological mechanisms involved should be understood. The following provides an overview of the response from the central nervous system tissue to implanted needle-like probes. As shown in Fig. 2-5, insertions of any object into the brain damages the tissue and results in a gradual scar formation. During insertion, blood vessels and nerves are disrupted, and therefore, micro hemorrhage takes place in the tissue. Neurons are either ripped or sliced as the electrode is inserted, and hence microglia derived from monocytes are activated, and astrocytes begin to proliferate, which forms a loose shield around the electrode for a considerable distance around tens of microns. A cascade of events, stemming from disruption of vessels at the barrier of blood and brain, takes place which leads to proliferation of immune components [11].

Several kinds of cell populations are involved in the inflammatory and wound healing response to probes or in general materials which are implanted in the central nervous system, among them glial cells have the largest influence in this process.

Figure of tissue's acute and chronic response removed for copyright reasons. Please refer to [20].

Figure 2-6. Tissue's acute (a) and chronic (b) response to implanted probe [20]. The glial cells completely surround the foreign structure in chronic applications

1.7.1 Astrocytes

Astrocytes are the most prevalent type of glial cell. They play a role in supporting brain tissue and nourishing neurons (for instance, they supply neurons with lactate derived from glucose). They also play a role in scar formation.

1.7.2 Microglia

Microglia are a major type of glial cells involved in the brain's scar healing response and electrode encapsulation, constituting 5–11% of the total number of glial cells in the brain . They are mobile cells that surround fragments of damaged cells within neural tissues. Generally, they act as cytotoxic cells killing pathogenic cells or as phagocytes secreting enzymes to degrade cellular debris and damaged matrix after injury or during regular cell turnover [11], [21].

1.8 Stages of the Immune Response

In response to brain injury, glial cells such as astrocytes and microglia proliferate to form a glial scar. Under normal conditions, astrocytes help to control the chemical environment of neurons. Previous work examining astrocyte response to brain injury has shown there are two phases of the foreign body response to device insertion into the brain.

1.8.1 Acute Response

The early response is observed immediately after device insertion, followed by a long term sustained response (Fig. 2-6(a)). The early response starts within hours of implant insertion and is characterized by an increased number of astrocytes and microglia in the area surrounding the device. This area can extend to a few hundred microns around the insertion site, and the response is proportional to the cross-sectional area of the devices [11].

1.8.2 Chronic Response

As shown in Fig. 2-6(b), the second component of the neural tissue reaction to implant is a chronic process which takes place on a slower timescale after implantation and results in the formation of a tight cellular sheath around the implant [22]. The sheath which forms around the insertion site is composed of loosely packed cells. As time passes, it becomes thinner and tighter with 5 to 7 layers of compact, dense cells with small nuclei, effectively isolating the electrodes from the brain tissue. This effect causes an increase in the impedance of the implant [2]. In addition to the glial scar sheath which surrounds the implant, neuronal cell loss may also result in electrode failure. Recent work have found a significant reduction in the number of neuronal processes and neurons in the close vicinity of the implanted probe [11], [24]. This effect varies depending on the biocompatibility properties of the coating and materials used in implant.

1.9 Reducing Inflammation and Improving Biocompatibility

Several solutions for reducing the reactive response and inflammation of the cortical tissue at the implantation site have been proposed. Some of them are related to the design of the shape and mechanical properties of the implant to reduce the initial injury. Yet to extract stable and accurate

signals from the neurons for long period of time, the electrode biocompatibility should be improved. The goal of these strategies is to inhibit the immune response of neural tissue either by modifying the surface of the probe using specific drug coatings or by injecting anti inflammatory drugs through microfluidic channels to the tissue electrode interface.

Some of current research in the field of neural implants are focused on making the surface of existing electrodes more biocompatible. This can be done through surface modifications on these probes. A biocompatible neural implant has several characteristics such as low protein adsorption, better specific cell interactions, the ability to promote tissue integration, minimizing encapsulation and enhancing long-term performance of the chronically implanted neural probe. Conventional biomaterial surfaces without any surface modification process show that we cannot have any accurate control over the interactions which happen between tissue and cell [24]. In a biological environment there are many proteins such as cell adhesion proteins which adsorb nonspecifically to different surfaces to form a multiprotein monolayer with an ill defined and random distribution. In our work we improve this non selective adsorption through a biocompatible polymer.

A bioengineered implant surface can inhibit the inflammatory cell adhesion and glial scar forming while improving axon regeneration and tissue cell adhesion. In the surface modification area, two major strategies are being taken to minimize the undesired tissue reactions to implanted electrode. One of them is enhancing neuronal adherence and growth to the electrode by immobilizing the anti inflammatory biomolecules on electrode surface or through releasing growth agents

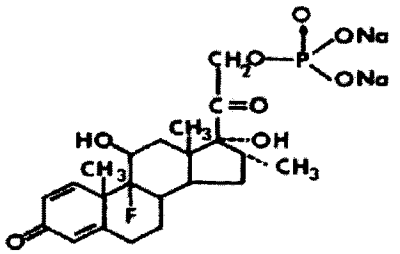

Figure 2-7. Dexamethasone, an anti-inflammatory drug [4].

from the electrodes. The other solution is mitigating the tissue reactive response through delivery of anti-inflammatory factors in the vicinity of the implanted electrode.

1.10 Anti-inflammatory Drugs

One of the most widely used anti-inflammatory drugs is Dexamethasone (DEX) (Fig. 2-7). It was first used in cardiac applications to maintain low stimulation threshold at pacemaker leads [11]. Inflammation at the electrode-tissue interface of cardiac pacemakers results in a fibrous sheat which significantly increases the stimulation threshold of the tissue. This increased threshold results in higher voltage outputs and lower battery life. To reduce this inflammation, pacemaker leads with capability of releasing anti-inflammatory agents were developed. The delivery of a anti-inflammatory drug which is embedded in the polymer coating has shown a good improvement in the tissue stimulation threshold [24]. DEX is a synthetic anti-inflammatory glucorticosteroid which is believed to act through the glucocorticoid receptors which are found in neurons and glial cells of the brain. This drug is in the form of dexamethasone sodium phosphate which is soluble in a saline solution and is stable at body temperature. When it is released inside the body, it quickly converts to its active form called dexamethasone. The DEX released by an implant could minimize the release of inflammatory mediators, and hinders the formation of a fibrous sheat around the probe.

1.11 Delivery of Anti-inflammatory Agents

In general, we can divide the drug delivery methods used for neural implants into two categories, systemic and local. Subcutaneous systemic injection of anti-inflammatory drugs has effectively minimized the reactive tissue response in cat's brain [25]. Yet, systemic injections have their own disadvantage which is exposing all of the parts of the body to high doses of the drug in some cases this makes a problem for the user because different drugs might have potential toxic characteristics when they reach body organs such as liver and kidneys. Considering this point, local delivery of drugs to the interface of tissue and implant would be more efficient and effective.

Local delivery of anti-inflammatory drugs can be performed through passive or active methods. Uncontrolled drug releasing coatings are a passive example. They are cheap and easily applied to existing neural probes compared to active methods. Yet, the problem is that the drug diffusion from the coating is dependent on the volume of the release medium. As the concentration of drug in the release medium gets closer to the saturation level, the drug release rate becomes lower and lower, reaching to the zero level at the time which the medium is saturated [24]. Therefore, when the release medium has a lower volume, drug is released slower and lasts longer than the case which the release medium has a larger volume. Hence, the release of drug in the insertion site does not have a constant rate. This results in an uncontrollable release of the drug which is not desired [4], [13].

Local drug injection using microfluidic channels is one of the active drug delivery mechanisms [26]. The amount of delivered drug can be controlled using microvalves and pumps. However adding more components to the neural implant arrays causes less reliability, more failure points and additional processing steps. Another active method is controlling the delivered dose from polymer based drug coatings using electrical signals [4]. We will comprehensively discuss the advantageous and limitations of this method in detail in Chapter 3. The active drug delivery approach

promises to improve the reliability and continuing functionality of implanted devices, thus paving the way for long term application of neural prostheses [20].

1.12 Electrode-tissue Interface Impedance

There are several factors that can change the electrode-tissue interface impedance; among them is the fibrous sheath which forms around the implant and the effect of the coating. Measuring this impedance is an effective method to characterize both electrode performance and quality of the recorded signal as it represents the resistive, capacitive and inductive barrier which neural signal confronts on its way to the signal processing and amplification circuits. Measuring the impedance can also help to compensate for the possible signal attenuation using digital signal processing techniques. Here we discuss the parameters which affect the value of the interface impedance and our solution to decelerate its increment.

1.12.1 Fibrous Sheath Effect

A study using impedance spectroscopy [17] showed that electrode impedance has a close relationship with fibrous sheath density. As microwires are generally made for single unit recordings, the increase of electrode-tissue interface impedance following implantation is one of the reasons that microwire recordings have been successful. Here, the high impedance makes it possible to isolate single action potential signals. Yet in case we want to record signals from many neurons, as in multi electrode probes, this is an undesired phenomenon. The scar sheath acts as an isolating layer therefore gradually decreases the signal amplitude. As the sheath forms, the amount of exposed surface is reduced, which increases the probe impedance. The microwire principle may apply to the Utah probe, which has relatively large recording sites at the shank tips. In contrast, the encapsulation is an obstacle for the

Michigan probe, which tends to record high-quality action potentials for the first one to two weeks after implantation.

1.12.2 Drug Coating Effect

Electrodes must be optimized to have stable impedance and no corrosion for long term biocompatibility. Ideally, they should have controlled electrode-tissue interface impedance. The importance of impedance fluctuation depends on how the electrode is going to be used. If we use the electrode for stimulation, the increase in the tissue-electrode impedance results in a decrement of the stimuli amplitude which is applied to tissue. This voltage drop across the interface can be compensated by an increase in the stimulation signal amplitude. Yet, if the electrode is used for monitoring neural signals, the increased interface impedance will further attenuate the minute neural signals, which directly decreases the overall SNR of the system. Hence, the quality of the recorded signals is more prone to degradation than the simulative effect of the exciting signals.

It is observed that applying a DEX coating on the Michigan probe significantly changed the magnitude of impedance at 1 kHz frequency yet because of the very high input impedance of the amplifier, the magnitude of the signals recorded by the coated probes is similar to the uncoated probes, therefore while the DEX coating can effectively reduce glial scar formation *in vivo*, the electrical performance of the electrodes was not affected by this coating [11], [25]. In this work we will investigate resistive and capacitive effects of the surface modification coating on the recording electrodes. The impedance of our surface modification coating will be investigated in Chapter 3.

1.13 Conclusion

According to the published experimental results, generally normal silicon based electrodes cannot maintain their activity inside the neural tissue more than few days. Also they have poor mechanical

properties such as inflexibility which make them more invasive to the brain tissue. Polymer based probes have more flexibility and less toxicity, yet they still have the signal attenuation problem in chronic experiments. Investigators have tried to make modifications to the biological properties of these electrodes surface using hydrogels and anti inflammatory drugs. These structures can be bound to bioactive compounds to improve the tissue-electrode adhesion.

Systemic and local DEX administration was effective at reducing the density of the scar sheath and down regulated the genes which controlled release of proinflammatory cytokines. Dexamethasone inhibits astrocyte hyperplasia and can also be incorporated into coatings applied to the electrode. The diffusion of these molecules into the tissue can be regulated by using electrically controllable drug packages on the electrode, so that a therapeutic dose is maintained over time. This technology may achieve the desired electrode neuron glial sheath interface that could lead to permanent long-term recording of neural activity.

Chapter 3

Controlled Drug Delivery System

Often recordings from electrodes of neural probe fail a few days after implantation. One mechanism may be the formation of astro-glial scar sheath around the implant. In this chapter, we investigate this problem from a biological perspective to inhibit the signal degradation and thus sustain an acceptable SNR.

One approach for reducing the pace of scar forming around the electrode is to introduce anti-inflammatory drugs, such as DEX, to the implantation site in a controlled manner. Neural probes with embedded micro fluidic channels and drug loaded probes are some of the strategies which have been already used for this goal [23]. Yet, each of these techniques suffers from major limitations. Although micro fluidic channels and valves allow a controlled release rate, they add to the complexity and cost of micro-fabrication process. Drug coating is a much simpler and cheaper approach, but it suffers from lack of sufficient control on the released drug dose [13].

Recently, Drug delivery systems have been introduced which utilize conductive polymers such as Polypyrrole (PPy). In this work, we discuss the electrochemically controlled release of drugs from conducting polymer, first introduced by Wadhwa et al. [4], and propose techniques to integrate such drug delivery system into neural implants. Primarily, we investigate the feasibility of modifying

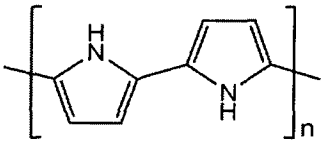

Figure 3-1. Polypyrrole chemical structure [28].

the surface modification of electrodes in a neural probe with a coating of drug-loaded polypyrrole, to locally release the loaded dopant in form of ions after receiving proper electrical stimuli.

Conductive polymers can be developed on a conductive surface by electrochemical methods [28]. The conductive property of polypyrrole is generally a result of its conjugated structure. In the chemical structure of Fig. 3-1, the double bonds (electrons) can be displaced from one pyrrole monomer to another monomer on the same chain [29].

3.1 Polymer Deposition

Polypyrrole can be synthesized through an electrochemical or chemical method which oxidizes the pyrrole monomers [31]. The underlying principle of electropolymerization and doping of PPy is shown in Fig.3-2.

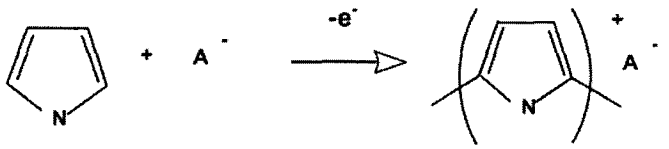

Figure 3-2. Electropolymerization of PPy [4].

In our study, we fabricate PPy films doped with tetraethyl ammonium hexafluorophosphate (TEAP) anions (PF_6^-) through a galvanostatic method. The reason to use TEAP (Fig. 3-3) is the large size of its cation compared to the anion. This inhibits the migration of TEAP cations from solution to the

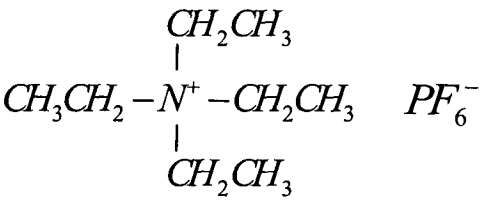

Figure 3-3. Chemical structure of tetraethyl ammonium hexafluorophosphate (TEAP).

polymer film [28]. The PF_6^- ions cause the PPy monomers become electrically oxidized and polymerized on the working electrode. The electrochemical setup has two electrodes (Fig. 3-4), the working electrode is a gold coated glass substrate masked to an area of 0.2 cm^2, and a platinum coated wafer with an area of 2 cm^2 is used as counter electrode. Unlike platinum and Indium tin oxide (ITO) glass, gold has a good adhesion to polypyrrole [28]. The size of the electrode is chosen to allow a cell current well above the minimum measurable current threshold of our potentiostat during the dopant release process; this increases the precision of our measurements in Section 3.5. The working and counter electrodes are connected to a potentiostat (Solarton Instruments) which sets a constant current flow between the working and counter electrodes. The thickness of the deposited polymer can be controlled via the total charge density during the process. A charge density of 60 mC/cm^2 is used to acquire a 110 nm thick polymer. The deposition medium is a 0.1 molar solution of pyrrole (Sigma) monomer and TEAP (Fluka) dissolved in propylene carbonate. The pyrrole monomers tend to oxidize spontaneously in room temperature. Therefore, to achieve a polymer film with good conductivity, pyrrole is stored in a freezer (-5° C) before experiments. Polypyrrole is synthesized by applying a 100 μA current through the working electrode and the platinum counter electrode. The galvanostatic current is enough to remove the electrons from pyrrole monomers and oxidize them which results in polymerization of monomers in vicinity of the working electrode surface [28]. Subsequently, the polymer chains move from solution to the surface of the gold electrode. The thickness of the deposited polypyrrole is controlled by the deposition charge per unit area of the working electrode.

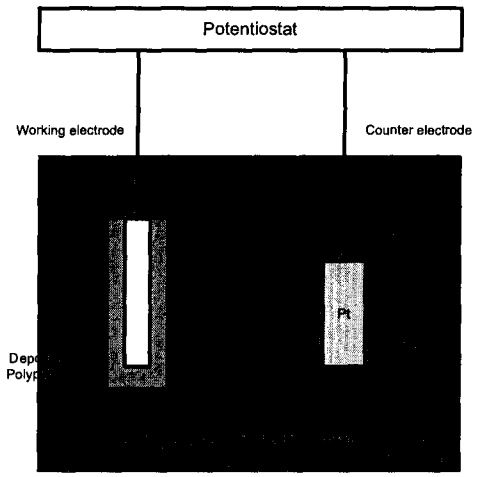

Figure 3-4. Two-electrode experimental setup for polymer deposition.

The deposition rate for a small-area working electrode (< 1 cm^2) and low deposition currents (< 0.01 μA) is roughly 3 μm/hr. It is possible to achieve films as thick as 30 μm using the galvanostatic method. A current density in the order of 5 mA/cm^2 tends to lift the gold layer (deposited by evaporation) from the glass substrate. Hence, to synthesize thick polymers we should increase the deposition time rather than increasing the current density. The film has a smooth surface for thicknesses below 1μm, yet the roughness increases as we develop a thicker polymer.

The presence of TEAP in the synthesis solution serves several functions: first, due to its solubility in propylene carbonate, it functions as a conducting electrolyte to allow oxidation of pyrrole monomers; second, TEAP is an amphiphilic surfactant that allows a high concentration of hydrophobic pyrrole monomer to be dissolved in an aqueous solution; and third, most importantly, its anions (PF_6^-) get incorporated into the porous polymer and act as a dopant in the controlled release procedure, where they can leave the polymer in the reduction phase of the reaction shown in Eq. 3-1.

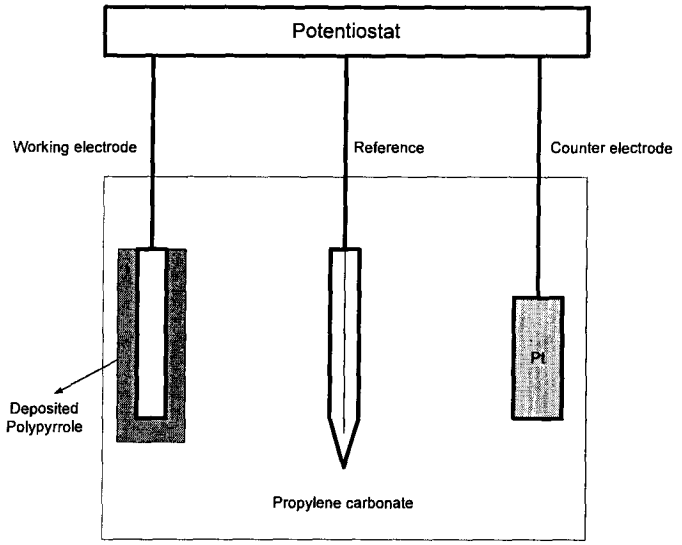

Figure 3-5. Experimental setup for Cyclic Voltammetry.

3.2 Cyclic Voltammetry of the Doped Polymer

In the method proposed by Wadhwa et al., the dopant (dexamethasone) is released from a polypyrrole coating. To release the dopant from the conductive polymer, a specific electrical stimulation should be applied to it. The fundamental principle behind the drug release process can be explained by the following oxidation (Eq. 3-1) and reduction (Eq. 3-2) reactions

$$[(PPy)^{x+}\ A^{-}{}_{x}] \overset{+xe^{-}}{\Longrightarrow} PPy + xA^{-} \tag{3-1}$$

$$[(PPy)^{x+}\ A^{-}{}_{x}] \overset{-xe^{-}}{\Longleftarrow} PPy + xA^{-} \tag{3-2}$$

Where A^{-} is the TEAP anion (PF_6^{-}). Movement of the anions out of the polymer results in dopant release. In Eq. 3-2, $(PPy)^{x+}\ A^{-}{}_{x}$, shows the oxidized state of the polymer, and $PPy + xA^{-}$, shows the polymer in reduced state [4] [32].

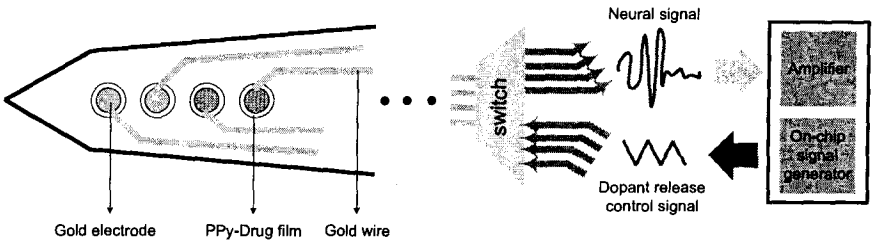

Figure 3-6. Schematic of the modified neural probe and the data-acquisition/stimulating circuits. The switch connects the appropriate circuit to the electrodes in the related mode of operation. These circuits can be implemented on a single chip and embedded to the neural probe.

3.3 Analyses of the Polymer Film

There are several ways to integrate the drug release system into a neural implant, yet we classify them into two general methods: the first is implementing the components of the drug-release system separated from the recording electrodes (separated method), and the second is to combine them with the recording pads (unified method).

Although in the separated method the released dopant can reach locations farther from the release site through diffusion process, this phenomenon may be insufficient or inefficient to propagate the minute dose of dopant to all electrodes in a probe where electrodes are spread along a 2 cm long substrate [12], [17] (i.e. some types of Michigan probe) or where the electrode shanks have different puncture locations as in three dimensional probes (i.e. Utah array). Hence, to embed the polymer based drug-release system into different types of neural probes, we propose the configuration shown in Fig. 3-6. Another advantage of the unified configuration is that the PPy is a biocompatible polymer and promotes cell adhesion to the surface of the electrodes [27], leading to a better signal quality.

Figure 3-6 demonstrates that the probe electrodes become double function devices acting mainly as recording devices and occasionally as excitation source for releasing the dopant ions from

the polymer structure. While the proposed system is advantageous in implant area, longevity, signal quality, and drug delivery efficiency, still the additional impedance introduced by the PPy coating to the neural signal path and its effect on the SNR of the recorded signal should be investigated.

3.3.1 Morphological Properties

To investigate morphological and electrical properties of the polymer coating, three sets of electrodes, each having four electrodes with a size of 4 mm^2 are made. Electrodes of each set are coated with PPy with the scheme shown in Table 3-I. Thickness, roughness and surface morphology of the deposited PPy-TEAP film is measured using AFM tapping mode. As demonstrated in Figs. 3-7(a) and (b), with a deposition current of 100 μA the film surface appears to be smooth and the root mean square (RMS) roughness (computed by AFM instrument) has a value of 29 nm and 32 nm for 80 sec and 160 sec deposition time, respectively. Increasing the deposition current to 1 mA severely increases the surface roughness to 3.4 μm (Fig. 3-8(c)). Also, the uniformity of the deposited film decreases as we increase the deposition current density, with some areas being smoother or rougher than the others.

From Fig. 3-7 it is evident that the thickness of the polymer film does not increase linearly with the increment of deposition charge density. This is due to the fact that the wrinkled polymer surface increases gradually, hence the charge density at the electrode surface becomes lower; ultimately, this results in a decreasing deposition rate, albeit we have kept the deposition current constant.

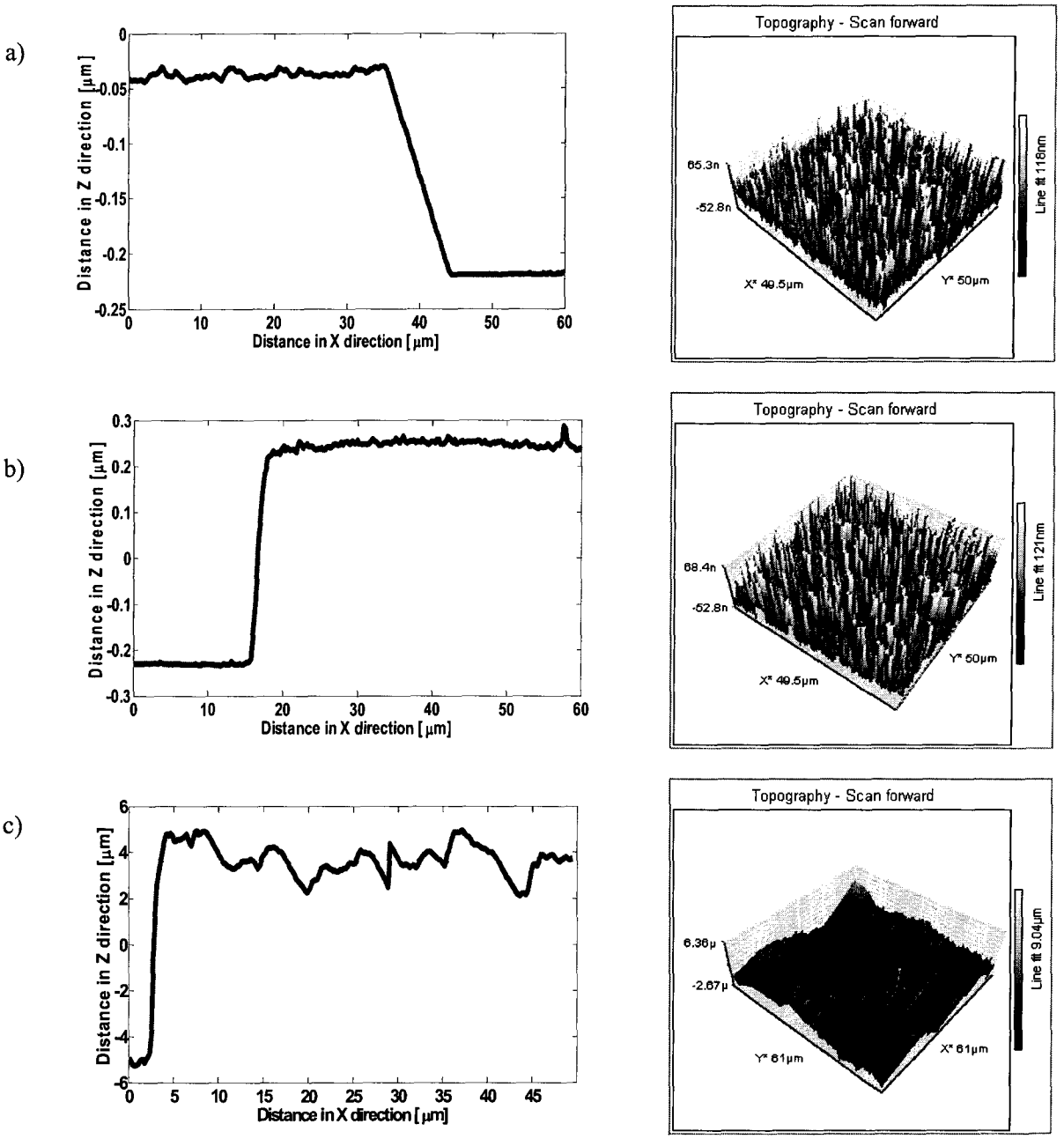

Figure 3-7. Measured Thickness and surface morphology for electrode 2 (R_{rms} ~ 29 nm), 3 (R_{rms} ~ 32 nm) and 4 (R_{rms} ~ 3.4 µm) respectively. As the polymerization charge increases the polymer film becomes rougher.

TABLE 3-I

SPECIFICATIONS OF THE TESTED ELECTRODES

Electrode #	1 (bare gold)	2	3	4
Deposition current	_	$100\mu A$	$100\ \mu A$	$1\ mA$
Deposition time	_	$80\ sec$	$160\ sec$	$10\ sec$
Polymer thickness	0	$150\ nm$	$290\ nm$	$\sim 10\ \mu m$
Polymer roughness (R_{RMS})	_	$29\ nm$	$32\ nm$	$3.4\ \mu m$

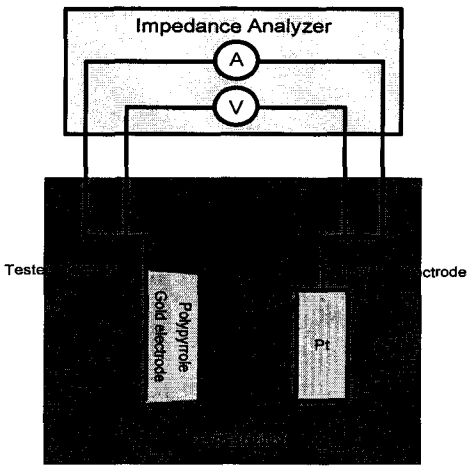

Figure 3-8. Four-point setup for measuring electrode-solution impedance. The measurements are done in an ionic solution to mimic the properties of cerebrospinal fluid. In-solution measurements allows for tracking the changes of double layer capacitance as the polymer roughness ins increased.

3.3.2 Electrical Properties

The electrical properties of the polymer-dopant film are evaluated using a four-point Agilent 4294A impedance spectrometer (Fig. 3-8). An alternating voltage v(ω) is applied to the samples through the inside leads and the resultant alternating current i(ω) is recorded by the outside leads. The impedance of the sample can be given by

$$Z(\omega) = \frac{v(\omega)}{i(\omega)} = |Z(\omega)|e^{i\theta(\omega)} \tag{3.3}$$

where θ is the phase angle and ω is the frequency. The samples are immersed in a 0.1M phosphate buffered saline (PBS) solution (PH 7.3, conductivity 27.9 mS) which is composed of potassium phosphate dibasic, potassium phosphate monobasic and NaCl in distilled water. This solution is used to keep the polymer film hydrated and approximates the physiological environment. An alternating voltage with a spectrum of frequency in the range of 40 Hz to 1 MHz is applied to the electrodes in order to characterize the electrode-solution interface impedance. The electrodes are fabricated on the same substrate to reduce the impedance measurement errors due to relative movement of samples inside the solution. Also the measurements are repeated with the three identical sets of electrodes and the results are averaged. The black lines in Figs 3-9 and 3-10 illustrate the average magnitude and phase of electrode-solution impedance for each of the electrodes versus frequency, respectively.

By integrating the value of resistors R_{PPy} and capacitors C_T along the area and thickness of the deposited polymer, we can further simplify this model to a resistor R_S in series with paralleled capacitor C_{total} and resistor R_{total} , where C_{total} and R_{total} are the total double layer capacitance and polymer resistance, respectively. It is important to note that here; R_{total} is due to both ionic and electronic conductance mechanisms. The value of R_S can be found by adding the calculated resistance of transmission line made by solution between the tested electrode and reference electrodes to the measured resistance of the setup contacts. By knowing R_s we can extract C_{total} and R_{total} from the resistance, capacitance and inductance which has been measured by the impedance analyzer. The dotted lines in Figs. 3-9 and 3-10 show the simulation results which have been performed to validate the simplified model based on R_s, C_{total} and R_{total}.

From Figs. 3-9 to 3-11, it can be concluded that the total resultant capacitance increases with deposition current density (a thicker film). This may be due to transition of the surface morphology from a smooth state in electrodes 2 and 3 to a "valley and mountain like" structure in electrode 4.

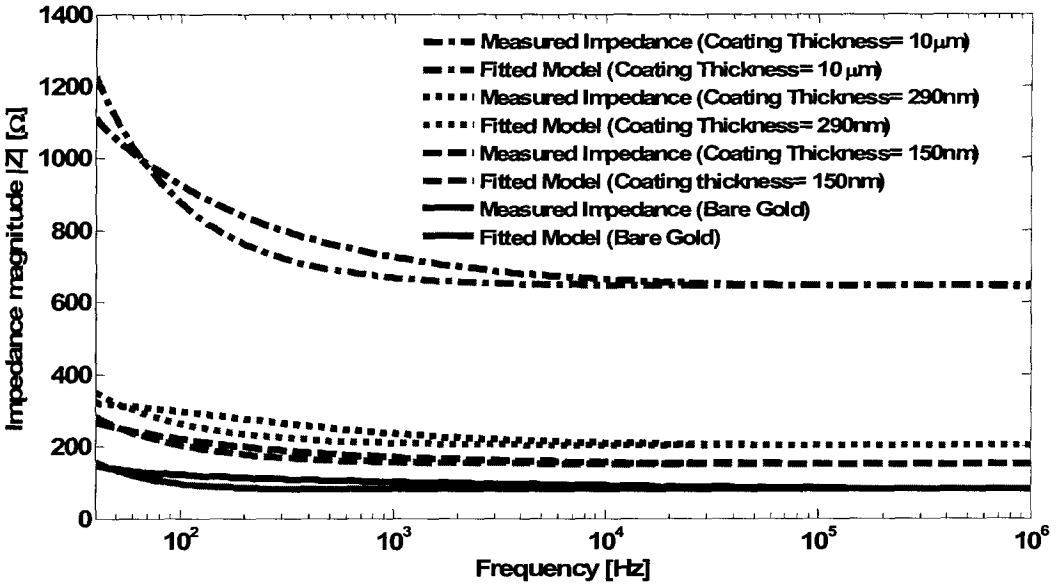

Figure 3-9. Measured (black) and simulated (red) impedance magnitude of electrodes 1, 2, 3 and 4. The impedance of the polymer film has a nonlinear relationship with the thickness of the polymer. Although the polymer in electrode 4 is ~35 time thicker than in electrode 3, the RMS resistance is ~5 times higher.

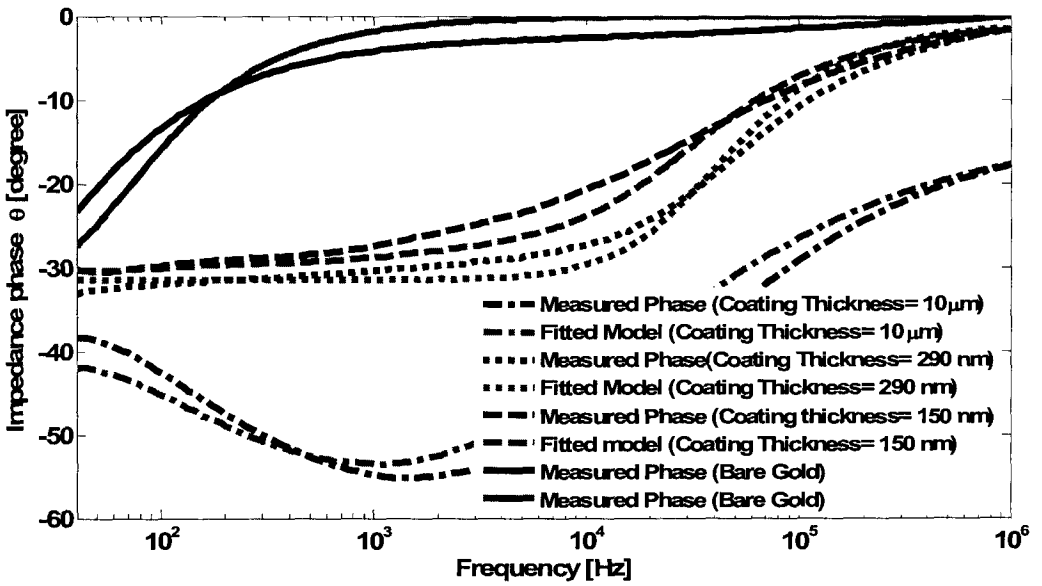

Figure 3-10. Measured (black) and simulated (red) impedance phase of electrodes 1, 2, 3 and 4.

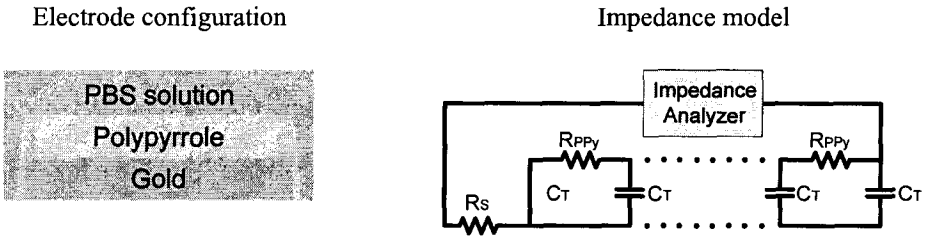

Figure 3-11. The schematic and simplified impedance model of the polymer film. R_s is composed of the resistances of the solution, polymer-electrode contact, and measurement leads-electrode contact which are in series. R_{PPy} and C_T are the unit resistance and capacitance of the polymer film and double layer respectively.

Also, in Fig. 3-9 it is observed that the impedance magnitude, |Z|, and frequency have an inverse relationship. When the frequency of operation increases, the impedance of the capacitors C_T reduces, resulting in the drop of total impedance. To investigate the effect of pad area on the electrode impedance, working electrodes with areas of 0.2 cm^2 and 0.4 cm^2 were used. The charge density is scaled in a manner to achieve an average polymer thickness of 150 nm for both sets of samples. The electrodes were tested with the same setup shown in Fig. 3-8. As the area of the reference electrode was several times larger than the working electrode, small difference was observed between the cell impedance with either of working electrodes. The effect of the pad size is attenuated due to two reasons: First, with thin (nm range) polymer coatings, the resistance of the solution dominates the impedance of electrode. Second, if we consider the distance between the working and reference electrode as a transmission line, doubling the area of the working electrode has a minimal effect on the resistance of the transmission line (distance between the electrodes is also important). Therefore, to have a fair comparison in Figs. 3-12 and 3-13, we normalized the solution resistance to a uniform transmission line with a cross section area equal to the area of working electrode in each case.

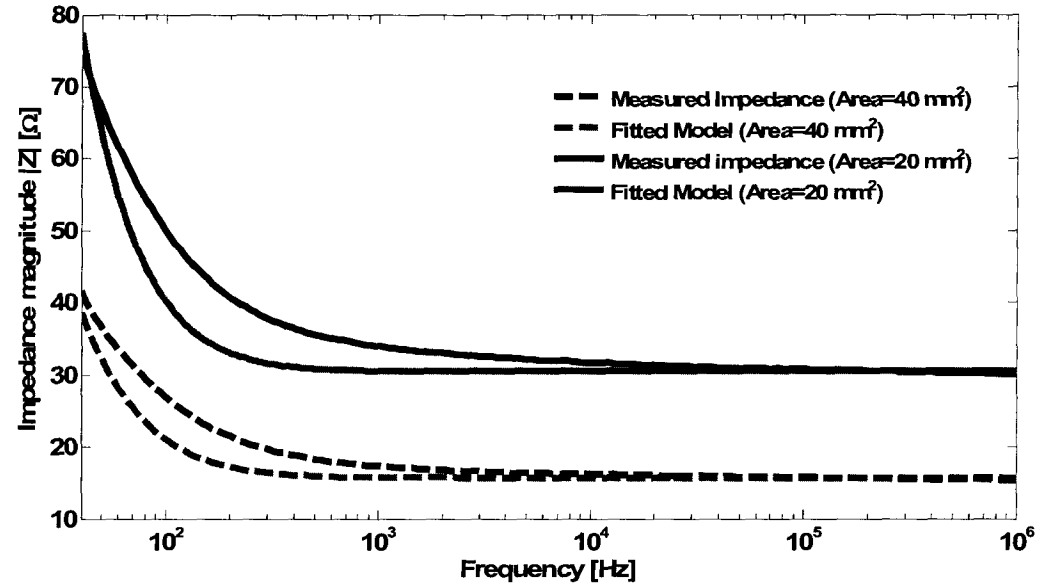

Figure 3-12. Measured (black) and simulated (red) impedance magnitude of electrodes with 0.2 cm^2 and 0.4 cm^2 active area. The attenuating effect of the inhomogeneous transmission line between the working and counter electrodes is de-embedded from the results.

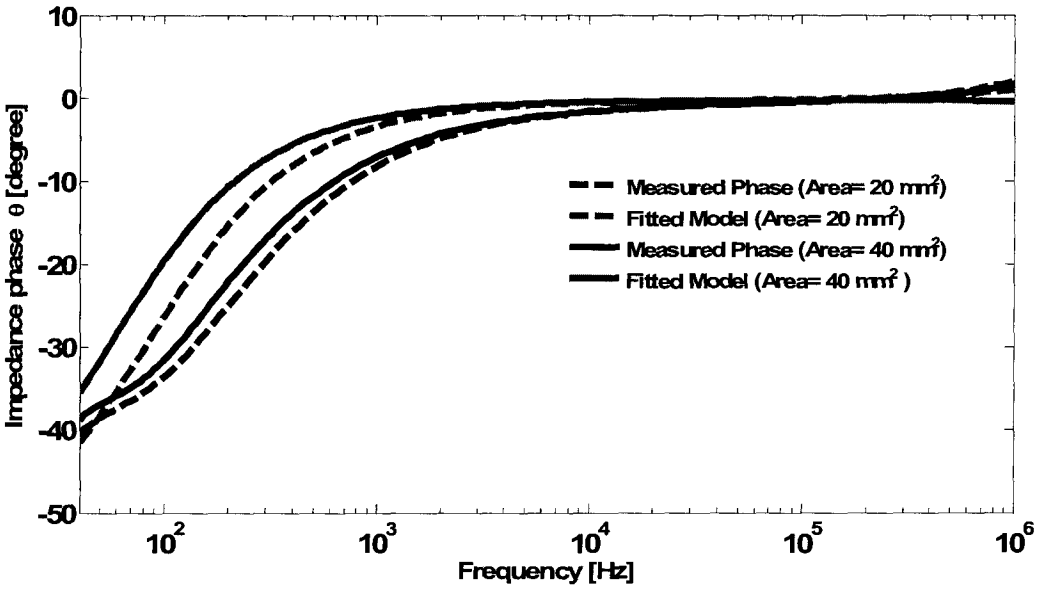

Figure 3-13. Measured (black) and simulated (red) impedance phase of electrodes with 0.2 cm^2 and 0.4 cm^2 active area.

To compare the results, the rms (root mean square) value of the impedance magnitude, |Z|, is calculated across the measurement bandwidth. Measurement results confirm an inverse relationship between the area and |Z|, unlike the relationship between the polymer thickness and |Z| which is highly nonlinear due to the properties of PPy and its double layer capacitance. Typical neural action potentials have amplitudes up to 500 μV when recorded extracellularly, with energy in the 100-Hz–7-kHz band [16], for such signals a 290 nm polymer coating can increase the initial impedance of the recording electrode up to 40%. This effect gets aggravated for low- frequency local field potentials (LFP) which have amplitudes as high as 5 mV and contain signal energy around 1 Hz [19]. The fact that the amplitude of LFP signals is one order of magnitude higher than that of neural action potentials may compensate for the increased signal attenuation and keep the SNR in an acceptable range. In summary, several factors such as the desired amount of drug in polymer reservoir, required SNR, amplitude of the specific type of neural signals which are going to be recorded and performance of the amplification circuits should be considered to choose an appropriate thickness of polymer-dopant film. At last, it is important to mention that the impedance of polymer coatings on all electrodes were measured at the as-grown state, where generally the impedance of the conductive polymers is higher than their cycled state [4].

3.4 Limitations of the Proposed System

In the previous section we discussed the effects of the surface modification coating (PPy film) on the recording performance of a neural probe with the proposed configuration (Fig.3-6). Yet, the main obstacle in the implementation of an electrically controlled drug release system is the side effects of the applied control voltage in the dopant release phase. Because the human body is a low resistance

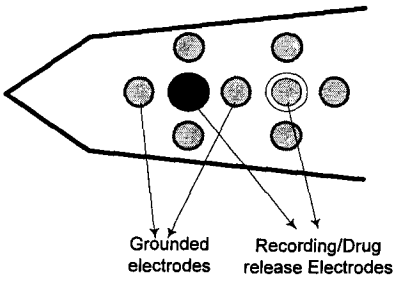

Figure 3-14. Proposed schematic of a neural probe to avoid undesired stimulation of neurons during dopant release phase. Additional electrodes are located around the main electrodes which are grounded while the dopant release signal is applied.

conductor (usually modeled with a 1 kΩ/m resistance), and because our nervous system functions electrically, currents which their amplitude is above a certain threshold can distort the physiological function of neurons. To stimulate a population of neurons it is necessary to have sufficient charge flow through them. While a minimum of 10^{-6} C charge is needed to initiate neural stimulation when applied through skin, in our case where we are operating inside nervous tissue, this number tremendously gets reduced to 10^{-12} C [5].

The circuitries of a neural probe share a single ground which is in the form of a screw which gets implanted in the vicinity of the neural implant. Therefore, during the drug release phase, neurons which are located in the vicinity of probe-to-ground path are prone to stimulation; an effect which is highly undesired. Such a low threshold is the major challenge of controlling the drug release rate using an electrical signal, which generally has alternating amplitude in the range of -1 V to 1V. A potential solution for this problem is shown in Fig. 3-14. We address this problem by adding grounded bare gold pads around the original polymer coated pads to decrease the leakage current to the adjacent nervous tissue. A similar design has been used in cochlear implants to measure the signal propagation inside tissue and resolve the crosstalk issue between stimulating and recording electrodes

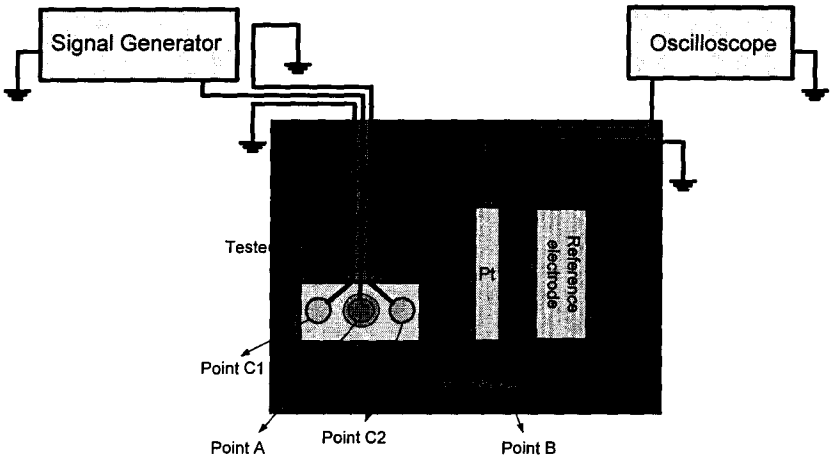

Figure 3-15. Test setup to characterize the effect of the grounded pads on the amount of current leaking into the solution. The platinum electrode (point B) is connected to a high impedance oscilloscope to measure the difference of the detected voltage between the cases where points C_1 and C_2 are floating or grounded.

[37]. To validate our solution we used the test setup shown in Fig. 3-15. The medium is a PBS solution with the properties reported in section 3.1. A sinusoidal signal is applied to the solution through a polymer coated pad (point A) and the signal is recorded at a 1 cm distance from point A (point B). Then two bare gold pads (Points C_1 and C_2), each located at 0.2 mm of the original pad were grounded and the signal amplitude is recorded again at point B. It is observed that the grounded pads highly attenuate the signal which is recorded at point B (Table 3-II). A reference electrode is used in the solution as a common between all devices (point C). The ratio

$$\frac{Distance\ between\ points\ A\ \&\ B}{Distance\ between\ point\ A\ and\ (C_1\ or\ C_2)} \tag{3-4}$$

is a decisive element in the attenuation factor as they have a linear-like relationship. To determine the correct value of Eq.3-4 the closest neuron to the electrode pad should be considered point B. Based on the stimulation threshold of that particular type of neuron the desired attenuation ratio and thus points C_1 and C_2 can be determined. Although the results are promising, still wide range of *in vivo*

Table 3-II

MEASUREMENT RESULTS FOR THE PROPOSED SETUP

Location in setup	Voltage[1] before grounding $C_{1,2}$	Voltage after grounding $C_{1,2}$
Point A	10 Vp-p[2]	10 Vp-p
Point B	3.75 Vp-p	44.1 mVp-p

experiments are needed to determine the appropriate probe design and its effectiveness to reduce the current leaking into the nervous tissue and hence decrease the undesired stimulation side effects. We believe that this issue will be a fundamental part of the future research in the field of electrically controlled drug delivery.

3.5 Conclusion

The morphological and electrical properties of the PPy-dopant film are examined to investigate the potential attenuation of neural signals due to the polymer coating impedance. In an electrode with a 10 μm-thick polymer film (which is 200 times thicker than the previously proposed drug delivery coating in [4]), the kΩ-range impedance of the surface modification coating may be negligible as compared to MΩ-range impedance of the scar layer which engulfs the unmodified electrodes in chronic implantations.

The measurements made in this study used electrodes with areas from 4-40 mm^2. Typical microelectrodes may have an area of 4×10^{-4} mm^2. While interfacial capacitance and charge transfer resistance have an inverse relationship with the area of electrodes [38], further work is necessary to verify whether the results presented here can be generalized to microelectrods. For example, the

[1] Measurements were done at 1kHz.

[2] A very high test voltage is used to make the voltage (after grounding) at point B detectable by the oscilloscope.

current density is larger at the edges of the electrode. Future work will characterize the effect of higher deposition currents and smaller electrode area on the final polymer thickness. Also, the thickness and roughness of the polymer is dependent on the deposition solution, concentration of monomers and ambient temperature. In neural electrodes with a certain geometric shape and area, scanning methods such as AFM can give the average thickness of the deposited polymer. Therefore, the deposition charge can be calibrated to achieve the desired thickness.

CHAPTER 4

Neural Recording LNA Design

The circuits in a neural probe (Fig. 2-2) perform several tasks including amplification, signal processing, and wireless transmission of the recorded signals. Among these tasks, proper amplification of the neural signals is the most important task of an implantable neural recording system. The neural signals are generally very weak and their amplitudes vary from tens to hundreds of microvolts [16]. From the noise perspective, a high-quality low-noise amplifier reduces the noise requirements of the succeeding circuits.

From a size and power dissipation standpoint, a multi-channel recording system would require an amplifier for each channel , but only one multiplexer, transmitter, and set of biasing circuitry, so the most significant portion of on-chip power and area consumption will be due to the amplifiers. Due to the very low amplitude of neural signals and the SNR requirements of neural recording system, the low-noise amplifier should be the first block in the signal path. The significance of this arrangement is that the contribution of the following blocks to the overall system noise will be divided by the amplifier gain, as opposed to having one amplifier and sampling the data from different channels where the noise of multiplexer gets directly added to the recorded signal. Therefore, the overall reduction (or optimization) of noise, power consumption and area of the design is very dependent to the amplifier's design and layout. The challenges in the design of such an

amplifier will be discussed in this chapter. Due to the importance of the neural amplifier noise performance, we comprehensively discuss the design strategies and test-bench noise measurement in Sections 4.6 and 4.7, respectively.

4.1 Requirements for a Neural Amplifier

There are several designs proposed for biosignal amplifiers in the literature. These designs have typically addressed a few of the required characteristics for such biosignal amplifiers [39]-[48]. In general, there are several requirements from biomedical and electrical points of view that should be considered and traded off during the design.

The microvolt range of biosignals put a stringent requirement on the noise level of the neural recording system for producing an acceptable overall signal-to-noise-ratio (SNR). One representative figure-of-merit for biosignal amplifiers is the input-referred noise which, when integrated over the frequency band of interest, should be lower than the extracellular background noise of 5-10 μVrms [42].

As the neural low-noise amplifier is located at the front end of the system, the intrinsic noise of amplifier has a direct impact on the overall noise of the neural recording. The amplifier adds noise to the recorded signals through the thermal noise and flicker (1/f) noise of its components. Besides the contributed noise by the transistors and resistors in the amplifier, the interference noise from the digital on-chip circuitry and the coupling noise, e.g., through the parasitic capacitances in the substrate or between interconnects, should also be considered. One way to minimize the effect of these additional noise sources is to have a fully-differential architecture for the amplifier [42] [44].

Another important requirement for biosignal amplifiers is that they must be able to reject large DC offsets. The dc potential generated the neural tissue interface which is engulfed by the

saline cerebrospinal and the electrode tips of neural probe can be as high as ± 50 mV [42]. If this DC potential reaches the amplifier inputs, the outputs will become saturated which will leave the amplifier nonfunctional.

The next requirements relate to the die area of the amplifier. As the number of amplifiers increase with number of recording channels, the area of the amplifier must be minimized in order to minimize the overall size of the neural recording system. There are several capacitors used in the design of neural amplifier and it is crucial to properly choose their values and structure.

Power dissipation of each amplifier should be kept below a certain limit from both biomedical and electrical points of view: to reduce the thermal effects and to increase the lifetime of neural recording system. Minimizing amplifier's power consumption is especially important when several amplifiers in a close proximity of neural tissue are used (as in neural recording system). Typical neural probes have tens (and recently up to hundreds) of electrodes [46] with an amplifier dedicated to each electrode. Hence, the power consumption of the neural recording system increases with the number of amplifiers. A heat flux of 80 mW/cm^2 can cause necrosis in the neural tissue [42]. This biological concern defines a strict limit to the power consumption of each amplifier in addition to the circuit-level limits. This results in a compromise between power consumption level and other design parameters (i.e., noise). There is a tradeoff between noise and power; the amplifier noise level is generally reduced as its power consumption increases. Lower power consumption also allows for a longer battery life, yet the biomedical limit for power dissipation is usually much more strict and hence the bottleneck of the design [46].

Another important parameter of the amplifier is its bandwidth. Typical neural action potentials have energy in the range from 100 Hz to 5 kHz [19], while local field potentials can contain signal energy below 1 Hz yet above DC to reject the dc interface potentials [42]. In this chapter, we will propose to have yet another function for the neural amplifier which allows processing of higher

frequency signals for the purpose of tissue-electrode interface impedance measurement. For this function, we need a relatively high cutoff frequency in the range of 50 to 100 kHz [3], yet we split the bandwidth to two separate modes in order to prevent unnecessary high-frequency noise from being amplified by the neural signal amplifier.

Another important characteristic of the design is the supply voltage of amplifier and other electrical components of the neural recording system. As an ideal neural recording system system is intended to be implantable, the embedded circuitry should be powered by a battery thus the low-voltage design of electrical components would be a great advantage. Also, as most of neural recording devices are used as subcutaneous implants, a lower supply voltage provides a safer operation environment and avoids neural shock hazards, e.g., in the presence of an unexpected leakage current. Previous neural amplifiers reported in literature are powered with various supply voltages in the range of 5V to 1.8 V. Some of them are 5 V [39] [42], 3.3V [44], 3V [47], 2.8 V [46], and 1.8 V [48]. The proposed neural amplifier uses a 0.5 V supply.

4.2 Ultra-low-voltage Analog Circuit Design

The scaling phenomenon in semiconductor industry has reduced the manufacturing costs and increased the functional density. The supply voltage shrinks as the device size is reduced. As the semiconductor technology node moves into nanoscale range, the traditional amplifier topologies will not fit into the strict requirements imposed by sub-1V power supplies; thus, ultra-low-voltage designs and biasing methods are needed. In this section, we discuss the methods, challenges and limitations of designing CMOS circuits (specifically amplifiers) with a 0.5 V supply voltage. Then, in Section 4.4, we will utilize these methods to design and layout a gate-input 0.5 V operational

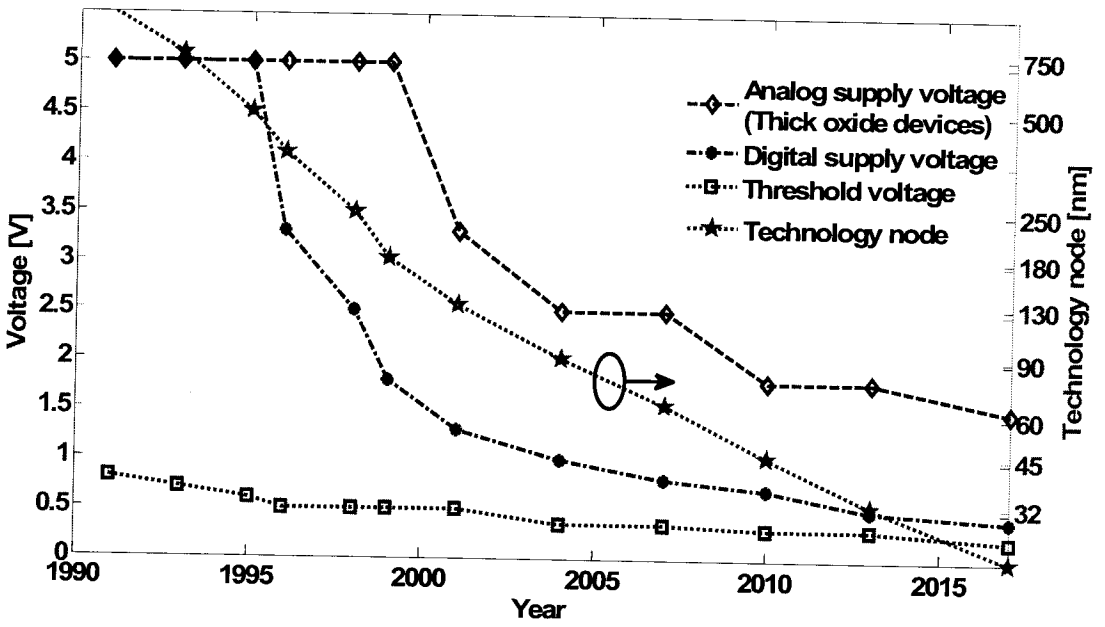

Figure 4-1. Simultaneous shrinkage of supply voltage, technology node and threshold voltage.

transconductance amplifier based on substrate-biased standard devices in a 0.18 μm CMOS technology. Based on the same methods, robust biasing circuits will be developed to bias the amplifier less dependent on temperature, fabrication and operation condition variations.

4.2.1 Motivation for 0.5 V Design

Modern system-on-chips require integration of analog and digital circuits together on the same chip. According to International Technology Roadmap for Semiconductors (ITRS), digital circuits operate with lower voltages as their device dimensions decrease. As shown in Fig. 4-1, a 0.5 V power supply voltage is anticipated for digital circuits in 35 nm technology. More important is the fact that the shrinkage of supply voltage for sub-micrometer technologies is mainly due to device breakdown and reliability concerns as well as power dissipation. Therefore, it may not be possible to internally boost the external low-voltage power supply [49].

As analog integrated circuits provide the interface between digital signal processing (DSP) systems and the physical world, their supply voltage should be reduced in accordance with the supply voltage of the digital part to ensure efficient use of the chip's DSP power in mixed-signal designs. This would be highly beneficial for an integrated neural recording system which has analog blocks such as amplifier and transceiver as well as digital section for drug release control, tissue-electrode impedance measurement and processing/filtering of the recorded signals. For digital circuits of an SoC, supply voltage scaling is highly beneficial as it quadratically reduces the power consumption. Based on the demands and requirements of both VLSI and biomedical technologies, the need for an ultra-low-voltage amplifier/circuitry is greatly increasing in the field of neural signal recording for two main reasons: first, the continued technology scaling of CMOS into sub-microscale dimensions to increase the speed and density of the devices; and second, to maintain reliability, enhanced battery-powered operation, and to reduce the risk of neural shock hazards and thermal effects (such as tissue necrosis) in bio-implant SoCs [50].

In general, different techniques have been reported in literature to lower the required supply voltage of analog circuits. Among these techniques are Miller compensated multi-stage amplifiers [51] [52], back-gate driving [53], clock voltage boosting [54], level-shifting [55], the switched-opamp method [56] and rail-to-rail input opamps [57] [58]. Several amplifiers operating down to 0.9 V and recently 0.5 V have been demonstrated [59] [60]. The values presented in Sections 4.2.2 to 4.2.4 are typical for a standard 0.18 μm technology.

4.2.2 Low-Voltage Operation of CMOS Devices

For fast sampling and high bandwidth applications, CMOS devices should operate in the strong inversion region, hence $(V_{GS} - V_T) > 0.2$ V [61]. In saturation region, while $V_{DS} > V_{DS,sat}$ and $V_{DS,sat} = (V_{GS} - V_T)/\alpha$, the device performance would be close to a transconductor or voltage-controlled

current source. While operating close to the strong inversion region, $V_{DS,sat}$ would be around 0.15 V and α is in the range of 1 to 1.5 [61]. To achieve low power consumption, high transconductance and high current efficiency, CMOS devices should be operated in weak inversion region, hence $(V_{GS} - V_T)$ < -0.05 V or -0.1 V. The drawback of this strategy is limited bandwidth of the device. Under these circumstances we need at least a minimum drain-source voltage of about 0.1 V to 0.125 V to remain in saturation [61].To have a safe margin in the design, V_{DS} is usually set to 0.15 V. While this requirement is independent of the threshold voltage of the device, we should keep V_T in range of 0.2 to 0.3 V (through biasing the device body) to guarantee satisfactory turn-ON/turn-OFF properties.

4.2.3 Obstacles of Ultra-low-voltage Design

A relatively high threshold voltage in CMOS devices is a major obstacle for the performance of analog circuits with ultra-low supply voltages down to 0.5 V. In addition, smaller available signal swings due to the low supply voltage leads to a higher power consumption in reducing the errors such as thermal noise and offset voltages [49]. High-speed analog circuits require devices with very low over drive voltage, biased in moderate or strong inversion. However, this is not a major problem in low-frequency biomedical circuits. In traditional designs, the supply voltage should be larger than signal swing plus threshold voltage plus several saturation drain-source voltage, $V_{DS,sat}$, or larger than signal swing plus several $V_{DS,sat}$. The task of designing analog building blocks with a 0.5 V supply voltage is challenging as conventional design methods are confined by the extremely low voltage headroom. This problem can be addressed from two perspectives: one is enhancement of fabrication technology and the other is circuit- level modifications. From manufacturing perspective, the solution is to

use a process that supports thick-oxide devices. Unlike normal devices, these have been moderately scaled [49]. The drawback is having slower devices due to the oxide barrier.

Another technology option is to use devices with low or zero threshold voltage which provide additional voltage headroom in circuits [49], yet low-threshold devices require extra masks and fabrication steps which makes the fabrication process more costly and time consuming. As the analog blocks generally occupy only 5 to 25% of the layout in VLSI systems, it would be hard to economically justify the additional process cost in mass production. Also, compared to normal devices, the characteristics of zero threshold devices are usually not constant and reproducible through fabrication and from die to die [59]. Considering the problems affiliated with an unconventional process, to design an ultra-low voltage neural amplifier, we use circuit-level design techniques along with a standard fabrication process.

4.2.4 Advantages of Ultra-low-voltage Operation

Besides the challenges of ultra-low-voltage design, operating near the threshold of devices in a particular technology has some benefits from both Biomedical (discussed in Section 4.1) and circuit-level points of view. One advantage of operating with an ultra-low supply voltage (i.e. $0.5\,V$ for $0.18\mu m$ technology) is elimination of parasitic bipolar effects in the circuit. We can utilize this phenomenon to forward bias the body-source junction of devices to reduce their threshold voltage V_T [61]. Unlike the traditional CMOS designs where the body of pMOS and nMOS devices are connected to V_{DD} and ground respectively, in low-voltage design, biasing the body terminals of all devices offers the choice of two design approaches: first, the signal can be applied to the body of the device whereas the gate is used to bias the device; second, we can apply the signal to the gate and use the body to control the bias of the device [61]. We exploit the second technique to design our gate-input OTA.

In a traditional n-well process only the substrate of pMOS devices could be accessed, yet modern CMOS processes offer a deep n-well option to engulf the nMOS device so that its body can be biased separately from the bodies of other nMOS devices. We utilize this feature in our layout to bias the body of each nMOS device with a certain voltage.

Although in general most of a biomedical circuit building blocks do not necessitate the high speed and hence required technology scaling as of other analog devices, the cost and integration constraints call for fabrication of the low-speed blocks (i.e., amplifier) on the same die and technology as the high-speed blocks (i.e., transceiver). One way of addressing this problem is through decreasing the operation supply voltage and operating the devices in the subthreshold region. Therefore, ultra-low-voltage operation would be specifically helpful in biomedical circuits designed in technologies below 90 nm.

4.3 Amplifier Design

The long-term, chronic response to an implanted array features a compact fibrous capsule that surrounds the device. This scar tissue isolates electrodes mechanically and electrically, and the thickness of this capsule and signal longevity can vary widely between electrode shanks in a single array [10], [11]. Electrical impedance spectroscopy can be used to characterize the structure of biological tissues. The frequency-dependent impedance arises from the presence of interfaces such as cell membranes which separate the conductive intracellular and extracellular spaces. The increased density of glial cells in the scar tissue could decrease the fraction of conductive extracellular medium, increase the capacitive component, and increase the overall tissue impedance around the implanted electrode.

Although it is common to report electrode impedance at 1 kHz, a sweep through wider frequency range up to 100 kHz will give information about the electrode-tissue interface as well as

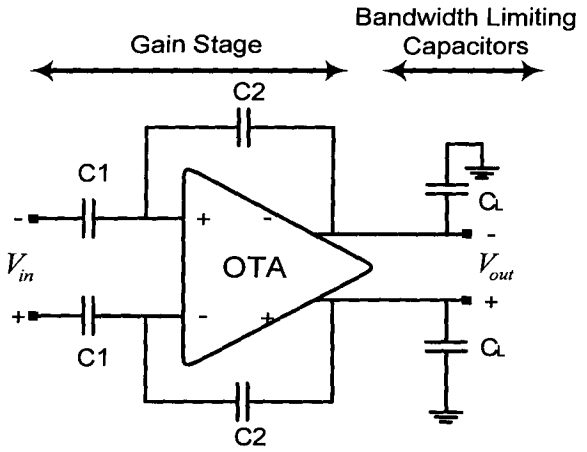

Figure 4-2. Schematic of fully differential biosignal amplifier. Capacitor C1 rejects the DC signals generated at the electrode-tissue interface. The capacitive feedback results in a substantially lower input-referred noise level compared to a resistive feedback

the tissue surrounding the implant [3]. Monitoring this impedance *in vivo* could permit compensation for eventual signal attenuation. One technique for measuring this impedance is to inject a test current with frequency from 10 mHz to few tens of kHz to the contact and perform the impedance measurement based on the recorded signals from the site [50]. In this case, the recording amplifier should accommodate the extended bandwidth required for such stimulation so that the resulting signals can be properly recorded. On the other hand, for recording neural signals, the high-pass cutoff frequency of the gain stage should be kept around 5 kHz or below (based on the type of neural signals) to achieve a low input-referred noise. Our design features bandwidth limiting capacitors C_L following the gain stage to form the passband of the amplifier based on the application . By changing the value of C_L, it is possible to adjust the amplifier's high-frequency cut-off point (and thus its bandwidth) for either neural recording mode (1 mHz to 5 kHz) or impedance measurement mode (1 mHz to 60 kHz). The simplified schematic of the biosignal amplifier is shown in Fig. 4-2. Using

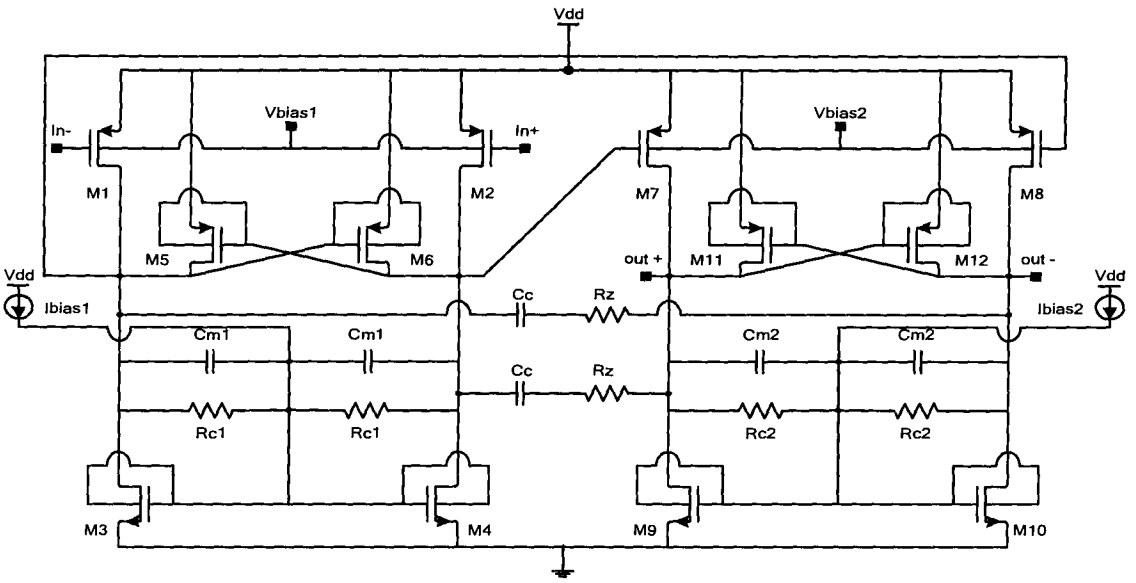

Figure 4-3. Schematic of the low-voltage OTA used in the amplifier. Two stages have been cascaded to increase the open loop gain. In this schematic the bodies of all devices have been biased to control the threshold voltage of devices.

capacitive feedback enables the rejection of large DC offsets at the tissue-electrode interface. The midband gain of the amplifier is set to ~40 dB by choosing C1/C2=100.

4.4 OTA Design

Typical supply voltage for a CMOS analog circuit designed in standard 0.18 μm process is 1.8 V which increases to 3.3 V in thick oxide 0.18 μm process. In this technology, the threshold voltage $|V_T|$ of pMOS and nMOS devices are 0.34 V and 0.41 V, respectively. Therefore, for ultra-low-voltage operation in the standard process, we choose a supply voltage of 0.5 V which is very close to the threshold of the devices. Figure 4-3 shows the schematic of the OTA. The structure is similar to the low-voltage OTA architecture presented in [60]. However, by eliminating the need for a resistive level shifting feedback configuration and proper device sizes and values, our amplifier's noise

performance is substantially improved compared to that of [49]. In [60], the input transistors of OTA, M1 and M2 were biased through resistive level shifters in amplifier's feedback configuration. Instead, we have biased the gates of these devises through the constant current drawn by current source loads, M3 and M4.

Input transistors M1 and M2 are pMOS devices which have less 1/f noise than nMOS transistors. Special attention has been paid to sizing of these transistors to reduce their noise contribution while maintaining sufficient g_m and therefore desirable gain of the OTA. The OTA consist of cascade of two similar stages to provide a sufficiently high gain. Given that the nominal supply voltage of the circuit is 0.5V, to maximize the output signal swing, the common-mode voltage level of V_{out} is set to 0.25 V.

As in 0.18 μm CMOS process, pMOS transistors have a $|V_T|$ of ~0.5 V, to make sure that input transistors are sufficiently turned on, their body source junction is biased to lower the V_T of transistors. As a 0.5 V supply is used for operation, the risk of forward-biasing of the junctions is minimized since the parasitic bipolar devices cannot be activated even with the overall power supply [61]. Vbias1 and Vbias2 are used to bias the bodies of input transistors in the first and second stage, respectively. This results in lowering the V_T by about 100mV. Resistors Rc1 detect the first stage output common-mode voltage which is fed back to the gates of M3 and M4 to achieve a good CMRR and a common-mode gain smaller than one. Transistors M5 and M6 act as a differential negative conductance and decrease the output conductance thus increasing the differential gain. These transistors act as diode-connected devices for common-mode signals. The differential and common-mode gain of each stage are given by

$$A_{diff} = \frac{g_{m1}}{g_{ds1} + g_{ds3} + g_{ds5} - (g_{m5} + g_{mb5}) + 1/R_{C1}} \tag{4-1}$$

$$A_{cm} = \frac{g_{m1}}{g_{m3} + g_{mb3} + g_{m5} + g_{mb5} + g_{ds1} + g_{ds3} + g_{ds5}} \tag{4-2}$$

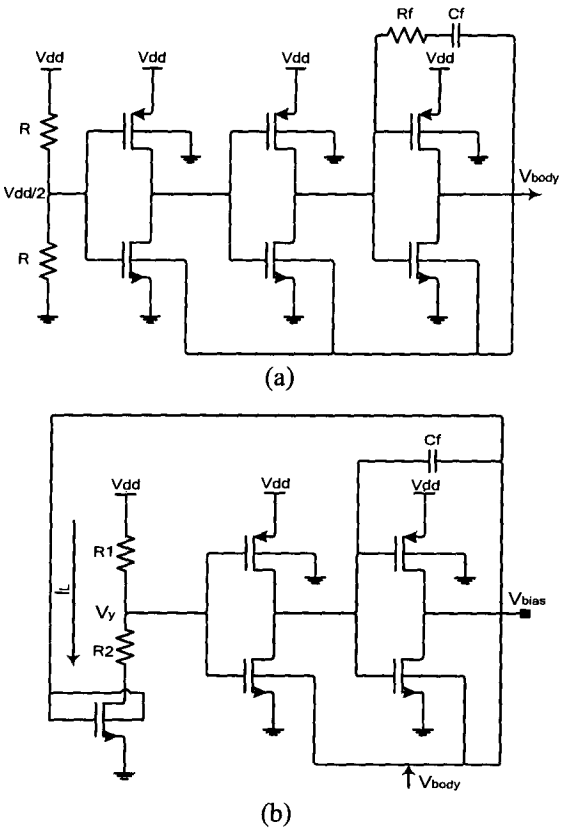

Figure 4-4. (a) Control circuit to fix the switching threshold voltage to VDD/2. (b) Circuit generating the bias voltage.

where g_{mi}, g_{mbi}, and g_{dsi} denote the transconductance, bulk transconductance, and output conductance of device Mi, respectively. Cc and Rz are used for Miller compensation to achieve 55° of phase margin (Rz is used to move the zero due to Cc into the left half plane).

4.5 On-Chip Biasing Circuits for the OTA

Biasing circuits are required for reliable and appropriate operation of the OTA. The biasing circuits should operate robustly in the presence of process, supply voltage, and temperature variations. The OTA architecture presented in Fig. 4-2 needs two biasing voltages and two current sources. Bias voltages Vbias1 and Vbias2 set the body potential of the input devices of first stage (M1 and M2) and

second stage (M7 and M8), respectively, to control the DC level of output at each stage. The forward biasing of the body-source junctions of these devises ensures the reduction of their threshold level and improves their inversion level. As the OTA operates with an ultra-low supply voltage, there would not be enough voltage to forward-bias the body-drain and body-source junctions, hence no risk of latch-up effect [62]. The current Ibias1 is used to generate a voltage drop over resistors Rc1 to bias the body and gate of M3 and M4 at 0.4V. In the same way Ibias2 is used for biasing M9 and M10.

Similar to [49], we use replicated difference amplifiers (DAs) accompanied by active feedback loops to design reliable biasing circuits. Fig. 4-3(a) shows the schematic of the control circuit composed of three identical DA stages, which is used to set the switching threshold of the other error amplifiers used in the biasing circuits to $V_{DD}/2$, independent of operation and fabrication parameters. The input of each inverter is compared with its switching voltage and the difference is amplified. In the control circuit, each inverter compares the input voltage to its own switching threshold voltage and amplifies their difference. This is done through connecting the bodies of nMOS transistors in a negative feedback configuration. If the switching threshold of DA1 is less than $V_{DD}/2$, the input voltage of DA2, the output voltage of DA3 and the body voltage of nMOS transistors decrease. This results in an increase of the switching threshold. In the same manner if the switching threshold is greater than $V_{DD}/2$, the feedback operates to compensate for it. Stability of the control circuit is guaranteed by accurate selection of resistor R_f and capacitor C_f .

The output of control circuit (V_{body}) is applied to the bodies of the nMOS devices in the biasing circuits (Fig. 4-3(b)) where each DA compares its input to the already fixed threshold level $V_{DD}/2$ to set the switching threshold voltage of each inverter to $V_{DD}/2$. The current I_L is drawn by transistor M_{sink} to create a voltage drop across the resistors. By controlling the *W/L* ratio of this device, I_L can be set to make the desired biasing voltages Vbias1 and Vbias2. A replica of this circuit

is used to drive the gate of a pMOS current source to generate Ibias1 and Ibias2. The compensating capacitor C_f is used to stabilize the circuit [61].

4.6 Noise Analyses of Neural Amplifier

One of the most important requirements of the amplifier in an implantable device is that its noise should be limited to a very low level. Since the signals being amplified are on the order of microvolts, the noise added by the amplifier must be minimized to avoid corrupting the signal to be amplified. The standard requirement for noise is that the input-referred noise level of the amplifier should be less than the typical extracellular neural background noise of 5-10 μVrms [42], [44].

Flicker noise (1/f noise) and thermal noise are the major noise mechanisms in analog CMOS circuits. In a semiconductor, thermal agitation of electrons (or charge carriers in general) results in thermal noise. This noise is in dependent of voltage applied to the device and with a good approximation, we can assume its spectral density as constant for frequencies up to THz. For a resistor, the thermal noise spectral voltage and current density are given by

$$V_R^2(f) = 4kTR \tag{4-3}$$

and

$$I_R^2(f) = \frac{4kT}{R} \tag{4-4}$$

respectively, where T is the temperature in Kelvins, k is Boltzmann's constant (1.38×10^{-23} J/K), and R is the resistors value. As in Eq. 4-3, the charge fluctuations and hence, thermal noise voltage density increases with the rise of temperature.

For CMOS devices, their thermal noise is different based on the region of operation. For saturation region we have

$$I_D = \frac{W\mu C_{ox}}{2L}(V_{GS} - V_T)^2 \tag{4-5}$$

where C_{ox} is the gate capacitance (F/m^2). From Eqs. 4-5 and 4-4 we can write the noise spectral current density as

$$I_n^2(f)\ (I^2/Hz) = 4kTg_m\kappa \tag{4-6}$$

and κ is the unitless gate coupling constant in saturation region. A typical value for κ in 0.18 μm technology is 2/3 [42], [62]. In the same manner, for triode region we have

$$I_D = \frac{W\mu C_{ox}}{L}[V_{DS}(V_{GS} - V_T) - \frac{V_{DS}^2}{2}] \tag{4-7}$$

hence, from Eqs. 4-4 and 4-7 we have

$$I_n^2(f)\ (I^2/Hz) = 4kT\left[\frac{\mu C_{ox}W}{L}\left[(V_{GS} - V_T) - \frac{1}{2}V_{DS}\right]\right] \tag{4-8}$$

Flicker noise is the other major noise source in CMOS devices which gets added to the signal and further degrades the SNR. Flicker noise, also known as 1/f noise, is explained through various effects such as charge trapping in CMOS device channel, or imperfections and impurities in the gate of device. The spectral voltage and current density of the flicker noise have an inverse relationship with frequency and can be given by

$$V_n^2(f)\ (V^2/Hz) = \frac{K}{WLC_{oxf}} \tag{4-9}$$

and

$$I_n^2(f)\ (I^2/Hz) = \frac{K}{f}\frac{g_m^2}{WLC_{ox}} \tag{4-10}$$

Respectively, where K (C^2/m^2) is dependent on the fabrication process. The low-frequency noise of a CMOS analog circuit is usually dominated by the flicker noise. An important characteristic of COMS devices and circuits is their 1/f noise corner. The input signals which have a frequency below the 1/f noise corner will be highly distorted by the circuit noise. In the very-low frequency circuits such as neural amplifiers, it is of a great importance to design the corner frequency as low as possible.

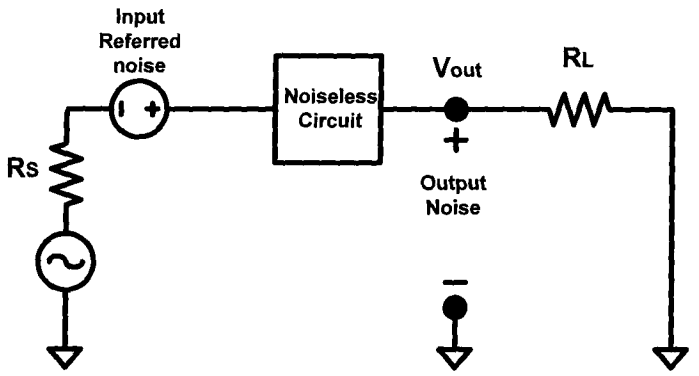

Figure 4-5. Equivalent input noise of a circuit.

In addition to the noise sources intrinsic to the transistors, we must also consider interference noise from the rest of the chip. Switching transients of digital circuits can be coupled into the analog circuitry through parasitic capacitances of the substrate or between interconnects. This type of noise can be minimized by using fully-differential architectures.

4.6.1 Analysis of Input-referred Noise

Input-referred noise is probably the most important figure-of-merit in a neural amplifier [42] [46] as it de-embeds the effect of amplifier gain on the reported noise voltage. Hence, it is used to compare the SNR of neural amplifiers with different gains for a given type of neural signal. A comprehensive explanation of its measurement methods is given in Section 4.7. In this section, we will discuss the theory behind it and analyze this figure for our neural amplifier.

For a given output noise spectrum, the equivalent input noise, or input-referred noise expressed in$V/\sqrt{Hz}$ unit, is the noise that if applied to the input of the circuit element specified as input would produces the same output noise assuming the circuit loading conditions were unchanged. The fact that we refer the circuit's intrinsic noise to its input gives us the ability to compare the input signal with the circuit noise level at the input; hence we can quantify the distortion of the input signaldue to the circuit noise. As shown in Fig. 4-5, the amplifier is considered noiseless and its noise

is represented by a noise source in the input which includes the noise of the amplifier and its load together. From the output perspective the noise of this model is equal to that of the original amplifier.

In the differential OTA topology of Fig 4-3, the noise sources are independent. Therefore, we can terminate the inputs of the OTA and calculate the total noise through superposition of the noise voltage in the outputs [62]. We can modify Eq. 4-6 for the CMOS devices in the first stage of the differential OTA in Fig 4-3 as

$$I_{n,diff}^2 \ (I^2/Hz) \ = 2 \times 4kT \times \frac{2}{3} \times (g_{m1} + g_{m3} + g_{m5}). \tag{4-11}$$

For simplicity, from now on we refer to $I_{n,diff}^2$ as I_n^2. From Eq. 4-11, we can write the noise voltage spectral density as

$$V_{n,CMOS}^2 \ (V^2/Hz) = \frac{16kT}{3} \ (g_{m1} + g_{m3} + g_{m5}) \ R_{C1}^2 \tag{4-12}$$

Also, from Eq. 4-3, we can calculate the thermal noise of resistors R_{C1} as

$$V_{n,R}^2 \ (V^2/Hz) \ = 2 \times 4kTR_{C1} \tag{4-13}$$

From Eqs. 4-12 and 4-13 we can write the total output thermal noise spectral density of the OTA, $V_{n,out}^2$, as

$$V_{n,out}^2 \ (V^2/Hz) = 8kT \left[\frac{2 \ R_{C1}^2}{3} \ (g_{m1} + g_{m3} + g_{m5}) \ + R_{C1}\right]. \tag{4-14}$$

As in Fig. 4-5, the input-referred thermal-noise voltage, $V_{n,in}^2$, is the output noise divided by the squared voltage gain of Eq. 4-1, $(g_{m1}R_{C1})^2$. Thus, from Eq. 4-14 we can write

$$V_{n,in}^2 \ (V^2/Hz) = \frac{8kT}{g_{m1}} \left[\frac{2}{3} \left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m5}}{g_{m1}}\right) + \frac{1}{g_{m1}R_{C1}}\right]. \tag{4-15}$$

Now that we have calculated $V_{n,in}^2$ of the first stage of the OTA, we can calculate the total input-referred noise, $V_{n-OTA,in}^2$, based on the noise relationship of cascaded devices [58], therefore

$$V_{n-OTA,in}^2 = V_{n-S1,in}^2 + \frac{V_{n-S2,in}^2}{(g_{m1}R_{C1})^2} \tag{4-16}$$

where $V_{n-S1,in}^2$, $V_{n-S2,in}^2$ and A_1 are input-referred noise of the first stage, input-referred noise of second stage, and the gain of first stage respectively. As both stages are exactly the same, we can write Eq. 4-16 as

$$V_{n-OTA,in}^2 = (1 + \frac{1}{(g_{m1}R_{C1})^2}) V_{n-S1,in}^2 . \quad (4\text{-}17)$$

Similar to [42], the input-referred noise of the amplifier, $V_{n-AMP,in}^2$, in Fig 4-2 is given by

$$V_{n-AMP,in}^2 = V_{n-OTA,in}^2 \left(\frac{C_1+C_2+C_{in}}{C_1}\right)^2 \quad (4\text{-}18)$$

where C_{in} is the input capacitance of the OTA.

If we assume IC as the inversion coefficient of the transistor which is defined as the ratio of its drain current I_D to the moderate inversion characteristic current I_S [63], where I_S is given by

$$I_S = \frac{W}{L} \cdot \frac{2\mu C_{ox} U_T^2}{\kappa} \quad (4\text{-}19)$$

where $U_T = kT/q$ is the thermal voltage. A device having IC>10 operates in the strong inversion and its transconductance is proportional to $\sqrt{I_D}$. A device which has IC<0.1 operates in the weak inversion (subtrhreshold) region and its transconductance is proportional to I_D. If 0.1<IC<10, the device operates in moderate inversion region. Both strong and weak inversion expressions overestimate the trannconductance for moderate region. Hence, for our low-voltage low-power design, we use EKV model [63] to calculate the g_m of each transistor in low-power/voltage design. This model is valid in all regions of operation [63]. EKV estimates the g_m of devices as

$$g_m = \frac{\kappa I_D}{U_T} \cdot \frac{2}{1+\sqrt{1+4 \cdot IC}} \quad (4\text{-}20)$$

Therefore, from Eqs. 4-15, 4-17 and 4-20, we will have

$$V_{n-OTA,in}^2 \ (V^2/Hz) = \left(1 + \frac{1}{(g_{m1}R_{C1})^2}\right) \times \frac{16kT}{3g_{m1}} \times \left(1 + \frac{I_3}{I_1}\beta_3 + \frac{I_5}{I_1}\beta_5 + \frac{3U_T}{\kappa I_1 R_{C1}}\right) \quad (4\text{-}21)$$

where

$$\beta_i = \frac{4}{(1+\sqrt{1+4\times IC_i})} \tag{4-22}$$

where IC_i represents the inversion coefficient of device M_i. From Eq. 4-21, to minimize the input-referred noise of the OTA, I_1Rc should be several times larger than U_T which is equal to 26 mV (at T=300K). Additionally, the current ratios I_1/I_3 and I_1/I_5 have to be larger than β_3 and β_5, respectively. Thus, $(W/L)_3$ and $(W/L)_5$ should be several times smaller than $(W/L)_1$.

On the other hand, to have an acceptable phase margin, the dominant pole $\omega_{P1}=g_{m1}/C_L$ should be several times smaller than poles at $\omega_{P2}=g_{m3}/C_3$ and $\omega_{P3}=g_{m5}/C_5$, where C_L and C_n are the bandwidth limiting capacitor and the total capacitances seen at the gate of the transistor M_n, respectively. This calls for decreasing $(W/L)_1$ or increasing $(W/L)_3$ and $(W/L)_5$. Therefore, there is a tradeoff between the input-referred noise and phase margin. Among ω_{P2} and ω_{P3}, ω_{P2} should be chosen more precisely as it is closer to ω_{P1}. Hence, to insure stability, $(W/L)_3$ cannot be aggressively decreased and in the OTA topology of Fig. 4-3 we have $I_1 \approx I_3$. While I_3/I_1 was chosen conservatively, to reduce the input-referred noise (Eq. 4-12), we designed $I_5/I_1 \approx 0.1\beta_5$ and $I_1 R_{C1} \approx 145\ U_T$ where β_5 =0.91 and β_3 =0.94. As the flicker noise is a major concern in a low-noise low-frequency design, all transistors specially the input pair, which are the main contributors of 1/f noise, are sized as large as possible. The transistor sizes, and resistor and capacitor values are summarized in Table 4-I. The input device M1 operates in weak inversion while M3 and M5 operate in moderate inversion.

TABLE 4-I
TRANSISTOR SIZES AND COMPONENT VALUES

Devices	*W/L* (μm)	I_D (μA)	Inversion Coefficient
M_1, M_2,M_7, M_8	250/0.3	33	0.50
M_3, M_4, M_9, M_{10}	86/0.45	36	2.39
M_5, M_6, M_{11} , M_{12}	11.4/0.25	3	2.63

Resistors		Capacitors		Bias	
Resistor	Value	Capacitor	Value	Vbias1	360 mV
Rc1	110 kΩ	Cc	10 pF	Vbias2	210 mV
Rc2	110 kΩ	Cm1	2 pF	Ibias1	2.28 μA
Rz	7.5 kΩ	Cm2	2 PF	Ibias2	1.2 μA

4.6.2 Noise Efficiency Factor

Another important figure of merit for comparison of the noise performance among neural amplifiers is noise efficiency factor (NEF). This figure of merit is widely used to compare the performance of amplifiers in terms of noise, power and bandwidth [42], [46]. It is defined as

$$NEF = V_{n-OTA,in} \times \sqrt{\frac{2 \cdot I_{tot}}{\pi . U_T . 4kT . BW}} \tag{4-23}$$

Where $V_{n\text{-}OTA,in}$ is the rms input-referred noise voltage of OTA, I_{tot} is the total supply current, and BW is the bandwidth of the amplifier. This figure describes how many time the noise of a circuit (i.e. amplifier) is larger than the noise of a single CMOS transistor (which its only noise is white noise), given a specific bandwidth and drain current. Hence, NEF is unitless.

Assuming typical value of κ=0.7 [62], and substituting the expression for amplifier thermal noise (Eq. 4-21) integrated across the bandwidth BW into Eq. 4-23 and setting

$$I_{tot} = 4I_{M1} + I_{biasing} = 150\ \mu A \tag{4-24}$$

we obtain NEF ≈ 5.5 for 60 kHz bandwidth. The noise contribution of the stages following the neural amplifier to the overall system noise is decreased by the factor of the amplifier's gain. Therefore, the additional input-referred noise of the bandwidth-limiting stage is negligible as the 40 dB gain provided by the amplifier reduces its noise floor requirements.

4.7 Input-Referred Noise Measurement

Input-referred noise is another figure of merit which has been widely used to characterize the noise performance of a neural amplifier [42]. This figure is specifically useful in finding the maximum allowable signal level at the input of a neural amplifier. Also, it allows for the comparison of noise performance of different amplifiers without having to consider their gain differences. In this section we elaborate on strategies for measuring input-referred noise and the affiliated challenges.

Performing an input-referred noise measurement can be a very tedious task based on the specifications of the circuit such as noise level, frequency of interest, and operation voltage. Also, the device packaging (loose die versus packaged), shielding and ambient noise are among the test environmental conditions which can affect the accuracy and feasibility of the measurement. In the next two sections we will discuss a few methods and associated challenges of such measurements.

4.7.1 ENR method

Noise factor is the key figure of merit quantifying the radio frequency (RF) receivers and LNAs noise performance. It is defined as the ratio of the SNR at the input of the circuit to the SNR at the output

$$NF = \frac{SNR_{in}}{SNR_{out}} \tag{4-25}$$

The relation between noise factor and noise figure (NF) is

$$NF(dB) = 10\log(Noisefactor) \tag{4-26}$$

If we make sure that the noise contribution of the load has been considered, the noise figure and input-referred noise can be related to each other. Considering the circuit of Fig. 4-5, we can write

$$SNR_{in} = \frac{V_S}{N_S} \tag{4-27}$$

$$SNR_{Out} = \frac{V_S \times G}{(N_{IR}+N_S)\times G} \tag{4-28}$$

where V_S, N_{IR}, N_S and G are the input voltage, input-referred noise, source noise and amplifier gain respectively. From Eq. 4-25, Eq. 4-27 and Eq. 4-28, we can calculate NF as the ratio of the sum of the available source and amplifier input-referred noise power to the available source noise expressed in dB:

$$NF = 10\log\left(\frac{N_S+N_{IR}}{N_S}\right) \tag{4-29}$$

From Eq. 4-29, we can write the input-referred noise power as

$$N_{IR}(V^2/_{Hz}) = N_S \times (10^{(\frac{N_F}{10})} - 1) \tag{4-30}$$

An amplifier whose spot NF (which is the NF given in Eq. 4-25, calculated over a narrow bandwidth centered around an arbitrary frequency within the spectrum of input signal) is 3dB has an input-referred noise equal to the noise power of the input source, or KT.

In Eq. 4-30, we have not considered the impedance at the amplifier front-end, R_S. However, for an unmatched condition the actual input-referred noise voltage for a particular spot NF is dependent on R_S. Therefore, we can change Eq.4-30 for input-referred noise voltage, V_{IRN} for unmatched impedance as

$$V_{IRN}\left({}^{V}/_{\sqrt{Hz}}\right) = \sqrt{(10^{(\frac{N_f}{10})} - 1) \times R_S \times N_S} \tag{4-31}$$

In the case that NF is equal to 3 dB, we would have

$$V_{IRN} = \sqrt{N_S \times R_S} = \sqrt{KTR_S} = 4.5\left({}^{nV}/_{\sqrt{Hz}}\right) = -174\ dBm. \tag{4-32}$$

From Eq. 4-25 and Eq. 4-26, we can calculate the noise floor of the amplifier as

$$Noise\ floor\ (dBm) = 10\log(N_{IR} + N_S) = NF + 10\log N_S = NF + N_s\ (dBm) \Rightarrow$$

$$Noise\ floor = NF + BW_{Res}\ (dB) - 174 \tag{4-33}$$

where BW_{Res} is the resolution bandwidth of the spectrum analyzer and -174 is the ambient noise (for $NF = 3dB$) in dBm . Therefore, as discussed in Section 4.1, the noise floor of the amplifier calculated by Eq. 4-33 should be lower than the amplitude of neural signals in order to detect them. Considering the neural action potentials which have the lowest amplitude among neural signals, the noise floor of an implantable neural recording device should be kept below 10μV or -84 dBm.

Based on Eq. 4-31, in order to measure the input-referred noise we have to first measure the noise figure of the amplifier. We used a spectrum analyzer (Agilent E4440 A) with the noise figure personality. Since the output of our neural amplifier could not drive the 50 Ω impedance of the spectrum analyzer, an active probe is placed between the output of the circuit and the input of the

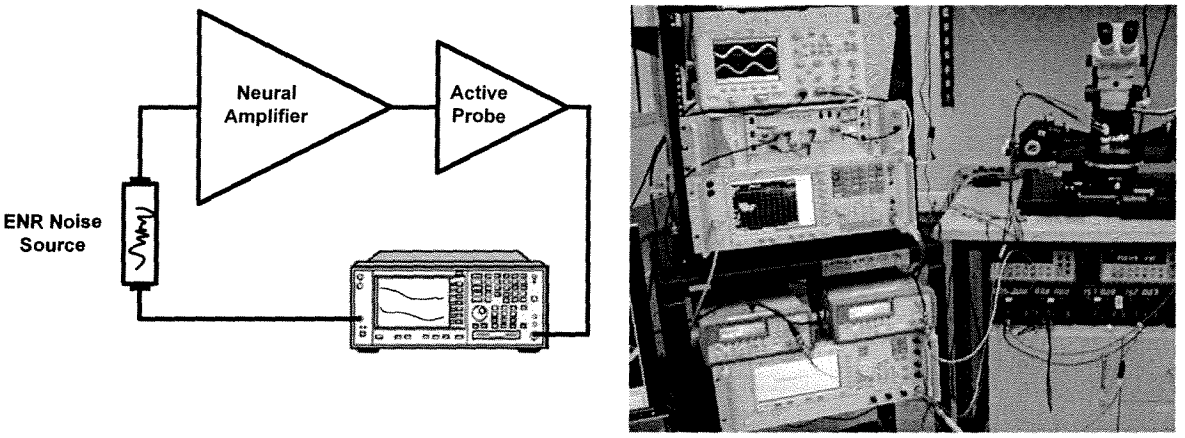

Figure 4-6. Schematic (Left) and test bench setup for input-referred noise measurement based on ENR method.

spectrum analyzer (Fig.4-6). The spectrum analyzer drives an excess noise ratio (ENR) source with known characteristics, and the generated noise drives the amplifier and active probe. The noise of the active probe gets added to the noise of the neural amplifier according the Fiirs equation format [58]:

$$NF_{DUT} = NF_{Amp} + \frac{NF_{AP}-1}{G_{Amp}} \tag{4-34}$$

where NF_{DUT}, NF_{Amp} and NF_{AP} are the noise figures of the device under test (neural amplifier and active probe), neural amplifier and active probe, respectively and G_{Amp} is the gain of the neural amplifier. We can de-embed the noise contribution of the active probe by calibrating the spectrum analyzer through measuring the NF of the active probe without having the amplifier in the measurement setup. Considering the fact that the noise figure of the ENR source is known to the spectrum analyzer and also elimination of the active probe noise through calibration process, the spectrum analyzer can calculate NF_{Amp} for the desired range frequency. The measured NF_{Amp} and Eq. 4-31 yield the amplifier input-referred voltage noise, V_{IRN} .

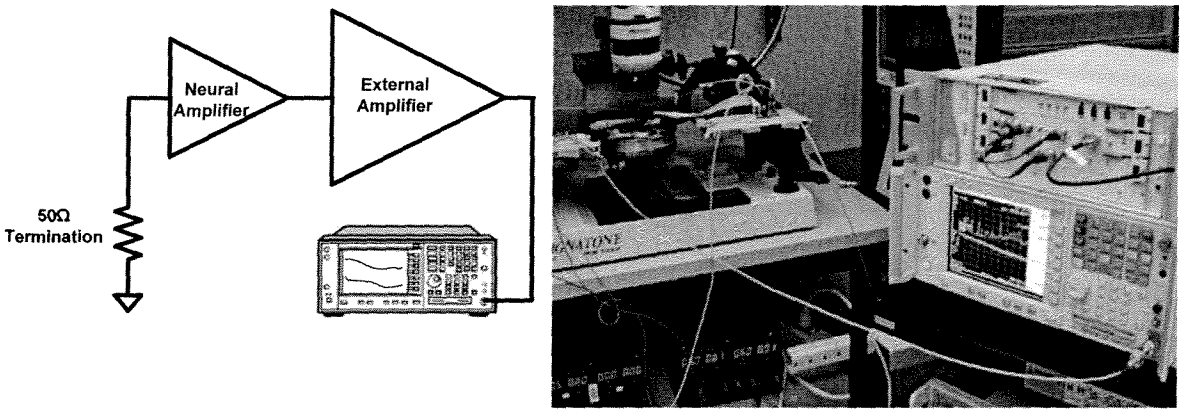

Figure 4-7. Schematic (Left) and test bench setup for input-referred noise measurement based on Gain method.

4.7.2 Gain method

The ENR method requires expensive equipments and software. There is another method for measurement of input-referred noise which is based on the measured gain, and total noise power in the output of the circuit (amplifier). Gain method is more accurate than the ENR method under certain conditions (i.e., noise figures more than 10 dB) [65]. From Eq. 4-29, we can write

$$NF = P_{Nout} - P_{NSout} \tag{4-35}$$

In this equation P_{Nout} is the total measured noise power in the output and P_{NSout} is the power of output noise due to the input source only, both indBm. Two factors contribute to the total output noise of a circuit: One is the undesired interfering signals at the input of the circuit, and the other is the noise of the device itself. From Eq. 4-32 and Eq. 4-35 we have

$$NF = P_{Nout} + 174(dBm) - BW(dB) - G_S \tag{4-36}$$

where BW is the bandwidth of interest and G_S is the gain of the whole system under test. As opposed to the ENR method where we used a controllable noise source, here we use a constant source of noise in the input. Hence, the differential inputs of neural amplifier are terminated with 50Ω impedances

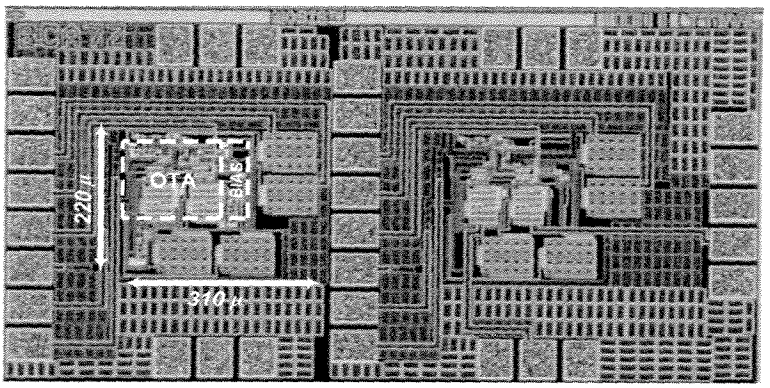

Figure 4-8. Die micrograph of the amplifier with on-chip biasing circuits (left) and without biasing circuits (right).

which based on Eq.4-2 generate a noise power of -174 dBm. The output of amplifier drives the input of the spectrum analyzer in order to measure the noise power of the chip. The main limiting factor in this method is the noise floor of the spectrum analyzer. The gain method is not effective if the noise power of the amplifier is lower than the noise floor of the spectrum analyzer. To solve this problem we amplified the output of our neural amplifier with an external amplifier and the resultant signal was connected to the input of the spectrum analyzer. Figure 4-7 shows the setup used for this method. The gain of the external amplifier is set to 60 dB in order to make the noise of our system distinguishable from the background noise of the measurement device. Similar to Eq. 4-34, the noise of the external amplifier gets added to the noise of the neural amplifier. Therefore, the measurements are done once with both amplifiers in circuit and once with the external amplifier alone to de-embed its noise from the neural amplifier noise. Also to calculate NF and hence the input-referred noise from Eq. 4-31 and Eq. 4-36, the gain of the neural amplifier is separately measured over the frequency of interest.

4.8 Measurements and Simulation Results

Measurements are performed to find the frequency response and noise performance of the amplifier. As shown in Fig.4-8, two prototypes of our circuit are laid out on a single die; one with on-chip biasing circuits (right), and the other with external biasing (left). The OTA is configured in a closed loop capacitive feedback configuration (Fig.4-2) with capacitors C1 and C2 having values of 10 pF and 100 fF, respectively to achieve a gain of 40 dB. Capacitors C_L are 7 pF on-chip MIM-capacitors which set the amplifier's bandwidth at ~60 kHz. The bandwidth of the amplifier can be decreased by increasing the value of the capacitors in the differential outputs of the amplifier. This can be achieved by ussing of chip capacitors in parallel with C_L.

In closed-loop configuration and operating in the tissue-electrode impedance measurement mode, the amplifier achieves a gain of 40 dB, a BW of 62 kHz and a phase margin of 55°as shown in Fig. 4-9. The measured and post-layout simulated input-referred noise of the amplifier are plotted in Fig.4-10 for the full-bandwidth mode of operation. The 1/f corner frequency is located at ~200Hz and integrating the area under this curve from 0.1 Hz to 60 kHz yields a value of 2.9 μV_{rms}. The 1/f noise is not a dominant noise source for neural action potentials and higher frequency impedance measurement signals, while it is the major noise source for very-low frequency LFP signals. Due to the high pickup noise of the spectrum analyzer at very low frequencies, we were not able to measure meaningful results below 10 Hz. The measured input-referred noise of Fig. 4-10 yields a noise efficiency factor of 5.95 over a 60 kHz bandwidth. Figure 4-11 compares the NEF of our design with that of some recent works. To have a fair comparison between the operating voltages, the supply voltages of these designs are plotted versus the technology in which they have been fabricated (Fig.4-12). Our amplifier works with a 0.5 V supply at 0.18 μm technology node. Measured and simulated performance parameters of this amplifier are listed in Table 4-II.

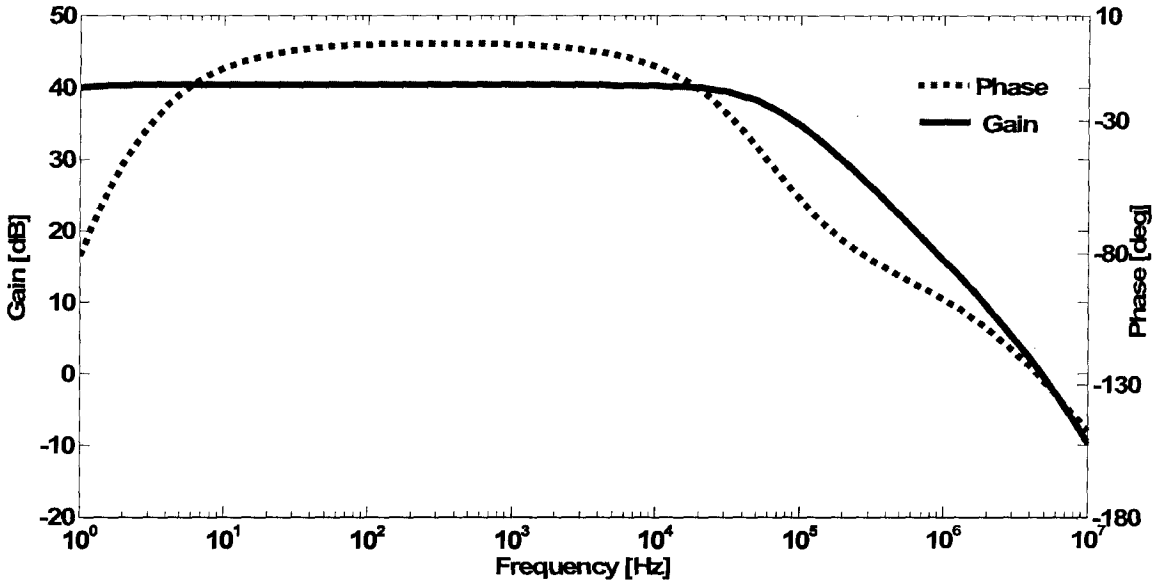

Figure 4-9. Post-layout simulated plot of the frequency response of amplifier.

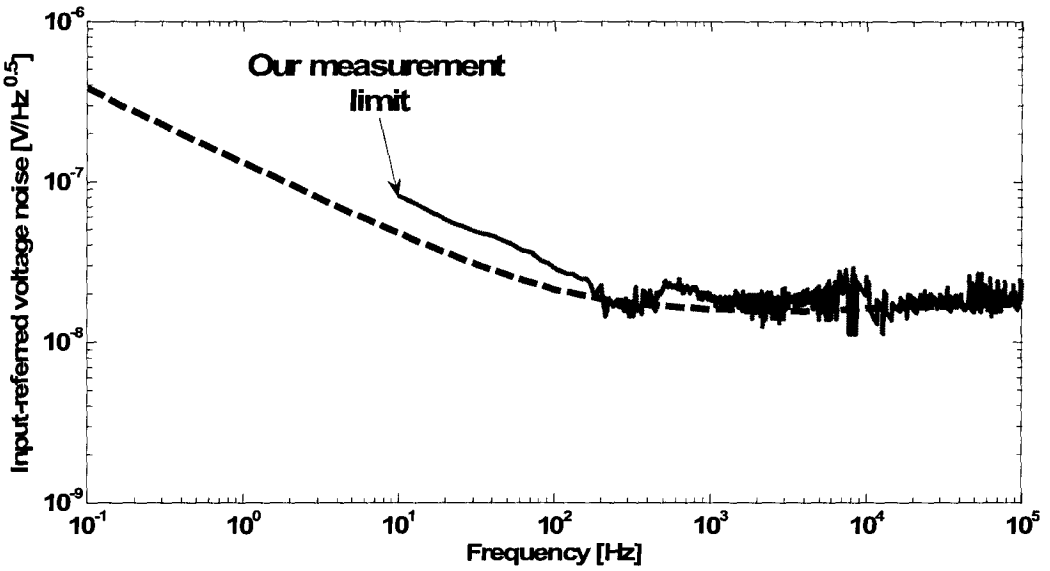

Figure 4-10. Measured (solid line) and post-layout simulated (dotted line) plot of the input-referred noise spectral density. Due to the limitation of our measurement devices we couldn't obtain meaningful data below 10 Hz.

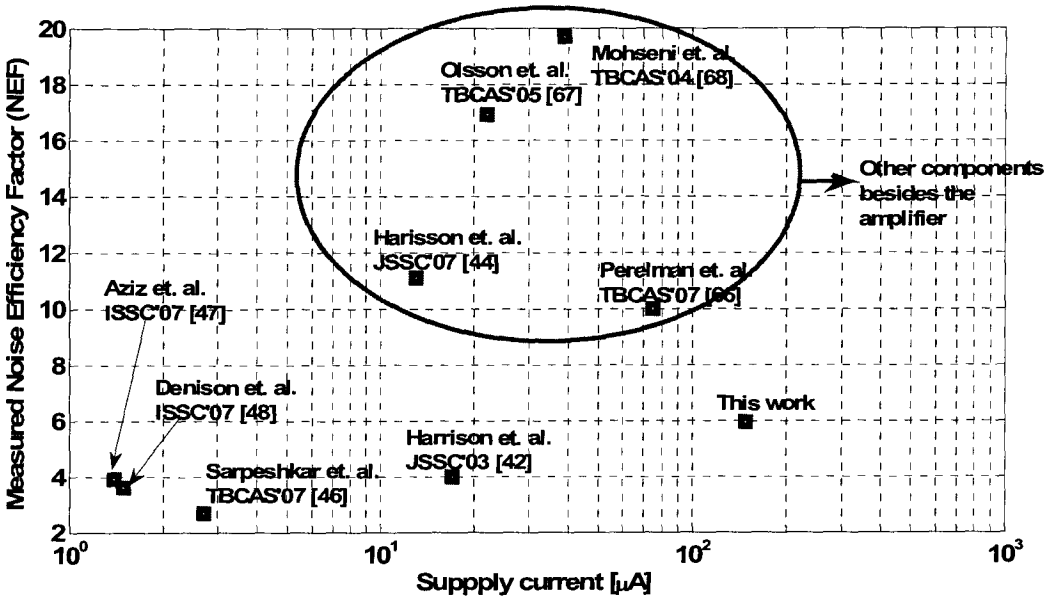

Figure 4-11. Supply voltage of recent neural amplifiers as a function of supply current.

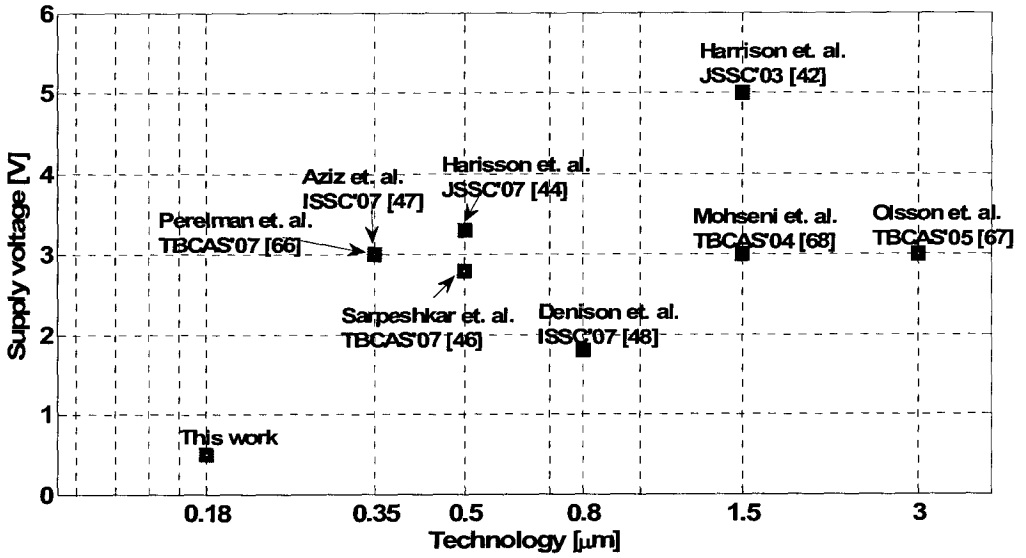

Figure 4-12. Supply voltage of recent neural amplifiers versus the technology of design.

TABLE 4-II
PERFORMANCE SUMMARY

Parameter	Simulation	Measurement
Supply voltage (V)	0.5	0.5
Technology (μm)	0.18	0.18
Total power (μW)	76	79
Mid-band Gain (dB)	40.1	40.3
Bandwidth (kHz)	61	62.1
Low-freq. cutoff (mHz)	0.91	1.1
Input-referred noise (μV_{RMS})	2.9	3.15[3]
Noise efficiency factor	5.47	5.95
CMRR (dB)	≥ 62	≥ 60
Phase Margin (°)	55	53
Area (mm^2)	N/A	0.069

4.9 Conclusion

An integrated ultra-low-voltage low-power low-noise biosignal amplifier with on-chip biasing circuit is presented. The 0.5 V supply voltage reduces the power consumption and enhances battery-powered operation. This amplifier can be used for recording a variety of biosignals including local field potentials and action potentials which have a frequency from mHz range to roughly 5 kHz. In addition, we introduced a feature for processing higher frequency sinusoidal stimulation currents which can be applied to tissue to measure the tissue-electrode impedance. Proper impedance measurement can be used to compensate for the signal attenuation due to formation of scar tissue around the implanted electrode; therefore our amplifier paves the way for chronic and accurate monitoring of signals in neural interfaces.

Our neural amplifier features a bandwidth adjustment capacitor which sets the high cut-off frequency of the amplifier. Therefore, the excessive noise can be filtered out in the neural recording

[3] Measured from 10 Hz to 61kHz

mode by decreasing the amplifier's bandwidth to 5 kHz. As tissue-electrode impedance characterization signals are generally one to two order of magnitudes larger than neural signals, we can record (amplify) them with 60 kHz bandwidth while having a favorable SNR. Tuning the amplifier's bandwidth can also be helpful to achieve a low-input referred noise voltage while recording neural signals below 100 Hz where the amplifier's noise is dominated by 1/f noise.

It is important to note that as the amplifier has sufficiently low thermal noise level (20 $nV/\sqrt{Hz}$) and considering the fact that the thermal noise is the dominant noise source in frequencies above 500 Hz (Fig. 4-10), the 3.15 μV_{RMS} input-referred noise of the amplifier over 60 kHz BW is still lower than the 5-10 μV_{RMS} extracellular background noise. Hence, it may be possible to eliminate the need for a bandwidth limiting stage while recording neural action potentials (> 100 Hz) with the price of a minute increase in the input-referred noise. However, for recording neural signals with frequencies in the range of ~DC to 100 Hz (generally LPF signals), limiting the amplifier's bandwidth would be highly advantageous.

Chapter 5

Conclusion and Future Work

We proposed several techniques to improve the quality of recorded neural signals and increase the longevity of the neural implants inside the tissue. A polymer based drug delivery system and its controllability issues were investigated to improve biocompatibility and performance of the MEMS section of a neural recording probe. We focused on the electrical properties of the surface-modification/drug-delivery coating to characterize its effects on the overall system. It seems that although the coating has some attenuating effects on the neural signals (based on their frequency), in long run it would increase the total signal-to-noise-ratio of the system.

At the circuit level, an ultra-low-voltage low-noise low-power neural amplifier was developed. As compared to the previous neural amplifiers, the circuit achieves a favorable input-referred noise while having comparable power consumption. The ultra-low-voltage operation of our neural amplifier is a great asset for fully implantable neural recording systems.

Considering the diverse frequency of neural signals and also the higher frequency tissue-electrode impedance characterization signals, a variable-bandwidth neural amplifier would allow for filtering out the excess noise and maximizing the SNR for each type of signals. Similar to [46], a tunable filter can be used following the gain stage, in which the bandpass characteristic could be controlled by a current or voltage.

Current trend in neuroscience calls for more electrodes to be embedded in a certain probe

area to achieve a good resolution into the activity of particular populations of neurons. Although highly beneficial for neuroscientists, single-neuron resolution is achieved with the cost of having an amplifier dedicated to each channel, and the tradeoff between the power and input-referred noise of the amplifier. As a result, a method which allows for the use of a single amplifier for all of the channels, while maintaining a comparable SNR, would tremendously cut the amplifier's power. This would be an active are of research in the area of neural recording systems.

A potential way to further improve the signal quality in neural recording systems is by measuring and monitoring the tissue impedance over a wide frequency range which may give information on the quality of the electrode-tissue contact, show change in the surrounding tissue, and indicate the recording ability of the electrode under these circumstances . This strategy in accord with the drug-releasing probe solution will address implant failure and its prevention in a compound way, first by monitoring the tissue-electrode impedance *in-vivo* and then releasing an appropriate amount of drug, based on the measured impedance. This impedance may also be used to compensate for signal attenuation with time. An established technique for measuring this impedance is to apply stimulation currents with frequencies in the range of 0.1 Hz to few tens of kHz to the electrode-tissue interface and perform the impedance measurement based on the recorded signals from the site. Currently this is performed using bulky impedance analyzers or on-chip circuits with high energy consumption, dissipating heat at levels which may cause tissue necrosis.

The emerging applications and increasing demand for long-term neural interfaces is accompanied with a need for low-voltage, power efficient on-chip subsystems (i.e. tissue-electrode contact impedance analyzer) which can be integrated on the neural probe. Based on the measured impedance, a specific amount of drug is released from the coating of the electrode to reduce the formation of the scar tissue around the recording sites. This method allows detection of any anomaly

appearing at the electrode-tissue contact level, thus ensures the precision of the recorded signal and prolongs the life of the implant.

Another aspect of electrically controlled drug release is the potential effect of the control signal on the surrounding neurons. Although the drug release rate can be controlled through application of proper stimuli, we should be careful about specifications of this signal. Currents leaking out of polymer structure can result in undesired effects if their amplitude is more than excitation threshold of neurons in the specific frequency of operation. Hence, frequency and amplitude of the release control waveform should be chosen in a way to circumvent any stimulation effect on the neurons. As discussed in Chapter 3, a possible solution for this problem may be through fabricating grounded pads around the recording electrodes to reduce the amount of leakage current which flows to tissue in the drug release phase of operation.

The other problem affiliated with the design of Fig. 3-6 is the distortion of the neural signal due to the noise of the electrical switch, located before the neural amplifier. Unlike the blocks following the neural amplifier which their contribution to the overall system noise is attenuated by the gain of the amplifier, the noise of this switch will be directly added to the neural signal which results in remarkable reduction of SNR. As this is an ultra-low-frequency switch (toggled only several times per day, based on the specifications of the drug-release system), it may be possible to implement it as a mechanical switch. However, MEMS switches have their own problems such as being relatively high voltage devices, fabrication costs and integration problems. Another solution is to separate the recording pads from the drug-release pads. While this strategy works for two dimensional neural probes (i.e. Michigan array) due to diffusion of drug to peripheral locations, it may not be a feasible solution for three-dimensional probes (i.e. Utah array) where the electrode shanks are fairly separated from each other (400 μm pitch [44]).

Previous works suggest that a concentration of 1 μM of the anti-inflammatory drug in the 500 μm radios of the implant is sufficient to substantially reduce the tissue reactive response. Our method of calculating the amount of released drug can be used along with diffusion properties of the drug inside the tissue to calibrate the release signal, and hence achieve the desired concentration.

Future work will also quantify the amount of dopant released using a direct measurement method, such as UV or IR spectroscopy, depending on the type of the dopant used. In this way we can confirm whether the calculation reflects actual dopant release. Using these methods we can also measure whether there is a significant release of the dopant due to diffusion.

Bibliography

[1] K. Najafi, and K. D. Wise, "An implantable multielectrode array with on-chip signal processing," IEEE Journal of Solid State Circuits. 21: 1035-1044, 1986.

[2] X. Navarro, T. Krueger, N. Lago, S. Micera, T. Stieglitz and P. Dario, "A critical review of interfaces with the peripheral nervous system for the control of neuroprostheses and hybrid bionic systems," Journal of Peripheral Nervous System. 10:229–258, 2005.

[3] C. Donfack, M. Sawan, and Y. Savaria, "Implantable measurement technique dedicated to the monitoring of electrode-nerve contact in bladder stimulators," Medical and Biological Engineering and Computing. 38 (4): 465-468, 2000.

[4] R. Wadhwa, C.F. Lagenaur, and X.T. Cui, "Electrochemically controlled release of dexamethasone from conducting polymer polypyrrole coated electrode," Journal of Controlled Release. 110 (3): 531–541, 2006.

[5] B.H. Brown, H. Smallwood, D.C. Barber, P.V. Lawford, and D.R. Hose, "Medical physics and biomedical engineering," Institute of Physics Publishing, 1999.

[6] M. Faist, J. Xie, D. Kurz, W. Berger, C. Maurer, P. Pollak, and C.H. Lucking, "Effect of bilateral subthalamic nucleus stimulation on gait in Parkinson's disease," Brain 124: 1590–1600, 2001.

[7] http://www.medel.com/english/10_About_Hearing_Implants/03_How_a_Cochlear_Implant_Works.php.

[8] M.A.L. Nicolelis, D. Dimitrov, J.M. Carmena, R. Crist, G. Lehew, J.D. Kralik, and S.P. Wise, " Chronic, multisite, multielectrode recordings in macaque monkeys," Proceedings of the National Academy of Sciences 100: 11041-11046, 2003.

[9] M.A.L. Nicolelis, C.R. Stambaugh, A. Brisben, and M. Laubach, "Methods for simultaneous multisite neural ensemble recordings in behaving primates," Methods for Neural Ensemble Recordings. 7:121–56, 1999.

[10] J.N. Turner, W. Shain, D.H. Szarowski, M.D. Andersen, S. Martins, M. Isaacson, and H.G. Craighead, "Cerebral astrocyte response to micro-machined silicon implants," Experimental Neurology. 156: 33– 49, 1999.

[11] D.H. Szarowski, M.D. Andersen, S. Retterer, A.J. Spence, M. Isaacson, H.G. Craighead, J.N. Turner, and W. Shain, "Brain responses to micro-machined silicon devices," Brain Reviews. 983: 23– 35, 2003.

[12] S. Retterer, K.L. Smith, C. Bjornsso, K. Neeves, A.J. Spence, J.N. Turner, W. Shain, and M. Isaacson, "Model neural prostheses with integrated microchannels: treating the reactive response to implantable devices," IEEE Transactions in Biomedical Engineering. 51: 2063–2073, 2004.

[13] Y. Zhong, G. McConnell, and R.V. Bellamkonda, "In vitro and in vivo study of a novel drug releasing coating for implanted neural electrodes," Neural Interfaces Workshop. November, 2004.

[14] Y. Zhong, X. Yu, R. Gilbert, and R. Bellamkonda, "Stabilizing electrode-host interfaces: a tissue engineering approach", Journal of Rehabilitation Research and Development. 38 (6): 632–667, 2001.

[15] T. Stieglitz, and J.-U. Meyer, "Microtechnical interfaces to neurons," in Topics in Current Chemistry Series, Microsystem Technology in Chemistry and Life Science, A. Manz, and H. Becker, Eds. Springer. 194: 131–162, 1998.

[16] J. Chen, K.D. Wise, J.F. Hetke, and S.C. Bledsoe, "A multichannel neural probe for selective chemical delivery at the cellular level. IEEE Transactions on Biomedical Engineering. 44: 760–769, 1997.

[17] M.A.L. Nicolelis, D. Dimitrov, J.M. Carmena, R. Crist, and G. Lehew, "Chronic, Multisite multielectrode recordings in macaque monkeys," Proceedings of National Academic of Science. USA 100:11041, 2003.

[18] K.C. Cheung, Y. Zhon, P. Renaud, and R. Bellamkonda, "Comparison Of tissue reaction to implanted polyimide and silicon microelectrode Arrays," BiosurfVI. Switserland, 2005.

[19] E.M. Maynar, C.T. Nordhausen, and R.A. Norman, "The Utah intracortical electrode array: a recording structure for potential brain-computer interfaces," Electroencephalogram Clinical Neurophysiology. 102: 228– 239, 1997.

[20] T. Stieglitz , M. Schuettler, and K.P. Koch, "Neural prostheses in clinical practice: biomedical microsystems in neurological rehabilitation," Biomedical Techniques. 49: 72–77, 2007.

[21] F. Berkenbosch, "Macrophages and astroglial interactions in repair to brain injury," Proceedings of National Academy of Science. 650: 186– 190, 1992.

[22] W.M. Grill, and J.T. Mortimer, "Neural and connective tissue response to long-term implantation of multiple contact nerve cuff electrodes," Journal of Biomedical Materials. 50: 215– 226, 2000.

[23] N.K. Guimard, N. Gomez, and C.E. Schmidt, "Conducting polymers in biomedical engineering," Polymers in Biomedical Applications. 32 (2): 876-921, 2007.

[24] W. Shain, L. Spataro, J. Dilgen, K. Haverstick, S. Retterer, M. Isaacson, M. Saltzman, and J.N. Turner, "Controlling cellular reactive responses around neural prosthetic devices using peripheral and local intervention strategies," IEEE Transactions on Neural Systems and Rehabilitation Engineering. 11: 186– 188, 2003.

[25] L. Spataro, J. Dilgen, S. Retterer, A.J. Spence, M. Isaacson, J.N. Turner, and W. Shain, "Dexamethasone treatment reduces astroglia responses to inserted neuroprosthetic devices in rat neocortex," Experimental Neurology. 194: 289–300, 2005.

[26] S.T. Retterer, K.L. Smith, C.S. Bjornsson, K.B. Neeves, A.J.H. Spence, J.N. Turner, W. Shain, and M.S. Isaacson, "Model neural prostheses with integrated microfluidics: a potential intervention strategy for controlling reactive cell and tissue responses," IEEE Transactions on Biomedical Engineering 51: 2063–2073, 2004.

[27] C.W. Lin, M.F. Lee, Y.F. Yang, and C.C. Wu, "Surface modification of Bio-MEMS micro-device with conducting polymer - studies with rat cardiomyocytes," Engineering in Medicine and Biology Society," IEEE-EMBS. 27: 2619-2621, 2005.

[28] M. Warren, "Electronic and structural effects on the electrochemistry of Polypyrrole," M.A.Sc thesis, University of British Columbia, 2005.

[29] K. West, L. Bay, M.M. Nielsen, Y. Velmurugu, and S. Skaarup, "Electronic Conductivity of Polypyrrole-Dodecyl Benzene Sulfonate Complexes," Journal of Physical Chemistry. 108: 15001-15008, 2004.

[30] G.J. Lee, S.H. Lee, K.S. Ahn, and K.H. Kim, "Synthesis and characterization of soluble polypyrrole with improved electrical conductivity," Journal of Applied Polymer Science. 84(14): 2583-2590, 2002.

[31] T. Yeu, K.M. Yin, J. Carbajal, and R.E. White, "Electrochemical characterization of electronically conductive polypyrrole on cyclic voltammograms," Journal of Electrochemistry. 138 (1-2): 2869–2877, 1993.

[32] B. Massoumi, and A. Entezami, " Electrochemically Controlled Binding and Release of Dexamethasone from Conducting Polymer Bilayer Films," Journal of Bioactive and Compatible Polymers. 17: 51-62, 2002.

[33] C. Wang, P.G. Whitten, C.O. Too, and G.G. Wallace, "A galvanic cell driven controlled release system based on conducting polymers," Sensors and Actuators B: Chemical. 129 (2) : 605-611, 2007.

[34] G.G Belmonte, and J. Bisquert, "Impedance analysis of galvanostatically synthesized polypyrrole films: correlation of ionic diffusion and capacitance parameters with the electrode morphology," Electrochimica Acta. 47: 4263–4272, 2002.

[35] X.Y. Cui, J.F. Hetke, J.A. Wiler, D.J. Anderson, and D.C. Martin, "Electrochemical deposition and characterization of conducting polymer polypyrrole/PSS on multichannel neural probes," Sensors and Actuators. 93 (1): 8 –18, 2001.

[36] Y.H. Xiao, X.Y. Cui, J.M. Hancock, M.B. Bouguettaya, J.R. Reynolds, and D.C. Martin, "Electrochemical polymerization of poly (hydroxymethylated-3,4-ethylenedioxythiophene) (PEDOT-MeOH) on multichannel neural probes," Sensors and Actuators. 99 (2-3): 437–443, 2004.

[37] L. Litvak, and E. Overstreet, "Forward masking method for estimating neural response". US Patents. 7,171,261. 2007 Jan, 30.

[38] G. T. A. Kovacs, "Introduction to the theory, design and modeling of thin-film microelectrodes for neural interfaces," in Enabling Technologies for Cultured Neural Networks, D. A. Stenger and T.McKenna, Eds. San Diego, CA: Academic. 121–166, 1994.

[39] P. Mohseni, and K. Najafi, "A low power fully integrated bandpass operational amplifier for biomedical neural recording applications," Proceeding of Second Joint EMBS/BMES Conference. 2: 2111-2112, 2002.

[40] R. H. Olsson, M. N. Gulari, and K. D. Wise, "Silicon neural recording arrays with on-chip electronics for in-vivo data acquisition," Proceedings of the Second Annual International IEEE-EMBS Special Topic Conference on Microtechnologies in Medicine & Biology. 2: 237-240, 2002.

[41] K. Guillory, and R. A. Normann, "A 100-channel system for real time detection and storage of extracellular spike waveforms," Journal of Neuroscience Methods. 91: 21-29, 1999.

[42] R. Harrison, and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," IEEE Journal of Solid-State Circuits. 38 (5): 958-965, 2003.

[43] A. C. Metting van Rijn, A. Peper, and C. A. Grimbergen, "High-quality recording of bioelectric events," Medical & Biological Engineering & Computation. 29:1035-1044, 1986.

[44] R.R. Harrison, P.T. Watkins, R.J. Kier, R.O. Lovejoy, D.J. Black, B. Greger, and F. Solzbacher, "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," IEEE Journal of Solid-State Circuits. 42 (1): 123-133, 2007.

[45] J. Jin, and K. D. Wise, "An implantable CMOS circuit interface for multiplexed microelectrode recording arrays," IEEE Journal of Solid State Circuits. 27 (3): 89-96, 1992.

[46] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An Energy-Efficient Micropower Neural Recording Amplifier," IEEE Transactions on Biomedical Circuits and Systems . 1 (2): 20-26, 2007.

[47] J. Aziz, R. Genov, M. Derchansky, B. Bardakjian, and P. Carlen, "256-Channel Neural Recording Microsystem with On-Chip 3D Electrodes," Solid-State Circuits Conference, Digest of Technical Papers. 42 (12): 160-594, 2007.

[48] T. Denison, K. Consoer, W. Santa, A.T. Avestruz, J. Cooley, an d A. Kelly, "A 2 μW 100 nV/rtHz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials," IEEE Journal of Solid-State Circuits. 42 (12): 2934-2945, 2007.

[49] S. Chatterjee, Y. Tsividis, and P. Kinget, "0.5 V Analog Circuit Techniques and Their Application in OTA and Filter Design," IEEE Journal of Solid-State Circuits. 40 (12): 2373–2387, 2005.

[50] D. R. Merrill , and P. A. Tresco, "Impedance characterization of microarray recording electrodes in vitro," IEEE Transactions on Biomedical Engineering, vol. 52, pp. 1960-1965, 2005.

[51] S. Pernici, G. Nicollini, and R. Castello, "A CMOS low-distortion fully differential power amplifier with double nested Miller compensation," IEEE Journal of Solid-State Circuits. 28 (7): 758–763, 1993.

[52] R. Hogervorst, J. Tero, R. Eschauzier, and J. Huijsing, "A compact power-efficient 3V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," IEEE Journal of Solid-State Circuits. 29 (12): 1505–1513, 1994.

[53] B. Blalock, P. Allen, and G. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," IEEE Transactions on Circuits Systystems. 45 (7): 769–780, 1998.

[54] U. Moon, G. Temes, E. Bidari, M. Keskin, L. Wu, J. Steensgaard, and F. Maloberti, "Switched-capacitor circuit techniques in submicron lowvoltage CMOS," IEEE International Conference on VLSI and CAD. 5: 349–358, 1999.

[55] S. Karthikeyan, S. Mortezapour, A. Tammineedi, and E. Lee, "Low-voltage analog circuit design based on biased inverting opamp configuration," IEEE Transactions on Circuits and Systems. 47 (3): 176–184, 2000.

[56] J. Crols, and M. Steyaert, "Switched-opamp: an approach to realize full CMOS switched-capacitor circuits at very low power supply voltages," IEEE Journal of Solid-State Circuits. 29 (8): 936–942, 1994.

[57] R. Hogervorst, J. Tero, R. Eschauzier, and J. Huijsing, "A compact power-efficient 3V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," IEEE Journal of Solid-State Circuits. 29 (12): 1505–1513, 1994.

[58] W.M. Leach, "On the calculation of noise in multistage amplifiers," IEEE transactions on Circuits and Systems. 42 (3): 176-178, 1995.

[59] S. Chatterjee, K.P. Pun, Y. Tsividis, and P. Kinget, "Analog Circuit Design Techniques at 0.5V," Springer, 2007.

[60] M. Abduli, and P. Kinget, "A 0.5 V fully differential gate-input operational transconductance amplifier with intrinsic common-mode rejection," IEEE International Symposium on Circuits and Systems, 2006.

[61] P. Kinget, S. Chatterjee, and Y. Tsividis, "0.5-V Analog Circuit Techniques and Their Application in OTA and Filter Design," IEEE J. of Solid-State Circuits. 40 (12): 2373-2387, 2005.

[62] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw Hill, 2001.

[63] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to lowvoltage and low-current applications," Analog Integrated Circuits. 8: 83–114, 1995.

[64] M. F. Iskander, "Electromagnetic fields and waves," Prentice Hall, 1992.

[65] Maxim Semiconductor, "Three methods for noise figure measurement," Application Notes, November 2003.

[66] Y. Perelman, and R. Ginosar, "An integrated system for multichannel neuronal recording with spike/LFP separation, integrated A/D conversion and threshold detection," IEEE Transactions on Biomedical Engineering. 54 (1): 130–137, 2007.

[67] R.H. Olsson, III, D.L. Buhl, A.M. Sirota, G. Buzsaki, and K.D. Wise, "Band-tunable and multiplexed integrated circuits for simultaneous recording and stimulation with microelectrode arrays," IEEE Transactions on Biomedical Engineering. 52 (7): 1303–1311, 2005.

[68] P. Mohseni, and K. Najafi, "A fully integrated neural recording amplifier with dc input stabilization," IEEE Transactions on Biomedical Engineering. 51 (5): 832–837, 2004.