COMPARATIVE ANALYSIS OF HIGH INPUT VOLTAGE AND HIGH VOLTAGE CONVERSION RATIO STEP-DOWN CONVERTERS EQUIPPED WITH SILICON CARBIDE AND ULTRAFAST SILICON DIODES

by

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ABSTRACT

DC to DC step-down applications with high input voltage and high voltage conversion ratio operational requirements, such as photovoltaic battery chargers, are subject to high conduction losses, high switching losses and substantial reverse-recovery losses when minority carrier principle diodes are used. The recent introduction of silicon carbide diodes with high breakdown voltages has made possible the elimination of reverse-recovery losses at high voltage levels and as such has sparked interest in their use due to the potential efficiency improvements.

This report presents the results of a comprehensive analysis on the use of silicon carbide diodes and their counterparts, ultrafast silicon diodes, in conventional buck converters and isolated current-fed buck converters in high input voltage and high voltage conversion ratio step-down applications. The analysis illustrates both theoretically, with the use of steady-state average models, and experimentally the substantial efficiency benefits of the use of reverse-recovery free silicon carbide diodes in the conventional buck converter and the small but significant improvement in the efficiency of the isolated current-fed buck converter. The improvements of the conventional buck converter paired with silicon carbide diodes are shown to be significant enough to grant the variant the most efficient position for power levels below 1 kW. In addition, the four variants are categorized based on their cost and performance; therefore, providing engineers with a convenient guide to aid their selection of the appropriate converter depending on the operational requirements.

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Special thanks are owed to my parents, who have supported me throughout my years of education with advice and understanding.

DEDICATION

To my parents

1 INTRODUCTION

1.1 Definition of the problem

High voltage step-down applications with high voltage conversion ratios, such as photovoltaic battery chargers, face extreme operating conditions that give rise to high transistor switching losses, high conduction losses and significant reverse-recovery losses when minority carrier principle diodes are used. Suitable converters must cope with such extreme conditions and imposed losses, compromising between simplicity, cost effectiveness, and efficiency. These goals are conflicting at times and are best achieved by adaptive topological and component selections, spurred by technological and conceptual innovations. The innovations bring with them interesting properties and facilitate new solutions to old problems.

One such technological innovation is the silicon carbide (SiC) power diode, a conventional Schottky diode with high breakdown voltages [6]. The insusceptibility of the SiC diode to reverse-recovery losses makes it an attractive option for high voltage applications compared to ultrafast silicon (Si) diodes which operate based on the minority carrier principal and are subject to reverse-recovery losses. The qualitative advantages of the SiC diode are obvious; however, the quantitative performance benefits and cost premiums are unknown. In addition, the appropriate topological selections are unclear given the revolutionary nature of the SiC improvements.

1.2 Literature Review

The scope of the topological comparison is limited to two popular step-down buck topology variants deemed appropriate by a literature review, namely the conventional buck topology and isolated current-fed buck topology. The conventional buck topology is the most rudimentary step-down topology, making it an attractive option for analysis due to its simplicity and cost effectiveness. In addition, it is susceptible to high reverse-recovery losses, as is noted in [1, 8] and shown in chapter 2; therefore, the potential benefits of the SiC diodes are meaningful and worth analyzing quantitatively. Pulse width modulating converters with quadratic DC conversion ratios were deemed inappropriate due to their low efficiency performance [7].

The isolated current-fed buck topology addresses many of the downsides of the conventional buck topology by isolating the converter into two regions with galvanic isolation [4, 5]; therefore, reducing transistor switching losses, reverse-recovery losses and front-end conduction losses as noted in chapter 3. The improvements minimize the potential benefits of the SiC diodes and permit the isolated current-fed buck topology to showcase the importance of topological choice selection. In addition, the inclusion of the isolated current-fed buck topology in the analysis provides results for a topology with galvanic isolation: a requirement in many commercial applications.

1.3 Thesis objectives and methodology

This thesis addresses the questions raised in the introductory section through a comparative analysis of the use of minority and majority carrier principle diodes in high input voltage and high voltage conversion ratio step-down applications. The objectives of the comparative analysis are to determine the performance advantage of the SiC diodes over ultrafast Si diodes in conventional buck and isolated current-fed buck converters, to determine the cost of the four variants, to determine the efficiency of the four variants and to present the findings in the form of a guide that engineers can use to select the appropriate high voltage step-down converter. The input voltage range is chosen to be 250V to 550V and the output voltage is chosen to be 48V. The methodologies chosen to achieve the mentioned objectives are based on theoretical and experimental benchmarks and are explained below.

A theoretical analysis of the conventional buck converter is presented in chapter 2. The steady state averaged model, equivalent circuit and individual losses are derived and shown for the case where both ultrafast Si and SiC diodes are employed. In addition, the prototype is explained and exhibited. Chapter 3 presents the same theoretical analysis of isolated current-fed buck converter with special attention given to the topological improvements over the conventional buck converter. In order to keep the results consistent the isolated current-fed buck converter is constructed using the conventional buck components. In addition, the prototype transformer leakage inductance problem is examined and the solution presented. The experimental results are presented in chapter

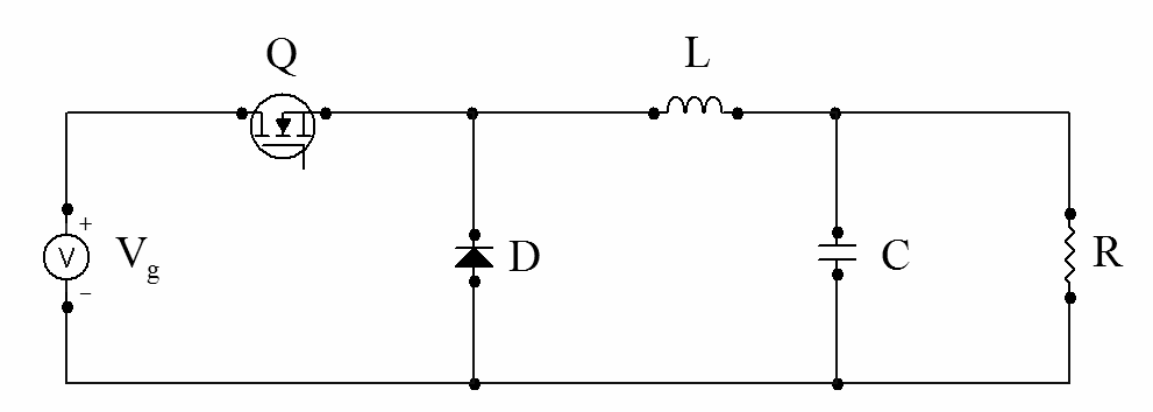
4: illustrating the cost, efficiency vs. input voltage, and load regulation. Comparisons to the theoretical predictions and results are made at appropriate times.

Chapter 5 is reserved for the discussion of the results and for recommendations. The suitability of each converter variant is debated based on the results from chapters 2, 3 and 4. Finally, the success of the thesis and the research it is based on is presented in the conclusion with a short discussion about further research.

2 CONVENTIONAL BUCK

The theoretical analysis of the conventional buck converter, shown in figure 2.1, is presented in this chapter. The analysis is broken up into four sections: analysis of operation, steady-state equivalent circuit model derivation, individual power loss analysis and experimental prototype discussion.

Figure 2.1 Schematic of conventional buck converter



2.1 Analysis of operation

During a normal operating cycle the conventional buck converter equipped with minority carrier principle diodes proceeds through seven stages transferring energy from the source to the inductor and discharging the stored energy into the load. The use of a majority carrier principle diode eliminates one stage; therefore, eliminating the need for

two analysis. A normal operating cycle, consisting of seven stages, is described below with reference to figure 2.2.

1. $(0 < t \leq DT_s)$

   The transistor is on and the diode is completely off (all of the minority charge is removed).

2. $(DT_s < t \leq DT_s + t_f)$

   The transistor switches off as the voltage across it ramps up. This time period corresponds to the time required for the gate driver to charge the MOSFET gate-to-drain capacitance.

3. $(DT_s + t_f < t \leq DT_s + t_f + t_{off})$

   The diode becomes forward-biased and current begins to commute through it, increasing linearly until all of the inductor current is flowing through it. This time period corresponds to the time required for the gate driver to discharge the MOSFET gate-to-source capacitance.

4. $(DT_s + t_f + t_{off} < t \leq Ts - t_{on} - t_{rr} - t_r)$

   The diode is on and the transistor is off.

5. $(Ts - t_{on} - t_{rr} - t_r < t \leq Ts - t_{rr} - t_r)$

   The transistor switches on. The first step in this process is for the current through the diode to decrease to zero. This time period corresponds to the time required for the gate driver to charge the MOSFET gate-to-source capacitance.

6. $(Ts - t_{rr} - t_r < t \leq Ts - t_r)$

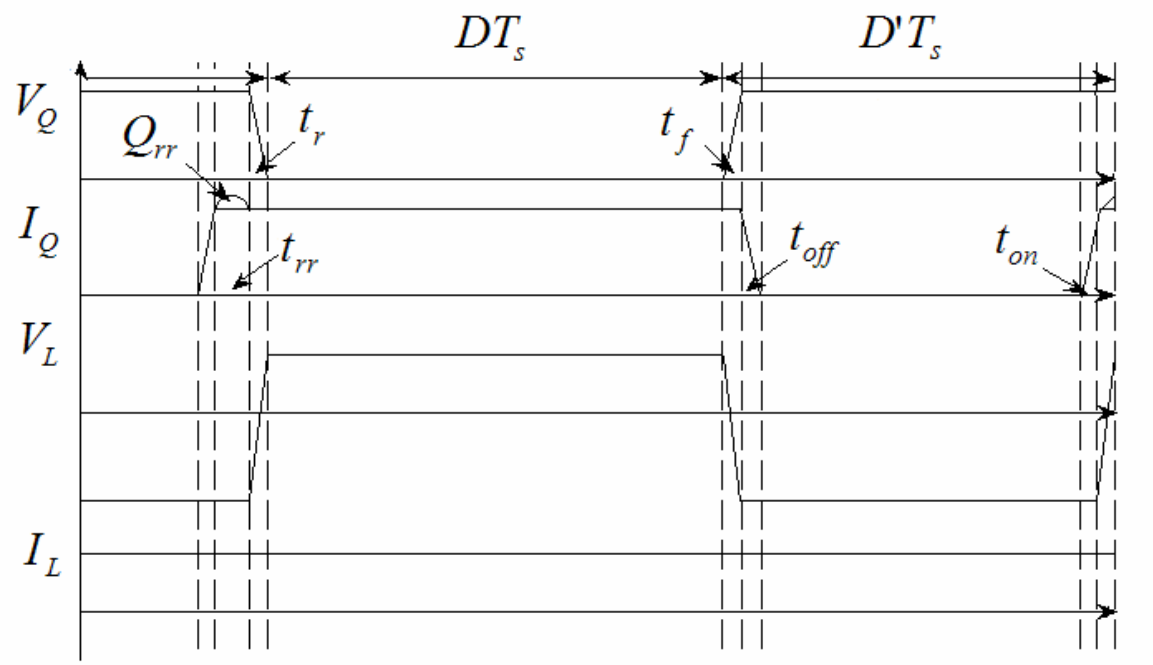
   The stored minority charge is removed from the diode. This occurs both actively, defined as Q_{rr}, and passively, via recombination.

7. ($Ts - t_r < t \leq Ts$)

   The transistor begins to switch on as the voltage across it ramps down. This time period corresponds to the time required for the gate driver to discharge the MOSFET gate-to-drain capacitance.

Figure 2.2 illustrates the transistor and inductor voltage and current waveforms of a normal operating cycle based on the above analysis of operation. The capacitor waveforms are omitted due to their simplicity.

Figure 2.2 Waveforms of a buck converter during normal operation



It is important to note that t_{rr} and Q_{rr} disappear from figure 2.2 when majority carrier principle diodes are used. The mathematical average steady-state analysis is presented in the next section.

2.2 Averaged steady-state equivalent model

This section presents the derivation of the averaged steady-state equivalent model using inductor volt-second balance, capacitor charge balance, and input average current principles and the small ripple approximations outlined in [1, 2, 3]. The section is broken up into five subsections: inductor voltage equation, capacitor current equation, input port equation, voltage conversion ratio and efficiency, and equivalent circuit model. The following names, along with those defined in previous subsections, are used to represent the model components.

R_{dson}	Transistor Q on-resistance
R_L	Inductor winding resistance
Vc	Output voltage
V_F	Diode D voltage drop
V_L	Inductor voltage
I_L	Inductor current
I_C	Capacitor current
I_G	Input current
D	Duty cycle
T_S	Switching period
t_r	Transistor voltage rise time
t_f	Transistor voltage fall time
t_{on}	Transistor current rise time
t_{off}	Transistor current fall time
t_{rr}	Silicon diode reverse-recovery time
Q_{rr}	Silicon diode reverse-recovery removed charge

2.2.1 Inductor voltage equation

This subsection illustrates the derivation of the inductor voltage equation using the principle of inductor volt-second balance as defined by equation 2.1.

$$\langle v_L \rangle = 0 \tag{2.1}$$

Using figure 2.1 and figure 2.2 as a guide the average inductor voltage is found to be

$$\langle v_L \rangle = (D + \frac{t_r + t_f}{2T_S})(V_g - V_C - I_L R_{dson}) - (D' - \frac{t_r + t_f}{2T_S})(V_F + V_C) - I_L R_L . \tag{2.2}$$

Replacing the duty cycle with the equivalent duty cycle defined by equations 2.3 and 2.4 transforms equation 2.2 into the simpler form of equation 2.5.

$$D_{eq} = D + \frac{t_r + t_f}{2T_S} \tag{2.3}$$

$$D'_{eq} = 1 - D_{eq} \tag{2.4}$$

$$\langle v_L \rangle = D_{eq}(V_g - V_C - I_L R_{dson}) - D'_{eq}(V_F + V_C) - I_L R_L \tag{2.5}$$

2.2.2 Capacitor current equation

The capacitor current equation is derived below using the capacitor charge balance principal.

$$\langle i_C \rangle = 0 \tag{2.6}$$

$$\langle i_C \rangle = I_L - \frac{V_C}{R} \rightarrow I_L = \frac{V_C}{R} \tag{2.7}$$

2.2.3 Input port equation

The last required equation is derived by averaging the input current.

$$\langle i_g \rangle = \frac{1}{T_S} \int_0^{T_S} i_g \, dt \tag{2.8}$$

$$\langle i_g \rangle = \frac{I_L}{T_S} (DT_S + t_r + t_f + \frac{t_{off} + t_{on}}{2} + t_{rr}) + \frac{Q_{rr}}{T_S} \tag{2.9}$$

$$\langle i_g \rangle = \frac{I_L}{T_S} (D_{eq} T_S + \frac{t_r + t_f + t_{on} + t_{off} + 2t_{rr}}{2}) + \frac{Q_{rr}}{T_S} \tag{2.10}$$

2.2.4 Voltage conversion ratio and efficiency

Using equations 2.5, 2.6 and 2.7 the voltage conversion ratio and efficiency as a function of equivalent duty cycle can be represented as equations 2.11 and 2.13 respectively.

$$\mu(D_{eq}) = \frac{V}{V_g} = \frac{D_{eq} - \frac{V_F}{V_g} D'_{eq}}{1 + \frac{R_{dson} D_{eq} + R_L}{R}} \tag{2.11}$$

$$\eta(D_{eq}) = \frac{P_{out}}{P_{in}} = \frac{V_C I_L}{V_g I_g} \tag{2.12}$$

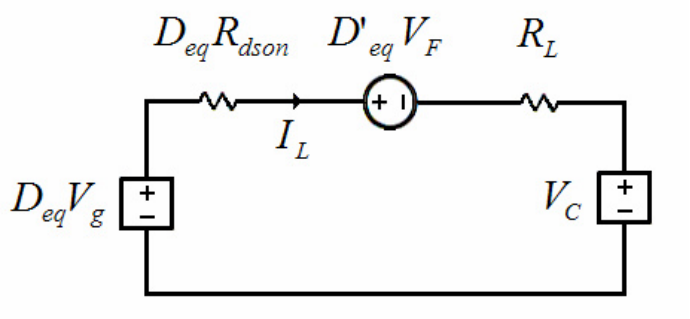
$$\eta(D_{eq}) = \mu(D_{eq}) \frac{I_L}{I_g} = \frac{\mu(D_{eq})}{D_{eq} + \frac{t_r + t_f + t_{off} + t_{on} + 2t_{rr}}{T_S} + \frac{Q_{rr}}{I_L T_S}} \tag{2.13}$$

The significance of the reverse-recovery loss is apparent in equation 2.13: the reverse-recovery time, t_{rr}, is doubled compared to the other switching times. Quantitative results are provided in the experimental prototype section.

2.2.5 Equivalent circuit model

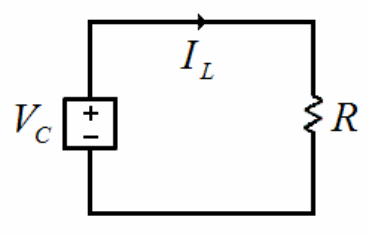
This subsection illustrates equations 2.5, 2.6 and 2.7 in the form of an equivalent circuit model in accordance with [1]. The first part of the equivalent circuit model is derived using equation 2.5 and is shown in figure 2.3.

Figure 2.3 Part of the equivalent circuit model based on inductor voltage equation



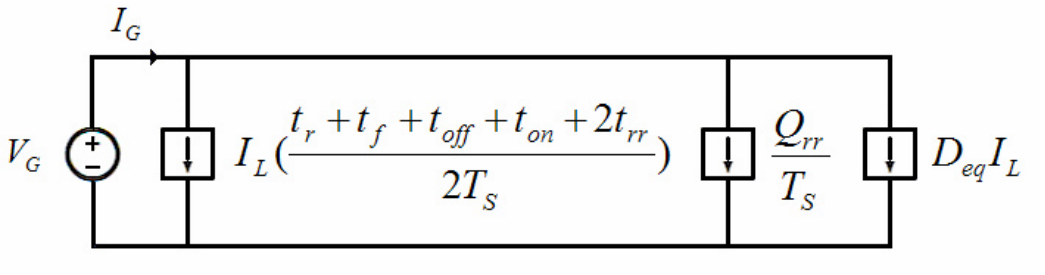
The second part of the equivalent circuit model is derived using equation 2.7 and is shown in figure 2.4.

Figure 2.4 Part of the equivalent circuit model based on capacitor current equation



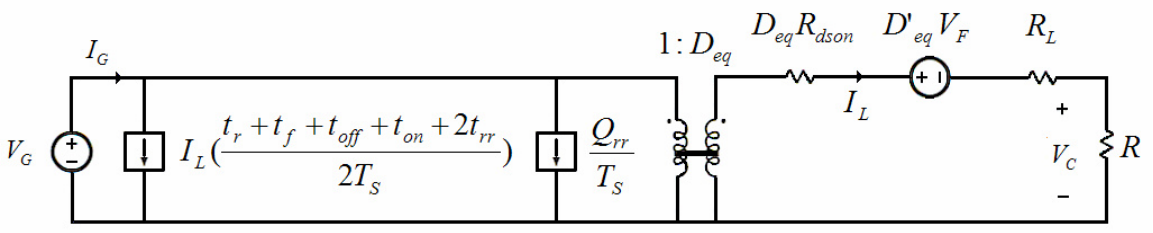
The third and last part of the equivalent circuit model is derived using equation 2.8 and is shown in figure 2.5.

Figure 2.5 Part of the equivalent circuit model based on input port equation



Combining the three parts together leads to the complete circuit model shown in figure 2.6.

Figure 2.6 Complete equivalent circuit model



2.3 Individual power loss analysis

This section illustrates the derivation of the individual power losses. The equations are used in the next section to shed further light on the quantitative significance of the reverse-recovery loss and the benefits of their elimination with SiC diodes. The section is broken up into five parts: inductor conduction loss, transistor conduction loss, diode conduction loss, transistor switching losses and reverse-recovery loss. The derivations are based on the complete equivalent circuit model shown in figure 2.6.

2.3.1 Inductor conduction loss

The inductor conduction loss is proportional to the resistance of the copper and the square of the RMS current that flows through it; however, due to the small ripple-approximation the RMS current is equal to the average current. The relationship is derived below into equation 2.14 and the definition of the resistance is also provided as equation 2.15.

$$P_L = I_L{}^2 R_L \tag{2.14}$$

$$R_L = \rho \frac{l}{A} \tag{2.15}$$

An important uncertainty in equation 2.15 is the temperature dependant resistivity. At room temperature (20˚C) the resistivity of copper is $1.724 \cdot 10^{-6}$ Ω-cm and $2.3 \cdot 10^{-6}$ Ω-cm at 100˚C, a 1.33 increase. In light of this discrepancy the working temperature of the converter is assumed to be 20˚C for the rest of the analysis. This is in accordance with standard inductor design principles.

2.3.2 Transistor conduction loss

The transistor conduction loss is subject to the combination of the equivalent duty cycle, transistor on-resistance and the square of the inductor current as is shown in figure 2.6.

$$P_{dson} = I_L{}^2 R_{dson} D_{eq} \tag{2.16}$$

2.3.3 Diode conduction loss

The diode conduction loss is the product of the inverse of the equivalent duty cycle, the diode on voltage drop and the inductor current.

$$P_d = V_F I_L D'_{eq} \tag{2.17}$$

2.3.4 Transistor switching losses

The transistor switching losses are composed of the transistor turn-on and turn-off losses imposed by the charging and discharging of the transistor gate-to-source and gate-to-drain capacitances.

$$P_{sw} = \frac{1}{2} V_g I_L \frac{t_{on} + t_r + t_f + t_{off}}{T_S} \tag{2.18}$$

2.3.5 Reverse-recovery loss

The reverse-recovery loss is a product of the removal of the stored minority charge. As such, it is relative to the reverse-recovery time and the removed minority charge. It is not present when majority carrier principle diodes are used.

$$P_{rr} = \frac{V_g I_L t_{rr} + V_g Q_{rr}}{T_S} \tag{2.19}$$

2.4 Experimental prototype

This section outlines the construction of a 32 kHz 1000 W conventional buck converter equipped both with ultrafast Si and SiC diodes. A theoretical analysis of the converter, based on the derived equations from previous sections, is also provided. The section is broken up into three parts: active component selection, inductor construction and theoretical analysis of prototype.

2.4.1 Active component selection

The components were selected in accordance with operational requirements and care was taken to select state-of-the-art devices. The component selection is shown in table 2.1.

Table 2.1 Conventional buck active component characteristics

Component	**Name**	**Manufacturer**	**$V_{breakdown}$**	**I_{max}**
Transistor	SPW47N60C3	Infineon	650 V	56 A
Diode (Si)	APT30DQ100BG	Microsemi	1000 V	30 A
Diode (SiC)	SDT12S60	Infineon	600 V	12 A

All of the active components were employed parallel in groups of three in order to decrease conduction losses.

2.4.2 Inductor construction

The construction of the inductor was based on the specification of the current ripple. In accordance, the current ripple was chosen to be 10% of the average current at 700W, 1.5 Amps for an output voltage of 48 V. This goal was achieved with an 506 μH inductor constructed in two parts: the first part was composed of two 77439A7 cores wound 29 times with two paralleled AWG 12 copper wires and the second part composed of two 77439A7 cores wound 24 times with two paralleled AWG 12 copper wires. The inductance was determined using the inductor voltage equation rearranged as shown in equation 2.20.

$$L = \frac{V_C D' T_S}{2\Delta i_L} \tag{2.20}$$

The 77439A7 core was chosen because it comfortably satisfied the magnetic field intensity requirement, 5600 ampere-turns per meter at 1000W. In addition, two cores were used in order to keep the magnetic losses to a minimum, keeping the magnetic flux density below 0.04T and the core losses below 850mW per part. Also, the copper gauge was chosen using the conservative 700 circular mils per amp rule. It is important to note that the inductor was over-engineered on purpose so that it could be used in the isolated current-fed buck.

2.4.3 Theoretical analysis of the prototype

In order to shed light on the potential benefits of the use of SiC diodes in the conventional buck converter a theoretical analysis is presented below. The component information is shown below and is based on component datasheets.

P_{out}	:	800 W
V_C	:	48 V
V_F (Ultrafast)	:	1.2 V
V_F (SiC)	:	1.25 V
R_{dson}	:	0.02 Ω
R_L	:	0.01275 Ω
R	:	3 Ω
t_r	:	35 ns
t_f	:	40 ns

t_{off} : 6.94 ns

t_{on} : 4.63 ns

t_{rr} : 50 ns

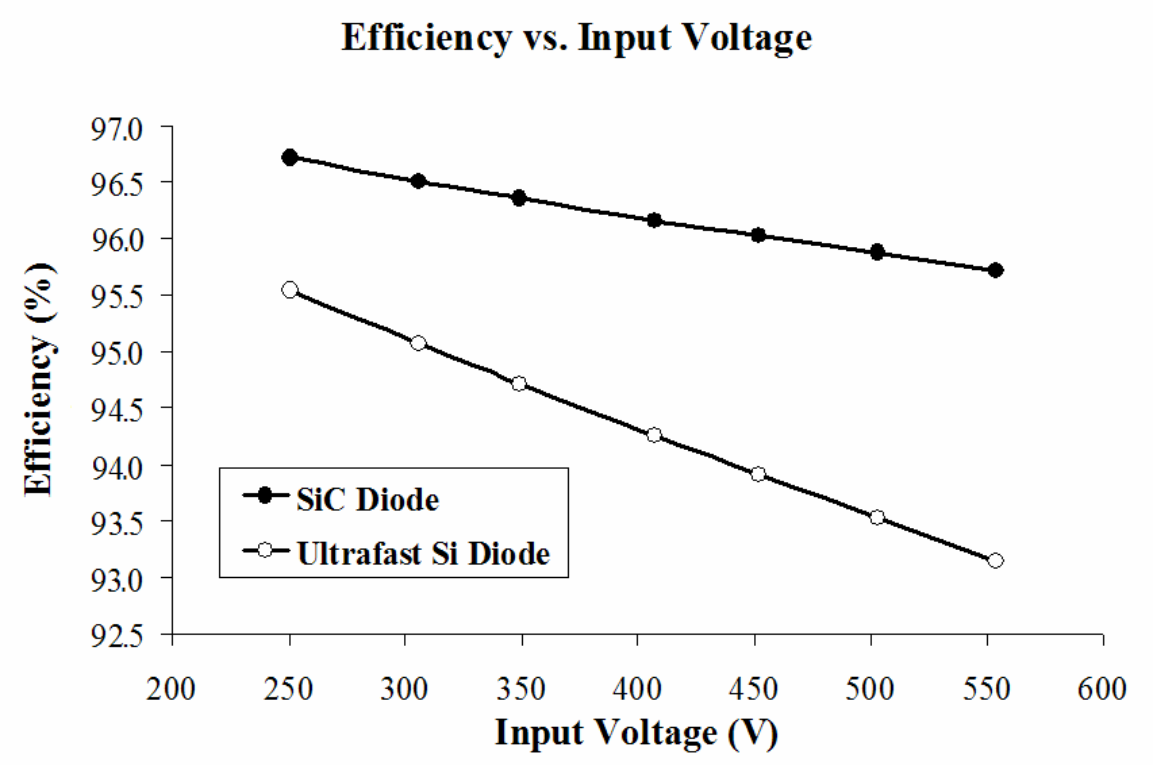
Q_{rr} : 400 nF

I_L : 16.67 A

f_S : 32 kHz

The efficiency vs. input voltage with constant output voltage of the conventional buck converter equipped with SiC and ultrafast Si diodes is presented in figure 2.7.

Figure 2.7 Theoretical efficiency vs. input voltage with constant output voltage of the buck converter



The improvement in efficiency due to the use of the SiC diode is exceptional, more so at higher input voltages. An investigation of the individual losses provides the explanation of the above results and is presented in figure 2.8 and figure 2.9.

Figure 2.8 Individual losses of a conventional buck converter with Si diodes

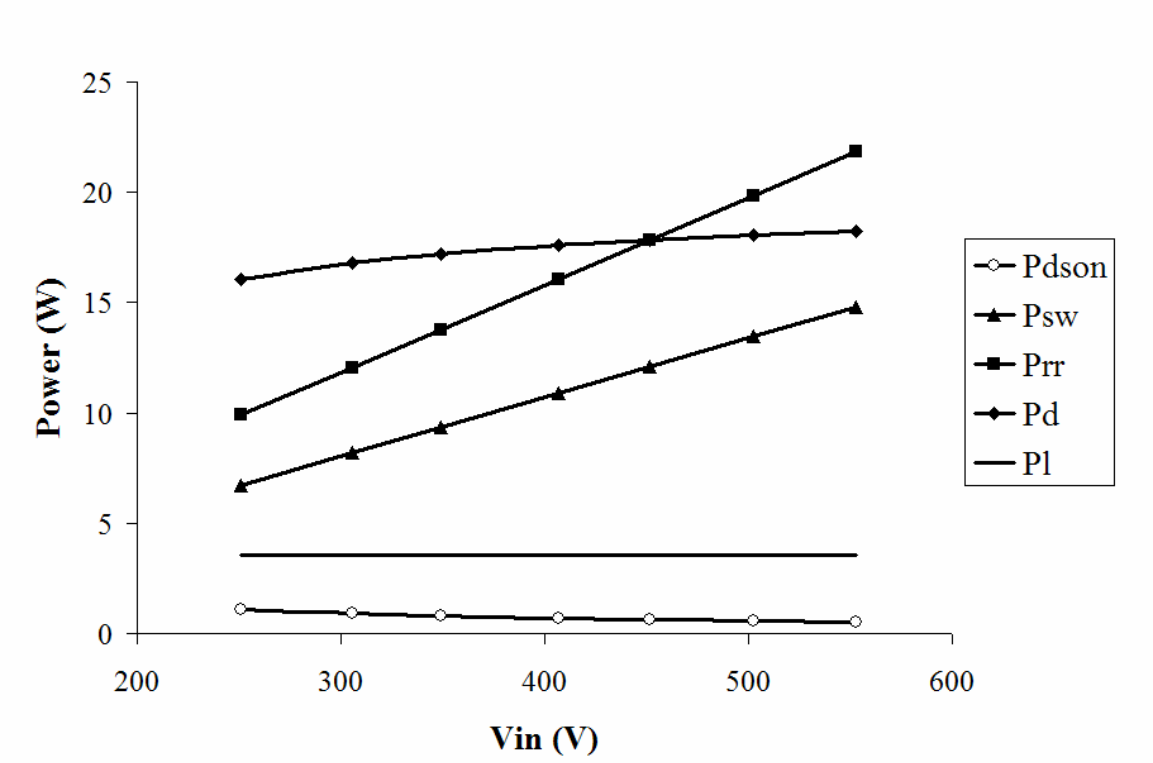


Figure 2.9 Individual losses of a conventional buck converter with SiC diodes

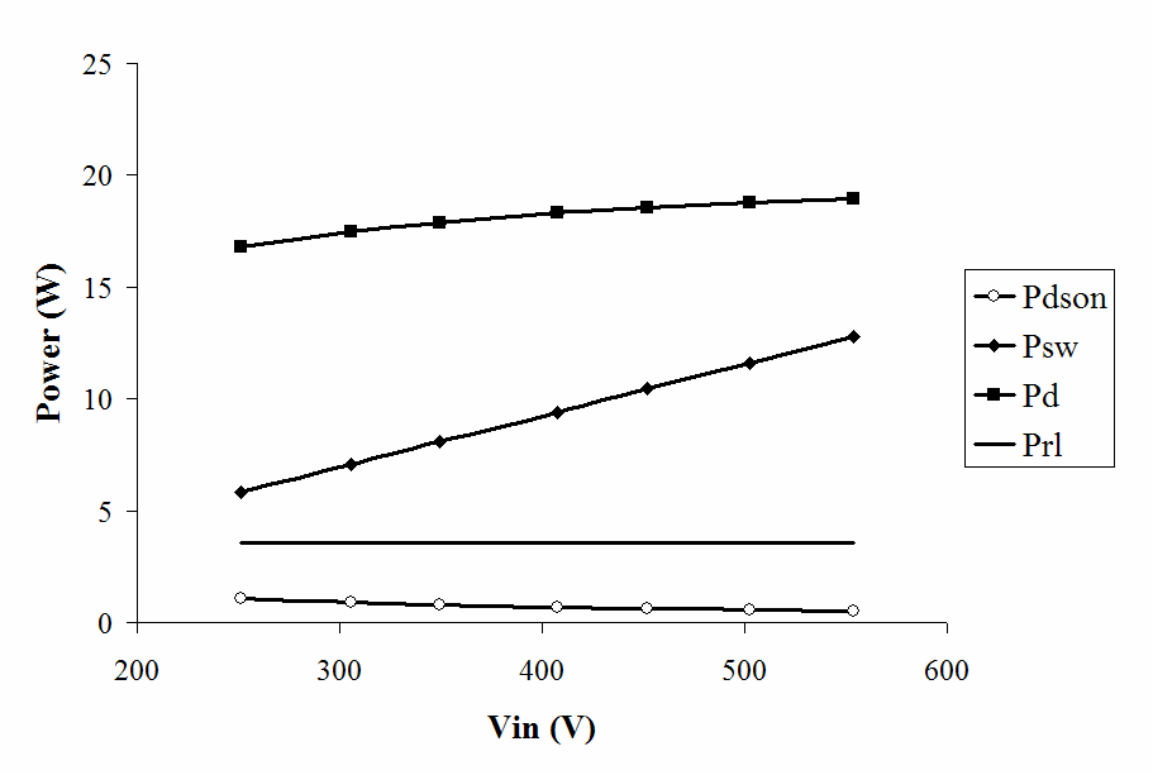
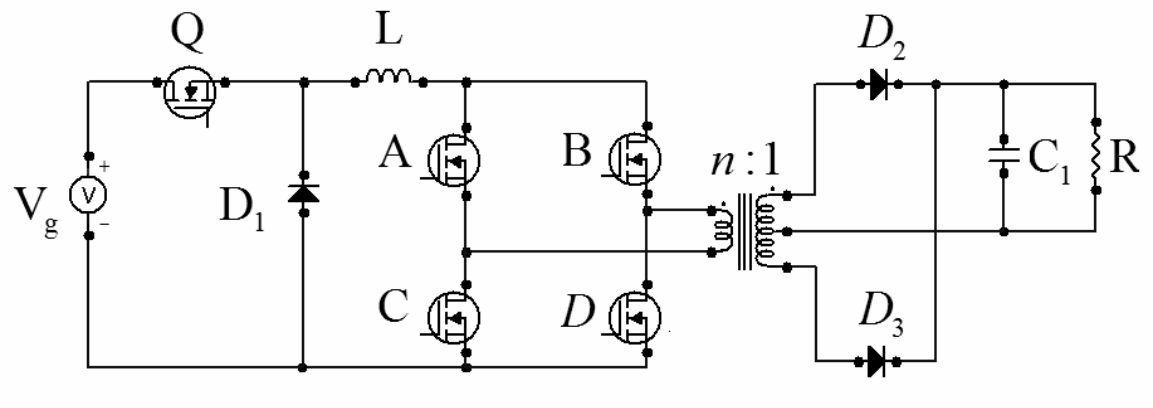


Figure 2.8 clearly illustrates the significance of the reverse-recovery process, providing strong evidence that the SiC diode is superior to the ultrafast Si diode at the 800W power output levels. Experimental results provide further benchmarks and can be found in the fourth chapter.

3 ISOLATED CURRENT-FED BUCK

The theoretical analysis of the isolated current-fed buck converter, shown in figure 3.1, is presented in this chapter. The analysis is broken up into four sections: analysis of operation, steady-state equivalent circuit model derivation, individual power losses and experimental prototype discussion.

Figure 3.1 Schematic of isolated current-fed buck converter

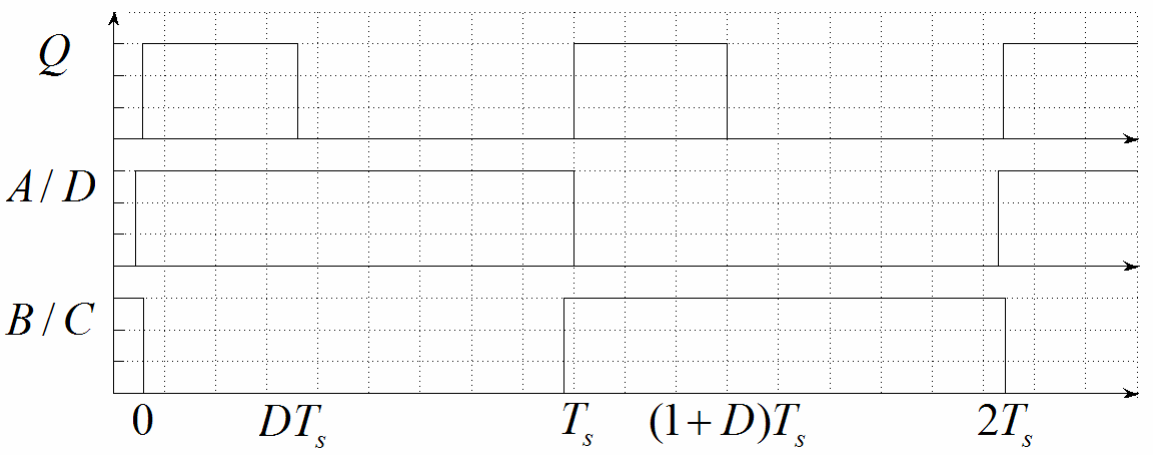


3.1 Analysis of operation

During a normal operating cycle the isolated current-fed buck converter goes through seven distinct stages. In this analysis the definition of a stage is expanded in order to keep the number of stages reasonable. In addition, the use of a minority carrier or majority carrier principle diode only serves to vary the time of one of the stages and as such only the minority carrier principle diode variant is examined. The full-bridge,

transistors A, B, C and D in figure 3.1, is operated at 50% duty cycle with a small overlap as shown in figure 3.2.

Figure 3.2 Isolated current-fed buck control signals



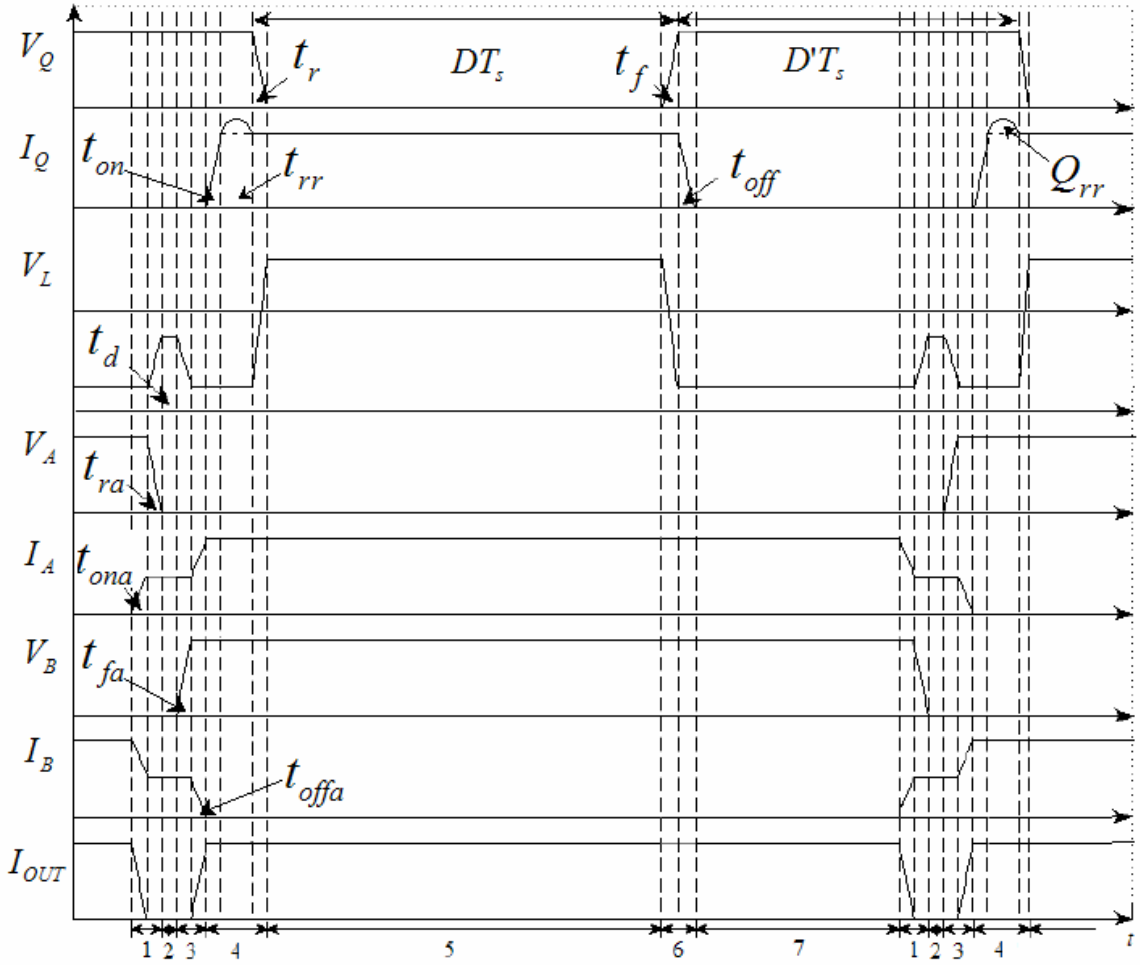
The above control scheme ensures an effective path for the inductor current to commute through at all times. The stages are numbered in accordance with figure 3.3.

1. Transistors A and D switch on, experiencing switching losses due to transistor gate-to-source and gate-to-drain capacitances.
2. Transistors A, B, C and D are on, ensuring a path for the inductor current during the full-bridge switch from the B/C conduction path to the A/D conduction path.
3. Transistors B and C switch off.
4. Transistor Q switches on, removing minority charge from the diode until it is reverse-biased.
5. Transistor Q is on and the diode off. The inductor is charged by the input source.
6. Transistor Q switches off.

7. Transistor Q is off and the diode on. The inductor is drained via a path through the diode.

Figure 3.3 illustrates the input transistor, full-bridge A and B transistors, and inductor voltage waveforms and input transistor, full-bridge A and B transistors and transformer combined output current waveforms of a normal operating cycle based on the above analysis of operation.

Figure 3.3 Isolated current-fed buck converter current and voltage waveforms



The magnetizing current is neglected in the above analysis and as such only one cycle is described.

3.2 Steady-state equivalent circuit model

This section presents the derivation of the averaged steady-state equivalent model using inductor volt-second balance, capacitor charge balance, and input average current principles and the small ripple approximations [1, 2, 3]. The section is broken up into five subsections: inductor voltage equation, capacitor current equation, input port equation, voltage conversion ratio and efficiency, and equivalent circuit model. The following names, along with those defined in previous subsections, are used to represent the model components.

R_{pri}	Transformer primary winding resistance
R_{sec}	Transformer secondary winding resistance
R_H	Full-bridge transistor on-resistance
R_Q	Transistor Q on-resistance
R_L	Inductor winding resistance
V_{D1}	Diode D1 voltage drop
V_{D2}	Diode D2, D3 voltage drop
V_C	Output voltage
V_L	Inductor voltage
I_L	Inductor current
I_G	Input current
n	Transformer turns ratio
D	Duty cycle

T_S	Transistor Q switching period
t_r	Transistor Q voltage rise time
t_f	Transistor Q voltage fall time
t_{on}	Transistor Q current rise time
t_{off}	Transistor Q current fall time
t_{offa}	Transistor A/B/C/D current fall time
t_{ona}	Transistor A/B/C/D current rise time
t_{fa}	Transistor A/B/C/D voltage fall time
t_{ra}	Transistor A/B/C/D voltage rise time
t_d	Full-bridge dead time
t_{rr}	Silicon diode reverse-recovery time
Q_{rr}	Silicon diode reverse-recovery removed charge

In addition, several time constants and an equivalent duty cycle are defined for convenience, denoted by equations 3.1-3.6.

$$t_1 = t_d + \frac{t_{fa} + t_{ra}}{2} \tag{3.1}$$

$$t_2 = \frac{t_r + t_f + t_{on} + t_{off} + 2t_{rr}}{2} \tag{3.2}$$

$$t_3 = t_d + t_{fa} + t_{ra} + \frac{t_{ona} + t_{offa}}{2} \tag{3.3}$$

$$t_4 = t_d + t_{fa} + t_{ra} \tag{3.4}$$

$$D_{eq} = D - \frac{t_r + t_f}{2T_S} \tag{3.5}$$

$$D'_{eq} = 1 - D_{eq} \tag{3.6}$$

3.2.1 Inductor voltage equation

The inductor voltage equation is provided below and was derived using the inductor volt second balance principal.

$$\begin{aligned}\langle v_L \rangle &= D_{eq}V_g - I_L(D_{eq}R_Q + R_L + (R_1 + n^2R_2)(1-\frac{t_3}{T_S}) + 2R_H(1-\frac{t_1}{2T_S})) \\ &- nV_C(1-\frac{t_1}{T_S}) - nV_{F2}(1-\frac{t_4}{T_S}) - V_{F1}D'_{eq} = 0\end{aligned} \tag{3.7}$$

3.2.2 Capacitor current equation

The capacitor current equation is provided below and was derived using the capacitor charge balance principal with the help of figure 3.3.

$$\langle i_C \rangle = nI_L(1-\frac{t_3}{T_S}) - \frac{V}{R} = 0 \rightarrow I_L = \frac{V}{nR(1-\frac{t_3}{T_S})} \tag{3.8}$$

3.2.3 Input port equation

The input port equation is provided below and was derived by averaging the input current over one switching period.

$$\left\langle i_g \right\rangle = I_L (D_{eq} + \frac{t_2}{T_S}) + \frac{Q_{rr}}{T_S} \tag{3.9}$$

3.2.4 Voltage conversion ratio and efficiency

Using equations 3.7, 3.8 and 3.9 the voltage conversion ratio and efficiency as a function of equivalent duty cycle can be represented as equations 3.10 and 3.11 respectively.

$$\mu(D_{eq}) = \frac{V_C}{V_G} = \frac{\frac{D_{eq}}{n} - \frac{V_{D2}}{V_G}(1 - \frac{t_4}{T_s}) - \frac{V_{D1}}{nV_G} D'_{eq}}{1 - \frac{t_1}{T_S} + \frac{D_{eq} R_Q + R_L + (1 - \frac{t_3}{T_S})(R_{pri} + n^2 R_{\sec}) + 2R_H (1 - \frac{t_1}{2T_S})}{n^2 R(1 - \frac{t_3}{T_S})}} \tag{3.10}$$

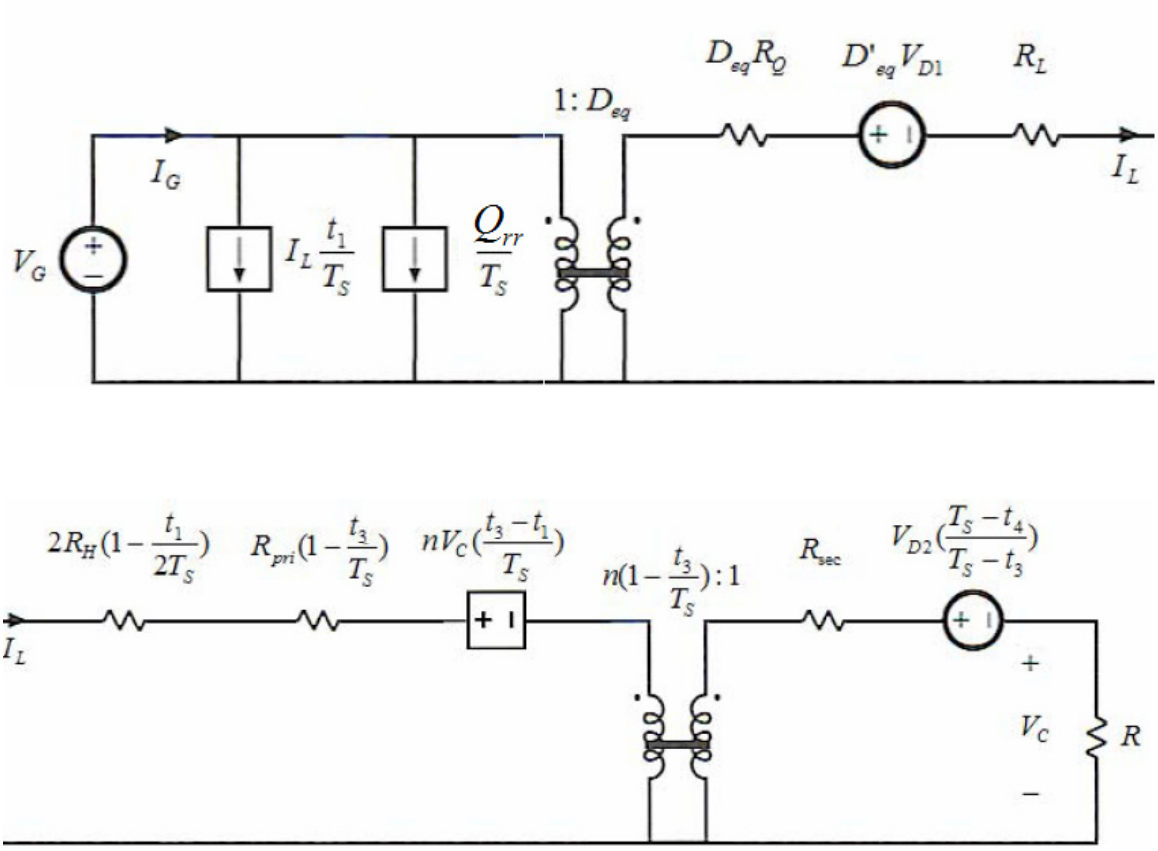
$$\eta(D_{eq}) = \frac{P_{out}}{P_{in}} = \frac{n(1 - \frac{t_3}{T_S})}{D_{eq} + \frac{t_2}{T_S} + \frac{Q_{rr}}{I_L T_S}} \mu(D_{eq}) \tag{3.11}$$

The above equations are non-trivial to decode and further analysis is needed.

3.2.5 Equivalent circuit model

The complete equivalent circuit model was derived using equations 3.7, 3.8 and 3.9 and is shown in two parts below for better presentability.

Figure 3.4 Equivalent circuit model of the isolated current-fed buck



3.3 Individual power losses

This section illustrates the derivation of the individual power losses in the same manner as section 2.3. The section is broken up into nine parts: inductor conduction loss, input port transistor conduction loss, full-bridge transistor conduction loss, transformer conduction loss, input port diode conduction loss, rectifying diode conduction loss, input port transistor switching loss, full-bridge transistor switching loss and reverse-recovery

loss. The derivations are based on the complete equivalent circuit model shown in figure 3.4.

3.3.1 Inductor conduction loss

The inductor conduction loss is easily extracted from figure 3.4 and is defined by equation 3.12. It is important to note that the reduction of the inductor current leads to significant loss reductions compared to the conventional buck converter.

$$P_L = I_L{}^2 R_L \tag{3.12}$$

3.3.2 Input port transistor conduction loss

The above step is repeated for the input port transistor conduction loss and is shown below. The same significant reduction is also present in this case; however, the loss is smaller due to the increased equivalent duty cycle.

$$P_{Qdson} = D_{eq} I_L{}^2 R_Q \tag{3.13}$$

3.3.3 Full-bridge transistor conduction loss

The full-bridge transistor conduction loss is composed of the full bridge transistor on-resistances. Majority of the time the total on-resistance is the sum of one active leg; however, during the transition between full-bridge legs the total resistance is halved due to the fact that all four transistors are active.

$$P_{Hdson} = 2I_L{}^2 R_H (1 - \frac{t_1}{2T_S}) \tag{3.13}$$

3.3.4 Transformer conduction loss

The transformer transfer energy from the input port to the output load at all times except during the transition of the full-bridge conduction paths. The overall transformer conduction loss is presented by equation 3.14.

$$P_{tr} = I_L{}^2 (1 - \frac{t_3}{T_S})(R_1 + n^2 R_2) \tag{3.14}$$

3.3.5 Input port diode conduction loss

The input port diode conduction loss is subject to the inverse of the equivalent duty cycle and is presented by equation 3.15. The expected reduction in losses compared to the

conventional buck diode conduction loss is two fold: the inductor current is reduced along side the inverse of the equivalent duty cycle.

$$P_{D1} = V_{D1} I_L D'_{eq} \tag{3.15}$$

3.3.6 Rectifying diode conduction loss

The rectifying diode conduction loss is subject to the transformer output current; therefore, during the full-bridge conduction path transition, when the current is flowing through all four transistors, it is zero. It is important to note that the diode is modeled as a constant voltage drop, as denoted in [1].

$$P_{D2} = nV_{D2} I_L (1 - \frac{t_4}{T_S}) \tag{3.16}$$

The overall diode conduction losses of the isolated current-fed buck may be comparable to the conventional buck due to the fact that the rectifying diodes have lower voltage breakdown requirements and smaller on-voltages. The full benefits will be discussed in the theoretical analysis in the next section.

3.3.7 Input port transistor switching losses

The input port transistor switching losses are self explanatory and are presented in equation 3.17. Reductions are expected compared to the conventional buck losses due to the decreased inductor current.

$$P_{Qsw} = V_g I_L \frac{t_r + t_f + t_{on} + t_{off}}{2T_S} \tag{3.17}$$

3.3.8 Full-bridge transistor switching losses

The full-bridge transistor switching losses are subject to the same principles as the input port transistor switching losses and are presented in equation 3.18.

$$P_{Hsw} = nV_C I_L \frac{t_{ra} + t_{fa} + t_{ona} + t_{offa}}{2T_S} \tag{3.18}$$

3.3.9 Reverse-recovery loss

The reverse-recovery loss equation is identical to the conventional buck and is shown in equation 3.19.

$$P_{rr} = V_g \frac{I_L t_{rr} + Q_{rr}}{T_S} \tag{3.19}$$

3.4 Experimental prototype

This section outlines the construction of a 32 kHz 2.0 kW isolated buck converter equipped both with ultrafast Si and SiC diodes. The isolated buck converter prototype is based on the conventional buck converter prototype described in the previous chapter. One benefit from the re-use of the conventional buck converter is the fact that higher output power levels can be achieved with the same components. A theoretical analysis of the converter, based on the derived equations from previous sections, is also provided. The section is broken up into five parts: active component selection, inductor construction, transformer construction, full-bridge over-voltage and theoretical analysis of prototype.

3.4.1 Components

The components were selected in accordance with operational requirements and care was taken to select state-of-the-art devices. The component selection is shown in table 3.1.

Table 3.1 Isolated current-fed buck active component characteristics

Component	**Name**	**Manufacturer**	**$V_{breakdown}$**	**I_{max}**
Full-bridge Transistor	IXFK140N30P	IXYS	300 V	140 A
Rectifying Diode (Schottky)	STPS80170C	ST	170 V	80 A

3.4.2 Inductor construction

Due to the low front end current a more liberal current ripple was selected. In accordance, the current ripple was chosen to be 50% of the average current at 800W, 2.5 Amps for an output voltage of 48 V and a transformer conversion ratio of 3.375. The increased conduction losses due to the high current ripple are 4.08% at the 800W output power level. The current ripple was achieved with an 803 μH inductor constructed in two parts: the first part was composed of two 77439A7 cores wound 29 times with two paralleled AWG 12 copper wires and the second part composed of three 77439A7 cores wound 37 times with two paralleled AWG 12 copper wires. The first part was re-used from the conventional buck converter and the second constructed from scratch.

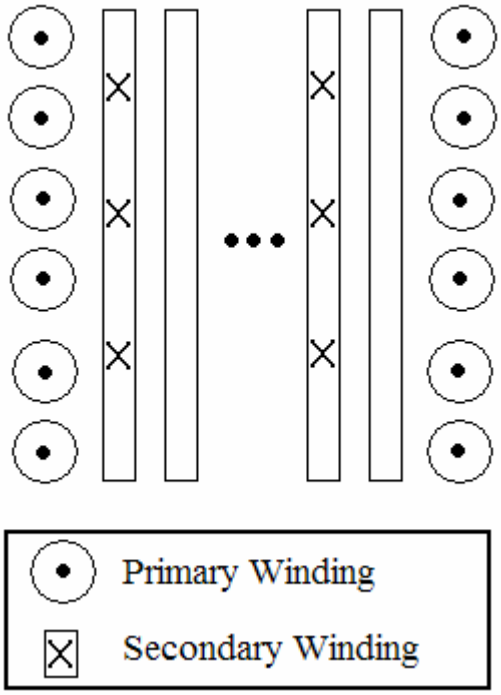
3.4.3 Transformer construction

The transformer was constructed using the K_g method outlined in [1], while taking into account the skin depth, proximity effect and leakage inductance. The leakage inductance was an important consideration given that it would lead to losses and full-bridge over-voltage conditions. The quantities used with the K_g method are shown below for a 2500 W output power level at 60 V.

ρ	0.000001724 Ω-cm
Itot	54.1 A
n_2/n_1	3.33
λ_1	0.012903 V-sec
K_u	0.25
β	2.7
K_{fe}	6.544759237 $W/T^{\beta}cm^3$
Core	2 x E80 (N27) 0R-48020-EC
A_c	8 cm^2
W_A	11 cm^2
MLT	15.8 cm
l_m	18.4 cm
ΔB	0.25 T

The results of the Kg method are a transformer with 27 primary turns and 8 secondary turns. The equivalent copper wire gauge of the two sides is AWG #14 and AWG #10 respectively. In order to decrease the proximity effect and subsequently the transformer leakage inductance the two sides were interleaved and modified such that the wire radius was less than the skin depth, 0.0593 cm. The primary side was constructed using three AWG #18 copper wires and the secondary side using two bifilarly interleaved 4.826 cm x 0.0254 cm foils. The interleaving scheme is shown in figure 3.5.

Figure 3.5 Isolated current-fed transformer interleaving scheme



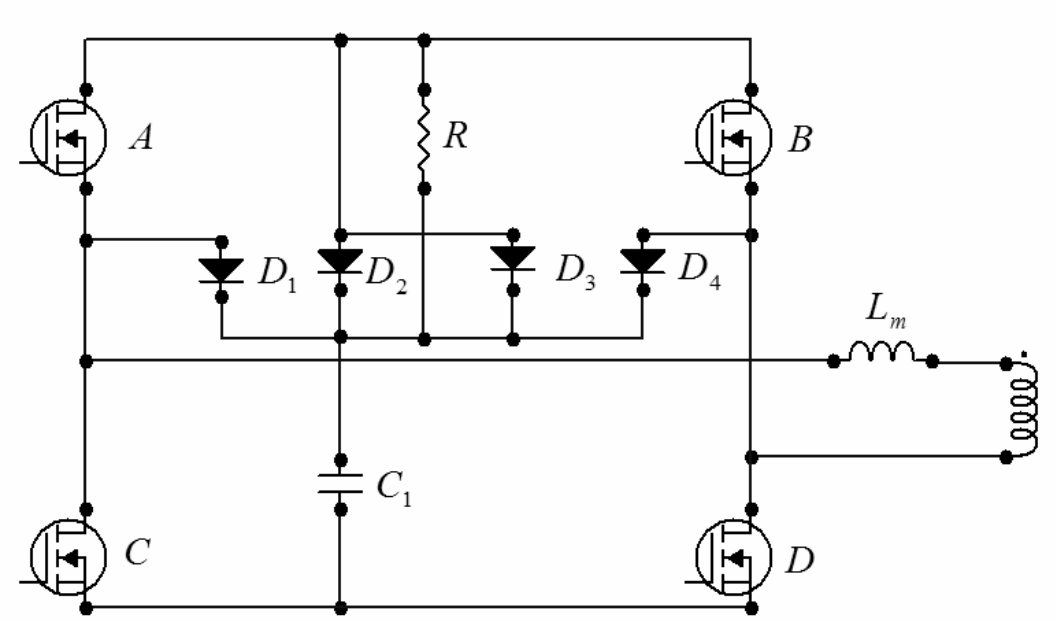
The primary winding is divided into two layers consisting of 14 and 13 turns respectively and the secondary winding is composed of 8 turns. The above scheme decreases the proximity effect and leakage inductance by minimizing the MMF and by insuring high

coupling. In addition, the dc resistance of the second winding is increased, due to the proximity effect, by a factor of 1.5 as shown by [1, p. 519]. The leakage inductance of the transformer was measured to be 4.2 μH.

3.4.4 Full-bridge over-voltage

Due to the leakage inductance of the transformer the full-bridge experiences over-voltage conditions during the full-bridge conduction path transition. A snubber minimizes the over-voltage and is shown in figure 3.6.

Figure 3.6 Isolated current-fed snubber schematic



The snubber relies on the C1 capacitor to control the full-bridge over-voltage caused by the transformer leakage inductance.

The snubber was designed to work up to the 2.4 kW output power level and exhibit a three time constant asymptotic voltage decline. The transformer leakage inductance power at the 2.4 kW level is 14.75 W. In accordance, the snubber components are shown in table 3.2.

Table 3.2 Snubber component characteristics

Component	**Part Name**	**Characteristic**
R	CB 15 27 5% B	27 Ω, 15W
D1/D2/D3/D4	RHRG3060	600V, 30A
C1		330nF, 300V

3.4.5 Theoretical analysis of the prototype

In order to shed light on the potential benefits of the use of SiC diodes in the isolated current-fed buck converter a theoretical analysis is presented below. The component information is shown below and is based on component datasheets.

P_{out} : 800 W

V_C : 48 V

V_{D1} (Ultrafast): 1.0 V

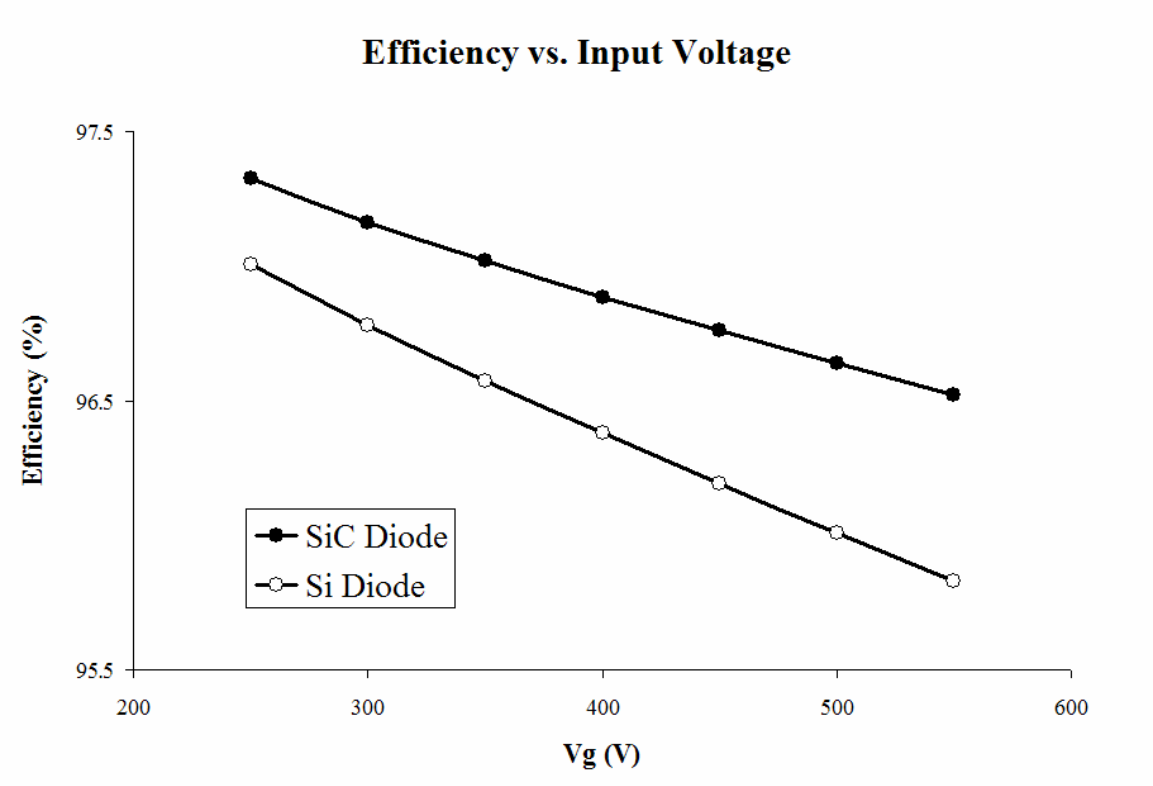
V_{D1} (SiC) : 1.05 V

V_{D2} : 0.65 V

R_{qdson}	:	0.02 Ω
R_{hdson}	:	0.024 Ω
R_1	:	0.017623 Ω
R_2	:	0.003105 Ω
R_L	:	0.015877 Ω
R	:	2.88 Ω
t_r	:	35 ns
t_f	:	40 ns
t_{off}	:	2.077 ns
t_{on}	:	1.385 ns
t_{rr}	:	30 ns
t_d	:	150 ns
Q_{rr}	:	200 nF
I_L	:	4.985 A
n	:	3.375
f_S	:	32 kHz

The efficiency vs. input voltage with constant output voltage of the isolated buck converter equipped with SiC and ultrafast Si diodes is presented in figure 3.7.

Figure 3.7 Theoretical efficiency vs. input voltage with constant output voltage of the isolated current-fed buck converter



The improvement in efficiency due to the use of the SiC diode is significant, more so at higher input voltages. The above efficiency vs. input voltage analysis does not include magnetic core losses; therefore, experimental efficiencies will be lower. An investigation of the individual losses provides the explanation of the above results and is presented in figures 3.8 and 3.9.

Figure 3.8 Individual losses of the isolated current-fed buck with SiC diode

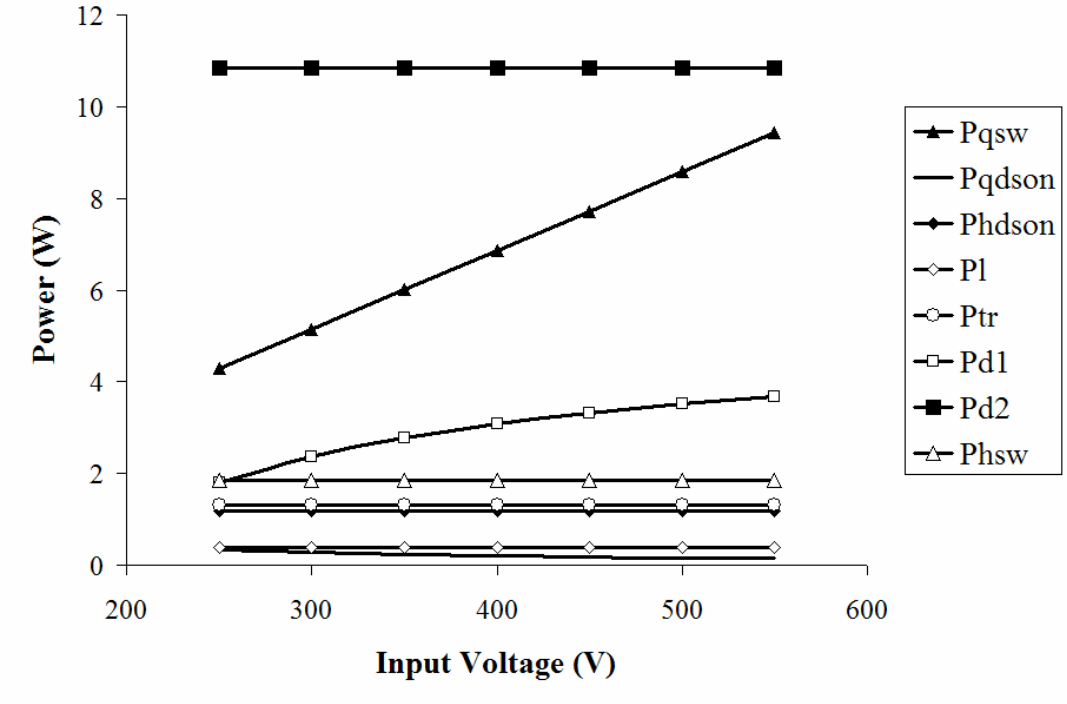
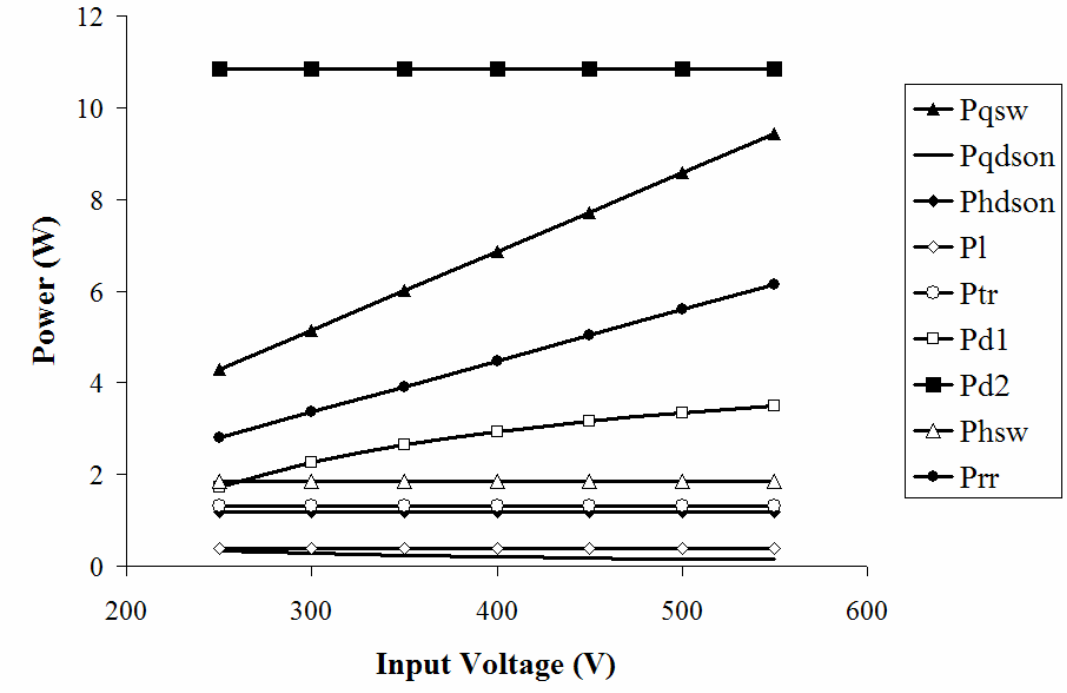


Figure 3.9 Individual losses of the isolated current-fed buck with Si diode



The isolated current-fed buck topology effectively reduces the reverse-recovery loss and the transistor switching losses compared to the conventional buck topology; however, it does this at the cost of increased overall conduction losses and magnetic core losses.

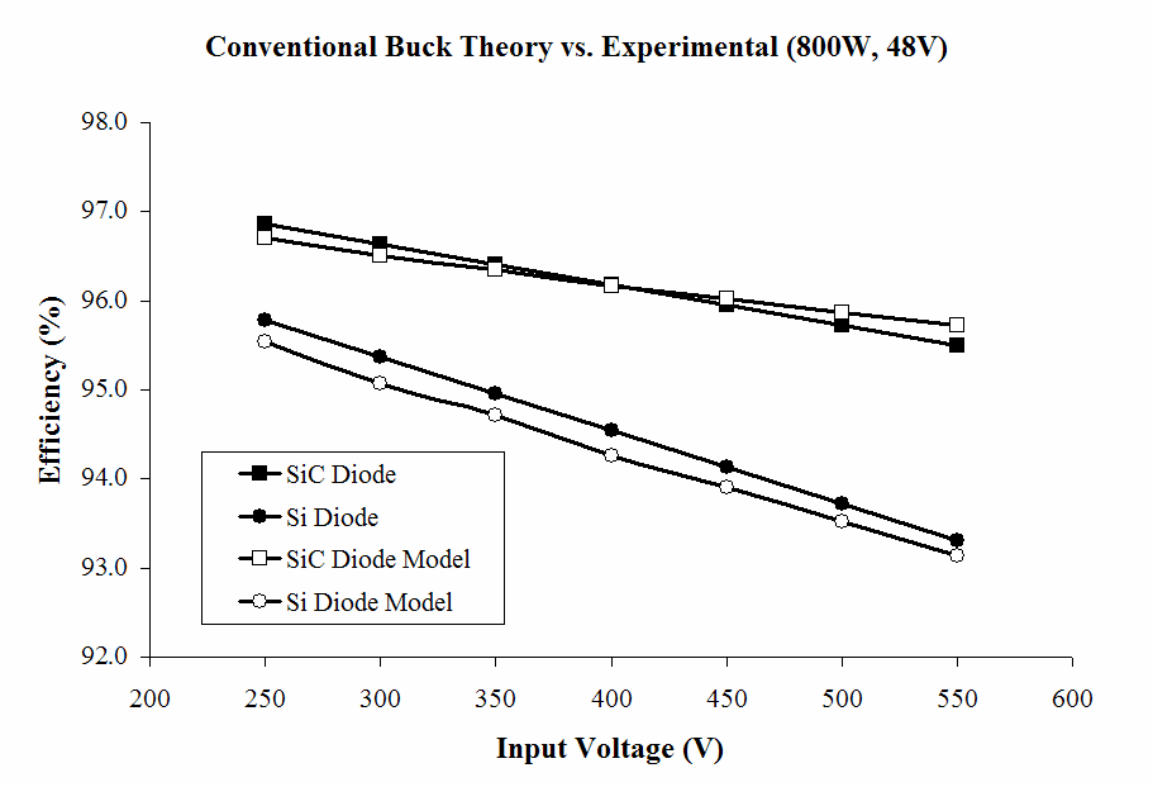
4 EXPERIMENTAL RESULTS

The experimental results of the two prototypes, described in sections 2.3 and 3.4, are comparatively presented in this section. The experimental data is obtained through the measurement of the terminal parameters with current shunt resistors. The results are organized in three parts: efficiency vs. input voltage, load regulation and cost analysis.

4.1 Efficiency vs. input voltage

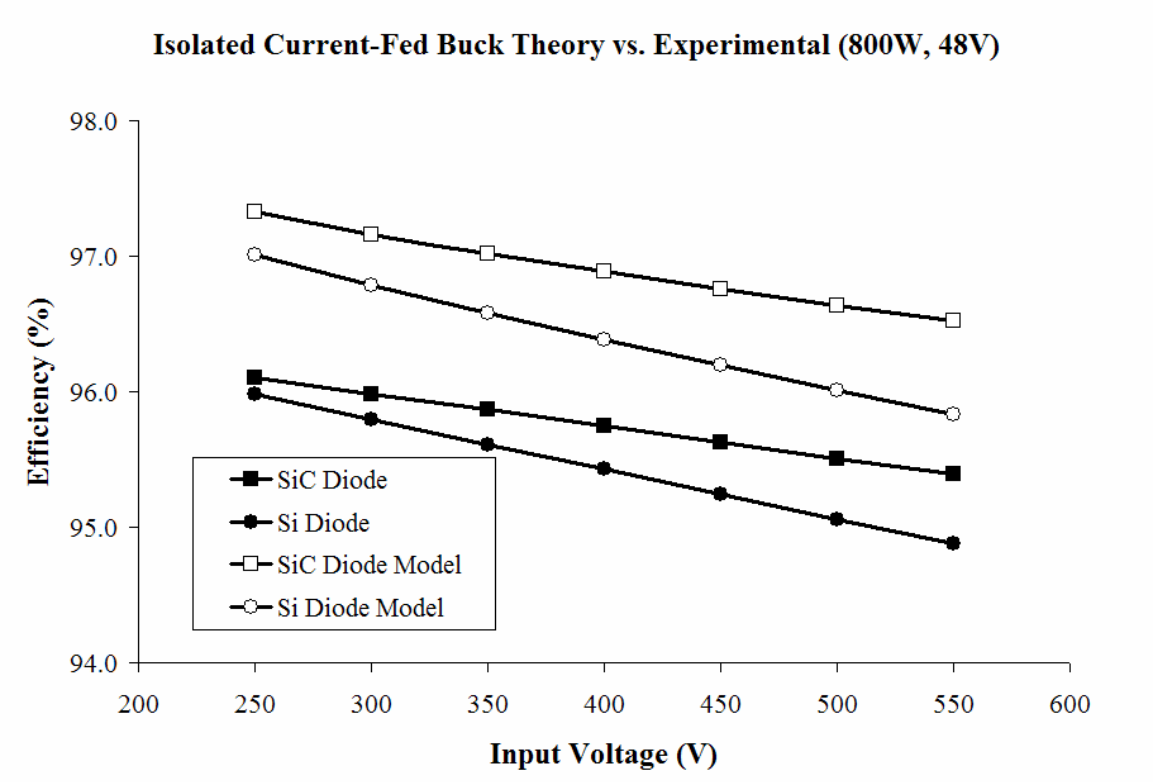
The efficiency vs. input voltage characteristics of the conventional buck and isolated current-fed buck are shown in the figures below. The theoretical predictions are also provided in figures 4.1 and 4.2 for the conventional buck and isolated current-fed buck respectively.

Figure 4.1 Theoretical and experimental efficiency vs. input voltage with constant output voltage of conventional buck



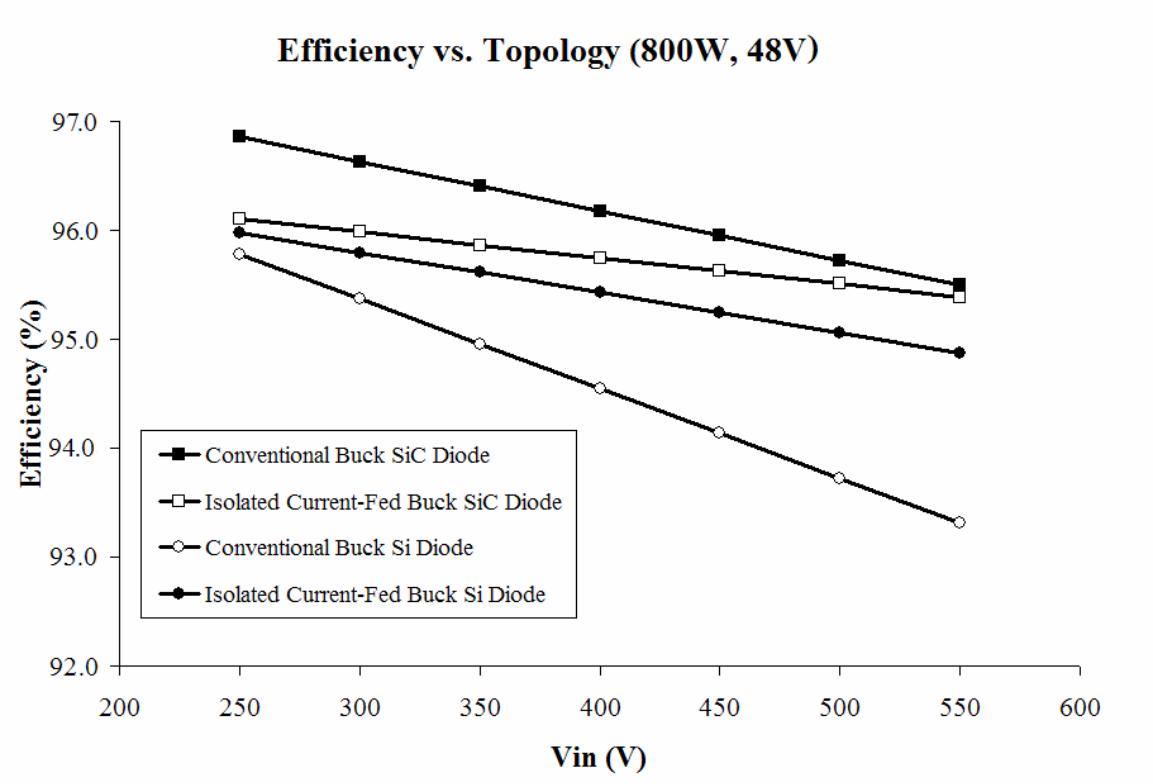
The theoretical and experimental results are within 0.3% of each other and exhibit the same trends, namely the superior efficiency vs. input voltage characteristics of the conventional buck equipped with SiC diodes. Figure 4.2 illustrates the differences between the theoretical and experimental results for the isolated current-fed buck.

Figure 4.2 Theoretical and experimental efficiency vs. input voltage with constant output voltage of isolated current-fed buck



The theoretical and experimental curves in the figure above share the same trend and the differences can be attributed mainly to the lack of magnetic core loss considerations in the model since the difference is constant between the two sets of data. The experimental results of the four converter variants are shown in figure 4.3.

Figure 4.3 Experimental efficiency vs. input voltage with constant output voltage results at 800W output power

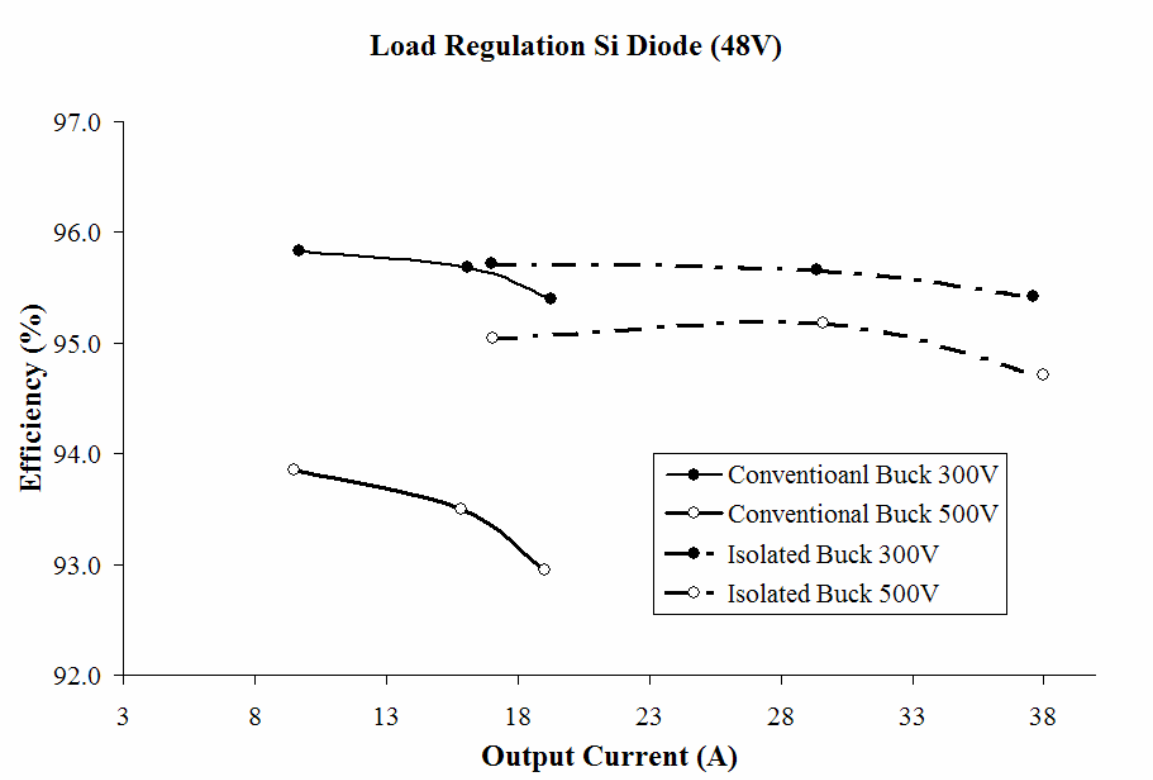


At the 800W output power level the conventional buck, equipped with SiC diodes, is the most efficient variant. The isolated current-fed buck, equipped with SiC diodes, is the second most efficient variant. In fact, for voltage levels above 450 volts it is almost undistinguishable from the conventional buck. The isolated current-fed buck, equipped with Si diodes, is a close third most efficient variant. In the last position is the conventional buck equipped with Si diodes. The load regulation characteristics of the four variants are provided in the next section.

4.2 Load regulation

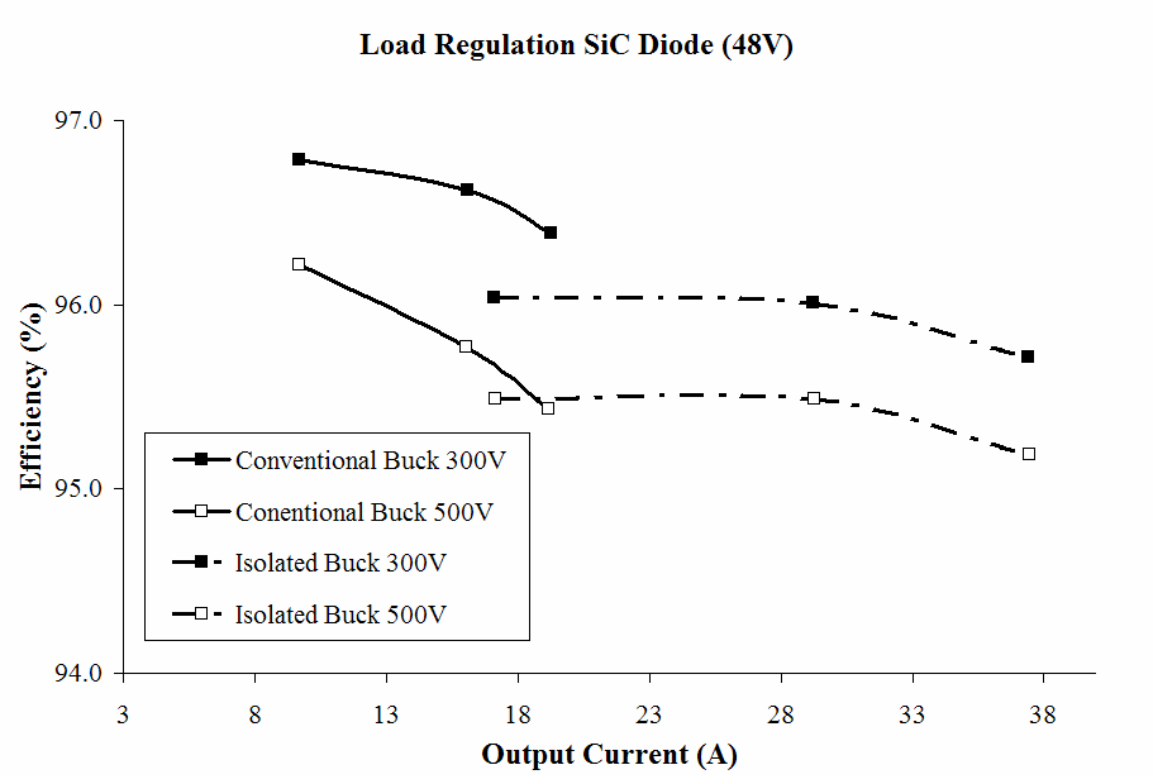
The load regulation characteristics of the conventional buck and isolated current-fed buck converters are presented in the figures below. The conventional buck converter results are in the 500 to 1000 W output power range, while the isolated current-fed buck converter output results are in the 800 to 1800 W output range. The selections are made to coincide with the conventional operating ranges of the two converters. The load regulations results with Si diodes are shown in figure 4.4.

Figure 4.4 Load regulation results with Si diodes



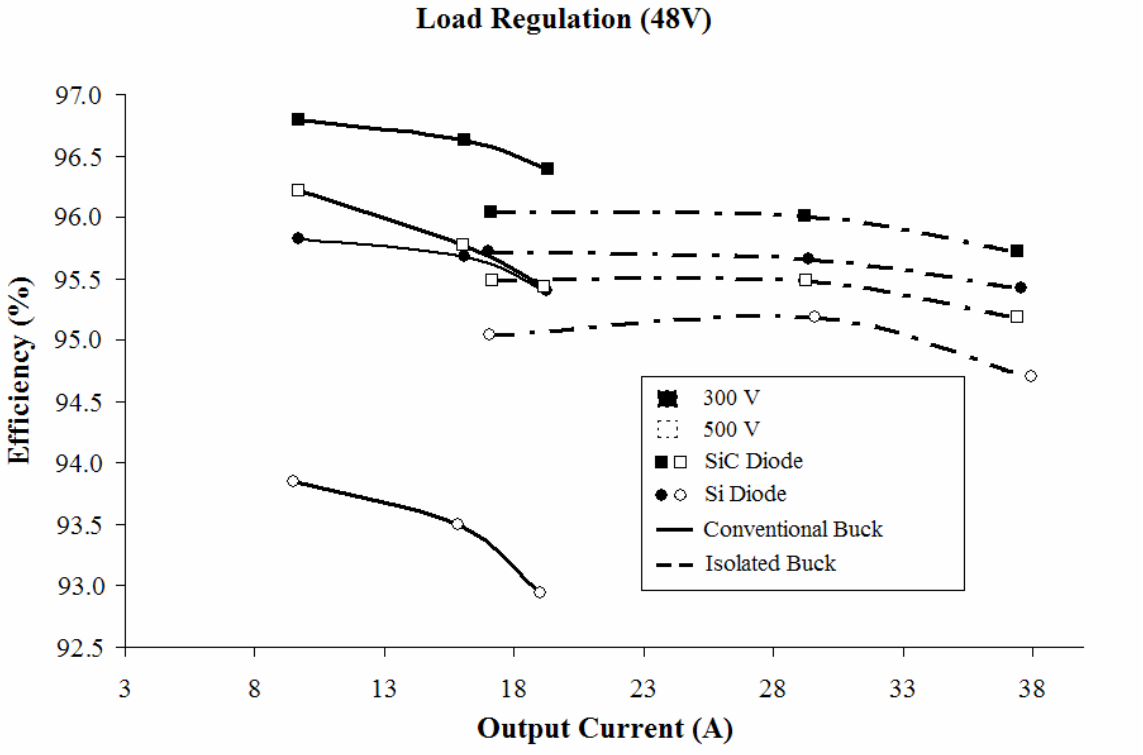
The isolated current-fed buck has a flatter load regulation and is less susceptible to input voltage variations. For output current levels above 17 A, at 300V, the conventional buck converter losses the efficiency crown. The load regulation results with SiC diodes are shown below in figure 4.5.

Figure 4.5 Load regulation results with SiC diodes



The conventional buck converter is the most efficient option, at all voltages, below the 20 A output current level; however, the efficiency begins to drop significantly at this point. In fact, the isolated current-fed buck converter provides the best efficiency for output current levels above 23 A. Figures 4.4 and 4.5 are combined to comparatively present the Si and SiC diode load regulation results and are provided in figure 4.6.

Figure 4.6 Load regulation results of all converter variations



The above figure 4.6 illustrates the benefits of the SiC diode compared to the Si diode in both converters. The efficiency of both converters is improved to the point where comparable performance is attained with SiC diodes at 500 V as with Si diodes at 300 V. The average efficiency of the four variants is presented in table 4.1.

Table 4.1 Average efficiency of the four converter variants

	Isolated Buck (SiC Diode)	**Isolated Buck (Si Diode)**	**Conventional Buck (SiC Diode)**	**Conventional Buck (Si Diode)**
Average Efficiency	95.66%	95.29%	96.02%	94.54%

The average efficiency is calculated using the six efficiency points per converter from figure 4.6.

4.3 Cost Analysis

This section presents the component cost analysis of the four converter variants analyzed in the previous sections. It is assumed that the component costs are major and that the manufacturing costs are similar for all four variants. The cost analysis is broken up into two sections: total cost and cost per output watt.

4.3.1 Total cost

The component costs are presented below with the names correspondent to those in figures 2.1 and 3.1. The quotes are gathered from Digikey and internal Xantrex database. The magnetic components include the cost of manufacturing.

Table 4.2 Component costs

Component type	Component	Part name	Cost per part (# parts)
MOSFET	Q	SPW47N60C3	9.71 (100)
MOSFET	A/B/C/D	IXFK140N30P	10.74 (50)
SiC Diode	D1	SDT12S60	9.14 (1000)
Si Diode	D1	APT30DQ100B	2.42 (1000)
Schottky Diode	D2/D2	STPS80170C	2.13 (1000)

Component type	Component	Part name	Cost per part (# parts)
Inductor 506µH	L	4 x 77439A7	16.84
Inductor 803µH	L	5 x 77439A7	18.90
Transformer	Xfrm	2 x 0R48020EC	19.86
Si Diode	Snubber D1/D2/D3/D4	RHRG3060	1.32555 (1000)

The data from table 4.2 in conjunction with the prototype specifications are used to construct the total cost table 4.3.

Table 4.3 Total cost of converter variants

Component	Isolated (SiC)	Isolated (Si)	Conventional (SiC)	Conventional (Si)
Q	29.14	29.14	29.14	29.14
L	18.90	18.90	16.84	16.84
D1	27.43	7.25	27.43	7.25
D2/D3	4.26	4.26	0	0
A/B/C/D	42.97	42.97	0	0
Transformer	19.86	19.86	0	0
Snubber D1/D2/D3/D4	5.30	5.30	0	0
Total cost	147.86	127.68	73.41	53.23

The above table illustrates the total cost dynamics of the four converter variants; however, it does not take into account the efficiency and power output potential of the converters. The next subsection analyses the cost per output watt.

4.3.2 Cost per output watt

A useful metric is the cost per output watt and is presented in Table 4.4 for the average power and maximum power. Equation 4.1 describes the relationship is presented below.

$$\frac{\$}{W} = \frac{\sum \$}{P_{in}\eta} \tag{4.1}$$

The equation simply states that the cost per output watt is the total cost of the converter divided by the output power. The efficiency is the average value of the 300V and 500V efficiencies.

Table 4.4 Cost per output watt

Power Level	Isolated (SiC)	Isolated (Si)	Conventional (SiC)	Conventional (Si)
800W Input Power	19.30 c	16.87 c	9.56 c	6.91 c
Average Input Power	11.89 c	10.31 c	10.92 c	7.89 c
Maximum Input Power	8.61 c	7.46 c	8.27 c	6.11 c

The average input power for the conventional buck converter is 700W and for the isolated current-fed buck converter is 1300W. The maximum input power for the

conventional buck converter is 925W and for the isolated current-fed buck converter is 1800W.

5 DISCUSSION AND CONCLUSION

The theoretical and experimental results are discussed in this section in line with the thesis objectives described in the introduction. The analysis is broken up into four parts: SiC diode benefits, converter suitability discussion, conclusions, and further research.

5.1 SiC Diode Benefits

The benefits of the SiC diode compared to the ultrafast Si diode in high voltage applications are quantitatively significant in both converters analyzed. Theoretically this was predicted by the identical equation 2.19 and 3.19 which are reproduced below for convenience as equation 5.1.

$$P_{rr} = \frac{V_g I_L t_{rr} + V_g Q_{rr}}{T_S} \tag{5.1}$$

The reverse-recovery process forces the current and voltage to be at their maximum across the transistors during the reverse-recovery time. This is troublesome due to the fact that the voltage is independent of the input and output powers and leads to high reverse-recovery losses at all output power levels as was predicted in the theoretical analysis and shown in the experimental results. On the other hand, the current is dependant on the input and output powers and is thus less detrimental to the performance.

Experimentally this is presented in figure 4.6 where the difference between the SiC diode and Si diode converter variants is similar at all output power levels but not input voltages. In addition, the reverse-recovery losses are greater in the conventional buck converter compared to the isolated current-fed buck converter due to the higher inductor current.

Quantitatively the efficiency benefits of the SiC diode in both the conventional and isolated current-fed buck converter are outlined in table 5.1.

Table 5.1 SiC diode efficiency benefits

Conditions (P_{out}, V_g)	**Isolated current-fed buck**	**Conventional buck**
500W, 300V	N/A	0.96%
500W, 500V	N/A	2.37%
800W, 300V	0.32%	0.94%
800W, 500V	0.45%	2.27%
1400W, 300V	0.35%	N/A
1400W, 500V	0.31%	N/A
1800W, 300V	0.30%	N/A
1800W, 500V	0.48%	N/A

The isolated current-fed buck converter result for the 1400W output power 500V input voltage is erroneous; however, the quantitative benefits are clear and in line with the expectations. The SiC diode is beneficial efficiency wise for high voltage applications irregardless of the power level; however, it is more suited for use in the conventional buck converter. It is important to note that the improvements in efficiency reduces the strain on the cooling solution and are one additional benefit.

5.2 Converter suitability discussion

This section outlines a guide to the appropriate converter and diode component selection for high input voltage and high voltage conversion ratio applications based on the results from the previous chapter. The guide makes suggestions based on the efficiency, cost, output power and galvanic isolation.

For applications with output power requirements below 1000W the conventional buck converter is the topology to choose if galvanic isolation is not required. When efficiency is the primary concern the SiC diode provides the best average efficiency as is shown in Table 4.1 at 96.02%, 1.48% greater than the Si diode performance. The Si diode provides the cheapest combination option at 7.89 cents per watt, 3.03 cents or 27.7% lower than the SiC diode combination. In the case where galvanic isolation is required the price per watt doubles and the efficiency falls to the 95.7% level when a SiC diode is used and 95.4% level when Si diode is used.

For applications with output power requirements above 1000W the isolated current-fed buck converter is the topology of choice irregardless of the galvanic isolation requirement. The SiC diode still provides the best performance; however, on average the performance advantage is only 0.35% compared to the Si diode. The price premium of the SiC diode is 1.58 cents per watt or 15.3% compared to the Si diode which has 10.31 cents per watt average price index.

It is important to note that the price of the four converter variants can be reduced with intelligent component selection. In the case of the conventional buck converter a transistor with a lower on-resistance can be selected due to the low conduction loss as is shown by figure 2.8. In addition, in the case of the isolated current-fed buck converter the full-bridge and input transistors with lower on-resistances can be selected to drastically reduce the price at the cost of degradation in performance as can be seen in figure 3.7.

5.3 Conclusions

The SiC diode is the ideal performance diode choice in high input voltage and high voltage conversion ratio applications irregardless of the topological choice. The performance benefits are greater in the conventional buck converter compared to the isolated current-fed buck converter as was predicted by the theoretical analysis and shown by the experimental results. In fact, the performance benefits are significant enough to promote the conventional buck converter to the most efficient choice for output power levels near and below 1000W.

The novelty of the SiC manufacturing process brings with it a price premium that will decrease over time as the process is refined and supply increases; however, even at the current 2008 prices the 15.3% isolated current-fed buck converter and 38.4% conventional buck converter SiC diode price premium may be acceptable considering the improved performance and reduced cooling requirements.

5.4 Further research

The converter prototypes were designed using state-of-the art active components with price premiums. Further research could examine the drawbacks between performance and cost with respect to the component selection. The theoretical analysis and experimental results from this thesis provide ample background information to intelligently experiment with appropriate components and extract performance and cost drawbacks and benefits. In addition, further research on system integration, temperature dependence on efficiency and converter reliability would provide useful engineering data.

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