MODELLING AND APPLICATIONS OF MOS VARACTORS FOR HIGH-SPEED CMOS CLOCK AND DATA RECOVERY

by

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Abstract

The high-speed clock and data recovery (CDR) circuit is a key building block of modern communication systems with applications spanning a wide range from wireline long-haul networks to chip-to-chip and backplane communications. In this dissertation, our focus is on the modelling, design and analysis of devices and circuits used in this versatile system in CMOS technology. Of these blocks, we have identified the voltage-controlled oscillator (VCO) as an important circuit that contributes to the total noise performance of the CDR. Among different solutions known for this circuit, LC-VCO is acknowledged to have the best phase noise performance, due to the filtering characteristic of the LC tank circuit. We provide details on modelling and characterization of a special type of varactor, the accumulation-mode MOS varactor, used in the tank circuit as a tuning component of these types of VCOs.

We propose a new sub-circuit model for this type of varactor, which can be easily migrated to other technologies as long as an accurate model exists for MOS transistors. The model is suitable whenever the numerical models have convergence problems and/or are not defined for the specific designs (e.g., minimum length structures). The model is verified directly using measurement in a standard CMOS 0.13μm process, and indirectly by comparing the tuning curves of an LC-VCO designed in CMOS 0.13μm and 0.18μm processes. Using a varactor, a circuit technique is proposed for designing a narrowband tuneable clock buffer, which can be used in a variety of applications including the CDR system. The buffer automatically adjusts its driving bandwidth to that of the VCO, using the same control voltage that controls the frequency of the VCO. In addition, a detailed analysis of the impact of large output signals on the tuning characteristics of the LC-VCO is performed. It is shown that the oscillation frequency of the VCO deviates from that of an LC tank.

Table of Contents

Abstract ..... **ii**

Table of Contents ..... **iii**

List of Tables ..... **v**

List of Figures ..... **vi**

List of Abbreviations and Terms ..... **x**

Acknowledgements ..... **xii**

Chapter 1 Introduction **1**

1.1 Clock and Data Recovery Methods 3
1.2 Why CMOS? 5
1.3 Contributions 7
1.3.1 A New Varactor Model 8
1.3.2 High-speed Tuneable Driver/Buffer 8
1.3.3 Effect of Large Signals in LC-VCO Tuning Characteristics 8
1.4 Organization of Thesis 9

Chapter 2 Background and Comparison of VCOs and Phase Detectors **10**

2.1 VCO Phase Noise and its Impact on System Operation 11
2.1.1 Comparison of Popular VCO Architectures 15
2.1.2 LC-Based VCOs 18
2.2 CDR Phase Detectors 21
2.3 Linear and Bang-Bang CDR Models 27
2.3.1 Linear CDR Model 28
2.3.2 Bang-Bang PD Model 33
2.4 Time-Domain Comparison of the Two PDs 36
2.4.1 Time-Domain Simulations of Bang-Bang and Linear CDRs with Noise Considerations 37
2.5 Summary and Conclusion 39

Chapter 3 Modelling and Characterization of MOS Varactors **41**

3.1 Varactors 42
3.2 VCO Tuning Characteristics 45
3.3 Characterization of AMOS Varactors 49
3.3.1 De-embedding Technique 50
3.3.2 Parameter Extraction Procedure 53
3.4 Varactor Modelling 55

3.5 Experimental and Simulation Results 58
3.5.1 Experimental Results in a Standard 0.13μm CMOS Process 58
3.5.2 Simulation Results in a Standard 0.18μm CMOS Process 62
3.6 Conclusion 64

Chapter 4 High-Speed Tuneable Narrowband CMOS Driver 67
4.1 Background 69
4.2 Proposed Solution 73
4.2.1 Design Example 75
4.3 Simulation Results 77
4.4 Conclusion 81

Chapter 5 Impact of Large Signals on LC-VCO with Accumulation MOS Varactors 83
5.1 MOS Varactors 85
5.2 MOS Varactors in LC-VCOs 87
5.2.1 Small-signal Analysis 89
5.2.2 Large-signal Analysis 90
5.3 Simulation Results 94
5.4 Conclusion 100

Chapter 6 Conclusions 102
6.1 Accomplishments 103

References 107

Appendices 116
Appendix A – Jitter Terminology 116
Appendix B – Flicker Noise Generation and Modelling for CDR Applications 118
Appendix C – The *Analog Verilog* Code for the AMOS Varactor 123

List of Tables

Table 2-1. Comparison between phase noises of different wireless standards 13

Table 2-2. Comparison of existing popular oscillator architectures 18

Table 4-1. Summary of bandwidth extension using the series-peaking technique 72

Table 4-2. Resonance frequency and gain at five voltages on the control line for typical and two extreme corners 80

List of Figures

Figure 1-1. CDR is used whenever the data is sent serially without the timing information. (a) Original serialized data at the transmitter, (b) same data but distorted and mixed with noise at the receiver. 2
Figure 1-2. Filter-based clock and data recovery 3
Figure 1-3. Generic closed-loop solution for clock and data recovery 4
Figure 2-1. GSM channel around 1.8 GHz 12
Figure 2-2. Channel interference in the case of larger-than-expected phase noise 12
Figure 2-3. A block diagram of a frequency synthesizer 14
Figure 2-4. A gain stage with a positive feedback loop 15
Figure 2-5. Relaxation oscillator 16
Figure 2-6. Ring oscillator 17
Figure 2-7. A simple LC-VCO 18
Figure 2-8. Different versions of LC-based oscillator 20
Figure 2-9. Block diagram of a generic clock and data recovery system. 21
Figure 2-10. Hogge (linear) phase detector [48]. 23
Figure 2-11. Alexander (bang-bang) phase detector [49]. 24
Figure 2-12. Phase detectors usage per technology process reported in ISSCC (2001-2007) 24
Figure 2-13. Bang-bang vs. linear phase detector used in recent ISSCC works from 2001-2007, sorted based on the ratio of link speed to transition frequency. 25
Figure 2-14. Simulated characteristic of the linear phase detector shown in Figure 2-10. PD out is the average of the *error* signal over one clock period, or 2π. 28
Figure 2-15. System-level model of a linear CDR. 29
Figure 2-16. A second-order filter commonly used in PLL-based systems 29
Figure 2-17. Jitter transfer characteristics of a typical linear CDR. 31
Figure 2-18. Jitter tolerance of a typical linear CDR. 33

Figure 2-19. Simulated characteristic of the bang-bang phase detector shown in Figure 2-11. 34
Figure 2-20. System-level model of the bang-bang CDR. 35
Figure 2-21. Operation of the linear CDR in the time domain. Left-hand side is the control voltage of the VCO when the low-frequency jitter source has large amplitude. Right-hand side is the control voltage when the high-frequency jitter source has large amplitude. 37
Figure 2-22. Operation of the bang-bang CDR in the time domain. Left-hand side is the control voltage of the VCO when the low-frequency jitter source has larger amplitude. Right-hand side, is the control voltage when the high-frequency jitter source has larger amplitude. 38
Figure 2-23. BB CDR response to zero input jitter source. 39
Figure 3-1. An nMOS transistor configured as a varactor 42
Figure 3-2. C-V characteristics of an nMOS transistor (Figure 3-1) 43
Figure 3-3. Cross-section of an accumulation-mode MOS varactor (AMOS) 44
Figure 3-4. An LC-VCO with an nMOS current source 45
Figure 3-5. Measured vs. modeled VCO tuning characteristics (extracted piece-wise linear model) 47
Figure 3-6. C-V characteristics for three different values of the oscillator voltage swing (Vpeak) 48
Figure 3-7. Top-view of the test structures: (a) short, (b) open, and (c) DUT (varactor array) 50
Figure 3-8. Micrograph of the test structures in 0.13μm CMOS, from left to right: short, open, and the varactor array (DUT) 50
Figure 3-9. Equivalent lumped model of the varactor (DUT) with associated parasitics (open/short de-embedding) 51
Figure 3-10. Alternative lumped model for open/short de-embedding (OSD) 52
Figure 3-11. Equivalent lumped model of the integrated varactor 53
Figure 3-12. Simplified circuit of the two-port varactor in Figure 3-11 54
Figure 3-13. SPICE model developed for the varactor 57
Figure 3-14. Micrograph of a VCO test structure in 0.13μm CMOS 59
Figure 3-15. Measured phase noise of the VCO with pMOS tail current (Figure 2-8b) at three different supply voltages (1.2V, and 1.2V ± 5%) 60

Figure 3-16. Measured vs. modeled tuning characteristics (new sub-circuit model) 61
Figure 3-17. Comparison between the model and measured results for a varactor (m=60, width=7.9μm, and length=0.13μm) in a 0.13μm CMOS process 61
Figure 3-18. Comparison between the foundry varactor model and our model in a standard 0.18μm CMOS process. 63
Figure 3-19. Comparison of the tuning curves for the two LC-VCO designed in a standard 0.18μm CMOS process using the foundry varactor model and our sub-circuit model. 64
Figure 4-1. Two cascaded high-speed circuits with total node capacitance C_L in between. 67
Figure 4-2. (a) A common-source amplifier with a capacitive load, (b) Same amplifier with shunt peaking 70
Figure 4-3. Bandwidth extension using shunt peaking technique: depending on the ratio of zero to the pole of the original first order system (m), there could be different frequency responses 71
Figure 4-4. (a) A common-source amplifier with split drain parasitic and load capacitance, (b) Same amplifier with series-peaking inductance between the two capacitors. 71
Figure 4-5. Bandwidth extension using series peaking technique 72
Figure 4-6. Using a tuned load, amplification occurs at the desired frequency but it is limited to that frequency only. 73
Figure 4-7. Two cascaded high-speed circuits with the proposed resonator stage in between. 75
Figure 4-8. Voltage controlled oscillator (left) followed by the tuneable inductive driver stage (dashed box). There is also one-stage resistive buffer block between VCO and inductive driver to create isolation (not shown here) 76
Figure 4-9. VCO operating frequency vs. control voltage simulated for extreme process corners, temperature and supply values (PVT). 78
Figure 4-10. 3D illustration of buffer gain vs. control voltage. The VCO tuning curve has been illustrated for the typical process. The peaks of buffer gain closely track the changes in VCO frequency. 79
Figure 4-11. Layout of the tuneable amplifier in a standard 0.18μm CMOS process with a differential Inductor (N=3, width=15μm and inner diameter =80μm). 80
Figure 5-1. CMOS LC-tank VCO 84
Figure 5-2. C-V characteristic of an accumulation-mode nMOS varactor 87

Figure 5-3. LC-tank circuit 88

Figure 5-4. Circuit schematic of an LC-VCO designed in a standard CMOS 0.18µm technology for 4 GHz to 6 GHz operation range. 94

Figure 5-5. Tuning curves of four VCOs, all with the same architecture as shown in Figure 5-4 but with different *m* factors for transistor M_3. 96

Figure 5-6. Oscillation frequency of the LC-VCO of Figure 5-4 for different *m* factors (*m*=*3*..30), when $V_{Control}$=*1.8V.* 97

Figure 5-7. Oscillation frequency of an LC oscillator shown in Figure 5-4 with fixed tank capacitors of 1.1pF for different *m* factors (*m*=*3*..30). 99

Figure 5-8. Output waveform for two different *m* values at $V_{Control}$ = 1.8V. The solid line shows the output for *m*=8 while dashed line shows the VCO output for *m*=20..... 100

List of Abbreviations and Terms

AMOS	Accumulation-mode MOS varactor
AR	Auto Regression
BBPD	Bang-Bang Phase Detector
BER	Bit Error Rate
BPF	Band-Pass Filter
BSIM	BSIM is a physical MOSFET model with extensive built-in dependencies of important dimensional and processing parameters such as channel length, width, gate oxide thickness, junction depth, substrate doping concentration, etc.
CDMA	Code-Division Multiple Access
CDR	Clock and Data Recovery
CMC	Canadian Microelectronic Corporation
CML	Current-Mode Logic
CMOS	Complementary Metal-Oxide Semiconductor
CP	Charge Pump
DCD	Duty-Cycle Distortion
DEMUX	De-Multiplexer
DETFF	Double-Edge-Triggered flip-flop
DFF	D-Flip-flop
DUT	Design/Device Under Test
FD	Frequency Detector
FET	Field Effect Transistor
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
ISI	Inter-Symbol Interference
ISS	impedance-standard-substrate
ISSCC	International Solid-State Circuit Conference
ITRS	International Technology Roadmap for Semiconductors
GSG probe	Ground-Signal-Ground Probe
GSM	Global System for Mobile Communications
LDD	Lightly Doped Drain/Source
LO	Local Oscillator
LTI	Linear Time Invariant
LVDS	Low Voltage Differential Signaling
MOSFET	Metal-Oxide Semiconductor FET
MUX	Multiplexer
NSERC	Natural Sciences and Engineering Research Council of Canada
OSD	Open-Short De-embedding

PCB	Printed-Circuit Board
PD	Phase Detector
PFD	Phase/Frequency Detector
PLL	Phase-Locked Loop
PMDC	Polarization mode dispersion compensator
PSRR	Power supply rejection ratio
PVT	Process, supply voltage and temperature variations
RAM	Random Access Memory
RMS	Root-Mean-Squared
RX	Receiver
SATA	Serial Advanced Technology Attachment
SAW	surface acoustic wave
SDH	Synchronous Digital Hierarchy
SERDES	Serializer / Deserializer
SETFF	Single-Edge-Triggered flip-flop
SiP	System-in-a-Package
SNR	Signal to noise ratio
SoC	System-on-a-chip
SONET	Internet Synchronous Optical Networks
SRAM	Static RAM
TX	Transceiver
TF	Transfer Function
UI	Unit Interval
VCO	Voltage-Controlled Oscillator
VNA	Vector Network Analyzer
WLAN	Wireless Local Area Network
WMAN	Wireless Metropolitan Area Network
WPAN	Wireless Personal Area Network
XOR	Exclusive-OR

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Chapter 1

Introduction

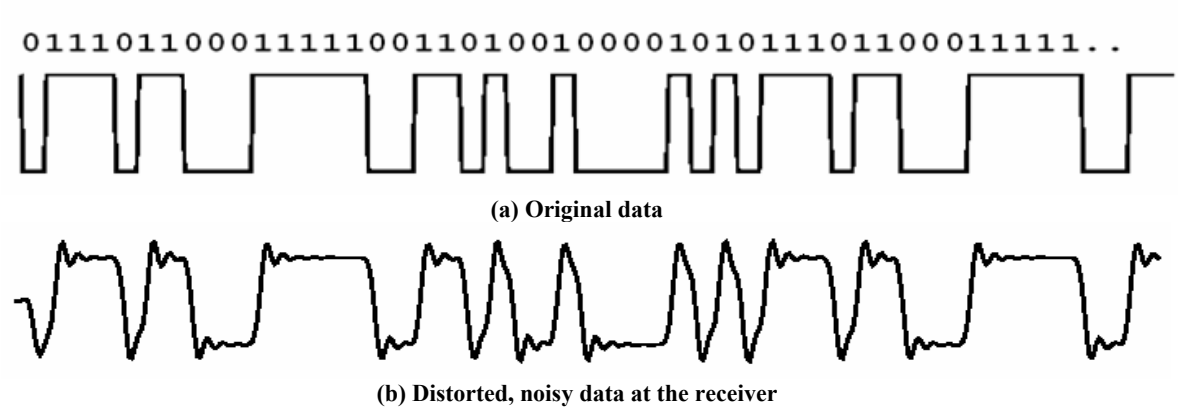
The rapid growth of telecommunication networks, along with the advent of new Internet and multimedia applications is continuously increasing the demand for higher speed data communication and driving the industry for more innovation in this area. Data transmission can be performed through different media, such as air (i.e., wireless transmission), coaxial cables, twisted copper wires and optical fibre. Optical fibre is the most promising medium for high-speed and/or long-distance data transmission, mainly due to its higher bandwidth and lower loss. A typical optical fibre has loss of around 0.24 dB/km [1], which is much lower than that of other transmission media. This unique low-loss characteristic of optical fibre makes it an excellent solution for long-distance data transmission, and even at very high frequencies where aluminium/copper traces fail, it is used for backplane interconnects. Although high-frequency optical signals benefit from their low-loss characteristic compared with lossy electrical signals, they require amplification and regeneration due to degradation mechanisms to which they are subjected, such as optical pulse dispersion and attenuation.

There has been some work on optical-domain amplification and signal regeneration, however, the problem has not been solved completely. For example, there has been some interesting work on developing a polarization-mode dispersion compensator (PMDC) in the optical domain, which eliminates distortion of optical signals over fibre optic networks caused by asymmetries in fibre. However, the existing solutions are costly and/or bulky. Another

fundamental issue in the optical domain is the lack of storage elements (i.e., optical memory cells). Due to these reasons, the signal has to be converted from optical to electrical for amplification, regeneration and data processing. The speed performance of these electronic interfaces is the main bottleneck preventing effective utilization of fibre-based systems.

Clock and data recovery (CDR) systems are key blocks inside these interface units [2]. They improve the signal-to-noise ratio (SNR) by regenerating clean data from the noisy, distorted received signal.

Besides their applications in high-speed optical communication networks such as Internet Synchronous Optical Networks (SONET) and Synchronous Digital Hierarchy (SDH), CDRs are used in other systems for applications such as serial advanced technology attachment (SATA, which is a replacement for parallel ATA), chip-to-chip communications and backplane interconnects. They are embedded in transceivers for serializing and de-serializing data inside serializer/deserializer (SERDES) blocks.



(a) Original data

(b) Distorted, noisy data at the receiver

Figure 1-1. CDR is used whenever the data is sent serially without the timing information. (a) Original serialized data at the transmitter, (b) same data but distorted and mixed with noise at the receiver.

In general, whenever the data is sent serially without the timing information[1] (Figure 1-1a), at the receiver, it is distorted and mixed up with noise

[1] Sometimes clock signal is also sent with the data but CDR is still required for data regeneration [3].

due to various degradation mechanisms such as inter-symbol interference (ISI), attenuation, random noise, and crosstalk (Figure 1-1b). The use of CDR is then required in order to extract the timing information from the data and reconstruct the original data.

1.1 Clock and Data Recovery Methods

Clock and data recovery has traditionally been performed using open-loop systems such as the one shown in Figure 1-2. In such systems, the fundamental harmonic of the clock signal is typically extracted from the data by means of differentiation, rectification and band-pass filtering of the data stream. A differentiator can be a simple edge detector such as an XOR block that compares the data and its delayed version. This generates tiny pulses at transition points (i.e., rising and falling edges). The extracted clock is then used to re-time the data using a D-flip-flop (DFF).

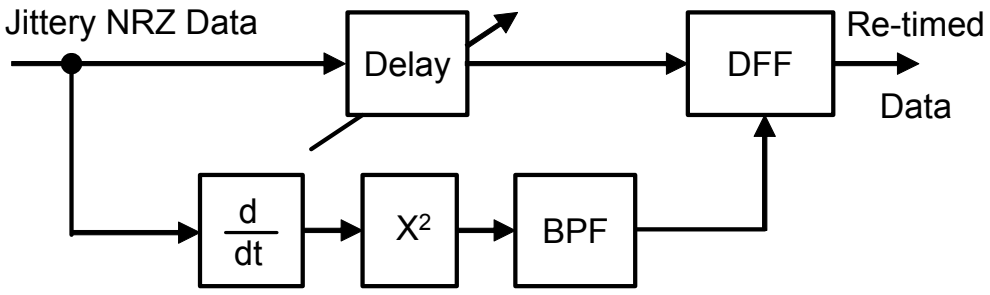


Figure 1-2. Filter-based clock and data recovery

Filter methods, such as the one discussed here, are very difficult for on-chip integration, since the band-pass filters (BPFs) need to be very selective (i.e., with high quality factors). However, on-chip passive filters suffer from low quality factors, which makes the method impractical using available fabrication processes [4]. As a substitute, band-pass filtering could be provided externally by a surface acoustic wave (SAW) filter; however, these filters suffer from high loss and relatively low speed of operation, which limits their applicability for high-speed systems [5]. Moreover, process, temperature and supply variations (PVT) change the frequency of the filter as well as the delay of the *delay block* (Figure

1-2), making the control of sampling time very difficult. In general, systems utilizing SAW resonator filtering require matching of SAW and circuit temperature coefficients, along with custom delay lines for setting the timing of the recovered sampling clock with respect to the data eye [6].

The above-mentioned limitations suggest using feedback-based methods, especially now that fully monolithic designs are feasible at high-frequencies using state-of-the-art fabrication process. Figure 1-3 illustrates the generic closed-loop system for clock and data recovery. This system is very similar to a phase-locked loop (PLL) system, which is used for clock alignment. The main difference lies in the random nature of the input signal (data instead of the periodic signal). The random data patterns require special types of phase/frequency detection, which are different than those used in a normal PLL. Chapter 2 describes two CDR systems with different types of phase/frequency detectors (PFD) and provides a detailed comparison of the previous work. Aside from the PFD, the rest of the system is similar to a PLL. It includes an amplifier or a charge pump (CP) for converting and amplifying the output voltage of the PFD to current, a low-pass filter for filtering the control voltage of the voltage-controlled oscillator (VCO) and finally a decision circuit, which is usually a DFF.

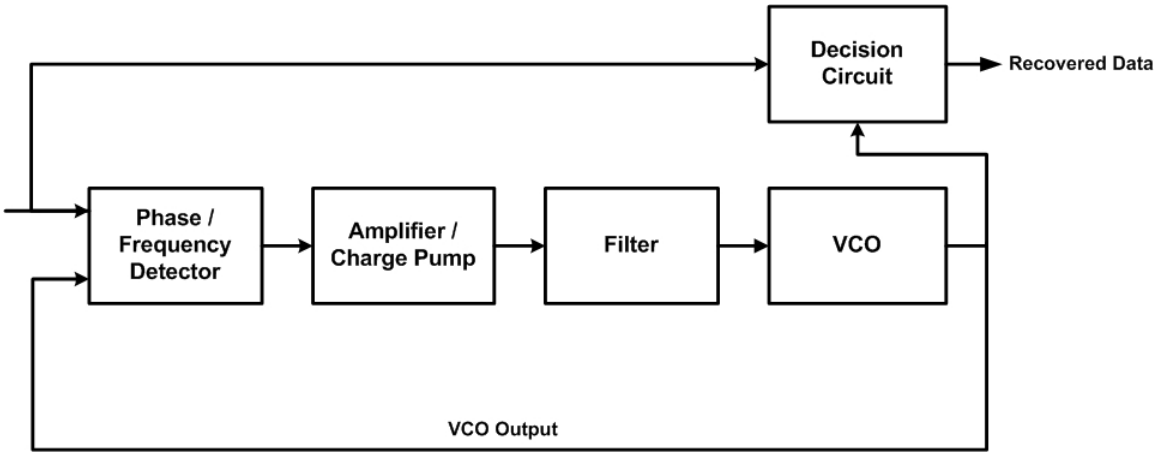


Figure 1-3. Generic closed-loop solution for clock and data recovery

The CDR system has been extensively implemented in various technologies. However, the next sections provide an overview of CDRs and

explain why we are interested in complementary metal oxide semiconductor (CMOS) implementation.

1.2 Why CMOS?

CDR circuits have been predominantly implemented in technologies such as III-V, Silicon bipolar, and SiGe BiCMOS due to their high-speed and low-noise characteristics [7, 8]. However, circuits implemented in these technologies suffer from a number of drawbacks. First, they are still expensive relative to CMOS, which is the mainstream IC technology for digital designs. Second, circuits designed in these technologies generally dissipate more power compared to the same circuits designed in CMOS. Besides, by using CMOS, one could implement the analog and mixed-signal blocks (e.g., CDR) on the same chip with digital blocks (i.e., system-on-a-chip or SoC). This eliminates the need for power-hungry output stages, which typically drive low-input-resistance (e.g., 50Ω loads). SoC implementation also reduces the number of costly packages, off-chip components, and the area of printed-circuit boards (PCB). Another possible technology could be BiCMOS; however, BiCMOS technology is not suitable for leading-edge SoC designs, as the scaling in BiCMOS is not done as aggressively as for CMOS.

Recent advances in CMOS technologies (e.g., aggressive scaling) have made it an attractive alternative for implementing high-speed systems. In addition, due to the current large number of CMOS foundries around the world, the time-to-market is usually shorter for designs implemented in CMOS [5]. CMOS foundries also provide higher manufacturing yield as compared with other foundries.

Despite these advantages, there are a few drawbacks to CMOS. Designing high-speed mixed-signal circuits (e.g., multi-gigahertz systems) in advanced CMOS technologies is very challenging. Issues such as speed, substrate noise coupling, and reduced voltage headroom pose many difficulties in the design of high-speed analog CMOS circuits [9]. Therefore, accurate device

models, novel circuit techniques and innovative system architectures must be devised to guarantee the reliability and performance of the system.

With aggressive technology scaling, one of the design dilemmas in recent years has been dealing with constantly varying device models, especially models for on-chip passive components that are provided by the foundries, and usually are not as accurate as one would desire (especially when the design kit is first released). Although these passive components may not seem as important for digital designs, they are an integral part of high-speed analog designs. For instance, a VCO, which is a key block of PLL, requires a tuning component. In the case of LC-tank VCOs, this is usually done using on-chip varactors. From the foundry standpoint, developing accurate models for varactors has lower priority than for MOSFET models, which are critical for digital IC design. The currently existing models are sometimes released in the second or later revisions of the design kits. These models are currently developed empirically by fitting a curve to the measurement results. They are based on mathematical curve fitting, which tends to get more complicated as technology advances. For instance, the current varactor models in a 90nm CMOS process is more complicated and has more parameters as compared to the hyperbolic tangent model used in a 0.18μm CMOS process. The associated increase in computational complexity results in longer simulation times, and in some cases creates convergence problems. In addition, these models are usually valid for a small number of test cases provided by foundries. The test cases are usually designed for use in general-purpose applications and do not include varactors with minimum gate lengths. This substantially limits the use of these models in aggressive analog and mixed-signal designs where minimum-size varactors are needed.

The shrinking voltage headroom dictated by the digital world adds to these difficulties. Therefore, it is the responsibility of the analog designer to come up with circuit techniques that accommodate the limitations of the technology. One of the design challenges at high frequencies is the design of the driver/buffer stage. These buffers are normally required to drive the capacitive load of the circuit. The load usually consists of MOSFET parasitic capacitances,

interconnect parasitics, and the input capacitance of the next stage. For example, in the case of CDR systems, the VCO has to drive a number of flip-flops in the phase-detector block, depending on the system architecture. However, the low transition frequency (unity current-gain frequency) of the technology is the limiting factor for building high-gain drivers. If a resistive driver with no bandwidth extension technique can operate at that frequency, several cascaded drivers are required in order to drive a large capacitive load, which increases the power consumption.

Another issue in systems using LC-VCOs with MOS varactors, which is usually neglected by designers, is the effect of large output swings of LC-VCOs on the VCO tuning characteristic. Use of varactors as a tuning component in LC-VCOs may have some implications in predicting the VCO tuning characteristics as the varactor C-V characteristic is voltage dependent. This issue may result in design iteration if the tuning range of the fabricated VCO falls outside the desired range.

1.3 Contributions

The goal of this dissertation is to present some solutions at the circuit and device modelling levels for the key building blocks of the CDR system. Since the generic closed-loop CDR architecture (Figure 1-3) is based on the PLL circuit, the solutions discussed here are either directly or indirectly applicable to other systems that incorporate PLL circuits (e.g., clock generators and frequency synthesizers). For instance, issues such as VCO phase noise are common between all these systems. In Chapter 2, we discuss and compare different VCOs in the context of frequency synthesizers. However, the same VCO can be used directly inside CDRs as well as other PLL-based systems. In the following sections, we explain the key contributions of this work.

1.3.1 A New Varactor Model

We have developed a model for a popular type of varactor, namely, an *accumulation nMOS* varactor. Unlike the current numerical models, this model is based on sub-circuits with MOS transistors and passive components. Therefore, as long as there is a valid model defined for MOS transistors, our varactor sub-circuit model could be constructed. The use of this model is not limited to a few examples or a particular length varactor. In addition, we have shown that the model has ease of migration to other technologies by verifying it in two different CMOS processes. Some of the recent issues in advanced CMOS processes (e.g., 90nm CMOS), such as gate leakage current, are also considered in the model (unlike the current foundry models), since the leakage current is modelled in the MOS transistors.

1.3.2 High-speed Tuneable Driver/Buffer

We have introduced a new circuit that uses an adjustable load to drive the clock signal generated by the VCO. The driver automatically tunes its centre frequency to that of the VCO oscillating frequency. Therefore, there is no need for a large-bandwidth driver, which amplifies the noise and other unwanted signals together with the clock signal. This circuit technique has become feasible by using varactors to control the resonance frequency of the driver stage. The circuit concept has been verified using simulation of a 5GHz LC-VCO and a driver designed in a standard CMOS 0.18μm technology.

1.3.3 Effect of Large Signals in LC-VCO Tuning Characteristics

We have studied the effect of large signals on the LC-VCOs mathematically by solving the differential equation of the tank circuit in both the small-signal and large-signal regimes. We have shown that in the large-signal regime, the oscillation frequency is not just a function of the tank inductance and capacitance whenever the capacitance is a function of the voltage. The study shows that the VCO frequency is also a function of the higher-order harmonics of the output voltage. The analytical results are verified using circuit-level

simulations of multiple 4GHz–6GHz LC-VCOs, designed in a standard CMOS 0.18μm technology with different output swings.

1.4 Organization of Thesis

In Chapter 2, we review and compare the performance of the two key blocks of PLL-based systems: VCOs, and phase detectors. We compare different VCO architectures and demonstrate the importance of the VCO phase noise by using some examples and studying this block in the context of frequency synthesizers. Then we turn our attention to the phase detector, which comes in different forms depending on the type of the PLL-based system. CDRs are mainly designed based on one of the two popular phase detector architectures: linear and bang-bang. We review a major body of recent work done over the past seven years, in particular, papers published in the IEEE International Solid-State Circuits Conference (ISSCC), to determine the trend in industry. We collect some of the reasons why designers prefer one architecture to another. We also compare the two architectures at the system-level and study their performance in the frequency domain as well as in the time domain.

Chapter 3 deals with the characterization and modelling of accumulation-mode MOS varactors. We will introduce a new circuit-based model for the accumulation MOS varactor. Chapter 4 explains the details of our proposed circuit technique for the VCO clock buffer design using AMOS varactors. Chapter 5 investigates the impact of the large signal outputs in LC-VCOs with the AMOS varactor as the tuning component. Concluding remarks are made in Chapter 6.

Chapter 2

Background and Comparison of VCOs and Phase Detectors

In this chapter, we review two key blocks used in PLL-based systems: VCOs and phase detectors. These blocks are important in determining the overall performance of the system. They affect the noise performance as well as the loop dynamics of the system. We will demonstrate the importance of the VCO phase noise by using some examples and studying this block in the context of frequency synthesizers. Frequency synthesizers are similar to the CDR systems aside from their different type of phase detectors and extra dividers. Following that, CDR phase detectors are reviewed. We study two of the most popular approaches to phase detection in CDRs: linear (a.k.a., Hogge) and binary (a.k.a., Alexander, bang-bang (BB) or early/late). In doing so, we

- review the most recent work in the area and study the rate of usage of the two popular PDs: bang-bang and linear, and identify the major reasons for selecting a particular PD for a design
- develop a system-level model for comparing bang-bang and linear PDs
- simulate and compare the two systems in the time-domain, considering jitter on the incoming data with two different frequencies and amplitudes, which results in different output jitter and transfer functions.

2.1 VCO Phase Noise and its Impact on System Operation

In recent years, the demand for wireless communications has increased considerably. Wireless communication systems encompass a wide variety of standards. Such systems include cellular phones (e.g., GSM, CDMA), wireless local area networks (WLAN), wireless personal area networks (WPAN), wireless metropolitan area networks (WMAN), etc. The adoption of any of these technologies depends on many variables, such as cost and market demand. Over time, the implementation cost of the technologies goes down, which further accelerates their adoption. A high-tech market research firm, In-Stat, forecasts that the worldwide wireless market will grow to more than 2.3 billion subscribers by 2009 [10].

Typical RF transceivers have a built-in frequency synthesizer, namely a local oscillator (LO), to generate a signal with the desired frequency used for up and downconversions. Wireless standards strictly specify the minimum level of the received signal, the maximum level of unwanted signal, the channel bandwidth and the spacing between two adjacent channels. Using these specifications and targeting the required signal-to-noise ratio (SNR) after downconversion, the maximum amount of acceptable phase noise on the LO can be calculated. This procedure is conceptually depicted in Figure 2-1 for the GSM-1800 standard. Using the information provided in the figure and knowing the desired SNR (e.g., 9 dB after downconversion), the maximum acceptable phase noise at 600 kHz offset from the carrier (which is at the centre of the adjacent channel) is calculated to be -121 dBc/Hz [11].

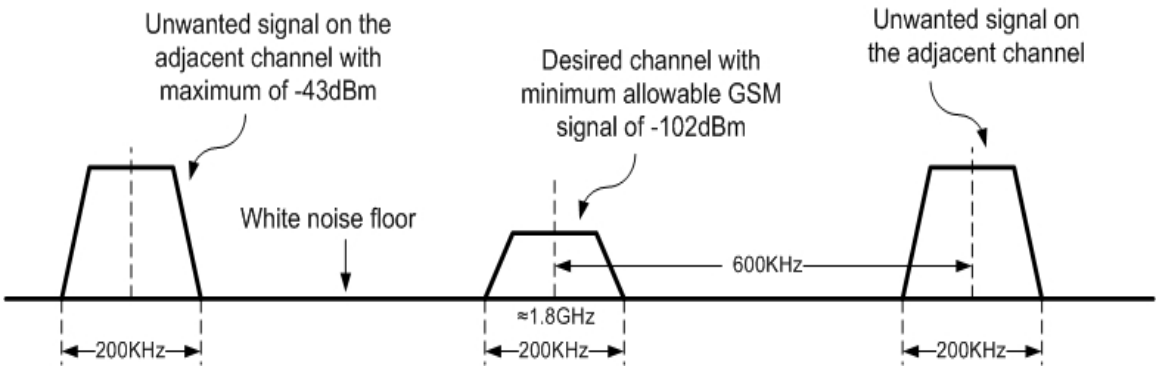


Figure 2-1. GSM channel around 1.8 GHz

Figure 2-2 illustrates the problems that may arise if the LO spectrum extends to the adjacent channel with relatively high power spectral density: after downconversion, there will be an overlap between the spectra of the desired signal and the unwanted adjacent channel, which makes the recovery of the data almost impossible.

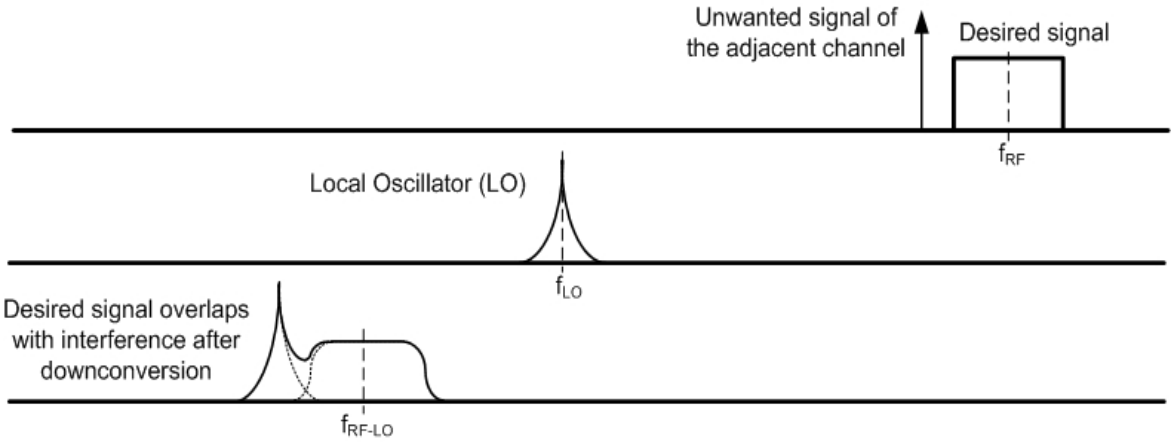


Figure 2-2. Channel interference in the case of larger-than-expected phase noise

LOs are usually in the form of VCOs. They are placed inside a feedback loop as part of a PLL system. As a result, they constantly align their zero-crossings with the reference clock. The amount of generated phase noise, within the bandwidth of the PLL, can be reduced by the loop characteristics. Table 2-1 compares the maximum allowable phase noise of some of the wireless standards at their nominal frequencies.

Figure 2-3 shows the block diagram of a PLL-based frequency synthesizer typically used in integrated wireless transceivers. This synthesizer comprises a phase (and usually frequency) detector (PD or PFD), a charge pump, a low-pass filter, a voltage-controlled oscillator (VCO), a reference and a feedback divider block (/M and /N). The output frequency of the block is N/M times the reference frequency. Therefore, by adjusting the N/M ratio, different multiples (integer or fractions) of the reference frequency can be generated.

Table 2-1. Comparison between phase noises of different wireless standards

Wireless Standard		Frequency	Phase Noise
GSM	850	850MHz	-121dBc/Hz at 600KHz
	900	900MHz	-121dBc/Hz at 600KHz
	1800	1800MHz	-121dBc/Hz at 600KHz [11]
	1900	1900MHz	-121dBc/Hz at 600KHz
WLAN	802.11a	5.0GHz	Many WLAN transceivers specify "integral" noise in degrees rms over a frequency range, e.g., integral of phase noise from 10K to 10M < 1.2º rms for the whole TX path, or 0.8º rms for the synthesizer. This may also be translated to an average phase noise spec, like P.N. < -90dBc/Hz at < 100KHz (in-band, or close-in)
	802.11b	2.4GHz	
	802.11g	2.4GHz	
WPAN	ZigBee (802.15.4)	900MHz 2.4GHz	-95dBc/Hz at 5MHz
	Bluetooth (802.15.1)	2.4GHz	-94dBc/Hz at 100KHz [12]

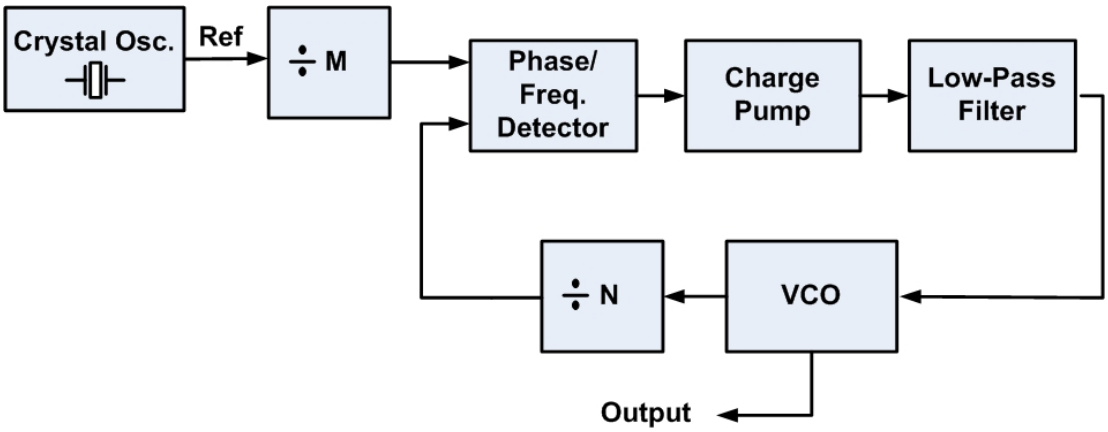


Figure 2-3. A block diagram of a frequency synthesizer

Later in this chapter, we will show that the jitter transfer function from the reference to the output of this system exhibits a low-pass characteristic. As a result, high-frequency phase noise[2] of the reference clock is attenuated by the loop, while its low-frequency (close-in) noise passes through the system to the output. On the other hand, the phase jitter of the VCO will see a high-pass function to the output. Meaning that only the low-frequency jitter of the VCO is suppressed within the bandwidth of the phase-locked system.

The total output phase noise is a function of the phase noise of each of the PLL blocks, the original input phase noise generated by the reference clock, noise on the supply/ground lines, and the noise-shaping characteristics of the loop. While there are different techniques for optimizing the performance of the synthesizers to reduce the total phase noise, the VCO plays a key role in the total phase noise of the system. This is because high-frequency perturbation on the VCO control line tends to appear at the output in the form of phase variations. In addition, any high frequency (a.k.a. out-of-band) phase noise generated by the VCO due to supply, substrate, or device noise cannot be suppressed by the loop and travels directly to the output.

In the following sections, various aspects of some of well-known VCO architectures, including their phase noise performance, are compared. The LC-

[2] The time-domain counterpart of phase noise is jitter, which is a more common term in wireline applications.

VCO is identified as having the best performance in terms of phase noise. In the next section, the building components of various LC-VCOs are studied, and their effects on overall phase noise are investigated. To facilitate this investigation, three forms of LC-VCOs are studied. These LC-VCOs are implemented in a standard 0.13μm CMOS process. We show that the tuning characteristic of LC-VCOs cannot be easily predicted using simple models in simulators. A more detailed analysis of the tuning characteristics of the LC-VCO is provided in Chapter 5.

2.1.1 Comparison of Popular VCO Architectures

VCOs are one of the key building blocks of RF transceivers, and affect the function, and jitter performance of the system. They are utilized inside PLL-based circuits (e.g., in frequency synthesizers as part of the LO) to generate a clean and low-jitter clock signal for the operation of other blocks of the frequency synthesizer or transceiver. Typical oscillator circuits require some form of positive feedback around a gain stage in order to sustain their oscillation. This concept is illustrated in Figure 2-4. The closed-loop system (oscillator) has to fulfil the following two *Barkhausen conditions* at all times for continuous oscillation:

$$\begin{cases} |H(j\omega)| \geq 1 \\ \angle H(j\omega) = 360^\circ \end{cases} \quad \text{(2-1)}$$

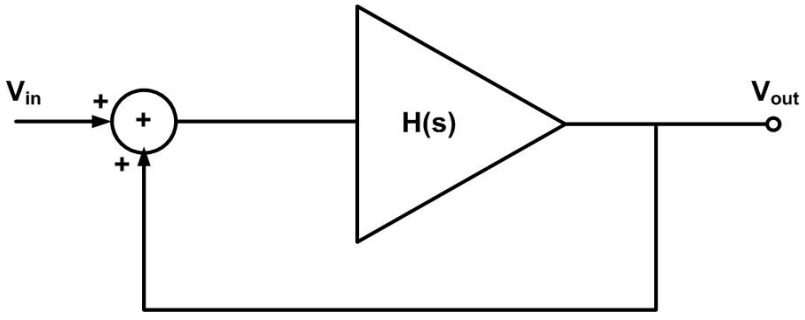


Figure 2-4. A gain stage with a positive feedback loop

Three common categories of oscillator circuits are relaxation (Figure 2-5), ring (Figure 2-6), and LC-based (Figure 2-7) oscillators. In a relaxation oscillator

(a.k.a., multi-vibrator), the oscillation relies on non-linear switching that charges and discharges a capacitor with a controllable time constant. The oscillation

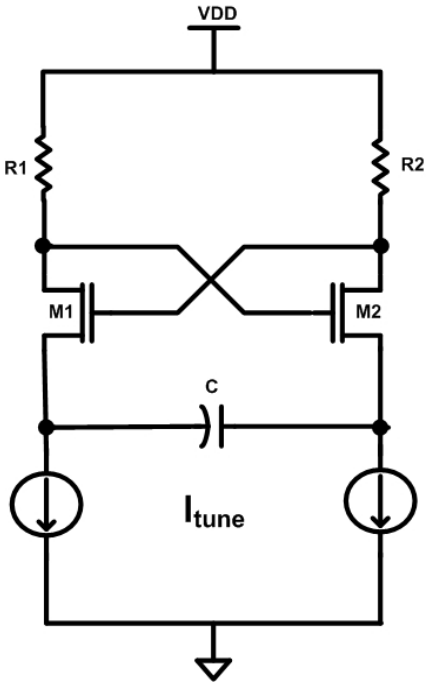


Figure 2-5. Relaxation oscillator

frequency can be tuned by adjusting the time constant to generate variable time constants, using, for example, a varactor or a controllable current source. Relaxation oscillators are usually limited to moderate frequencies.

Ring oscillators (Figure 2-6) are normally designed by cascading an odd number of inverters in a loop. Alternatively, an even number of differential delay cells can be used with an explicit polarity inversion in the feedback connection. A variable delay element (e.g., variable resistor or current source) is used for tuning. The frequency range can also be adjusted by digitally adding or removing inverters from the chain (coarse tuning). On the downside, both ring and relaxation oscillators suffer from poor frequency stability, which manifests itself as higher phase noise. As a result, sometimes a stability acquisition aid is required. This circuit could be designed again using a PLL, which is locked on a clean reference clock (e.g., crystal resonator).

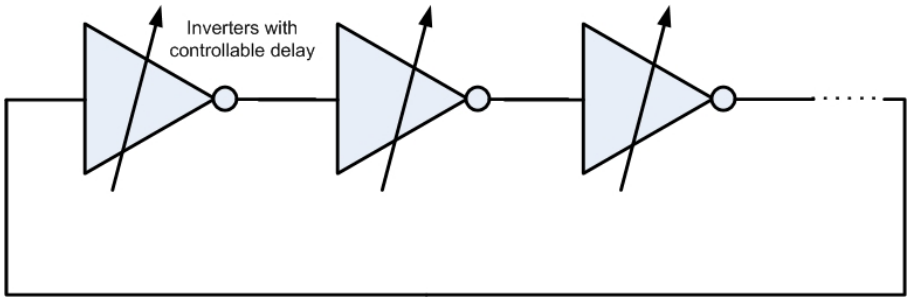


Figure 2-6. Ring oscillator

LC-based oscillators are usually made with a differential pair amplifier, using an LC tank as the load. By connecting the outputs to the inputs, the amplifier starts to amplify the inherent white noise at its inputs around the resonance frequency of the tank, provided that its open loop gain is greater than one (first of the two *Barkhausen conditions*). Noise at other frequencies is filtered out by the LC tank. This filtering characteristic of LC-based oscillators has made them the best in terms of phase-noise performance. Furthermore, compared to the other two oscillator architectures, LC oscillators typically operate more reliably at higher frequencies, provided an LC tank of moderate to high quality factor. However, LC-based oscillators suffer from their inherently narrower tuning range. Moreover, the integration of these oscillators is more costly due to the large space allocated to on-chip inductors. It should be noted that as technology advances, achieving higher frequencies becomes more feasible, which in turn requires smaller (less spacious) inductors. Table 2-2 summarizes the advantages and disadvantages of the three oscillator architectures [4].

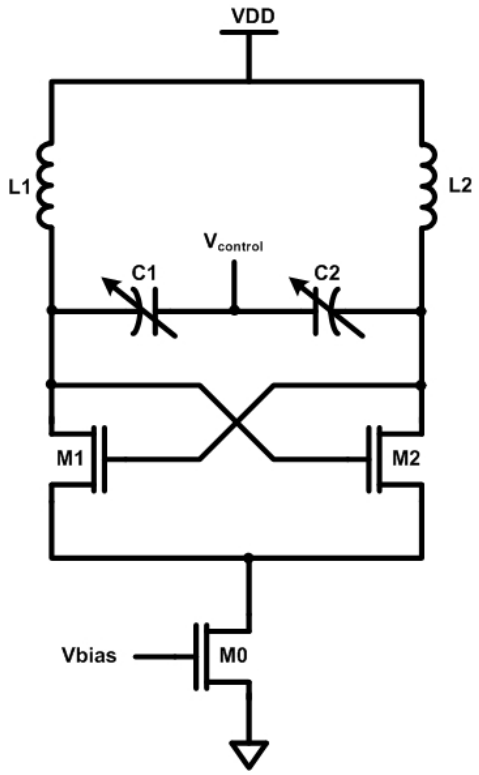


Figure 2-7. A simple LC-VCO

Table 2-2. Comparison of existing popular oscillator architectures

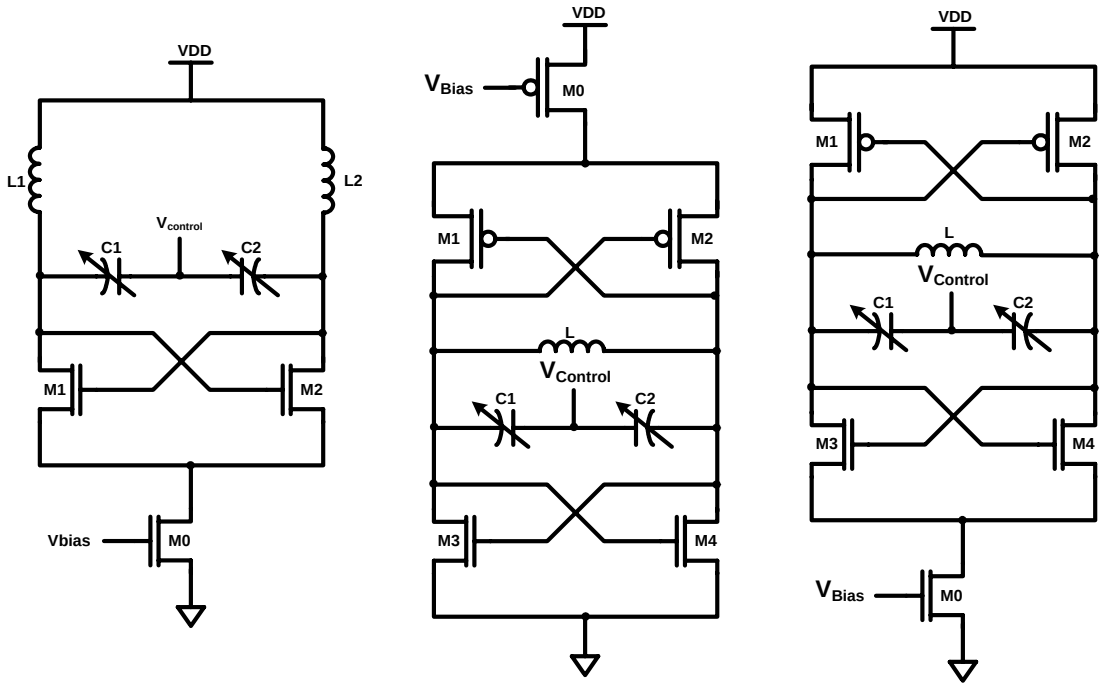
	LC Oscillator	Ring Oscillator	Multi-Vibrator
Speed	**Technology Dependent (0.01-10s of GHz)**		
Phase Noise	**Good**	**Poor**	
Integration	**Poor (Inductor and Varactor)**	**Excellent**	
Tunability	**Narrow**	**Wide**	
Stability	**Good**	**Poor (needs acquisition aid with a PLL)**	

2.1.2 LC-Based VCOs

Figure 2-8 illustrates three forms of typical LC-VCO implementations in CMOS. Figure 2-8a represents the simplest implementation, with an nMOS current source and an nMOS differential pair as the gain stage (also referred to as the *negative resistance*), which cancels out the loss of the tank. A pair of varactors has been used for frequency tuning. The use of differential signalling

provides another advantage over single-ended VCOs (e.g., ring oscillator in Figure 2-6). It results in higher oscillation swing in a constantly shrinking supply voltage environment, and less susceptibility to environmental noise due to rejection of the common-mode component of the noise.

Figure 2-8b and Figure 2-8c represent two other popular implementations of LC-VCOs. These implementations result in lower overall phase noise compared with the LC-VCO in Figure 2-8a. They have two differential pairs that generate negative transconductance to cancel the tank loss. In [13], the authors prove that if the oscillation waveform is symmetrical (i.e., equal rise and fall times), the DC component of the phase noise is eliminated, which is the component that also carries flicker (1/f) noise. As a result, the two architectures shown in Figure 2-8b and Figure 2-8c could potentially have lower phase noise compared with the architecture in Figure 2-8a, which has asymmetrical rise and fall times. Furthermore, the use of nMOS or pMOS current sources creates a level of shielding from the substrate (*ground*) or power supply (*Vdd*), respectively, which subsequently lowers the phase noise resulting from substrate or supply noise. In technologies where larger supply voltages are available, using voltage regulators is recommended for the VCO to further reduce the oscillator phase noise resulting from substrate and supply noise.



(a) Simple LC-VCO **(b) LC-VCO with a PMOS current source** **(c) LC-VCO with an nMOS current source**

Figure 2-8. Different versions of LC-based oscillator

Other than noise components contributed by the oscillator's active elements (as well as supply and substrate), there are other sources of noise resulting from the losses in non-ideal passive elements (inductors and varactors), which further degrade the overall phase noise performance of the LC oscillator. To reduce the noise floor due to the lossy inductors, inductors with higher quality factors (Q) need to be used, since they result in lower resistive loss and subsequently lower thermal noise and lower power dissipation. However, this, to some extent, is limited by the technology, as the thickness of the metal layers and substrate losses are technology dependent, leaving the designer with fewer degrees of design freedom (e.g., increasing the width of inductor wires to lower the loss would degrade the self-resonance frequency). Various solutions are limited by other criteria, such as silicon-area usage. Although the design of high-Q on-chip inductors is a topic of active research, our focus in this work remains mainly on varactors as the tuning element of LC-VCOs. The design,

characterization, and modelling of the varactors significantly affect the overall performance of the LC-VCO.

2.2 CDR Phase Detectors

Clock and data recovery is used to regenerate the transmitted data from the distorted, noisy data received at the receiver. The clock recovery task can be performed using either feedback or open-loop systems. A closed-loop approach is achieved by using PLL to align the phase of data and clock, or in other words, to trigger the flip-flop (data regenerating component) every time it is in the middle of the data eye.

Figure 2-9 illustrates a generic PLL-based clock and data recovery (CDR) system. Many recent closed-loop CDR architectures [14-44] have utilized different circuits for their voltage-controlled oscillator (VCO), phase detector (PD) and/or phase/frequency detector (PFD). The choice of circuit and system architecture depends on many design factors defined in accordance with the application, as well as other general constraints such as types of accessible technology processes, available space (e.g., silicon area), maximum available supply voltage, and, obviously, cost. Some of the key design factors include link speed, jitter/phase noise, bit error rate (BER), and power consumption.

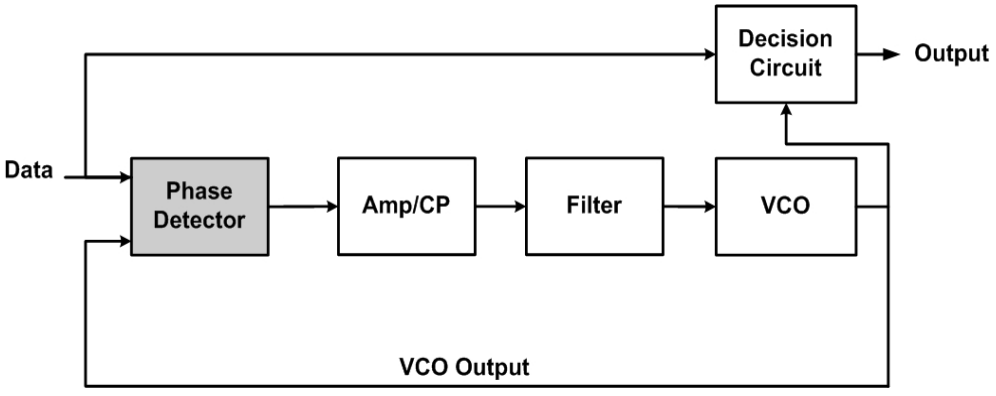


Figure 2-9. Block diagram of a generic clock and data recovery system.

Among the stated design factors, jitter is a key factor that can affect the choice of the VCO as well as the PD. This parameter, which is equivalently

referred to as phase noise in the frequency domain, indicates the amount of unwanted variation in the clock period. Different metrics are used to indicate the system jitter: *rms jitter* (in the context of *random jitter)* in PLL is usually defined as the standard deviation (σ_x) of the phase difference between the transmitted clock/data and the recovered clock [45]. The *peak-to-peak jitter* (i.e., a metric to measure *deterministic jitter*) is the maximum variation of the clock edges. Since *jitter* is a very important characteristic of CDR systems (and PLLs in general), designers have used different terms in order to explain the jitter performance of the system. Appendix A: "Jitter terminology", explains some of the most well-known terms used for jitter.

The amount of jitter in the recovered clock could stem from different sources:

- Internal noises (e.g., thermal, and flicker noise) generated by active and passive elements in CDR blocks
- Jitter associated with the incoming data (or the reference clock)
- Noises coupled into the blocks from the external sources (e.g., noise on the substrate or supply lines)
- Ripples on the VCO control line, which could be due to the data patterns
- Non-idealities (low Q) of the resonance circuits (in case of LC-VCO) which could cause internal noise

The dynamics of the CDR loop shapes the overall response of the system to these jitters.

One of the significant contributors to CDR jitter is the VCO, which was examined earlier in this chapter [45-47]. Here, we turn our attention to the PD as another important component affecting the *jitter transfer function* and the dynamics of the CDR loop.

There have been various types of phase detection circuits reported in the literature. However, when examined carefully, more than eighty percent of these

circuits are variants of two types of circuits: linear, or Hogge PD [48], shown in Figure 2-10 and bang-bang (BB), a.k.a. Alexander PD [49], shown in Figure 2-11.

We reviewed all of the papers published in the IEEE International Solid-State Circuits Conference (ISSCC) from 2001 to 2007, in order to determine the trend in the leading-edge circuit design community, and the reasons for choosing between different types of PDs. We found a total of 31 papers that had incorporated a PLL-based CDR in their systems [14-44]. Seven of them had used a variant of linear PD (i.e., 23%), and nineteen used BBPD (i.e., 62%). Five of the papers had either used a different type of PD (e.g., phase to digital in [39]) or had not reported details of their PD circuit. Although this survey is by no means conclusive, it could be a good indication of designer preference. Figure 2-12 summarizes this survey, using a bar-chart. The chart shows how many times each type of PD has been used in different technologies, and has been sorted in ascending order according to the technology transition frequency, f_T. It shows that BBPD is more popular, especially in CMOS designs where f_T tends to be lower.

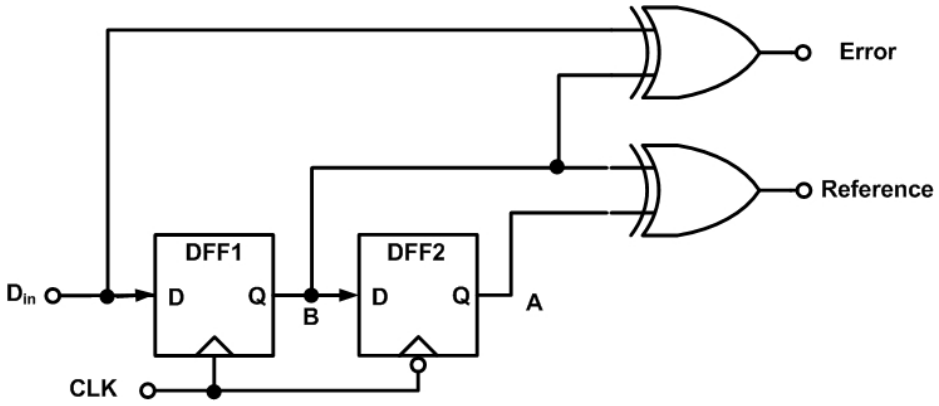


Figure 2-10. Hogge (linear) phase detector [48]**.**

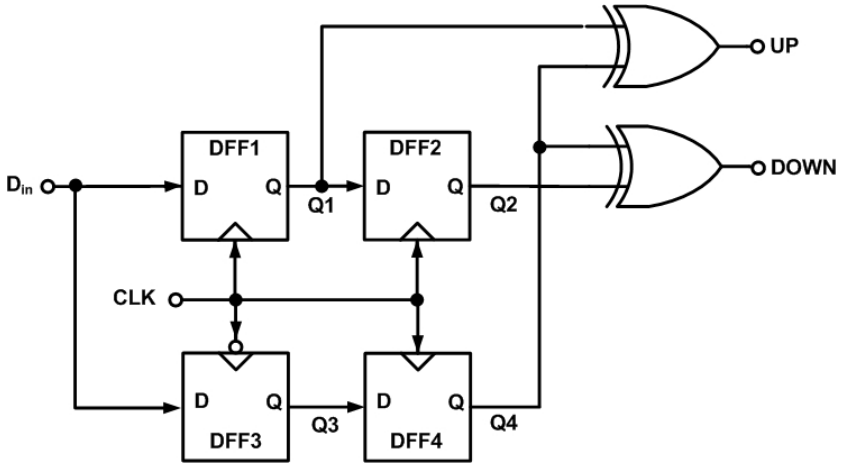


Figure 2-11. Alexander (bang-bang) phase detector [49]**.**

In an effort to obtain more conclusive results, we sorted all designs in a two dimensional system where the y-axis represents the ratio of the link speed to transition frequency, f_T, and the x-axis represents the link speed. We used the ratio of speed to f_T in order to obtain normalized results and make them comparable. Since some papers did not report their nominal transition frequency, we used some approximate numbers obtained from [50, 51]. This comparison is drawn in Figure 2-13.

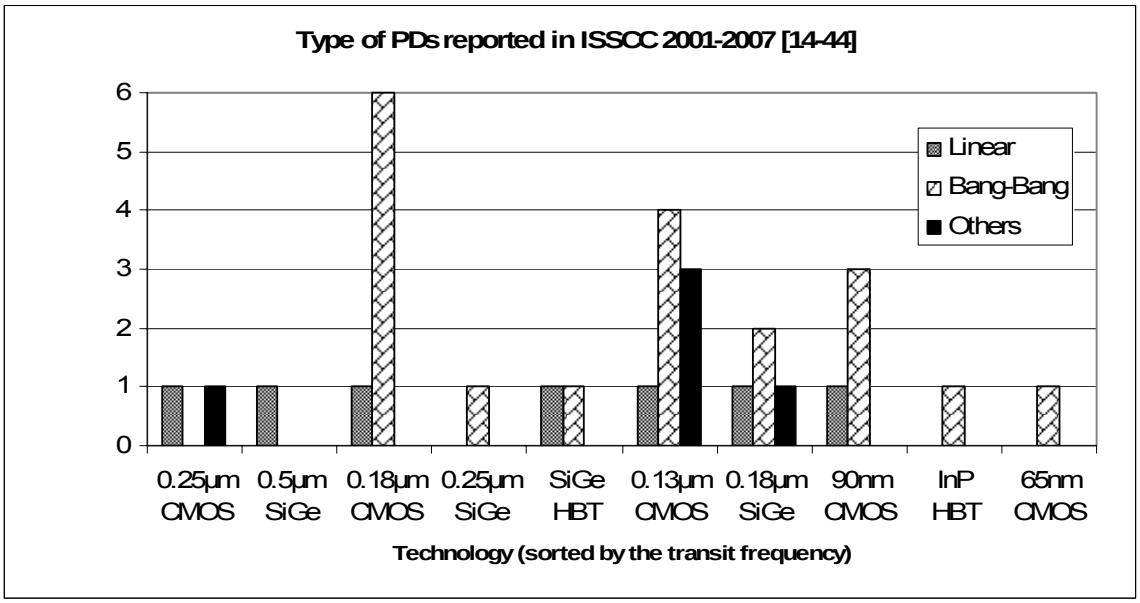


Figure 2-12. Phase detectors usage per technology process reported in ISSCC (2001-2007)

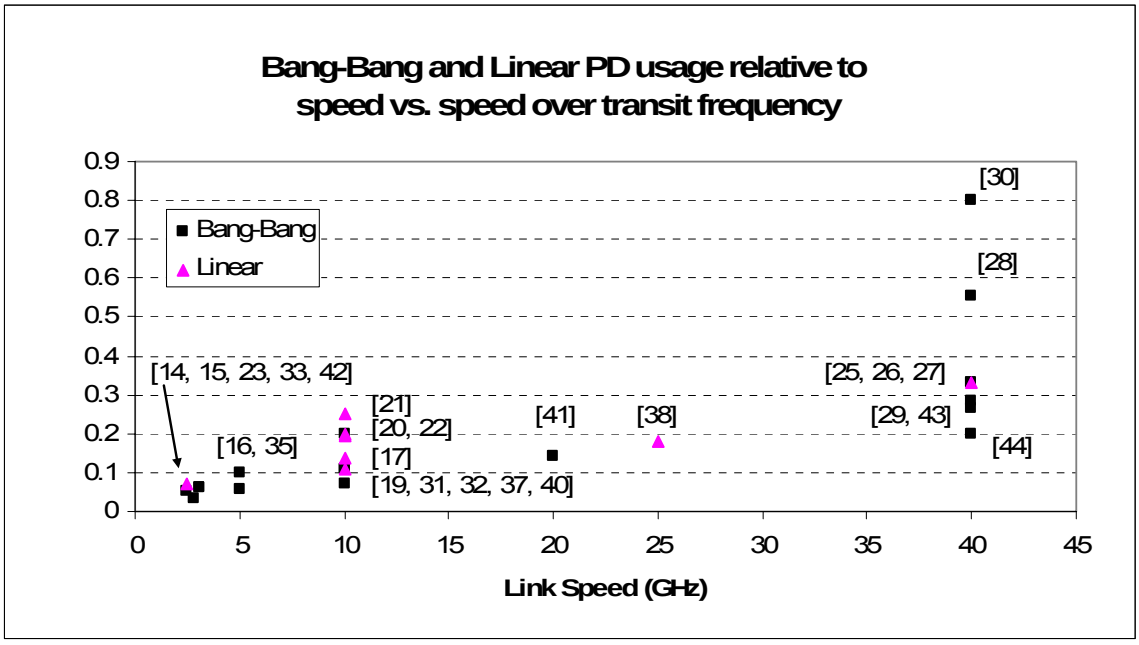


Figure 2-13. Bang-bang vs. linear phase detector used in recent ISSCC works from 2001-2007, sorted based on the ratio of link speed to transition frequency.

It can be seen that as the data rate (i.e., the link speed) becomes comparable to the f_T of the process, the use of BBPD is almost inevitable [28, 30]. In addition, BBPD has been used more frequently, especially, at higher data rates relative to linear PD. This observation is consistent with [52], which claims that up until 2001 all CDRs operating at data rates greater than $0.4f_T$ are bang-bang. As a result, Bang-Bang PD has become a popular choice for state-of-the-art high-speed CDR systems. Designers have had different reasons to justify their preference. Some of the facts underlying their decisions are summarized here:

- Timing skew and speed of linear PD circuits are the limiting factors for aggressive designs because they produce narrow pulses with widths proportional to the phase error between the data and clock. This requires a process speed in excess of that required to sample data at a given rate [52]. On the other hand, a full-rate BB CDR could literally operate up to the speed of the fastest flip-flop that could be designed in a process.

- Most linear PDs require at least some analog processing at the full bit rate, which limits their speed and makes it difficult to generalize the fraction-rate architecture [52].
- Linear PDs generally result in lower charge pump activity, which translates to lower jitter.
- Jitter of BBPDs, and the consequent ripples on the VCO control line, can be reduced by adding a third state to BB's binary operation (i.e., a ternary PD with three states: up, down and quiet or no change in the case of no transition).
- In many cases, BBPD gain is large enough to eliminate the need for a charge pump. Therefore, the charge pump circuit can be replaced by a voltage to current (V/I) converter.
- It is claimed that BBPDs are less sensitive to data patterns [53].
- It is shown that the BB loop output jitter grows at the square-root of the input jitter, as opposed to the linear dependence in linear PDs [52].
- BBPD leads to highly nonlinear PLL dynamics, which complicates the effort to find the required jitter-transfer characteristic [39].
- The high gain of BBPD at zero phase error suppresses static phase error due to charge-pump offset, and enables superior phase alignment for retiming the data symbols [35].
- Since the gain of the BBPD is dependent on jitter amplitudes of the input data and the recovered clock, it is not suitable for applications such as the SONET OC-192 receiver. Such applications require accurately controlled loop bandwidth [40].
- BB CDRs could combine the input retiming and phase detection functionalities, which inherently optimizes retiming clock alignment [29].
- BBPDs have output pulses with a fixed width, which reduces the required circuit bandwidth compared with linear PDs with possibly very narrow pulses [29].

- In BBPD, interleaving allows a lower rate clock, which reduces data retiming metastability and enhances the sharpness of the phase detector error outputs [29].
- In terms of simulation and analysis of noise, BB CDR is very sensitive. Noise affects the large-signal behaviour of the system, which invalidates any use of small-signal noise analysis [54]. The majority of noise simulators are incapable of performing large-signal noise analysis. This requires a special simulation strategy to predict the noise performance of the BB CDR.
- Another major advantage of BBPD over linear PD is its ability to provide frequency detection in addition to phase detection without requiring an external reference. This is because bang-bang topologies can provide a strong beat frequency in the presence of a clock and data frequency mismatch [5].

Some analyses of BB CDR performance were conducted in [52] and [54]. In the following sections, we develop a system-level model for each of the two CDRs and then discuss the *jitter transfer*, *jitter generation* and *jitter tolerance* of each type.

2.3 Linear and Bang-Bang CDR Models

The phase detector in the PLL-based CDR applications must sense the phase difference between the input data and the clock only on data transitions. In the CDR application, unlike other types of PLL-based systems (e.g., clock synthesizer), the random nature of the data and the periodic behaviour of the clock make the average value of the error signal (i.e., the phase difference) pattern dependent. Therefore, a second signal (reference signal) is required to find the phase difference. Both linear and BBPDs have two output signals. In the next sections, we construct a system-level model for both linear and BB CDRs. We assume that the CDRs are running at the full rate (i.e., clock frequency is equal to the data rate). Similar models can be developed for less than full-rate (e.g., half-rate or quarter-rate) CDRs by slightly modifying this model.

2.3.1 Linear CDR Model

Figure 2-14 shows the average of the *error* signal (*PD out*) for the linear PD of Figure 2-10 when the phase difference (*phase error*) between the two inputs (*data* and *clock*) varies for one clock cycle or from $-\pi$ to $+\pi$. For this particular example, we have assumed a data transition rate of 100%. While the pulse width of the *error* signal is a function of the phase difference between the data and clock transitions, the width of the pulses on the *reference* is always constant. This property results in a constant average value, which stays at about 0.5 or in the middle (*reference* is not shown in Figure 2-14). Therefore, we can assume that *PD out* is linearly proportional to the *phase error* (φ_{Data}- φ_{Clock}).

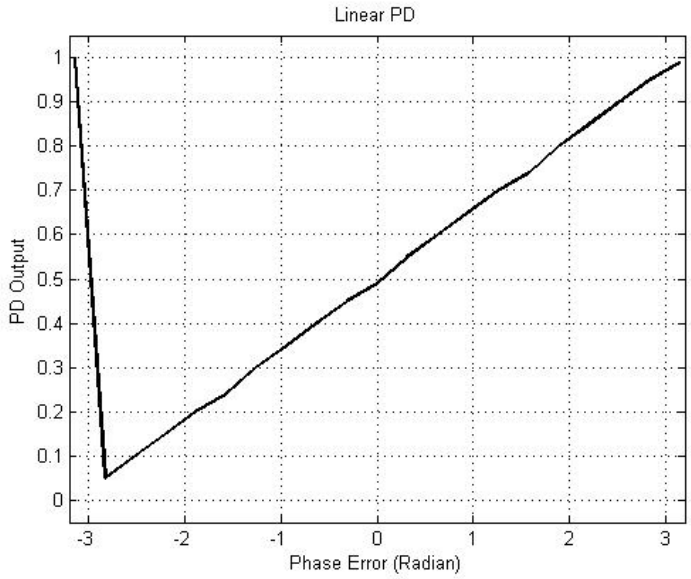


Figure 2-14. Simulated characteristic of the linear phase detector shown in Figure 2-10. PD out is the average of the *error* signal over one clock period, or 2π.

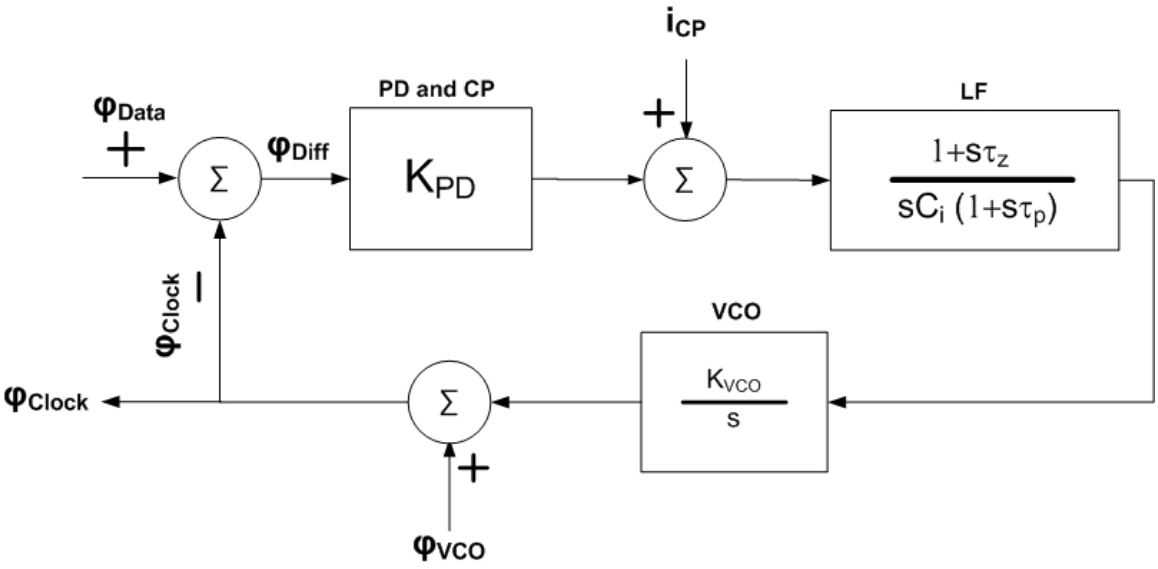


Figure 2-15. System-level model of a linear CDR.

The system-level model for the clock recovery portion of the linear CDR is depicted in Figure 2-15. Here, K_{PD} is the gain of the phase detector (or the combined gain of the PD and charge pump (*CP*)). VCO has been shown as an integrator with the gain of K_{VCO}. We have also identified major sources of noise drawn as excess inputs in the figure including noise generated in PD and CP, shown as a current input, $i_{CP,}$ and noise generated by VCO. The latter is frequency-modulated to the output frequency range shown as excess phase, φ_{vco} at the output.

We have assumed that the filter is a simple second-order filter normally used in CDRs. Shown in Figure 2-16, this filter is a series combination of the resistor, R and the capacitor, C_1 in parallel with the second capacitor, C_2.

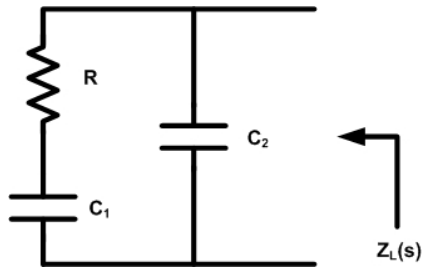


Figure 2-16. A second-order filter commonly used in PLL-based systems

Equation (2-2) is the expression of the impedance of this second-order filter, where the coefficients used in (2-2) are defined in (2-3), (2-4) and (2-5) according to the circuit of Figure 2-16.

$$Z_L(s) = \frac{1+\tau_z s}{C_i s\,(1+\tau_p\, s)}, \tag{2-2}$$

$$C_i = C_1 + C_2, \tag{2-3}$$

$$\tau_z = RC_1, \tag{2-4}$$

$$\tau_p = \frac{RC_1C_2}{C_1+C_2}. \tag{2-5}$$

When the *clock* is in the middle of the *data eye*, the *reference* and *error* outputs are equal but phase shifted by 180°. Therefore, integrating over one clock cycle results in zero sum. Since all the system blocks are assumed to be linear, we can define transfer functions to describe the relationship between the outputs to the different inputs shown in Figure 2-15.

If we assume that all the inputs in Figure 2-15 except for Φ_{Data}, the main data input, are zero, the main transfer function from data to output, which is also known as the *jitter transfer function* is calculated as follows:

$$\Phi_{Diff}(s) = \Phi_{Data}(s) - \Phi_{Clock}(s), \tag{2-6}$$

$$G_{fwd}(s) = \frac{\Phi_{Clock}(s)}{\Phi_{diff}(s)} = \frac{K_{PD}K_{VCO}Z_L(s)}{s}, \tag{2-7}$$

$$G_{Data}(s) = \frac{\Phi_{Clock}(s)}{\Phi_{Data}(s)} = \frac{G_{fwd}(s)}{1+G_{fwd}(s)}, \tag{2-8}$$

$$\frac{\varphi_{Clock}(s)}{\varphi_{Data}(s)} = \frac{K_{PD}K_{VCO}(1+s\tau_z)}{C_i s^2(1+s\tau_p)+K_{PD}K_{VCO}(1+s\tau_z)}. \tag{2-9}$$

where $Z_L(s)$ in (2-7) is the impedance of the second order filter and has been substituted by (2-2) in (2-9).

Figure 2-17 shows the simulated *jitter transfer* characteristics of a typical linear CDR. The transfer function has three poles where the third (due to capacitor C_2) is normally far apart from the other two accounting for the 40dB/dec decline in Figure 2-17. In most cases, the system can be analyzed with only two dominant poles in order to reduce its complexity.

Jitter generation, which is the measure of the intrinsic jitter produced by the CDR, is measured at the CDR's output. Two sources of jitter generation are the VCO and phase detector, whose corresponding transfer functions are as follows:

$$G_{VCO}(s) = \frac{\Phi_{Clock}(s)}{\Phi_{VCO}(s)} = \frac{1}{1 + G_{fwd}(s)}, \tag{2-10}$$

$$G_{PD}(s) = \frac{\Phi_{Clock}(s)}{i_{CP}(s)} = \frac{2\pi}{K_{PD}} G_{Data}(s). \tag{2-11}$$

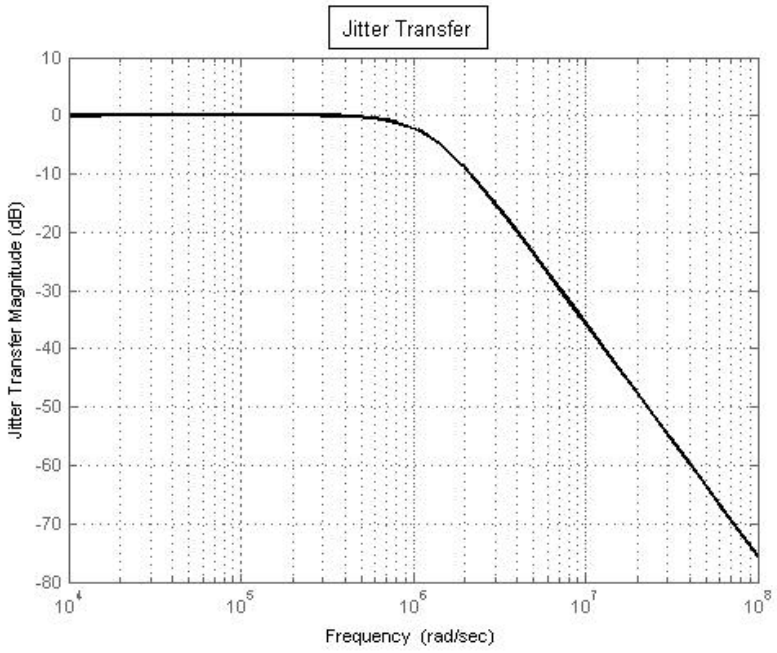


Figure 2-17. Jitter transfer characteristics of a typical linear CDR.

It can be inferred from these transfer functions that (2-10) has high-pass characteristics, while (2-11) is similar to *jitter transfer* but with a different gain.

Therefore, it is very important to design a low-noise VCO, as its high frequency jitter directly traverses to the output with no attenuation.

Jitter tolerance is the maximum input jitter that a CDR loop can tolerate without increasing the *BER* at a given jitter frequency [54]. The BER increases rapidly as the *phase error* approaches π (Figure 2-14). Assuming that the input phase jitter is in the sinusoidal form of

$$\Phi_{Data}(t) = \Phi_m \cos(\omega_\Phi t) \tag{2-12}$$

where ω_Φ is the angular frequency of the jitter and Φ_m is the amplitude of the jitter then as Φ_{Diff} (the phase error) approaches π [=half unit interval (UI)], *BER* rises rapidly [54]. Since (2-9) has low-pass characteristics and the rate of bit errors is a function of jitter amplitude and frequency, we can intuitively explain that at low jitter frequencies with a relatively high loop gain, the clock phase tracks the data phase very closely and Φ_{Clock}-Φ_{Data} rapidly goes to zero. Therefore, the larger *BER* at low frequencies is due to larger jitter amplitude. However, as jitter frequency increases, the closed-loop gain drops (Figure 2-17) and CDR loses its fast phase-tracking capability. More accurately, we can write

$$\left|\Phi_{Clock} - \Phi_{Data}\right| \geq \pi\ , \tag{2-13}$$

$$\left|\Phi_m (G_{Data} - 1)\right| = \pi\ , \tag{2-14}$$

$$Jitter Tolerance = \left|\Phi_{m,Max}\right| = \frac{\pi}{\left|G_{Data} - 1\right|}\ , \tag{2-15}$$

Which is illustrated in Figure 2-18. The *jitter tolerance* has been drawn for the linear CDR of Figure 2-15, which has a third-order *jitter-transfer function*. At lower frequencies, the slope is 40dB/dec, which later drops to 20dB/dec before it flattens out at high frequencies.

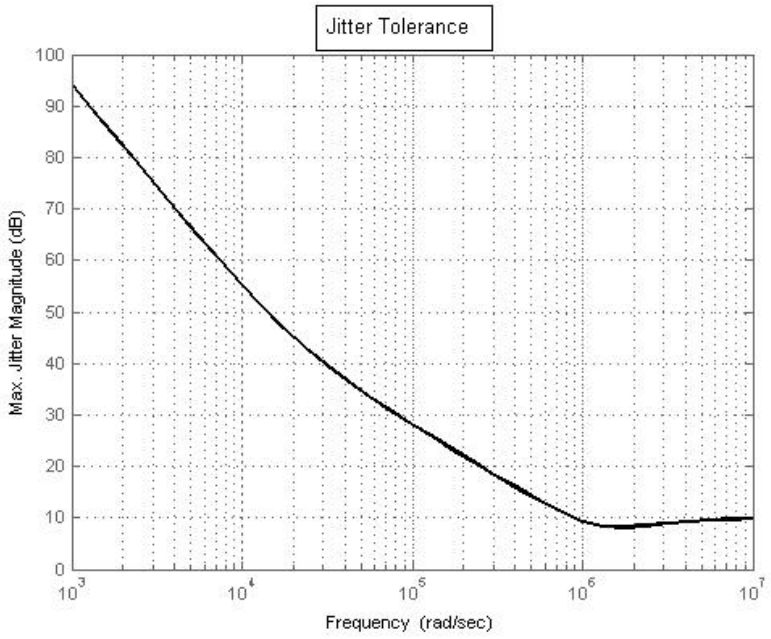


Figure 2-18. Jitter tolerance of a typical linear CDR.

2.3.2 Bang-Bang PD Model

Figure 2-19 shows the simulated characteristic of the BBPD shown in Figure 2-11. The output (*PD out*) is the average of the difference between the two binary signals (*up* and *down*) versus the *phase error* of the *clock* and *data* in one clock period or 2π radians (from $-\pi$ to $+\pi$). It is apparent that besides a narrow range around zero *phase error,* where PD shows a relatively constant finite slope, the relationship between *PD out* and *phase error* is nonlinear. If the *phase error* is less than zero, *PD out* is -1; otherwise it is +1. This result invalidates the straightforward linear time invariant (LTI) analysis that we performed earlier for the linear PD. The linear part is a side-effect of flip-flop metastability as well as the presence of jitter, which further helps linearize the narrow range [54].

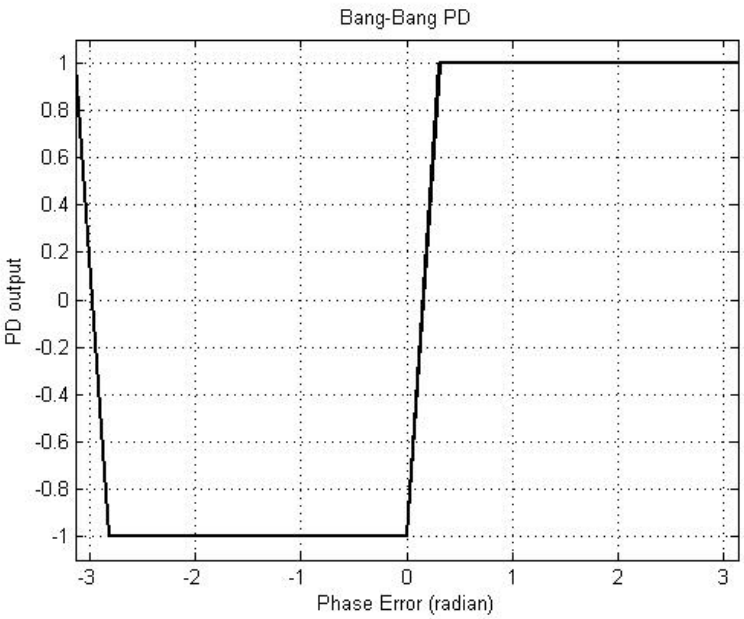


Figure 2-19. Simulated characteristic of the bang-bang phase detector shown in Figure 2-11.

If we assume an infinite slope around zero phase error, we can model the BBPD with the *sign function* and draw the BB CDR diagram as shown in Figure 2-20. We have modelled the PD using a *sign function* followed by a *gain* stage. The *sign function* samples the sign of *phase error* at the time intervals equal to the clock period (i.e., clock rising or falling edges). The sampling time is not constant and varies with the frequency of VCO. This non-uniform sampling time adds to the complexity of analysis. The rest of the system (i.e., a second-order filter and the VCO) are similar to the linear model. A frequency domain analysis of first-order and second-order loop dynamics of an ideal bang-bang (i.e., with infinite slope of the *sign function*) was conducted in [52]. A more complete analysis, which accounts for the finite slope of the BBPD, is discussed in [54]. Here we consider only the approximate expressions derived for *jitter transfer, jitter tolerance* and *jitter generation* of the bang-bang CDR in [52] and [54] without proof. Interested readers can refer to these two references for more information.

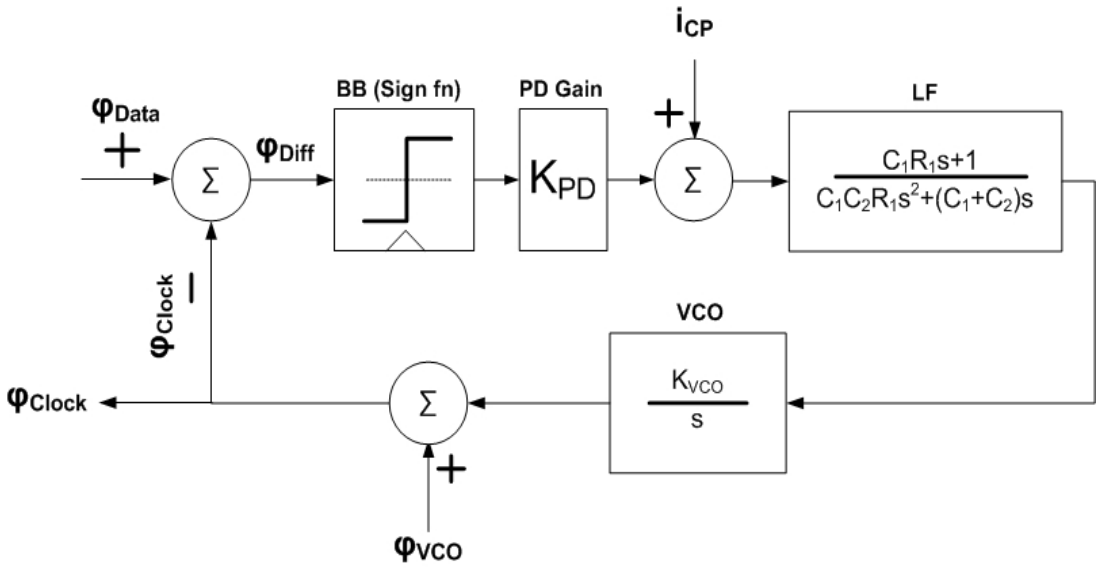


Figure 2-20. System-level model of the bang-bang CDR.

Jitter transfer of the bang-bang CDR comprises of two parts: the linear part and the non-linear part where *phase error* is larger than the threshold of the linear operation region (i.e., Φ_{lin}) and BBPD starts slewing. Similar to our linear analysis, we assume that input jitter is in the form of (2-12). For simplification, we further assume that the capacitor, C_2 is at least one order of magnitude smaller than C_1 and that C_1 is large enough to let the VCO control voltage track $I_{cp}R_1$ when slewing. Here I_{CP} is the charge pump current (different from the noise current, i_{cp} shown in Figure 2-20). With these assumptions, we can approximate the *jitter transfer* with a first order system as [54]:

$$G_{Data}(s) = \frac{\Phi_{Clock}(s)}{\Phi_{Data}(s)} = \frac{1}{1 + \dfrac{s}{\omega_{-3dB}}}, \tag{2-16}$$

where ω_{-3dB} is a function of maximum jitter amplitude, $\Phi_{Data,Max}$ as follows

$$\omega_{-3dB} = \frac{\pi K_{VCO} I_{CP} R_1}{2\Phi_m}. \tag{2-17}$$

If $\Phi_m < \Phi_{lin}$ the bang-bang CDR turns into a linear CDR and same linear modelling described in the previous section could apply. This dependence of the *jitter transfer* on the jitter amplitude of data when $\Phi_m > \Phi_{lin}$ is a drawback of the BB CDR; because it reduces the tracking range of the CDR and further limits the designer's power of prediction for the jitter transfer of the CDR.

Jitter tolerance of the BB CDR is very similar to the linear CDR shown in Figure 2-18. At very low frequencies, it has slope of 40dB/dec. We can write:

$$\left|\Phi_{m,Max}\right| = 1.26\frac{K_{VCO}I_{CP}\pi^2}{4C_1\omega_\phi{}^2}. \tag{2-18}$$

At higher frequencies, it follows this relationship:

$$\left|\Phi_{m,Max}\right| = \pi\sqrt{1+\frac{K_{VCO}{}^2 I_{CP}{}^2 R_1{}^2}{4\omega_\phi{}^2}}, \tag{2-19}$$

which has a declining slope of 20dB/dec before it flattens out at around 0.5UI.

2.4 Time-Domain Comparison of the Two PDs

In the previous section, we showed that the *jitter transfer* of the BBPD is a function of the input jitter amplitude. In this section, we analyze the two systems in the time domain to see how those frequency domain expressions shown in the previous sections manifest themselves in the time domain. We use them to predict the CDR behaviour in the time-domain. In order to perform a jitter analysis, we need to add both *white noise* and *flicker noise,* a.k.a. *1/f noise* to the data as well as the control line of the VCO. *White noise* can be generated in *Matlab*® by simply activating the random number generator (e.g., *randn()*) and giving the desired *standard deviation* and *mean* values. However, *flicker noise* generation is not so straightforward. Here, we use the sinusoidal form of jitter shown in (2-12) for our modelling. To show the effect of frequency, we use two different sample frequencies (high and low), which is instructive when the noise is frequency dependent, e.g., 1/f noise, present in practical circuits. For readers

interested in noise modelling, a method for *flicker noise generation and modelling* in *Matlab*® is described in *Appendix B.*

2.4.1 Time-Domain Simulations of Bang-Bang and Linear CDRs with Noise Considerations

In order to compare these two CDRs in the time domain, we devised two systems for linear and bang-bang CDRs as depicted in Figure 2-15 and Figure 2-19, respectively. Using *Simulink*® both systems were simulated at the full rate. The values of the filter components used were as follows: R1=1KΩ, C1=1nF and C2=100pF for both systems. The VCO gain was 1MHz/V and the PD gain, K_{PD}, was set to 1m for the BB CDR and 0.1m for the linear CDR. Two sinusoidal noise sources (i.e., shown in (2-12)) were summed up with the input phase, one oscillating at 10 MHz (in band) and the second at 100 MHz (out of band) in order to observe the CDR response to high-frequency and low-frequency jitters as well as the jitter amplitude. We did two experiments with the linear CDR: first, we selected the amplitude of the high-frequency jitter to be $\Phi_{m1}=1$, and the low-frequency jitter to be $\Phi_{m2}=10$. The phase of the data (or the clock that transmits the data) then becomes

$$\Phi_{Data}(t) = \omega t + \Phi_{m1}\cos(\omega_{\Phi 1} t) + \Phi_{m2}\cos(\omega_{\Phi 2} t). \qquad (2\text{-}20)$$

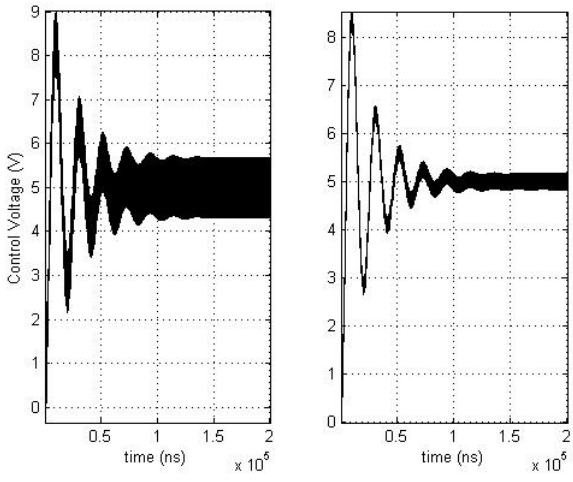


Figure 2-21. Operation of the linear CDR in the time domain. Left-hand side is the control voltage of the VCO when the low-frequency jitter source has large amplitude. Right-hand side is the control voltage when the high-frequency jitter source has large amplitude.

For the second experiment, we switched Φ_{m1} and $\Phi_{m2.}$ We picked the larger amplitude (i.e., 10) for the high-frequency source and the smaller amplitude (i.e., 1) for the low-frequency source. Figure 2-21 shows the VCO control line for the linear CDR for each of the above cases. It can be seen that the high-frequency jitters (right-hand side) are suppressed more than low-frequency jitters (left-hand side). This result shows the low-pass characteristics of the jitter transfer function, as anticipated from (2-8).

We repeated the same set of experiments for the bang-bang CDR, and, as expected, obtained similar results (Figure 2-22). The BB CDR also suppresses high-frequency jitters more than low-frequency. In other words, the system has low-pass characteristics.

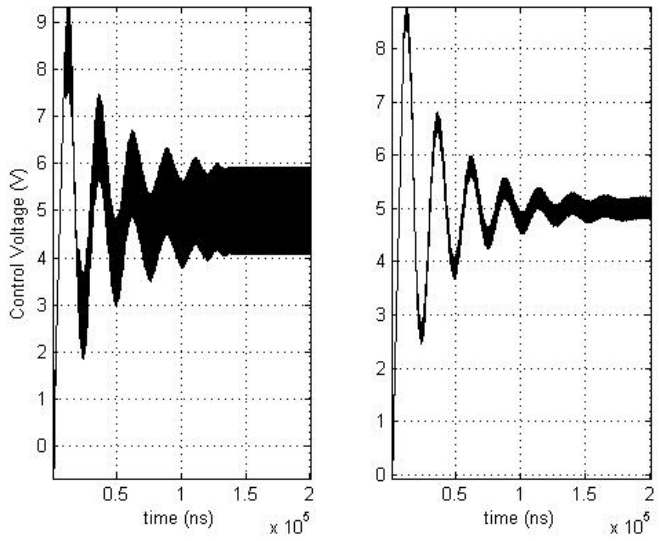


Figure 2-22. Operation of the bang-bang CDR in the time domain. Left-hand side is the control voltage of the VCO when the low-frequency jitter source has larger amplitude. Right-hand side, is the control voltage when the high-frequency jitter source has larger amplitude.

One characteristic of the BB CDR that we discussed earlier is the dependence of the jitter transfer function on the amplitude of the jitter. To show this, we repeated the same experiment. However, this time we turned off both of the sinusoidal jitter sources: the result is illustrated in Figure 2-23. Note that the shape of the response has changed from that of Figure 2-22. The settling time

has improved and the system does not show oscillatory behavior as much as before. This is because the dynamics of the system has changed and the -3dB frequency of the jitter transfer function is lower now since the jitter amplitude is smaller (i.e., the dependence of the jitter transfer function on the jitter amplitude).

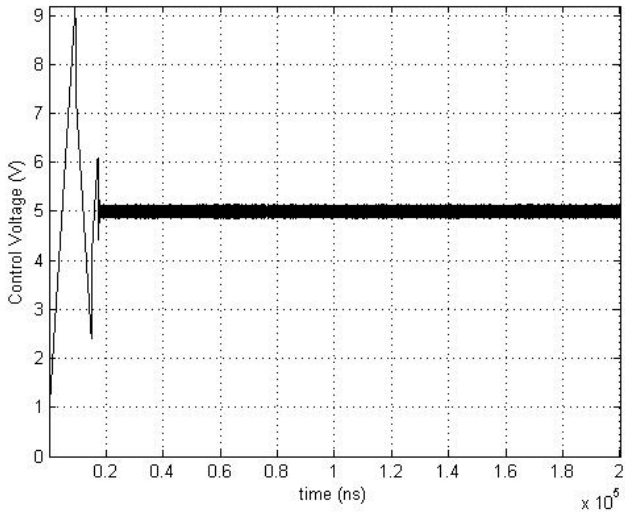


Figure 2-23. BB CDR response to zero input jitter source.

2.5 Summary and Conclusion

VCOs are among the critical building blocks of many communication systems such as CDRs and wireless RF transceivers. Their conversion gain (voltage to frequency) and in particular, phase noise, can affect overall system performance. Among various VCO architectures, LC-VCOs have superior phase noise performance and are therefore used extensively in RF transceivers as well as CDR systems.

Our survey of most recent works on CDR systems published from 2001 to 2007 in ISSCC revealed that designers tend to use BBPD whenever the speed requirement of the link is comparable to the process transition frequency. In addition, the use of BBPD is more common in state-of-the-art designs. This preference for using BBPD is attributed to the simple binary phase detection that can be performed at any speed, provided there is a functional flip-flop at that frequency. Moreover, the design of multi-phase CDR architectures is more

feasible with BBPD, as linear PD requires some analog data processing at the link speed. BBPDs are especially suitable where unaided frequency acquisition must be performed [5]. On the contrary, unlike linear CDRs, bang-bang jitter transfer characteristics depend on the jitter amplitude. Another drawback of the BB CDR is the difficulty of noise performance prediction, as it is highly nonlinear and requires large-signal noise analysis whereas most current simulators are only capable of small-signal noise simulation.

System-level models for the two types of CDRs were developed (with noise consideration). Important CDR parameters such as jitter transfer, jitter tolerance and jitter generation were derived and compared for the two systems.

A time-domain simulation of both systems with jitter consideration at the input line was performed. We demonstrated that the jitter transfer of a BB CDR is a function of input jitter amplitude when the phase error is larger than the threshold of the linear-range operation of the BBPD.

Chapter 3

Modelling and Characterization of MOS Varactors

In this chapter, a detailed study is performed on a popular type of varactor used as a tuning component in most recent LC-VCO circuits. Some varactor test structures are used to characterize the tuning curve of the LC-VCOs and their relationship with the C-V curve of varactors. A novel practical model for accumulation-mode MOS (AMOS) varactors is introduced, which can be easily migrated to different technologies given that the model for MOS transistors has already been defined. This model is superior to existing mathematical models (for example those based on *hyperbolic tangent* function). The existing models, in our experience and that of others [55], would often require a long simulation time and/or are prone to convergence problems, particularly in advanced processes. Another drawback of current models is that foundries provide a few sample varactor models, which are accurate only when the required capacitance is in the foundry pre-defined range. In some cases, even this limited number of samples is provided few years after the first release of the design kit. Besides these limitations, foundries usually provide general-purpose varactor models (e.g., based on curve fitting at mid-frequency operation), that are not designed for high-performance applications (i.e., minimum gate lengths) [55].

Our new model is intended to address these issues by using sub-circuit components that come with the design kit in the first release. Although our modelling and characterization of this type of varactor has been performed in a standard 0.13μm CMOS, we have verified the results by using simulation and comparison of LC-VCO and varactors in a more mature technology, a standard

0.18μm CMOS. All of our results show good agreement between the model and either our measured results or foundry-provided models. Section 3.5 details these experimental and simulation results. The chapter is concluded in Section 3.6.

3.1 Varactors

A varactor is a principal component of an LC-VCO used for frequency fine-tuning. Digitally-controlled switched varactors or switched capacitors could also be used for coarse-tuning in some designs. Traditionally, reversed-biased pn junction diodes have acted as the varactor for LC-VCOs (this is still true in the case of bipolar VCOs). However, MOS-based varactors are gaining popularity over the reverse-biased diodes due to their wider tuning range and higher Q factor, both of which improve with every new process generation [56]. Higher doping levels in silicon, which in turn results in lower resistive losses and lower phase noise, have driven this improvement. This has become more evident in recent designs in advanced CMOS technologies (e.g., 0.18μm, 0.13μm, 90nm) as implementation of monolithic high-speed VCOs becomes feasible [5, 53].

An nMOS varactor can have the same structure as an nMOS transistor, with gate as the first terminal and drain, source, and bulk connected together to form the second terminal (Figure 3-1). MOS varactors operate in four main regions, based on the voltage across the varactor terminals: accumulation, depletion, weak inversion, and strong inversion (Figure 3-2).

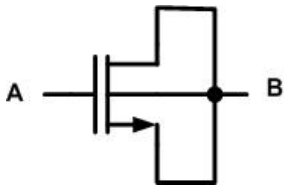


Figure 3-1. An nMOS transistor configured as a varactor

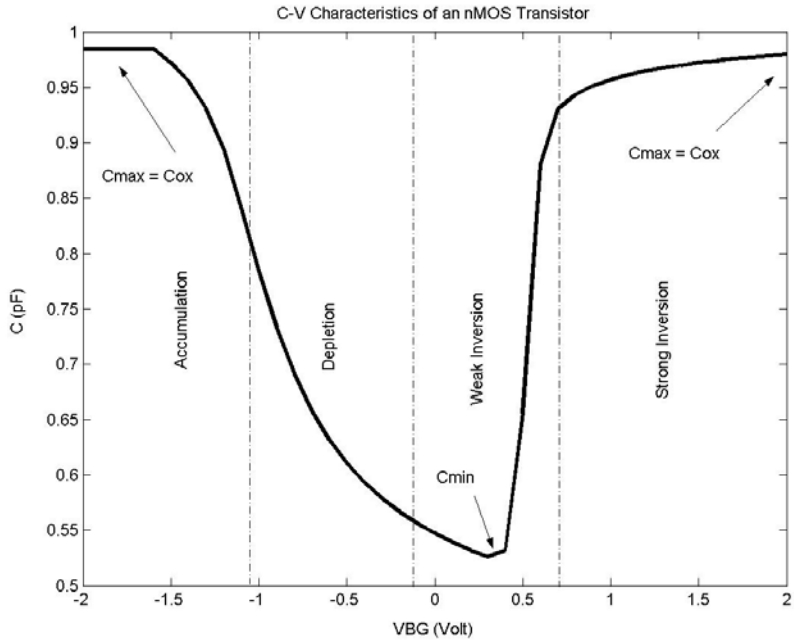


Figure 3-2. C-V characteristics of an nMOS transistor (Figure 3-1)

Most varactors are designed to predominantly operate in accumulation and strong inversion regions. A recent study on accumulation-mode and inversion-mode varactors reveals that LC oscillators based on accumulation-mode varactors demonstrate lower power consumption and lower phase noise at large offset frequencies from the carrier than those based on strong inversion varactors [56].

In most applications, designers would like to ensure that the capacitance of the varactor is a monotonic function of the biasing voltage. In an LC-VCO, it would be desirable to have the varactor operate predominantly in accumulation mode. However, using a regular nMOS, as shown in Figure 3-1, does not guarantee this, as the operation region is voltage-dependent. It is also worth noting that the C-V curve of a regular nMOS is frequency-dependent. Figure 3-3 illustrates the cross-section of a varactor structure. It may seem similar to an nMOS transistor; however, the n+ regions have been buried in an n-well, instead of a p-well. This configuration guarantees that the device does not ever enter the inversion-mode; hence, the name accumulation-mode MOS varactor (AMOS).

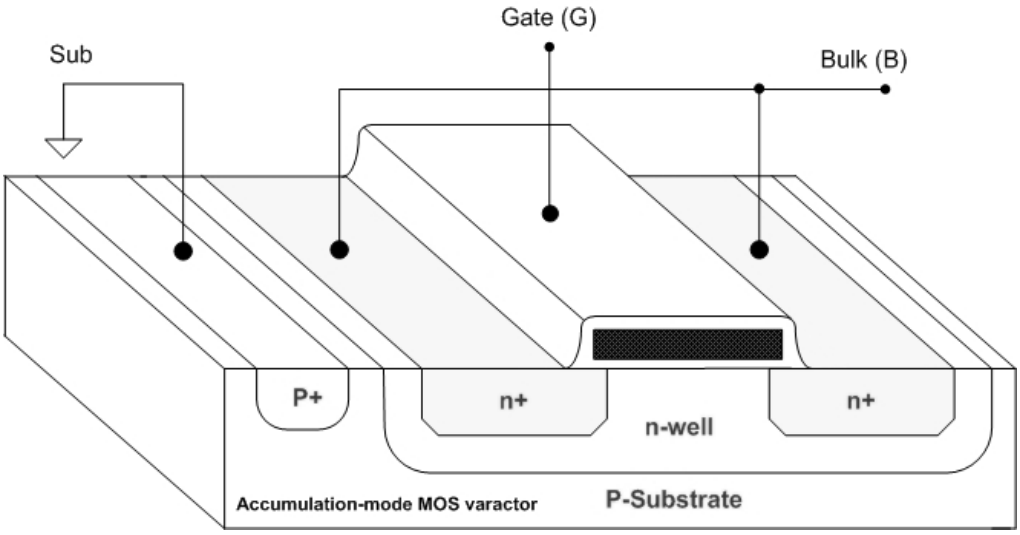


Figure 3-3. Cross-section of an accumulation-mode MOS varactor (AMOS)

The C-V characteristics of a MOS varactor can be predicted using 2D/3D numerical simulators. Unfortunately, these simulation tasks require precise knowledge of the underlying doping profiles, which is usually not readily available. An alternative is to perform capacitance measurements. However, measuring sub-pico-farad capacitances is difficult and requires a fairly expensive S-parameter RF measurement set-up. Therefore, it is very useful to predict the tuning characteristics of LC oscillators using standard foundry-supplied models for MOSFETs.

Recently, a lot of effort has been expended on modelling the C-V characteristics of MOS varactors, partly due to the increasing popularity of CMOS LC-VCOs in which such varactors are used. One type of model is based on physically meaningful parameters that describe the characteristics of the device with different equations for different regions of operation [57]. Other models based on the physical parameters of the device have been reported in [58, 86, 87]. However, simulating and using these types of models is not simple in SPICE or similar simulators, as they require defining mathematical functions inside the tool or requires access to the doping profile of the device. Other models have been developed based on sub-circuits utilizing BSIM SPICE models [59]. These models are suitable for simulator implementation within the

circuit-design environment and could be easily adopted for future technologies. In the following sections, we introduce a new model that takes advantage of already developed foundry models of transistors to create a practical model for AMOS varactors. First, we take a closer look at the tuning characteristics of LC-VCOs, which further emphasizes the need for a good varactor model. A detailed analysis of the tuning characteristics of these types of VCOs will be covered in Chapter 5.

3.2 VCO Tuning Characteristics

For the following analysis, we used a standard LC-VCO circuit with current source isolating the core of the oscillator from the ground, as shown in Figure 3-4. The circuit is designed for 5-6 GHz operation using a standard 0.13μm CMOS process. Inductance *L* is 1.5nH, and the total equivalent capacitance is in the range of *0.35pF* to *0.65pF*.

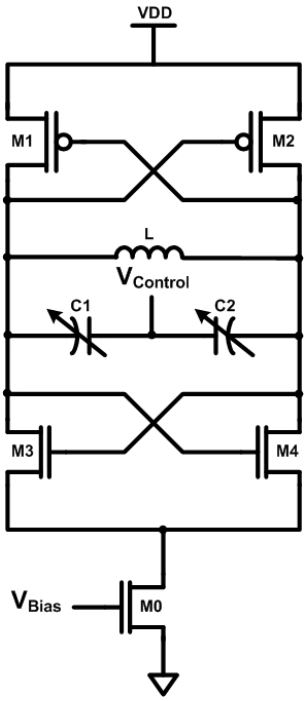


Figure 3-4. An LC-VCO with an nMOS current source

It may seem that modelling of the tuning characteristics is a straightforward task, as the oscillation frequency is given by the following well-known tank formula:

$$f_{osc} = \frac{1}{2\pi\sqrt{L\,C(V)}} \tag{3-1}$$

where *L* is the inductance and *C(V)* is the equivalent capacitance for a given biasing point. A simple test, however, indicates that the modelling process is more involved than it might initially appear. From the measured tuning characteristics, the equivalent capacitance can be extracted from (3-1) as follows (Note that the experimental devices are described later in the chapter):

$$C(V) = \frac{1}{4\pi^2 f_{osc}{}^2 L} \tag{3-2}$$

By determining the *C(V)* values using (3-2), an extracted piece-wise linear model of the voltage-dependent capacitance can be fed back to SPICE for LC-VCO simulation to compare the actual oscillation frequency with the simulated one. The results of this comparison, shown in Figure 3-5, indicate discrepancies up to 7%, which is quite significant and may often result in design iteration if the tuning curve is outside the desired range.

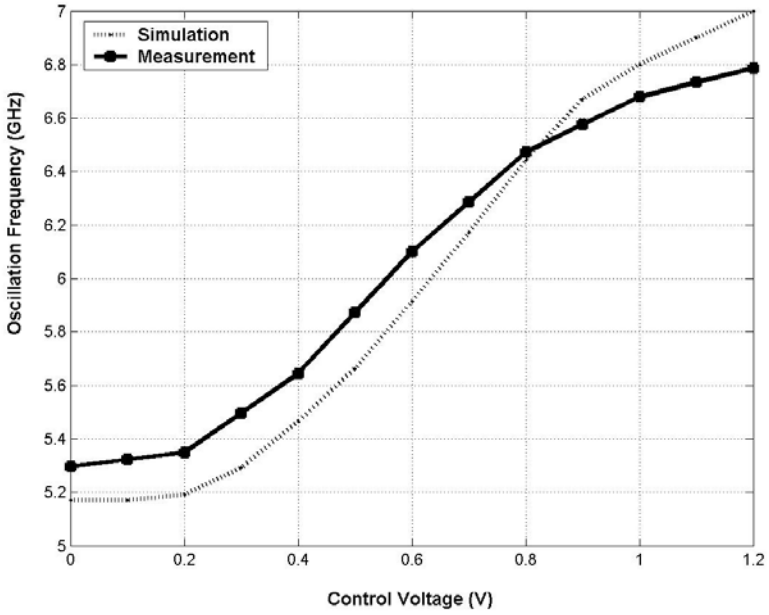


Figure 3-5. Measured vs. modeled VCO tuning characteristics (extracted piece-wise linear model)

These discrepancies can be attributed to the effective varactor capacitance. The varactor capacitance is modulated in time, depending on the signal swing of the oscillator output, which in turn changes the effective capacitance of the tank [60-62].

To approximate the effective capacitance, we found the ratio of the rms value of the varactor's current, *i(t)*, to the rms value of *dV/dt,* where *V(t)* is the periodic voltage across the varactor. In our calculations, we neglect the current components at harmonics of f_{osc} as they play a small role in determining the frequency of oscillation. Equation (3-3) is the revised version of (3-1), used to obtain the VCO's tuning characteristic:

$$f_{osc} = \frac{1}{2\pi\sqrt{L\left(C_{av}(V) + C_{par}(V)\right)}} \tag{3-3}$$

In this equation, C_{par} is the equivalent parasitic capacitance associated with the input of the next buffer, interconnects, and device capacitances of M1-M4 (Figure

3-4), the latter being somewhat voltage dependent. C_{av} is the average capacitance of C_1 and C_2 in series (Figure 3-4).

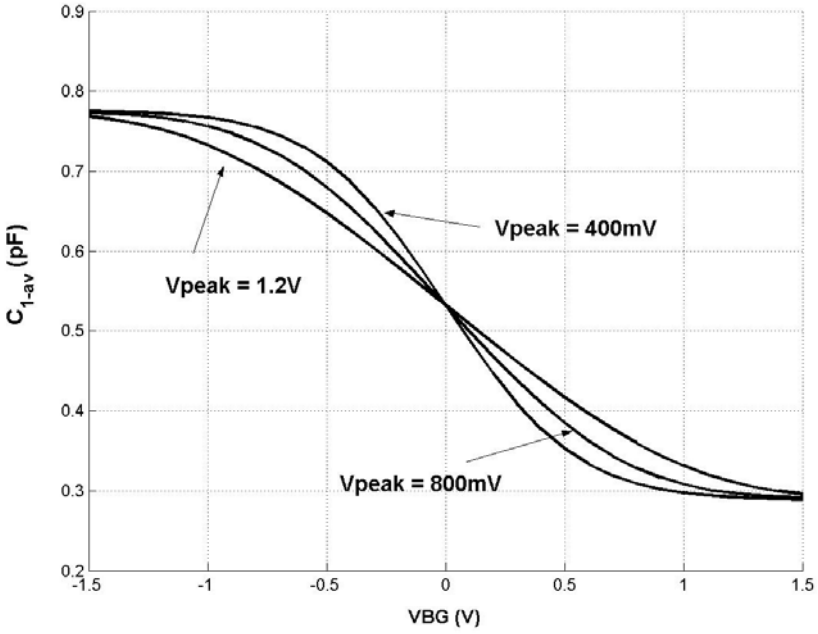


Figure 3-6. C-V characteristics for three different values of the oscillator voltage swing (Vpeak)

As shown in Figure 3-6, $C_{1\text{-}av}$ in the figure refers to the average capacitance of C_1 calculated for different output swings. If the voltage swing is small (compared to nonlinearities of the C-V characteristics), then the equivalent large-signal C-V characteristic closely resembles its small-signal counterpart. For large values of the voltage swing, however, the equivalent characteristics gets smoothed or averaged over a larger voltage range. As a result, the tuning characteristic becomes dependent on the voltage swing, which in turn is affected by the magnetic and resistive losses in the tank.

Calculation of the equivalent large-signal C-V characteristics is not easy and depends on many parameters as well as the shape of the oscillator's output (rectangular, sinusoidal, etc.). However, at high frequencies the current waveform can be approximated by a sinusoid due to the finite switching time and

limited gain [63]. Equation (3-4) shows the relationship between the swing and tank losses in this LC-VCO:

$$V_{Tank} \approx I_{tail} R_{loss}. \tag{3-4}$$

where R_{loss} is the equivalent parallel resistance of the tank and I_{tail} is the drain current of the current source transistor (M0 in Figure 2-8b). These calculations are rough approximations, designed to provide some insight into the actual differences between C-V characteristics when generated with different tank voltages. They indicate that more accurate modelling is required to find the correct C-V characteristics. Since this subject requires detailed mathematical analysis, Chapter 5 is dedicated to it.

In the following sections, we explain our method for varactor de-embedding, characterization, and parameter extraction, we used in order to find the actual varactor capacitance before we develop our new varactor model. These steps are required in order to have a benchmark for both modeling and comparison of the model values.

3.3 Characterization of AMOS Varactors

Several AMOS varactor test structures were placed on a test chip. In addition to the varactors, a short structure and an open structure were also placed on the chip to facilitate the de-embedding procedure. All the devices were laid out in a standard 0.13μm CMOS process. For this experiment, two different varactors were characterized. Both varactors were made up of multiples of a unit varactor cell: one had 100 multiples (*m100* array) and the other had 60 multiples (*m60* array). The unit varactor cell had a width of 7.9μm and a gate length of 0.13μm. To reduce the effect of distributed gate resistance, contacts were used on both sides of the polysilicon gates. Therefore, the equivalent gate resistance was one-forth of the single gate resistance. Figure 3-7 illustrates the three test structures: (a) the short structure, (b) the open structure, and (c) the device under test (DUT), i.e., varactor array.

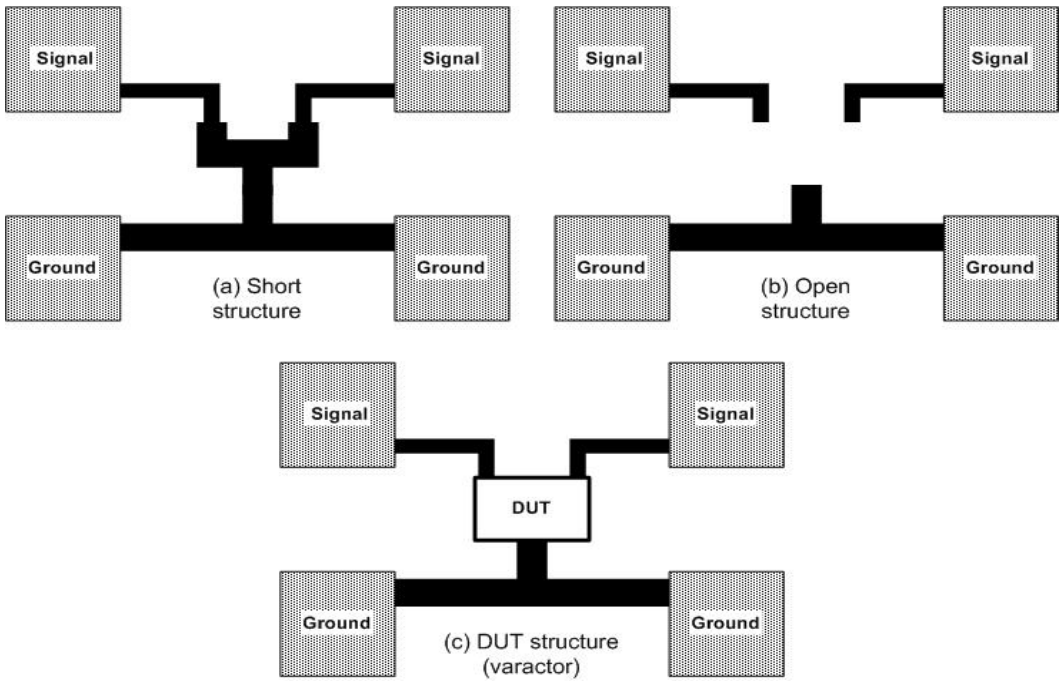


Figure 3-7. Top-view of the test structures: (a) short, (b) open, and (c) DUT (varactor array)

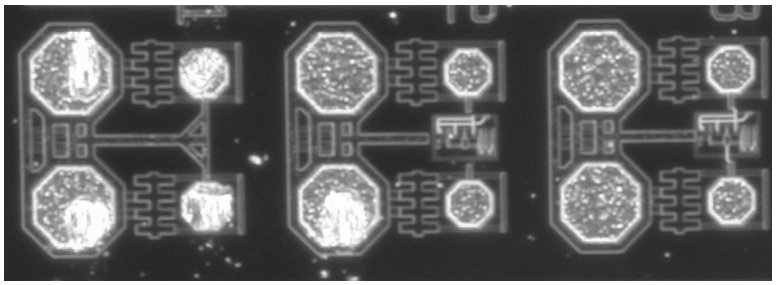


Figure 3-8. Micrograph of the test structures in 0.13µm CMOS, from left to right: short, open, and the varactor array (DUT)

Figure 3-8 shows the micrograph of some of the test structures on the die. These test structures from left to right are: short, open (including dummy varactors), and the varactor array (DUT).

3.3.1 De-embedding Technique

De-embedding is a technique required whenever dealing with characterization of small size devices at high frequencies. Traces and pads that connect the micro-size device to the measurement equipment, account for parasitics such as resistance, inductance and capacitance, which can affect the

reading on the instrument. Therefore, they should be accounted for and their parasitic values must be deducted from the actual measurement.

We used *Agilent 8510C* Vector Network Analyzer (VNA) for two-port RF characterization. S-parameters of the varactors, open, and short structures were measured from 100 MHz up to 6 GHz. The varactor voltage was varied in the range of -1.5V to 1.5V, with 100mV resolution.

Different de-embedding techniques are commonly used in the industry. In [64], a three-step de-embedding technique is described that employs two short structures, an open structure and a thru-structure instead of only short and open structures. A number of de-embedding techniques are discussed in [65]. We used two-step open/short de-embedding (OSD). Figure 3-9 shows the equivalent circuit representation of the parasitic series impedance and shunt admittance of interconnects and contact pads, respectively. Z_1 and Z_2 are the interconnection series impedances from the pads to the varactor. Y_1 and Y_2 are the equivalent shunt admittances between the signal and ground (pad capacitance, substrate capacitance, and resistance). We used signal-ground (SG or GS) probes. However, ground-signal-ground (GSG) probes are preferred, as they result in balanced electrical characteristics.

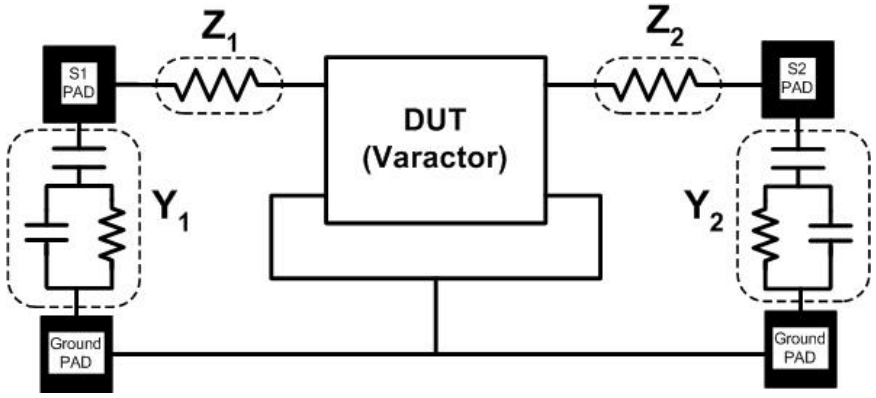


Figure 3-9. Equivalent lumped model of the varactor (DUT) with associated parasitics (open/short de-embedding)

Figure 3-10 illustrates a different lumped model for OSD, as presented in [65]. Here Z_1' and Z_2' are the impedances between the probe tips and the pads

on the CMOS chip as the probe calibration is performed on an impedance-standard-substrate (ISS). The ISS uses gold metallization instead of typical aluminium traces, and has a lower resistance.

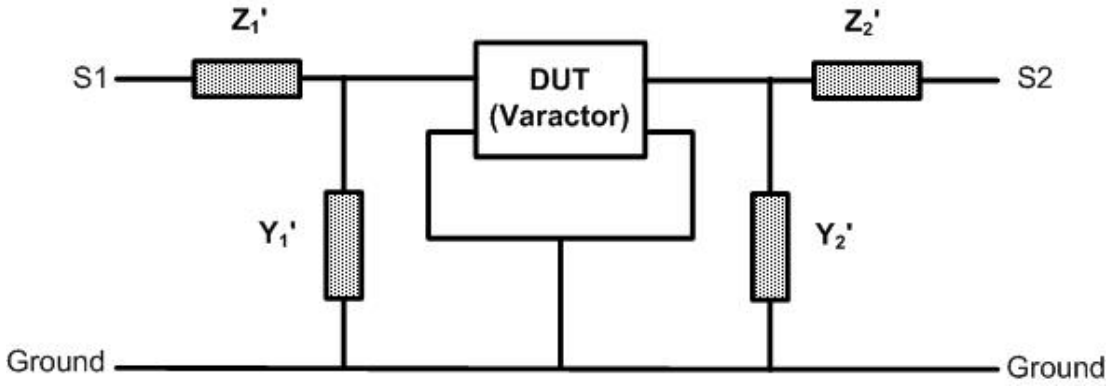


Figure 3-10. Alternative lumped model for open/short de-embedding (OSD)

Both approaches to de-embedding shown in Figure 3-9 and Figure 3-10 were carefully considered. However, we concluded that in our setup, interconnection impedances are dominant; therefore, the first model is appropriate here. Based on the parasitic lumped model of Figure 3-9, Y_1 and Y_2 are extracted from the following equations:

$$Y_1 = Y_{11,open} \tag{3-5}$$

$$Y_2 = Y_{22,open} \tag{3-6}$$

Z_1 and Z_2 can then be calculated using the following equations:

$$Z_1 = \frac{1}{Y_{11,short} - Y_1} \tag{3-7}$$

$$Z_2 = \frac{1}{Y_{22,short} - Y_2} \tag{3-8}$$

$Y_{ii,open}$ and $Y_{ii,short}$ (i=1,2) are the input and output admittances of the open and short structures, respectively.

3.3.2 Parameter Extraction Procedure

Figure 3-11 shows the circuit model of the AMOS varactor [57]. In this figure, C_S represents the main variable capacitance associated with the series capacitance of the gate oxide and the depletion region under the gate. C_f models the fringing capacitance related to the sidewalls of the gate, L_g is the inductance of the poly gate, R_s is the poly gate and channel resistance (the latter is voltage dependent), and R_{nwell} is the resistance of the n-well. C_{dep} is the depletion capacitance associated with the reversed-biased p-sub/n-well diode. R_{sub} and C_{sub} are the substrate parasitics, and R_{sd} is the resistance of the n+ regions (bulk electrode).

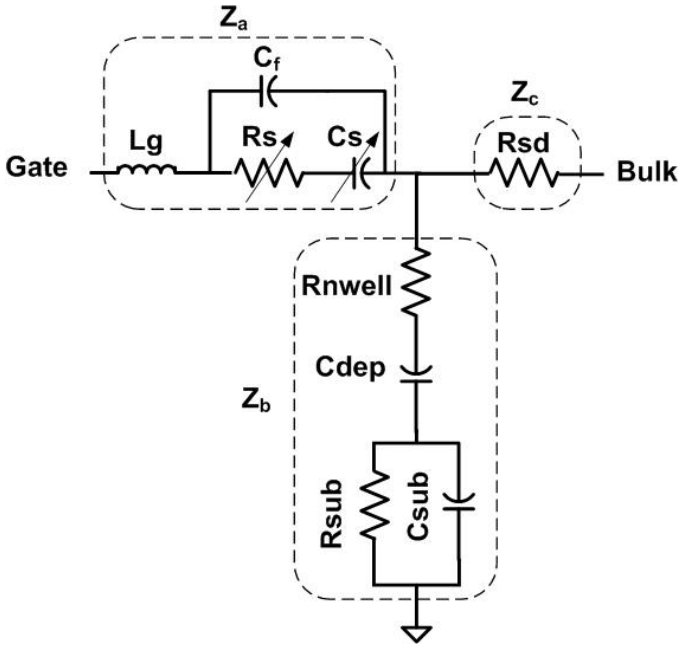


Figure 3-11. Equivalent lumped model of the integrated varactor

In order to verify the model shown in Figure 3-11, we need to characterize the de-embedded on-chip varactors (*m60* and *m100* arrays). Figure 3-12 shows the simplified form of Figure 3-11. In this figure, we have neglected R_{sd} (Z_c) as the impedance of the highly doped n+ regions is very small (less than 1Ω in these test structures).

Using the simplified circuit shown in Figure 3-12, we extract Z_a and Z_b from the following two equations:

$$Z_a = \frac{1}{Y_{11}} = Z_{11} - Z_{12} \tag{3-9}$$

$$Z_b = Z_{12} = Z_{21} = Z_{22} \tag{3-10}$$

where Z_{11}, Z_{12}, Z_{21}, and Z_{22} are the equivalent Z-parameters of the two-port varactor (Figure 3-12) and Y_{11} is the input admittance (gate-side) of the equivalent Y-parameters.

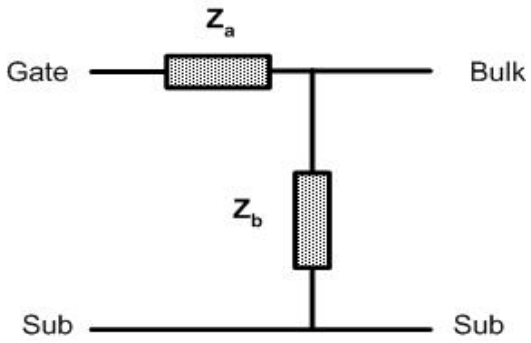


Figure 3-12. Simplified circuit of the two-port varactor in Figure 3-11

Z_a can be written as (neglecting C_f):

$$Z_a = R_S + \frac{1}{j\omega C_S} + j\omega L_g \tag{3-11}$$

Using (3-11) and employing numerical methods, we extracted the elements of Z_a for both varactors (*m60* and *m100* arrays). In (3-11), R_s is equal to the real part of Z_a (i.e., Re(Z_a)), and C_s is calculated as

$$C_S = \frac{1}{\omega^2 L_g - \omega \,\mathrm{Im}(Z_a)} \tag{3-12}$$

where L_g is also calculated at higher frequencies (e.g., 6 GHz) as follows:

$$L_g = \frac{1 + \omega C_{S-Low} \operatorname{Im}(Z_a)}{\omega^2 C_{S-Low}} \tag{3-13}$$

$C_{S\text{-}Low}$ is the capacitance calculated at lower frequencies (e.g., 100 MHz) in (3-12), where $\omega^2 L_g$ is insignificant and can be removed from the equation.

The quality factor (Q) of the varactor, which is the ratio of the stored energy to the dissipated energy (resistive loss) in the varactor, can also be approximated by [59]:

$$Q = \left| \frac{\operatorname{Im}(Z_a)}{\operatorname{Re}(Z_a)} \right| \tag{3-14}$$

The substrate effect (Z_b) is calculated using similar methods described for Z_a.

3.4 Varactor Modelling

As indicated earlier, modelling of tuning characteristics using (3-1) is fairly complicated. Not only do the varactor C-V characteristics have to be measured, but also the losses of the tank have to be determined to properly find the oscillation swing and hence the effective tank capacitance. An alternative approach would be to use the equivalent circuit representation of the varactor created from foundry-supplied transistor models and SPICE simulation to predict the tuning range. If a varactor is operating in the strong inversion mode, an nMOS transistor with tied source and drain can be used as a primitive model, since the varactor structure is the same as that of a MOS transistor. However, varactors that are working in the accumulation mode are usually laid out as shown in Figure 3-3. This structure inhibits the formation of the inversion layer. Wider tuning range and lower parasitic resistance are other advantages of this implementation [56]. However, the use of a plain transistor for modelling this varactor is not viable because the device does not resemble a transistor.

Figure 3-11 illustrates the model of this varactor constructed with passive circuit elements, and based on physical parameters [57]. As mentioned above, this model requires the implementation of non-straightforward equations (e.g., hyperbolic tangent) in the circuit-design environment and may involve other approximations as well. Moreover, the model cannot be easily scaled to future technologies. We have considered a number of different equivalent models reported in the literature.

We developed a new model that closely approximates the measured characteristics of the VCO [66]. This improved model is shown in Figure 3-13, and is a modified version of that proposed in [59]. The overlap capacitance C_{ov}, a voltage source V_{offset}, and a voltage source (dashed lines) between the bulk and drain/source have been added in the new model relative to [59]. Use of this offset voltage is very important in order to reduce the total error between the measured and model values.

To model the varactor capacitance, the equivalent circuit contains a voltage source V_{offset}, a capacitor C_{ov}, and a pMOS device with its source and drain connected to the ground with a high impedance (e.g., 1GΩ resistors) to resemble floating (non-existing) source and drain. The open circuit for the source/drain terminal is required to eliminate the inversion layer capacitance present in the channel of the pMOS device but absent in the varactor structure (see Figure 3-3). As a result, the gate to n-well (bulk) capacitance of the pMOS device represents the varactor capacitance properly with an additional channel length correction for LDD (Lightly Doped Source/Drain) regions.

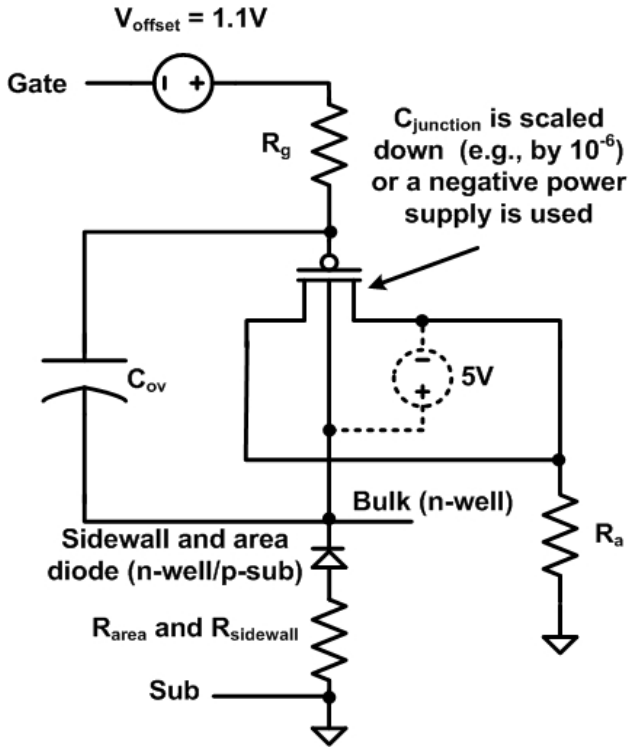


Figure 3-13. SPICE model developed for the varactor

Unfortunately, in this configuration, the gate-source and gate-drain overlap components of the varactor get neglected; as a result, they have to be added back by using the fixed capacitor, C_{ov}. V_{offset} represents a difference of the metal-semiconductor work function ϕ_{MS}, as the pMOS has p+ poly gate doping while the varactor has n+ poly doping due to their different source/drain diffusions. As doping levels in the polysilicon layer are typically close to degeneration, the V_{offset} is close to silicon bandgap (i.e., $E_g(T)/q$), which is about 1.1V at room temperature. Finally, the junction capacitance of the pMOS transistor has to be scaled down, as it is not present in the AMOS varactor. This can be done either by changing the scaling factor inside the SPICE model or adding a negative power supply between source/drain and the bulk (e.g., -5V) to enlarge the depletion area and reduce the junction capacitance.

In terms of sensitivity of the model components to PVT, R_a is insensitive. It is an arbitrary large resistance used for making the p+ regions floating. The negative supply voltage is also insensitive as it can always be replaced by the

largest possible voltage supported by the technology. The 1.1V offset voltage is sensitive to temperature. The C_{OV}, gate resistance, n-well diode and substrate resistance (e.g., R_{area} and $R_{sidewall}$) are layout dependent. Their exact value depends on the arrangement of unit cells and dummy cells.

3.5 Experimental and Simulation Results

We used different techniques and technologies, to verify our model. First, using our varactor and LC-VCO circuits designed in a standard 0.13μm CMOS process, we verified our model both directly by comparing the measured and simulated varactor values, and indirectly by comparing the tuning curves of the LC-VCOs. In a second approach, we switched to a mature standard 0.18μm CMOS process. This design kit has been out for several years and foundries have updated the models many times. Therefore, the existing varactor model provided by foundries has been used by designers many times and could be used as a valid source for comparison. In this process, we again designed an LC-VCO once with the foundry mathematical model (*hyperbolic tangent function*) and once using our own model. Also we did a direct comparison between a sample of the foundry varactor C-V curve, and the same varactor using our own model.

Section 3.5.1 and Section 3.5.2 discuss these results in a 0.13μm CMOS and a 0.18μm CMOS process, respectively.

3.5.1 Experimental Results in a Standard 0.13μm CMOS Process

Three different VCO structures were fabricated in a standard 0.13μm CMOS process with a 1.2V power supply. No special mixed-signal process option has been used. The micrograph of one of the VCOs is shown in Figure 3-14. Varactors are implemented as n+ accumulation-mode MOS capacitors with no additional mask required. Thus, the obtained designs are portable to various CMOS processes of different foundries.

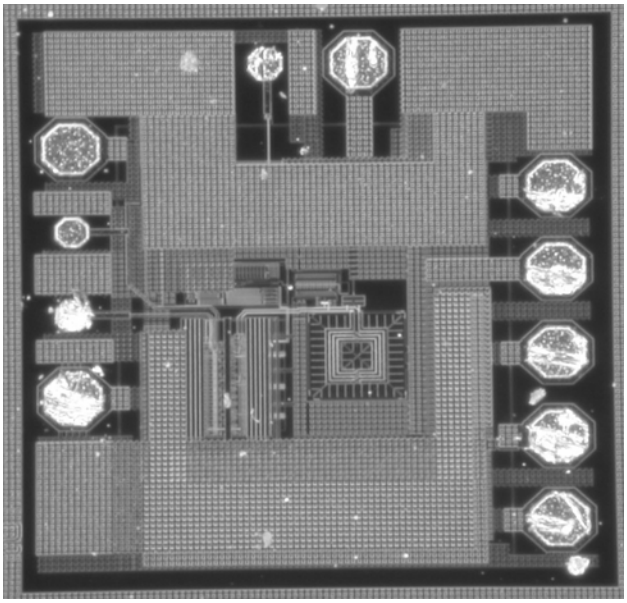


Figure 3-14. Micrograph of a VCO test structure in 0.13μm CMOS

The three implementations have similar architectures as those depicted in Figure 2-8b and Figure 2-8c, but with different varactor values. The tail current in all three versions is 1.5mA; hence the DC power consumption is 1.8mW, excluding output driver and biasing circuits. The structure that incorporates an nMOS tail current source (Figure 2-8c), exhibits higher sensitivity to power supply noise, while that with a pMOS tail current source (Figure 2-8b) has the best power supply rejection ratio (PSRR), due to the extra isolation from the power supply by the current source.

In addition to the three VCO circuits, a biasing circuit and an output driver stage were added to drive an external 50Ω load. Individual varactor and inductor test structures were also included for S-parameter measurements. Open and short de-embedding structures were added for proper extraction of the equivalent circuit, as explained earlier in Section 3.3.1.

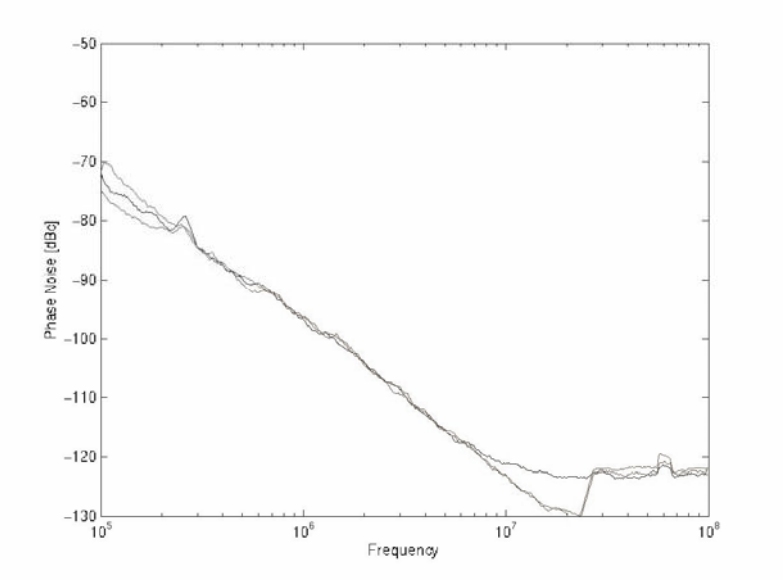


Figure 3-15. Measured phase noise of the VCO with pMOS tail current (Figure 2-8b) at three different supply voltages (1.2V, and 1.2V ± 5%)

The phase noise of all three VCOs was measured using a spectrum analyzer equipped with a phase noise module. Figure 3-15 compares the phase noise of the VCO with the pMOS tail current shown in Figure 2-8b, for three different supply voltages (1.2V, and 1.2V ± 5%) at the nominal temperature with the control voltage set to the mid-point (600mV). The phase noise at 1 MHz offset from the carrier for the 3 different supply voltages was -95.8/-95.5/-95.5 dBc/Hz, respectively.

The tuning characteristics were simulated using the varactor model described in Section 3.4. Excellent agreement between the model and the measurement was obtained, as shown in Figure 3-16. The results in Figure 3-16 are shown for a VCO test structure with a greater number of varactor fingers (varactor with 100 fingers, width of 7.9μm and length of 0.13 μm) and hence a lower centre frequency, compared with the results shown in Figure 3-5. The disagreement between the measured and simulated points for the whole tuning range is calculated to be about 0.035GHz (i.e., rms error) or approximately 0.71%. This number also includes lab equipment and measurement errors.

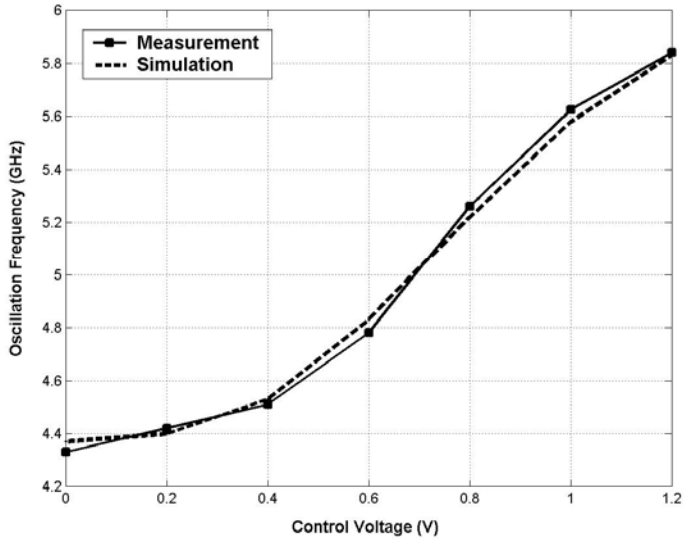


Figure 3-16. Measured vs. modeled tuning characteristics (new sub-circuit model)

We also verified the model directly using the measured results of a de-embedded varactor (i.e., with 60 fingers, width of 7.9μm and length of 0.13 μm). Figure 3-17 shows the result of this comparison. The rms error is calculated to be around 0.02pF or 3.1%, and includes the error related to measurement equipment.

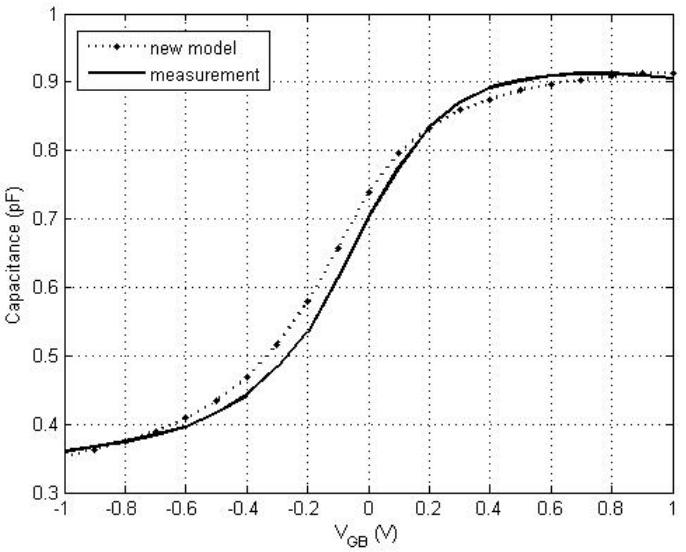


Figure 3-17. Comparison between the model and measured results for a varactor (m=60, width=7.9μm, and length=0.13μm) in a 0.13μm CMOS process

Note that neither of these devices (varactor with 60 fingers and 100 fingers), could be modeled using the foundry models as they are designed for the minimum finger length (i.e., 0.13μm). The foundry models are for more general-purpose designs and only cover a few samples with the finger length of 0.4μm, which is not suitable for aggressive designs. The second advantage of our model, is its relatively fast simulation time, as opposed to current mathematical models that are based on curve-fitting techniques.

3.5.2 Simulation Results in a Standard 0.18μm CMOS Process

To verify that this new model can easily be ported to other technologies, we decided to use a mature process (i.e., 0.18μm CMOS) and compare our model with the foundry model. In order to do that, we picked one of the foundry-provided varactor structures that operates in a range of 0.44pF to 1.24pF. This varactor has 100 fingers with width of 2.5μm and length of 0.5μm. In our design kit, 0.5μm is the only length available to designers. However, the minimum length supported by the process is 0.18μm. We compared the foundry varactor, which is defined using math function with our own sub-circuit model: the error was slightly less than 5%. Since the error was mostly around the variable part of the C-V curve, we noticed that it could be fixed by a slight horizontal shift on the x-axis. We therefore reduced the offset voltage to 1V from 1.1V. This time, the two graphs were in good agreement with an rms error of 0.0148pF, or about 1.68%. The result of this comparison are depicted in Figure 3-18. The major disagreement is on the flat part of the two curves (lower end with minimum capacitance). However, in most varactor applications, designers incorporate varactors to benefit from their variable range (i.e., varactor is biased at about the mid-point of the variable range). Here, the two curves show very good agreement in the variable range.

While we still cannot precisely account for the error in the offset voltage, we emphasize that the silicon bandgap voltage is a topic of active research. Recent studies show that experimental observations and theoretical calculations for the gap in silicon nanocrystalline are in substantial disagreement, which is

especially pronounced at smaller sizes. Theoretical calculations seem to overestimate this value [67].

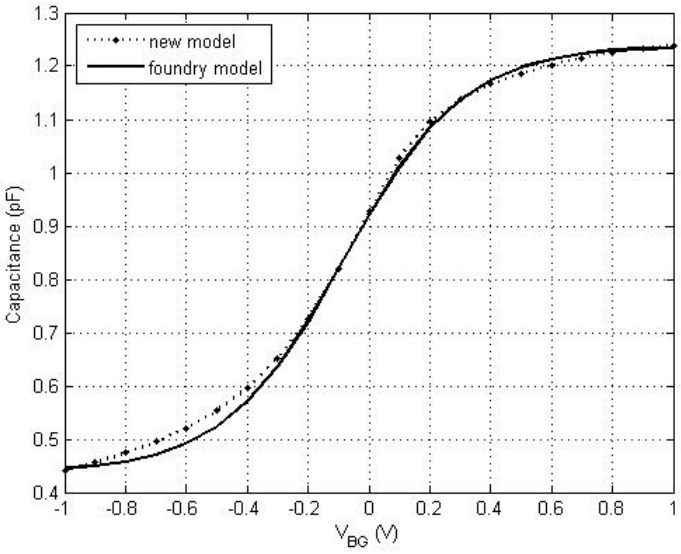


Figure 3-18. Comparison between the foundry varactor model and our model in a standard 0.18µm CMOS process.

Using the adjusted offset voltage of 1V, we used the above varactor models to design two LC-VCOs for operation in the range of about 5GHz to 6.5 GHz. The circuit architectures are the same as the LC-VCO circuit shown in Figure 2-7. However, one was designed with the foundry model and the second using our sub-circuit model. We simulated the two circuits by varying the control voltage from 0.9V to 2.7V in order to cover the entire tuning range of the varactor. The two tuning curves are depicted in Figure 3-19, and are in good agreement with an rms error of about 0.0313 GHz, or approximately 0.53%.

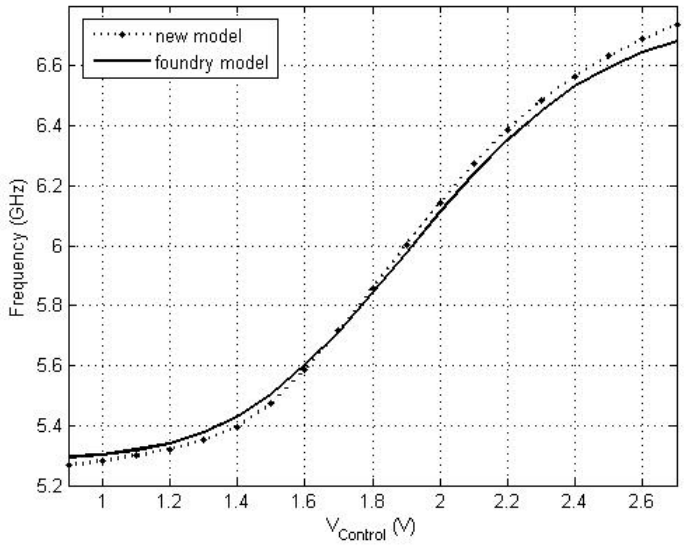


Figure 3-19. Comparison of the tuning curves for the two LC-VCO designed in a standard 0.18µm CMOS process using the foundry varactor model and our sub-circuit model.

3.6 Conclusion

In this chapter, the importance of the VCO output signal in the C-V characteristics and tuning curves was pointed out and described using some practical examples. We established that more detailed modelling is required to accurately predict the tuning characteristics of LC-VCOs from simulations. Further study of this issue is postponed to Chapter 5, where we show both mathematically and using simulations that the change in the frequency of LC-VCO is due to changes in the voltage amplitude and shape.

Varactors are the main tuning component of LC-VCOs, and are normally used for fine-tuning. As one of the elements of the LC tank, they play an important role in determining the quality factor of the tank and hence, the phase noise performance and tuning capability of LC-VCOs.

In this chapter, we detailed the new varactor model we created using sub-circuit components and, particularly, MOSFETs and some passive components. The model described the accumulation-mode nMOS varactor. Some of the key

advantages of this model over current foundry-provided models include the following [55]:

- Overcomes the simulation convergence problems and/or long simulation times associated with foundry models particularly in leading-edge technologies such as 90nm or shorter gate length CMOS processes.
- Foundry-provided models are limited to a few samples provided for general-purpose designs for mid-frequency ranges.
- Foundry-provided models are not easily scalable to other technologies. Besides, they normally take few years to develop and mature.
- Foundry models are based on curve fitting to the measurement results for a few particular-size test structures. Therefore, for a different size structure they would not be as accurate.
- In the fine-gate-length processes with gate leakage problem (e.g., 90nm CMOS), the leakage current of the varactor is not considered in the foundry-provided model. However, by using our sub-circuit model, which incorporates a MOS transistor as the main component of the varactor, we automatically consider the leakage problem.
- Current foundry models are not suitable for aggressive high-frequency RF designs where designers have to use minimum length varactors.

We verified our sub-circuit model using different approaches by taking direct and indirect measurement of varactor devices and LC-VCO tuning curves in a standard 0.13μm CMOS process. The comparison results were in good agreement. To show the scalability of the model, we used a different process (0.18 μm CMOS) which has been matured over a number of years and has accurate models. Comparison of foundry models with the varactor model and circuits designed using the sub-circuit model further verifies the accuracy of the model.

The model still has some limitations. For example, the 1.1V offset voltage used to account for the silicon bandgap voltage difference between p+ and n+

material is temperature dependent and requires more accurate modeling. The components representing the substrate parasitics (i.e., diode and resistors) are layout dependent and their exact value depends on the layout structure. The same thing applies to the overlap capacitance, C_{OV}. The process variations can be different for nMOS varactor and its equivalent pMOS sub-circuit model used in the simulation, which may cause some errors in the final results. These limitations can be the subject of future work on AMOS varactor modeling.

Chapter 4

High-Speed Tuneable Narrowband CMOS Driver

One of the challenges in the design of high frequency (multi-GHz) circuits is the design of amplifiers/drivers with sufficient gain and bandwidth. This subject has been the topic of research since early 1930s [85]. These driver circuits prove useful when the output of one stage is not capable of directly driving the subsequent circuit. This situation occurs mainly because of the nodal capacitance between the two blocks at high frequencies (Figure 4-1).

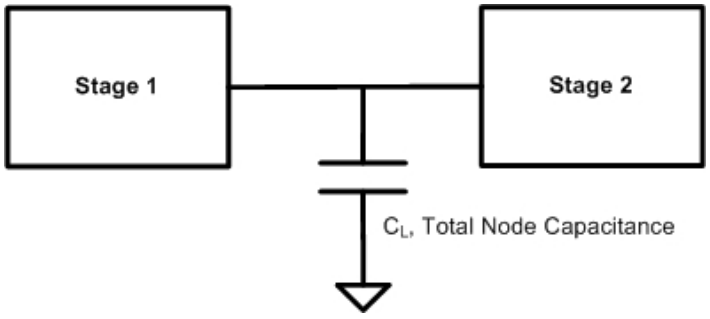


Figure 4-1. Two cascaded high-speed circuits with total node capacitance C_L in between.

A common solution practised in the past and still used in some leading-edge high-speed applications is to design a separate chip dedicated to the high-speed analog and RF blocks. This chip is fabricated in technologies such as III-V, silicon bipolar, or SiGe BiCMOS, relying on their naturally higher speed and lower noise characteristics [68-70]. The rest of the system is then designed on a different chip using a low-cost CMOS technology, which is the mainstream IC process for digital systems. However, there is an industry-wide trend toward implementing both analog/RF and digital circuits on a single chip using a

standard low-cost CMOS process, i.e., system-on-a-chip (SoC). This would result in a shorter time-to-market. It also allows savings on packaging as well as power consumption due to the elimination of power-hungry output stages between the chips. Due to Moore's Law and aggressive scaling of the CMOS process, achieving higher speeds is becoming more feasible. For instance, in a typical 0.18μm CMOS technology, the transition frequency (f_T) of an nMOS transistor with overdrive voltage of 500 mV is approximately 50 GHz [71]. While higher transit frequencies are achievable in more advanced CMOS technologies, a robust CMOS circuit is usually designed to operate at a fraction (e.g., one-tenth or lower) of f_T, which creates many challenges in the design of wideband amplifiers. The large DC gain of a conventional multi-stage CMOS amplifier with resistive load tends to drop sharply at multi-gigahertz frequencies. In addition, various tradeoffs between design specifications (e.g., noise, power consumption, bandwidth and output swing) make many circuit architectures impractical for high-frequency applications. A reason for the sudden drop of the gain in multi-gigahertz frequency range is the effect of the parasitic capacitances of MOSFET transistors and of interconnects. These parasitics are not negligible at high frequencies. They create a short resistive path at high frequencies between the input and the output of the transistor.

Over time, designers have proposed different solutions based on the design constraints imposed by different load and drive conditions (e.g., amplifiers for wireline applications versus wireless applications [72] or other specific applications discussed hereafter) to partially compensate for the bandwidth loss while trying to maintain other qualities of the circuit unchanged. This chapter proposes a solution for the case, where the driving signal is periodic with a variable frequency over a predefined range e.g., output clock of a voltage-controlled oscillator (VCO) in a clock and data recovery (CDR) system. In many such applications, the clock generators are not capable of driving the next block either directly or with the use of conventional resistive-load drivers due to their insufficient drive capability and limited bandwidth.

The next section reviews some of the well-known techniques currently used for bandwidth extension and high-frequency amplification. Section 4.2 describes our proposed solution, which we introduce in the context of a design example with applications in CDR systems. Simulation results are explained in Section 4.3. The chapter is summarized and concluded in Section 4.4.

4.1 Background

Since the 1930s, inductors have been widely used for bandwidth extension techniques e.g., *shunt* and *series peaking* [72]. Shunt peaking is a common method for bandwidth extension that was originally used in vacuum tube circuits in the 1940s [73]. The concept is as follows: assume a single-stage amplifier like the common-source stage illustrated in Figure 4-2a, which has one dominant pole at *1/RC*. This amplifier is used extensively in a single-ended or differential form or (sometimes cascaded in multiple stages) to achieve high gains or high driving capability. In order to extend the bandwidth, an inductor is inserted in series with the resistor (Figure 4-2b) to resonate with the load capacitance. This inductor generates a zero at *R/L* in the numerator (as well as a second pole in the denominator) of the voltage-gain transfer function (TF). Ideally, this zero should cancel the pole at *1/RC* and extend the -3 dB bandwidth to the second dominant pole of the TF. However, the addition of the inductor changes the dynamics of the system to that of a second-order system, or subsequently changes the location of the original pole. The denominator would then be $1+j\omega RC-\omega^2 LC$ instead of $1+j\omega RC$. Depending on the ratio of the zero to the original pole of the first-order system ($m=L/R^2C$), the frequency response exhibits different characteristics. Figure 4-3 shows three different responses for *m=0* (no shunt peaking)*, 0.41* (maximally flat with 72% bandwidth extension) and *0.71* (maximum bandwidth with 1.5 dB of peaking and 84% bandwidth extension) [73].

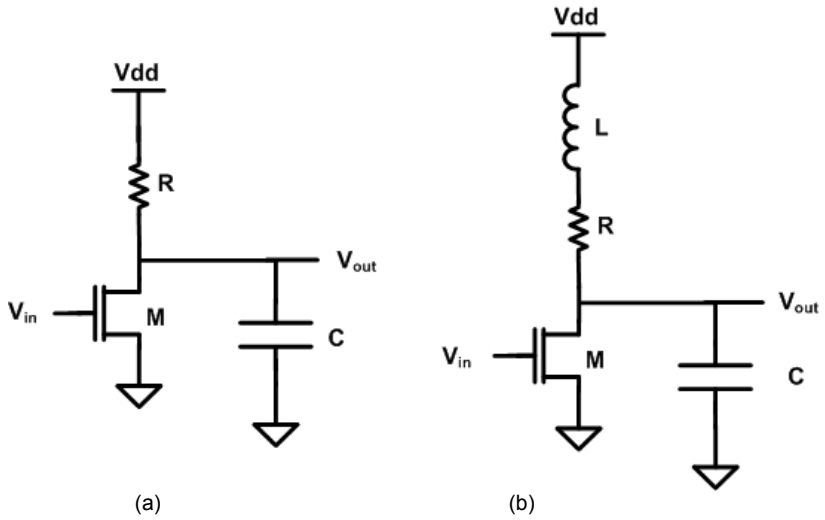


Figure 4-2. (a) A common-source amplifier with a capacitive load, (b) Same amplifier with shunt peaking

The peaking could be improved by adding a capacitor in parallel with the inductor. This method is called *bridged-shunt peaking*. This shunt capacitance is already present in on-chip inductors due to the inherent fringing parasitic capacitances of the metal wires [72].

Another technique is based on capacitance splitting and the ratio of the drain capacitance to the load capacitance. This technique is capable of extending the bandwidth more than four times [72]. Figure 4-4a shows the same common-source amplifier but with split load capacitance (drain parasitics and load capacitance). An inductor is inserted between the two capacitors as shown in Figure 4-4b, which creates *Series Peaking* [72].

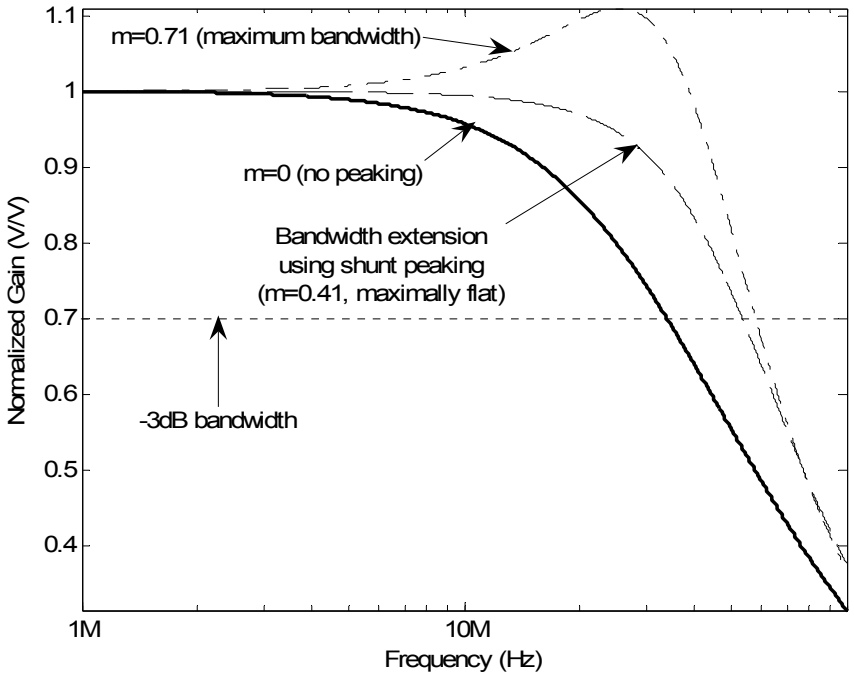


Figure 4-3. Bandwidth extension using shunt peaking technique: depending on the ratio of zero to the pole of the original first order system (m), there could be different frequency responses

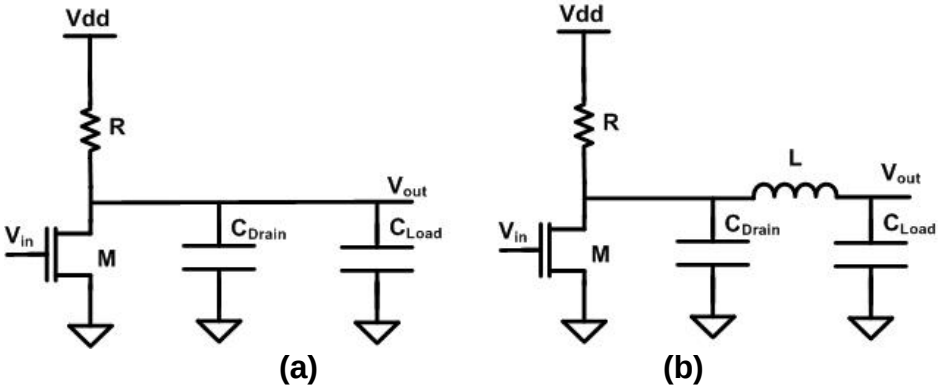


Figure 4-4. (a) A common-source amplifier with split drain parasitic and load capacitance, (b) Same amplifier with series-peaking inductance between the two capacitors.

Figure 4-5 illustrates bandwidth extension using series peaking. Depending on the value of k_c, the ratio of the drain capacitance to total node capacitance ($k_c = C_{Drain} / (C_{Drain} + C_{Load})$) and m ($m=L/R^2C$), different bandwidth extension and peaking values can be achieved.

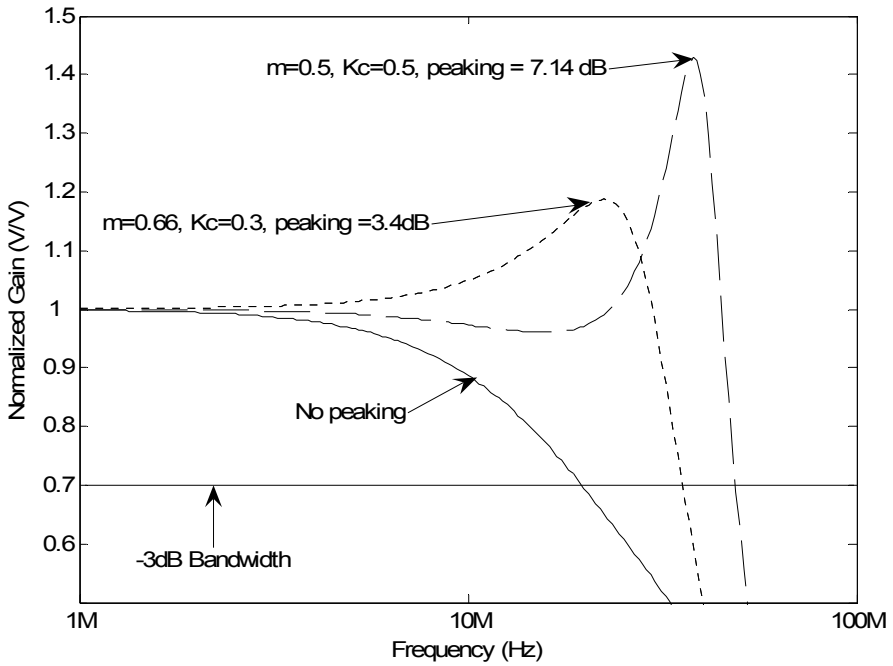


Figure 4-5. Bandwidth extension using series peaking technique

Table 4-1 summarizes different examples resulting from different k_c and m values. For instance, with equal capacitors and m set to *0.5*, a bandwidth extension ratio of up to 2.5 can be achieved [72].

Table 4-1. Summary of bandwidth extension using the series-peaking technique

$m = \frac{L}{R^2 C_{Total}}$	$k_C = \frac{C_{Drain}}{C_{Total}}$	**Bandwidth Extension Ratio**
0	0	1
0.50	0.5	2.5
0.66	0.3	1.8

An alternative approach to achieving higher gain and swing at high frequencies is to use a tuned load where at the frequency of interest, the load inductance resonates with the load capacitance: this is called a *tuned amplifier*. The gain-bandwidth product (GBP) is roughly independent of the centre frequency. The -3 dB bandwidth is *1/RC* and the gain at resonance is $g_m R$, which yields the constant product of g_m/C [74]. Figure 4-6 shows two examples of such

circuits. Both circuits resonate around 5 GHz; however, one has low quality factor (Q) inductance and the other has high-Q inductance (i.e., relative to each other). The input clock frequency is intended to be at or very close to the resonance frequency. The circuit provides a large output swing given the input at or near the frequency of interest (5 GHz). Although this type of driver could generate large swings at the resonance frequency, the gain drops abruptly as the operating frequency deviates from the resonance frequency (Figure 4-6). Therefore, the design challenge would still be to achieve the desired gain over a relatively large bandwidth at high frequencies. This could be alleviated to some extent through the use of low-Q inductors (e.g. on-chip multi-metal/stacked inductors), which provide wider bandwidth around the resonance frequency. The disadvantage is that lower Q results in a lower peak at the resonance frequency and consequently a lower overall gain.

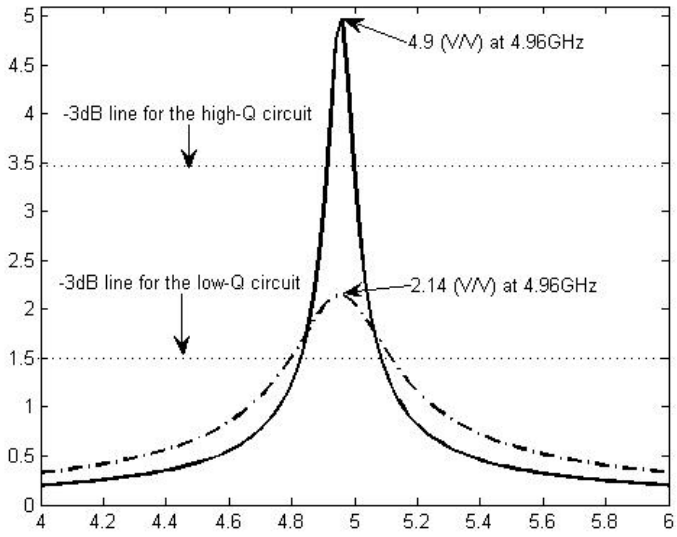


Figure 4-6. Using a tuned load, amplification occurs at the desired frequency but it is limited to that frequency only.

4.2 Proposed Solution

In some applications such as clock synthesizers or data recovery systems, adequate gain is required at the buffered output of the clock over a fairly wide frequency range (i.e., the tuning range of the oscillator). The buffer is used to

drive the relatively large capacitive load of the next stage (e.g., high-speed divider in a synthesizer PLL, or input stage of up- and down-converter mixers in a radio). However, at any given data-rate, the output only oscillates at or around a fixed frequency, and no amplification is required at other frequencies. In other words, the power/gain could be concentrated around the frequency tone of interest rather than spreading over a large band to amplify the noise or unwanted signals all over the spectrum. These applications suggest the use of tuneable amplifiers.

Figure 4-7 proposes a solution for the problem posed in Figure 4-1 by adding a tuneable amplifier in between the two stages. Here, C_L accounts for the total node capacitance. It includes drain parasitics, input capacitance of the next stage, interconnect parasitics, and a variable capacitor as the tuning component (e.g., an accumulation-mode MOS (AMOS) varactor [47, 56]). This load could be on the order of several hundred femto farads in deep sub-micron technologies (e.g., in a 0.18μm or finer gate length CMOS process). In this work, an AMOS varactor and inductive loads are used to design a high-frequency tuneable driver/amplifier. The AMOS varactor together with the rest of the nodal capacitance resonates with the driver's inductive load at the frequency of interest. For proper operation, this resonance frequency is adjusted along with the frequency of the input signal through the varactor control signal. A similar circuit has been used in [34] where instead of a varactor, a bank of fixed capacitors is used. In this case, the centre frequency of the driver is tuned using an array of binary weighted metal-to-metal capacitors. These capacitors are not voltage dependent, however, due to their discrete values, the resonant frequency of the buffer cannot be tuned continuously.

At any given time, the instantaneous resonance frequency of an LC circuit is given by (4-1). Note that this equation is not accurate as unlike [34] varactor is voltage dependent. This subject will be elaborated upon in Chapter 5.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{4-1}$$

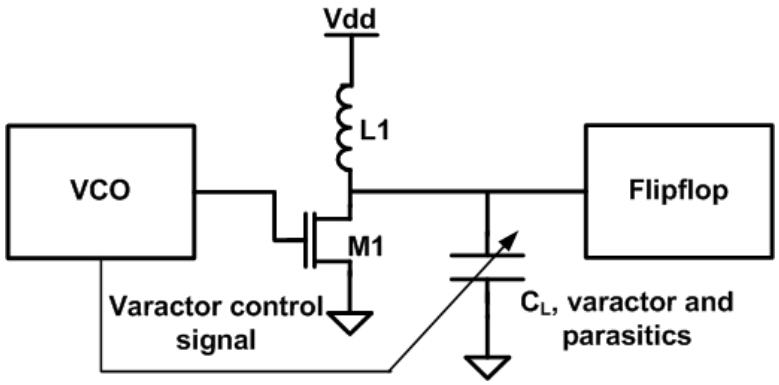


Figure 4-7. Two cascaded high-speed circuits with the proposed resonator stage in between.

This technique is explained in the context of a d*esign example* in the next subsection. The proposed amplifier exhibits sufficient gain at multi-gigahertz frequencies. Furthermore, the design ensures that the resonance frequency of the output is automatically adjusted with that of the input. The technique is introduced in the context of a driver stage for a clock signal generated by a VCO to drive a high-speed flip-flop circuit that operates in the 5-6 GHz range. This idea could be extended to other similar applications.

4.2.1 Design Example

A differential LC-VCO is used to provide differential clock signals for the flip-flop circuit of a 40 Gb/s clock and data recovery system designed in a standard 0.18μm CMOS technology. In the 1/8th rate architecture introduced in [75], the VCO operates around 5 GHz and has differential outputs (Clk, Clk_Bar) that are to drive the flip-flop clock inputs. However, the VCO followed by a differential resistive-load buffer is not able to drive the large capacitive load imposed by the next stages differential inputs, unless multiple stages with excessive power consumption are used. In addition, the driver has to be able to drive the signal over the VCO's entire tuning range. These limitations complicate the design of the driver stage and suggest the use of the proposed tuneable amplifier.

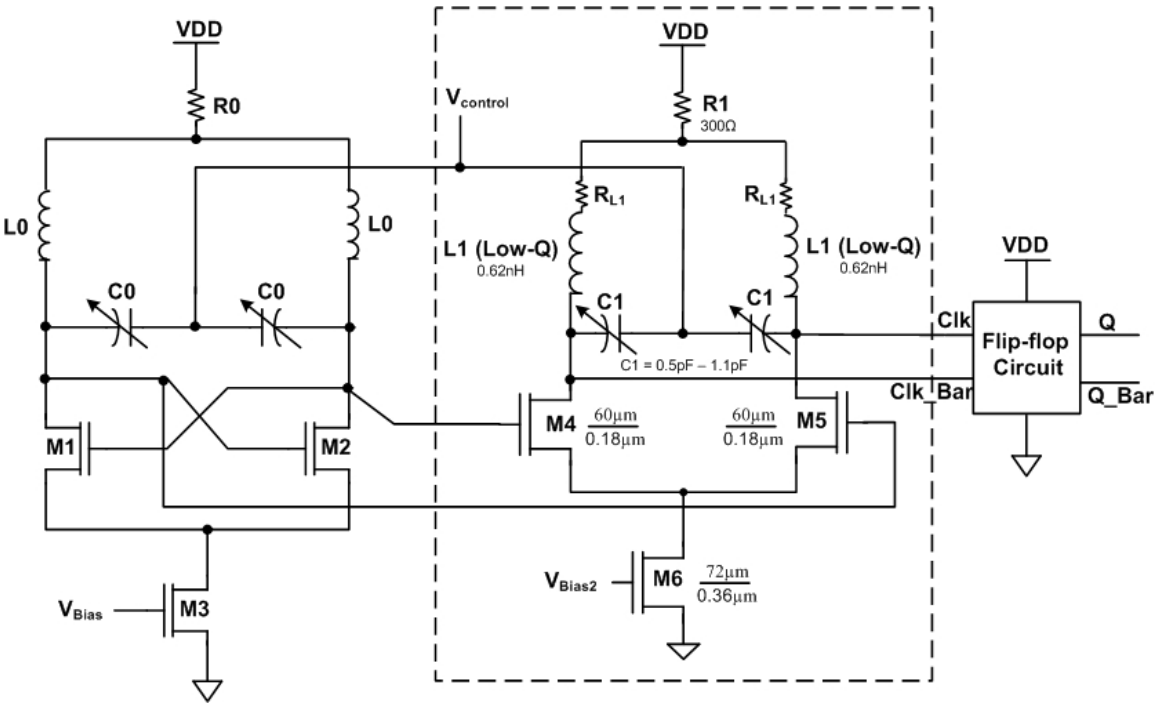


Figure 4-8. Voltage controlled oscillator (left) followed by the tuneable inductive driver stage (dashed box). There is also one-stage resistive buffer block between VCO and inductive driver to create isolation (not shown here)

Figure 4-8 shows an LC-VCO circuit followed by a differential inductive driver, shown in the dashed box, which drives the flip-flop clock inputs (e.g., equivalent to 1pF capacitive load). In practice, there is also a small resistively loaded amplifier between the VCO and the inductive driver. This amplifier is not shown in the figure but it provides one level of buffering between the sensitive VCO circuit and the rest of the system. The gain of this resistive amplifier is enough to drive the capacitance of the driver stage and cannot be directly used for driving high capacitive load.

The inductor of the driver stage resonates with the combined capacitance of the node, including the parasitic capacitances of the transistors, interconnects and the varactor, around the VCO's centre frequency. The proximity of the driver's peak frequency can be calculated according to (4-1), where C is made up of two components: a fixed part (interconnects and transistors) and a variable part (i.e., the voltage-dependent varactor capacitance). This formulation is shown in (4-2), and will be discussed in detail in Chapter 5.

$$f = \frac{1}{2\pi\sqrt{L\,(C_{fixed} + C_{\mathrm{var}}(V))}}\,. \tag{4-2}$$

Resistors R0 and R1 have been added to shift down the output common-mode voltage, in order to take advantage of the full tuning range of varactors C0 and C1. Depending on the load size (i.e., size and number of flip-flops, as well as layout parasitics), the value of C1 is chosen so that the total capacitance resonates with the inductor in the vicinity of the VCO's operating frequency. The inductor is a differential centre-tapped 3-turn octagonal structure with an inductance of about 2×0.62nH. The inner diameter of the inductor is 80μm. The capacitance of the varactor varies between 0.5pF to 1.1pF, corresponding to maximum and minimum control voltages, respectively.

4.3 Simulation Results

The VCO is simulated for different process, supply voltage and temperature corners (PVT). Two extreme corners of the VCO, which would limit the tuning range, are slow nMOS, slow pMOS at 125°C with 2.0V supply and fast nMOS, fast pMOS at -40°C with 2.0V supply. The tuning ranges for four corners, together with the typical corner, are illustrated in Figure 4-9. The overall tuning range guaranteed over PVT is 4.85 GHz to 5.75 GHz. Each of the driver's differential outputs is connected to a fixed capacitor of 1pF to model a large capacitive load (e.g., multiple flip-flop clock inputs in the case of high-speed divider circuit).

Since the circuits were designed in a relatively mature technology (i.e., CMOS 0.18μm) and the model for the passive components such as the inductor and the varactor were obtained from the foundry-measured results, the post layout simulation is very reliable.

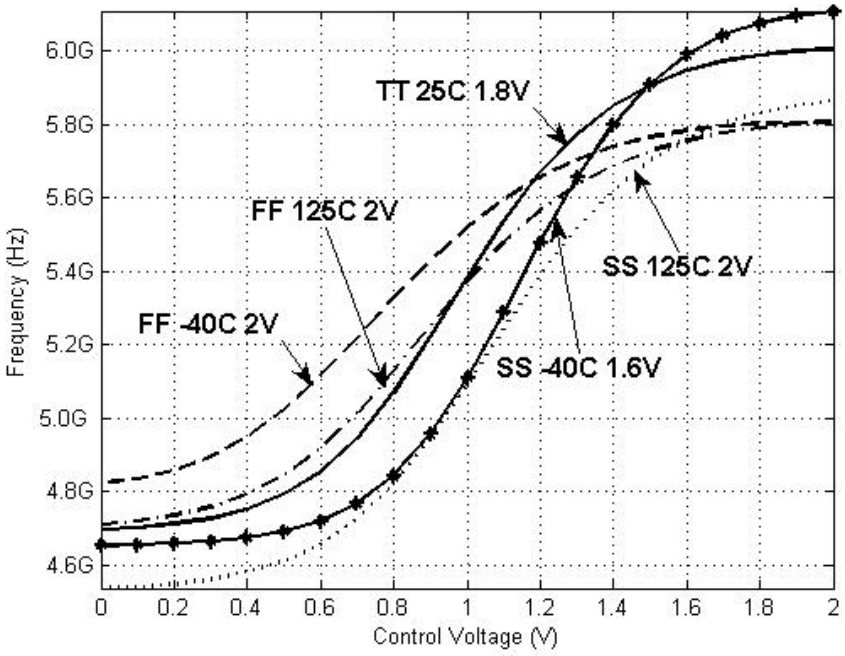


Figure 4-9. VCO operating frequency vs. control voltage simulated for extreme process corners, temperature and supply values (PVT).

Figure 4-10 illustrates a 3D plot of the frequency response of the inductive driver versus the control voltage. The 3D vertical plane that cuts through the Gaussian-shaped frequency response represents the VCO tuning range. The intersection of this plane and the frequency response surface shows the actual gain of the driver. This intersection is not always at the peak but closely tracks the changes of the VCO frequency.

The goal here is to drive a large capacitive load. High voltage gain is not the primary goal as long as the voltage amplitude is sufficiently large to switch the gate of the next stage (e.g., flipflop inputs). Due to this reason, use of low-Q inductor is beneficial as it results in an amplifier with a larger bandwidth. Therefore, if the tank resonance is not exactly the same as the VCO frequency, the amplifier bandwidth is large enough to cover the VCO resonance frequency. This concept is illustrated in Figure 4-6 by using a high-Q and low-Q inductor for a tuned amplifier.

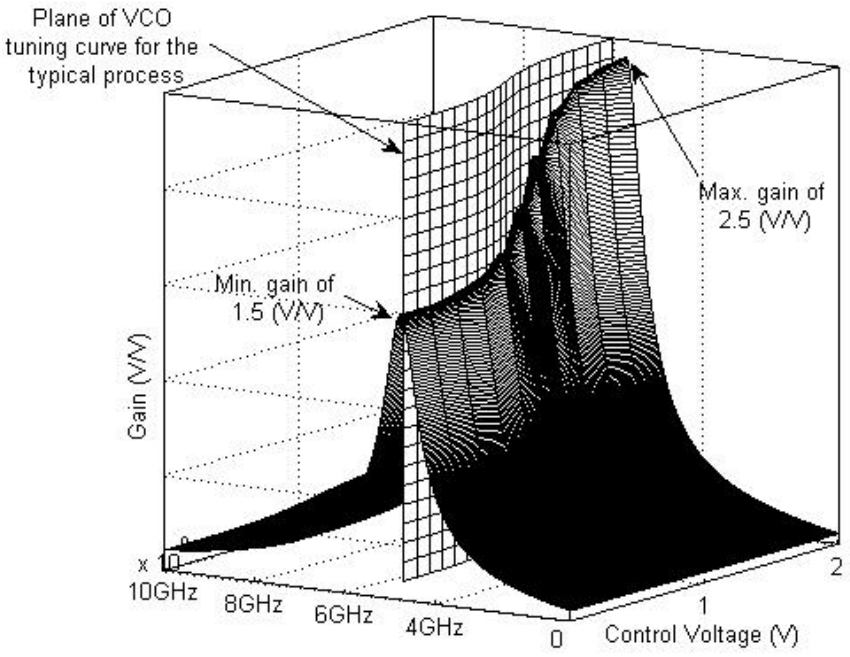


Figure 4-10. 3D illustration of buffer gain vs. control voltage. The VCO tuning curve has been illustrated for the typical process. The peaks of buffer gain closely track the changes in VCO frequency.

Table 4-2 shows the driver's voltage gain (large-signal gain with 1pF capacitive load) at five voltages for the typical as well as the two VCO extreme corners. The gain is roughly constant around 1.5 V/V for the typical corner (25°C, 1.8V) while it is higher (average 2.9 V/V) for the fast -40°C 2V corner and lower (average of around 1 V/V) for the slow 125°C 2V corner. For the typical corner, the power consumption of the driver is 5.1mW at 5 GHz. While the gain varies for extreme corners, it is still sufficient to drive the next stage with acceptable switching time. Simulations are conducted using RF models of non-ideal varactors and inductors provided by the foundry. The varactor is modelled using a hyperbolic tangent capacitance function and parasitic RLC and diode elements.

Table 4-2. Resonance frequency and gain at five voltages on the control line for typical and two extreme corners

Control Voltage	Peaking Frequency/ Gain (V/V)		
	Slow, 125°C, 2.0V	***Typical, 25°C, 1.8V***	***Fast, -40°C, 2.0V***
300mV	4.56GHz / 0.95	4.73GHz / 1.49	4.90GHz / 2.4
600mV	4.66GHz / 1.03	4.86GHz / 1.55	5.12GHz / 2.4
900mV	4.95GHz / 1.11	5.22GHz/ 1.51	5.43GHz / 2.9
1.2V	5.39GHz / 1.06	5.67GHz / 1.54	5.66GHz / 3.3
1.50V	5.70GHz / 1.23	5.91GHz/ 1.71	5.77GHz / 3.4

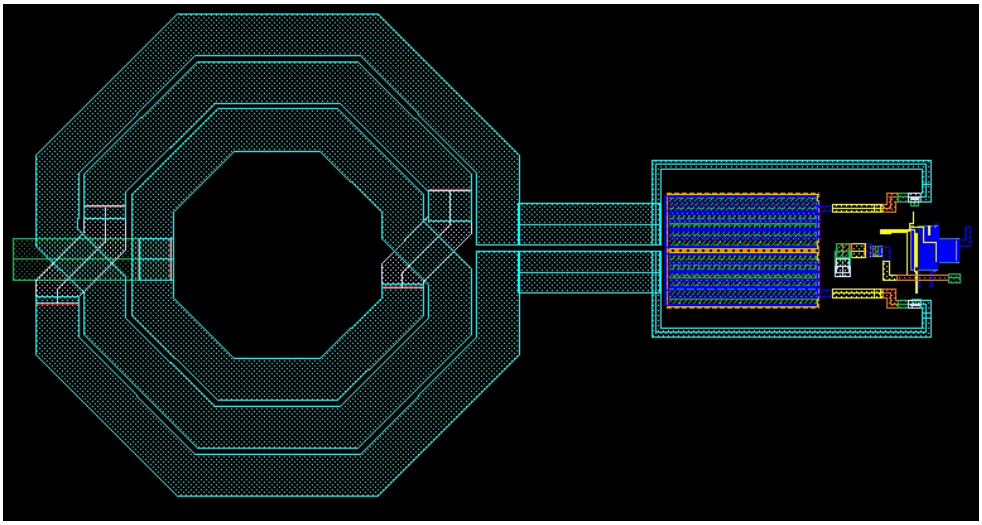


Figure 4-11. Layout of the tuneable amplifier in a standard 0.18µm CMOS process with a differential Inductor (N=3, width=15µm and inner diameter =80µm).

Figure 4-11 shows the layout of the driver. An octagonal inductor is used in this design. The octagonal structure occupies a smaller area and at high frequencies shows lower resistance due to the skin effect, compared with square inductors. The inductor structure is differential, which provides a higher level of symmetry. The inductor is realized using metal layers 5 and 6 in a standard 0.18µm CMOS process. The inner diameter of the inductor is 80µm and the metal width is 15µm with 2µm spacing between turns. We chose to use this octagonal inductor as we already had access to an accurate model. However,

use of stacked inductor in this case is more suitable as it is even smaller and has lower Q.

4.4 Conclusion

In this chapter, we have described an approach to designing a tuneable high-frequency amplifier/driver. The technique proves useful for systems with a narrowband input signal whose centre frequency varies over a relatively wide frequency range (e.g., output driver of a VCO). These systems require large output swings to drive a relatively large capacitive load (≈ 1.2Vpp on 1pF). In the proposed design, the centre frequency of the driver is automatically adjusted with the frequency of the input signal via a feedforward control signal from the prior stage. The boosted signal swing provides faster switching for the subsequent logic stages. Given the multi-gigahertz nature of the circuits, inductor values are in the range of one nano-henry and, therefore, are sufficiently small for on-chip integration.

The concept is exemplified using a driver stage between a VCO and the next stage (flip-flops). The advantage of this method is that it uses the same control signal that controls the VCO frequency to adjust the peaking frequency of the narrowband driver. In other words, the feedforward from the VCO control line automatically adjusts the resonance frequency of the driver in order to maintain a sufficient gain over the entire frequency band of operation. There is no need for a separate control circuitry, which simplifies design. The output amplitude boosted by the auto-tuned peaking in the driver stage provides faster switching and guarantees reliable operation for the high-frequency flip-flop over PVT variations.

The output of the 0.18um LC-VCO has a large differential swing, typically in the range of 1.2 to 1.4Vpp. However, buffering it through a cascade of resistively loaded current-model logic drivers would have reduced the swing significantly. It also requires two to three stages with excessive power to deliver an acceptable swing to the input of the high-speed flip-flop. The use of the tuneable driver has reduced the power consumption of the clock driver by more

than a factor of 2, while maintaining a large clock swing in excess of 1Vpp. This large signal swing also boosts the maximum operating frequency of the flip-flop or divider driven downstream.

Chapter 5

Impact of Large Signals on LC-VCO with Accumulation MOS Varactors

A VCO is one of the key building blocks of many modern RF communication systems. Among different architectures, LC-based VCOs are very popular, compared with other architectures such as ring or relaxation VCOs. This popularity is mainly due to lower jitter. A detailed study and comparison of different VCO architectures was provided in Chapter 2.

Figure 5-1 shows the circuit of a CMOS LC-VCO. Despite its lower phase noise, this type of VCO has a smaller tuning range compared to other VCO architectures. With the technology scaling and the constantly shrinking supply voltage, it becomes more difficult to obtain the required tuning range for a given application. To overcome this drawback, the use of MOS varactors with a steep C-V characteristic is almost inevitable.

Consider an LC-VCO such as the one shown in Figure 5-1. The voltage at one end of the varactor is continuously changing, since it is the VCO oscillating output. Therefore, the effective varactor capacitance seen from the inductor ends changes as the VCO oscillates. This change of capacitance invalidates the use of the following simplistic formula to calculate the oscillating frequency of an LC tank (it may only be used for approximating the oscillation frequency):

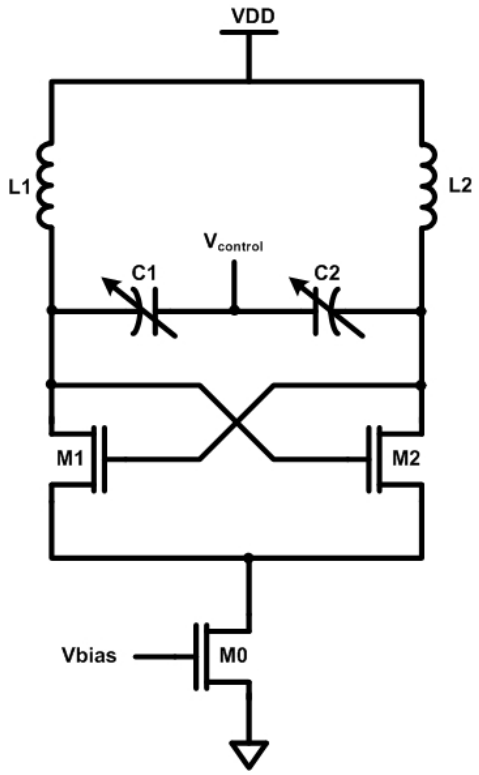


Figure 5-1. CMOS LC-tank VCO

$$f = \frac{1}{2\pi\sqrt{L(C_{fixed} + C_{\text{var}}(V))}}, \tag{5-1}$$

where L is the series combination of L_1 and L_2 shown in Figure 5-1, C_{fixed} is the interconnect and transistor parasitics and C_{var} is the voltage-dependent component of the transistor parasitic capacitance plus the varactor capacitance (i.e. the series combination of C_1 and C_2 in Figure 5-1). Normally, the varactor capacitance is the dominant component. This oscillation of the output signal modulates the variable capacitance, C_{var}, over time. In other words, the effective varactor capacitance is no longer equal to the DC C-V characteristic of the varactor.

This dependence of the oscillation frequency of the negative resistance oscillators to voltage and output harmonics has been studied since 1934 [85]. A number of recent publications in particular, have studied this effect and pointed out the influence of the LC VCO output amplitude on the shape of the output

waveform and the tuning range of the VCO. In [76], a swing- averaging technique is introduced where the varactor capacitance is averaged over the entire supply voltage range (*vdd*). This method provides some insight into the differences between DC C-V characteristic and the effective C-V characteristic; however it is assumed that the output swing is rail to rail, which is not a valid assumption and suggests that further accurate analysis is required. In [60], a weighted averaging technique using a Fourier series is utilized. In [61], differential equation and Fourier series are used to find the effective varactor capacitance and calculate the fundamental oscillation frequency of the VCO. In [62], the output behavior of an LC-VCO is investigated using the current-balance technique. In another recent study, the changes in the tank's frequency are investigated as a function of the oscillator's bias current [77]. The problem is studied from a different angle in [88] to investigate the phase noise and the effects of higher-order harmonics on the phase noise of the oscillator.

In this section, we divide our analysis into two parts: first, we analyze the circuit with the assumption of small signal output. Using the *Jacobian* linearization technique, we solve the differential equation of the LC tank. The second analysis is performed on large signal outputs by describing the output voltage using a *Fourier series* and calculating the dependence of the output frequency on the output amplitude. The differentiation between small signal and large signal is important, as the effective capacitance is substantially different. The analytical results are then compared with simulated results obtained from circuit-level simulations of multiple LC-VCOs in a standard 0.18μm CMOS process.

5.1 MOS Varactors

Before delving into mathematical calculations of the LC-VCO and subsequently tank oscillation frequency, we will briefly review the operation of MOS varactors, which was covered extensively in Chapter 3.

In the past several years there has been considerable work done on the modelling and characterization of MOS varactors. An nMOS varactor can have the same structure as an nMOS transistor with drain, source, and bulk connected together to form one terminal while the gate is the other terminal. Based on the voltage across the varactor (V_{BG}), the operation of these types of devices can be divided into three main regions: accumulation, depletion, and inversion. It has been shown that VCOs with varactors operating predominantly in the accumulation-mode have superior performance in terms of phase noise and power consumption over those operating in inversion mode [56].

Unlike inversion-mode varactors, accumulation-mode nMOS varactors are usually laid out by placing two n-plus regions in an n-well, which forms a two-terminal varactor that does not operate in the inversion mode. In other words, the capacitance becomes a monotonic function of the voltage. Figure 5-2 shows the C-V characteristic of an AMOS varactor. Here, the capacitance decreases monotonically with voltage, rather than displaying the usual V-shaped C-V curve for the capacitance of an nMOS transistor (for more information see Figure 3-2 in Chapter 3). Note that the curve shown in Figure 5-2 represents only the DC C-V characteristics of the varactor and is valid as long as the voltage across the varactor (V_{BG}) can be considered DC. The approximate linear range where the varactor characteristics can be defined as a line (capacitance C versus V_{BG}) has been indicated by two dashed lines in the figure.

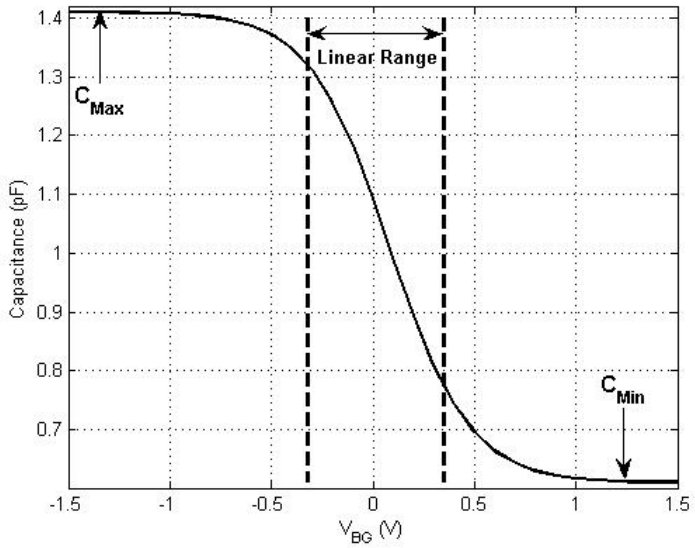


Figure 5-2. C-V characteristic of an accumulation-mode nMOS varactor

Some effort has been made to model this nonlinear C-V characteristic. We explained the modelling issue in detail in Chapter 3 and proposed a new sub-circuit model generated using passive elements and transistor models provided by the foundry. This model is especially suitable for circuit simulators. However, for intensive math calculations, other mathematical models can be more helpful. In another work, the *hyperbolic tangent* function was used to describe the C-V characteristic [78]. This model and its simplified versions, which we will show later in the chapter, are suitable for our study of the large signals in LC-VCOs. The intent is to find the relationship between the VCO output swing and frequency of oscillation. In the next section, the effect of the output swing on AMOS varactors in LC-VCOs is investigated.

5.2 MOS Varactors in LC-VCOs

Consider the RLC circuit shown in Figure 5-3, which models the LC-tank of the VCO of Figure 5-1 in the steady-state. Here, C is an AMOS varactor. The negative transconductance, $-g_{active,}$ is the equivalent transconductance of the cross-coupled active devices, which is equal to $-2/g_m$. In the steady-state, the tank resistance, R_{tank}, and the negative transconductance, $-g_{active,}$ cancel each other [79]. The remaining circuit is a lossless LC tank with a variable

capacitance that oscillates if one applies an excitation current or voltage to it. Our goal here is to come up with an expression to explain the oscillation frequency of this tank (i.e., an LC tank with a variable capacitor). For the sake of comparison, we will compare this oscillation frequency with that of a lossless LC circuit with a fixed capacitance, which is $\omega_{nom} = 1/\sqrt{LC}$.

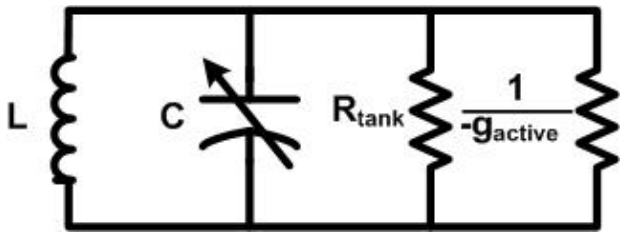


Figure 5-3. LC-tank circuit

In the non-ideal world with limited quality factors for both capacitor and inductor, the nominal frequency of a pure LC tank with fixed *L* and *C* depends on the quality factors of passive components, and is actually equal to $\omega_{osc} = \omega_{nom}\left(1 - \frac{1}{Q_L^{\,2}} + \frac{1}{Q_C^{\,2}}\right)$ [80]. The energy losses in the inductor due to resistive impurities will therefore cause the oscillation frequency to decrease, while those of the capacitor will cause the frequency to increase.

Since the tank voltage is continuously varying with time, we need to calculate the changes in amount of charge stored in the capacitance with respect to voltage change for any marginal change in voltage (shown in (5-2)) in order to get a sense of the capacitance value at any instant in time. Note that any use of large signal relationships such as the known relationships, between charge and voltage of a fixed capacitor *Q=CV* is invalid here: this relationship is only valid for fixed capacitance. In this case, the large signal capacitance cannot be defined for varactors in the same way that it is defined for a fixed capacitance. Therefore, we will be using the small signal capacitance, defined as follows:

$$dQ = C(V)dV \tag{5-2}$$

Using *Kirchoff's current law* (KCL), we write a KCL equation for the node between the inductor and varactor in Figure 5-3:

$$\frac{1}{L}\int V dt = -\frac{dQ}{dt} = -C\frac{dV}{dt}. \tag{5-3}$$

By differentiating from (5-3) and applying the *chain rule*, the following second-order nonlinear differential equation is derived where *C* is a function of *V* and *V* is a function of time:

$$C\frac{d^2V}{dt^2} + \left(\frac{dC}{dV}\right)\left(\frac{dV}{dt}\right)^2 + \frac{1}{L}V = 0 \tag{5-4}$$

As can be seen from (5-4), an additional nonlinear term is present in the second-order differential equation. Therefore, the solution is not as straightforward as for a pure LC resonator with a fixed capacitance. In the subsequent sections, we study the solution to this equation in both small signal and large signal regimes.

5.2.1 Small-signal Analysis

Equation (5-4) is nonlinear and is difficult, if not impossible to solve analytically. However, assuming small signal variations for both *V* and *dV/dt*, we can use linearization techniques to solve the equation. Defining *h(t)* = *dV/dt*, (5-4) can be converted into a system of first-order differential equations and can be solved using the *Jacobian* linearization technique in the vicinity of its *static equilibrium point*:

$$\begin{cases} \dfrac{dV}{dt} = h = f(h,V) \\ \dfrac{dh}{dt} = \dfrac{\dfrac{1}{L}V + h^2\left(\dfrac{dC}{dV}\right)}{C} = g(h,V) \end{cases}. \tag{5-5}$$

The *static equilibrium point* is where both *g* and *h* in (5-5) are zero. To find the static equilibrium point of (5-5), *dV/dt* and *dh/dt* are set to zero, resulting in

(dV/dt,V)=(h,V)=(0, 0). Note that this corresponds to zero current and zero voltage across the LC tank. The *Jacobian matrix* of (5-5) at the equilibrium point is:

$$\begin{bmatrix} \frac{\partial f}{\partial V}(0,0) & \frac{\partial f}{\partial h}(0,0) \\ \frac{\partial g}{\partial V}(0,0) & \frac{\partial g}{\partial h}(0,0) \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ \frac{1}{LC} & 0 \end{bmatrix}. \qquad (5\text{-}6)$$

C in (5-6) is the varactor capacitance obtained from the DC characteristics (i.e. C_{VBG} or the capacitance at the DC level of the output obtained from Figure 5-2). The *eigenvalues* of this matrix, which are the poles of the linearized system, determine the behaviour of the system around the static equilibrium point, i.e., whether the response is oscillatory, over-damped, etc. Since the *eigenvalues* of this matrix are purely imaginary ($\pm j/\sqrt{LC}$), the output of the VCO or *V(t)* is a sinusoidal signal, which oscillates around the equilibrium point with the angular frequency of $1/\sqrt{LC}$. This oscillatory behavior is valid as long as *V* and *dV/dt* remain very close to their equilibrium state, i.e., VCO operates in the small-signal regime.

5.2.2 Large-signal Analysis

The above-mentioned equations and conditions are not valid for the VCO when the gate voltage of the varactor experiences large swings and rapid changes (large *dV/dt*), which is normally the case in oscillators. This large swing results in deviations of the varactor capacitance from its DC value, and therefore, deviating the output waveform from a pure sinusoid. However, the periodic output can still be expressed using *Fourier series*. For large signal swings, output fundamental frequency differs from $1/\sqrt{LC}$ and the output waveform is a superposition of many harmonics of this new frequency.

Using the chain rule, (5-3) can be expressed as:

$$\frac{1}{L}\int V(t)dt = -\frac{d(\int C(V)dV)}{dV}\frac{dV}{dt} = -C(V)\frac{dV}{dt}. \quad (5\text{-}7)$$

Note that *C(V)* appears in the right-hand side of (5-7), due to the time invariant characteristic of the AMOS varactor. The C-V characteristic of AMOS varactors can be approximated using a *hyperbolic tangent function* [78]:

$$C(V) = C_{Center} + K\tanh(\alpha(V_{BG} - V)), \quad (5\text{-}8)$$

where C_{centre} =½ (C_{max}+C_{min}), K = C_{min} - C_{centre}, (C_{max} and C_{min} are shown in Figure 5-2) $\alpha>0$ is the expansion coefficient and is constant [78], V_{BG} is the bias voltage of the varactor assuming the gate terminal is AC grounded but connected to a DC source for biasing (the bias circuit is not shown in Figure 5-3), and *V* is the output voltage of the tank in Figure 5-3 (AC variations on the varactor). The *C(V)* of an AMOS varactor can be approximated linearly in the narrow steep linear range indicated by dashed lines in Figure 5-2 as follows:

$$C(V) = C_{V_{BG}} - \alpha KV, \quad (5\text{-}9)$$

Also, with the assumption of a periodic output, we express *V(t)* using the following Fourier series:

$$V(t) = \sum_{m=1}^{\infty} a_m \cos(m\omega t), \quad (5\text{-}10)$$

Note that *V(t)* is not necessarily sinusoidal, as otherwise we would have been able to solve (5-4) for the particular *sinusoidal* solution. As we stated earlier, (5-4) does not have a known closed-form solution. Therefore, we use the *Fourier series* for *V(t)* to derive the oscillation frequency.

Using (5-9) and (5-10) for *C* and *V*, respectively, and substituting them in the original differential equation (5-3), we have

$$\frac{1}{L}\sum_{m=1}^{\infty}\frac{a_m}{m\omega}\sin(m\omega t) = \left(C_{V_{BG}} - \alpha K\sum_{m=1}^{\infty} a_m\cos(m\omega t)\right)\times\left(\sum_{m=1}^{\infty} m\omega a_m \sin(m\omega t)\right) \quad (5\text{-}11)$$

Now we try to solve (5-11) for ω by equating the coefficient of the main harmonic (sinωt) from the two sides of the (5-11) (after converting the right-hand side to terms of a *Fourier series* again). Since solving this in general for an infinite number of terms is not practical, we consider three cases: the output signal, *V(t)* has only one harmonic (pure sinusoidal signal), two harmonics and three harmonics. The assumption of three harmonics is very close to reality as the higher terms in the *Fourier series* are less significant due to their very small coefficients.

Case I: *V(t)* is made up of only one harmonic:

$$V(t) = a_1 \cos(\omega t) \Rightarrow \omega = \frac{1}{\sqrt{LC_{V_{BG}}}}, \tag{5-12}$$

Case II: *V(t)* is made of the two first harmonics:

$$V(t) = a_1 \cos(\omega t) + a_2 \cos(2\omega t), \tag{5-13}$$

and the frequency of the main harmonic is as follows:

$$\omega = \frac{1}{\sqrt{LC_{V_{BG}}\left(1 - \frac{\alpha K a_2}{2C_{V_{BG}}}\right)}}, \tag{5-14}$$

Case III: *V(t)* is made up of the first three harmonics

$$V(t) = \sum_{m=1}^{3} a_m \cos(m\omega t), \tag{5-15}$$

which results in the following oscillation frequency:

$$\omega = \frac{1}{\sqrt{LC_{V_{BG}}\left(1 - \frac{\alpha K a_2 (a_1 + a_3)}{2a_1 C_{V_{BG}}}\right)}}. \tag{5-16}$$

These results give us some insight about the actual oscillation frequency of the tank (or equivalently, the LC-VCO). First, ω in all three cases, has one major component, which is $1/\sqrt{LC}$. However, (5-14) and (5-16) show that the actual frequency could deviate from the nominal frequency or (5-12) depending on the coefficients of the first, second and third harmonics (i.e., a_1, a_2 and a_3). If we normalize (5-16) relative to the nominal oscillation frequency or (5-12), we obtain:

$$\frac{\omega_{osc}}{\omega_{nom}} = \frac{1}{\sqrt{\left(1 - \frac{\alpha K a_2 (a_1 + a_3)}{2 a_1 C_{V_{BG}}}\right)}} . \qquad (5\text{-}17)$$

Equation (5-17) indicates that deviations are due to harmonics of the output signal. Depending on the magnitudes of these coefficients, the actual oscillation frequency could differ from the nominal frequency. In addition, it is clear that the second-order harmonic has significant importance. If we assume that $a_1 >> a_3$ (i.e. the coefficient of the first harmonic is significantly larger than that of the third harmonic), we can rewrite (5-17) as follows:

$$\frac{\omega_{osc}}{\omega_{nom}} \cong \frac{1}{\sqrt{\left(1 - \frac{\alpha K a_2}{2 C_{V_{BG}}}\right)}} . \qquad (5\text{-}18)$$

Therefore, the smaller the a_2, the closer the frequency is to its nominal value. Once again, we emphasize that these results are obtained by assuming a linear varactor (i.e., varactor operating in the linear range of Figure 5-2 or roughly inside the two vertical dashed lines).

The next section verifies these frequency discrepancies analytically derived here, using simulations of LC-VCOs at the circuit-level with accurate foundry models in SPICE.

5.3 Simulation Results

In order to verify the presented analysis at the circuit-level, we designed multiple LC-VCOs in a standard CMOS 0.18μm technology with 1.8V supply voltage. The circuit schematic of the VCO is shown in Figure 5-4.

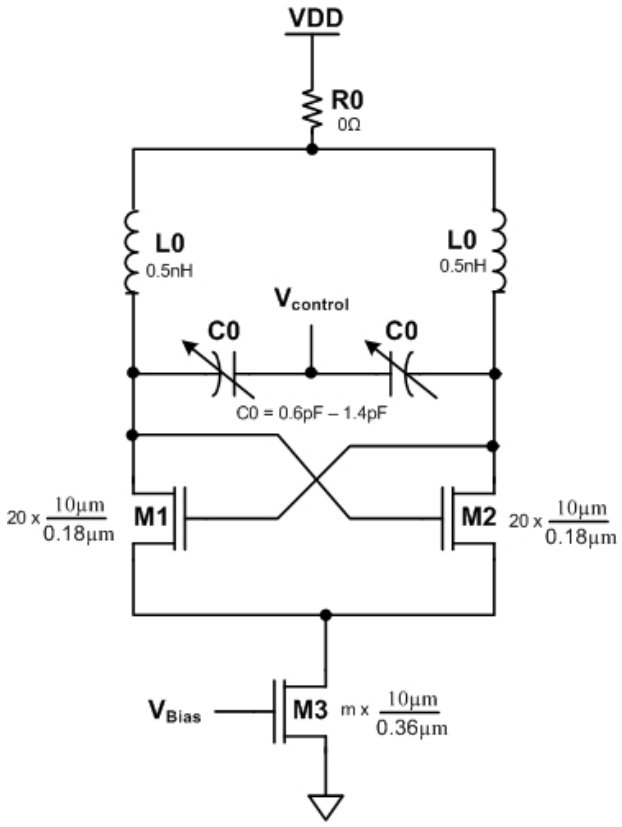


Figure 5-4. Circuit schematic of an LC-VCO designed in a standard CMOS 0.18μm technology for 4 GHz to 6 GHz operation range.

The inductor is a differential centre-tapped 3-turn octagonal structure with inductance of about 2×0.62nH. The inner diameter of the inductor is 80μm and the wire width is 15μm, with 2μm spacing. The major capacitance of the tank is provided by two series accumulation-mode nMOS varactors connected back-to-back with a common bulk used as the control terminal. Each varactor capacitance varies between 0.6pF to 1.4pF (Figure 5-2). The varactor structure is a 10-by-10 matrix of nMOS devices laid out in n-well with a unit aspect ratio of 2.5μm/0.5μm. Transistor M_3 acts as the current source. Resistor R_0 is normally used to lower the output DC level to about supply mid-point (i.e., 0.9V) in order to

benefit from both the positive and negative range of the varactor C-V characteristic. The aspect ratios of all transistors are indicated in the figure.

The VCO output amplitude can be limited by two independent mechanisms: supply voltage, and the tail current. Since the supply voltage normally comes with the technology and the designer does not have control over it, we use the tail current to control the output amplitude and verify the dependency of the output frequency on the shape of the output amplitude. If we assume that at high frequencies (i.e., multi-GHz), the current waveform could be approximated by a sinusoid due to the finite switching time and limited gain [63], the differential output swing, V_{output} can be estimated as follows:

$$V_{Output} \approx I_{tail} R_{loss}\,, \tag{5-19}$$

Where R_{loss} is the combined magnetic and resistive losses of the tank mostly dominated by the resistance of the metal wire in the inductor, the *skin effect* at high frequencies, the *Eddy current* and loss through the substrate. All these effects are very difficult or costly to be controlled by the designer. Therefore, the simple approach to controlling the amplitude is to adjust the tail current. We selected four different multiplication factors for M_3 (m = 4, 6, 10, 14). We also decided to keep the output DC level at 1.8V (i.e., R_0 = 0Ω) in order to have consistent comparison between all four VCOs. Otherwise, the DC level would have changed with the change in the tail current as the drop in the resistor R0 would have been different for different m values. We swept the control voltage, $V_{control}$ from 1.0V to 2.7V to cover the entire variable range of the varactor (Figure 5-2). Using the four m factors, we obtained four different amplitudes with average single-ended values of: 0.31V, 0.51V, 0.82V and 1.01V. As expected, the tuning curves obtained from these simulations are substantially different depending on the output amplitudes and their shape (higher order harmonics). Figure 5-5 shows the four tuning curves, with their respective average single-ended amplitudes indicated with arrows.

We conducted another experiment to observe the exact changes in oscillation frequency at a fixed control voltage. For this experiment, $V_{Control}$ is set

to 1.8V, which biases the varactor at about the mid-point of its C-V curve (Figure 5-2) with the highest *dC/dV*. Then we swept *m* factor from 1 to 30 to change the current and consequently the output amplitude. For the first two points (*m*=1, 2), there is no oscillation as the transconductance, g_m, and subsequently the gain, are small, and the differential pair does not have enough closed-loop gain to cancel the tank loss and amplify the noise (i.e., the *Barkhausen conditions* are not satisfied). For *m* values larger than 2, the circuit starts to oscillate with the single-ended amplitude increasing from 0.13V to 1.78V. Figure 5-6 shows the output frequency versus amplitude for the fixed control voltage of 1.8V (mid-point of the C-V characteristic).

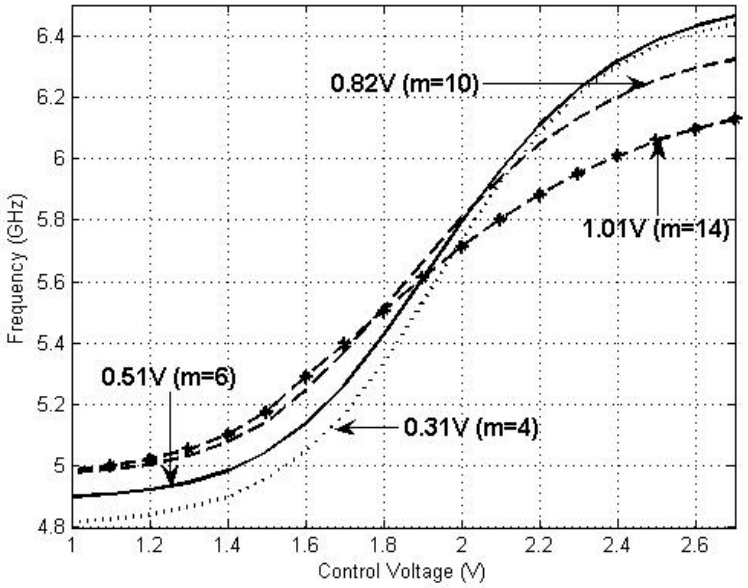


Figure 5-5. Tuning curves of four VCOs, all with the same architecture as shown in Figure 5-4 but with different *m* factors for transistor M_3.

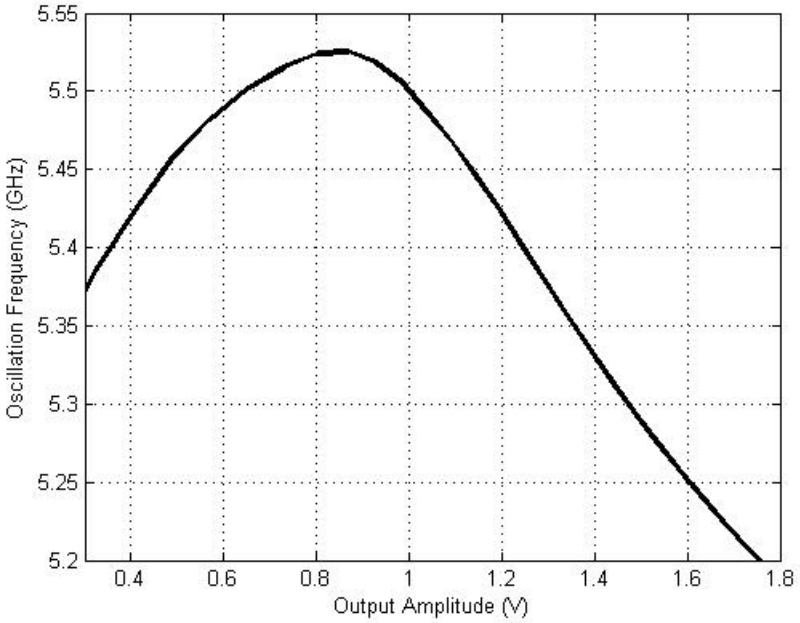


Figure 5-6. Oscillation frequency of the LC-VCO of Figure 5-4 for different *m* factors (*m=3*..30), when $V_{Control}$=1.8V.

Note that at higher frequencies the losses of the tank increases due to the skin effect (i.e., R_{loss} goes up). Therefore, even with a fixed current, the amplitude would go up slightly when we increase the control voltage. As a result, the output values shown in the figure are the average amplitudes for the entire tuning range. The highest tuning range is obtained for the smallest amplitude (from almost 4.8 GHz to about 6.4 GHz). As the amplitude increases, the curves are smoothed out.

It can be observed that the frequency peaks as the output amplitude reaches about 800mV. The initial rise in the frequency could have been the result of two independent effects:

1. The first effect that results in a rise of frequency can be explained from our mathematical analysis summarized in (5-18). In summary, the rise in the tail current and therefore, output amplitude, increases the magnitude of the coefficient of the second harmonic, which according to (5-18) will result in a rise in frequency.

2. The second reason for this rise in frequency is due to the non-ideal current source (the tail current) [77]. The even harmonics of the output current will flow through transistor M_3 of Figure 5-4. In an ideal world, this transistor acts as a current source with infinite output impedance. However, in reality, the impedance is finite: for instance, there is the capacitance, C_p, associated with the drain node of M_3, which accounts for the source parasitic capacitances of the differential pair as well as the drain parasitic capacitance of M_3, and interconnect parasitics. This capacitance is seen from the tank circuit as negative capacitance [77], and hence, reduces the total tank capacitance. Therefore, the oscillation frequency will go up.

In order to find out how much of the frequency change can be attributed to each of the above-mentioned phenomena, we performed another experiment. We replaced the varactors of the LC-VCO in Figure 5-4 with fixed capacitors. The capacitor value was equal to the varactor value with $V_{BG}=0V$ or $C=1.1pF$ (i.e., varactor biased at approximately mid-point of its linear range). We then ran the same experiment by changing the *m* factor of the M_3 from 1 to 30. The oscillation frequency was calculated for every point. This result is illustrated in Figure 5-7.

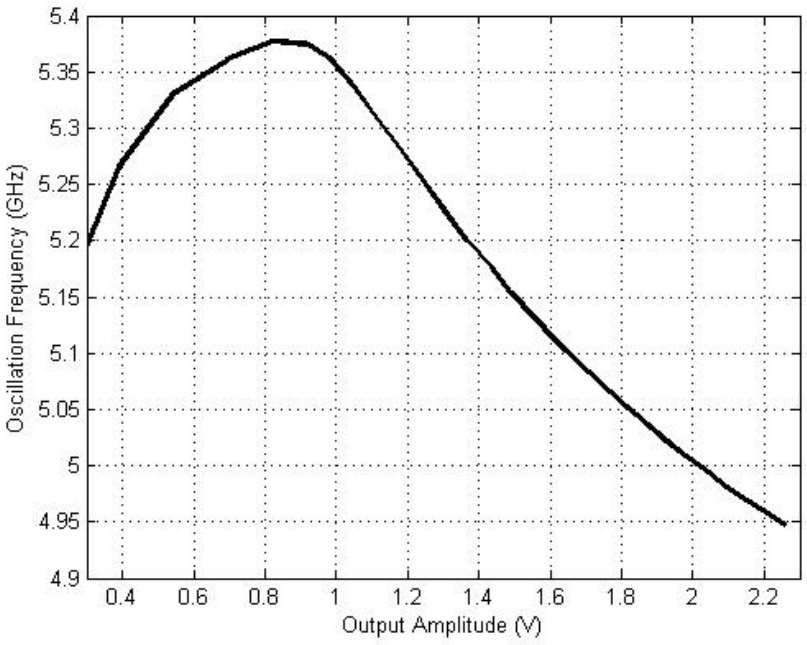


Figure 5-7. Oscillation frequency of an LC oscillator shown in Figure 5-4 with fixed tank capacitors of 1.1pF for different *m* factors (*m*=*3*..30).

It can be seen that the frequency variations for the LC-VCO are about 5.1%, as shown in Figure 5-6 (from 5.35GHz to 5.55GHz), compared with 2.1% in the LC oscillator with fixed capacitors shown in Figure 5-7 (from 5.2GHz to 5.35GHz). This indicates the influence of the output harmonics on the oscillation frequency resulting from the presence of a variable capacitor. One other difference between these two figures is the maximum amplitude of the output. It can be seen that the oscillator with a fixed capacitor has a higher amplitude for the same amount of current. That is because we used pure capacitance with no resistive loss for this capacitor, which increases the quality factor of the tank.

As the oscillation amplitude grows, the signal path experiences severe nonlinearity and eventually saturation, causing the signal to deform and be clipped at the two ends. Therefore, the coefficients of the higher-order harmonics become significant due to harmonic distortion. The output waveforms are depicted in Figure 5-8 for two scenarios where *m*=8 and *m*=20. The smaller waveform still resembles a sinusoidal signal while the larger waveform suffers from harmonic distortion and no longer resembles a sinusoidal signal.

The same observation can be made on the tuning curves of Figure 5-5 where the frequency of m=6 is always higher than m=4 but the trend changes for higher *m* values. If we continue to increase the current, at some point the tail current source enters the triode region and will not act as a constant current source anymore (starts to switch between on and off conditions with an average total current). The output amplitude stays almost constant, as does the output frequency. The simulation results indicate that frequency discrepancies could be as much as 6%, depending on the output shape and voltage (with constant control voltage).

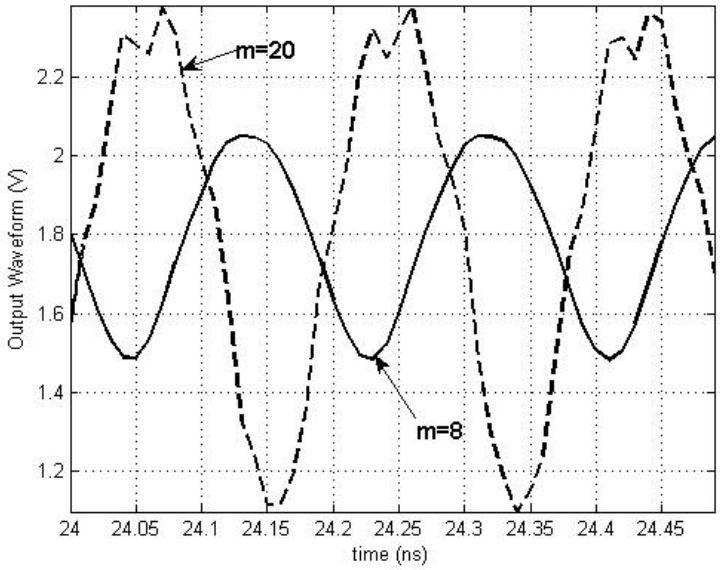


Figure 5-8. Output waveform for two different *m* values at $V_{Control}$ = 1.8V. The solid line shows the output for *m*=8 while dashed line shows the VCO output for *m*=20.

5.4 Conclusion

In this chapter, the effect of the output signal swing of an AMOS LC-VCO has been analyzed quantitatively and qualitatively. We have shown that for small-signal swings, the output frequency is almost the same as the nominal frequency of a tank circuit with fixed inductance and capacitance $\left(1/\sqrt{LC}\right)$. However, for large signal swings the frequency deviates from its nominal value. The output signal of a large swing AMOS LC-VCO consists of many harmonics. An approximate formula for estimating the relationship between the frequency of an

LC tank with a linear capacitance and the tank output amplitude has been derived. In addition, using circuit-level simulations we further verified the significance of the output amplitude by investigating the changes in the tuning curves of multiple LC-VCOs designed for multi-GHz operation (4.8 GHz to 6.4 GHz) in a standard CMOS 0.18μm process. We showed that the curves smooth out as the output amplitude becomes larger. We also showed that the VCO frequency can rise or fall, depending on the output shape and amplitude. Initially, the frequency rises with amplitude due to non-idealities of the tail current source and the capacitance associated with that node as well as the output harmonics (mainly the second harmonic as shown in (5-18)). Later, the frequency drops due to the presence of the large higher-order harmonic in the output. Simulations indicate that output frequency can undergo a greater than 6% variation for a fixed-control voltage.

Chapter 6

Conclusions

Everyday, new bandwidth-hungry Internet applications such as the video sharing website, youtube.com, are emerging. Bandwidth requirement are growing at an extremely fast pace, which calls for more robust Internet infrastructure capable of handling bit rates of a few terabits per second. This massive network infrastructure is currently deployed worldwide, across the continents and under the oceans using thousands of kilometres of optical fibre cable. Although the loss of optical fibre is negligible, several regeneration sites are still required between every two Internet hubs to ensure reliable data transfer and acceptable signal-to-noise ratio at the user's end.

The clock and data recovery block is the key building block, functioning in these regeneration sites, inside the SERDES chipsets. They are also an integral part of the receiver, used for extracting the timing information and de-serializing the data for further processing by subsequent blocks.

We explained the importance of implementing this key block in the CMOS technology. Among the reasons, we cited lower cost, lower power, higher manufacturing yield, and shorter time-to-market. However, the major disadvantage of this technology is its lower speed, as opposed to other higher speed technologies (e.g., III-V, or silicon bipolar), which poses many new challenges for designers who are dealing with high-speed circuits.

In this dissertation, we proposed solutions at the device, and circuit levels to address issues confronting designers in some of the key blocks of high-speed

CMOS CDR systems. In the next section, we summarize the key accomplishments discussed in the previous chapters.

6.1 Accomplishments

- **Bang-bang or linear?**

We reviewed most recent works published in ISSCC from 2001 to 2007. Our studies showed that bang-bang PDs have a simpler operation than linear PDs; they only need to take a sample of the data at the clock edges, unlike linear PDs, which operate on the pulse width. Therefore, a small timing skew or delay can deteriorate the operation of the linear CDR, while the simple operation of the BBPD allows its operation at rates comparable to the technology transition frequency. Our survey of most recent relevant work further confirms the fact that BB CDRs are used more often at high frequencies (see Figure 2-12 and Figure 2-13). Bang-bang topologies are also more suited for multi-phase clocking, since the data sampling can be easily expanded to multi-phase solutions. However, a major drawback of BB CDRs is the dependence of the jitter transfer function on the amplitude of jitter, explained in Chapter 2. This relationship is formulated in (6-1) where ω_{-3dB} is the cut-off frequency of the low-pass jitter transfer function.

$$\omega_{-3dB} = \frac{\pi K_{VCO} I_{CP} R_1}{2\Phi_{Data,Max}} . \qquad (6\text{-}1)$$

In conclusion, linear CDRs usually result in lower output jitter. At high frequencies, however, implementation of BBPDs is easier and more feasible.

- **Modelling an AMOS varactor**

We identified the LC-VCO as a low-phase-noise oscillator suitable for designs such as CDRs and frequency synthesizers where phase-noise performance is of significant importance. The need for an accurate model for varactors as the tuning component of these VCOs was investigated by studying the discrepancies between the measured and simulated tuning curves. We introduced a new sub-circuit model in order to address some of the shortcomings of the current existing

models. The current foundry-provided models are based on curve fitting to measured results of particular test structures. These models often result in convergence problems and/or require long simulation times [55]. Furthermore, they cannot be easily ported to other technologies and are only valid for a few particular varactor structures, which are normally designed for average (non-minimum) gate lengths. Therefore, they are not suitable for aggressive (e.g., high-speed) designs that require minimum gate lengths.

The model that we have introduced here, can be ported from one process to other CMOS processes as long as a valid device model exists for MOSFET transistors in the target technology. The model is not limited to a particular gate length. In addition, since it is based on transistor models, it automatically incorporates some of the non-idealities of leading-edge technologies such as the leakage current of the gate oxide in the 90nm CMOS process or finer gate length process, provided these non-idealities have been accounted for. This makes it possible to use the varactor in the design as soon as the first version of the design kit becomes available (foundries normally include their limited library of passive elements in the second or newer revisions of the design kit).

The model was verified independently using two different processes (0.18μm CMOS and 0.13μm CMOS). We used two approaches to verify the model. In the direct method, we extracted the measured values for the varactor and compared them against the simulated values. In the indirect method, we used the varactor inside the LC-VCOs and then compared the measured and simulated tuning curves of those LC-VCOs. In all cases, we obtained good agreement between the model and the measured values.

The model still has some limitations which can be the topic of future work. For example, the offset voltage used to account for the silicon bandgap voltage difference between p+ and n+ material is temperature dependent and requires more accurate modeling. The components representing the substrate parasitics (i.e., diode and resistors) are layout dependent and their exact value depends on the layout structure. The same thing applies to the overlap capacitance, C_{OV}. The

process variations can be different for nMOS varactor and its equivalent pMOS sub-circuit model used in the simulation, which may cause some errors in the final results. These limitations can be the subject of future work on AMOS varactor modeling.

During this study, we also investigated different de-embedding techniques for varactor characterization and showed how to eliminate the undesired components from the actual device-under-test (DUT) to find the accurate characteristics of the device.

- **High-speed tuneable clock buffer**

We showed that one of the challenges in CMOS high-speed design is dealing with parasitic capacitances of interconnects and transistors, which are not negligible at higher frequencies due to the frequency dependency of impedance and the given short period (i.e., high frequency) for charging and discharging these small capacitances. For instance, in a CDR system, the VCO clock has to drive the capacitive load of flip-flops in the phase-detector block. Driving this load in the multi-GHz range is not easy with the current transit frequencies of technologies and often requires an inductive load instead of a resistive load. We described a novel technique for high-frequency amplification using inductance and capacitance resonance. This technique proves useful in applications where the frequency of the input signal varies within a predictable range (e.g., the VCO in a CDR). The driver provides a large swing with fairly low power (i.e., about 5mW). Although it is a narrowband driver, its centre frequency is tuneable over a large bandwidth. This feature is obtained by using an AMOS varactor to control the resonance frequency of the driver. Using the proposed technique, a clock driver is designed and simulated in a standard 0.18μm CMOS technology. The monolithic driver operates in a frequency range of 4.85GHz to 5.8GHz over process, voltage, and temperature (PVT) variations, and consumes a nominal DC power of 5.1mW while delivering 1.2 Vpp to a 1 pF load at the centre frequency of 5GHz.

- **Relationship between the output voltage and the oscillation frequency of the LC-VCO**

We investigated the effect of the output shape and amplitude on the frequency of oscillation in LC-VCOs with accumulation-mode MOS varactors. We showed that the varactor C-V characteristic is different for small-signal and large-signal regimes. We derived the relation between the operating frequency of an LC-VCO and its oscillation amplitude using Fourier series expansion of the output voltage. We showed that this frequency differs from the simplistic relation used to describe the nominal frequency of a tank ($\omega_{nom} = 1/\sqrt{LC}$). The ratio of the tank nominal frequency to the LC-VCO frequency for the first three harmonics was calculated, for when the varactor is modeled as a line in its linear region:

$$\frac{\omega_{osc}}{\omega_{nom}} \cong \frac{1}{\sqrt{\left(1-\frac{\alpha K a_2}{2C_{V_{BG}}}\right)}}, \qquad (6\text{-}2)$$

To validate the analytical results, multiple 5-6 GHz LC-VCOs were designed each with different oscillation amplitudes using a standard 0.18μm CMOS technology. Simulation results of VCOs further confirms the impact of the output amplitude on the oscillation frequency. We showed that the frequency of the LC-VCO increases to a certain point with an increase in amplitude due to the non-ideal current source as well as the above-mentioned reasons. After that, the frequency starts to decrease, due to harmonic distortion and the effect of larger coefficients for higher order harmonics (Figure 5-8).

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Appendices

Appendix A – Jitter Terminology

This appendix explains many useful jitter terms used by designers in papers and technical reports, in alphabetic order.

Accumulating Jitter - *Accumulating jitter* is a variation in the delay between an output transition and the subsequent output transition. It is generated by autonomous blocks (i.e., blocks that are self-driven) such as oscillators or VCOs. These blocks generate the new output state as a result of the previous output state [54].

Cycle-to-Cycle (or Period) Jitter – Cycle-to-cycle (or period) jitter is the variation from one period to the next adjacent period of the signal. In order to determine the variation between adjacent periods, all consecutive periods need to be measured. Cycle-to-cycle jitter is the most difficult to measure, usually requiring a timing interval analyzer.

Deterministic Jitter - The predictable component of jitter is called *deterministic jitter* or *data pattern dependent jitter*. It comes from many sources, including duty-cycle distortion (DCD), inter-symbol interference (ISI), and word-synchronized distortion due to imperfections within a data serializer (e.g., bit 3 of each data word always appears early).

Jitter Generation - *Jitter generation* is the measure of the intrinsic jitter produced by the PLL and is measured at its output. Jitter generation is measured by applying a reference signal with no jitter to the input of the PLL, and measuring its output jitter. Jitter generation is usually specified as a peak-to-peak period jitter value [81].

Jitter Tolerance - Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock in the presence of jitter of various magnitudes at

different frequencies) when jitter is applied to its reference. Jitter tolerance is usually specified using an input jitter mask [81]. In other words, jitter tolerance is the maximum input jitter that a CDR loop can tolerate without increasing the bit error rate.

Jitter Transfer or Jitter Attenuation - Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various bandwidth settings. Since intrinsic jitter is always present, jitter attenuation will appear to be lower for low frequency input jitter signals than for high frequency ones. Jitter transfer is typically specified using a bandwidth plot [81].

Peak-to-Peak Jitter - *Peak-to-peak jitter* is the difference between the maximum and minimum phase of the clock signal over all time. Peak-to-peak jitter is the worst case of cycle-to-cycle jitter.

Random Jitter - The random component in jitter is due to the noise inherent in electrical circuits and typically exhibits a Gaussian distribution. Random jitter (RJ) is due to stochastic sources, such as substrate and power supply. Electrical noise interacts with the slew rate of signals to produce timing errors at the switching points. *Random jitter* is additive as the sum of squares, and follows a bell curve. Since *random jitter* is not bounded, it is characterized by its standard deviation (rms) value.

RMS Jitter - *RMS jitter* is the standard deviation of jitter.

Synchronous Jitter - *Synchronous jitter* is a variation in the delay between when the input is received and the output is produced. It is generated by driven blocks (i.e., blocks in which transition at their output is a direct result of a transition at their input) such as PFD, CP and FD [54].

Appendix B – Flicker Noise Generation and Modelling for CDR Applications

To devise a simulation setup that closely mimics the real world situation, we need to take into account different types of noise (white and flicker in the case of CDR) at sensitive entering points and internal blocks of the CDR system. Two sensitive spots that largely affect the overall performance of the system are the added noise (intrinsic) on the input data and the VCO output, which could both be responsible for a portion of the total phase noise on the retimed output data. VCO frequency-modulates the noise on the control line as well as the internal device noise to near its oscillating frequency at the output. While the high-frequency noise on the output of VCO cannot be suppressed by the feedback loop, it is directly reflected on the retimed data. The input data can also carry a significant amount of noise generated from the non-ideal reference clock at the transmitting site as well as other noises picked up on the way to the destination. Although this noise is low-pass filtered with the CDR loop filter, we still need to consider it in the input as it is not insignificant.

The addition of white noise at different points is relatively easy, as most simulation tools have some sort of random sequence generator built into them. However, generating *flicker noise*, and adding it to the phase of the data or clock may not be as straightforward.

Here we show a scheme for generating *1/f noise* and adding it as phase noise to both input data and VCO output, accompanied by a *Matlab*® code used to generate random flicker noise. The method utilized for flicker noise generation was obtained from [82].

Colored noise, which has been reported as a source of noise in many devices and systems, is seen to produce noises with an auto-spectral density proportional to $1/f^{\alpha}$, where f is the frequency and α is a real number between 0 and 2. For $\alpha = 1$, the noise is called flicker noise, a.k.a. 1/f or pink noise. Although the source of this noise in electronic devices has been extensively investigated over the past 50 years, studies show that the physical mechanism

and the origin of 1/f noise is still not fully established [83]. Even some recent works suggest that lower measured 1/f noise relative to simulated results is not due to over-design, as reported by designers. Rather, it is due to an autp-spectral density other than 1/f [84], which takes place in fast and small transistors. However, here we stick to the same 1/f definition and define our power spectral density as follows:

$$S_X(\omega) = \frac{k^2}{\omega}. \tag{6-3}$$

$\omega = 2\pi f$ is the angular frequency, and *'k'* is a constant of the flicker noise. If we assume that the noise power per one Hertz at offset frequency, f_0 relative to the carrier frequency, f_c is P_0 dBc/Hz, we can calculate the constant k of the flicker noise, as follows:

$$p_0 = \frac{1}{2\pi} S_X(\omega_0)\, \omega_b . \tag{6-4}$$

where $\omega_b = 2\pi f_b / f_c$ is the desired bandwidth in radians measured relative to the carrier (f_b = 1 Hz), and $\omega_0 = 2\pi f_0 / f_c$ is the offset frequency in radians relative to carrier. Therefore, the average noise amplitude could be calculated as follows:

$$p_0 = \frac{1}{2\pi}\frac{k^2}{\omega_0}\omega_b, \tag{6-5}$$

$$p_0 = \frac{k^2}{2\pi f_0}, \tag{6-6}$$

$$k = \sqrt{2\pi f_0\, p_0}\ . \tag{6-7}$$

Note that the constant k is not a function of carrier frequency, f_c. Using (6-5), one can calculate the constant of the flicker noise, which can be applied to a randomly generated white noise with zero mean and the desired standard deviation in the time domain. Then using a *Finite Impulse Response* (FIR) technique and *auto regression* filtering, a sequence of *1/f* noise can be

generated. Figure is the *Matlab*® code for generating noise with *1/f* characteristics, developed using the algorithms described in [82]. A sample flicker noise in time domain generated using the code in Figure has been illustrated in Figure . The equivalent frequency domain of this noise obtained using *Fast Fourier Transform* (FFT) is shown in Figure B-.

```
main_tone = 1e9;  % Frequency of Main Harmonic
resolution = 0.001*1/main_tone;
t = 0:resolution:10/main_tone; % Time Domain
f0 = 10e3; % offset frequency from main tone
% dbc_per_hz = -70; % Power of the flicker noise at the offset
% frequency f0
num_taps = 200;   % number of taps for AR filter

% Generate white noise. Apply gain for desired dBc/Hz.

k = sqrt(2*pi * f0 * 10^(dbc_per_hz/10));
wn = k * randn(1,length(t)); % white noise

fprintf(Constant of the white noise = %f.\n', k);

% Generate 1/f AR filter and apply to white noise to produce 1/f
%  noise

a = zeros(1,num_taps);
a(1) = 1;
for ii = 2:num_taps
   a(ii) = (ii - 2.5) * a(ii-1) / (ii-1);
end
theta = filter(1,a,wn);

% theta (1/f noise) could be added to control voltage of the VCO
```

Figure B-1. Matlab® code for 1/f noise generation for VCO control line

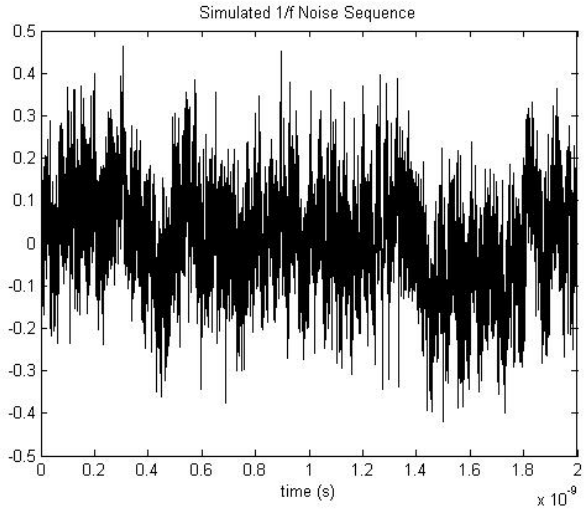

Figure B-2. Samples of 1/f noise in time domain

After obtaining random noise with the desired power, we need to phase-modulate it correctly to the signal (data or clock). In the case of VCO, we could simply add this to the control voltage of the VCO and it will be automatically frequency modulated and added to the phase of the output as the VCO performs voltage-to-frequency conversion.

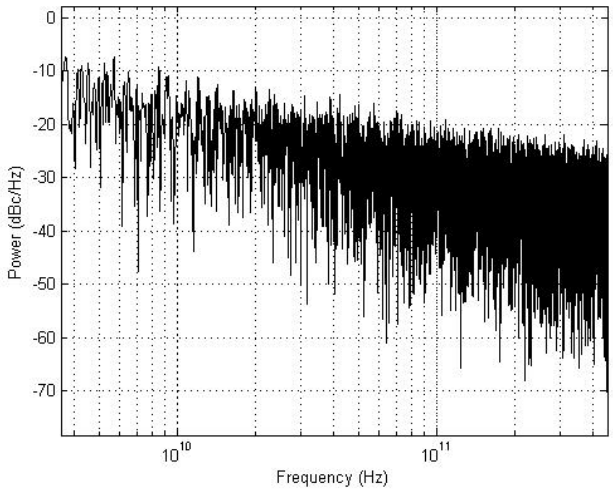

Figure B-3. Auto-spectral density of the generated 1/f noise in Figure obtained using Fast-Fourier Transform (FFT).

However, this is not as easy for random input data. To add the phase noise to the input data, we used the architecture shown in Figure B-. The clean and jitter

free data is fed to a flip-flop and read using a jittery clock generated by a VCO. The VCO control voltage can carry all different components of the noise (i.e., white noise and flicker noise).

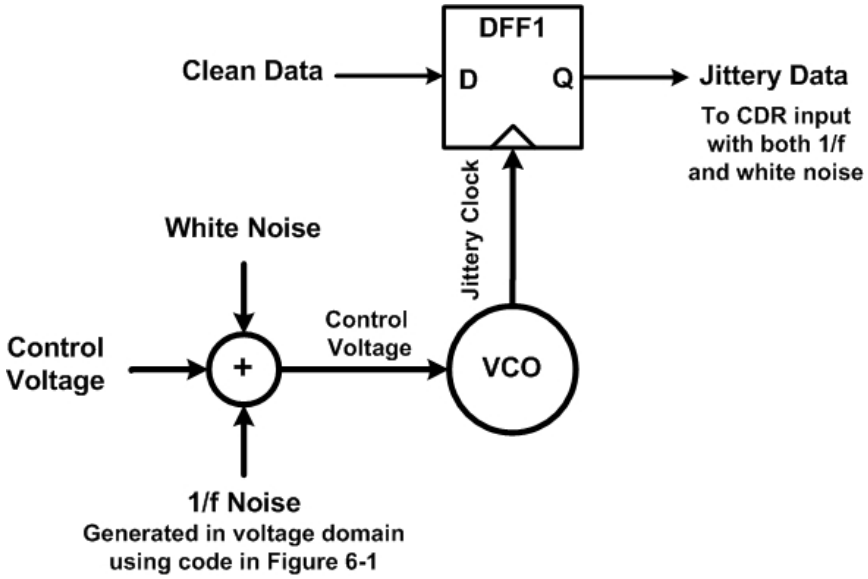

Figure B-4. Adding 1/f and white noise to the clean data

Appendix C – The *Analog Verilog* Code for the AMOS Varactor

The following code was used to define a *VerilogA* module for an AMOS varactor in a standard CMOS 0.18µm with Cadence® [81]:

```
// VerilogA for Varactor_Ahdl cell in PhD_Chip library
`include "constants.vams"
`include "disciplines.vams"

module Varactor_Ahdl(p,n);
inout p,n;
electrical p,n;

parameter T=25;
parameter Tnominal=25;

real Delta_T;
real q,v;
real Vgnorm0, dVgs0, dCg0,Cgmin0, T1_Vgnorm, T2_Vgnorm;
real T1_Cg, T2_Cg, T1_Cgmin, T2_Cgmin, Vgnorm_T, Cgmin0_T, dCg0_T,
dVgs0_T;
real T1_dVgs, T2_dVgs;

analog begin
      Vgnorm0=456m;
      dVgs0=-116m;
      dCg0=1.029p;
      Cgmin0=950f;
      T1_Vgnorm=965.6u;
      T2_Vgnorm=-1.841u;
      T1_Cg=-65.64u;
      T2_Cg=183.6n;
      T1_Cgmin=350.3u;
      T2_Cgmin=10.71u;
      Delta_T=T-Tnominal;

      Cgmin0_T=Cgmin0*(1+T1_Cgmin*Delta_T+T2_Cgmin*Delta_T*Delta_T);
            dCg0_T=dCg0*(1+T1_Cg*Delta_T+T2_Cg*Delta_T*Delta_T);
            dVgs0_T=dVgs0*(1+T1_dVgs*Delta_T+T2_dVgs*Delta_T*Delta_T);

      Vgnorm_T=Vgnorm0*(1+T1_Vgnorm*Delta_T+T2_Vgnorm*Delta_T*Delta_T);
      v=V(p,n);
      q=(Cgmin0_T+dCg0_T)*v+dCg0_T*Vgnorm_T*ln(cosh((v-
      dVgs0_T)/Vgnorm_T));
      I(p,n)<+ddt(q);
 end
endmodule
```