Ultra Wideband Coplanar Waveguide Based Impedance Transformer with Slow-wave Electrodes

by

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BASc, University of British Columbia, 2007

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF
THE REQUIREMENTS FOR THE DEGREE OF
MASTER OF APPLIED SCIENCE
in
The Faculty of Graduate Studies

(Electrical and Computer Engineering)

THE UNIVERSITY OF BRITISH COLUMBIA

(Vancouver)

June 2010

Abstract

A new type of broadband impedance transformer loaded with capacitive fins (ITF) and suitable for use up to 100 GHz is presented. The development of ITF is motivated due to the growing demand for the ever increasing transmission speed in the telecommunications industry. At millimetre wave frequencies, impedance matching is crucial to reduce reflections between mismatched loads, allowing for cleaner signal transfer and higher bit rates.

Conventional tapered impedance transforms have been used in the past to achieve wideband impedance matching. In order to improve the performance of tapered impedance transformers, we adopted a slow-wave electrode design approach. A typical ITF structure utilizes capacitive loading fins to control the impedance along the line. This increases the effective microwave index of the impedance transformer. Compared with conventional, unloaded, tapered impedance transformers, ITF structures extend the impedance matching range and the operating bandwidth for the same amount of on-chip real-estate. We have designed ITFs capable of impedance matching resistive loads from ~ 10 Ω to ~ 229 Ω, on a 650 μm thick GaAs substrate, for frequencies up to 70 GHz. Several design examples are used to demonstrate the performance and flexibility of these ITF structures. The ITF design technique can be used to make impedance transformers that operate up to 100 GHz.

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Acknowledgements

I would like to thank my parents for their support, encouragement, and faith throughout my education. I would like to express my gratitude to my supervisor, Dr. Nicolas A.F. Jaeger, for suggesting this project, and to Dr. Nicolas A.F. Jaeger and Dr. Lukas Chrostowski for providing continual guidance and support during my research. My thanks extend to those individuals in the Electrical Engineering department who have helped me during my research.

I would like to also acknowledge the support of the Natural Sciences and Engineering Research Council (NSERC) of Canada.

Based on the work of this thesis, the following manuscript has been submitted to for publication:

[1] Xia Yao, Nicolas A. F. Jaeger, "Ultra Wideband CPW Based Impedance Transformer with Capacitive Fins"

Chapter 1

Introduction

1.1 Motivation for Designing Ultra Wideband Impedance Transformer

Impedance transformers are important components at millimetre wave frequencies and they are typically used to reduce reflections between mismatched loads for cleaner signal transfer and higher bit rates. The growing demand for channel transmission capacity in the telecommunications industry has lead to a on-going interest in the development of millimetre wave electronic devices. In 2008, Dr. Lukas Chrostowski and his research group at the Electrical Engineering Department at the University of British Columbia proposed the design of a high-speed transistor-VCSEL (Vertical Cavity Surface Emitting Laser) on a GaAs substrate, suitable for optical communications with modulation frequencies approaching 100 GHz. In order to complement Dr. Lukas Chrostowski's research, we began investigating the development of on-chip impedance transformers that are capable of matching the impedance of the input terminals of the transistor-VCSEL to the electronic driver for frequencies as high as 100 GHz. Since the exact impedance value of the transistor-VCSEL is unknown during the time of this research, our design goal is to achieve an impedance matching range as wide as possible. In addition, our impedance transformer can be used to match DFB laser diode (e.g. VCSEL has an input impedance of 30~70 Ω [1], DFB laser diode has input impedance of ~ 10 Ω [2]).

Traditional impedance matching circuits include lumped LC networks and transmission line transformers. Lumped LC networks (such as single stub, double stub, capacitors, and inductors) can be used to match impedances at a single frequency. With the advent of photolithography, the fabrication of lumped elements could be realized for use at frequencies up

to ~ 60 GHz [3]. Impedance matching circuits designed using lumped elements typically require less on-chip real-estate than transmission line transformers, but have very limited operating bandwidths. In many cases, it is necessary to keep the reflection coefficient below a specified value over a given frequency band [4]. This can be achieved by using transmission line impedance transformers such as multisection quarter-wave transformers, chebyshev transformer, and exponentially tapered transformers. Tapered impedance transformers offer the widest operating bandwidths but at a cost of increased device lengths. Hence, it would be beneficial if the size of transmission line transformers can be reduced.

In recent years, attractive impedance transformers, based on microstrip and coupled transmission lines, have been demonstrated [5]-[7]. These proposed impedance transformers operate below 5 GHz and are several centimetres long. Hence, they are not suitable for MMIC applications. In [8], a tapered slotline impedance transformer is designed to match 50 Ω to 480 Ω on aluminium-nitride substrate. This impedance transformer is able to achieve an operating frequency range from 4 to 18 GHz. However, the actual design approach and the electrode dimensions are not discussed in the paper.

Miniaturized impedance matching circuits utilizing meandered coplanar waveguide (CPW) were demonstrated in [9] and [10] for MMIC wireless RF front-end applications. In these structures, the λ/4 CPW transmission lines are folded together to achieve size reduction. However, these impedance transformers have limited operating bandwidths and the impedance matching ranges of these devices were not explored. In [11], slow-wave electrodes in the form of interdigitated stubs are used to design CPW, 4-section quarter-wave impedance transformers, and RF shorts. The slow-wave design approach is able to shorten the length of the devices. In particular, by utilizing capacitive loading structures, the 4-section quarter-wave impedance

transformer is able to achieve a length reduction of 80%. However, this impedance transformer has a limited operating bandwidth.

In this thesis, we focus on developing Coplanar Waveguide (CPW) based impedance transformers on GaAs substrate to match the port impedances of three-terminal devices. Initially, we investigate the device characteristics of traditional transmission line impedance transformers, such as triangularly tapered transformer and exponentially tapered transformers. Then, we show that we can improve the performance of conventional tapered impedance transformers by adopting a slow-wave electrode design approach. Namely, one can change the geometry of the capacitive loading fins to change the impedance along the length of the CPW line. The added capacitance is able to expand the impedance matching range and the operating bandwidth of the impedance transformer. This design approach makes matching to low impedance devices possible and is able to shorten the device length such that on-chip real-estate savings can be realized.

1.2 Organization of this Thesis

This thesis is entirely based on computer simulation. In addition to this introductory chapter, background theory on how to design CPW lines, traditional tapered impedance transformers, slow-wave electrodes, and impedance transformers with fins is provided in Chapter 2. In Chapter 3, simulation methods are provided to verify our design approach. Simulation results that demonstrate the behaviour of various types of devices over various impedance matching ranges are presented. Chapter 4 comprises a summary of the work, major conclusions and suggestions for future research.

Chapter 2

Impedance Transformer Theoretical Analysis

2.1 Introduction

In this chapter, background theory is provided on designing impedance transformers. In section 2.2, methods for computing the characteristic impedance of CPW and designing the desirable microwave propagation modes are given. In section 2.3, conventional impedance transformers and their design parameters are reviewed. In section 2.4, slow-wave electrode theory, on which this thesis is based, is introduced. Finally, in section 2.5, the concept of using fins to improve the performance of impedance transformers is presented.

2.2 Coplanar Waveguide Design

As discussed in Chapter 1, our impedance transformer is designed to match the output impedance of the source, i.e., the electronic driver to the input impedance of a transistor-VCSEL on GaAs substrate. The transistor-VCSEL has three input terminals, namely the collector, the base, and the emitter. Two of the three terminals will be grounded and one will be excited by the high speed microwave signal. Hence, the impedance transformer should consist of three metal traces. The center metal trace carries the high frequency signal and the two outer conductors are grounded. This impedance transformer topology resembles the basic structure of a coplanar waveguide (CPW), as shown in Figure 2.1.

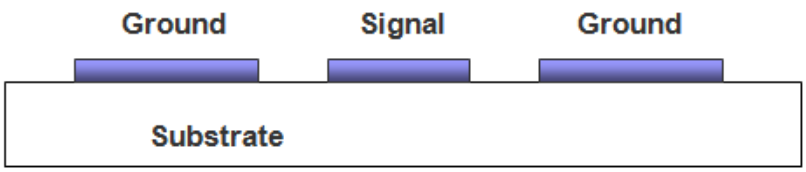

Figure 2.1 Typical CPW structure

Before designing the impedance transformer, we will first analyze the behaviour of the CPW line, i.e., determine the characteristic impedance and the propagation modes of the CPW line, as explained in the following sections.

2.2.1 Characteristic Impedance

The characteristic impedance of the CPW line Z_o can be described by the following formula [12]

$$Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.1}$$

where R is the resistance per unit length along the line, L is the inductance per unit length along the line, G is the conductance per unit length shunting the line, and C is the capacitance per unit length shunting the line. At gigahertz frequencies, equation 2.1 can be simplified to

$$Z_o = \sqrt{\frac{L}{C}} \tag{2.2}$$

This formula indicates that Z_o is inversely proportional to the square root of the capacitance per unit length of the CPW line. Capacitance exits between the center electrode and the two grounded outer conductors. When the substrate is conductor backed, capacitance also exists between the center electrode and the back side conductor. One can increase the impedance of the

line by choosing a lower dielectric constant material as the substrate, by increasing the thickness of the substrate, and by narrowing the width of the center electrode.

For conventional coplanar waveguide on a dielectric substrate of finite thickness, the approximate impedance value of the CPW line can be computed using readily available formulas as follows [13]

$$Z_o = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \frac{K(k')}{K(k)} (ohms) \tag{2.3}$$

$$k = \frac{W}{W + 2G} \tag{2.4}$$

$$k' = \sqrt{1 - k^2} \tag{2.5}$$

$$K(k) = \int_0^1 \frac{dt}{\sqrt{(1 - t^2)(1 - k^2 t^2)}} \tag{2.6}$$

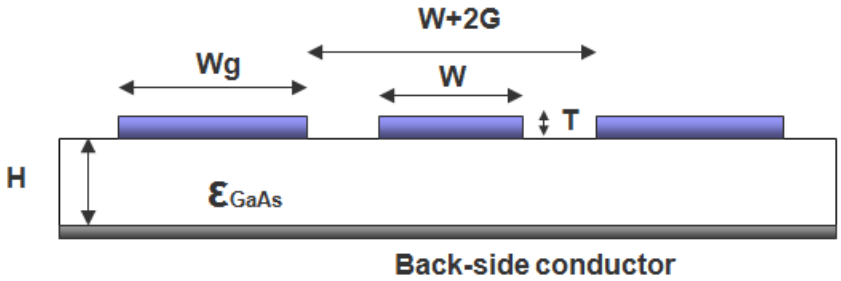

Figure 2.2 Cross section of CPW line

where W is the width of the center electrode, G is the gap between the center electrode and a ground electrode, *K(k)* is the complete elliptic integral of the first kind, and ε_{eff} is the effective microwave permittivity.

For standard coplanar waveguide, the effective microwave permittivity ε_{eff} is a function of frequency, and can be described by

$$\varepsilon_{eff} = \left(\frac{c}{v_p(f)}\right)^2 \tag{2.7}$$

where c is the velocity of light in free space, and v_p is the propagation speed of the microwave. For conductor-backed CPW, at low frequencies, when H is big and G is small, we can assume that half of the electric field lines of the CPW are in the air and half of the electric field lines are in the GaAs substrate. Thus, ε_{eff} can be computed by

$$\varepsilon_{eff} \approx \frac{\varepsilon_{GaAs} + \varepsilon_{air}}{2} = 6.95 \tag{2.8}$$

As frequency increases towards infinity, the value of ε_{eff} rises towards $\varepsilon_{GaAs} \approx 12.9$ [14]. As shown in Figure 2.3, the microwave phase velocity on GaAs does not change significantly from 1 to 100 GHz.

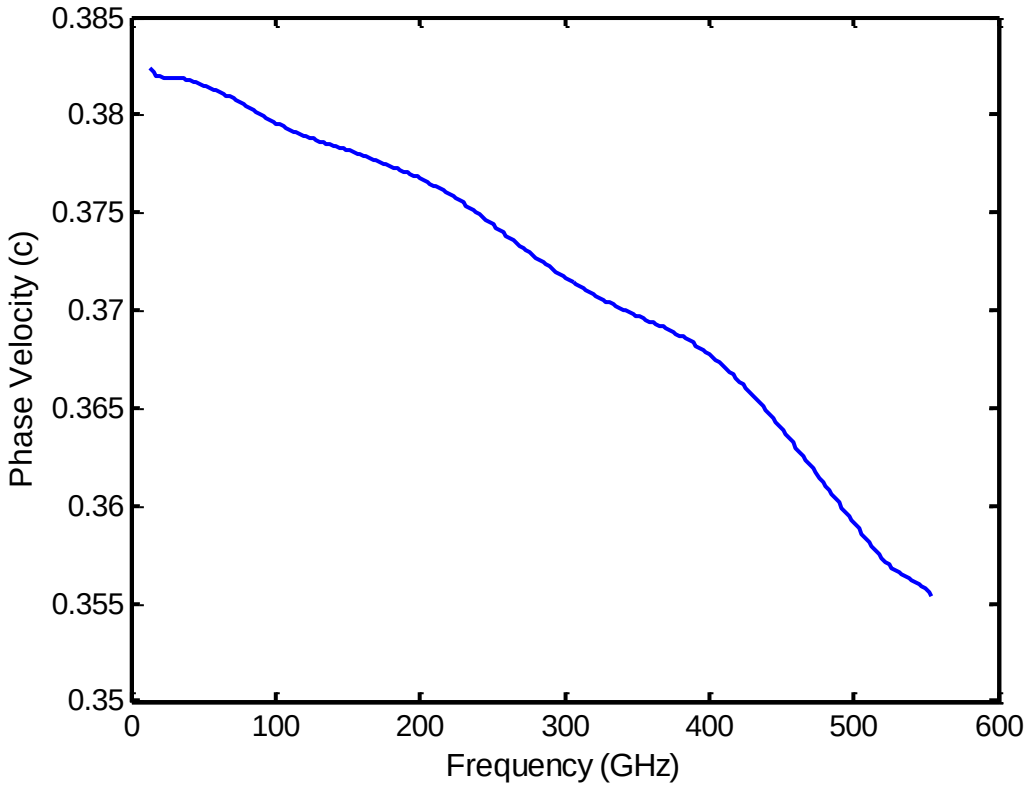

Figure 2.3 CPW microwave phase velocity on GaAs substrate [15]

In our simulations, we assume ε_{eff} stays relatively constant at 6.95 across the entire 1 to 100 GHz simulation range. The effective microwave index n_{eff} can be computed by

$$n_{eff} \approx \sqrt{\frac{\varepsilon_{GaAs} + \varepsilon_{air}}{2}} = 2.63 \tag{2.9}$$

When the structure of the CPW line changes (multiple dielectric layers are used, or the height of the substrate layer changes, or metal enclosure is used, or the electrode geometry becomes asymmetric, or the metal traces of the CPW line are not on the same dielectric layer), different formulas should be used to compute the characteristic impedance of the CPW line [16]. In general, these formulas are derived by first analyzing of the capacitance of the CPW structure,

and then using curve-fitting techniques to adjust parameters in the formula to fit experimental data. Most of these formulas can only be used for specific structure types. As a result, the use of formulas to compute the impedance values of the CPW line is limited. When the shape of the metal traces becomes irregular, i.e. when fins and pads are used, no formula can be used to compute the impedance of the line. In our design process, the impedance values of the CPW lines are computed using SONNET® V.12. This program generates reliable impedance values for any CPW structure across the 1 to 100 GHz frequency range.

2.2.2 Propagation Modes and Design Parameters

There are infinite numbers of possible electrode dimensions that one can use to design the CPW line such that one of the modes will see a specific line impedance, i.e., 50 Ω. For example, one could increase the width of the center electrode (W) and the size of the gap (G) at the same time to maintain the same impedance value of the CPW line for the coplanar mode. When designing the CPW line, one should also consider the substrate landscape usage, and more importantly, all of the modes supported by the CPW line.

The dimensions of the CPW should follow strict design guidelines to ensure that power does not couple into any undesired microwave modes in the frequency range of interest. There are four possible types of modes for a CPW line. These types of modes are the microstrip modes, the coplanar modes, the surface wave parallel plate modes, and the slotline modes [17]-[18]. Here, given the dimensions used, we can limit our discussion to the fundamental mode of each type. Different types of CPW propagation modes are shown in Figure 2.4.

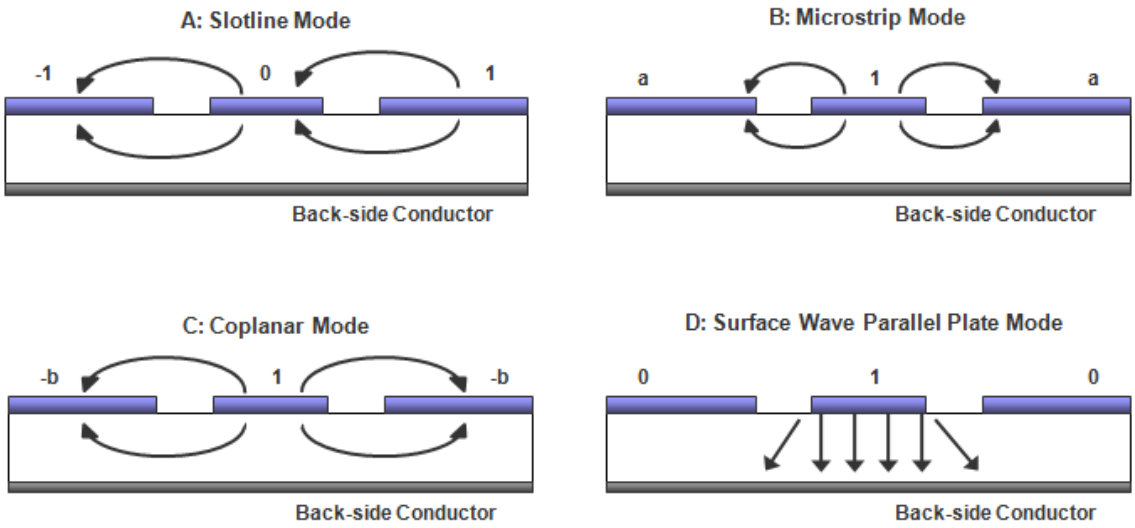

Figure 2.4 CPW propagation modes, A: slotline mode, B: microstrip mode, C: coplanar mode, D: surface wave parallel plate mode

When the CPW is excited with a signal on the center conductor and the two side conductors are at zero potential (0 1 0), the excitation is a combination of the microstrip mode (*a* 1 *a*) and the coplanar mode (*-b* 1 *-b*), as shown in equation 2.10.

$$\begin{pmatrix} 0 \\ 1 \\ 0 \end{pmatrix} = \frac{1}{(a+b)} \left[b \cdot \begin{pmatrix} a \\ 1 \\ a \end{pmatrix} + a \cdot \begin{pmatrix} -b \\ 1 \\ -b \end{pmatrix} \right] \tag{2.10}$$

The values of *a* and *b* are both functions of the physical dimensions of the line. In general, *a* does not equal *b* and the phase velocity of the two modes are different, resulting in finite potentials appearing on the outer ground conductors. The width of the ground conductors should be chosen to be wider than the spacing between them (W_g > W+2G) such that the value of *a* approaches 1 and the value of *b* approaches 0. This makes the coplanar mode approach the excitation mode (0 1 0), which is the desired propagation mode of the line.

The surface wave parallel plate mode is highly undesirable. This mode arises due to the finite thickness of the substrate and the back-side conductor. When power couples into the surface wave parallel plate mode, significant power loss occurs. To suppress this mode, one can confine the dimension of W+2G to be less than H/3 (even slight violation of this design rule can lead to sharp resonance spikes in the S21 plot) [17]-[18].

Another unwanted propagation mode is the slotline mode. This mode comes with the three conductor nature of the CPW line. For this propagation mode, the three unconnected conductors are at different potentials and the direction of the electric field in one of the slots of the CPW is reversed as compared to the coplanar mode. The center conductor sits at zero potential, with one of the outer conductor carrying a positive potential and the other outer conductor carrying the negative potential, represented by (-1 0 1). In practice, this propagation mode can be suppressed by connecting the two ground planes. For MMIC circuits, this could be achieved by using an airbridge. However, adding an airbridge will only alter the characteristics of impedance transformer due to the capacitance it forms with surrounding structures. Moreover, when symmetrical excitation (0 1 0) is used, power is unlikely to couple into the slotline mode. As a result, airbridges are not used in our impedance transformer designs.

In our design process, we found that the size of W+2G plays the most critical role in setting the microwave propagation modes. Upon knowing all the design criteria, one can choose the smallest possible W+2G to suppress, or even eliminate, all the unwanted resonance spikes in the S21 plots. By following the above design guidelines, the symmetrical excitation (0 1 0) only launch the coplanar mode.

2.3 Different Types of Impedance Transformers

For high frequency electronic circuits, maximum possible signal energy should be transferred from the source to the load. In other words, the signal should propagate in a forward direction with negligible reflection. Reflected signals not only reduce the transmitted power but also deteriorate the signal quality. Impedance transformers help maintain a high energy transfer level and reduce the amount of reflections between the source and the load.

In general, impedance transformers can be classified into three categories, namely single-section impedance transformers, multi-section impedance transformers, and tapered impedance transformers. Single-section impedance transformers, such as single-section quarter-wave transformers, have very narrow operating bandwidths. Multi-section impedance transformers, such as binomial transformers and chebyshev transformers, are bandpass devices. Tapered impedance transformers, such as triangular tapered transformers, exponentially tapered transformers, and Klopfenstein tapered transformers, are high pass devices and have the widest operating bandwidths. For our design purpose, which is to achieve impedance transformation up to 100 GHz, we will focus on designing tapered impedance transformers.

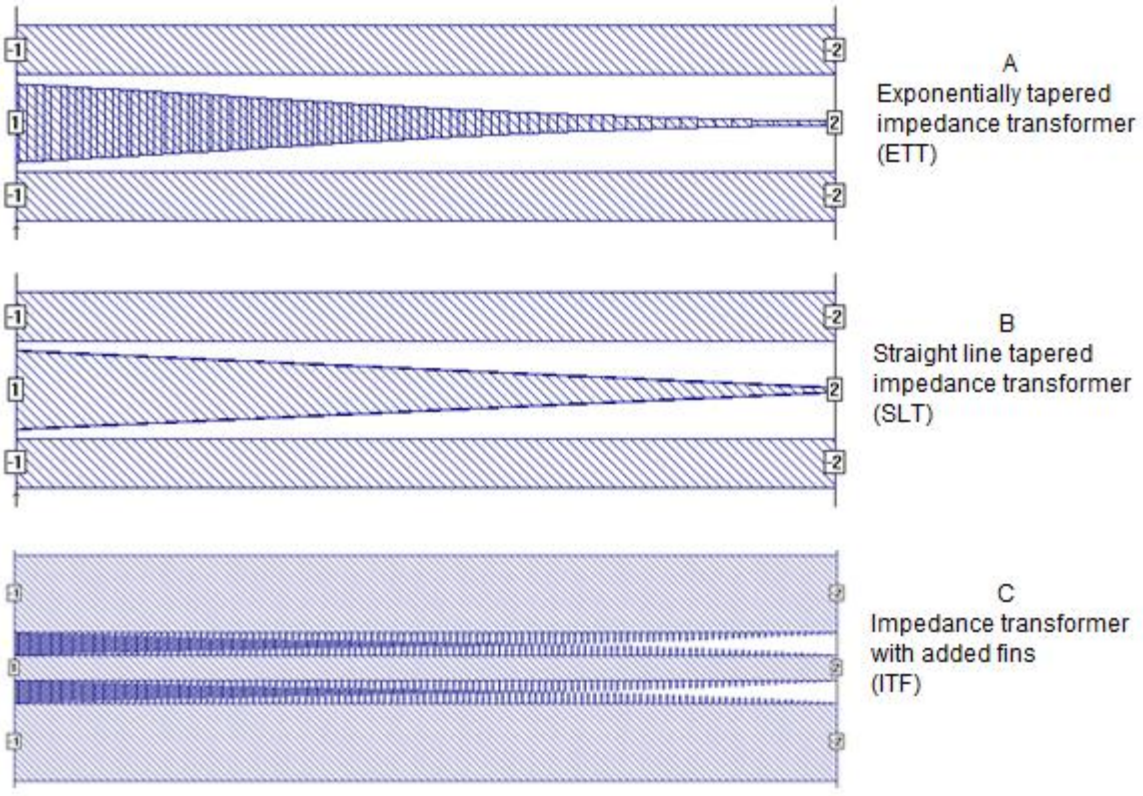

Figure 2.5 Three types of simulated impedance transformers, ETT, SLT, and ITF

In Chapter 2, the theoretical model of triangularly tapered impedance transformer (TTT) and exponentially tapered impedance transformer (ETT) are studied. In Chapter 3, we mainly simulated three types of tapered impedance transformers, namely the exponentially tapered impedance transformer (ETT), the straight line tapered impedance transformer (SLT), and impedance transformers with added fins (ITF). The typical layouts of the simulated structures are shown in Figure 2.5. It should be noticed that SLTs are different from TTTs, although often times SLTs have triangular shape.

2.4 Triangular Tapered and Exponentially Tapered Impedance Transformers

It is desirable to have the least amount of reflection at the input port of the impedance transformer while achieving the widest operating bandwidth. For these design purposes, tapered impedance transformers such as triangular tapered transformer (TTT) and exponentially tapered transformer (ETT) are considered. Compared to TTTs and ETTs, Klopfenstein tapered transformers are mathematically complicated to design and they do not improve the bandwidth or transmission coefficient in significant ways. Therefore, we did not analyze Klopfenstein tapered transformers.

For TTT, $\frac{d}{dx}(\ln Z(x))$ is a triangular function [19], where $Z(x)$ is the impedance along the length of the impedance transformer, and x is the position along the length of the impedance transformer. The total reflection coefficient seen at the input port of TTT can be expressed as

$$\Gamma_{in} = \frac{1}{2} e^{-j\beta L} \ln R_{load} [\frac{\sin(\beta L/2)}{\beta L/2}]^2 \tag{2.11}$$

$$\beta = \frac{2\pi n_{eff}}{\lambda} \tag{2.12}$$

$$n_{eff} \approx \sqrt{\frac{\varepsilon_{GaAs} + \varepsilon_{air}}{2}} = 2.63 \tag{2.13}$$

where L is the length of the impedance transformer and λ is the operating wavelength of the microwave signal.

For ETT, $\frac{d}{dx}(\ln Z(x))$ is a constant. The impedance along the length the transformer varies exponentially according to the following relationship

$$Z_{Load} = Z_{in} e^{c_1 L} \rightarrow c_1 = \frac{1}{L} \ln \frac{Z_{Load}}{Z_{in}} \tag{2.14}$$

where L is the length of the impedance transformer and c_1 is a coefficient. Once Z_{load}, Z_{in}, and L are known, c_1 can be first computed and then substituted back into the above formula to compute the impedance values along the length of the device. The total reflection coefficient seen at the input port of ETT can be expressed as

$$\Gamma_{in} = \frac{\sin(\beta L)}{\beta L} \tag{2.15}$$

In Figure 2.6, normalized total reflection coefficients versus βL for TTT and ETT are plotted. It can be seen that both types of transformer behave like high pass filters (low reflection coefficient leads to high transmission power).

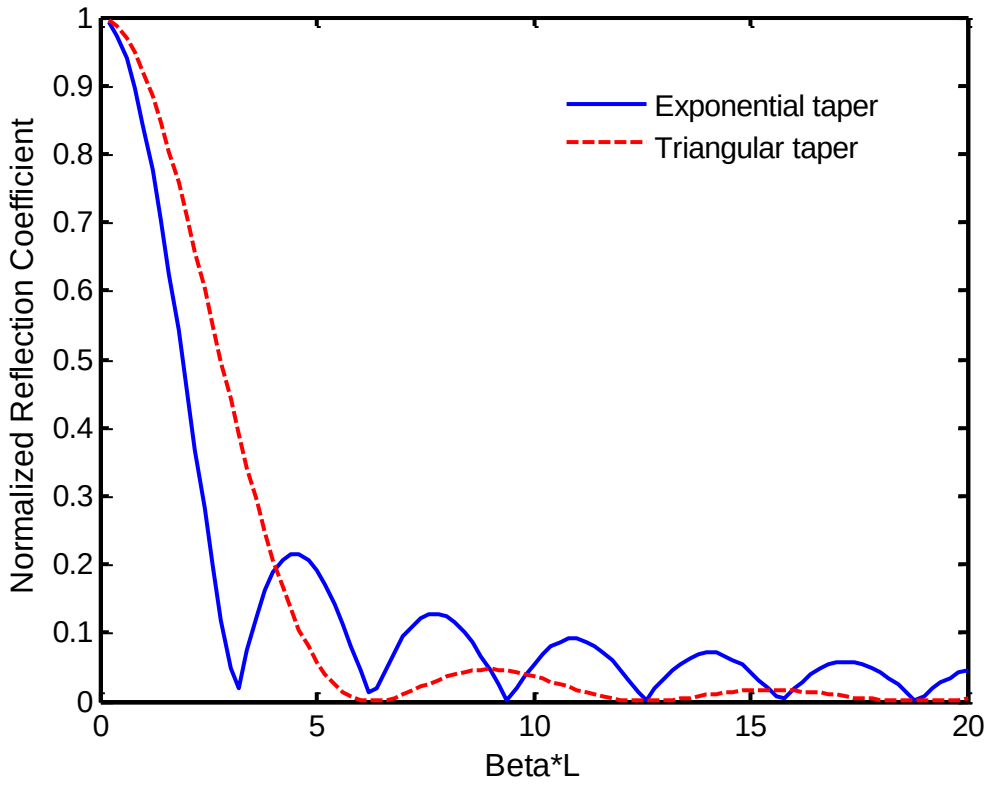

Figure 2.6 Normalized Γ_{in} versus βL for TTT and ETT

The total reflection coefficient Γ_{in} is greatest at low frequencies. As frequency increases, Γ_{in} drops dramatically and reaches the first null at π for ETT, and 2π for TTT. The operating frequency at which Γ_{in} reach the first null is called the 'cutoff frequency' of the impedance transformer. The cutoff frequency of ETT and TTT can be expressed as $f_{cutoffETT} = \frac{c}{2 * L * n_{eff}}$ and $f_{cutoffTTT} = \frac{c}{L * n_{eff}}$ respectively. Nominally, the impedance transformer starts working at the cutoff frequency. Therefore, in order to widen the operating bandwidth, one always wants to

decrease the cutoff frequency. To do so, the designer can increase n_{eff} or L. Since the cutoff frequency of ETT is theoretically half of that of TTT for the same device length, we will limit our discussion to ETT in the following sections.

2.5 Design Parameters of ETT

As previously stated, n_{eff} and L determine the position of the cutoff frequency (f_{cutoff}) ETT. As n_{eff} and L increases, f_{cutoff} decreases, which widens the operating bandwidth. However, increasing L also increases the overall electrode loss and the number of potential resonances (not to mention the increased real-estate usage). Therefore, the designer should always look for the optimum L for specific design criteria. Table 2.1 and Figure 2.7 illustrate the relationship between L and f_{cutoff} for ETT.

Cutoff Frequency (GHz)	ETT length (mm)
1	57.69230769
5	11.53846154
10	5.769230769
20	2.884615385
30	1.923076923
40	1.442307692
50	1.153846154
60	0.961538462
70	0.824175824
80	0.721153846

Table 2.1 ETT length L versus f_{cutoff}

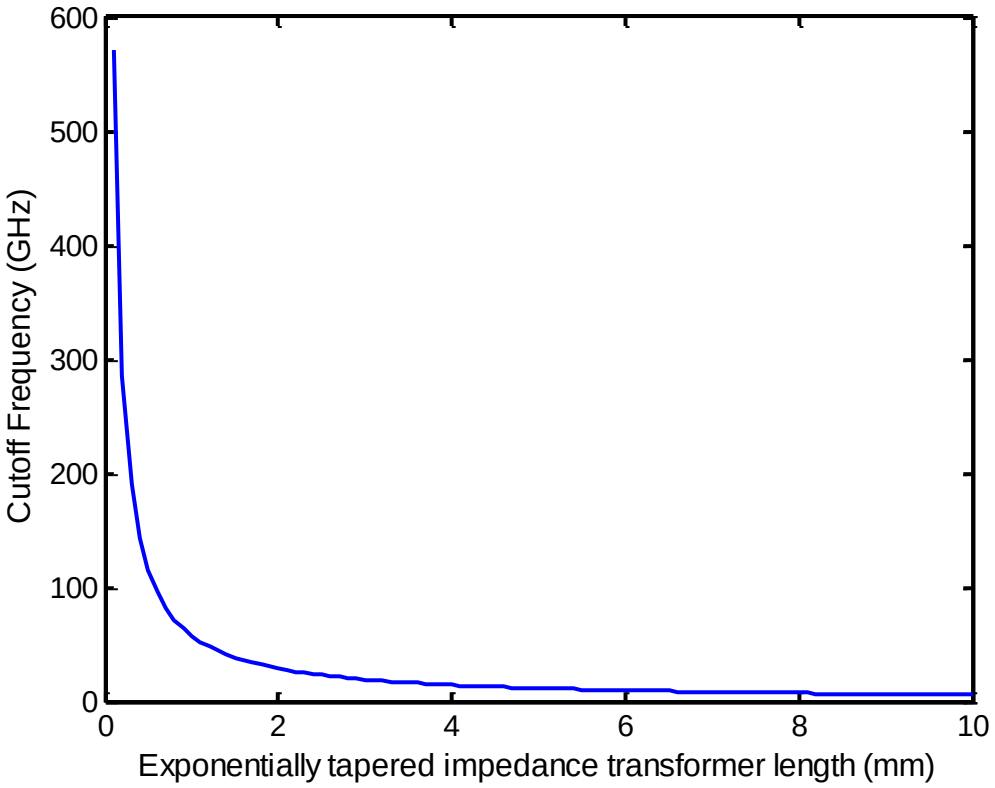

Figure 2.7 ETT length L versus f_{cutoff}

In order to limit the electrode loss of the impedance transformer to be less than 3 dB and to have the cutoff frequency below 30 GHz, L can be chosen from 2 mm to 6 mm, which positions f_{cutoff} at ~ 28.8 GHz and ~ 9.2 GHz respectively. When L is greater than 6 mm, the impedance transformer experiences too much electrode loss and too many potential resonances. On the contrary, when L is smaller than 2 mm, the cutoff frequency becomes too large which limits the operating bandwidth of the device. In our simulations, we mainly studied the device characteristics of 2 mm long devices because they offer a good balance between performance and on-chip real-estate usage.

In standard CPW, the effective microwave index n_{eff} is a fixed variable once the substrate material is chosen (for GaAs substrate, n_{eff} is fixed at ~ 2.63). In what follows, we have developed techniques to increase n_{eff} of the CPW line by adopting a slow-wave electrode design approach. This allows us to reduce the length of the impedance transformer, lower the minimum impedance that can be matched, and significantly lower the cutoff frequency.

2.6 Slow-wave Electrode Theory

The slow-wave electrodes on which this work is based were designed to match the propagation speed of a microwave to that of light in an electro-optic modulator [20]. In them, capacitive elements in the form of fins were added to coplanar strips. In this work, we employ interdigitated capacitive loading fins in the CPW structure. The addition of the capacitive elements to the coplanar electrodes significantly changes the capacitance per unit length while inducing negligible changes to the inductance of the line. Because $Z_o = \sqrt{\frac{L}{C}}$ and $v_{phase} = \frac{1}{\sqrt{LC}}$, increasing the capacitance of the line not only lowers the characteristic impedance but also slows down the propagation speed of the microwave.

Upon knowing the geometry of the CPW with loaded capacitive elements, the exact value of CPW line impedance Z_o and n_{eff} can be computed using SONNET® V.12. SONNET® V.12 generates a set of Y-parameters through its EM analysis which can be used to compute the impedance of the line Z_o and n_{eff} [21]. The following equations are used

$$Y_o = \pm j\sqrt{Y_{12}^2 - Y_{11}^2} \tag{2.16}$$

$$Z_o = 1/Y_o \tag{2.17}$$

$$\beta L = n\pi - j\log(-Y_{11}/Y_{12} + jY_0/Y_{12}) \tag{2.18}$$

$$v = 2\pi f/\beta \tag{2.19}$$

$$n_{eff} = c/v \tag{2.20}$$

where Y_{11} and Y_{12} are numerical results from the EM analysis, β is the complex propagation constant, L is the length of the CPW line, v is the propagation speed of the microwave and c is the speed of light.

2.7 Impedance Transformer with Added Fins

While the performance of ETT is good, we need to achieve a broader impedance matching range and wider operating bandwidth. We have developed a new type of impedance transformer (IT) loaded with fins (ITF). The concept of this new type of IT has its roots in the slow-wave electrode theory, in that adding interdigitated fins between the center and GND electrodes increases the line capacitance which in turn lowers the impedance of the line.

Therefore, instead of gradually tapering the center electrode to change the line impedance, one can gradually increase or decrease the fin capacitance of the line. Geometry-wise, ITF has a uniform width center electrode which translates to lower losses, with fins gradually growing longer on both the center and GND conductors along the length of the ITF. The low impedance end of the ITF has longer fins as compared to the high impedance end, see Figure 2.8.

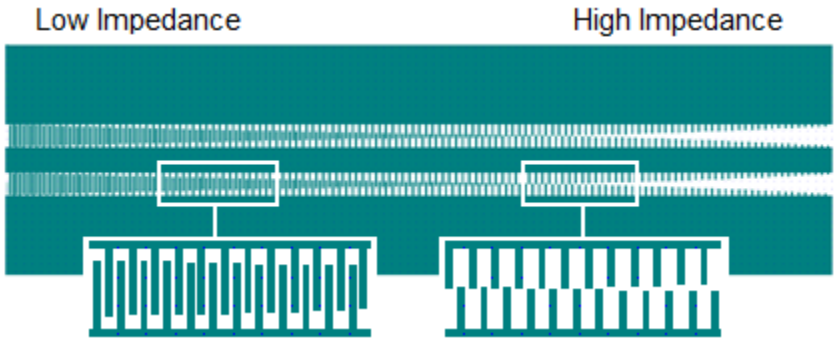

Figure 2.8 Typical ITF structure

To design ITF, one can first generate a table of impedance values corresponding to different fin geometries, namely the length and width of the fins. Then the designer can match the impedance values along the length of the ETT (or any other type of impedance transformer) to particular fin geometries to make the layout of the ITF. This process can be automated with a Matlab program.

The designer can use capacitive elements in any arbitrary shape, not necessarily restricted to the form of fins. However, we have found that using the fins is the most space-economic approach, in that the fins can expand or contract vertically (the direction perpendicular to the direction of propagation of the microwave) to increase or decrease the capacitance. This

approach also accommodates the most number of impedance sections along the length of the impedance transformer, thus providing the smoothest form of transition.

2.8 Summary

In this chapter, we have presented the background theory necessary to design transmission line based impedance transformers. The methods for computing the characteristic impedances of coplanar waveguide based transformers are presented. We also introduced design guidelines used to suppress unwanted propagation modes. The theoretical models of triangularly tapered and exponentially tapered impedance transformers are explored. We found that by increasing the effective microwave index and the length of the impedance transformer, we could widen the operating bandwidth of these devices. Next, we reviewed the slow-wave electrode theory on which this work is based. Equations that are used to convert SONNET output Y-parameters to characteristic impedance and the effective microwave index are also presented. Lastly, we introduced the concept of using impedance transformer with fins (ITF) and how the fins can be used to control the impedance along the transmission line.

Chapter 3

Numerical Simulation

3.1 Introduction

The numerical simulations of the impedance transformer structures are performed using SONNET® V.12. Its EM analysis engine applies the method of moments directly to two Maxwell's equations (Gauss's law and Ampere's law). The following is a brief summary of EM's computational procedure [22]:

- EM first subdivides, or meshes, the metal of a circuit into small subsections
- EM then takes one of the subsections and, ignoring all other subsections, calculates the voltage everywhere due to current on that one subsection (done by a 2-D FFT)
- EM repeats this process for each subsection
- The field distribution due to current is solved to determine subsection coupling
- EM places current on all subsections simultaneously and adjusts those currents such that the total voltage (due to current on all subsections) is zero wherever there is a conductor
- The current that gives zero voltage across all conductors is the solution to the problem

SONNET® V.12 relies on having the SONNET box wall to facilitate its 2-D FFT computation. Therefore, the SONNET box wall will always be in the simulation environment, acting as a metal enclosure, causing potential box resonances, or interacting with electric fields that are too close to the box walls. The designer must know where to position the box wall to minimize these effects. The SONNET box top cover can also cause potential box resonances.

However, the top cover can be set to the impedance of air, as a way of removing it from the environment. In our simulations, SONNET box resonances were not found to be significant. Most resonances were removed by proper designs of the CPW lines.

For each simulation, our SONNET project is set up as shown in Figure 3.1. The project environment consists of two layers. The top layer is air with dielectric constant of 1. The thickness of the air layer is set to 1 mm, which is sufficiently far away from the metal traces. The bottom layer is GaAs with a dielectric constant of 12.9 and a loss tangent of 0.006. The thickness of the GaAs layer is set to either 650 μm or 325 μm, based on the thicknesses of commercially available wafers. Depending on the simulation needs, the SONNET box dimensions can vary. The longitudinal direction of the box is defined as the propagation direction of the microwave signal, with the transverse direction of the box perpendicular to it.

Most of our simulated structures have three metal traces. In the SONNET simulation environment, the center electrode begins with Port1 on the box wall, and terminates with Port 2 on the opposite side of the box wall. The terminal port impedances are set to the impedance values that we have designed our impedance transformers to match. The two outer ground electrodes begin with box wall port '-1' and end at box wall port '-2'. This configuration ensures that all of the current flowing through the center electrode eventually returns via the two ground electrodes. In other words, this setup resembles the real device where the center electrode is excited with the microwave signal, and the signal's return path is the two outer ground electrodes.

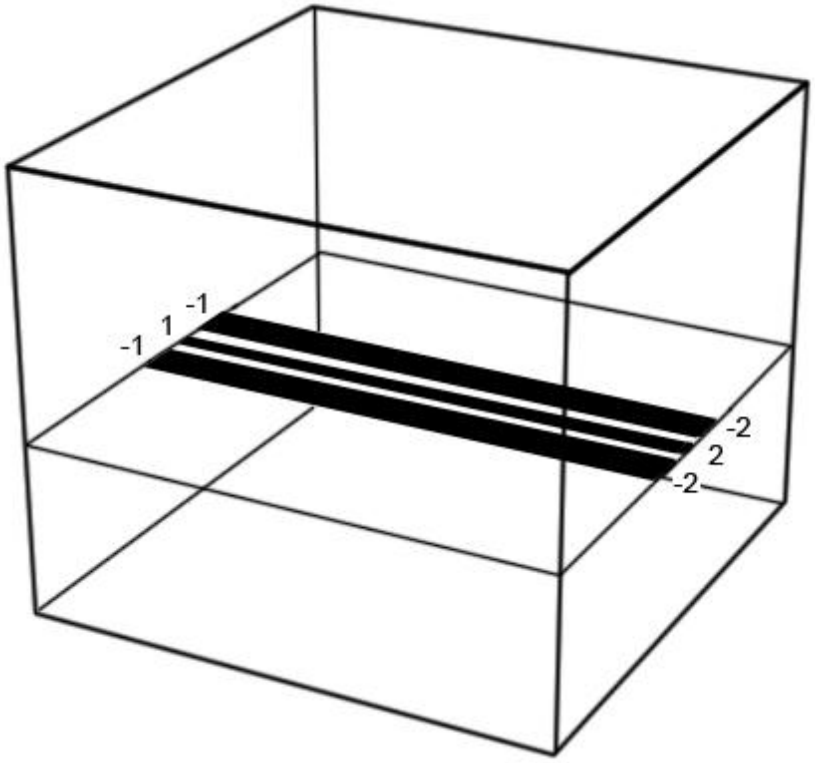

Figure 3.1 Typical SONNET project setup

The two outer electrodes should never be connected to the back-side metal plane through a via. In that case, the entire ground plane would act as a big metal plate offering multiple return paths which supports numerous unwanted propagation modes. These modes would appear as huge resonance spikes in the S21 plots.

We used two different types of conductor in our simulation, namely lossless metal and gold. The lossless metal allows us to examine the behaviour of our impedance transformers without considering metal loss. Gold is then used to determine how electrode dimensions will affect line losses. The information is combined to optimize our designs.

3.2 Generate Coplanar Waveguide Impedance Map

Our simulation strategy is to begin building and testing simple structures such as a regular CPW and determine its impedance. SONNET® V.12 EM analysis engine can compute the line impedance for a regular CPW structure. EM also allows the designer to vary the dimensions of the line in fixed steps over specified ranges to compute the line impedance for each variation. This feature allows us to fix the ground electrode dimensions, and determine the different impedance values of the line for different center electrode width. Figure 3.2 shows a 0.5 mm long CPW section, in which W+2G is 240 μm. The ground electrodes are 260 μm wide. The width of the center electrode is set to vary in 2 μm steps until the center electrode fully span the gap between the two ground electrodes (but not making contact, 1 μm space remains).

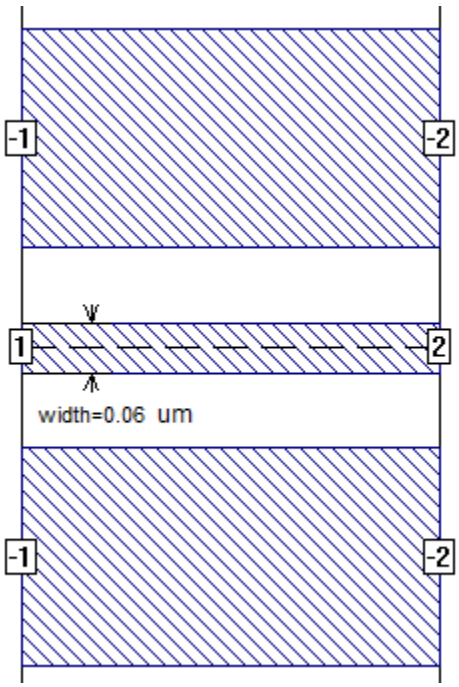

Figure 3.2 CPW center electrode width sweep

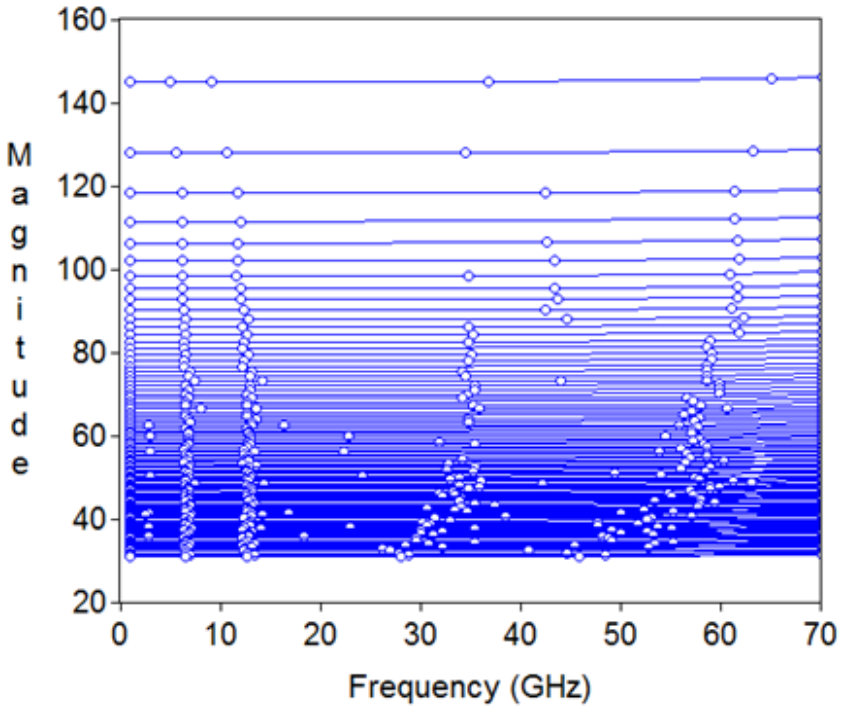

Figure 3.3 Typical impedance map of CPW line

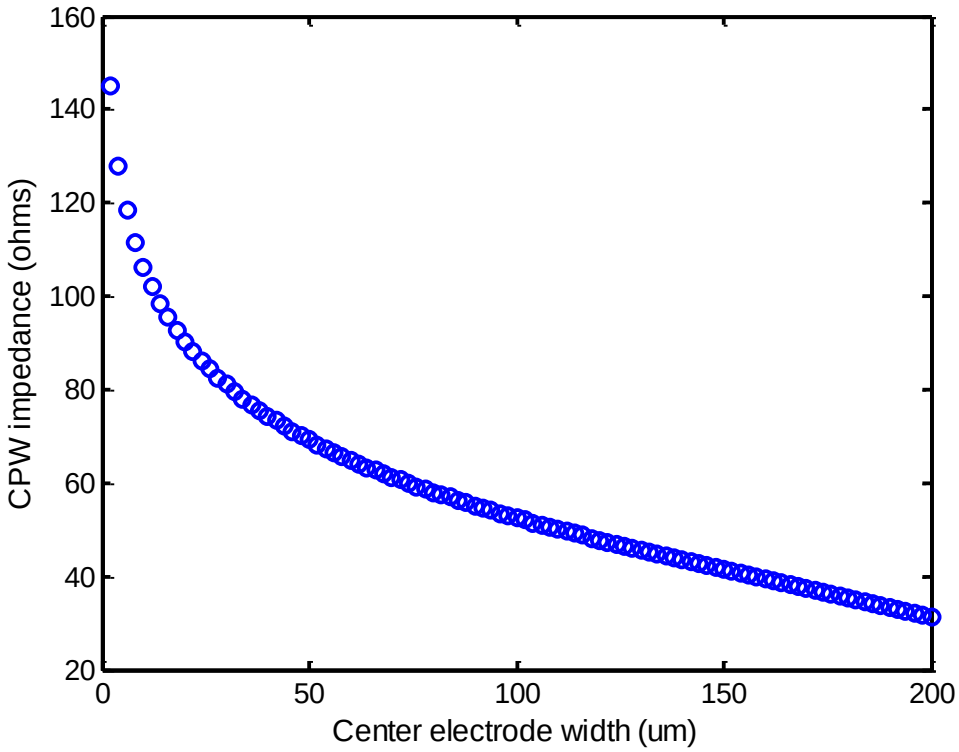

Figure 3.4 Impedance values of CPW line at 1 GHz

The scanned result is an 'impedance map', as shown in Figure 3.3. Each blue line represents the impedance values of the CPW line for a given center electrode width across 70 GHz frequency range. These values can be obtained from EM's 'Port Z_o' output. 'Port Z_o' represents the impedance of the cross section of the metal at the specified port on the SONNET box wall. Since our CPW consists of three metal traces with fixed electrode widths across the length of the box, the 'Port Z_o' values can be used as the impedance of the CPW line.

When the electrode dimensions are fixed, the impedance values of the line change as frequency changes. For example, in Figure 3.3, the impedance values of the line increase slightly as frequency rises. According to our observations, this deviation is usually less than 5%. In our simulations, we assumed that the impedance values of the line do not change significantly from 1 to 100 GHz. Hence, the impedance values at 1 GHz are used for further computation. Figure 3.4 shows the impedance values of the CPW line at 1 GHz.

3.3 Unmatched Port Impedances to the Line

For a regular CPW structure, when the impedance of Port1, Port2, and the CPW line do not match one another, the line's transmission and reflection characteristics become undesirable. Namely, the magnitude of S21 ripples, or in many cases settles at levels much lower than 1, depending on how mismatched the impedances are. A 2 mm long CPW connecting 30 Ω (Port1) and 100 Ω (Port2) is shown in Figure 3.5, in which W+2G is 260 μm. The CPW line is designed to be 50 Ω.

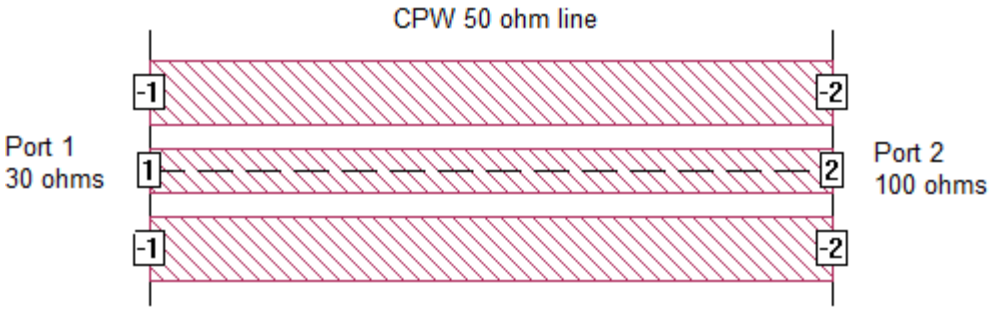

Figure 3.5 Mismatched ports and line

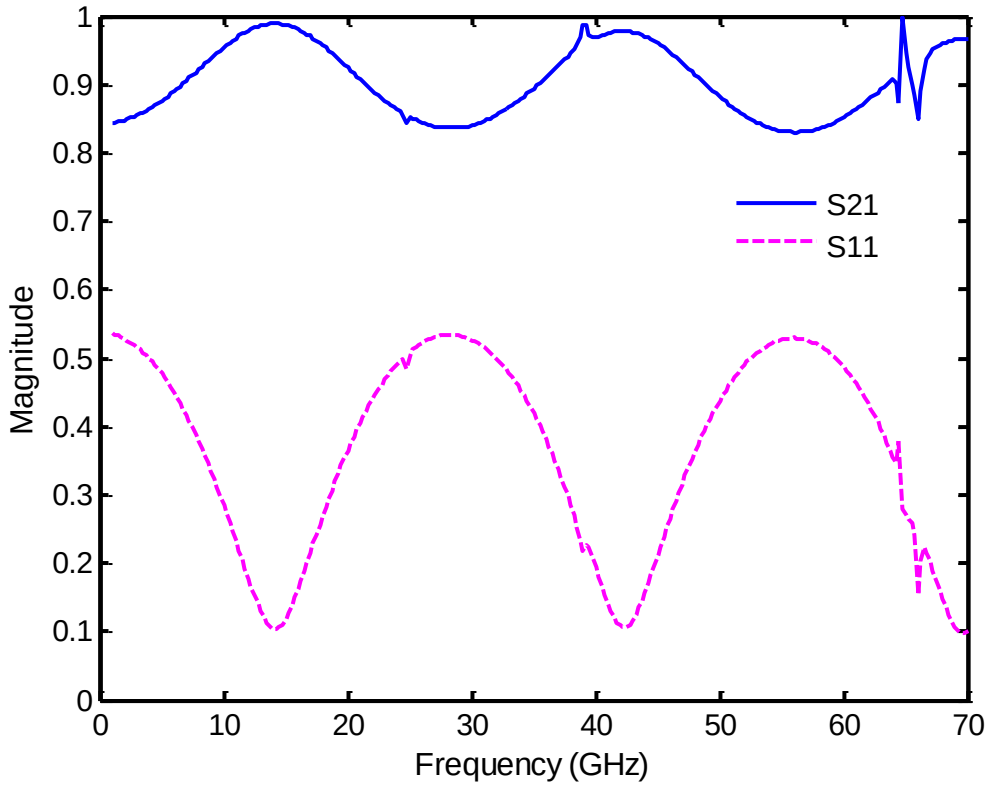

Figure 3.6 S21 and S11 response of the mismatched ports and line

In this example, S21 ripples between 0.85 and 1 as the frequency increases, as shown in Figure 3.6. There are a few noticeable resonance spikes due to poor design choices of W and G. S11 ripples between 0.5 and 0.1, which indicates a significant amount of reflection.

3.4 Matched 50 Ω Line and Ports

When the CPW line is properly designed to match both port impedances, transmission lines with desirable S21 and S11 characteristics can be made. Table 3.1 lists three CPW lines with different electrode dimensions. All three lines are designed to have characteristic impedance of 50 Ω and matched to 50 Ω ports. We assume the conductor type to be 1 μm thick gold in order to include electrode loss. All three devices are 2 mm long. The device characteristics of these CPW lines are compared in Figure 3.7.

	Z_o (Ω)	W+2G (μm)	W (μm)	W_g (μm)
CPW1	50	100	48	190
CPW2	50	170	82	190
CPW3	50	260	126	190

Table 3.1 Three different 50 Ω CPW lines and their dimensions

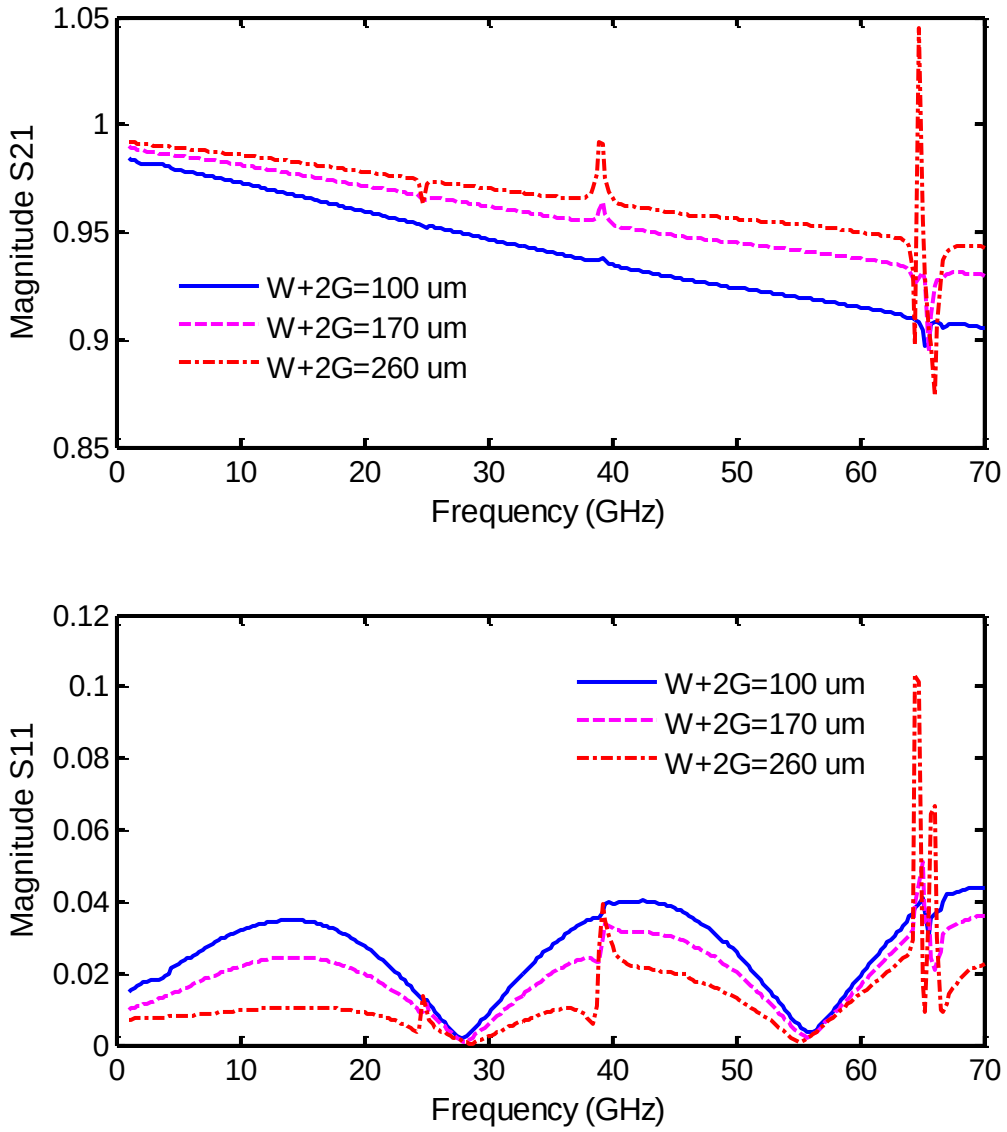

Figure 3.7 S21 and S11 responses of 50 Ω CPW lines

For CPW1, W+2G is 100 μm. Its S21 response is a straight line spanning the entire 1 to 70 GHz frequency range. The S21 level stays above 0.9 and there is no severe resonance spike. As frequency increases, the S21 level drops off gradually due to electrode loss and substrate loss. The S21 response of CPW1 is the ideal transmission line response.

For CPW2 and CPW3, W+2G is chosen to be 170 μm and 260 μm respectively. There are some noticeable resonance spikes in their S21 and S11 responses due to unwanted parallel plate surface wave modes. As W+2G increases, the resonances grow stronger, as shown in Figure 3.7.

The width of the center electrode plays a critical role in controlling electrode loss. The relationship between the center conductor width and the electrode loss at 1 GHz for a W+2G=260 μm CPW line is plotted in Figure 3.8. It is shown that when the center electrode is very narrow, the electrode loss is greatest due to current crowding. As the center electrode widens towards 116 μm (this geometry represents ~ 52 Ω), the electrode loss decreases to a minimum value of 0.0166 dB/mm. As the center electrode widens further, the outer edge of the center electrode approaches the inner edge of the ground electrode. This induces current crowding again and the CPW line loss rises towards 0.021 dB/mm.

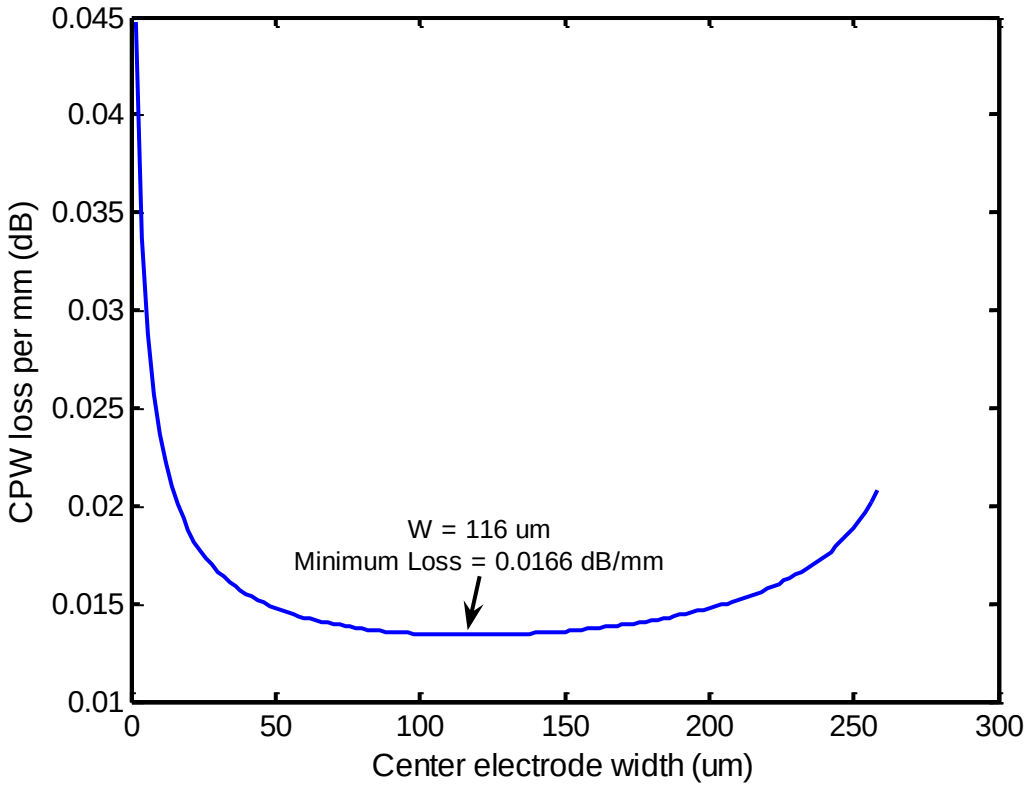

Figure 3.8 Electrode loss vs. center electrode width at 1 GHz for W+2G=260 μm CPW line

When designing a regular CPW line, it is best to first choose the dimension of W+2G to avoid unwanted resonances and then find the width of the center electrode that matches the impedance value of interest. This may not produce a CPW line with the lowest conductor loss, but it ensures that there is no unwanted resonance in the operating frequency range.

When designing an impedance transformer with fins (ITF), one can first choose W+2G to avoid unwanted resonances and then choose the center electrode width (W). The dimension of W is a trade-off between center conductor loss and the maximum amount of capacitance that can be added to the line. For example, when W is large, the center conductor loss is low. However, this leaves a smaller gap (G) in which to place the capacitive loading fins. We have found that setting the center electrode to 60 μm was a good design choice for ITFs. This leaves enough

room to add capacitive loading fins and reduces center conductor loss. We found that choosing center electrode width W to be less than 30 μm induced severe electrode loss.

Another interesting observation throughout our simulation process was that the EM analysis engine occasionally returned sharp resonant spikes with values greater than 1. Such values are not realistic. Upon further investigation, we found in [23] that these peaks are:

"Remnants of the poles in the Green's function used in the Sonnet Suites and correspond to the sequential entry of the surface-wave modes. Although the poles are removed one by one in the final results, some oscillations remain and are an unavoidable artefact".

In short, regardless of which way the resonance spikes point, either up or down, the spikes indicate significant power loss at particular frequencies due to unwanted microwave modes. As a result, the designer can revise the impedance transformer design.

3.5 Metal Thickness

We have used gold in our simulations to analyze electrode loss, primarily because we would later fabricate the devices using gold as the deposition material. Our goal is find a suitable gold thickness for the fabrication. A 0.5 mm long section of 50 Ω CPW line matched to 50 Ω ports at both ends was used to determine the electrode loss per millimetre. Different gold thicknesses are modeled, and the electrode loss across the entire length of the line is extracted from SONNET output[1].

[1] The EM analysis output 'GMAX' is used to determine line loss.

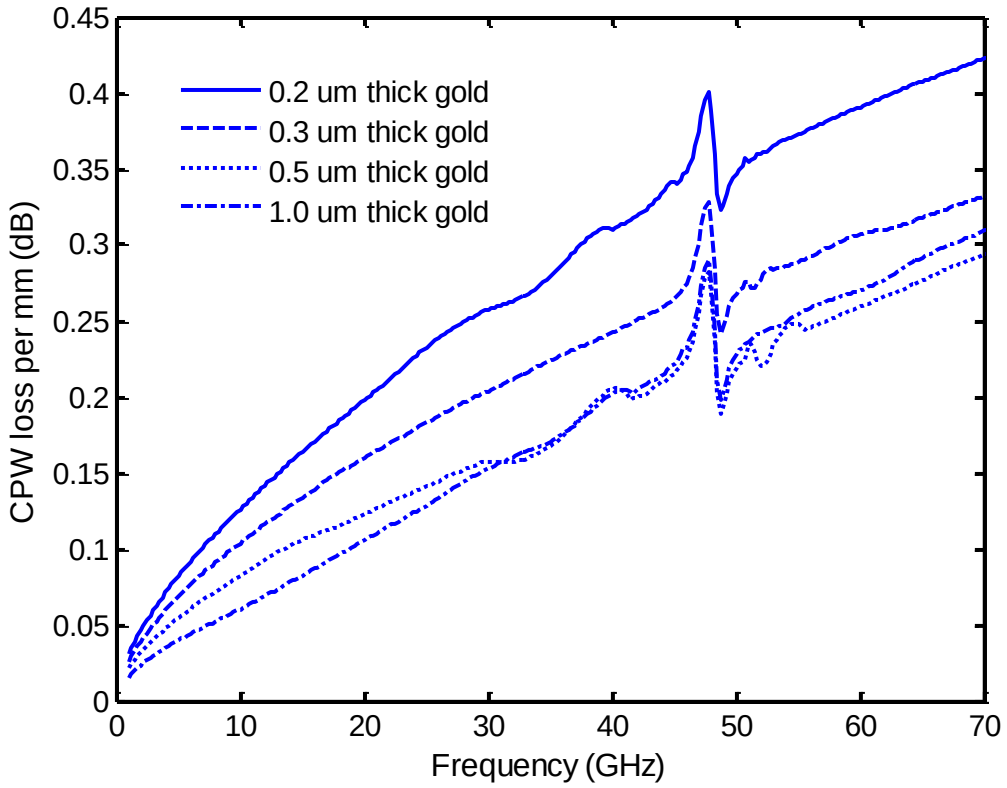

Figure 3.9 Metal loss for different thicknesses

As shown in Figure 3.9, as the thickness of the gold electrode increases from 0.2 μm to 1 μm, the electrode loss decreased by 0.12 dB/mm at 60 GHz. Increasing the thickness of the metal beyond 1 μm does not lower the metal loss any further. Therefore, we concluded that 1 μm is a good design choice for metal thickness.

3.6 Exponentially Tapered (ETT) and Straight Line Tapered (SLT) Impedance Transformers

In this section, we will present some of the simulation results for conventional tapered impedance transformers and see how the device lengths and the size of the SONNET box affect

the performance of the devices. In particular, we will analyze the behaviours of ETTs and SLTs. SLTs are the tapered impedance transformers that we in fact used in many of our simulations due to their ease of layout. To design an SLT, the widths of the ends of the center electrode are chosen so that the impedance values of the ends of the line match the port impedances of the source and the load. The two ends are then geometrically connected in a straight line fashion to form the taper. A typical SLT structure is illustrated in Figure 3.10. Later, we will show that the behaviours of SLTs and ETTs are nearly identical.

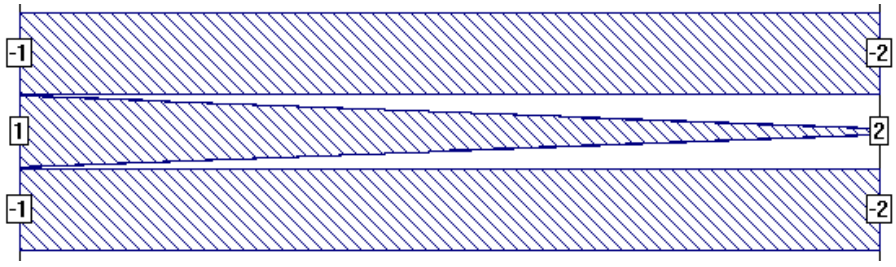

Figure 3.10 Typical SLT structure

3.6.1 Device Characteristics of ETT, SLT and Mismatched CPW

To examine the behaviour of conventional tapered impedance transformers, we analyzed three devices, namely a regular CPW line, an ETT, and a SLT. Figure 3.11 A, B, and C illustrates these three devices respectively.

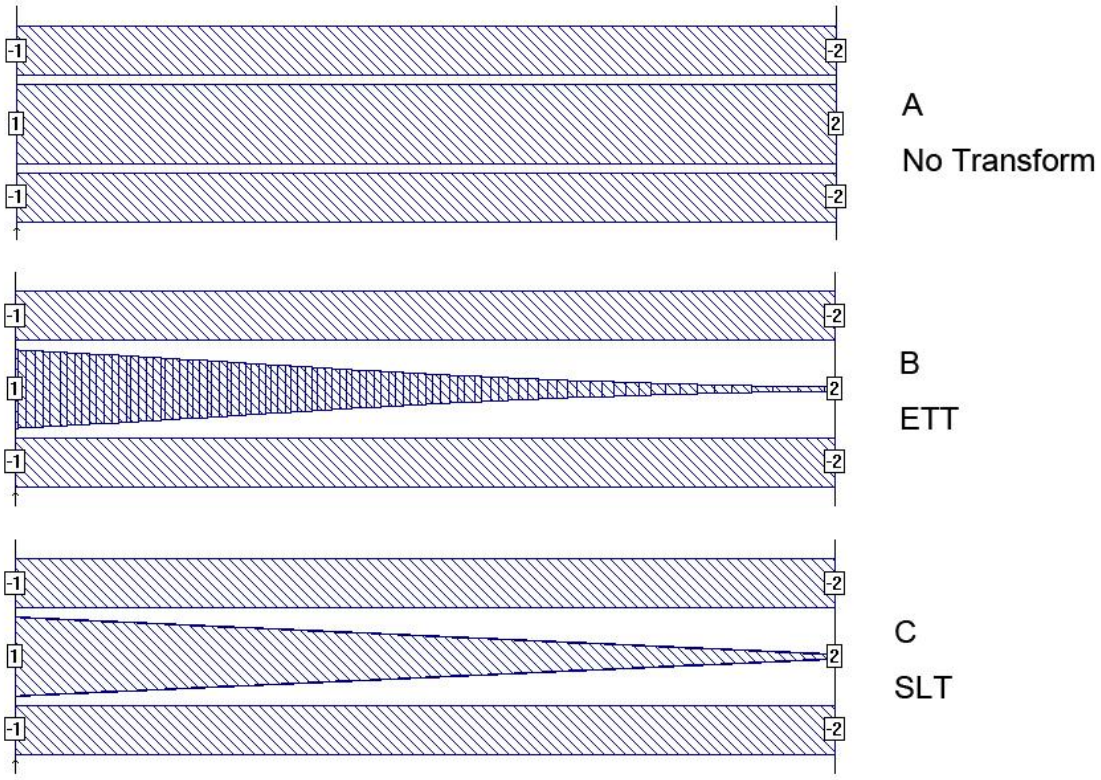

Figure 3.11 Simulation setup to test ETT, SLT, and unmatched CPW line

All three structures are placed in 2 mm long and 1 mm wide SONNET box. All three devices are 2 mm long. The substrates are 650 μm thick GaAs. The metal types are set to lossless to exclude the effect of conductor loss. For all three setups, Port1 is set to 30 Ω and Port2 is set to 100 Ω, establishing a mismatched port impedance situation. For the setup in Figure 3.11 A, the CPW line impedance is designed to be 30 Ω, which is matched to Port1 but not to Port2. An exponentially tapered impedance transformer (ETT) is shown in Figure 3.11 B, where the center electrode is exponentially tapered from 30 Ω to 100 Ω. Figure 3.11 C illustrates a straight line tapered impedance transformer (SLT), tapered from 30 Ω to 100 Ω. The device characteristics for these three structures are shown in Figure 3.12.

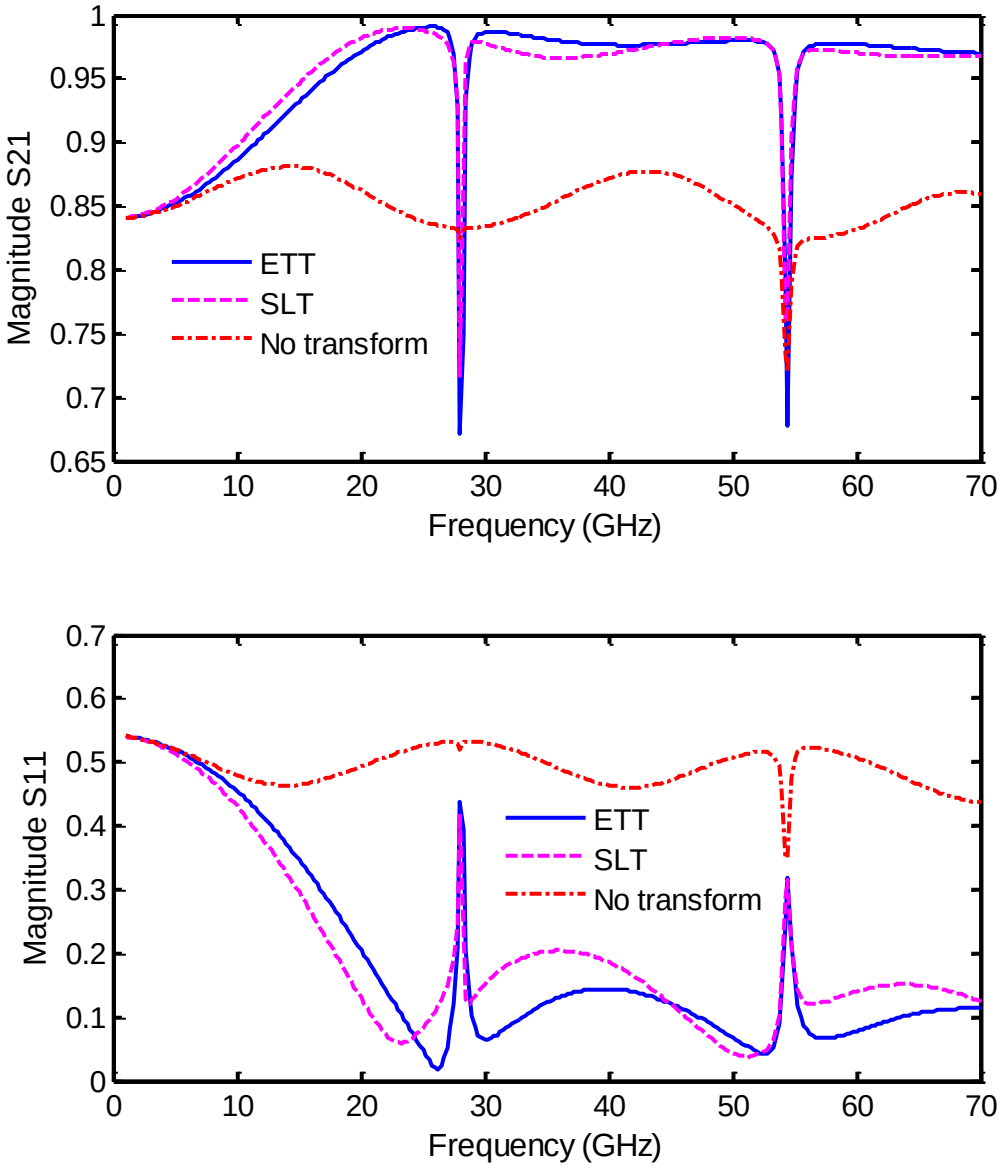

Figure 3.12 S21 characteristics for ETT, SLT and mismatched CPW line

The values of S21 and S11 at low frequencies (such as 1 GHz) can be estimated by DC analysis as $S11 = \frac{100\Omega - 30\Omega}{100\Omega + 30\Omega} = 0.54$ and $S21 = \sqrt{1 - S11^2} = 0.84$. As shown in Figure 3.12, when the CPW line is mismatched at Port2, S21 ripples around 0.84 across the simulated

frequency range. In other words, only approximately 0.84*0.84=70% of the power is delivered from Port1 to Port2. ETT and SLT improve the transmission response significantly. As expected, for tapered impedance transformers, S21 is 0.84 at 1 GHz. As the frequency increases towards the cutoff frequency (~ 23 GHz for SLT and ~ 28 GHz for ETT), the values of S21 rise towards 1. Upon reaching the cutoff frequency, S21 stays more or less at a constant level near 1, indicating the establishment of maximum power transfer from Port1 to Port2. The simulation results of ETT match the theoretical prediction.

There are two significant resonance spikes occurring at 27 GHz and 55 GHz. The resonances occur due to poor choices of W+2G. In other simulated 2 mm long impedance transformers, the locations of the resonance spikes also occur at these two frequencies.

Another important thing to notice is that the device characteristics of ETT and SLT are almost the same. This is probably due to the great similarity between the shapes of ETT and SLT. This observation is also encountered in all other simulations comparing ETTs to SLTs that are of equal length and match the same two impedances.

From a purely simulation point of view, ETTs and SLTs can be used interchangeably. In our later simulations, we used SLTs to quickly generate device responses of the impedance transformers mainly for the ease of layout (laying out ETTs is considerably more time intensive).

3.6.2 Model Impedance Transformer Length

As the length of the impedance transformer increases, the cutoff frequency decreases. To examine this behaviour, we analyzed three SLTs with different device length, namely 2 mm, 3 mm and 6 mm. These three SLTs match 26 Ω to 90 Ω on a 650 μm thick GaAs substrate. The electrodes are assumed to be lossless. The devices are designed to have resonance spikes so that

we can observe the behaviour of these resonances as the device length changes. The simulation results are shown in Figure 3.13.

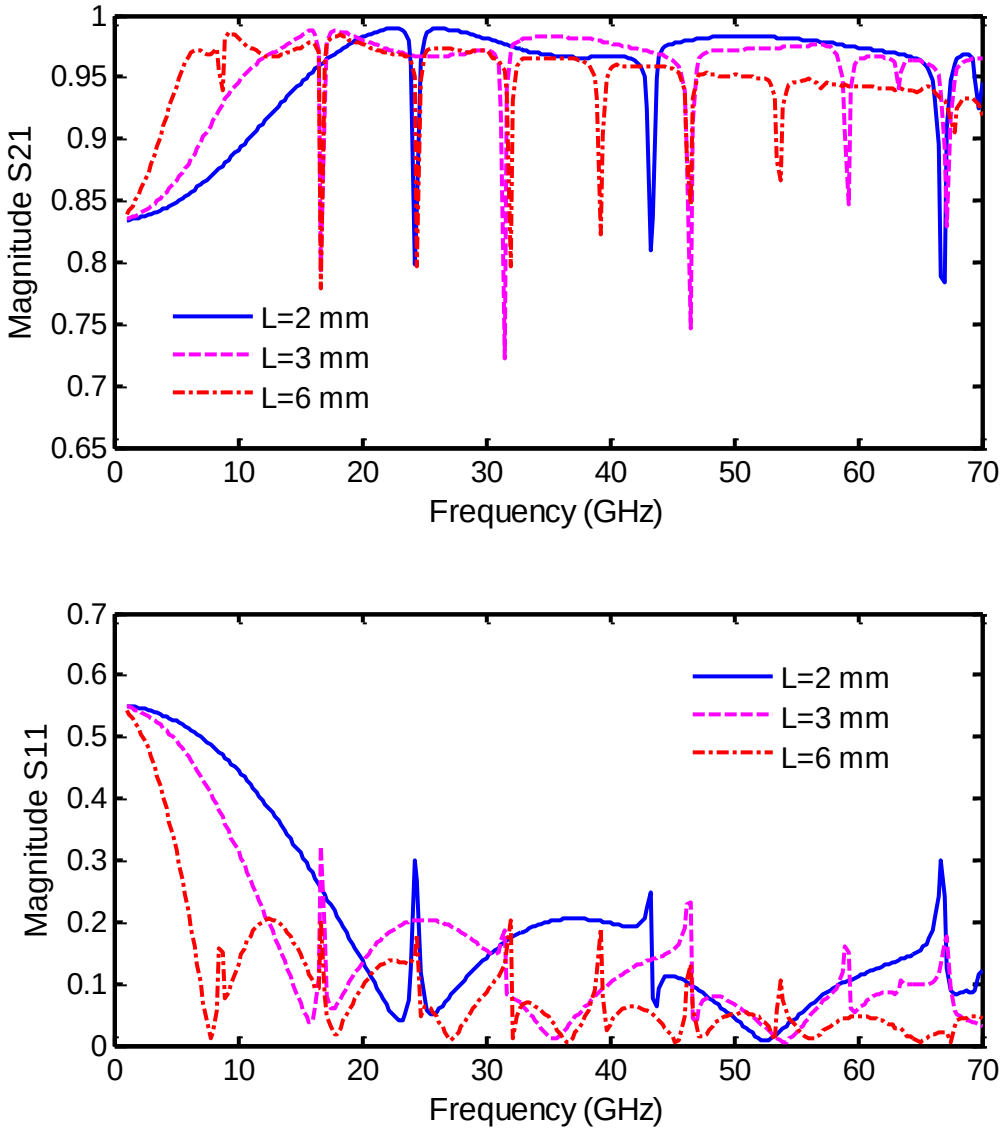

Figure 3.13 S parameter responses for lossless SLTs of different device length

As the total device length increases from 2 mm to 6 mm, the cutoff frequency decreases from ~ 23 GHz to ~ 10 GHz. However, longer devices suffer from greater signal loss in the GaAs substrate, especially at high frequencies. Moreover, there are significantly more resonance spikes in a 6 mm long device than there are in a 2 mm long device. These resonance spikes are more or less equally spaced in frequency.

In another set of simulations, we used 1 μm thick gold instead of lossless metal to examine how different device lengths affect the performance of lossy structures. In these simulations, W+2G is chosen to be 100 μm so that the 2 mm long SLT will not exhibit significant resonances over the frequency range of interest. All SLTs are designed to match 25 Ω to 100 Ω on 650 μm thick GaAs substrates. The S21 responses comparing the performance of SLTs with different device length are shown in Figure 3.14.

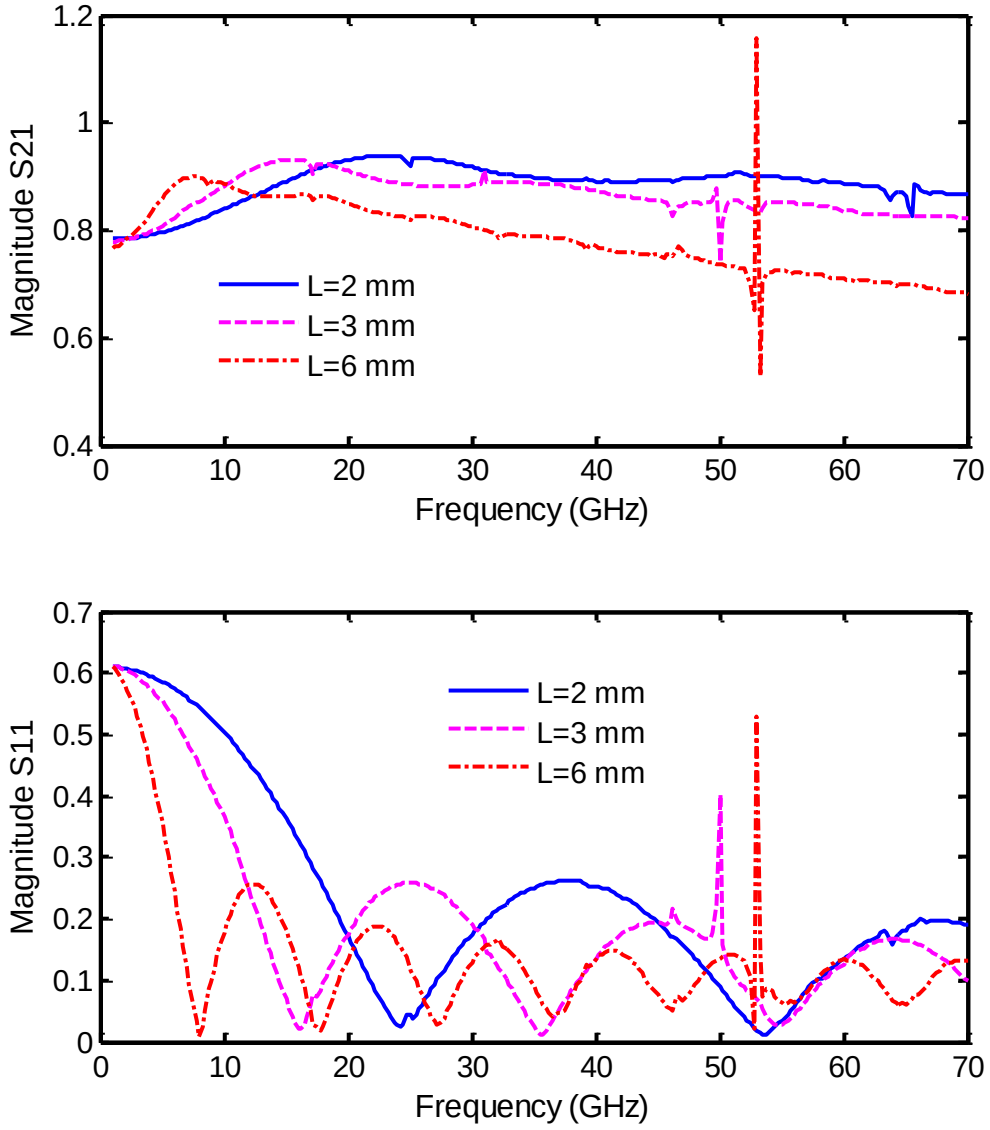

Figure 3.14 Device characteristics of gold SLTs with different device lengths

As can be observed, despite that we choose W+2G to suppress resonances in the 2 mm long device, the 3 mm and 6 mm long devices do have significant resonances. As expected, this means that the occurrence of resonances not only depend on the dimensions of W+2G and the

thickness of the substrate, but also depends on the length of the impedance transformers, i.e., longitudinal resonances.

As the frequency increases, the S21 level of the 6 mm long device drops more rapidly than the 2 mm and 3 mm long devices subject to electrode loss in the 1 μm thick gold conductor. Conduct loss rises dramatically as the length of the line increases.

In conclusion, when designing impedance transformers, the designer should pick the shortest possible device length to avoid high conductor loss and potential longitudinal resonances.

3.6.3 Model SONNET Box Width

The width of the SONNET box is another important variable in setting up the simulation environment. If the SONNET box walls are positioned too close to the simulated structure, the box walls can interact with the electric field of the stimulated structure and alter the response of a device. On the other hand, when the box is very wide, the effect from the box wall is weakened but much longer simulation time may be needed.

A set of simulations were made to examine where the box wall should be positioned relative to the simulated structure. The setup is shown in Figure 3.15. The simulated structure is a 2 mm long 50 Ω CPW line that is matched to 50 Ω ports and in which W+2G=100 μm. The device is 500 μm wide. Four box sizes were considered, namely when d = 1000 μm, 350 μm, 150 μm, and 50 μm. Figure 3.16 shows the simulation results.

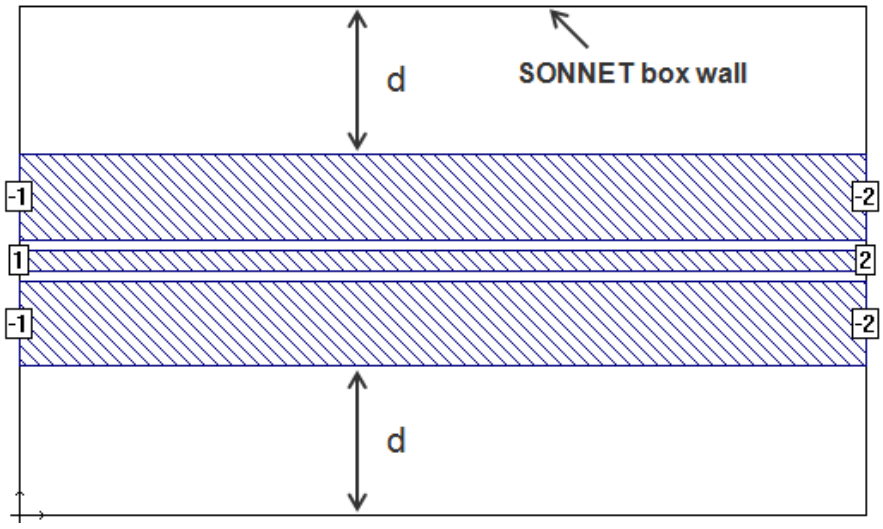

Figure 3.15 Simulation setup to examine the effect of SONNET box wall

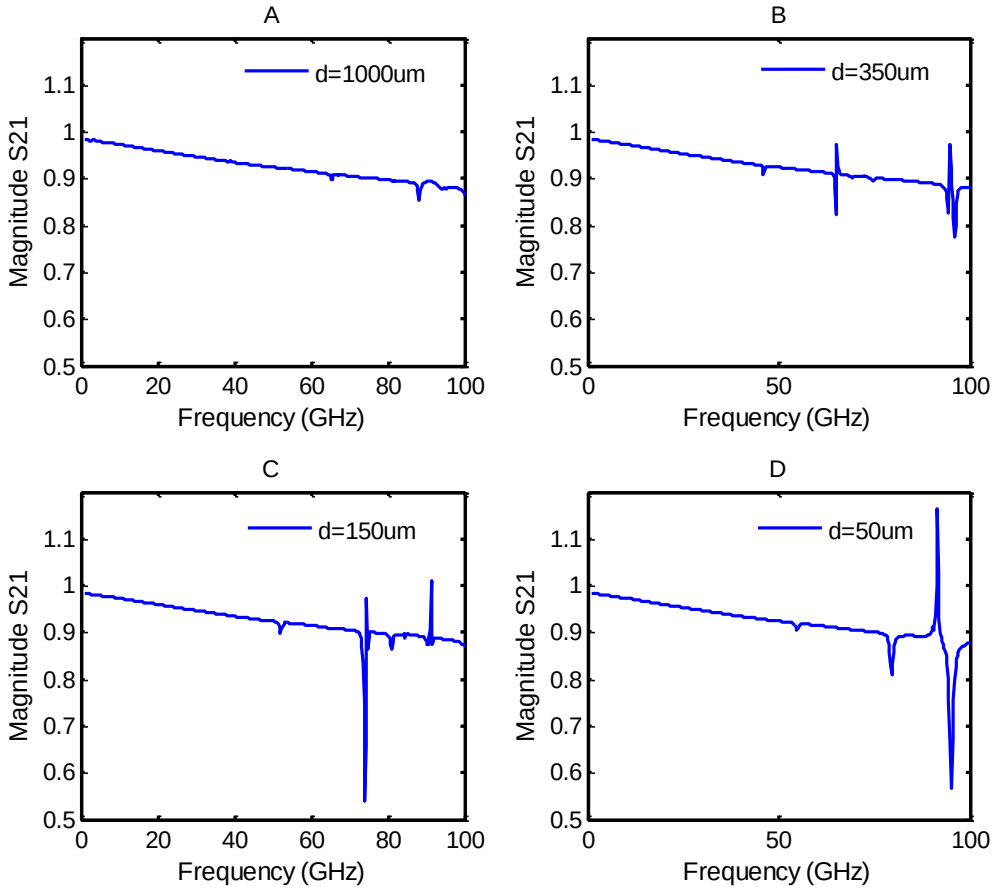

Figure 3.16 Device responses for four SONNET box widths, d = 1000 μm in A, d = 350 μm in B, d = 150 μm in C, d = 50 μm in D.

It can be seen that when d is 50 μm, 150 μm, and 350 μm, significant resonance spikes occur in the S21 plot. As the box wall moves away from the device, the magnitude of the resonance spikes decreases. When d is equal to 1000 μm, the interaction between the box wall and the electric field of the device becomes very weak and the resonance spikes are suppressed.

From here on, in our simulations we will set the box walls 1000 μm away from the outer edges of the device in order to reduce their interactions with the electric field. Setting the box

wall further away will return more or less the same device responses but significantly increase the simulation time.

In the SONNET simulation environment, when there are many sources that cause resonances, the best design approach is to suppress all possible resonances, i.e., by choosing the smallest W+2G, the length of the device, and the appropriate box width, instead of dealing with individual resonances and their sources.

3.7 Procedure to Build an Impedance Transformer with Added Fins (ITF)

Based on the slow-wave electrode theory described in section 2.3 and 2.4, building an impedance transformer loaded with fins (ITF) becomes possible. For the ITFs we designed, the capacitive loading is achieved by adjusting the length of the interdigitated capacitive fins. Since the amount of fin capacitance changes gradually along the length of the impedance transformer, we must know the impedance values that correspond to particular fin geometries. Therefore, the first step is to generate an 'impedance map' for different fin lengths. The following setup, as shown in Figure 3.17, is commonly used to generate such an 'impedance map'.

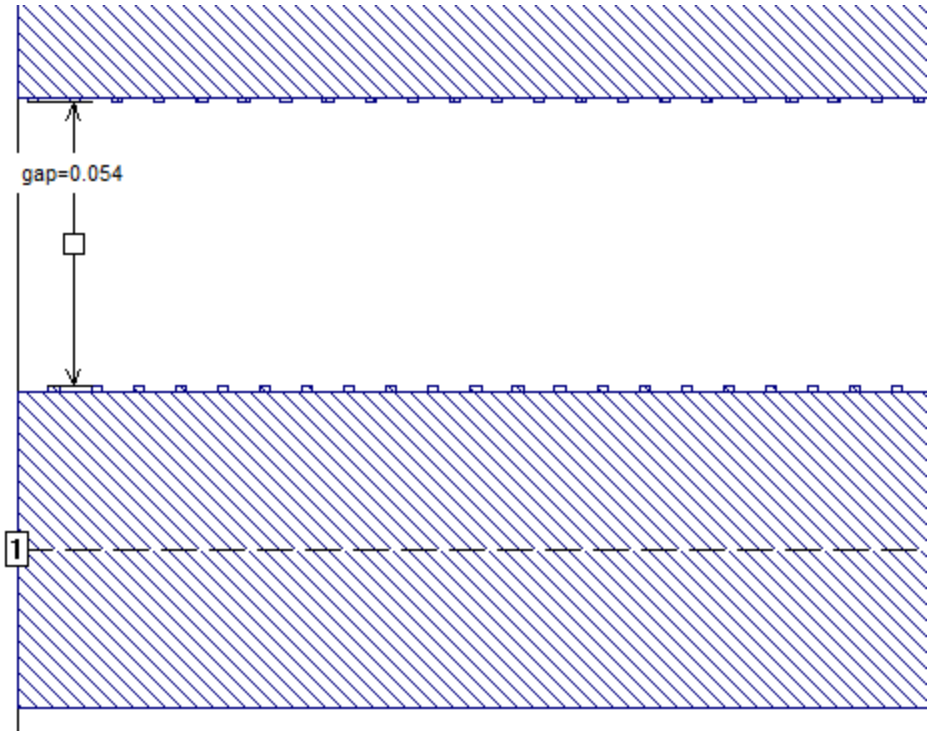

Figure 3.17 Setup to generate 'impedance map' of fins

In this setup, the CPW device length is set to 0.5 mm. This device length is arbitrarily chosen such that we can extract a uniform impedance value for the fin sections without consuming significant simulation time. In between the center and the outer conductor, small fin structures are positioned in interdigitated fashion. The lengths of the fins are initially set to 1 μm, which represents very little fin capacitance added to the CPW. Then we grow the length of all the fins 1 μm at a time, to examine the properties of the line until the fins expand the entire gap between the center and outer electrodes (but not making contact with the other electrode, i.e., a 1 μm gap remains). After running the simulations, we can extract 'y parameters' from the EM analysis engine (the port impedances can be set to any values, since they don't affect the outcomes of the 'y parameters'), and use the equations described in section 2.3 to find the impedance values of the CPW line as a function of fin length. This process can be automated

using the step-through function of the EM analysis engine and a separate Matlab program. The 'impedance map' for W+2G=170 μm CPW line with 4 μm wide fins is shown in Figure 3.18.

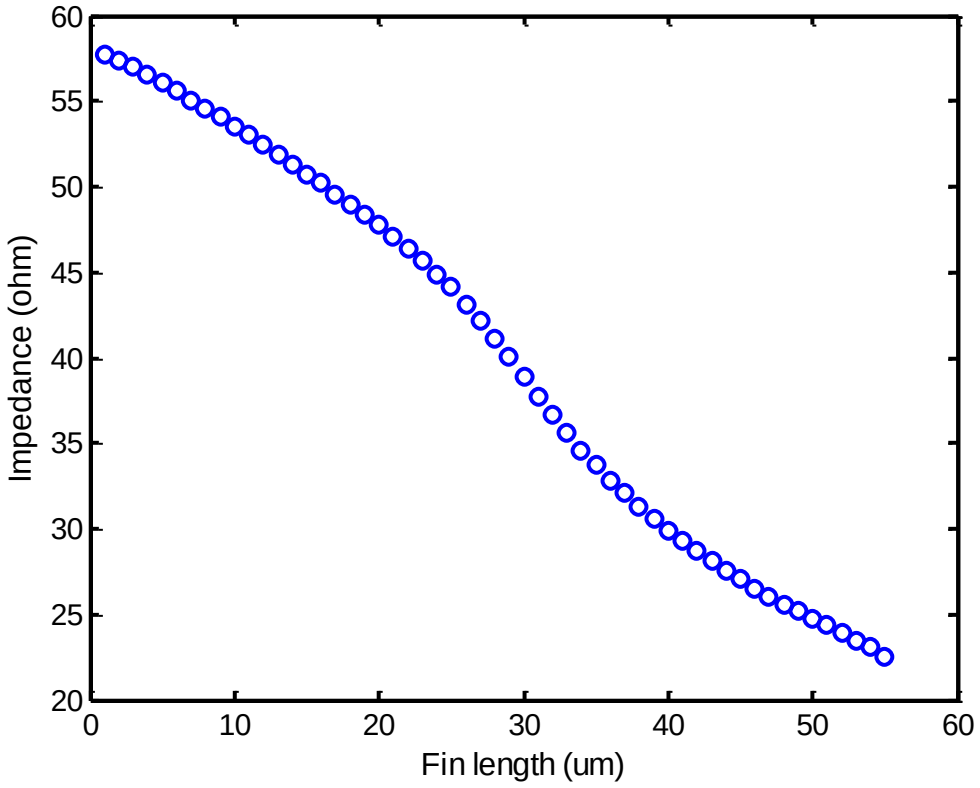

Figure 3.18 Impedance map for W+2G=170 μm line with 4 μm wide fins

It can be seen that as the lengths of the fins grow from 1 μm to 54 μm, the impedance values decrease smoothly. The range of the impedance values is from ~ 23 Ω to ~ 57 Ω. As the amount of capacitive loading increases, the effective microwave index rises, indicating that the microwave travels slower where the fins are longer. Figure 3.19 shows the microwave index versus fin length. The effective microwave index rises from 2.6 to 6.6 as the lengths of the fins increase. The amount of slowing is quite dramatic when the CPW section is fully loaded with fins.

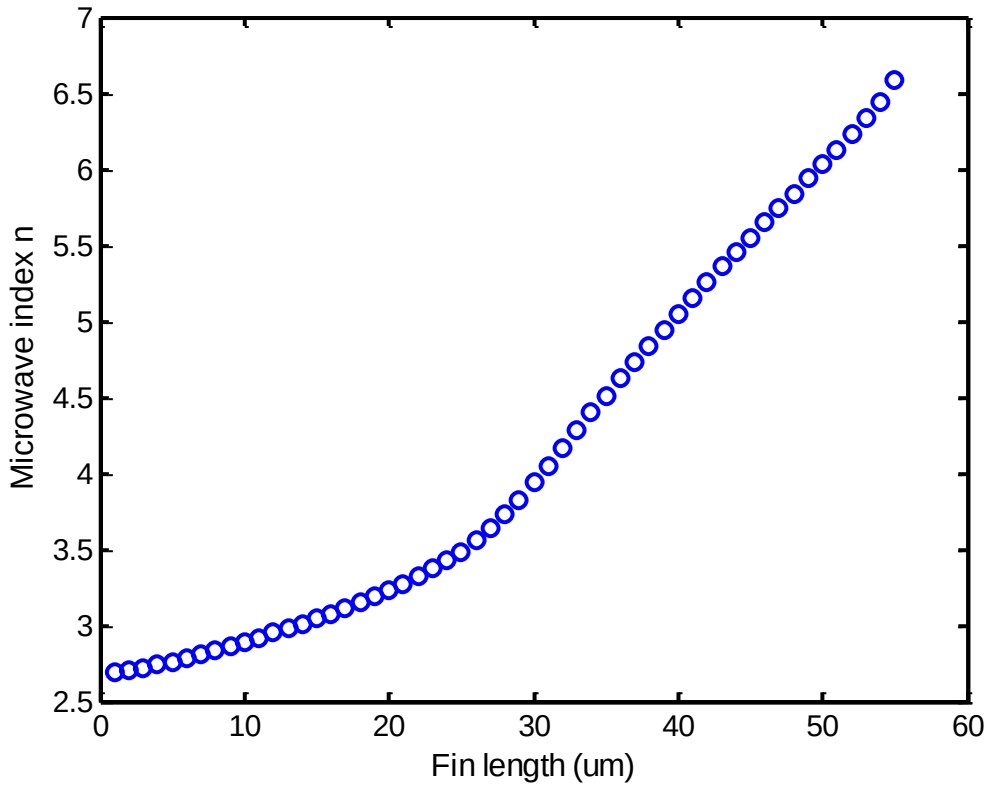

Figure 3.19 W+2G=170 μm 4 μm fin effective microwave index

Once the 'impedance map' is generated, ITF can be made by matching the geometries of the fins to the impedance values along the length of a regular ETT (or any impedance transformer). In doing this, we did not take into account that n_{eff} has changed along the length of the impedance transformer. That is, we did not scale the physical length of the impedance transformer according to the values of the n_{eff} that are represented by different fin geometries. A typical ITF structure is shown in Figure 3.20.

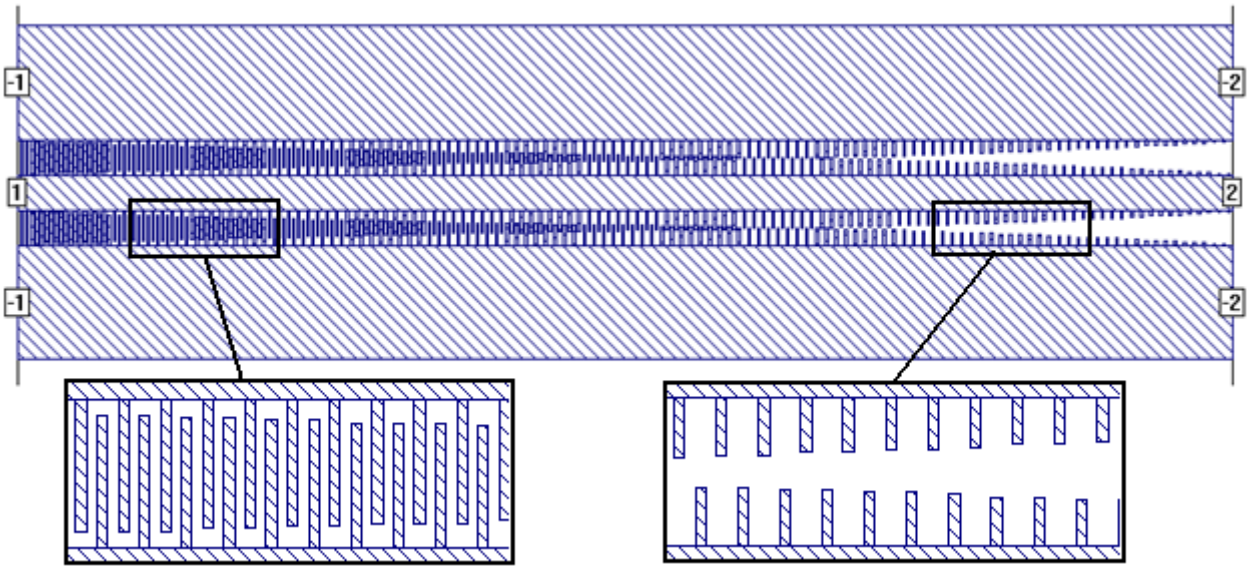

Figure 3.20 Typical ITF structure

In our designs, to represent a single impedance value, the length of each section of the ITF is set to be 4 times the width of the fins. For example, if the width of the fins is 2 μm, then each section is made to be 8 μm wide, to represent a single impedance value. The spacing between the fins is set to be equal to the width of the fins. Such arrangements allow each section to include the amount of combined capacitance from a pair of fins (one grown from the center conductor and one grown from the outer ground conductor). This maximizes the number of possible impedance values represented by the fins for a fixed gap distance between the center and the ground electrode.

In Figure 3.20, the fins in each section of the ITF have the same length (the lengths of one fin growing from the center electrode and one fin growing from the ground electrode are the same). The designer can also grow the fins in different ways. For example, as the impedance value decreases along the line, the fins on the center electrode can grow first until they expand fully across the gap, then fins on the ground conductor begin growing to introduce additional capacitance. Alternatively, the designer can grow the fins from the ground conductors first.

3.8 The First Simulated ITF Structure

The first ITF structure that we simulated (ITF1), which is shown in Figure 3.21, matches 18 Ω (Port1 on the left) to 81.6 Ω (Port2 on the right) on a 650 μm thick GaAs substrate. As the impedance gradually decreases towards the low impedance end of the device, 2 μm wide fins begin to grow from the center electrode until they fully span the entire gap (but not making contact with the ground electrode, a 1 μm gap remains). The fins on the outer conductor then grow to introduce additional capacitance until 18 Ω is reached at Port1. In fact, the lowest impedance value that can be reached by ITF1 is 16.22 Ω, i.e., the fins still have space to grow longer at the low impedance end of ITF1. The width of the center electrode W is set to be 10 μm in order to maximize the gap. The gaps between the center and outer electrodes are 120 μm. The metal is assumed to be lossless. The device is 2 mm long.

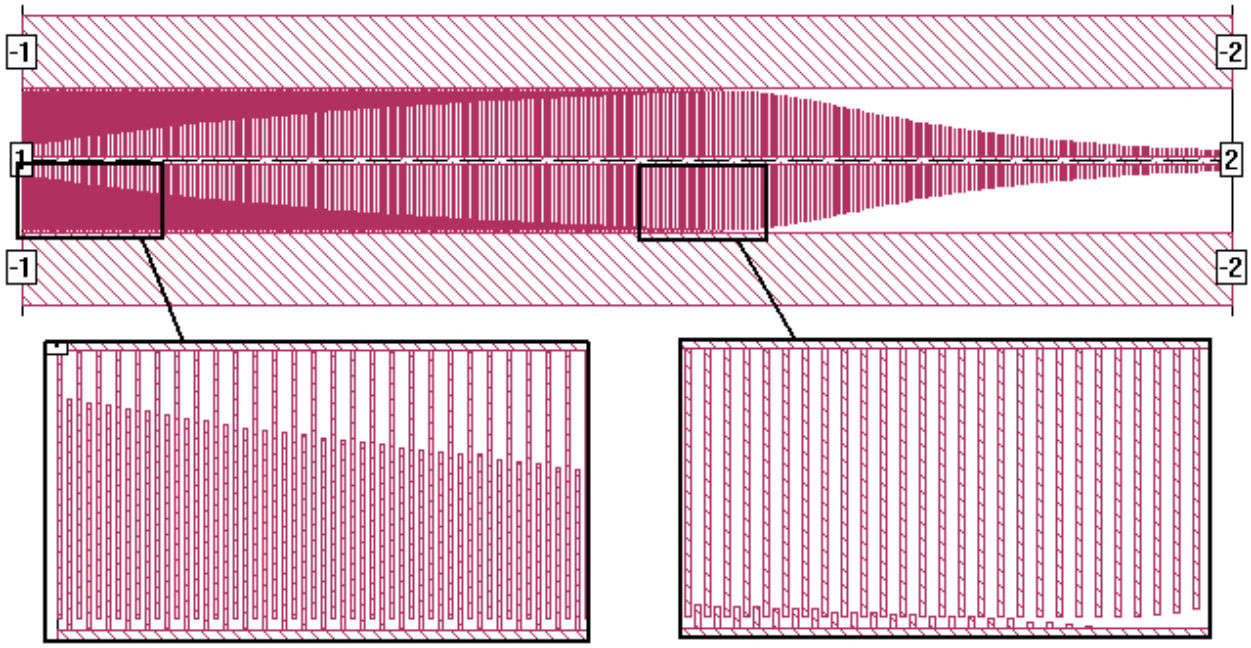

Figure 3.21 ITF1 and its detailed view

The device characteristics of ITF1 are compared with the behaviour of a regular 2 mm long exponentially tapered impedance transformer (ETT1). ETT1 is illustrated in Figure 3.22, which also matches 18 Ω to 81.6 Ω. The lowest impedance value that can be reached by ETT1 is 18 Ω. At the low impedance end of ETT1, the center electrode is 238 μm wide, which fully spans the space between the two ground electrodes (but not making contact, a 1 μm gap remains). The simulation results are shown in Figure 3.23.

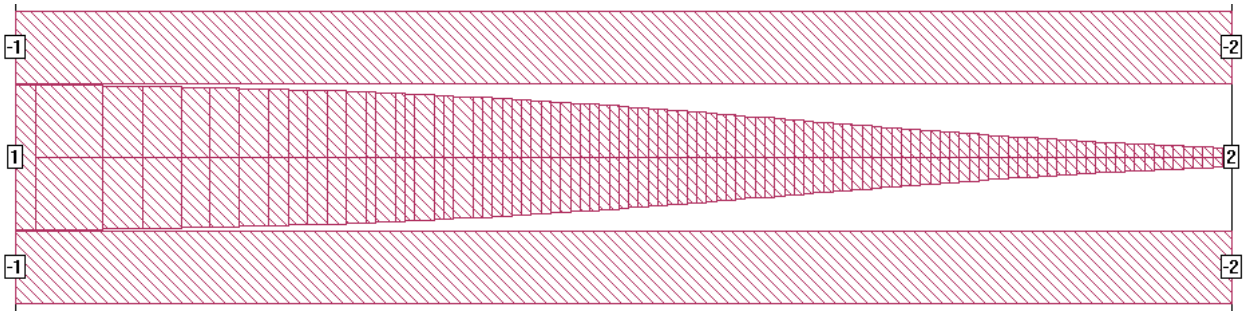

Figure 3.22 ETT1 matching 18 Ω to 81.6 Ω

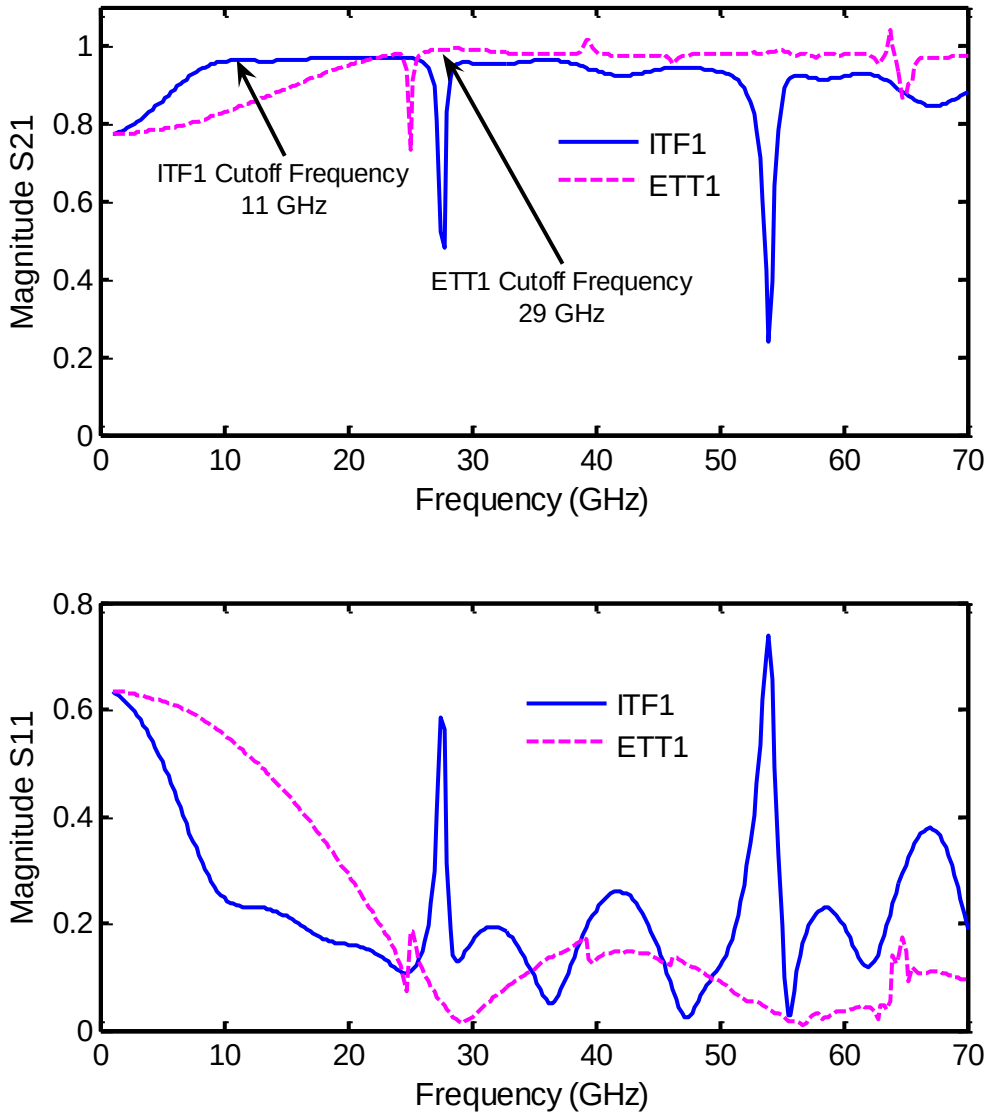

Figure 3.23 Device characteristics of ITF1 and ETT1

It can be seen that the S21 response of ITF1 exhibits the normal behaviour of a conventional tapered impedance transformer. The S21 value increases as frequency rises towards the cutoff frequency at 11 GHz. Then the S21 level gradually drops as frequency increases

further subject to substrate loss. Compared to ETT1, ITF1 suffer from greater substrate loss at high frequencies.

The two most important results to notice are that the cutoff frequency of ITF1 is decreased to 11 GHz and that ITF1 has the potential to match to lower impedance values than ETT1 can. These lower values are due to the slowing effect introduced by the capacitive loading fins. According to section 2.2.1, a higher microwave index n_{eff} value lowers the cutoff frequency. As fins are added to the impedance transformer, the value of n_{eff} rises above 2.6. Although the value of n_{eff} changes along the length of ITF1, the overall n_{eff} along the device is increased, which lowers the cutoff frequency. The cutoff frequency of a regular ETT with the same device length is ~ 27 GHz. For a regular ETT to have a cutoff frequency at 11 GHz, the impedance transformer should be 5.7 mm long, which could cause significant problems with regard to conductor loss, increase the substrate loss, and potentially introduce longitudinal resonances.

There are some undesirable resonances in the device characteristics of ITF1 because we have not optimized the dimension of W+2G. Nevertheless, we included the simulation results of ITF1 because they demonstrate what we are trying to achieve by using capacitive loading fins to design the impedance transformer. The n_{eff} values along the entire length of ITF1 are plotted in Figure 3.24.

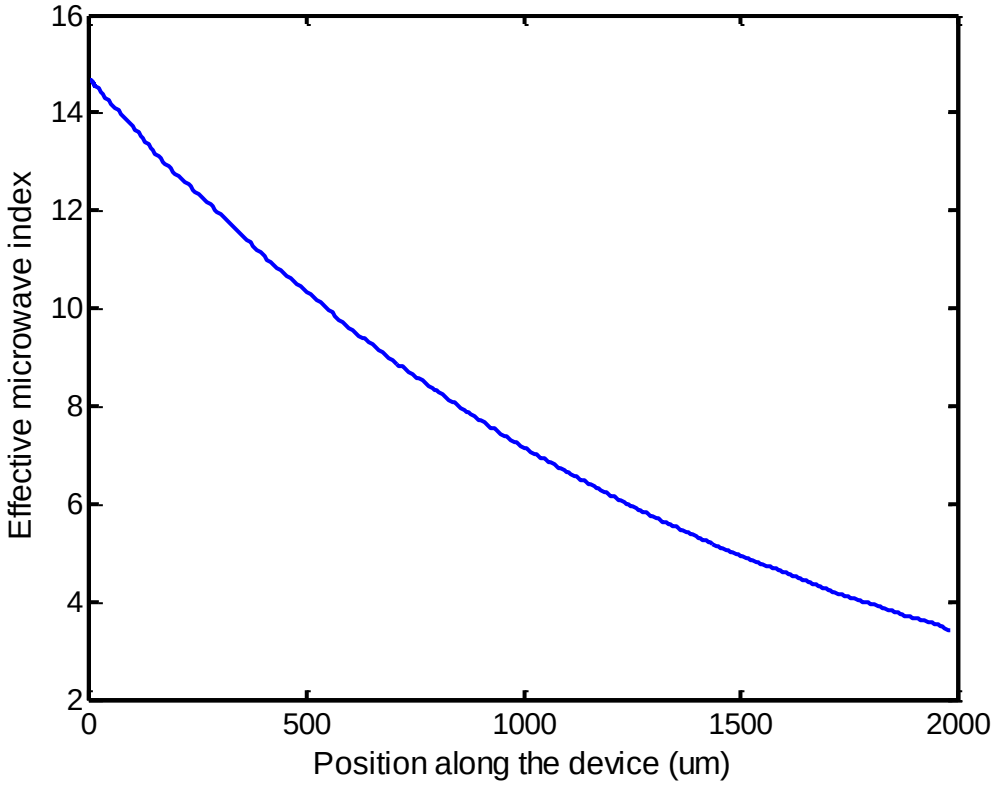

Figure 3.24 Effective microwave index along the length of ITF1

It can be seen that at the high impedance end of ITF1, n_{eff} is 3.4. As the impedance decreases, n_{eff} rises to as much as 14.5 at the low impedance end of the impedance transformer. The amount of slowing introduced by the 110 μm long, 2 μm wide fins at the low impedance end of ITF1 is very significant. Due to this capacitive loading effect, the electrical signal travels slower at the low impedance side of ITF1, and gradually speeds up towards the high impedance end.

In another simulation, we keep the same structure of ITF1, but set the electrodes to be 1 μm thick gold in order to examine the performance of the device when metal loss is included. We call this device ITF2. In Figure 3.25, we compare the device characteristics of ITF1 and ITF2.

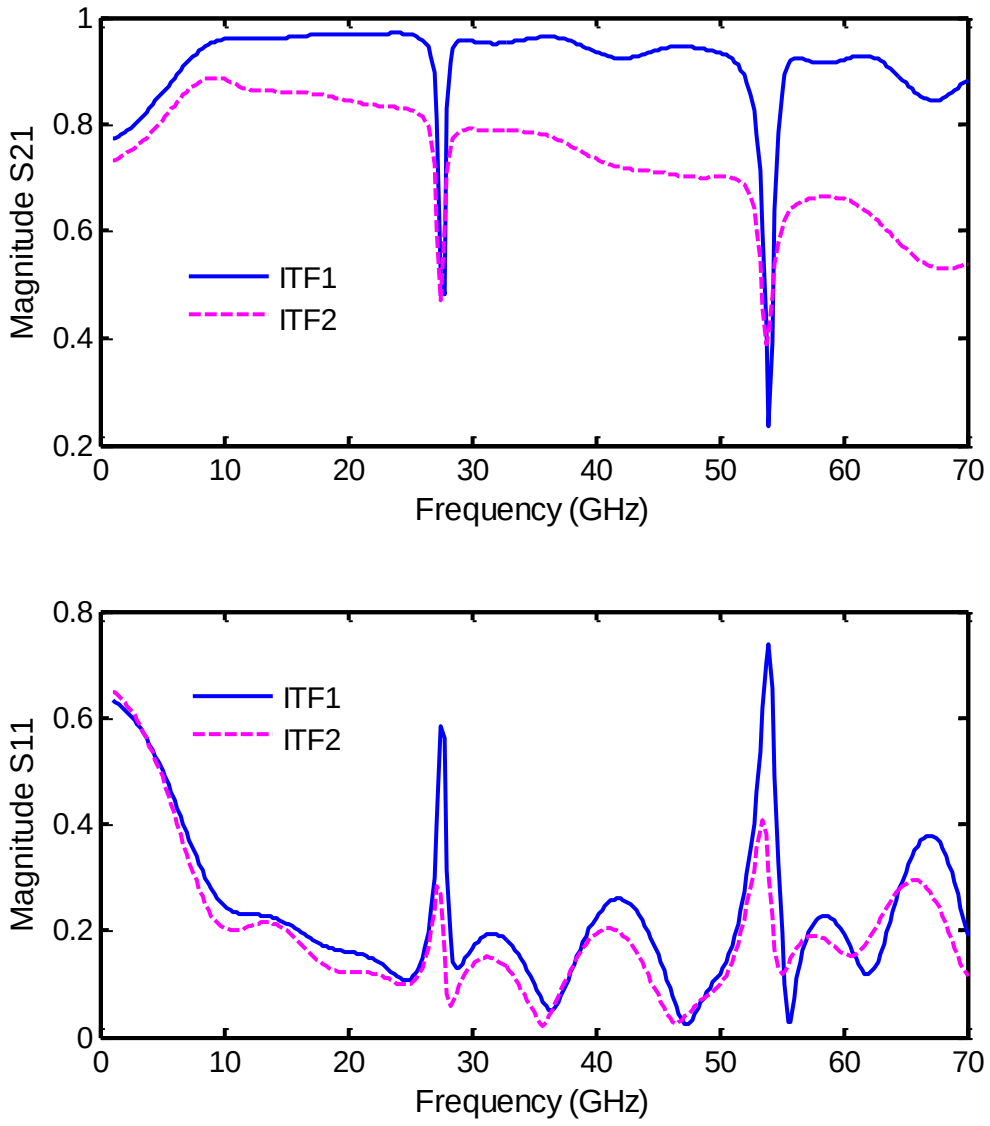

Figure 3.25 Device characteristics of ITF1 and ITF2

When the conductor loss is included, the S21 level drops more rapidly as frequency increases. The S21 level falls below 0.7 above 45 GHz. The S11 levels of these two devices are very similar.

The current density map of ITF1 is shown at four different frequencies in Figure 3.26. The high current density areas are red and the low current density areas are blue. The colouring scheme is normalized at each frequency.

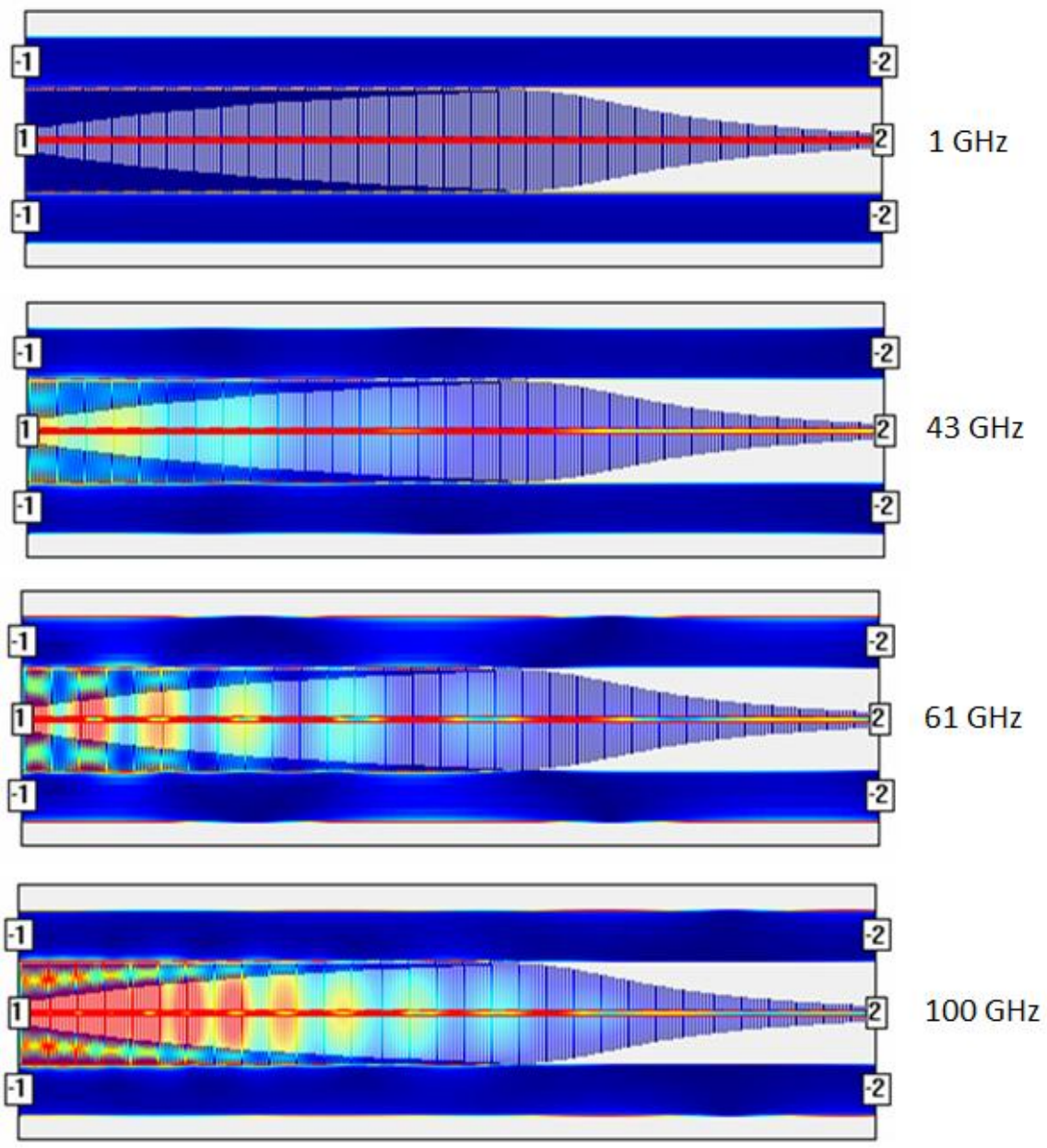

Figure 3.26 Current density map of ITF1 at 1 GHz, 43 GHz, 61 GHz, and 100 GHz

At 1 GHz, current density is highest in the center conductor. As frequency is increased, current density in the capacitive loading fins rises at the low impedance end of ITF1, where the

fins are longer. Above 60 GHz, distinct elliptical interference patterns of high current density form at the lower impedance end of ITF1. These elliptical patterns are more densely packed at the lower impedance end of ITF1 than they are at the higher impedance end. It is an indication that the microwave travels slower when the capacitive loading is greater.

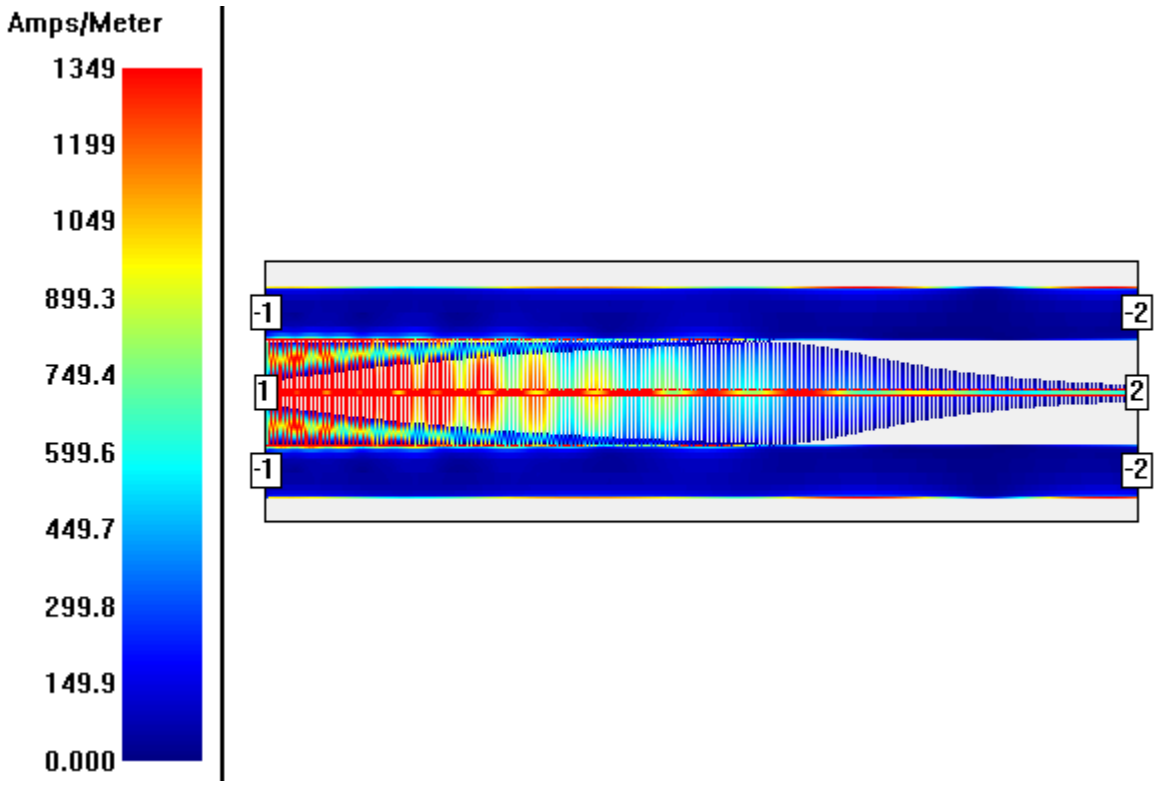

Figure 3.27 Current density reading at 100 GHz

Figure 3.27 shows the actual reading of current density of ITF1 at 100 GHz. The current density reading exceeds 1000 Amps/Meter along the center electrode and in many fins at the low impedance end of ITF1, which indicates significant amount of conductor loss in these regions. By widening the center conductor, one can significantly reduce the overall electrode loss. In many of our later simulated devices, the width of the center electrode is set to 60 μm along the

entire length of the fin sections. The conductor loss in the fins can be reduced by widening and shortening the fins.

3.9 Hybrid ITF

For a given center electrode width, adding capacitive loading fins to the CPW can only reduce the impedance of the line, but not increase it. Therefore, the highest impedance values of the line can only be reached by narrowing the center electrode. In order to design impedance transformers that can also match high impedance values, we can combine sections that utilize capacitive loading fins with sections that only taper the center electrode in a single structure. We call this type of impedance transformer the hybrid ITF.

Properly designed ITFs can outperform traditional CPW tapered impedance transformer, i.e., having lower reflection coefficient, wider operating bandwidth, and wider impedance matching range. The following example is a 2 mm long hybrid ITF (ITF3) matching 27 Ω to 102 Ω on a 650 μm thick GaAs substrate. ITF3 is shown in Figure 3.28. The conductor is chosen to be 1 μm thick gold. In order to suppress resonances, W+2G is chosen to be 100 μm. For the ITF sections that are loaded with fins, the width of the center electrode (W) is 40 μm wide, and the gap between the center and outer electrode (G) is 30 μm. The device characteristics of ITF3 are compared with those of ETT3 (ETT3 is a 2 mm long exponentially tapered impedance transformer matching 27 Ω to 102 Ω, in which W+2G is also 100 μm), as shown in Figure 3.29.

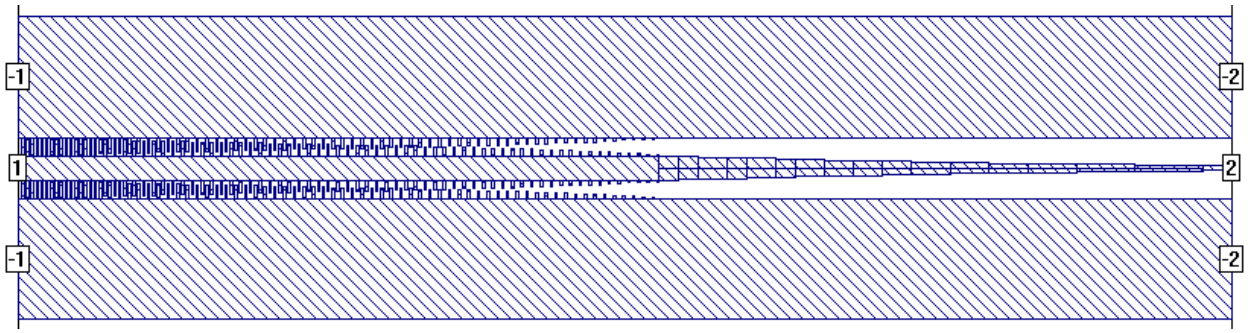

Figure 3.28 ITF3 matching 27 Ω to 102 Ω, W+2G = 100 μm

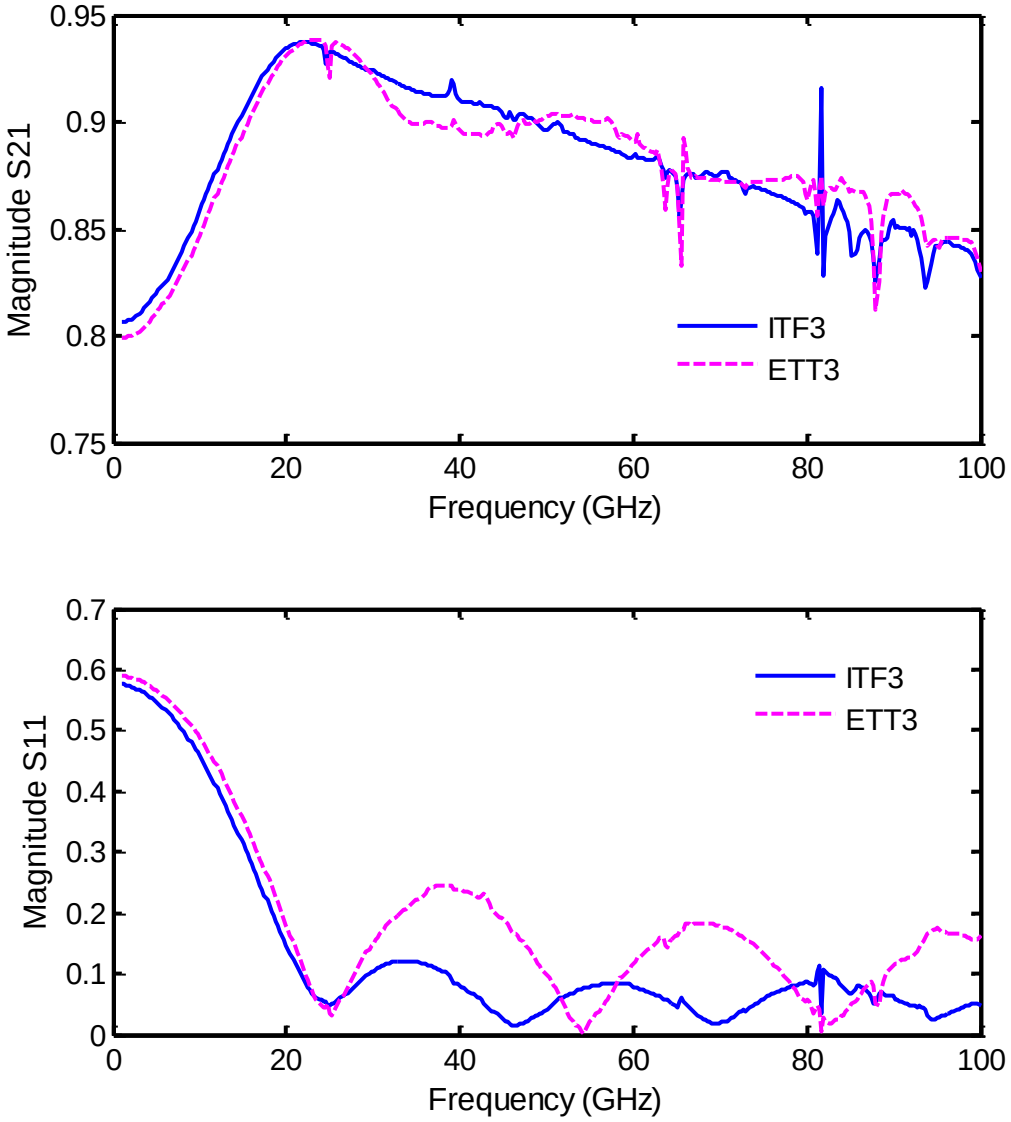

Figure 3.29 Device characteristics of ITF3 and ETT3 matching 27 Ω to 102 Ω

The S21 behaviour of ITF3 and ETT3 are very similar. The cutoff frequency of ITF3 and ETT3 is 24 GHz and 25 GHz, respectively. The fins used in ITF3 are used to control the impedance values along the line, but not to change n_{eff} dramatically. Hence, the fins did not lower the cutoff frequency significantly. Both S21 curves stay above 0.8 beyond the cutoff

frequency. Given that W+2G = 100 μm, there is no severe resonance. The S11 performance of ITF3 is noticeably better than that of ETT3. Beyond the cutoff frequency, the S11 level of ITF3 remains below 0.13. This shows that properly designed ITF can outperform ETT.

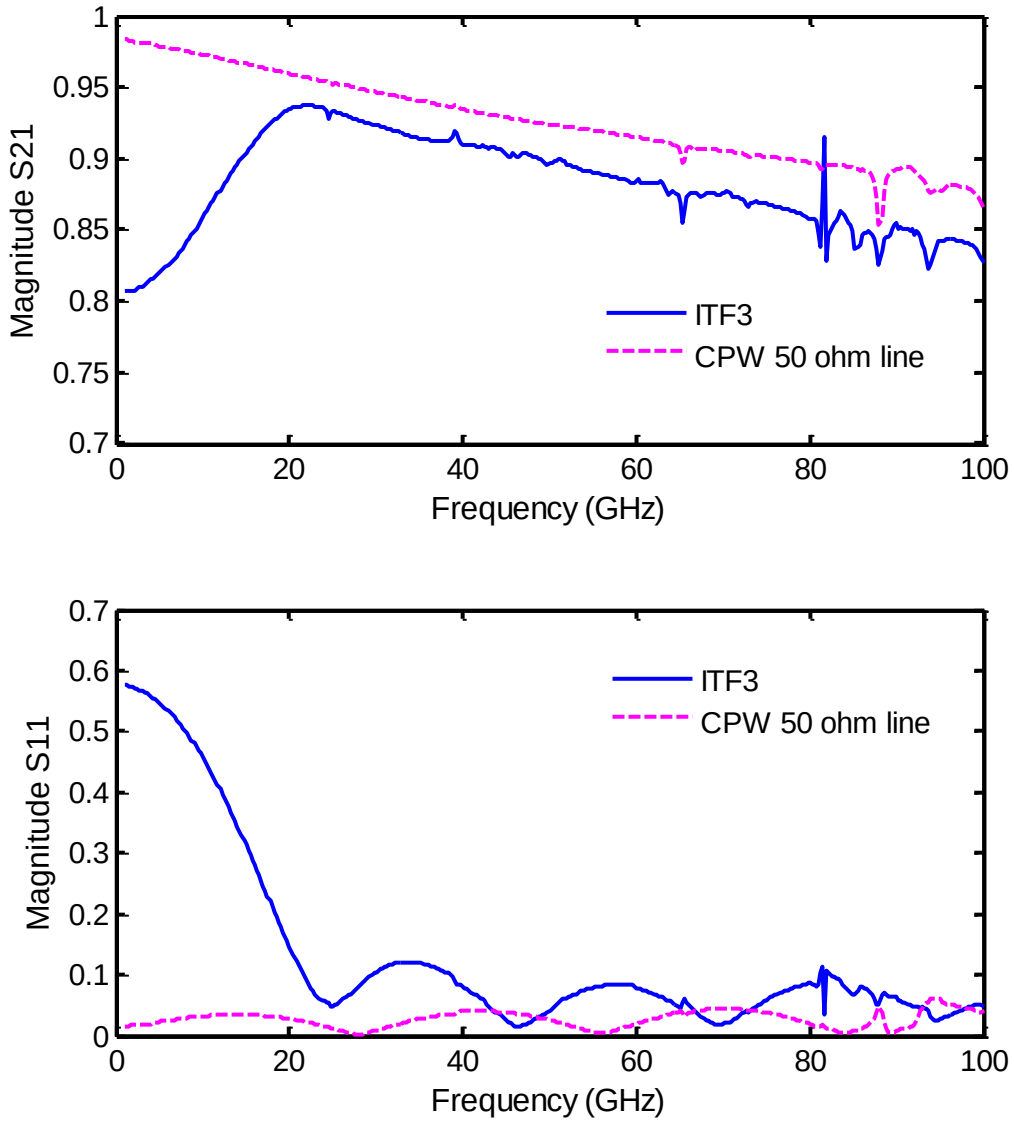

Figure 3.30 Device characteristics of ITF3 and a standard 50 Ω line

Figure 3.30 compares the device characteristics of ITF3 with those of a standard 50 Ω line. It can be seen that the S21 and S11 levels of ITF3 are comparable to those of a standard 50 Ω line for frequencies beyond the cutoff frequency.

3.10 Real-estate Saving Using ITF

One of the benefits of using ITFs is that ITFs can achieve similar device performance as conventional tapered impedance transformers but with shorter device lengths. When ETT and ITF have the same cutoff frequency, the electrode length of the ITF is always shorter due to the higher values of n_{eff} that are used. To demonstrate this, we simulated an ITF (ITF4) and an exponentially tapered impedance transformer (ETT4). Both devices match 24 Ω to 57 Ω and have W+2G=170 μm. ITF4 employs 4 μm wide fins and is 2 mm long, as illustrated in Figure 3.31. In contrast, ETT4 does not utilize any capacitive loading fins and is 2.75 mm long. To simulate electrode loss for both devices, the metal layer is chosen to be 1 μm thick gold. In Figure 3.32, device characteristics of ITF4 are compared with those of ETT4.

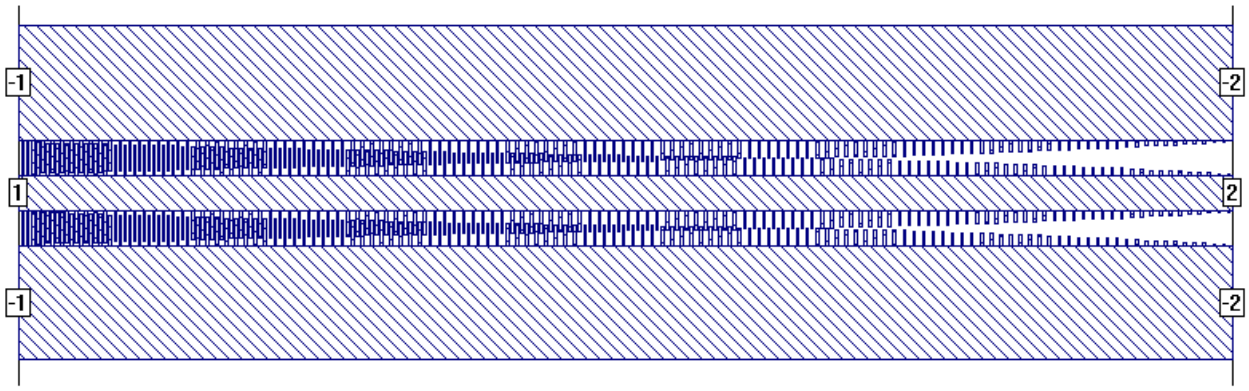

Figure 3.31 ITF4 matching 24 Ω to 57 Ω utilizing 4 μm fins

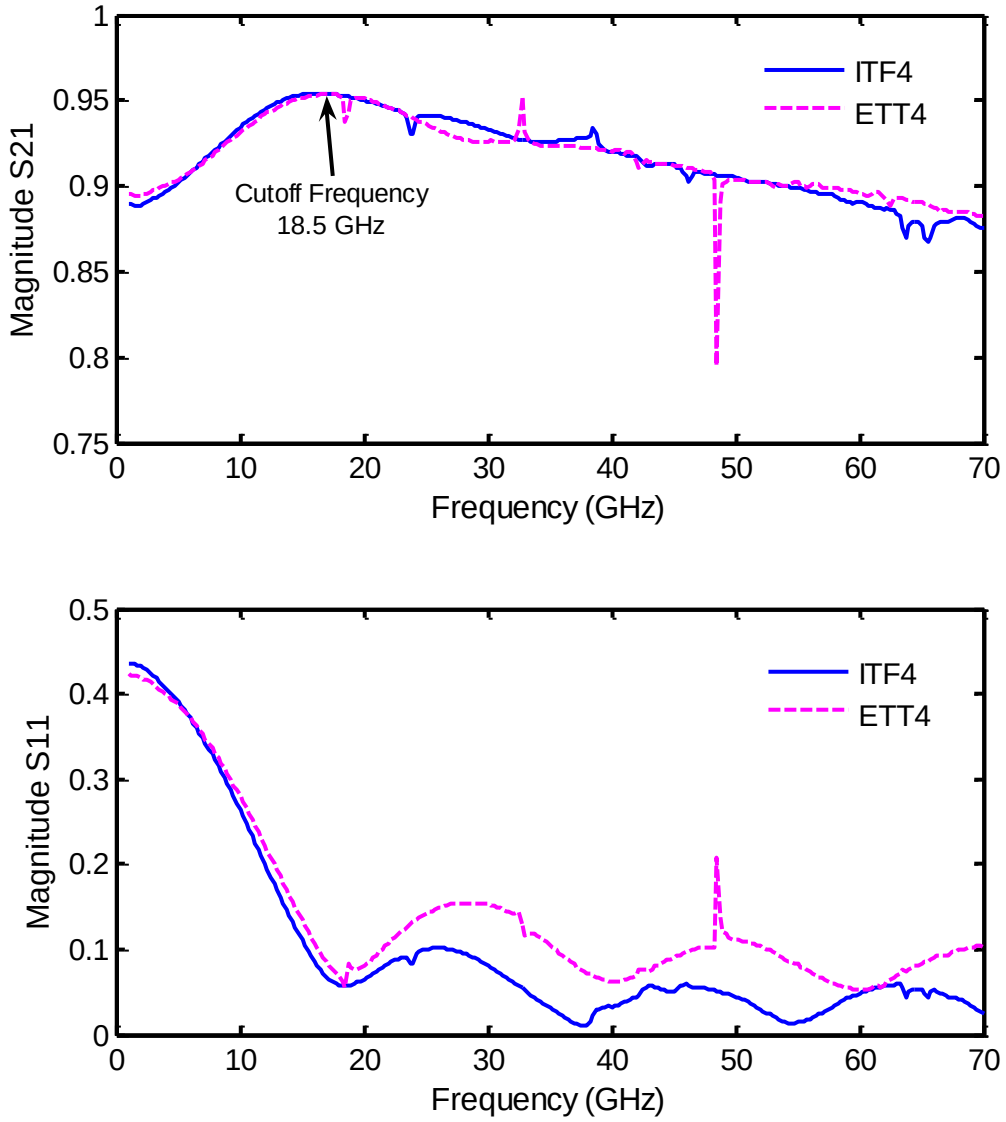

Figure 3.32 Device characteristics of ITF4 and ETT4

As shown in Figure 3.32, the cutoff frequencies of ITF4 and ETT4 are both 18.5 GHz. The S21 level of ITF4 shows a similar level of performance as that of ETT4. However, ETT4 is 37.5 per cent longer than ITF4. By using ITF, one can achieve the same device performance with

shorter electrode length, saving ‘on-chip real-estate’. When thinner fins are used, even greater real-estate savings can be achieved.

3.11 Impedance Matching Range of ITF

Given the same minimum feature size of 1 μm for fabrication, ITF can match impedances to lower values than ETT can. This is due to the excess amount of capacitance introduced by the interdigitated fins. Table 3.2 lists impedance matching ranges of the impedance transformer when different sizes of fins are used.

	Fin Width	Z range (Ω)	n_{eff}
Type A : W+2G = 170 μm W = 60 μm G = 55 μm	1 μm fin	12.62~57.8	2.65~11.1
	2 μm fin	17.22~57.8	2.65~8.42
	4 μm fin	22.5~57.8	2.65~6.58
	CPW taper (no fin)	23.9~193.87	2.65
Type B : W+2G = 260 μm W = 60 μm G = 100 μm	1 μm fin	10.17~68.5	2.65~15.3
	2 μm fin	14.12~68.5	2.65~11.6
	4 μm fin	19.0~68.5	2.65~8.91
	CPW taper (no fin)	24.48~229.1	2.65

Table 3.2 Impedance matching ranges of the impedance transformer when different sizes of fins are used

In our simulations, we mainly analyzed ITFs with two different W+2G dimensions, namely 170 μm and 260 μm (named Type A and Type B devices). The dimensions of W and G are listed in Table 3.2 column one. As explained in section 3.4, W is set to 60 μm to reduce conductor loss in the center electrode. G is chosen so that the fins have 54 μm and 99 μm space to grow in Type A and Type B devices respectively. The impedance matching ranges of different types of fins are shown in column 3. For example, in Type A devices, 1 μm wide fins cover the impedance matching range from 12.62~57.8 Ω when the length of the fins varies from 0 μm to 54 μm. The corresponding values of n_{eff} are shown in column 4.

As shown in Table 3.2, the impedance matching range of different kinds of fin sections and regular CPW sections overlap, i.e., 30 Ω can be designed by using 1 μm wide fin sections, 2 μm wide fin sections, 4 μm wide fin sections, and regular CPW sections. As the width of the fins decreases, the added capacitance per unit length increases dramatically. Impedances as low as 10.17 Ω can be reach with 99 μm long and 1 μm wide fins in W+2G=260 μm structures (with thinner and longer fins, lower impedance values can be reached). This makes matching to low impedance devices possible given the same on-chip real-estate. Correspondingly, the microwave index n_{eff} reaches 15.3 for this fin geometry.

Figure 3.33 illustrates a 2 mm long ITF (ITF5) matching 14 Ω to 68 Ω on a 650 μm thick GaAs substrate. W+2G is 260 μm and the fins are 2 μm wide. The center electrode is 60 μm wide. The electrodes are set to be 1 μm thick gold. The device characteristics of ITF5 are shown in Figure 3.34.

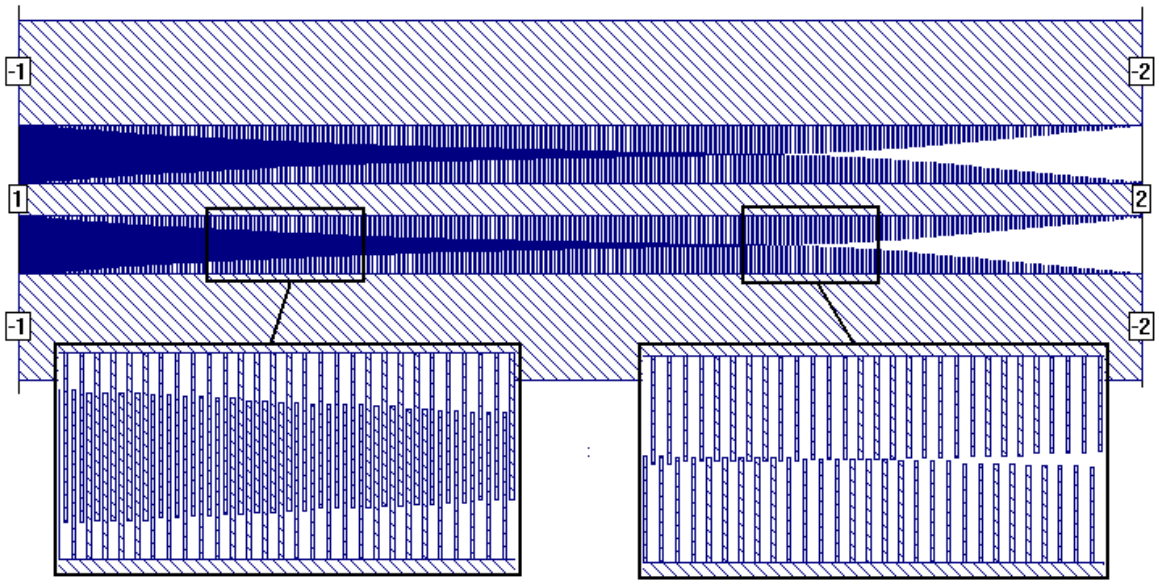

Figure 3.33 ITF5 matching 14 Ω to 68 Ω with 2 μm wide fins

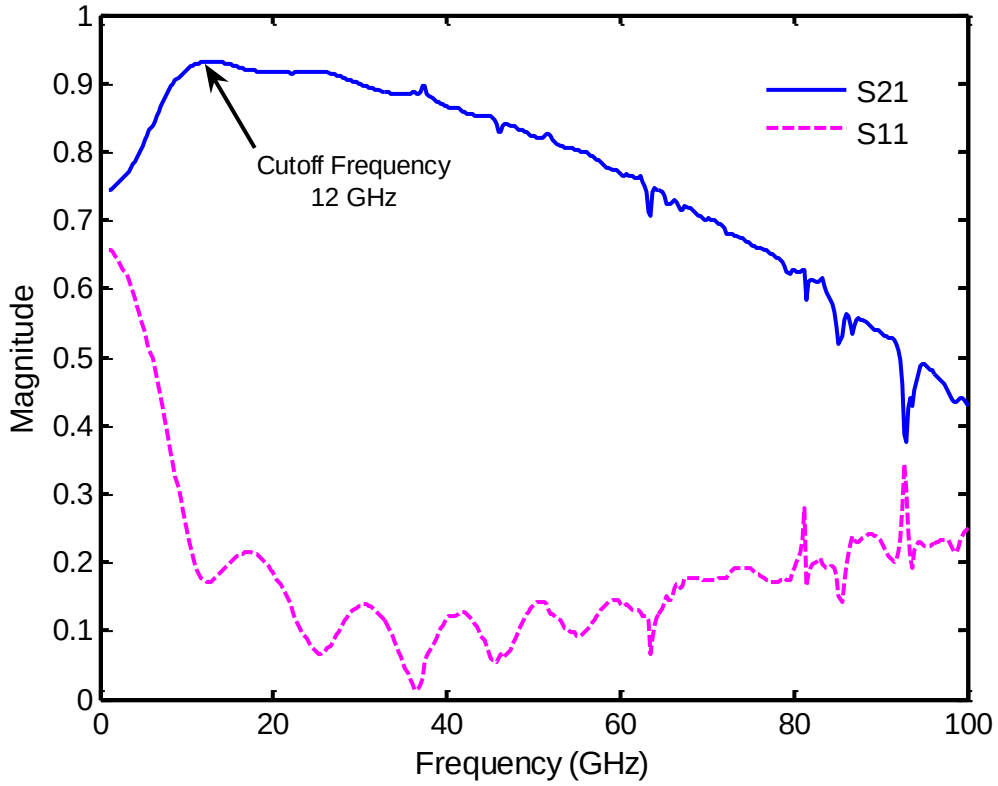

Figure 3.34 S parameter characteristics of ITF5 matching 14 Ω to 68 Ω

The excess amount of capacitive loading dramatically increased the effective microwave index. The cutoff frequency is lowered to ~ 12 GHz. ITF5 behaved reasonably well up to 40 GHz. As the frequency rises above 40 GHz, the S21 level drops more rapidly due to the conductor loss in the 2 μm wide fins. Compared with ITFs that employ 4 μm wide fins, the conductor loss in 2 wide μm fins is more significant. In the following section, we will examine electrode loss in the fins.

3.12 Electrode Loss in the Fins

In this section, we analyze the amount of electrode loss of the transmission line at various frequencies when fins of different sizes are used. In particular, the electrode loss of 1 μm wide and 2 μm wide fins are examined. A 0.5 mm long transmission line loaded with fins that are of equal length and width are used to determine the line loss. In the simulation setup, the center conductor is 60 μm wide, and W+2G is 260 μm. This leaves 99 μm for the fins to grow into. The metal is set to be 1 μm thick gold. During the analysis, the fins grow in 1 μm steps so that we can obtain the electrode loss of the line when fins of different lengths are used. For example, Figure 3.35 illustrates a transmission line section used to analyze electrode loss for a particular fin geometry, where all the fins are 60 μm long and 2 μm wide.

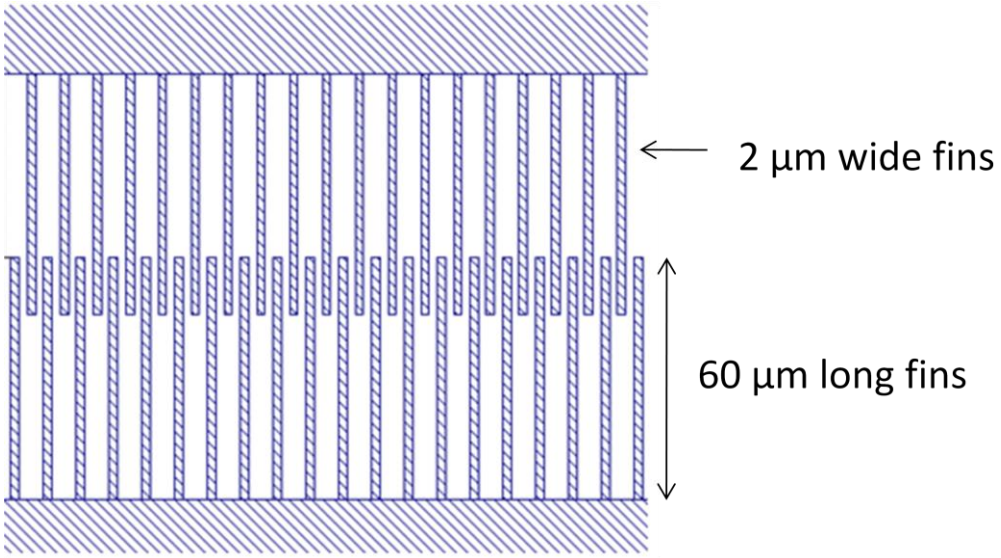

Figure 3.35 Transmission line loaded entirely with 60 μm long and 2 μm wide fins

The simulation results for 2 μm wide fins and 1 μm wide fins are shown in Figure 3.36 A and B respectively. Each plot contains the electrode loss for 99 fin lengths at four different frequencies, namely 70 GHz, 50 GHz, 30 GHz, and 10 GHz. For example, when 99 μm long and 2 μm wide fins are used, the transmission line loss reaches ~ 5 dB/mm at 70 GHz.

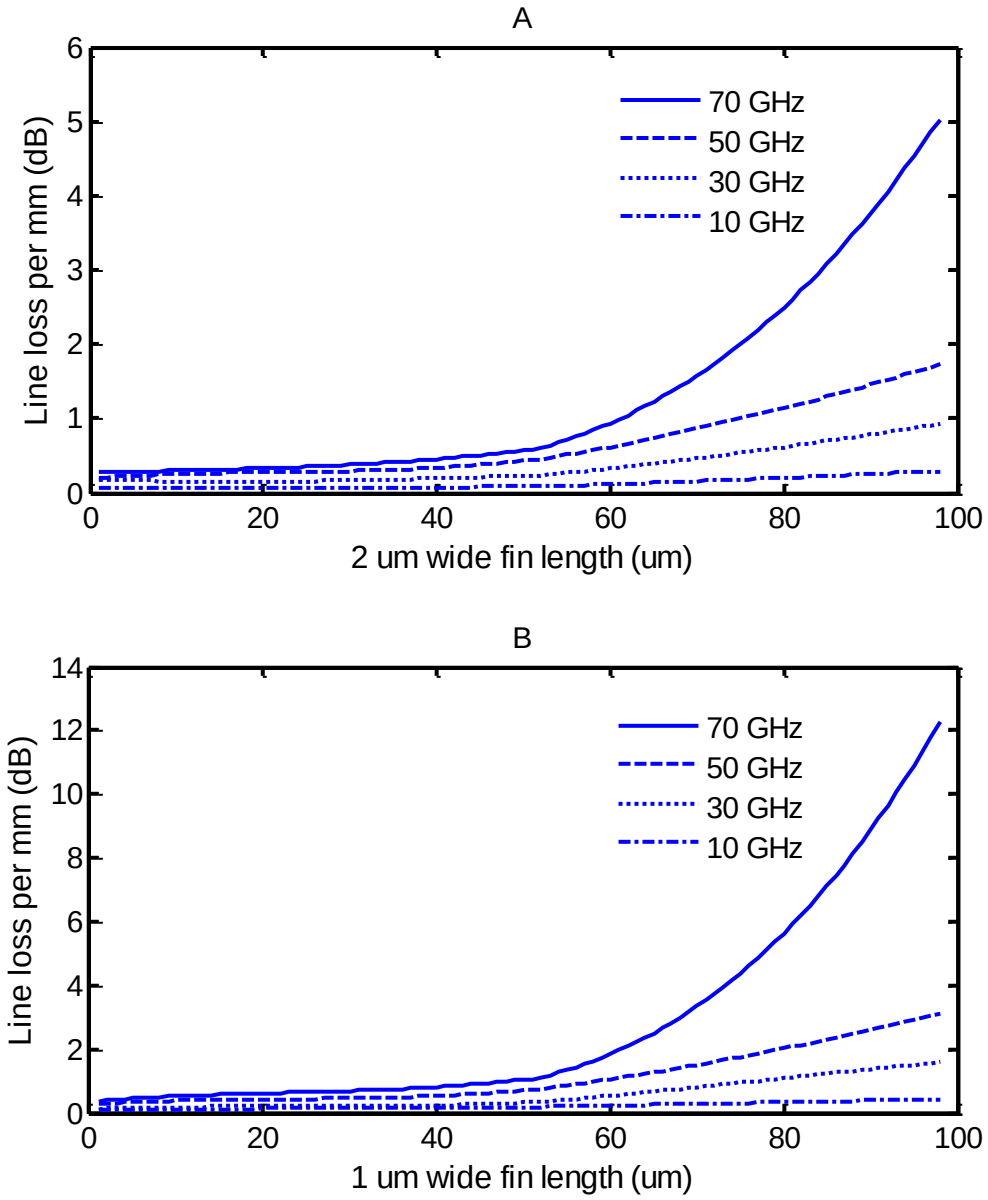

Figure 3.36 Transmission line loss, A when 1 μm are used, B when 2 μm wide fins

It can be seen that as the frequency and the lengths of the fins increase, the electrode loss begins to rise dramatically. In particular, when the length of the fins exceeds 50 μm, the electrode loss becomes very significant. Moreover, the electrode loss in the 1 μm wide fins is much greater

than in the 2 μm wide fins. For example, at 50 GHz, when the length of the fins are 80 μm, the electrode loss in the 1 μm wide fins and the 2 μm wide fins are ~ 4 dB/mm and ~ 2 dB/mm respectively.

We did not simulate any ITFs that were entirely loaded with 1 μm wide fins due to computing power limitations. Simulating ITF with 1 μm wide fins typically requires 30 GB of RAM. Our computer has an Intel® i7 2.93 GHz CPU (this CPU supports eight parallel computing threads) and 12 GB of RAM. When running a simulation that requires more RAM than the computer has, the computer must constantly transfer information back and forth between the RAM and the hard disk, i.e., there is a large amount of memory swapping. This increases the simulation time dramatically. Given the SONNET computing licence that we have (a single desktop high performance solver licence, which supports up to eight parallel threads), we estimate that it takes at least two days for the EM analysis engine to simulate the structure at one frequency. SONNET typically analyzes the structure at around 50 different frequency locations between 1 and 100 GHz. This means that simulating an ITF that is entirely loaded with 1 μm wide fins could take up to four months. In comparison, simulating a 2 mm long ITF loaded with 2 μm wide fins takes one week.

Although using narrower fins allows the structure to reach lower impedance values, the amount of conductor loss at high frequencies limits the operating bandwidth of the ITF. In order to minimize electrode loss due to the fins above 40 GHz, the designer can employ thinner types of fins only when matching to impedance values that require the use of thinner fins. For example, according to Table 3.2, when matching 10.17 Ω to 229.1 Ω in W+2G = 260 μm structures, tapered CPW sections are used for impedance values from 24.48 Ω to 229.1 Ω, 4 μm wide fin sections are used from 19 Ω to 24.48 Ω, 2 μm wide fin sections are used from 14.12 Ω to 19 Ω, and 1 μm wide fin sections are used from 10.17 Ω to 14.12 Ω. This design approach employs the

connection of different kinds of fin sections and regular CPW sections. We will examine the behaviour of such connections in the following section.

3.13 Mixing Various Types of Fins with Regular CPW Sections

In the following set of simulations, we mixed various types of fin sections and CPW sections to form transmission lines. These transmission line sections are designed to represent the same impedance value on a 650 μm thick GaAs substrate. The electrodes are assumed to be lossless. Figure 3.37 shows a transmission line made by connecting regular CPW sections with 4 μm wide fin sections, in which W+2G = 170 μm. All sections of the line are designed to have an impedance of 26 Ω. The transmission line is terminated with two 26 Ω ports. The entire structure is 0.3 mm long. The device characteristics of this structure are shown in Figure 3.38.

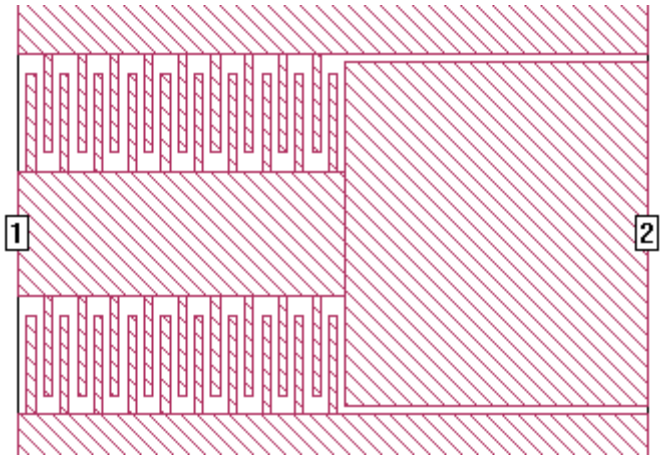

Figure 3.37 26 Ω transmission line made by mixing regular CPW sections and 4 μm wide fin sections

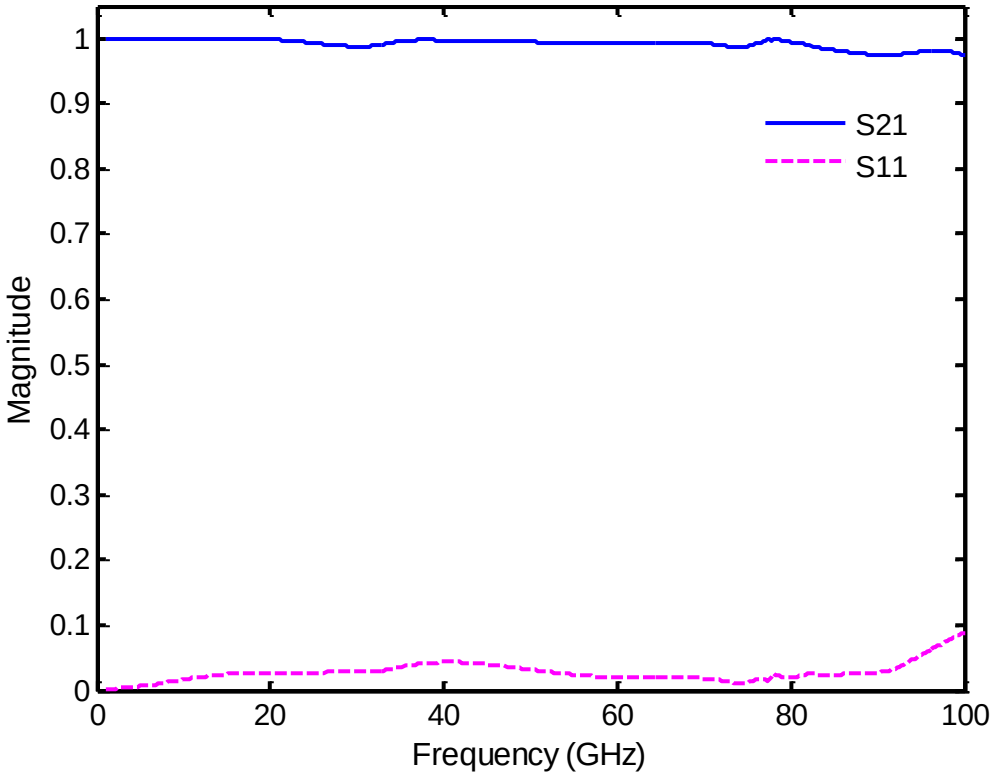

Figure 3.38 Device characteristics of the 26 Ω transmission line

It can be seen that the overall S21 level stays around 1 over the entire simulated frequency range. This indicates that connecting regular CPW sections to fin sections that representing the same impedance value form well behaved transmission lines.

In another simulation, using the same substrate and lossless electrodes, 2 μm wide fin sections are mixed with 4 μm wide fin sections, in which W+2G=170 μm. All impedance sections are designed to have impedance value of 22.5 Ω. The transmission line is terminated with two 22.5 Ω ports. This transmission line is illustrated in Figure 3.39. The entire device is configured to be 0.3 mm long. As expected, the overall S21 level stays around 1 across the entire simulated frequency range, as shown in Figure 3.40.

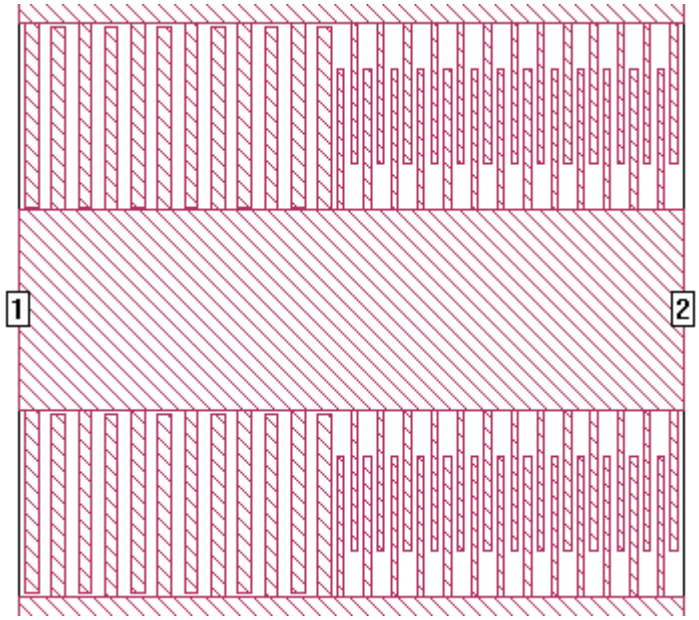

Figure 3.39 22.5 Ω transmission line made by mixing 2 μm wide fin sections and 4 μm wide fin sections

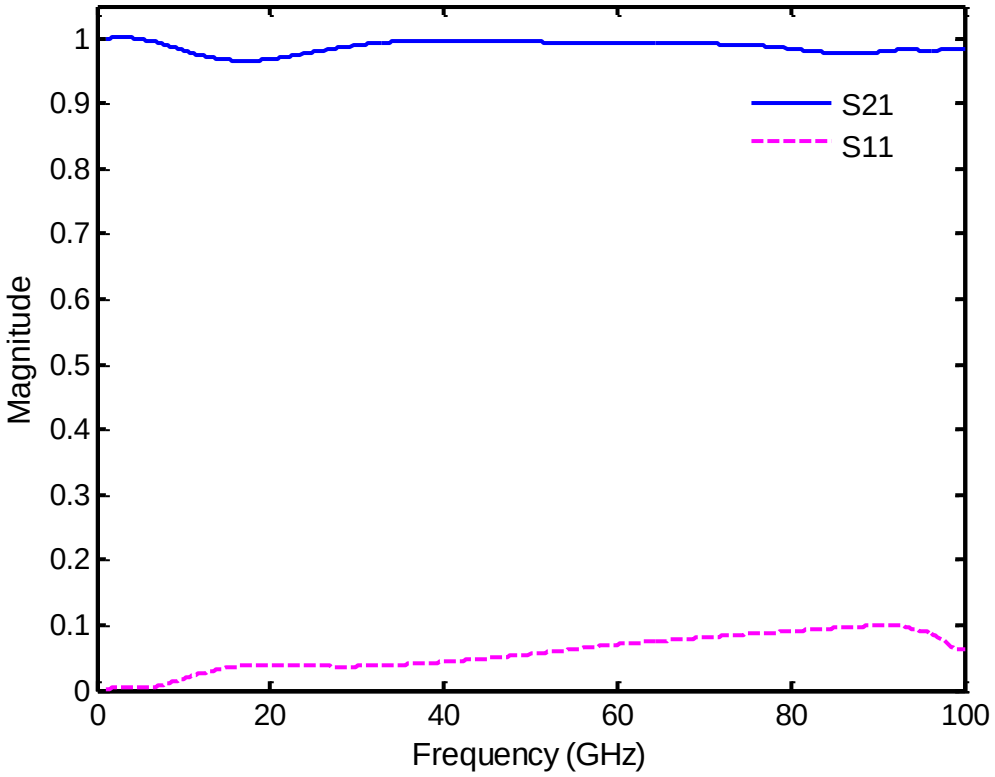

Figure 3.40 Device characteristics of the 22.5 Ω transmission line

In general, when different types of transmission line sections (with fins or without fins) that have the same impedance values are connected together, the overall S21 levels stay around 1 from 1 to 100 GHz. From a purely simulation point of view, we did not observe any noticeable discontinuities that are introduced by connecting different types of transmission line sections. In the following section, we utilize different types of transmission line sections to design impedance transformers.

3.14 Design ITFmix

As previously stated, narrower fins allow the impedance transformer to match impedances as low as 10 Ω. However, the electrode loss in the fins severely degrades the performance of the impedance transformer. In order to reduce the amount of conductor loss in the ITF, we have designed a new type of ITF utilizing different sizes of fins, called the ITFmix. The concept of ITFmix is as follows: when matching from high impedance to low impedance, the ITFmix first uses tapered CPW sections; if the impedance value along the line is lower than the lowest impedance value that can be matched by a CPW taper, fin sections are added; transmission line sections loaded with the next thinner size of fins are used only when matching to impedance values that require the use of thinner fins. This design approach minimizes the total length of the fin sections that are used and reduces the unnecessary use of thinner fins. As a result, the overall electrode loss is lowered and the high frequency response of the device can be improved.

The following simulation demonstrates an ITFmix matching 12.6 Ω to 100.5 Ω on a 650 μm thick GaAs substrate. The device is 2 mm long, in which W+2G is 170 μm. The electrodes are 1 μm thick gold. Tapered CPW sections are used to cover the impedance range from 24 Ω to 100.5 Ω. Here, 2 μm wide fin sections are used from 17.2 Ω to 24 Ω, and at the low impedance end of the device 1 μm wide fin sections are used from 12.6 Ω to 17.2 Ω. The device is illustrated in Figure 3.41 and Figure 3.42.

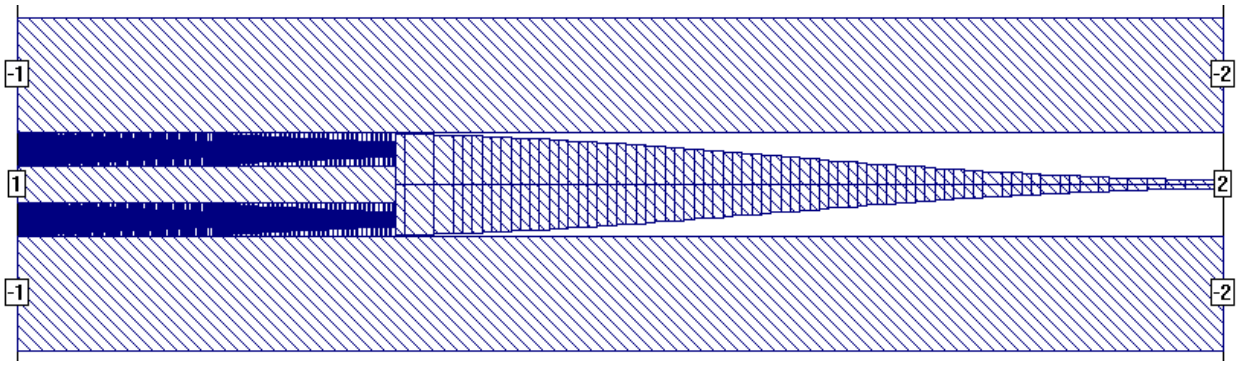

Figure 3.41 ITFmix matching from 12.6 Ω to 100.5 Ω

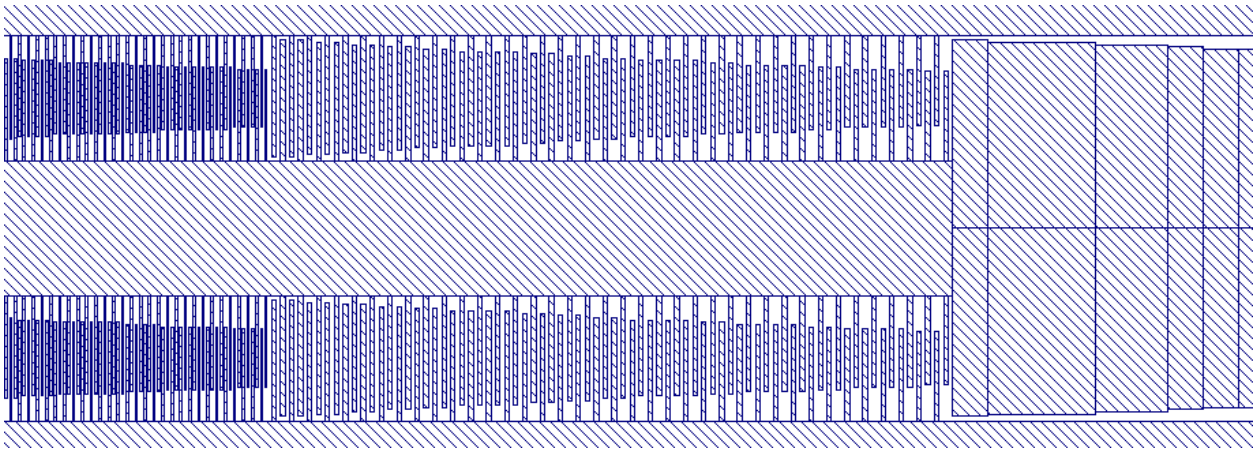

Figure 3.42 Detail of ITFmix using 1 μm wide fin sections, 2 μm wide fin sections and tapered CPW sections

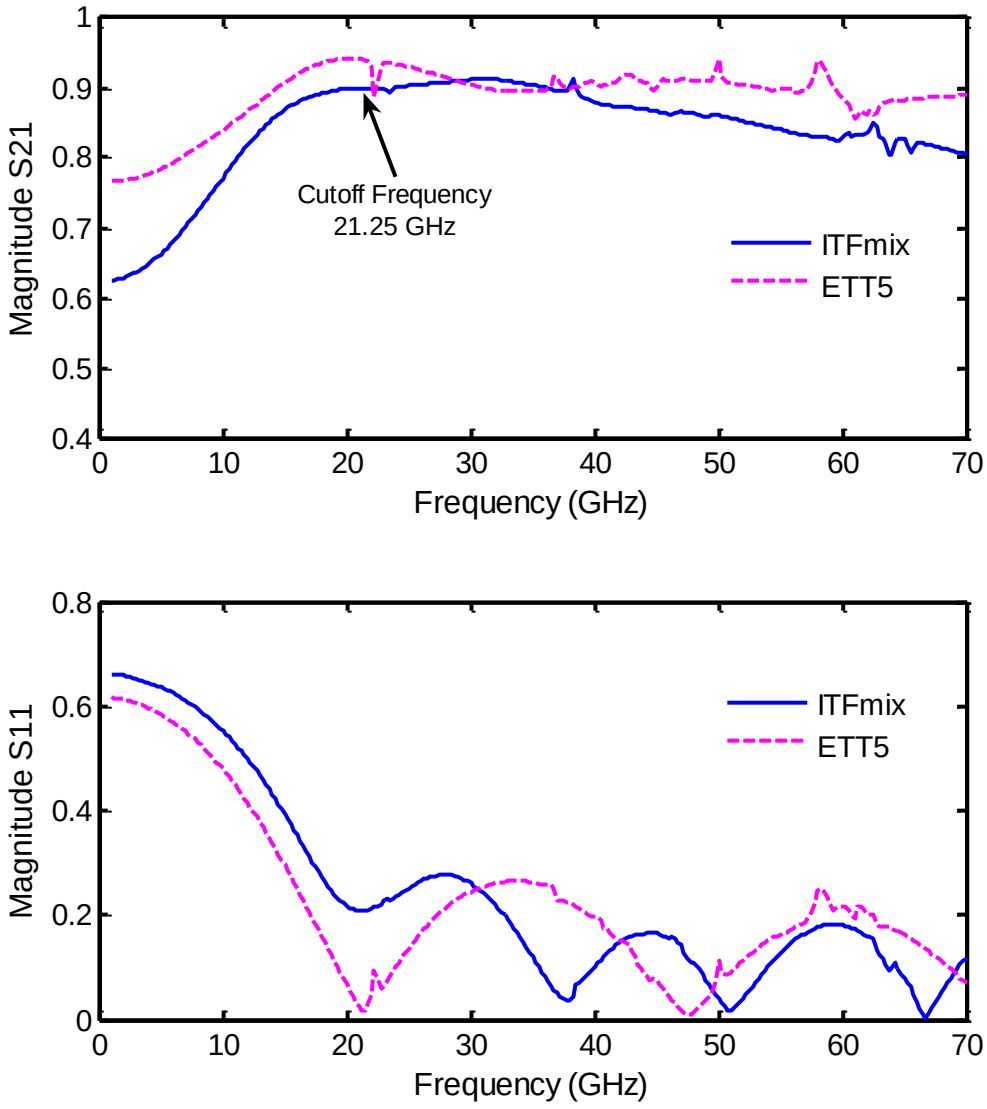

Figure 3.43 Device characteristics of ITFmix and ETT5

The device characteristics of this ITFmix are compared with those of ETT5 (ETT5 is a 2.25 mm long exponentially tapered impedance transformer, matching 24 Ω to 100.5 Ω) in Figure 3.43. As shown in the plot, the cutoff frequency of each device is about 21.25 GHz. The S21 level of ITFmix shows a similar level of performance as that of ETT5 from 21.25 GHz to 40

GHz. As frequency rises above 40 GHz, ITFmix suffers from slightly higher electrode loss in the fins. However, due to the use of various sizes of fins to extend the lower impedance matching range, the overall S21 level of ITFmix stays above 0.8 from 21.25 GHz to 70 GHz. This makes the ITFmix a wideband impedance transformer. Beyond the cutoff frequency, the overall S11 level of ITFmix is slightly lower than that of ETT5. Most importantly, ITFmix is able to match down to 12.5 Ω and is 0.25 mm shorter than ETT5. This shows the advantages of using ITFmix as compared to regular ETT. Following this design approach, impedance transformers capable of matching ~10.17 Ω to ~ 229.1 Ω can be realized.

3.15 Summary

In this chapter we presented the simulation results of many analyzed structures. When the impedance map is generated for a particular W+2G dimension, we can build well behaved transmission lines and tapered impedance transformers that match the impedances of the source and the load. We have found that the SONNET box walls can be positioned 1000 μm away from the outer edges of the tested structure to reduce their interaction with the device. As the length of the impedance transformer increases, electrode loss increases and potential longitudinal resonances occur. The optimum thickness of the gold layer is determined to be 1 μm to minimize electrode loss.

The method we used to generate the impedance map for the fin sections is presented. We have shown that properly designed ITFs can outperform conventional tapered impedance transformers. With the use of capacitive loading fins, the lowest impedance value that can be reached is extended from ~ 24 Ω to ~ 10.17 Ω. Hybrid ITFs have an impedance matching range from ~10.17 Ω to ~ 229.1 Ω. The overall effective microwave index of the device is

increased due to the slowing effect introduced by the fins. This allows us to design ITFs that have similar device characteristics (i.e., the same cutoff frequency, similar S21 and S11 levels) as those of regular tapered impedance transformers but of shorter device lengths. Hence, on-chip real-estate savings can be achieved. In addition, we analyzed the electrode loss of various types of fins. Finally, we introduced the ITFmix, which uses thinner fins only when matching to impedance values that require the use of thinner fins. This design approach is able to enhance the operating bandwidths of the impedance transformers. We have demonstrated that ITFs are capable of matching ~10 Ω to ~ 229 Ω on 650 μm thick GaAs substrates up to at least 70 GHz.

Chapter 4

Summary, Conclusion, and Suggestions for Future Work

4.1 Summary

In this thesis we focused on designing coplanar waveguide based impedance transformers for matching the input impedances of millimeter wave electronic components. The goal was to achieve the widest possible impedance matching ranges and operating bandwidths. In Chapter 2, we presented the basic design guidelines to build coplanar waveguides so that our devices support the coplanar mode and suppress other unwanted modes. We explored the theoretical models of various types of conventional impedance transformers and found that by increasing the effective microwave index and the length of the device, we could widen the operating bandwidths of the impedance transformers. In addition, we reviewed the concept of slow-wave electrodes and proposed to incorporate capacitive loading fins in the CPW line to design impedance transformers.

In Chapter 3, simulation results of different test structures are presented. The methods that we used to generate impedance maps were introduced. We simulated coplanar waveguides that were matched and mismatched to the ports. We analyzed exponentially tapered impedance transformers of different lengths. The optimum width of the SONNET box was determined in order to reduce the interaction between the test structures and the box walls. We analyzed several ITF structures and showed that the cutoff frequencies of the impedance transformers were significantly decreased with the use of capacitive loading fins. The impedance matching ranges and the electrode loss of various types of fin sections were explored. Finally, we proposed using ITFmix structures to extend the lower impedance matching ranges and to enhance the operating

bandwidths of the impedance transformers. We have demonstrated that ITFs are capable of matching ~10 Ω to ~ 229 Ω on 650 μm thick GaAs substrates up to at least 70 GHz.

4.2 Conclusion

Impedance transformers loaded with capacitive loading fins and suitable for high frequency broadband impedance matching are presented. By adding and reducing the amount of capacitance introduced by the interdigitated fins, we can precisely control the impedance and the effective microwave index of the transmission line. We have shown that one can use interdigitated capacitive loading fins in CPW to significantly increase n_{eff}, and thereby reduce the length of the impedance transformer, lower the minimum impedance that can be matched, and significantly lower the cutoff frequencies. Compared to regular tapered impedance transformers, ITFs can achieve similar device characteristics with shorter electrode lengths, which saves on-chip real-estate.

In order to reduce electrode loss, we designed ITFmix structures that use different types of fins to extend the lower impedance matching range. ITFmix structures only employ thinner fins when it matches impedance values that require the use of thinner fins. This design approach is able to extend the lower impedance matching range of the impedance transformer and maximize the operating bandwidth of the device.

The ITF design approach can be applied to other types of impedance transformers, such as triangularly tapered transformers and Klopfenstein tapered transformers, to extend their impedance matching ranges and to save on-chip real-estate.

4.3 Suggestions for Future Work

In this thesis, we focused on using impedance transformers to match real impedances. In many practical situations, one has to deal with impedance values that have reactive components. Thus, techniques that utilize the slow-wave design approach to match complex impedance values should be explored in the future. Also, it is possible to build theoretical models that describe the behavior of ITFs. Given a particular design criteria, one can derive the optimum device length and the suitable amount of fin capacitance that should be used to achieve the greatest amount of real-estate saving. In addition, one can fabricate some CPW and ITF structures and measure their device characteristics to verify the simulation results presented in this thesis.

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